INTERFACE REFERENCE MANUAL

DATA MACHINES, INC.

A Division of Decision Control, Inc.

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GENERAL DESCRIPTION

1.1 INTRODUCTION

The DATA 620 Computer is a high-speed, parallel binary computer. Its extensive instruction repertoire, flexible input/output, and modular packaging make it ideally suited for application as a general-purpose machine or as an on-line system component.

Its features include:

- Fast operation	1.8-microsecond memory cycle
- Large instruction repertoire	107 standard, with over 200 micro-instructions, plus 23 optional
- Expandable word length	16- or 18-bit configurations
- Modular memory	4096 words standard, 32,768 maximum
- Multiple addressing modes	Six, including direct, indirect, relative, index, immediate and extended (optional).
- Flexible I/O	64 device addresses on standard I/O Bus; optional interlaced input/output and direct memory access
- Extensive software	All programming and diagnostic aids required for efficient system use
- Modular packaging	Convenient book rack drawer contains main processor; peripheral controllers are mounted in slide drawers.

The DATA 620 is simple in design and is easy to program, operate, and maintain. As a system component, it is easily integrated with other equipments through the use of standard or special peripheral interface elements. The Central Processor and its associated power supplies and peripheral controllers all mount in standard 19-inch equipment cabinets and require no special cabling or air conditioning facilities.

1.2 PURPOSE OF THIS MANUAL

This manual provides basic circuits and logic design, and timing information on the standard and optional input/output facilities of the DATA 620 Computer, plus design examples for several I/O

functions. Using this information, the system designer may integrate the computer with special interfaces tailored to specific system requirements.

This manual also contains information on cabling, grounding, and installation procedures and thus serves as a basic document for system planning purposes.

While a detailed knowledge of the internal computer is not essential for successful interface design, it is recommended that the system designer have a general familiarity with the computer organization and operation. The available documents for the DATA 620 are summarized in Table 1-1. The reference manuals for the standard peripheral controllers will be particularly useful for design examples.

Table 1-1
DATA 620 DOCUMENTS

DMI PUBLICATION NUMBER	TITLE
S-2000- XXXX	Systems Reference Manual
S-2001- XXXX	Interface Reference Manual
S-2002- XXXX	Programmer Reference Manual
S-2003- XXXX	FORTRAN Manual
F-2002- XXXX	Subroutine Manual
F-2001- XXXX	Maintenance Manual
F-2004- XXXX	ASR-33 Teletype Controller Reference Manual
F-2005- XXXX	Buffer Interlace Controller Reference Manual
F-2006- XXXX	Magnetic Tape Controller Reference Manual
F-2007- XXXX	600 LPM Line Printer Reference Manual
F-2008- XXXX	300 LPM Line Printer Reference Manual
F-2009- XXXX	Paper Tape System Controller Reference Manual
F-2010- XXXX	100 CPM Card Reader Reference Manual
F-2011- XXXX	Priority Interrupt Reference Manual

1.3 COMPUTER ORGANIZATION

The overall organization and basic information paths of the DATA 620 Computer are shown in Figure 1-1. The basic system is composed of the following functional elements: Memory Section, Control Section, Arithmetic/Logic Section, Operational Register Section, and Input/Output Section. An optional input/output facility, Direct Memory Access, is also available.

1.3.1 Memory Section

Memory modules are independent, each with separate address and data registers and internal control and timing. Minimum memory size is 4096 words. Total memory may be 4096, 8192, 16,384, or 32,768 words. These modules are added to the M Bus on a plug-in basis by standard cables and connectors.

1.3.2 Control Section

The control section decodes the program instructions into timing and control signals for the entire machine. There are 107 standard instructions decoded; an additional 24 instructions may be supplied as options. Over 200 micro-coded instructions may be derived from the standard instruction set.

1.3.3 Arithmetic/Logic Section

This section contains the gating elements required to perform all programmed arithmetic and logic operations. It is also used for internal control operations such as instruction and operand address modification.

1.3.4 Operational Register Section

Operational registers include the A, B, X, and P Registers. A and B form a double-length register for arithmetic and logical operations. The B Register may also be used for indexed addressing. The X Register is a full 16-bit hardware index register. Indexed addressing using B or X requires no additional time for execution of the instruction. Registers A and B may also be used for direct input/output transfers. The instruction counter, P, holds the memory address of the instruction being executed by the control sections. The S Bus provides routing of these registers to the Arithmetic Unit.

1.3.5 Input/Output Section

This section provides transmission of control and data signals to and from peripheral devices attached to the I/O Cable. A total of 64 peripheral device addresses are available. External program sense and interrupt functions are also transferred to and from the Control Section through the I/O Section. Data transfers may be single-word (program controlled) or block (using the optional Buffer Interlace Controller).

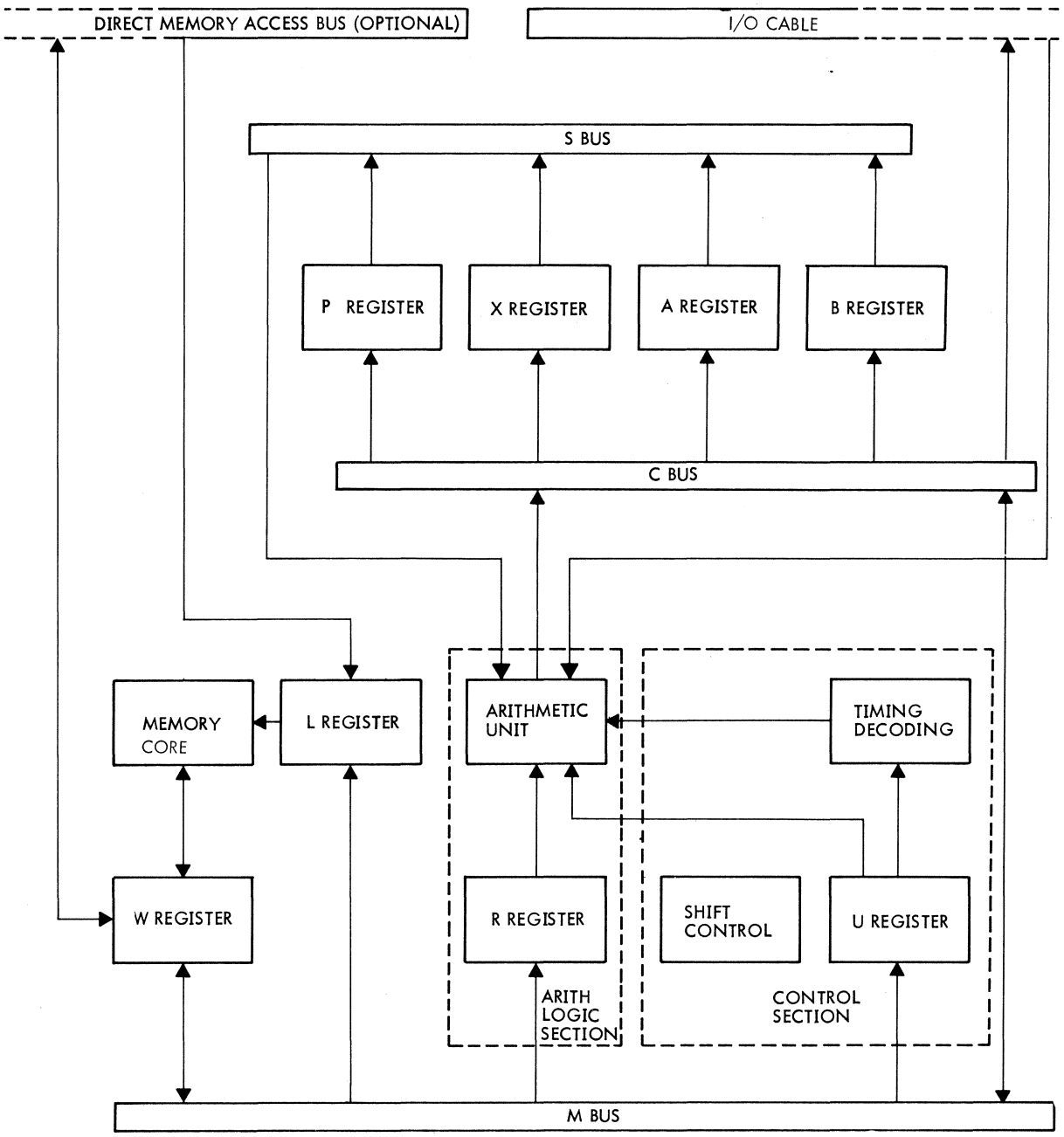

Fig. 1-1 DATA 620 Organization

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1.3.6 Direct Memory Access (DMA)

This optional facility provides a high-speed priority data path between memory and any set of peripheral devices attached to its D Cable. The DMA permits input/output transfers to be completely overlapped with program operations when they occur in separate memory modules.

SECTION II
DATA 620 STANDARD INPUT/OUTPUT SYSTEM

2.1 ORGANIZATION

As shown in Figure 1-1, the I/O Section of the computer communicates with the operational registers and the memory through the C Bus. Data and control signals are transmitted to and from external peripheral devices through the I/O Cable.

2.1.1 Overall Operation

The overall organization of the DATA 620 I/O System, including a typical set of peripheral devices, is shown in Figure 2-1. Standard or special peripheral devices are in parallel on the I/O Bus. Any number of logical devices, up to a total of 64, may be added. The following types of information transfers between the Central Processor and the external devices through the I/O Bus may be executed:

External control. An external control code is transmitted under program control from the Central Processor to a device.

Program sense. The Central Processor can sense the status of a selected external line under program control.

Single word transfer to/from the A and B Registers. A single word may be transferred to or from the A and B Registers under program control.

Single word transfer to/from memory. A single word may be transferred to or from any memory location under program control.

Program interrupt. An external device may force the Central Processor to execute an instruction in a specified location in the memory.

Buffer Interlace Controller (BIC) transfer to/from memory. Blocks of words may be transferred to or from sequential memory locations under control of an optional Buffer Interlace Controller. Devices controlled by the BIC may also be operated under program control (single word transfers).

Interlace data transfers. Single words may be transferred to/from memory by the control signals available on the I/O Cable. Buffer Interlace Controllers use the lines for performing interlaced data transfers.

2.1.2 I/O Cable

A typical functional organization of peripheral devices on the I/O Cable is shown in Figure 2-2. The I/O Cable consists of the E Bus plus a set of control lines. The E Bus contains 16 (or 18) pairs

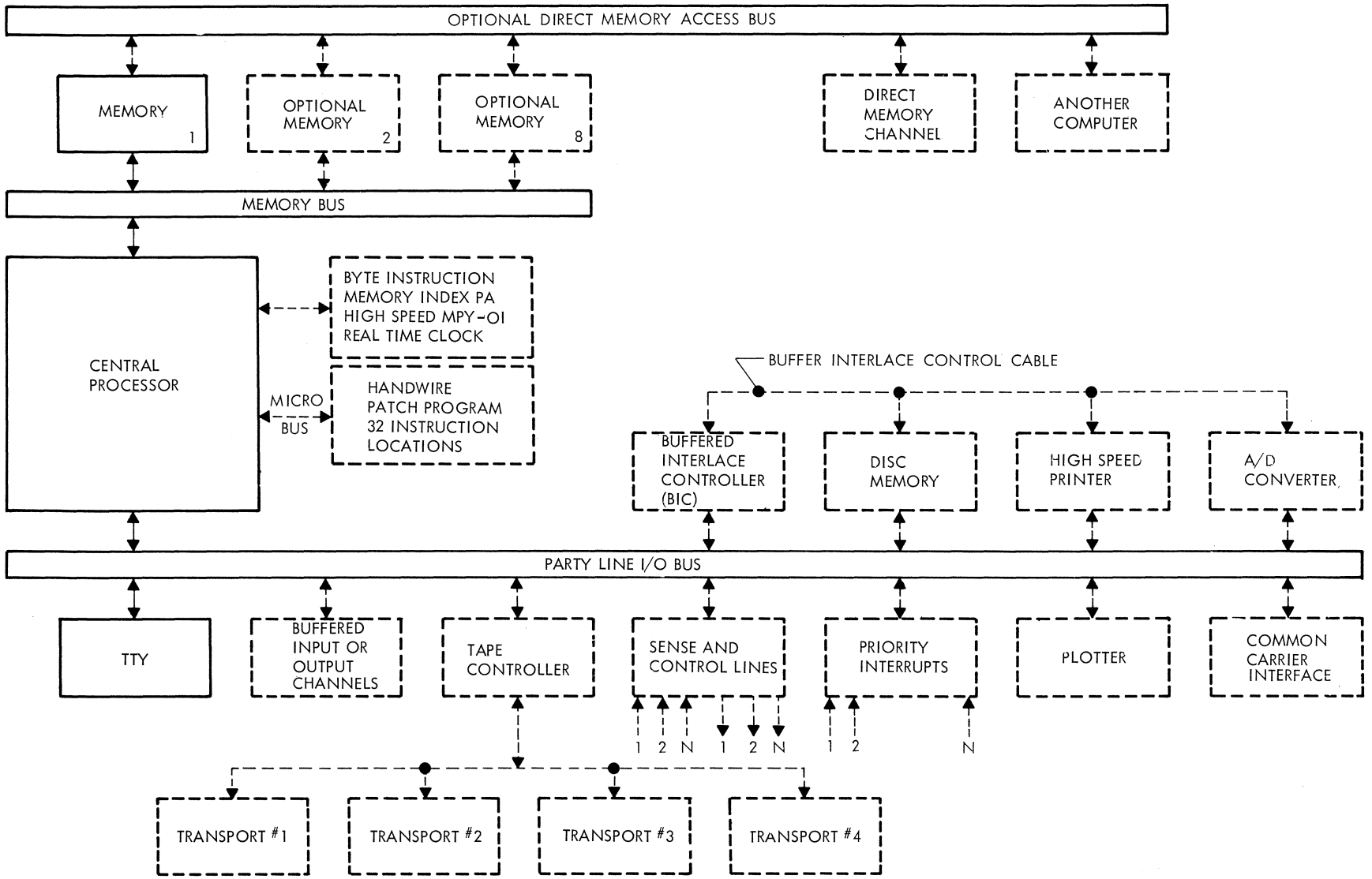

Fig. 2-1 DATA 620 I/O System Organization

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of bi-directional lines which transmit control codes, addresses, and data between the Central Processor and the peripheral devices connected in parallel to the cable. The 12 I/O control lines transmit timing signals to and from the Central Processor to synchronize the information transfers over the E Bus. Most interfaces designed use four of the 12 lines.

Information transfers with the DATA 620 are synchronized by peripheral controllers; these controllers may, in turn, control one or more peripheral devices. The Central Processor can communicate directly with all peripheral controllers under program control. It may determine when a device is ready to send or receive information by sensing associated sense lines, or it may be notified by means of a program interrupt. All standard peripheral controllers contain the necessary sense and external control functions for proper operation.

Priority Interrupt and Sense Line modules are available for use for special systems interfacing.

Where block transfers of data independent of program control are required (such as from tapes, drums, commutators, etc.), the Buffer Interlace Controller may be provided. This element contains hardware registers which automatically generate the proper memory addresses for successive data transfers with the DATA 620 memory and a device through its controller.

2.1.3 Input/Output Operations

All I/O operations are either one or two phase; Sense and External Control are single-phase while Data Transfers and Trap Transfers* are two-phase. Each phase is terminated with a control pulse. During information transfers over the I/O Bus, the E lines may carry control codes, addresses, or data, depending on which type of operation is being performed. The control signals defining the type of operation are listed in Table 2-1. Table 2-2 summarizes the information carried on the E Bus for the specified operations. The timing signals present on the I/O control lines during each operation are also indicated.

When a control code is on the E Bus (first phase), lines EB11-EB15 carry a control signal which defines the operation. The control codes transmitted over the E Bus are summarized in Table 2-3. The Function Ready (FRYX-I) pulse is generated to indicate that a control code is on the E Bus.

2.1.4 Input/Output Section Logic and Connector

The logical organization of the DATA 620 I/O Section and layout of the standard I/O connector are illustrated in Figure 2-3 and detailed in Table 2-4. E Bus outputs from the computer are transmitted by a set of line driver circuits; these signals are gated through drivers by the internally generated E Bus Drive signal (EBDX+). E Bus inputs to the computer are gated through the E Bus Receivers by the internally generated E Bus Receive signal (EBRX+). The I/O drivers and receivers are not gated.

The computer and each I/O logic drawer have two identical connectors wired in parallel. Any internal signals required are jumpered from one of the connectors to the logic. The second connector is normally for the I/O Cable to the next I/O logic drawer. In the case of the last device on the I/O Bus, the second connector has a termination "shoe" inserted. This "shoe" contains terminating resistors

*Trap operation is used for buffered input/output operations, such as those performed by the standard Buffer Interlace Controller. Special interface designs also may take advantage of the trap facilities of the computer.

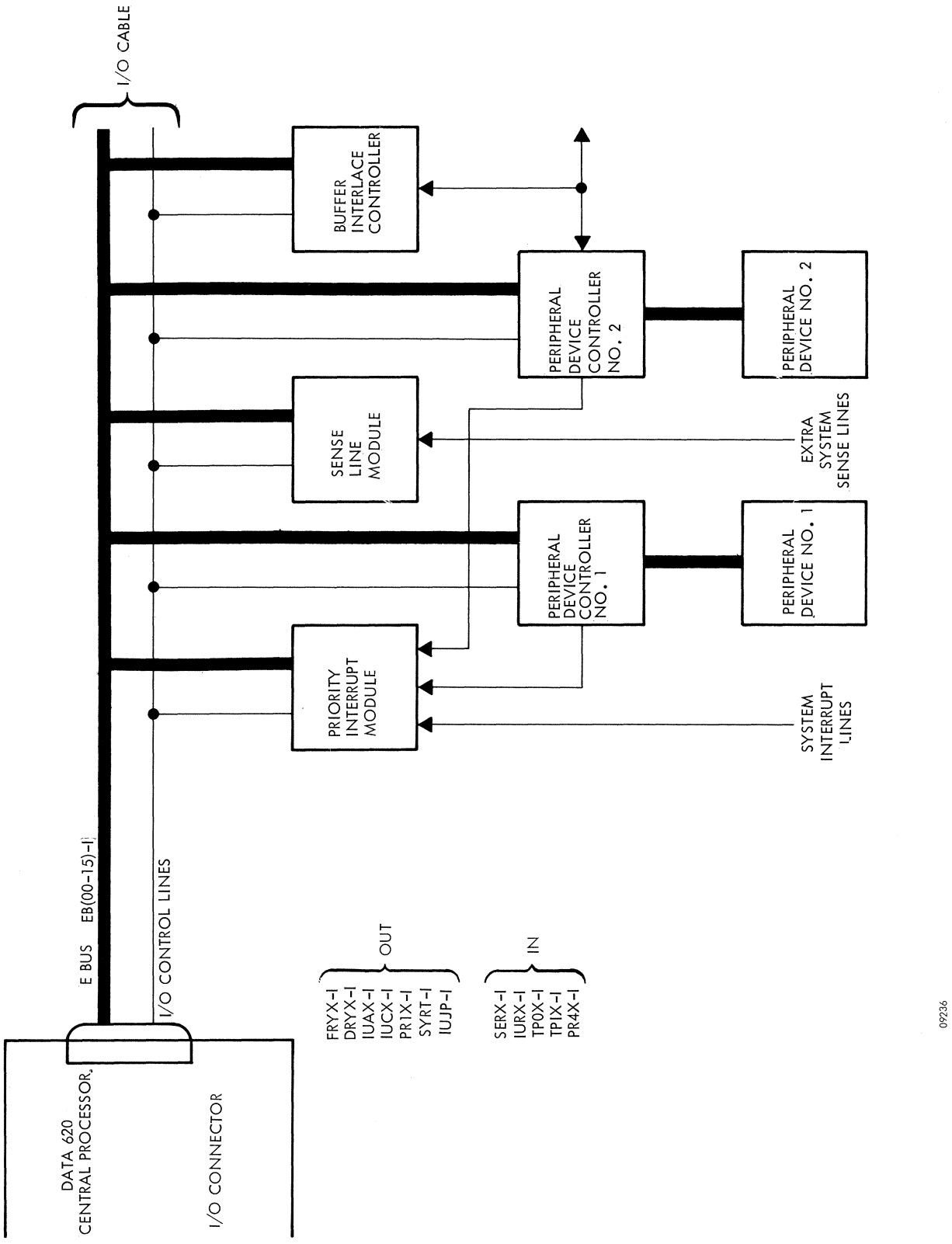

Fig. 2-2 DATA 620 Standard I/O System, Functional Diagram

Table 2-1
I/O CONTROL LINE SIGNALS

CONTROL LINE	SYMBOL	FUNCTION
Function Ready	FRYX-I	Indicates that the E Bus contains address information. The type of address depends upon the state of IUAX-I: IUAX-I = TRUE: A memory address is on the E Bus from an Interrupt or BIC module. IUAX-I = FALSE: A device address, possibly with an associated function code, is on the E Bus from the DATA 620.
Data Ready	DRYX-I	Indicates that the E Bus contains data.
Sense Response	SERX-I	Indicates logical state of line designated by sense line address on E Bus.
Interrupt Request	IURX-I	Indicates a demand from the Interrupt module to force program to execute one instruction at the location specified by address on E. Bus. This address will be placed on E Bus when IUAX-I becomes TRUE.
Interrupt Acknowledge	IUAX-I	Indicates that external interrupt demand is being acknowledged. Address is placed on E Bus and removed at FRYX-I.
Trap Output	TPØX-I	Indicates that a Buffer Interlace Controller (or equivalent) is requesting a data transfer from memory.
Trap Input	TPIX-I	Indicates that a Buffer Interlace Controller (or equivalent) is requesting a data transfer to memory.
Interrupt Clock	IUCX-I	A 1.1-mc clock. Clock is OFF when IUAX-I is TRUE.
Priority Out	PRIX-I	Priority line used with Interrupt and Buffer Interlace Controller modules for priority determination.

Table 2-1 (cont'd)
I/O CONTROL LINE SIGNALS

CONTROL LINE	SIGNAL	FUNCTION
Priority In	PR4X-I	Priority line returned to computer to permit console interrupt.
Priority 2 and 3	PR(N)X-I	Intermediate priority lines that are used on the I/O Bus allowing flexible priority assignments.
Interrupt Jump	IUJP-I	Indicates that a Jump-and-Mark instruction is being executed for an Interrupt Request.
System Reset	SYRT-I	Line which becomes TRUE when the SYSTEM RESET button on the control console is pressed. Used to initialize each controller connected to the I/O Cable.

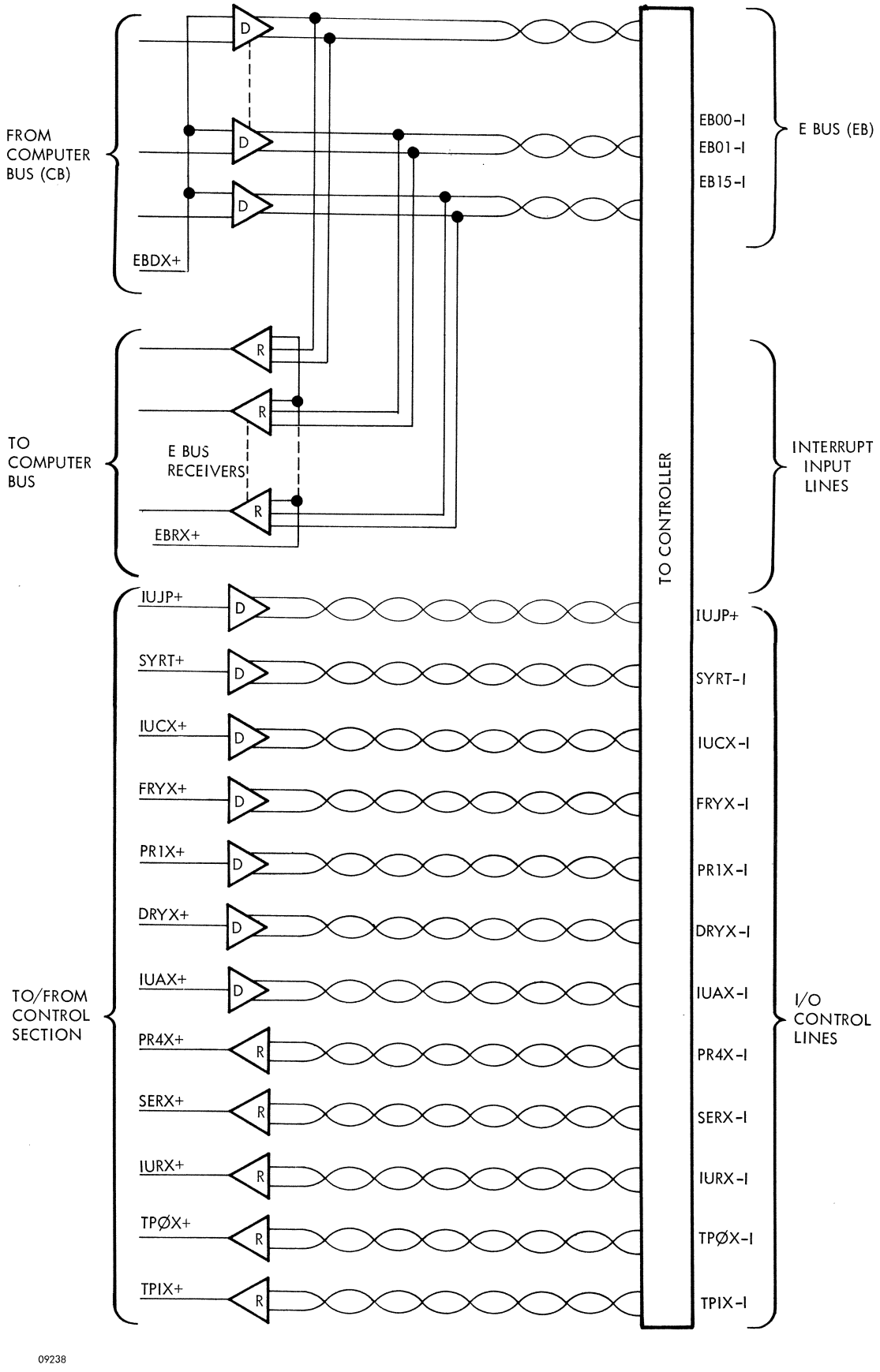

Fig. 2-3 DATA 620 I/O Section and Standard Connections

Table 2-2
E BUS AND I/O CONTROL SIGNALS

	OPERATION						
	External Control	Sense	Data Transfer (Single Word I/O)		Trap Sequence (Buffer Interlace Control)		Interrupt Sequence
					TPOX-1 or TPIX-1		
Control Lines	FRYX-1* (Phase 1)	FRYX-1* SERX-1* (Phase 1)	FRYX-1* (Phase 1)	DRYX-1 (Phase 2)	IUAX-1, FRYX-1 (Phase 1)	IUAX-1, DRYX-1 (Phase 2)	IURX-1 IUAX-1 (Phase 1)
EB00-1 to EB05	Device Address	Device Address	Device Address	Data being Trans-fered In or Out	Memory Address In	Data In or Out	Use lines 01-15 for interrupt location by pairs.
EB06-1 to EB08-1	Function Code	Function Code	Not Used				
EB09-1 EB10-1	Not Used	Not Used	Not Used				
EB11-1	External Control Command						
EB12-1		Sense Command					
EB13-1			Data Transfer In				
EB14-1			Data Transfer Out				
EB15-1							

E Bus Meaning

*IUAX Interlock - used in the address decoding term.

Table 2-3
SUMMARY E BUS SIGNALS

OPERATION	EB15-I	EB14-I	EB13-I	EB12-I	EB11-I	EB10-I, EB09-I	EB08-I	EB07-I	EB06-I	EB05-I to EB00-I
Output from Memory							0	0	0	
Output from A Register		1	0	0	0	Unused	Note 1	0	1	Device Address ($00-63_{10}$)
Output from B Register							Note 1	1	0	
Input to Memory							0	0	0	
Input to A Register		0	1	0	0	Unused	Note 1	0	1	Device Address ($00-63_{10}$)
Input to B Register							Note 1	1	0	
Sense State of External Device		0	0	1	0	Unused	Function Code			Device Address ($00-63_{10}$)
Send function code to External Device		0	0	0	1	Unused	Function Code			Device Address ($00-63_{10}$)

Note 1: If EB08-I is TRUE, selected register in computer is cleared.
If EB08-I is FALSE, selected register in computer is not cleared.
Bits EB06- to EB08- generally ignored I/O Controller, during Input or Output commands.

Table 2-4
I/O CONNECTOR PIN ASSIGNMENTS

PIN	FUNCTION
A	EB00-I
B	R
C	EB01-I
D	R
E	EB02-I
F	R
H	EB03-I
J	R
K	EB04-I
L	R
M	EB05-I
N	R
P	EB06-I
R	R
S	EB07-I
T	R
U	EB08-I
V	R
W	EB09-I
X	R
Y	EB10-I
Z	R
a	EB11-I
b	R
c	EB12-I
d	R
f	EB13-I
g	R
h	EB14-I
i	R
j	EB15-I
k	R
m	EB16-I
n	R

PIN	FUNCTION
p	EB17-I
q	R
r	
s	
t	IU15-I
u	R
v	IU14-I
w	R
x	IU13-I
y	R
z	IU12-I
AA	R
AB	IU11-I
AC	R
AD	IU10-I
AE	R
AF	IU09-I
AH	R
AJ	IU08-I
AK	R
AL	IU07-I
AM	R
AN	IU06-I
AP	R
AR	IU05-I
AS	R
AT	IU04-I
AU	R
AV	IU03-I
AW	R
AX	IU02-I
AY	R
AZ	IU01-I
BA	R

PIN	FUNCTION
BB	IU00-I
BC	R
BD	INRU-I
BE	R
BF	FRYX-I
BH	R
BJ	DRYX-I
BK	R
BL	SERX-I
BM	R
BN	IUCX-I
BP	R
BR	IUAX-I
BS	R
BT	TPIX-I
BU	R
BV	TPOX-I
BW	R
BX	PR1X-I
BY	R
BZ	PR2X-I
CA	R
CB	PR3X-I
CC	R
CD	PR4X-I
CE	R
CF	IUJP-I
CH	R
CJ	SYRT-I
CK	R
CL	IURX-I
CM	R
CN	AINX-I
CP	R
CR	-6V
CS	Gnd

to -4 volts. When adding an additional device to the system, the termination "shoe" is removed and installed on the second connector of the added device, with the interconnecting cable in its place.

2.1.5 Logic Levels

Logic levels for VersaLOGIC circuits are nominally 0 volt for a logic ZERO and -12 volts for a logic ONE. Over the I/O Cable, however, the sense of the logic signals is inverted and the voltage is changed. That is, binary "1's" are transmitted over the E Bus at the 0-volt level and binary "0's" are transmitted at the -6-volt level. Control lines rest at the -6-volt level; a control pulse is defined by the signal level rising to 0 volt for the prescribed time interval, and then returning to the -6-volt level. The standard Line Receivers convert the I/O Cable signals to 0 and -12 volts while the Line Drivers convert the 0- and -12-volt signals to the I/O Cable signals. One line of the twisted pair is terminated at each end by 100 ohms to -6 volts, with the other line grounded. The Line Driver acts as a switch across the pair to bring the potential difference between the lines to zero (indicating a logic "1"). When the driver is turned off, the voltage returns to -6 volts (indicating a logic "0"). The drivers are capable of supplying 100 ma of current. The receiver input impedance is 7.5k ohms. Up to 18 receivers may be added to any twisted pair, and up to 18 drivers may drive any twisted pair. Figure 2-4 shows one signal pair on the I/O Bus.

2.2 PROGRAM CONTROL FUNCTIONS

Interfacing functions fall into two major categories: programmed operations, and automatic operations. The programmed operations are: External Control (single bit out), Sense Operations (testing a single bit), Data Transfer In (full word inputs), and Data Transfer Out (full word outputs). The following paragraphs describe the programmed operations and examples of their use. The party line adapter is a special card for use in interfacing the programmed operations.

2.2.1 I/O Cable Adapter Card

The I/O Cable Adapter Card is a standard VersaLOGIC module (VL121) designed to facilitate interfacing with the DMI 620 I/O Cable (see Figure 2-5). Subsequent paragraphs show typical examples illustrating the use of the I/O Adapter. The organization of this card is such that many types of I/O interfaces may be simplified by its use. The address detection gates are used for forming the address; this also incorporates the IUAX-I signal for address lock-out during trap and interrupt sequences. The two flip-flops are used to implement the two-phase technique for I/O transfers (i.e., remember whether data is being transferred in or out). In some cases, one of the two flip-flops is used to implement a Buffer Ready function. The sense response driver (connected directly to the SERX-I line) has a logic inverter to allow direct OR'ing of many sense functions. The power driver is multipurpose.

The various uses of the I/O Cable Adapter Card are shown in paragraphs 2.2.2 through 2.2.5.

2.2.2 External Control Operation

External control operations are single-phase operations. The External Control Instructions (EXC XYY, where YY contains the device address and X contains the function code) transmits a Function Code and a Device Address on the E Bus for 900 nanoseconds (Figure 2-6). Functions EB00 through EB05

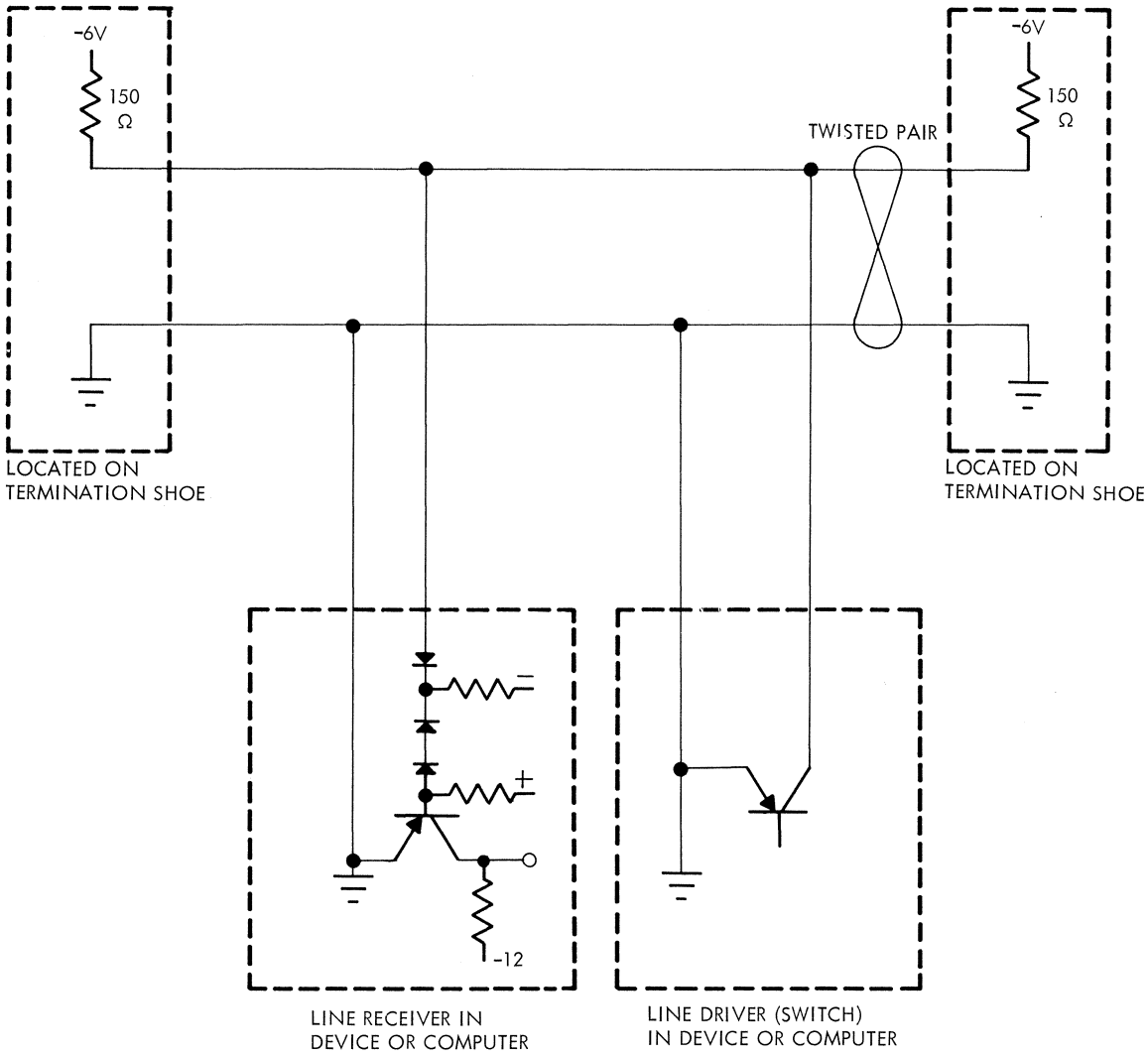

Fig. 2-4 Typical Line Location on I/O Bus

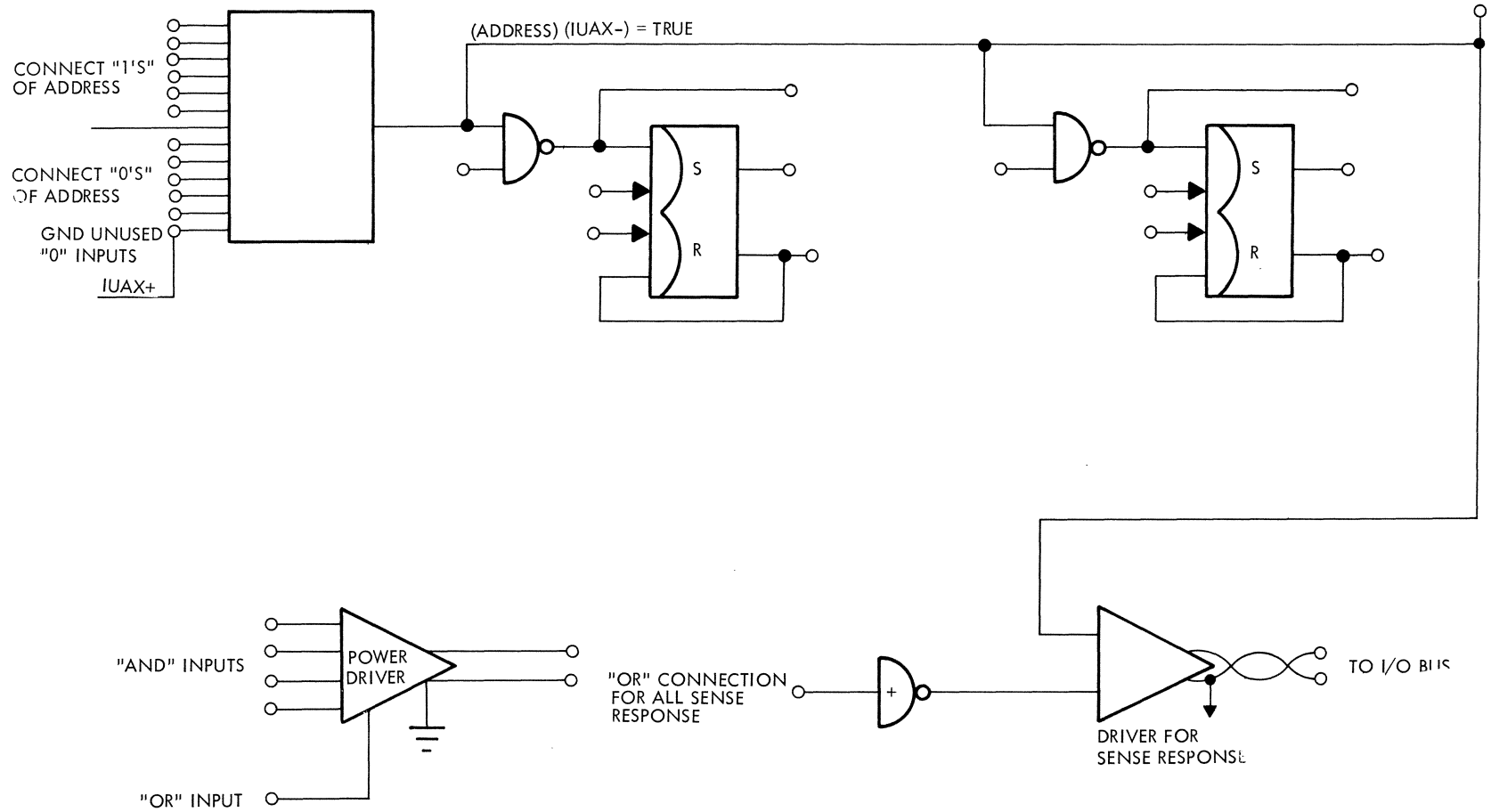

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Fig. 2-5 Functional Organization of I/O Cable Adapter Card (VL121)

contain a device address, and bits EB06-08 indicate the particular function code for that device. EB11 is true indicating that an External Control Function is being performed (see Table 2-3). The pulse FRYX+ is used with the address to form a 450-nsec pulse for setting and resetting flip-flops. The address overlaps FRYX+ by 100 nsec to allow for logic delays in forming the pulse signal in the power drivers.

An example of implementing eight external control lines is shown in Figure 2-7. This example requires four VersaLOGIC cards. As shown in Figure 2-7, only the meaningful I/O signals need be used to form the External Control function. The output of the select gate (EB06-08 describes one of eight) is a 450-nsec pulse (GND true).

2.2.3 Program Sense Function

Program Sense Functions are single-phase operations. The Sense instruction is a two-word instruction. The first word in the sense instruction contains the Function Code and Device Address which addresses a particular external sense function. The second word is the conditional jump address. The Sense instruction transmits the function code on the E Bus for 1350 nsec (see Figure 2-8). Lines EB00-EB05 contain the device address, lines EB06-EB08 dictate the particular function to be sensed, and EB12 is true indicating a sense command. The EB12 line need not be used in forming a sense response command because the computer will not respond to the SERX-I line unless a sense command is being executed. The function address · (IUAX-I) can be directly used to enable a sense line driver. The user has the option of using the EB12 line for any case where he must know if a function is being sensed. The FRYX-I signal is normally not used for a sense response command, but is furnished for the user that desires a clocking pulse while performing a sense function. The SERX-I line is the return line to the computer with all sense line drivers connected to this line. The SERX-I line must be driven within 600 nsec after time T_0 (see Figure 2-8), if the computer is to recognize a "Sense Condition Met".

An example of sense function decoding is shown in Figure 2-9. This example illustrates the logic required to implement eight sense functions. The line receivers interface with the I/O Cable signals shown. Lines EB00-EB05 plus the signal IUAX+ are used at the address detection gate to form the enable for all sense lines. Lines EB06-EB08 are decoded into the six combinations shown, with the final decoding provided on the eight NAND gates with the corresponding sense lines. The AND-OR function is formed by attaching the NAND outputs and inverting. This function enables the line driver circuit (the inverter and line driver are located on the adapter card).

2.2.4 Data Transfer In Operation

Data Transfer In is a two-phase I/O operation (both phases are completed during one instruction). The device address is transmitted during the first phase. During the second phase, data is placed on the E Bus by the addressed I/O device. Data is transferred into the computer by one of the Data Input instructions, either to one of the computer registers or directly into the memory. The first-phase timing is similar to the first phase of other I/O functions. EB13 is true to indicate a Data Transfer In function (lines EB00-EB05 contain the device address).

Since the E Bus is time-shared, a flip-flop (in the selected device) is used to remember that the addressed device is to place data on the bus during the second phase. This flip-flop, Data Transfer In (DTIX+), is set at the trailing edge of FRYX+ (with the proper enabling conditions), reset with the trailing edge of DRYX+, thus enabling data onto the E Bus. The timing of the Data Transfer In operation is shown in Figure 2-10. As indicated, the selected data must be enabled onto the E Bus no later than 700 nsec after the trailing edge of the pulse FRYX+.

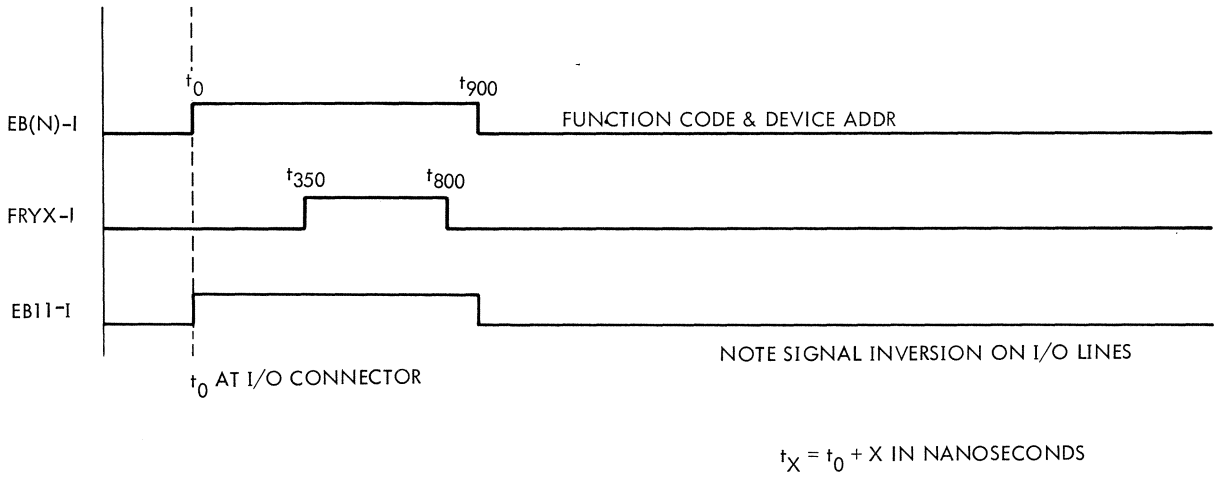

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Fig. 2-6 External Control Timing

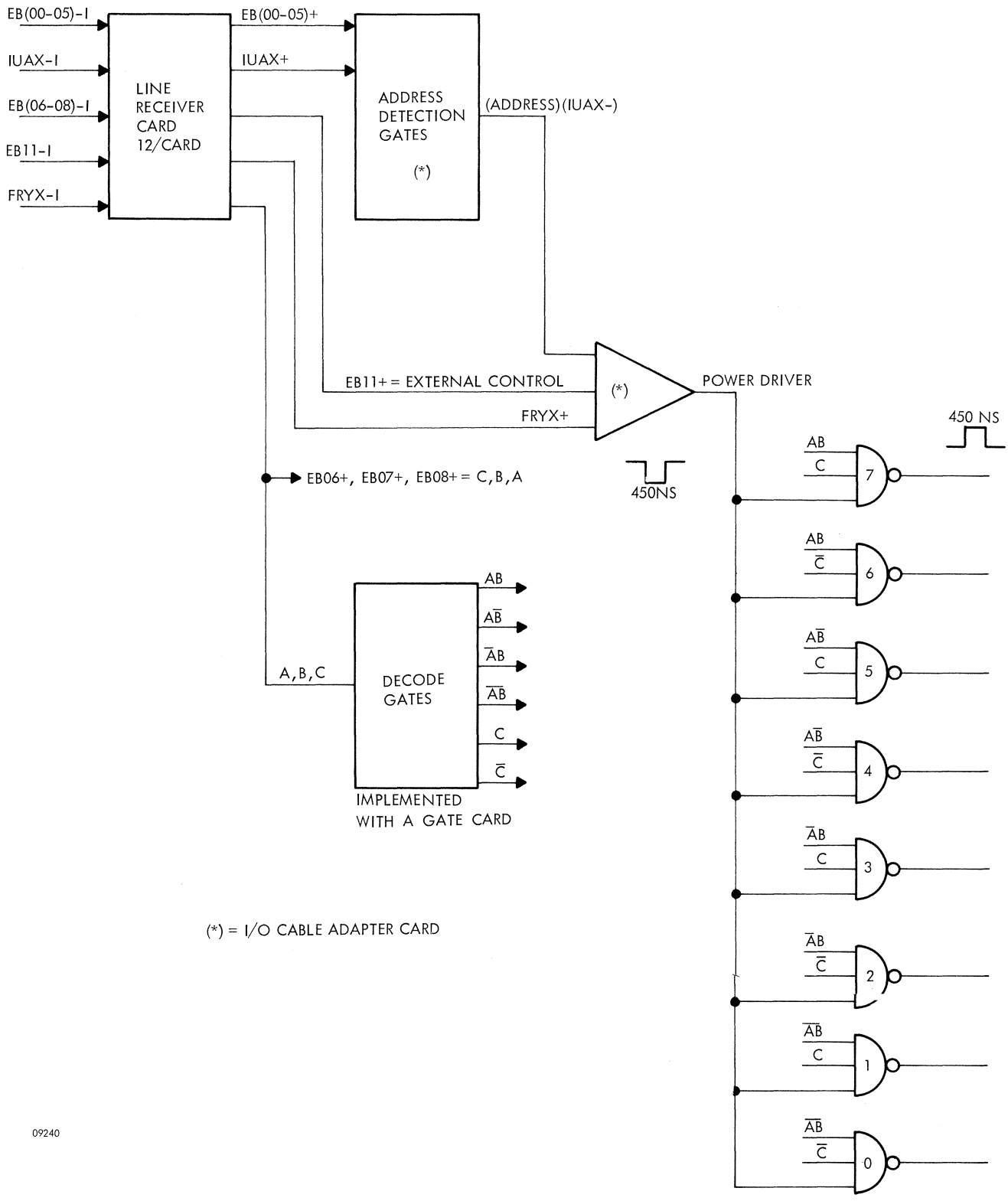
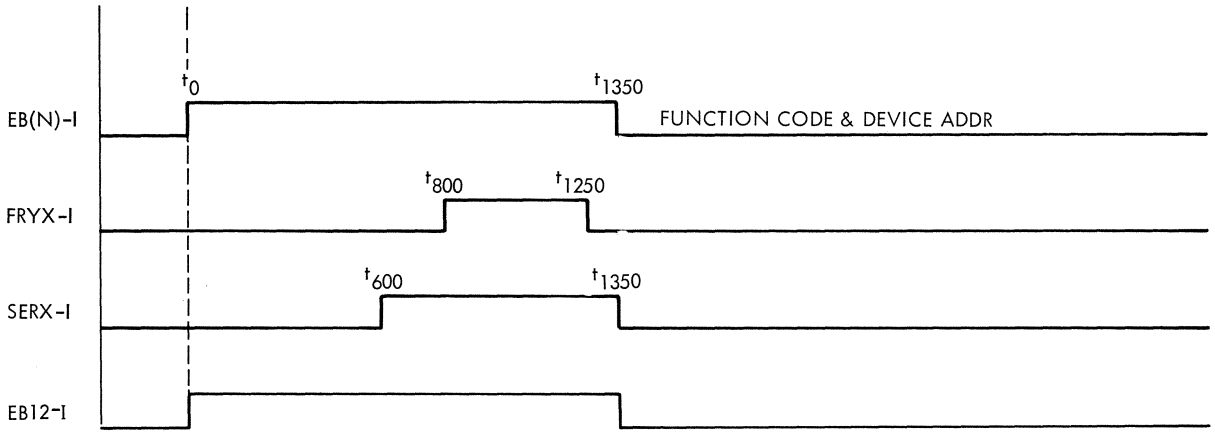


Fig. 2-7 Example of External Control for Eight EXC Lines



$t_X = t_0 + X$ IN NANOSECONDS

SERX- MUST BE ON (IF RESPONSE IS TRUE) t_{600},
NORMALLY OFF t_{1350}, MUST BE OFF t_{1950}

NOTE SIGNAL INVERSION ON I/O LINES

Fig. 2-8 Sense Response Timing

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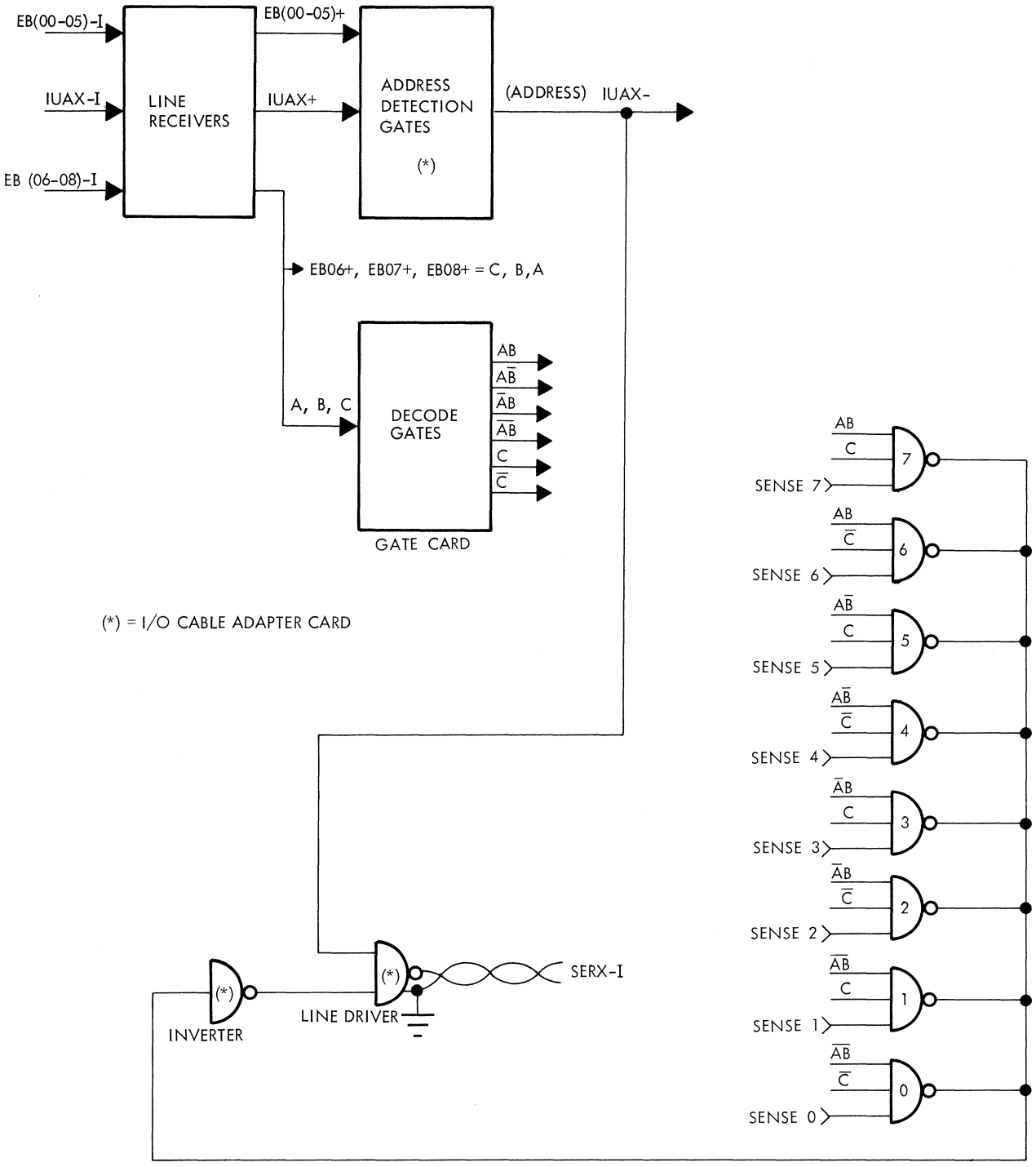

Fig. 2-9 Example of Sensing Eight Sense Lines

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An example of the Data Transfer In operation, shown in Figure 2-11, illustrates the standard Buffered Input Channel. In this configuration, a full data word storage register is provided. External data is loaded into the register by a "Drop In" pulse. This pulse also sets the Buffer Ready flip-flop which can be sensed by the computer.

The Data Input instruction will, by means of the address decoding logic and the FRYX+ pulse, set the DTIX+ flip-flop. This immediately enables the line drivers and transfers the contents of the register to the E Bus. The data remains on the E Bus until the trailing edge of DRYX+, at which time all flip-flops in the Buffered Input Channel are reset.

The standard Gated Input Channel configuration is formed by removing the data word storage register and connecting the external data directly to the gated line drivers. All other functions are identical.

2.2.5 Data Transfer Out Operation

Data is transferred from the computer to an external device by one of the Data Output instructions. Data from the computer can originate from one of the computer registers or directly from the memory. The Data Transfer Out is a two-phase operation where the first phase outputs the function code (EB00-EB05 = address and EB14 = Data Output). This phase is terminated and the selected device strobes this information with the pulse DRYX+. As shown in Figure 2-12, the computer removes the data 100 nsec after the DRYX+ pulse. The overlap of 100 nsec allows the user to form a register-set pulse with a power driver and strobe EB00 - EB(N) information into a flip-flop register. Since the address code is not on the E Bus during the second phase, a flip-flop is used to store the device selection. This flip-flop is called DTØX+ (Data Transfer Out) and is used to enable the DRYX+ pulse to strobe the E Bus data into the register. The DTØ flip-flop is set during the first phase of the I/O instructions with FRYX+, and is reset during the second phase with DRYX+.

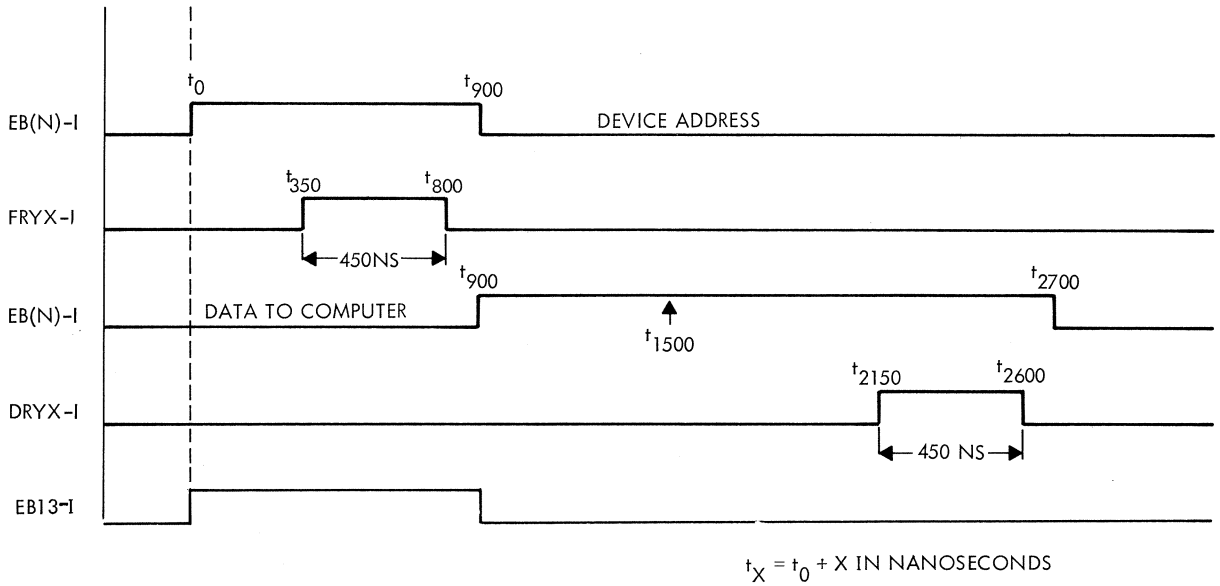
Figure 2-13 shows an example of a Data Transfer Out operation with a standard Buffered Output Channel. The external device must request data with a request pulse. This pulse sets the Buffer Ready flip-flop (BRYX). The Buffer Ready flip-flop is connected to the sense return line and may be sensed by the computer at any time. In the example shown, the buffer register is reset when the DTØX flip-flop is set (by the level going to -12 V) and loaded with the FRYX+ pulse. The DTØX and BRYX flip-flops are reset with the DRYX+ pulse.

2.3 AUTOMATIC CONTROLLED FUNCTIONS

Automatic Controlled Functions, especially interrupts and traps, can demand the computer system to perform a function that is independent of a particular instruction being executed. The program-controlled functions of paragraph 2.2 are all executed under control of DATA 620 instructions.

2.3.1 Priority Lines and Interrupt Clock

The devices that connect to the I/O Cable and perform demand-type functions must first establish a priority to resolve two or more simultaneous demands to the computer. The priorities of the devices are determined every 1.8 usec and are clocked with the interrupt clock IUCX-I (a 1.1-mc signal). The computer sends a Priority Out signal (PR1X-I, see Table 2-2) when a device may have priority, and receives a Priority In signal (PR4X-I) when no device is demanding computer intervention.



EB(N)-I - DATA - NORMALLY ON t_{900}, MUST BE ON t_{1500}
NORMALLY OFF t_{2700}, MUST BE OFF t_{3300}

NOTE SIGNAL INVERSION ON I/O LINES

Fig. 2-10 Timing of Data Transfer In

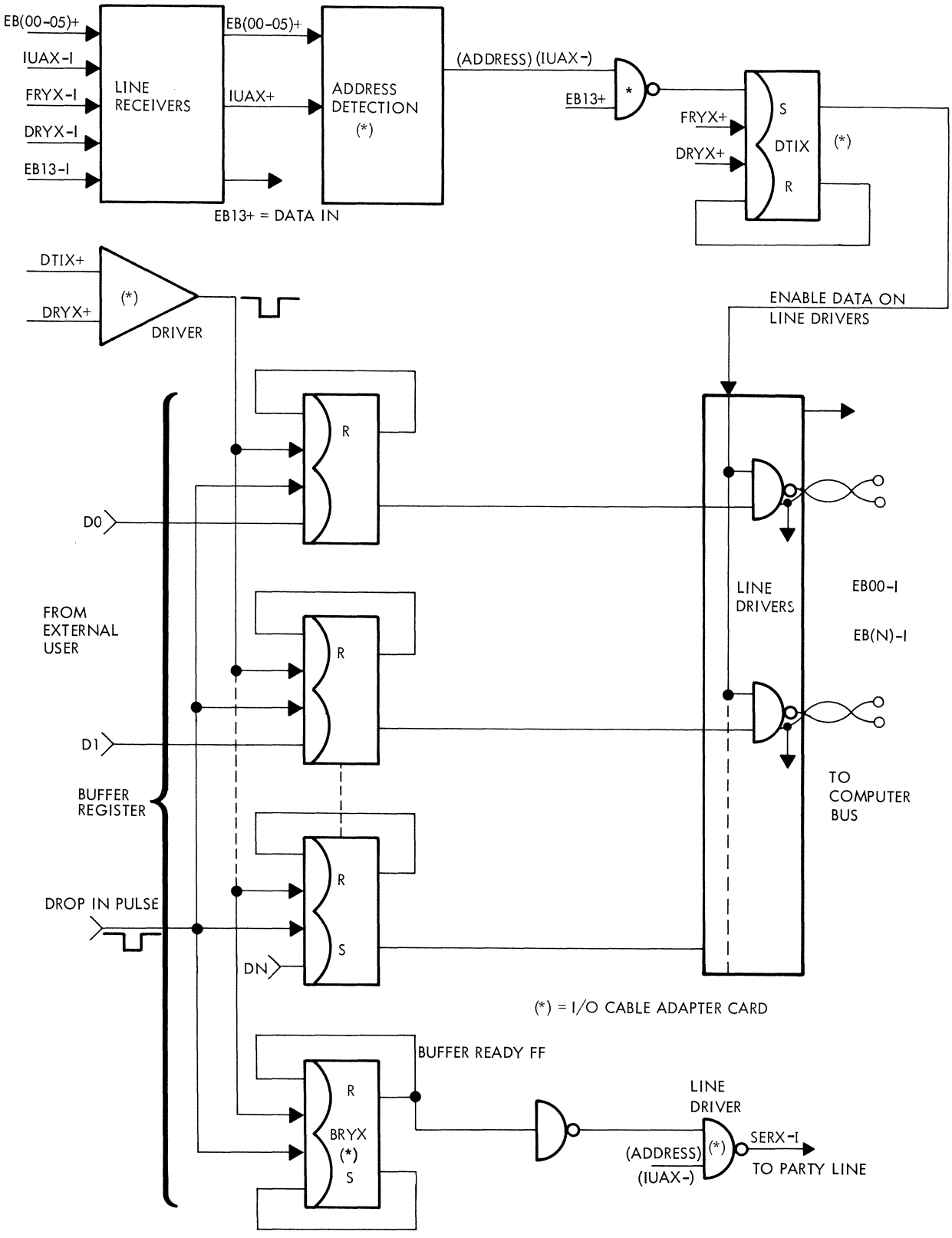
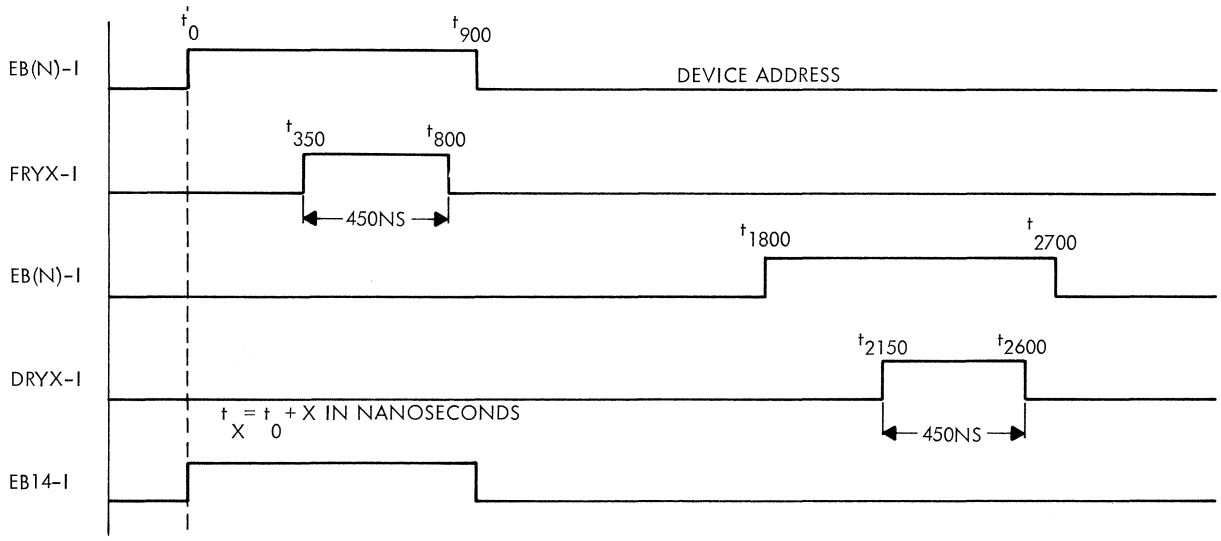


Fig. 2-11 Example of Buffer Data Transfer In



NOTE SIGNAL INVERSION ON I/O LINES

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Fig. 2-12 Data Output Timing

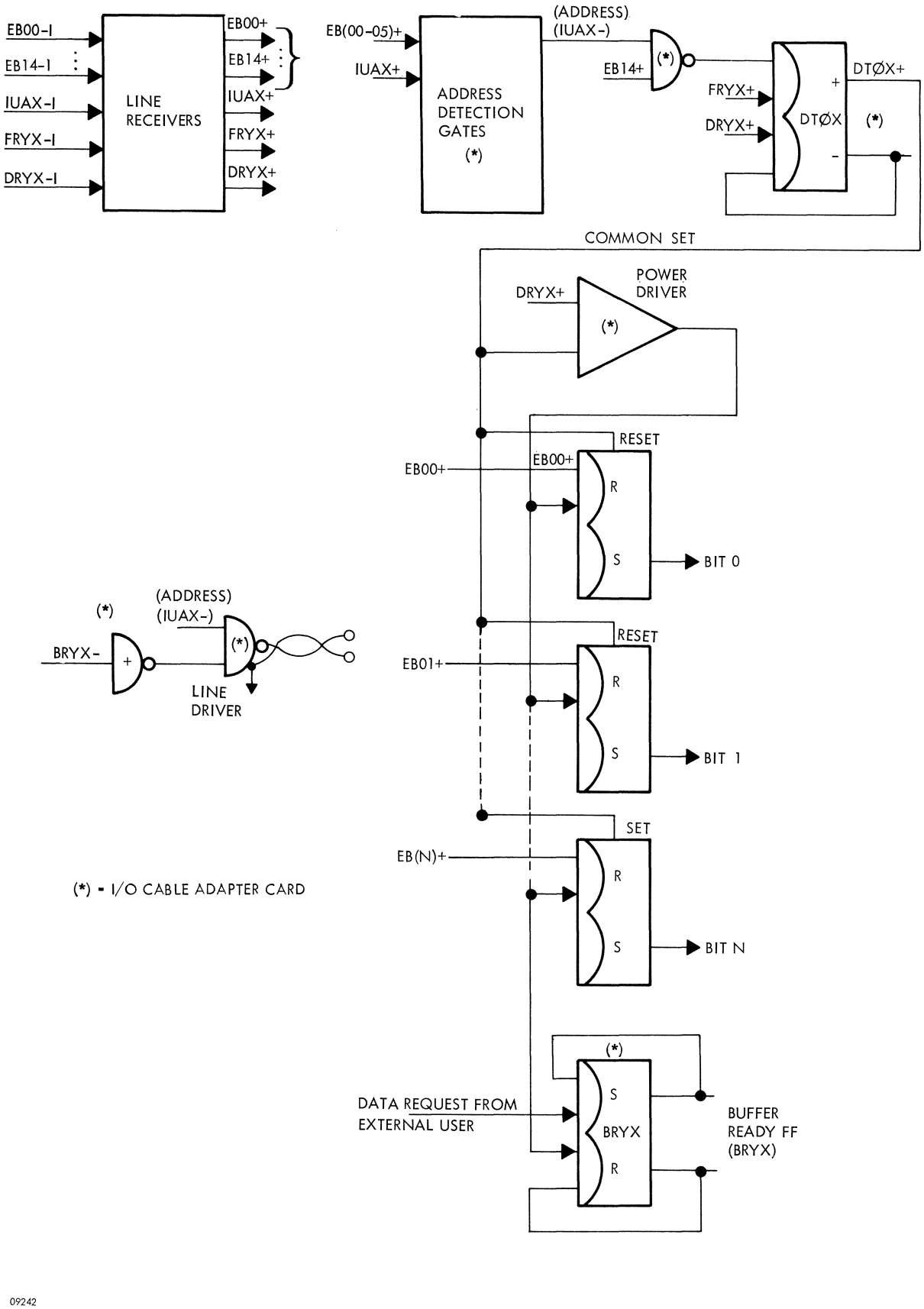


Fig. 2-13 Example of Buffer Data Transfer Out

The basic computer has two built-in priority devices, both internal program interrupts. The power failure interrupt is permanently wired for the highest priority. Unless power failure (scanned every 1.8 usec) is detected, the computer holds the PR1X-I signal on the bus. If no device wants a demand function, the Priority In signal (PR4X-I) will return true from the I/O Cable. The PR4X-I signal allows the console interrupt to be enabled (the second of two internally wired interrupts).

The intermediate priority lines (PR2X-I, PR3X-I, see Table 2-2) are used to allow the designer to assign priorities to units not physically adjacent. The only requirements in priority logic are that the chain not be broken unless the demand device wants to interrupt or trap the computer.

If the PR1X-I signal is TRUE, requests will be accepted from a device. This signal is FALSE only when a power failure has been detected and the power fail interrupt is in process; during that time, all trap requests from the devices on the I/O Bus are ignored by the DATA 620.

The PR4X-I signal will be FALSE when any device is generating a request (TPØX-I, TPIX-I, or IURX-I). During this time, interrupt requests from the console are ignored by the DATA 620.

The priority assignment among multiple devices on the I/O Bus is made by inhibiting a trap request from one unit when a request from a higher-priority unit is on. Thus, each device has priority logic which receives a priority input which, when true, indicates that it may generate a request. The output of this priority logic is set false when the device is generating a request, indicating that no unit of lower priority may generate a trap or interrupt request.

The simplest assignment of priorities is to let the physical position on the I/O Cable determine the priority. This is illustrated in Figure 2-14. The Priority Output (PR1X-I) from the Central Processor serves as the input to the highest-priority logic, its output is the input to the second, and so on. When the highest-priority unit generates a trap request, all lower priority units are inhibited from generating a trap or interrupt request.

Where physical location on the I/O Cable does not correspond to the priority assignment, an arrangement such as illustrated in Figure 2-15 is used. The priority of each device may be set up as desired and the priorities may be reassigned at any time by a simple change of jumpers.

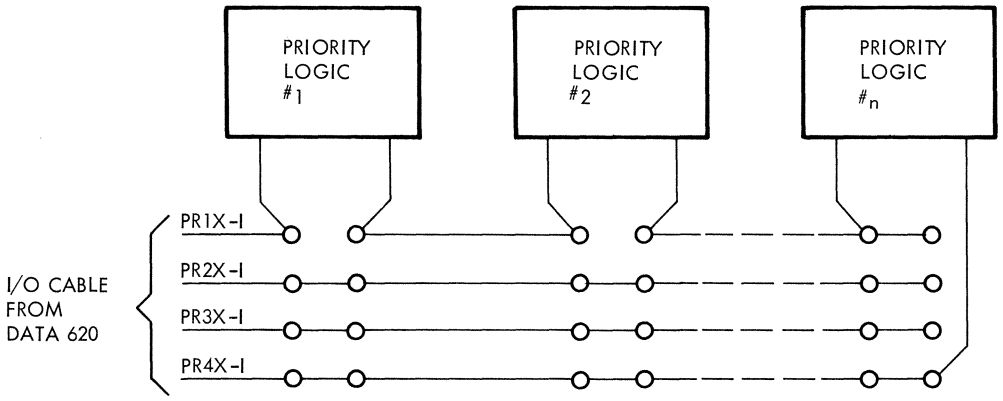
The Interrupt Clock (IUCX-I) line is used by all devices that will request either an interrupt or a trap from the computer. All requests should be turned on at the IUC time so that multiple requests have time to settle the priority chain, and lower-priority requests may remove their signals before the Interrupt Acknowledge signal (IUAX-I).

2.3.2 Computer Interrupts

The following paragraphs describe the philosophy for requesting and acknowledging interrupts. The Interrupt Module, Model 620-27, is implemented using these Control Lines*.

As shown in Figure 2-16, the signals used are Interrupt Request (IURX-I), Interrupt Acknowledge (IUAX-I), and the E Bus for sending the interrupt address to the computer. When an interrupt device wants to execute an interrupt, the device places an Interrupt Request signal on the I/O Cable, if the priority line coming into the device is TRUE. The device must also set FALSE the priority signal

*The reader should consult the Interrupt Module manual for a detailed description of its operation and interface.



NOTE: PR2X-I AND PR3X-I ARE NOT NEEDED.

Fig. 2-14 Priority Assignment by Physical Order on the E Bus

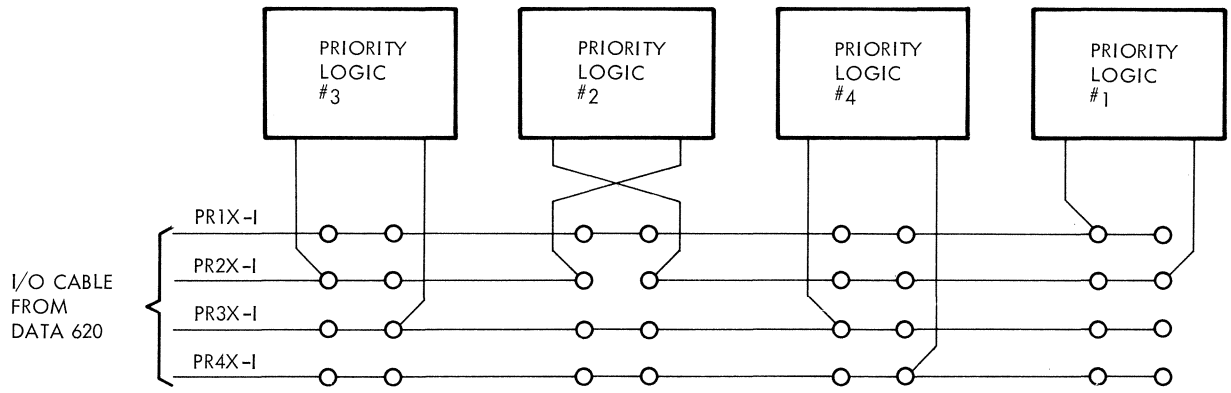


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Fig. 2-15 Priority Assignment by Jumpers

for all downstream requesting devices. After the completion of the instruction being executed, the computer will respond with an Interrupt Acknowledge (IUAX-I).

As shown in Figure 2-16, the IURX-I signal will be true for a variable period of time until the IUAX-I signal. This time will vary depending on the instruction being executed. The device must have the interrupt address on the E Bus 600 nsec after IUAX-I becomes true, and must remove the address and IURX-I signals within 150 nsec after IUAX-I goes false.

2.3.3 Interlaced Data Transfers

The following paragraphs describe the philosophy for performing data (full word) transfers directly to and from the memory connected with the computer. The Buffer Interlace Controller (BIC, Model 620-15) is implemented using the following technique. (The interested user should consult the BIC Manual for its use and interfacing requirements.)

Basically, the trap (interlace) sequence is a three-phase operation: Request, Address, and Data. First, the device requests a trap into or out of memory (with a TPIX-I or TPØX-I). Second, the computer acknowledges with an IUAX-I and the device places the address of the desired memory location on the E Bus, and third, after the computer responds with a FRYX-I, the data is placed on the E Bus (either from the device or from the computer). The sequence ends with a DRYX-I pulse that strobes the data into or out of the computer and all signals are removed from the bus (see Figure 2-17).

2.4 MISCELLANEOUS SIGNALS

2.4.1 Systems Reset (SYRT-I)

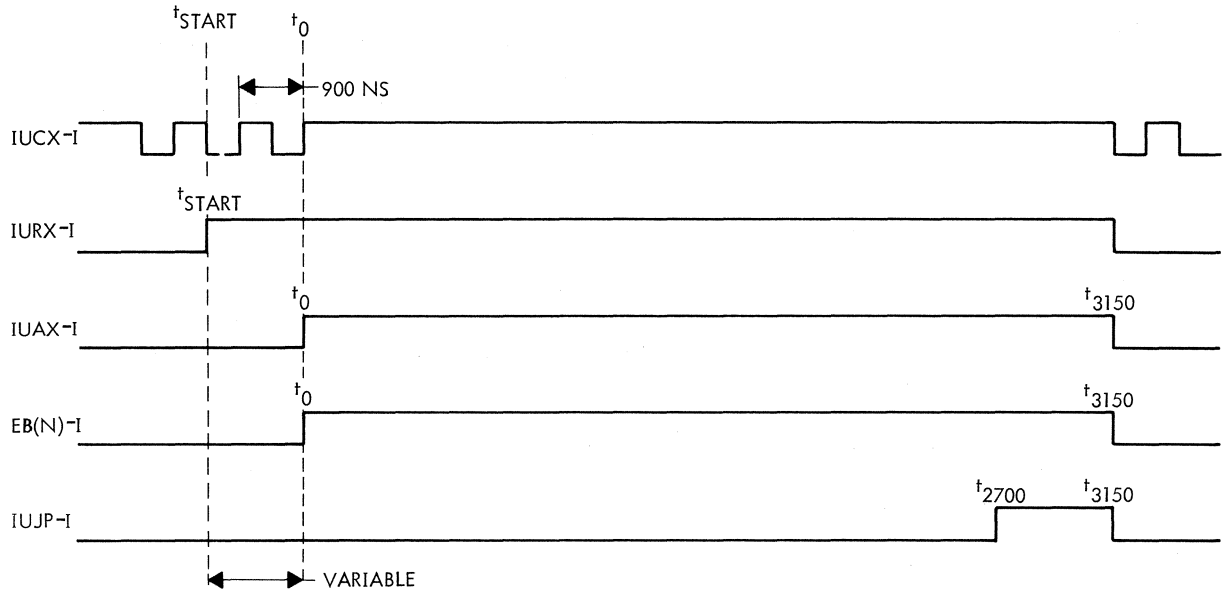
The SYRT-I signal is provided for initializing I/O controllers when the "System Reset" switch is pressed on the computer console. The SYRT-I signal rises to ground when pressed, and returns to -4 volts when released. This signal is connected to a line receiver to convert to standard Versa-LOGIC voltages for use in the I/O devices.

2.4.2 Interrupt Jump (IUJP-I)

The Interrupt Jump signal (IUJP-I) indicates that the instruction being executed due to an Interrupt Request (IURX-I) is a Jump-and-Mark instruction. The interrupt module uses this signal to inhibit further requests. The module may then be enabled under program control.

2.4.3 Interrupt Lines IU00-I through IU15-I

The Interrupt Lines on the I/O Cable are used for communication between the I/O devices and a priority interrupt module. In the absence of any interrupts, these lines may be used for user communications.



IUCX-I - REMOVED AT t_0 , RETURNS t_{3150}

IURX-I - NORMALLY REMOVED AT t_{3150}, MUST BE t_{3300}

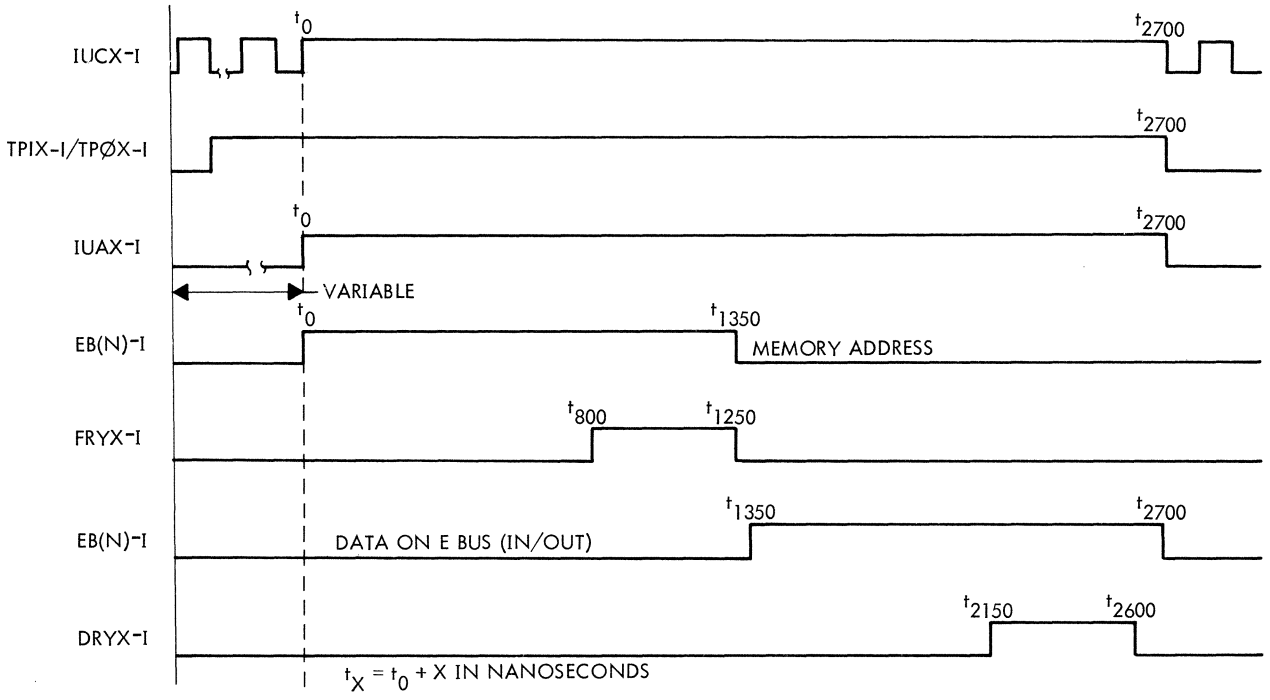
IUAX-I - NORMALLY REMOVED AT t_{3150}, MUST BE t_{3300}

EB(N)-I - ADDRESS NORMALLY ON t_0, MUST BE ON t_{600}

IJUP-I - PRESENT IF JUMP-AND-MARK INSTRUCTION

NOTE SIGNAL INVERSION ON I/O LINES

Fig. 2-16 Timing of Interrupt Sequence



IUCX-I - REMOVED AT t_0 RETURNS AT t_{2700}

TPIX-I/TPØX-I - NORMALLY REMOVED AT t_{2700} , MUST BE REMOVED BY t_{2900}

EB(N)-I ADDRESS - NORMALLY ON t_0 , MUST BE ON t_{600}
NORMALLY OFF t_{1350} , MUST BE OFF t_{1950}

EB(N)-I DATA (IN) - NORMALLY ON t_{1350} , MUST BE ON t_{1900}
NORMALLY OFF t_{2600} , MUST BE OFF t_{2900}

EB(N)-I DATA (OUT) - WILL BE ON t_{1500} , WILL BE REMOVED t_{2700}

NOTE SIGNAL INVERSION ON I/O LINES

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Fig. 2-17 Timing Sequence of Trap In/Out

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