SYSTEM REFERENCE MANUAL

DATA/620

DATA MACHINES, INC.

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Address comments concerning this manual to:
DATA MACHINES, INC.
Div. of DECISION CONTROL , INC.
1590 Monrovia Avenue
Newport Beach, Calif. 92660
or use comment sheet located in the rear of this manual.

TABLE OF CONTENTS

TABLE OF CONTENTS (cont'd)

TABLE OF CONTENTS (cont'd)

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I
INTRODUCTION

SECTION I
INTRODUCTION

1.1 THE DATA 620

The DATA 620 is a high-speed, parallel, binary computer. Its flexible design and modular packaging make it ideal for operation both as a general-purpose machine and for application as an on-line system component.

Its features include:

- Fast operation: 1.8-microsecond memory cycle
- Large instruction repertoire: 107 standard, 21 optional; over 128 additional instruction configurations which can be micro-coded.
- Expandable word length: 16- or 18-bit configurations
- Modular memory: 2048 word minimum, 4096 words standard, 32,768 maximum; plug-in module expansion.
- Multiple addressing modes: direct, indirect, relative, index, immediate, and extended (optional).
- Flexible I/O: up to 64 devices on the I/O Cable, including optional interlaced data transmission and direct memory access operations.
- Extensive software: complete package includes an assembler, mathematic and I/O library, AID, diagnostics, and FORTRAN.
- Modular packaging: convenient book-rack assembly mounts in a standard 19-inch cabinet. No special mechanical or environmental facilities are required.

The advanced design techniques used throughout the DATA 620 system provide solutions to real-time data acquisition, telemetry processing, process control, and simulation problems. In addition, the DATA 620 is equally well suited for scientific computations. Special attention has been given to the interfacing problems usually encountered in integrating a digital computer into a system. As a result, the DATA 620 can be joined to a system with unparalleled efficiency.

The unique design of the DATA 620 makes it easy to program, operate, and maintain. The entire main processor, including all options and up to 8192 words of memory, is in a convenient, 26-1/4 inch high book rack package. Only 90 circuit boards, of 14 different types, are used in the basic 16-bit configuration. Memory and logic power supplies are separate 5-1/4 inch rack-mounted units. Peripheral interfaces may be mounted either in 7-inch slide drawers or in standard 19-inch card modules. Installation is easy; no special mounting, cabling, or air-conditioning provisions are required. Maintainability of the DATA 620 is enhanced by easy front access to all components and wiring, making it

unnecessary to remove panels or move the computer rack. Using standard VersaLOGIC circuit modules, proved by over four years of use, the DATA 620 is a computer of outstanding reliability.

A complete set of software provided with the DATA 620 permits rapid preparation of application programs. The system software includes:

- FORTRAN - Subset of ASA FORTRAN
- DATA 620 ASSEMBLY SYSTEM (DAS) - Two-pass symbolic assembler
- AID - On-line debugging and utility package
- MAINTAIN - Complete set of computer and peripheral diagnostics
- SUBROUTINE LIBRARY - Complete library of transcendental functions, single- and double-precision arithmetic, format conversion, and peripheral service routines.

A wide variety of peripheral equipments are available to provide the DATA 620 user with a complete system suited to specific needs.

1.2 USE OF THE MANUAL

This manual provides the basic information required for programming and using the DATA 620, and is intended to be used in conjunction with other DMI publications for the 620-series Computers. These publications are listed in Table 1-1.

The Interface Reference Manual provides detailed information for installing the DATA 620, and for integrating the DATA 620 with special system components.

Information required by the programmer for using the system software packages is contained in the Programmers Reference, Basic FORTRAN, and Subroutine Manuals.

The Maintenance Manual is a five-volume set containing the detailed design theory, logic and timing diagrams, circuit board data, maintenance procedures, and diagnostic programs.

Detailed design and maintenance information on peripheral device controllers is contained in individual reference manuals for these units. Operating and maintenance procedures for optional peripheral devices (tape transports, printers, etc.) are contained in the manufacturers' reference manuals furnished with the equipment.

Section II of this manual contains an overall description of the DATA 620 system, and describes the word formats used in the Computer. Section III describes the complete instruction set for the Central Processor. The input/output system, including all Input/Output, Sense, Control, and Interrupt instructions is described in Section IV. Section V provides information required for using the Control Console of the Computer. Standard peripheral devices are described in Section VI.

Table 1-1
DATA 620 DOCUMENTS

DMI PUBLICATION NUMBER	TITLE
S-2000-XXXX	Systems Reference Manual
S-2001-XXXX	Interface Reference Manual
S-2002-XXXX	Programmers Reference Manual
S-2003-XXXX	Basic FORTRAN Manual
F-2002-XXXX	Subroutine Manual
F-2001-XXXX	Maintenance Manuals
F-2004-XXXX	ASR-33 Teletype Controller Reference Manual
F-2005-XXXX	Buffer Interlace Controller Reference Manual
F-2006-XXXX	Magnetic Tape Controller Reference Manual
F-2007-XXXX	600 LPM Line Printer Controller Reference Manual
F-2008-XXXX	300 LPM Line Printer Controller Reference Manual
F-2009-XXXX	Paper Tape System Controller Reference Manual
F-2010-XXXX	100 CPM Card Reader Controller Reference Manual
F-2011-XXXX	Priority Interrupt Reference Manual

1.3 SPECIFICATIONS

Specifications of the DATA 620 Computer are listed in Table 1-2.

Table 1-2
DATA 620 SPECIFICATIONS

SPECIFICATION	CHARACTERISTICS
TYPE	General-purpose digital computer for on-line data system applications. Magnetic core memory: binary, parallel, single-address, with bus organization.
MEMORY	Magnetic core, 16 bits (18 bits optional): 1.8 microseconds full-cycle, 700 nanoseconds access time, 2048 words minimum, 4096 words standard, expandable in 4096- or 8192-word modules to 32,768 words. Power failure protection (voltage and frequency), non-volatile. Each module contains data and address registers. Memory operates with the processor or direct memory access channel. Thermal overload protection is standard.
ARITHMETIC	Paralle, binary, fixed point, 2's complement.
WORD LENGTH	16-bits standard; 18-bits optional.
SPEED (fetch and execute)	
Add or Subtract	3.6 microseconds
Multiply (optional)	16 bits - 18.0 microseconds 18 bits - 19.8 microseconds
Divide (optional)	16 bits - 18.0 to 25.2 microseconds 18 bit - 19.8 to 28.8 microseconds
Register change class	1.8 microseconds
Input/Output	From A or B - 3.6 microseconds From Memory - 5.4 microseconds Optional - 556,000 words/second
OPERATIONAL	
A Register	Accumulator, input/output; 16 or 18 bits.
B Register	Low-order accumulator, input/output, index register; 16 or 18 bits.

Table 1-2 (cont'd)
DATA 620 SPECIFICATIONS

SPECIFICATION	CHARACTERISTICS
X Register	Index register, multi-purpose register; 16 or 18 bits.
P Register	Instruction counter; 16 or 18 bits.
BUFFER REGISTERS	
R Register	Operand register, 16 or 18 bits.
U Register	Instruction register; 16 or 18 bits.
L Register	Memory location register, 12 or 13 bits. One L Register per memory module.
W Register	Memory word register; 16 or 18 bits. One W Register per memory module.
CONTROL	
Addressing Modes	Six as follows:
	Direct: to 2048 words
	Relative to P Register 512 words
	Index with X Register, hardware: to 32,768 words (does not add to execution time).
	Index with B Register, hardware: to 32,768 words (does not add to execution time).
	Multi-level indirect: to 32,768 words
	Immediate: operand immediately follows instruction
	Extended: operand address immediately follows instruction.
Instruction Types	Four, as follows:
	Single Word, Addressing
	Single Word, Non-Addressing
	Double Word, Addressing
	Double Word, Non-Addressing

Table 1-2 (cont'd)
DATA 620 SPECIFICATIONS

SPECIFICATION	CHARACTERISTICS
Instructions	107 standard, over 128 micro-instructions, plus 21 optional.
Micro-Exec Hardware Program (option)	Facility and hardware to construct a hardwired program external to the DATA 620. Eliminates stored-program memory accessing for hardwired programs.
Control Panel	Display and data entry switches on all operational registers; three sense switches; manual interrupt; instruction repeat; single step; run; power on/off; system reset; Instruction Register.
Maintenance Panel	Contains test points and jacks for: Computer Bus, Basic Timing, Start/Stop, Sequence Control, Instruction Control, Run-Repeat Test, Set R and U, Arithmetic Control; Set A, P, B, X; Memory Control; I/O Control.
INPUT/OUTPUT	
Data Transfer	Four modes, as follows: Single word to/from memory (program control) Single word to/from A and B Registers (program control) Optional Interlaced data channel (up to 202,000 words/second) Optional Direct Memory Access (up to 556,000 word/second)
External Control	Up to 512 external control lines.
Program Sense	Up to 512 status lines may be sensed.
Interrupts	Power failure, thermal overload, and manual interrupts standard; expandable in groups of eight priority on/off, arm/disarm. Each interrupt line has a unique memory destination.
PHYSICAL CHARACTERISTICS	
Dimensions Main Processor	26-1/4 inches high, 28 inches deep.

Table 1-2 (cont'd)
DATA 620 SPECIFICATIONS

SPECIFICATION	CHARACTERISTICS
Memory Power Supply	5-1/4 inches high.
Logic Power Supply	5-1/4 inches high.
Access	All drawers mounted for full front access.
Weight	400 pounds including power supplies.
Power	600 watts, single phase, 115 V ± 10 V, 60 cps ± 2 cps. Power supplies are regulated. Additional regulation is not required with normal commercial power sources. A constant-voltage ferroresonant transformer provides magnetic regulation of the -12 V output. The +6 V output is Zener regulated.
Construction	Modular logic pages unhinge and unplug. All drawers are connector-coupled.
Expansion	Main Processor contains all internal operations, plus space for memory expansion to 8192 words. Peripheral controllers and special interfaces are available in 7-inch drawers or card module mounts.
Installation	Mounts in standard 19-inch cabinet. No air conditioning, subflooring, special wiring, or site preparation required.
Environment	0°C to +45°C; 0 to 90% relative humidity.
LOGIC AND SIGNALS	8-mc VersaLOGIC, 2.2-mc clock. Logic levels are 0 V (false), -12 V (true). Noise rejection is 2 V at ground, 6 V at -12 V. Worst-case design.
SOFTWARE	
DAS Assembler	Modular two-pass symbolic assembler which operates within the basic 4096-word memory size. Includes 35 basic pseudo-ops plus provision for adding application-oriented macros and pseudo-ops.
FORTRAN	Modular one-pass compiler; subset of Basic FORTRAN for 4096-word memory with full FORTRAN structure available with expanded systems. Includes provisions for adding application-oriented statements as well as other capabilities as required.

Table 1-2 (cont'd)
DATA 620 SPECIFICATIONS

SPECIFICATION	CHARACTERISTICS
AID	Relocatable program analysis package which assists programmers in operating the machine and debugging other programs. Includes basic operational executive and subroutines, and capability for expansion for extended supervisory control functions.
Maintain	Modular, two-mode diagnostic package which provides fast verification of Central Processor and peripheral operation, and assistance in isolating and correcting suspect faults. Includes capability for expanding routines for diagnosis of special system hardware.
Subroutines	Complete library of basic mathematical, single- and double-precision, number conversion, and peripheral communication subroutines plus provisions for adding application-oriented routines.

SECTION II
DATA 620 SYSTEM DESCRIPTION

SECTION II
DATA 620 SYSTEM DESCRIPTION

2.1 COMPUTER ORGANIZATION

The DATA 620 is organized with a unique bus structure, selection logic, and nine registers. The organization provides universal information routing, buffered processing, micro-programming capability, indexing without time penalty, and buffered input/output data transfer. A unique optional facility, Micro-Exec, is also available which permits complex algorithms to be implemented with external control hardware. This capability provides increases in processing speed in excess of 400 percent over normal programmed operations.

The organization of the DATA 620 is shown in Figure 2-1. This diagram shows the major functional elements of the machine, including the registers and busses provided for information transfer.

The major functional elements of the DATA 620, indicated in Figure 2-1, are: Memory, Control Section, Arithmetic/Logic Section, Operational Registers, Internal Busses, Input/Output (I/O) Bus, and Direct Memory Access Bus.

2.1.1 Memory

The internal store of the DATA 620 consists of one or more core memory modules connected to the internal M Bus. The full memory cycle is 1.8 microseconds. Each module contains its own Location (L) Register and Word (W) Register. The minimum memory size is 2048 words. The standard 4096-word memory permits full utilization of the basic system software packages. The total capacity may be expanded to 32,768 words in 4096- or 8192-word increments. Modules added after installation are plugged into the M Bus Cable without changing the existing wiring.

Instruction words read from memory are transferred to the Control Section for execution. Words may be transferred, under program control, from memory to the Arithmetic/Logic Section, to the Operational Registers, or to the I/O Bus. Words may be transferred, under program control, to memory from the Operational Registers and the I/O Bus.

When one or more optional Buffer Interlace Controllers are used, the system is capable of direct transfer between memory and peripheral devices on the I/O Bus, concurrent with computations. Addition of the Direct Memory Access option permits external devices to directly control the memory for I/O transfers, with full overlap between I/O and program operations in separate memory modules.

2.1.2 Control Section

The Control Section provides the timing and control signals required to perform all operations in the computer. The major elements in the section are the U Register, the Timing and Decoding Logic, and the Shift Control.

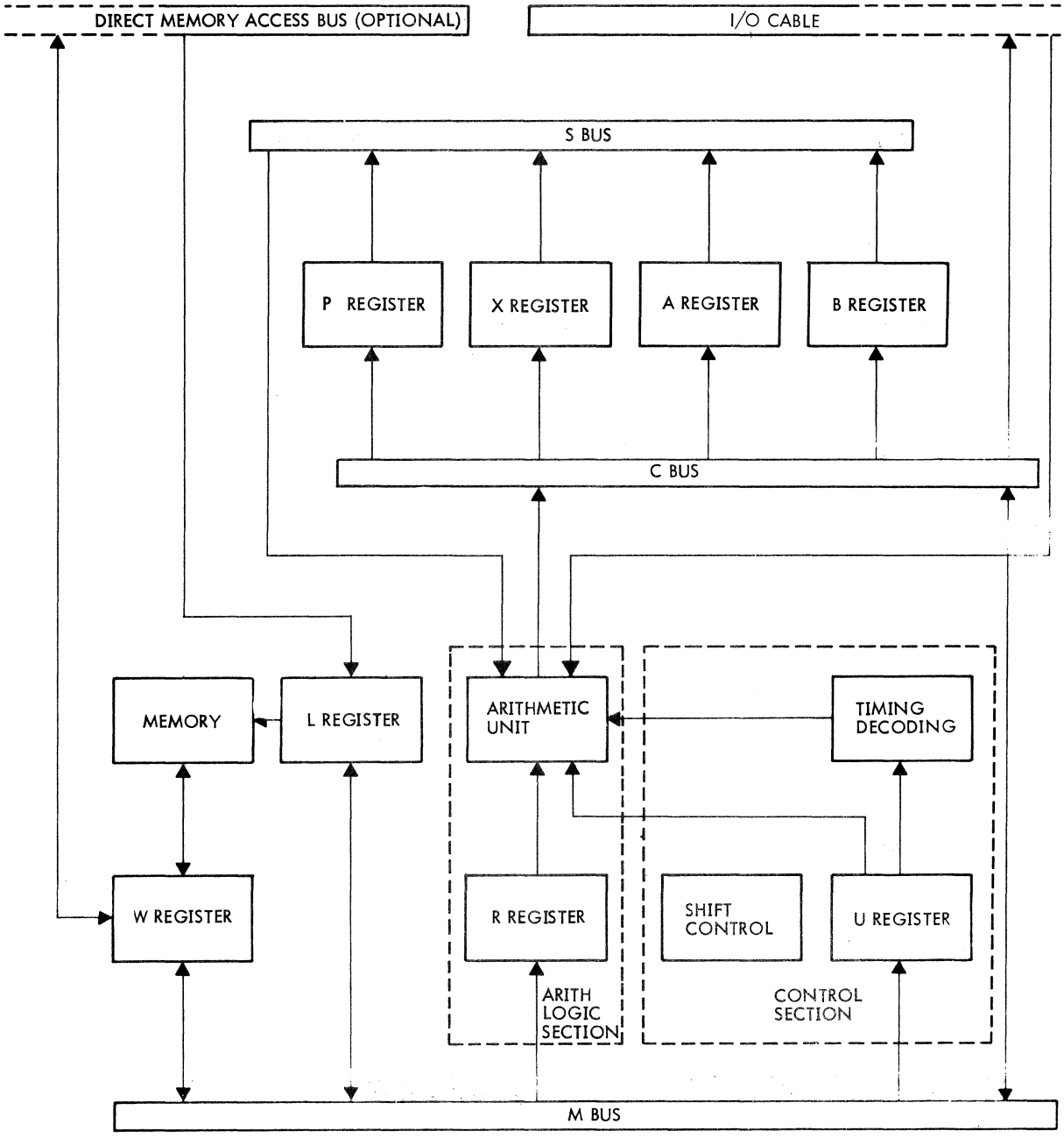


Fig. 2-1 DATA 620, Functional Organization

The U Register (Instruction Register) is 16 bits long. This register receives each instruction from memory through the M Bus and holds the instruction during its execution. The control fields of the instruction word are routed to the Decoding and Timing Logic where the codes determine the required timing and control signals. The address field from U, used for various addressing operations, is also routed to the Arithmetic/Logic Section.

The Decoding Logic decodes the fields of the instruction word held in U to determine the control signal levels required to perform the operations specified by the instruction. These levels select the timing signals generated by the Timing Unit.

Timing Logic generates the basic 2.2-mc system clock. From this clock, Timing Logic derives the timing pulses which control the sequence of all operations in the computer.

The Shift Control contains the shift counter and logic which control operations performed by the shift, multiply, and divide instructions.

2.1.3 Arithmetic/Logic Section

This section consists of two elements: the R Register and the Arithmetic Unit.

The R Register receives operands from memory and holds them during instruction execution. The operands may be either data or address words. This register permits transfers between memory and I/O during the execution of extended-cycle instructions.

The Arithmetic Unit contains gating required for all arithmetic, logic, shifting, and optional byte handling operations performed by the computer. Indexed and relative address modifications are performed in this section without increased instruction execution time.

The Arithmetic Unit also controls the gating of words from the operational registers, and the I/O, onto the C Bus where they are distributed to the operational registers or to memory. This facility is used to implement many of the micro-instructions of the computer.

2.1.4 Operational Registers

The basic DATA 620 Computer contains nine registers. Two registers are added for each additional memory module.

The operational registers consist of the A, B, X, and P registers. Three of these (A, B, and X), are directly accessible to the programmer. The P Register is indirectly accessible through use of the jump class instructions which modify the program sequence. The operational registers are described in the following paragraphs.

A Register. This full-length, 16/18-bit register is the upper half of the accumulator. This register accumulates the results of logical and addition/subtraction operations, the most-significant half of the double-length product in multiplication, and the remainder in division. It may also be used for input/output transfers under program control.

B Register. This full-length, 16/18-bit register is the lower half of the accumulator. This register accumulates the least-significant half of the double-length product in multiplication, and the quotient in division. It may also be used for input/output transfers under program control and as a second hardware index register.

X Register. This full-length, 16/18-bit register permits indexing of operand addresses without adding time to execution of indexed instructions.

P Register. This full-length, 16/18-bit register holds the address of the current instruction and is incremented before each new instruction is fetched. A full complement of instructions is available for conditional and unconditional modification of this register.

2.1.5 Internal Busses

The unique bus structure of the internal computer not only provides flexible routing facilities, but also is used to implement microprogrammed bit and byte manipulations.

M Bus. This bus provides the parallel path and selection logic for routing instructions and data between memory and the Arithmetic/Logic Section, the Control Section, and the I/O Bus. The M Bus permits input/output transfer simultaneous with the execution of extended instructions such as shift, multiply, and divide.

C Bus. This bus provides the parallel path and selection logic for routing data between the Arithmetic Unit, the I/O Bus, the M Bus, and the operational registers. The C Bus provides the distribution function for microprogrammed bit manipulations, and permits data to be simultaneously routed to multiple operational registers.

S Bus. This bus provides the parallel path and selection logic for routing data from the operational registers to the Arithmetic Unit.

2.1.6 Input/Output Bus

The bidirectional I/O Bus provides the parallel path between the computer and all peripheral devices. This bus contains the data and control lines required for transmitting ready, sense, function, and interrupt signals as well as data words between the computer and peripheral devices.

2.1.7 Direct Memory Access (DMA)

The optional Direct Memory Access and Overlap Control (Model 620-14) provides separate memory bus and priority control logic permitting an external device to directly access a memory module through the L and W registers of that module. DMA facilities may be added to each memory module in the computer. This facility permits internal program and DMA I/O cycles to occur simultaneously in separate modules. DMA assumes priority over the computer when operations occur in a common memory module.

2.1.8 Micro-Exec*

The Micro-Exec is a unique hardware technique for micro-step sequencing of the computer. This option provides hardware logic in which all computer control signals are made available on a pin board so that special hardware routines can be constructed. External control and special return instructions are provided for easy program entry and exit.

2.2 COMPUTER WORD FORMATS

There are three basic word formats used in the DATA 620: data, indirect address, and instruction. The instruction word format is further divided into four types: single-word addressing, single-word non-addressing, double-word addressing, and double-word non-addressing.

2.2.1 Data Word Format

The data word format is shown in Figure 2-2. This word may be either 16 or 18 bits depending upon the word length configuration of a particular machine.

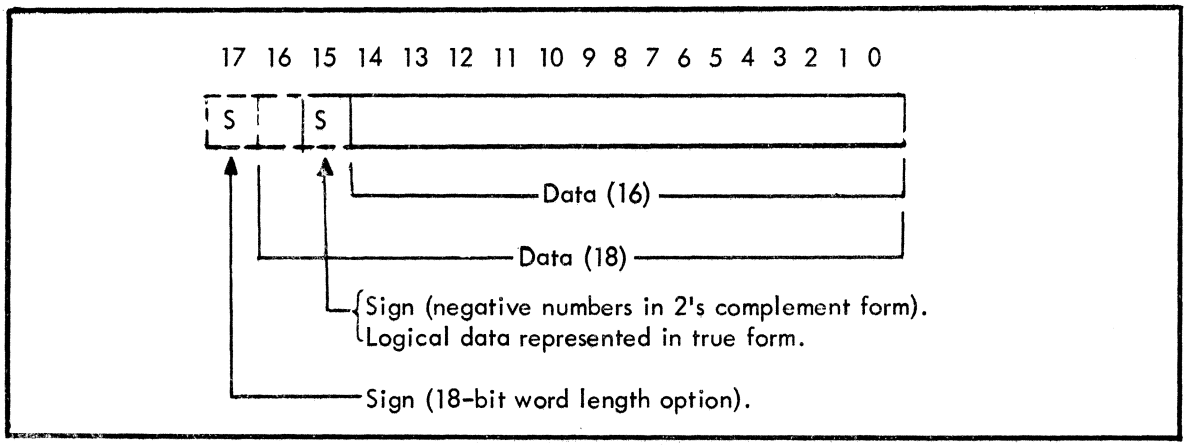


Fig. 2-2 Data Word Format

In the 16-bit format, the data occupies bit positions 14-0, with the sign in position 15. Negative numbers are represented in 2's-complement form. In the 18-bit format, the data occupies bits 16-0, with the sign in position 17.

2.2.2 Indirect Address Word Format

The indirect address word format is shown in Figure 2-3. This word will occupy a location in memory which is accessed by an instruction in the indirect address mode. Bit 15 contains the I Bit. If I = 0, bits 14-0 contain the location of an operand or instruction in memory. If I = 1, bits 14-0 contain the location of another indirect address word. Indirect addressing may be extended to any desired level.

*Registered.

Each level of indirect addressing adds one cycle (1.8 μs) to the basic execution time of an instruction.

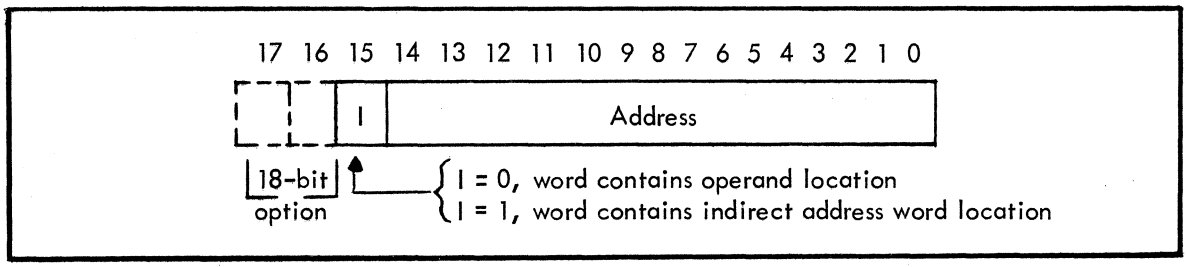


Fig. 2-3 Indirect Address Word Format

2.2.3 Single-Word Instruction Formats

Single-word instructions may be either addressing or non-addressing, as defined in paragraph 2.2.3.1 and 2.2.3.2.

2.2.3.1 Addressing instructions. The single-word addressing instruction format is shown in Figure 2-4. This type of word contains three fields, as follows:

o - Operation Code

m - Addressing Mode

a - Address Field

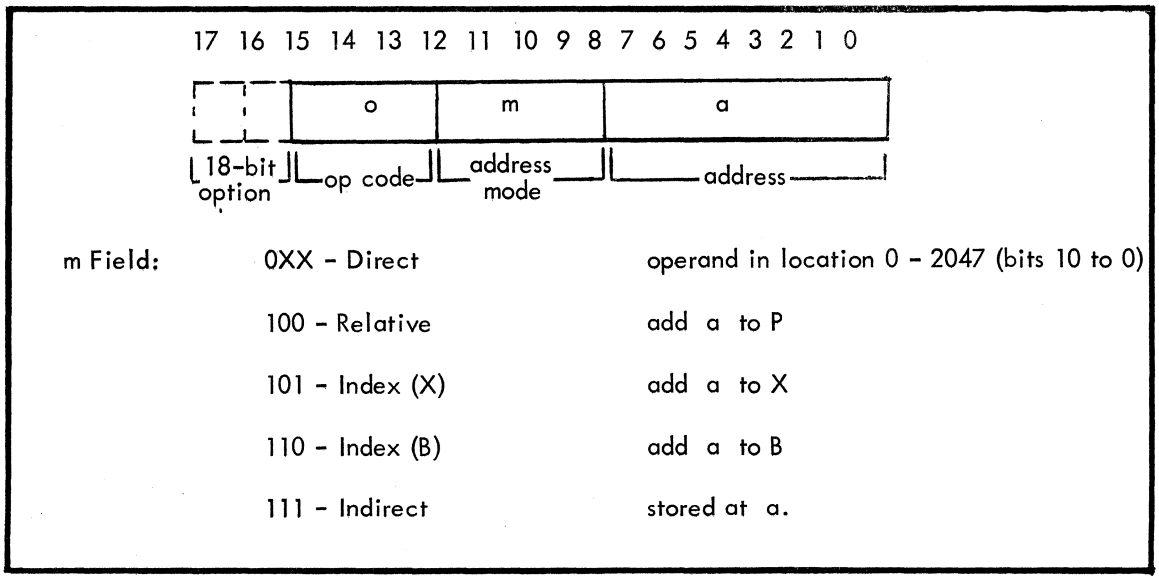


Fig. 2-4 Single-Word Addressing Instruction Format

All single-word addressing instructions may be executed in any one of five addressing modes: direct, relative to P, index with X, index with B, and indirect.

Single-word addressing instruction groups are as follows:

LOAD/STORE

ARITHMETIC

LOGICAL

2.2.3.2 Non-addressing instructions. The single-word non-addressing instruction format is shown in Figure 2-5. This instruction contains the following three fields:

c - Class Code

o - Operation Code

d - Definition

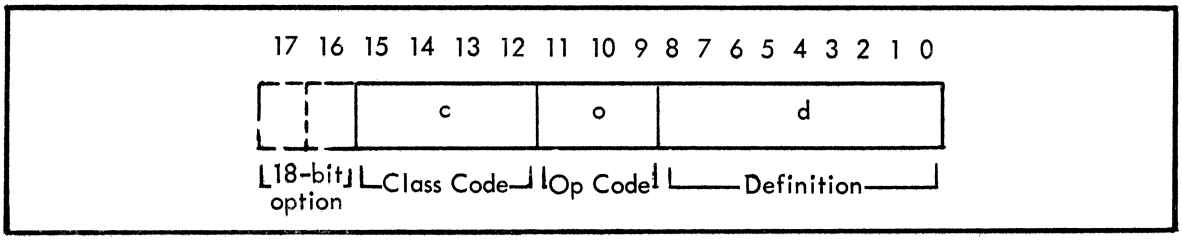


Fig. 2-5 Single-Word Non-Addressing Instruction Format

The d (Definition Field) specifies the action to be performed by the computer such as:

a. Number of shifts

b. Kind of register change as well as source and destination register

c. Input/output

d. Halt code

Single-word non-addressing instruction groups are as follows:

SHIFT

CONTROL

REGISTER CHANGE

INPUT/OUTPUT

2.2.4 Double-Word Instruction Formats

Double-word instructions may be either addressing or non-addressing.

2.2.4.1 Addressing instructions. This instruction contains three fields:

c - Class Code

o - Operation Code

d - Definition

The double-word addressing instruction is shown in Figure 2-6.

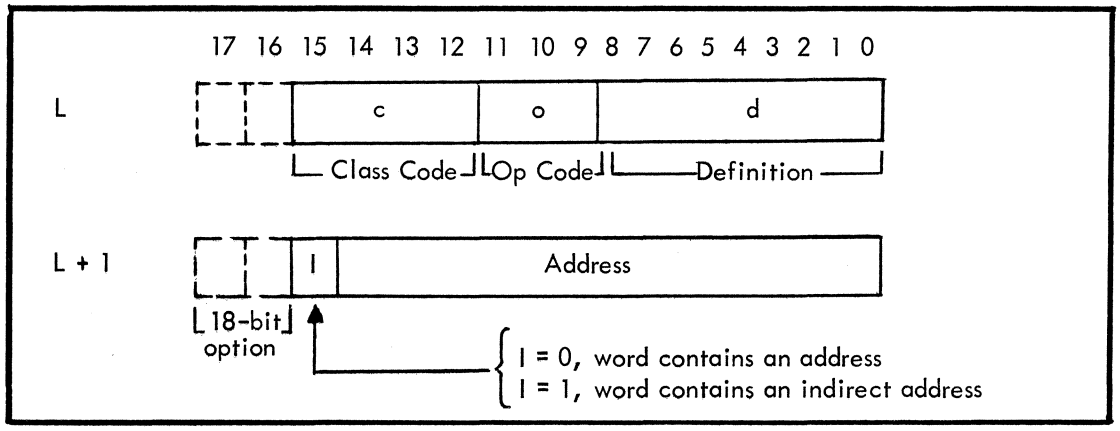


Fig. 2-6 Double-Word Addressing Instruction Format

This format is used for the following instruction types:

JUMP

JUMP AND MARK

EXECUTE

BYTE (Optional)

EXTENDED ADDRESS

For the Jump, Jump and Mark, and Execute groups, the Definition Field of the first word defines a set of nine logical states which condition the execution of the instruction. The second word contains the jump address, jump-and-mark address, or the location of the instruction to be executed if the condition is met. Indirect addressing is permitted.

For the optional Byte group, the Definition Field of the first word defines the type of masking to be performed on a word contained in memory. The second word contains the memory address of the word

to be masked during the Byte transfer. Indirect addressing is permitted.

For the Extended Address group of instructions, the Definition (d) Field is further divided into three subfields. The m field contains bits 0-2, the Op Code contains bits 3-6, with bits 7 and 8 left blank. Extended Address instructions are identical in operation to the single-word addressing instructions except that they allow direct addressing to 32,768 words of memory.

For the Memory Input/Output group, the Definition Field of the first word contains the number of the peripheral device and its mode, and the second word contains the memory address of the data to be transferred. Indirect addressing is permitted.

2.2.4.2 Non-addressing instructions. The double-word non-addressing instruction format is shown in Figure 2-7. This format is used for the Immediate group of instructions. There are 12 standard and two optional instructions in this group.

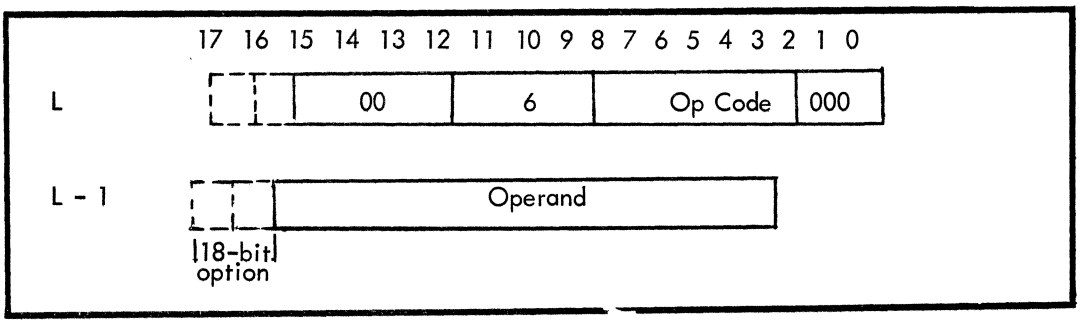


Fig. 2-7 Double-Word Instruction Format Immediate Type Instructions

The Op Code field contains the operation to be performed (bits 6 to 3). All single-word addressing type instructions may be performed as an Immediate type instruction. The operand is contained in the second word. Indirect addressing is not applicable.

SECTION III
DATA 620 CENTRAL PROCESSOR INSTRUCTIONS

SECTION III
DATA 620 CENTRAL PROCESSOR INSTRUCTIONS

3.1 GENERAL

This section describes DATA 620 instructions which affect operations in the Central Processor. Input/Output instructions are described in Section IV. Information provided for each instruction is as follows:

- The mnemonic that is recognized by the DATA 620 Assembler (DAS)
- Mnemonic definition
- Instruction timing
- Instruction description
- Registers altered by execution of the instruction
- Addressing modes permitted
- A flow chart, when required for complete understanding.

Instructions are divided into two classes: single-word and double-word. Each class contains both addressing and non-addressing groups of instructions. Microprogramming operations which can be implemented for various instruction types are summarized in Appendix G.

3.2 SINGLE-WORD INSTRUCTIONS

Single-word instructions may be either addressing or non-addressing. The addressing instruction groups are:

LOAD/STORE

ARITHMETIC

LOGICAL

The non-addressing instruction groups are:

CONTROL

SHIFT

REGISTER CHANGE

3.2.1 Single-Word Addressing Instructions

The format of the single-word addressing class instructions is shown in Figure 2-4. The operation is specified by the o field (bits 12-15). The address field a (bits 0-8) contains the base location of an operand in memory. Operand addressing may be in any one of five modes specified by the m field (bits 9-11).

Table G1(d), Appendix G, summarizes the addressing modes, and Tables G1(a), G1(b), and G1(c) summarize the operation codes for the single-word addressing instructions. Figure 3-1 shows the general operand addressing flow for this class of instructions.

For direct addressing, bits 10-0 specify the location of an operand within the first 2048 (0-2047) words of memory.

For relative addressing, the address field (a) is added to the P Register, mod 2^{15}, to form the effective address. This mode permits addressing an operand up to 511 words in advance of the current program location.

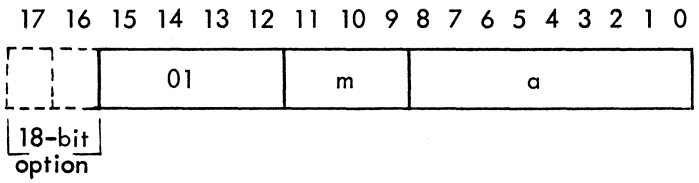
For index addressing with the X Register, the address field (a) is added to the X Register, mod 2^{15}, to form the effective address. Indexing does not increase the basic instruction execution time.

For index addressing with the B Register, the address field (a) is added to the B Register, mod 2^{15}, to form the effective address. Indexing does not increase the basic instruction execution time.

For indirect addressing, the address field (a) specifies the location of an indirect address word within the first 512 (0-511) words of memory. If I = 0 in the address word, the word contains the location of an operand. If I = 1, the word specifies the location of another indirect address word. Each level of indirect addressing adds one cycle (1.8 μs) to the basic instruction execution time.

3.2.1.1 Load/Store instruction group . The following paragraphs provide the mnemonic, description, and timing for each instruction in the Load/Store group. Figures 3-2 and 3-3 show the general flow for the Load/Store instruction group.

LDA Load A Register Timing: 2 cycles



The contents of the addressed memory location are placed in the A Register.

Relative: Yes
Indexing: Yes
Indirect Addressing: Yes
Registers Altered: A

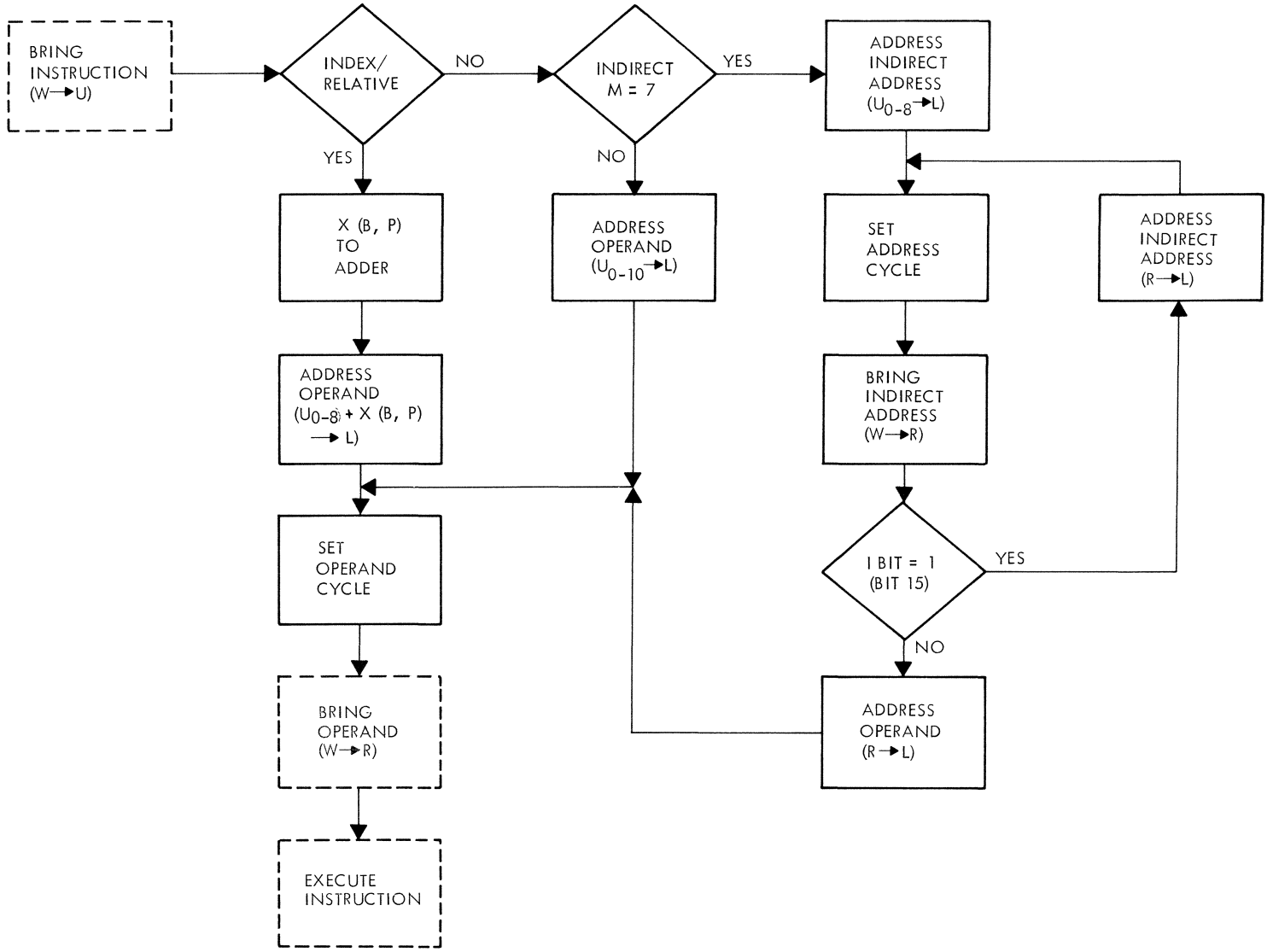


Fig. 3-1 Single-word Address Instruction, Operand Addressing, General Flow

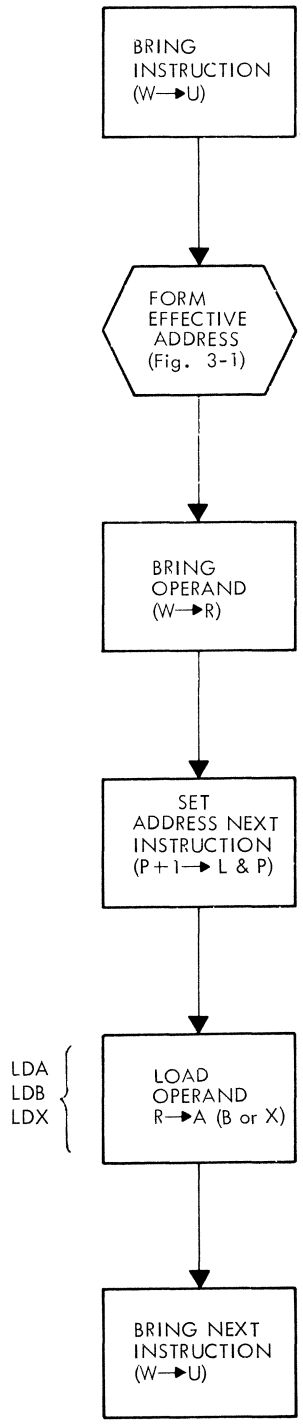


Fig. 3-2 Load-Type Instruction, General Flow

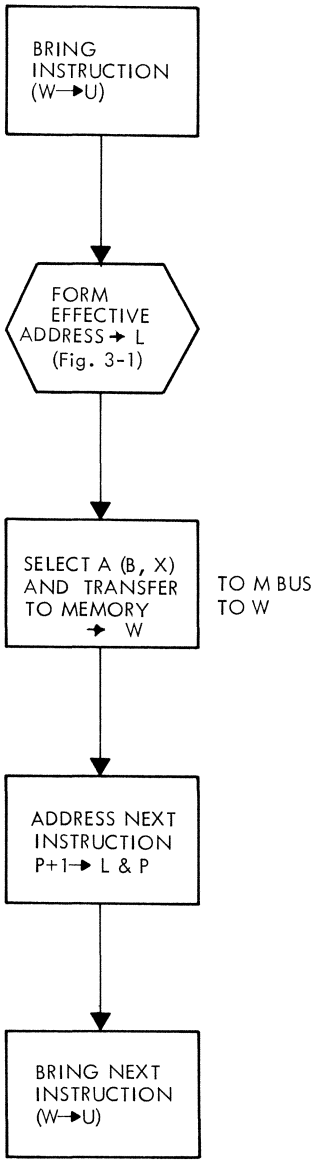


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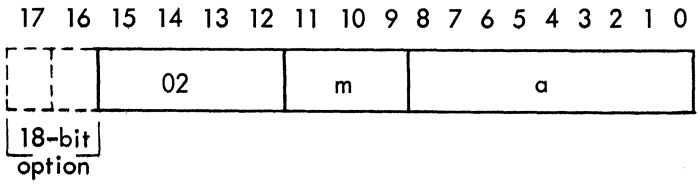
Fig. 3-3 Store-type Instruction, General Flow

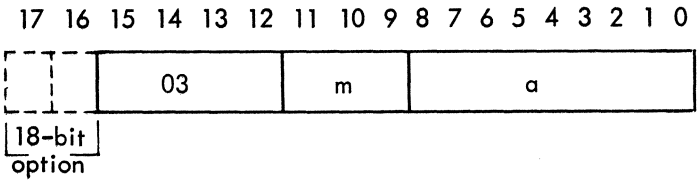
LDB — Load B Register — Timing: 2 cycles



The contents of the effective memory location are placed in the B Register.

Relative: Yes
Indexing: Yes
Indirect Addressing: Yes
Registers Altered: B

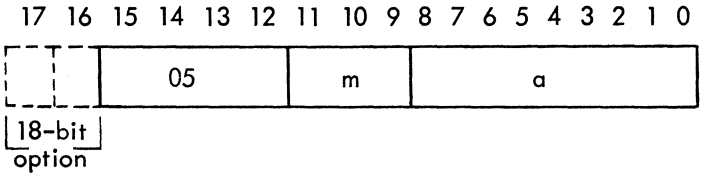
LDX — Load Index Register — Timing: 2 cycles



The contents of the effective memory location are placed in the Index Register.

Relative: Yes
Indexing: Yes
Indirect Addressing: Yes
Registers Altered: X

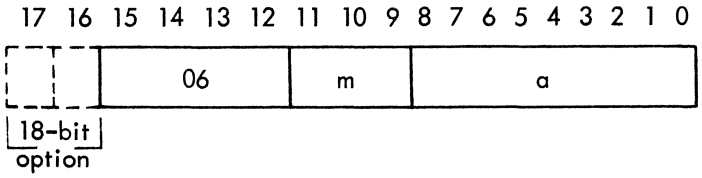
STA — Store A Register — Timing: 2 cycles



The contents of the A Register are placed in the effective memory location.

Relative: Yes
Indexing: Yes
Indirect Addressing: Yes
Registers Altered: Memory

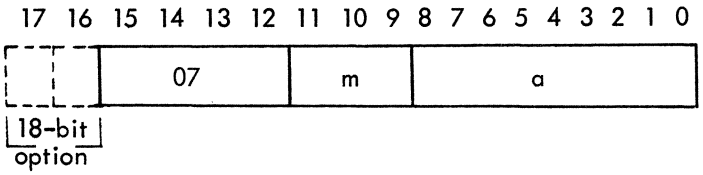
STB Store B Register Timing: 2 cycles



The contents of the B Register are placed in the effective memory location.

Relative: Yes
Indexing: Yes
Indirect Addressing: Yes
Registers Altered: Memory

STX Store Index Register

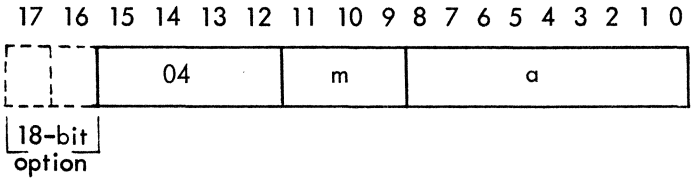


The contents of the B Register are placed in the effective memory location

Relative: Yes
Indexing: Yes
Indirect Addressing: Yes
Registers Altered: Memory

3.2.1.2 Arithmetic instruction group. The following paragraphs provide the mnemonic, description, and timing for each instruction in the Arithmetic group. Figures 3-4 and 3-5 show the general flow for the Arithmetic instruction group.

INR Increment Memory and Replace Timing: 3 cycles



The contents of the effective memory location are incremented by one, mod 2^{16} (2^{18}).

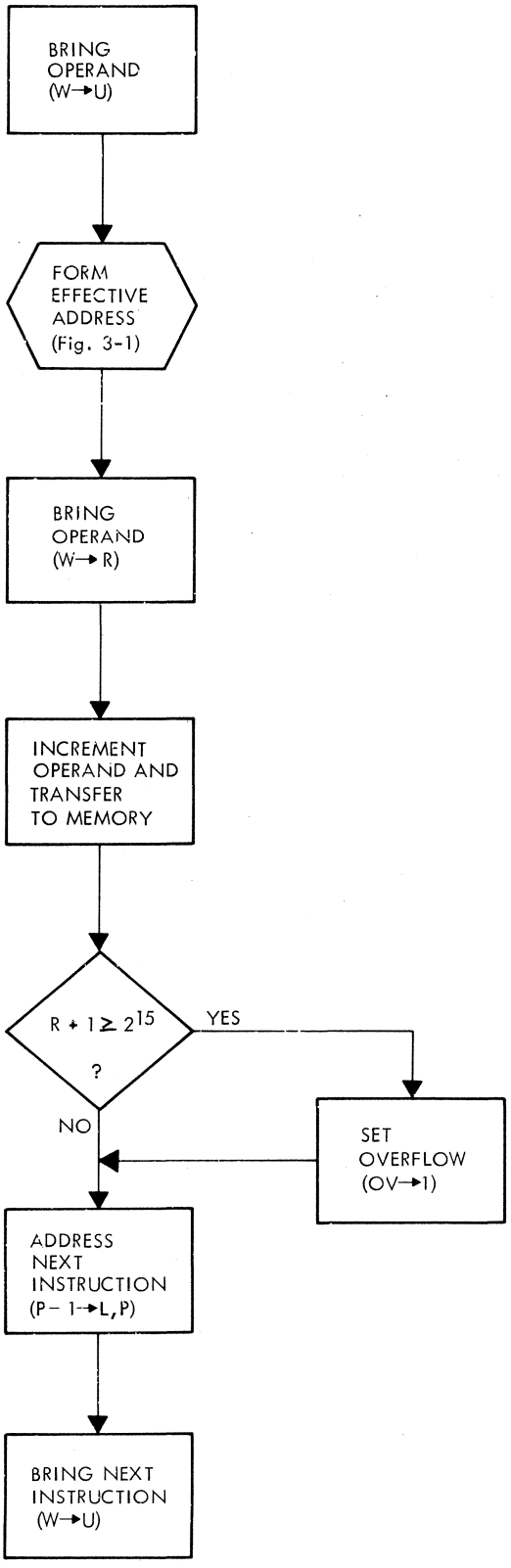


Fig. 3-4 Increment Memory and Replace Instruction, General Flow

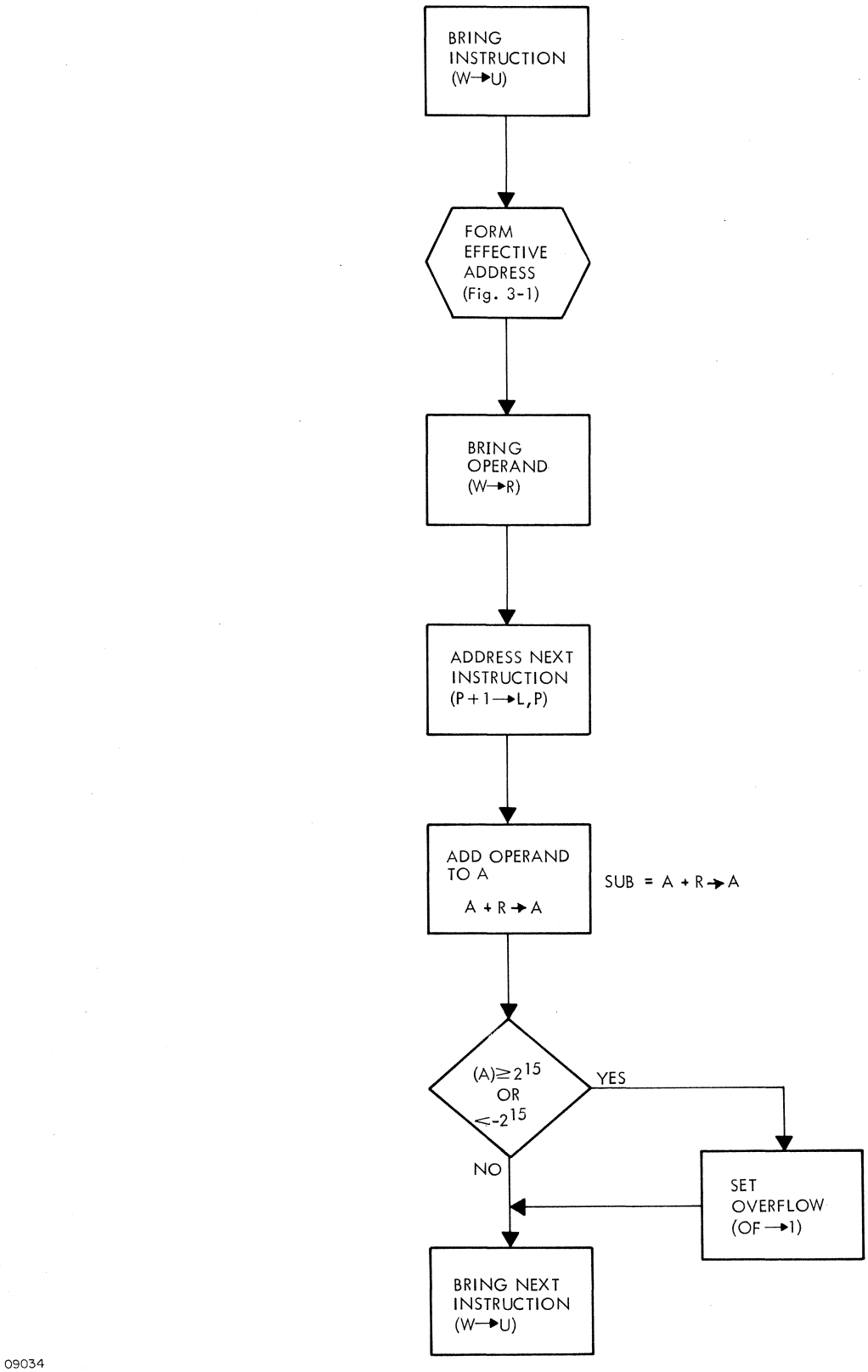
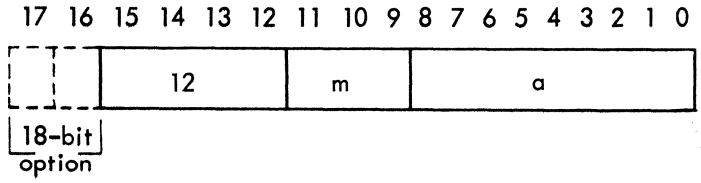


Fig. 3-5 Add Instruction, General Flow

After execution, if (M) $\geq 2^{15}$ (2^{17}), the overflow indicator, OF, is set.

Indexing: Yes
Indirect Addressing: Yes
Registers Altered: Memory, OF

ADD — Add Memory to A — Timing: 2 cycles

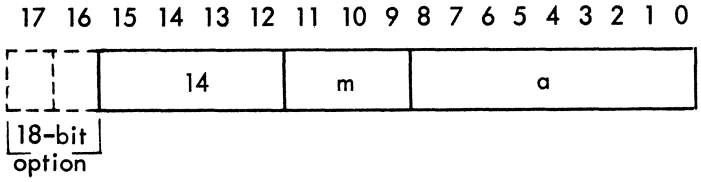


The contents of the effective memory location are added to the contents of the A Register and the sum is placed in the A Register.

After execution, if (A) $\geq 2^{15}$ (2^{17}) or $< -2^{15}$ (-2^{17}), the overflow indicator, OF, is set.

Indexing: Yes
Indirect Addressing: Yes
Registers Altered: A, OF

SUB — Subtract Memory from A — Timing: 2 cycles

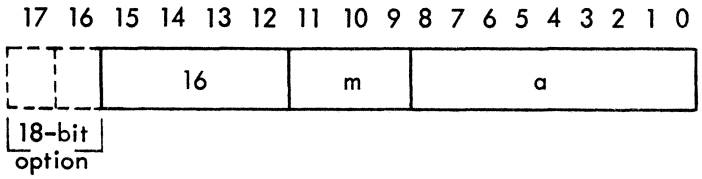


The contents of the effective memory location are subtracted from the A Register and the difference is placed in the A Register.

After execution, if (A) $\geq 2^{15}$ (2^{17}) or $< -2^{15}$ (-2^{17}), the overflow indicator, OF, is set.

Indexing: Yes
Indirect Addressing: Yes
Registers Altered: A, OF

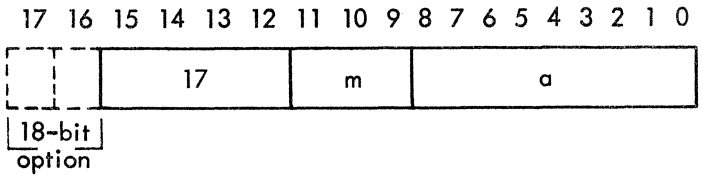
MUL — Multiply (optional) — Timing: 10 cycles (16 bits), 11 cycles (18 bits)



The contents of the B Register are multiplied by the contents of the effective memory location. The product is placed in the A and B Registers with the most-significant half of the product in the A Register, and the least-significant half in the B Register. The sign of the product is contained in the sign position of the A Register. The sign position of the B Register is set to zero.

Indexing: Yes
Indirect Addressing: Yes
Registers Altered: A, B

DIV — Divide (optional) — Timing: 10-14 cycles (16 bits), 11-16 cycles (18 bits)



The contents of the A and B Registers are divided by the contents of the effective memory location. The quotient is placed in the B Register and the remainder is placed in the A Register.

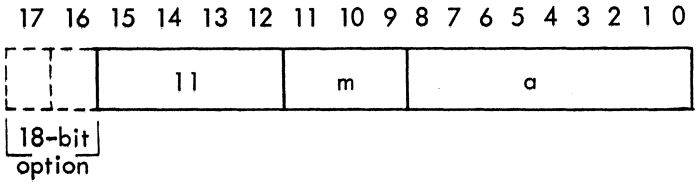
If $\frac{(A, B)}{M}$ 1,

overflow will not occur. If overflow does occur, the overflow indicator, OF, is set.

Indexing: Yes
Indirect Addressing: Yes
Registers Altered: A, B, OF

3.2.1.3 Logical instruction group. The following paragraphs provide the mnemonics, description, and timing for each instruction in the Logical Instruction Group.

ØRA — Inclusive-OR Memory and A — Timing: 2 cycles

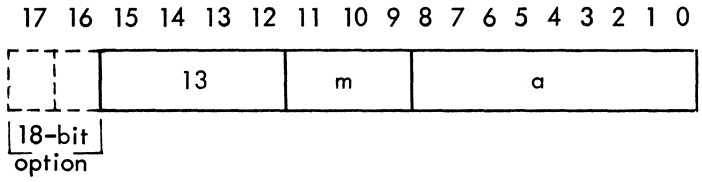


An Inclusive-OR operation is performed between the effective memory location and the A Register. The result is placed in the A Register. If either the effective memory location or A contain a "1" in the same bit position, a "1" is placed in the result. The truth table is shown below:

OPERATION		RESULT
Ai	Effective Memory Location (i)	Ai
0	0	0
0	1	1
1	0	1
1	1	1

Indexing: Yes
Indirect Addressing: Yes
Registers Altered: A

ERA — Exclusive-OR Memory and A — Timing: 2 cycles

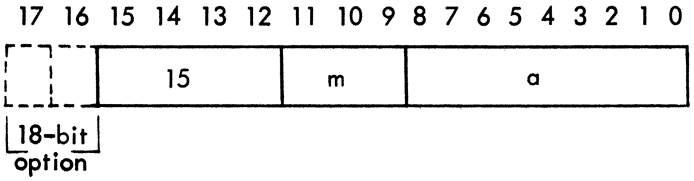


An Exclusive-OR operation is performed between the effective memory location and the A Register. The result is placed in the A Register. If the same bit position of the effective memory location and A contain a "0", or if both bit positions contain a "1", the result is zero. If the same bit position of the effective memory location and A are not equal; i.e., one contains a zero and the other a one, the result is a one. The truth table is shown below:

OPERATION		RESULT
Ai	Effective Memory Location (i)	Ai
0	0	0
0	1	1
1	0	1
1	1	0

Indexing: Yes
Indirect Addressing: Yes
Registers Altered: A

ANA — AND Memory and A — Timing: 2 cycles



The logical-AND is performed between the A Register and the contents of the effective memory location. The result is placed in the A Register. If the same bit position of both the effective memory location and A contain a one, the result is a one. The truth table for this follows.

OPERATION		RESULT
Ai	Effective Memory Location (i)	Ai
0	0	0
0	1	0
1	0	0
1	1	1

Indexing: Yes
Indirect Addressing: Yes
Registers Altered: A

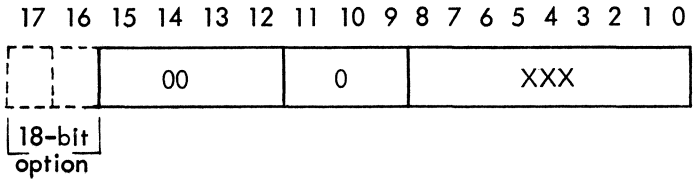
3.2.2 Single-Word Non-Addressing Instructions

The format of the single word non-addressing instruction class is shown in Figure 2-5.

A non-addressing single-word instruction includes the control group, the shift group, and the register change group. The operation is defined by the m field. The address field (a), as such, is not used by the control group instructions. For the shift group , the a field defines the type and number of shifts. For the register change group, the a field defines the type of transfer and the registers affected.

3.2.2.1 Control instruction group. The following paragraphs provide the menmonic, description, and timing for each instruction in the Control group. Table G2, Appendix G, summarizes the Control instructions.

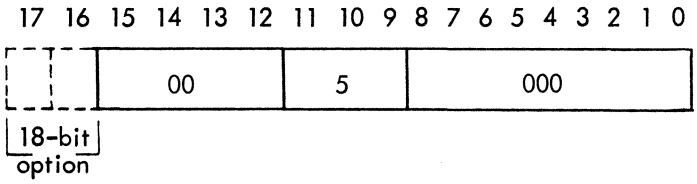
HLT Halt Timing: 1 cycle



When the computer executes the Halt instruction, computation is stopped and the computer is placed in the STEP mode. When the START button is pressed, computation starts with the next instruction in sequence.

Indexing: No
Indirect Addressing: No
Registers Altered: None

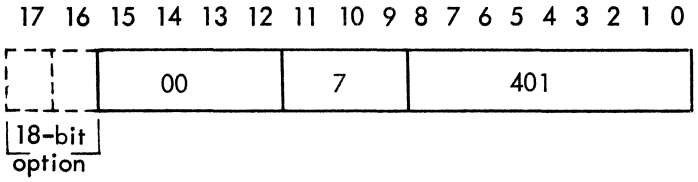
NØP No Operation Timing: 1 cycle



Execution of the NØP instruction does not affect the A, B, X Registers or Memory.

Indexing: No
Indirect Addressing: No
Registers Altered: None

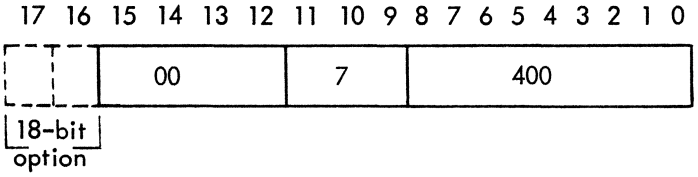
SØF — Set Overflow Indicator — Timing: 1 cycle



The overflow indicator, OF, is set to one.

Indexing: No
Indirect Addressing: No
Registers Altered: OF

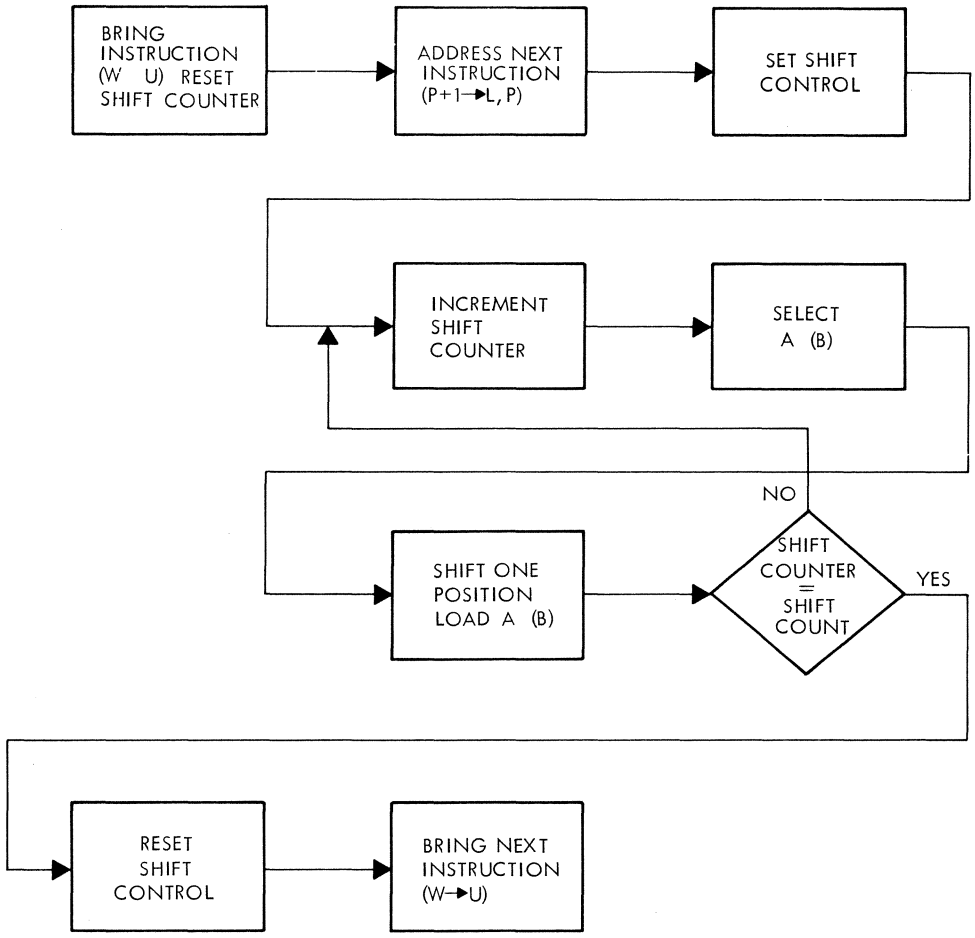
RØF — Reset Overflow Indicator — Timing: 1 cycle



The overflow indicator, OF, is reset to zero.

Indexing: No
Indirect Addressing: No
Registers Altered: OF

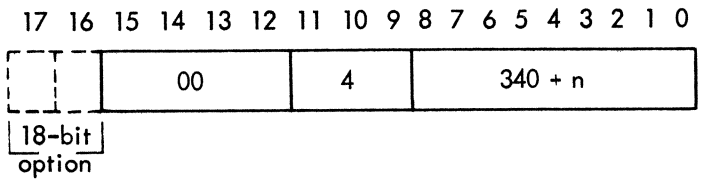
3.2.2.2 Shift instruction group. For shift instructions, the address field (a) defines the type of shift (bits 4-8) and the number of bit positions to be shifted (bits 0-4). The instruction format showing the use of each a-field bit is given in Table G3(a), Appendix G. Twelve of the possible sixteen shift operations defined by bits 4-8 are implemented. These are summarized in Table G3(b). Figure 3-6 shows the general flow for the shift instructions.



09035

Fig. 3-6 Single Register Shift Instruction, General Flow

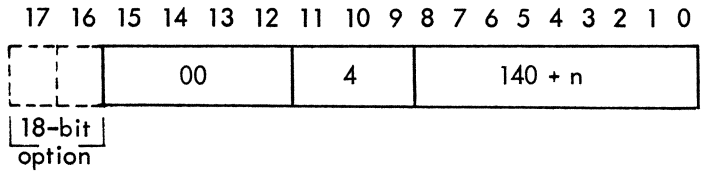
LSRA — Logical Shift A Right — Timing: 1 + 0.25 n cycles (n = number of shifts)



The contents of the A Register are shifted n places to the right (n = 0 to 37_8). Zeros are shifted into the high-order positions of the A Register. Information shifted out of the low-order position of the B Register is lost.

Indexing: No
Indirect Addressing: No
Registers Altered: A

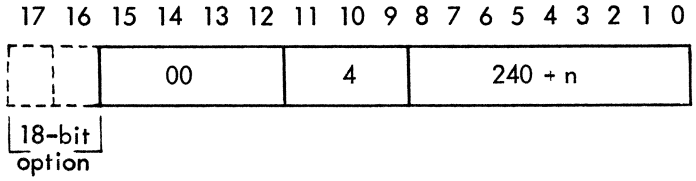
LSRB — Logical Shift B Right — Timing: 1 + 0.25 n cycles (n = number of shifts)



The contents of the B Register are shifted n places to the right (n = 0 to 37_8). Information shifted out of the low-order position of the B Register is lost. Zeros are shifted into the high-order position of the B Register.

Indexing: No
Indirect Addressing: No
Registers Altered: B

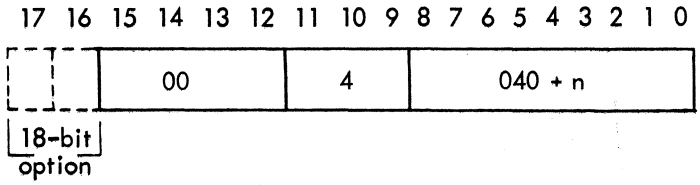
LRLA — Logical Rotate A Left — Timing: 1 + 0.25 n cycles (n = number of shifts)



The contents of the A Register are rotated left n places (n = 0 to 37_8). Bit position A_{15} (A_{17}) is rotated into bit position A_0.

Indexing: No
Indirect Addressing: No
Registers Altered: A

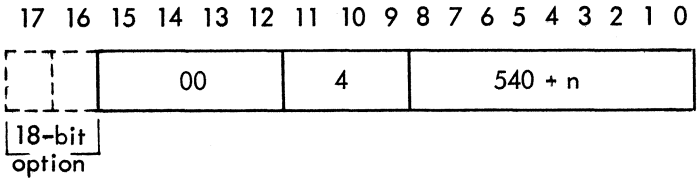
LRLB — Logical Rotate B Left — Timing: 1 + 0.25 n cycles (n = number of shifts)



The contents of the B Register are rotated n positions to the left (n = 0 to 37_8). Bit position B_{15} (B_{17}) is rotated into bit position B_0.

Indexing: No
Indirect Addressing: No
Registers Altered: B

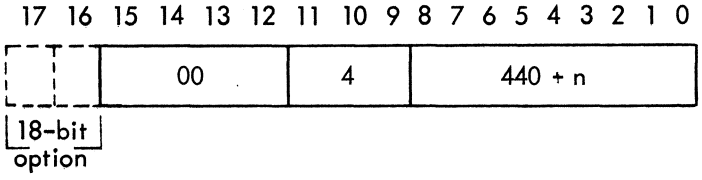
LLSR — Long Logical Shift Right — Timing: 1 + 0.50 n cycles (n = number of shifts)



The contents of the A, B Registers are shifted right n positions (n = 0 to 37_8). Bits shifted out of the low-order position of B are lost. Zeros are shifted into the high-order position of the A Register.

Indexing: No
Indirect Addressing: No
Registers Altered: A, B

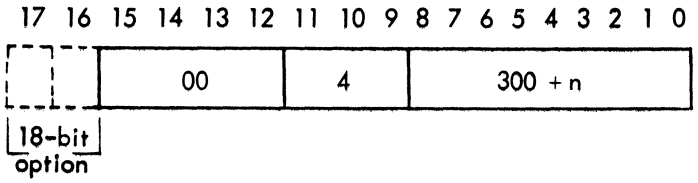
LLRL — Long Logical Rotate Left — Timing: 1 + 0.50 n cycles (n = number of shifts)



The contents of the A, B Registers are rotated n positions to the left (n = 0 to 37_8). Bit position A_{15} (A_{17}) is shifted into bit position B_0.

Indexing: No
Indirect Address: No
Registers Altered: A, B

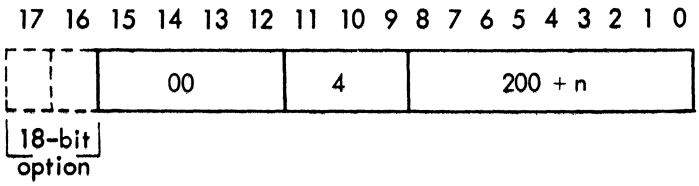
ASRA — Arithmetic Shift A Right — Timing: 1 + 0.25 n cycles (n = number of shifts)



The contents of the A Register are shifted n positions to the right (n = 0 to 37_8). Bits shifted out of the low-order position of A are lost. The sign bit of A, A_{15} (A_{17}) is extended n places to the right.

Indexing: No
Indirect Addressing: No
Registers Altered: A

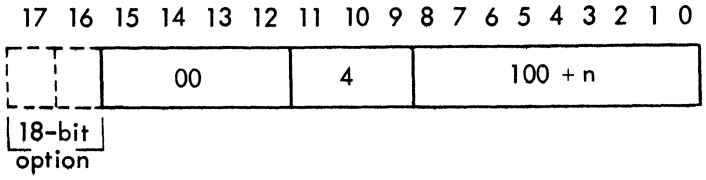
ASLA — Arithmetic Shift A Left — Timing: 1 + 0.25 n cycles (n = number of shifts)



The contents of the A Register are shifted n places to the left (n = 0 to 37_8). The sign bit, A_{15} (A_{17}), is retained and zeros are shifted into the low-order positions of A. Bits shifted out of A_{14} (A_{16}) are lost.

Indexing: No
Indirect Addressing: No
Registers Altered: A

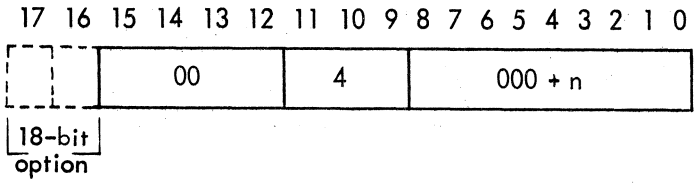
ASRB — Arithmetic Shift B Right — Timing: 1 + 0.25 n cycles (n = number of shifts)



The contents of the B Register are shifted n places to the right (n = 0 to 37_8). Information shifted out of the low-order position of B are lost. The sign bit of B, B_{15} (B_{17}) is extended n places to the right.

Indexing: No
Indirect Addressing: No
Register Altered: B

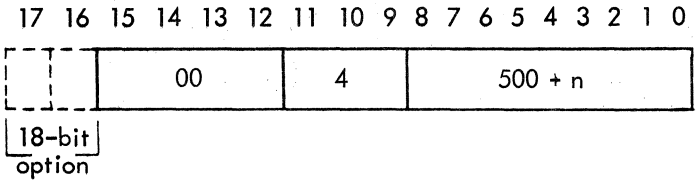
ASLB — Arithmetic Shift B Left — Timing: 1 + 0.25 n cycles (n = number of shifts)



The contents of the B Register are shifted n places to the left (n = 0 to 37_8). The sign bit of B, B_{15} (B_{17}), is retained and zeros are shifted into the low-order positions of B. Bits shifted out of B_{14} (B_{16}) are lost.

Indexing: No
Indirect Addressing: No
Registers Altered: B

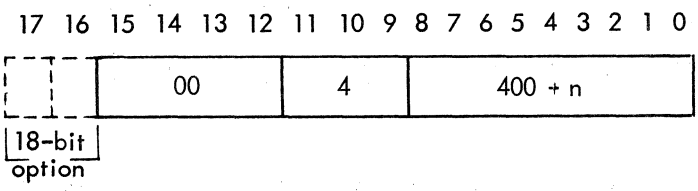
LASR — Long Arithmetic Shift Right — Timing: 1 + 0.50 n cycles (n = number of shifts)



The contents of the A, B Registers are shifted n places to the right (n = 0 to 37_8). Bit position A_0 is shifted into bit position $B_{14}(B_{16})$. The sign of the A Register, $A_{15}(A_{17})$, is extended n places to the right. The sign bit, $B_{15}(B_{17})$ of the B Register remains unchanged. Bits shifted out of the low-order position of the B Register are lost.

Indexing: No
Indirect Addressing: No
Registers Altered: A, B

LASL — Long Arithmetic Shift Left — Timing: 1 + 0.50 n cycles (n = number of shifts



The contents of the A, B Registers are shifted n places to the left (n = 0 to 37_8). Bit position $B_{14}(B_{16})$ is shifted into bit position A_0, with the sign of B, $B_{15}(B_{17})$ remaining unchanged. The sign of the A Register, $A_{15}(A_{17})$ is not altered. Information shifted out of $A_{14}(A_{16})$ is lost and zeros are shifted into the low-order positions of the B Register.

Indexing: No
Indirect Addressing: No
Registers Altered: A, B

3.2.2.3 Register Change Group. The register change instruction group provides a macro-operation facility, in that these instructions may combine several register change operations in a single instruction. The instruction format is shown in Fig. 3-7.

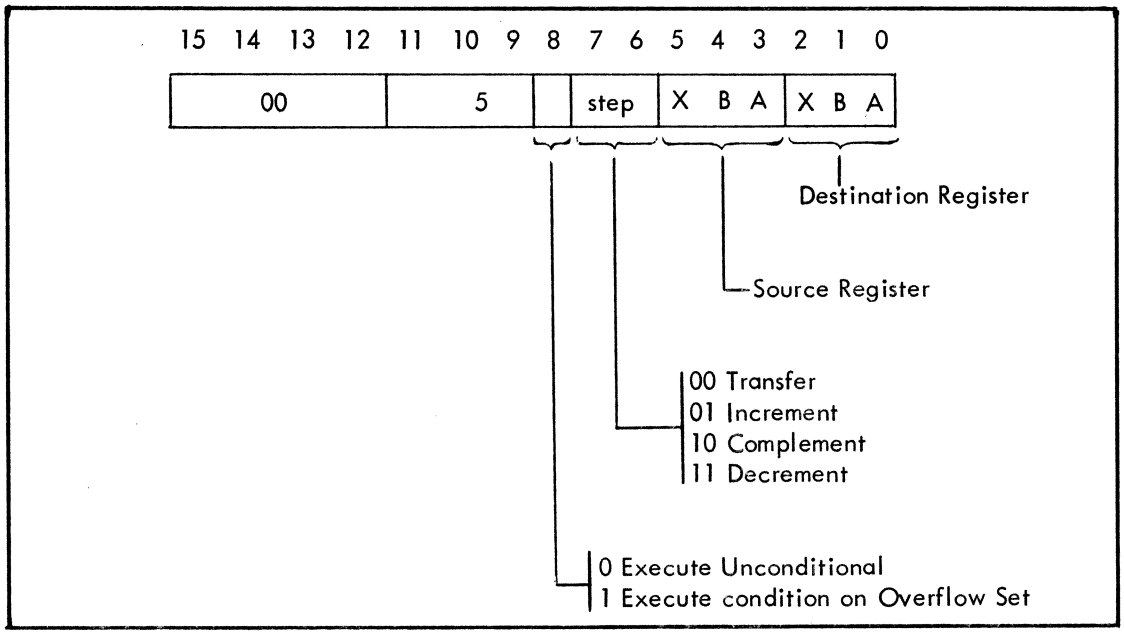
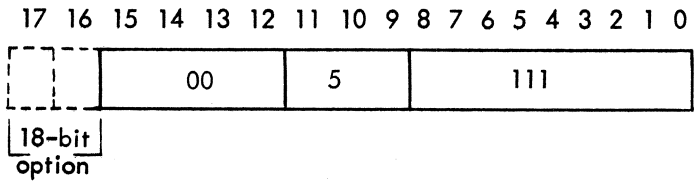


Fig. 3-7 Register Change Instruction

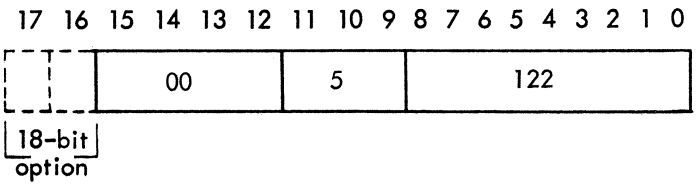
The address field a defines the source and destination of a parallel word transfer within the operational register set A, B, and X. Any combination of registers may be selected. The a field also specifies whether the word transferred will be unchanged, incremented, decremented, or complemented. The transfer may also be conditional on the overflow indicator.

Table G4(a), in Appendix G, defines the transfer control specified by the a field. If more than one source register is specified, the result will be the inclusive-OR of the group. Complementing causes transfer of the complement of the inclusive-OR (NOR) of a combination of source registers. A total of 512 different register change operations are possible. The most useful instructions are contained in the mnemonic repertoire recognized by the DAS assembler, summarized in Table G4(b), Appendix G.

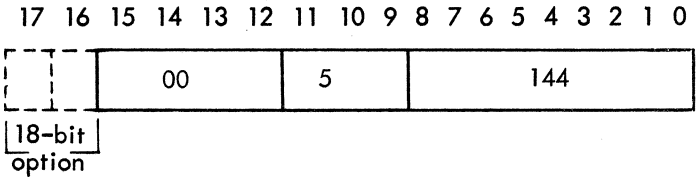
IAR — Increment A Register — Timing: 1 Cycle



IBR — Increment B Register — Timing: 1 Cycle



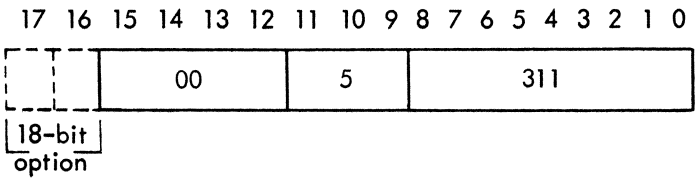
IXR — Increment X Register — Timing: 1 Cycle



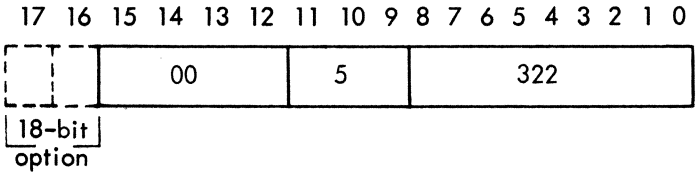
The contents of the A (B, X) Register are incremented, by one mod 2^{16} (2^{18}). If the sign of A (B, X) changes from plus to minus, the overflow indicator OF is set.

Indexing: No
Indirect Addressing: No
Registers Altered: A (B, X), OF

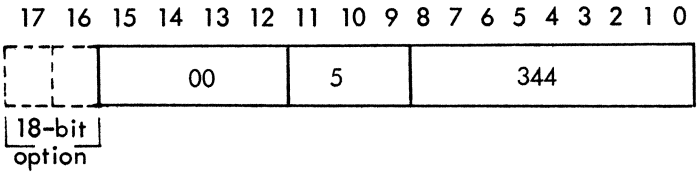
DAR Decrement A Register Timing: 1 Cycle



DBR Decrement B Register Timing: 1 Cycle



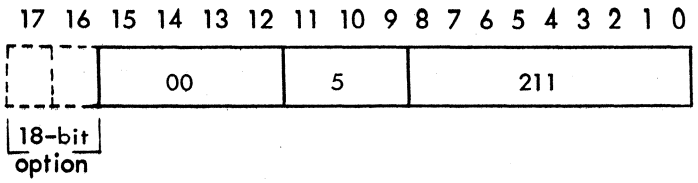
DXR Decrement X Register Timing: 1 Cycle



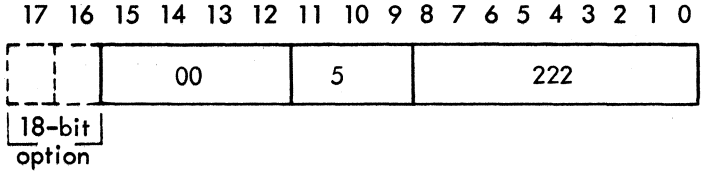
The contents of the A (B, X) Register are decremented by one mod 2^{16} (2^{18}). If the sign bit of the A (B, X) Register is changed from minus to plus, the overflow indicator, OF, is set.

Indexing: No
Indirect Addressing: No
Registers Altered: A (B, X), OF

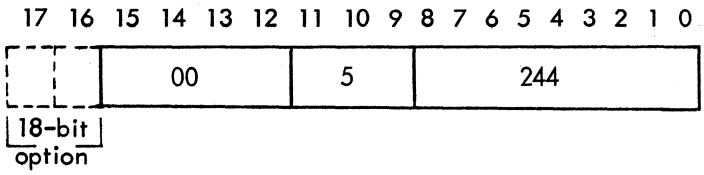
CPA — Complement A Register — Timing: 1 Cycle



CPB — Complement B Register — Timing: 1 Cycle



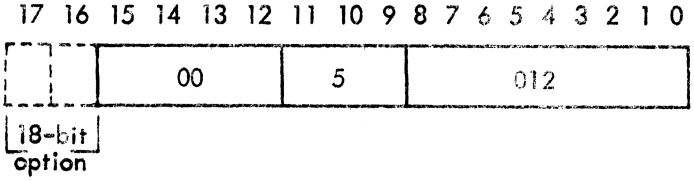
CPX — Complement X Register — Timing: 1 Cycle



The contents of the A (B, X) Register are complemented (1's-complement).

Indexing: No
Indirect Addressing: No
Register Altered: A (B, X)

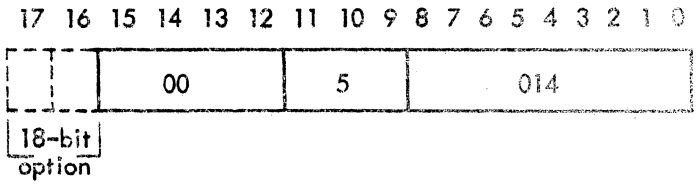
TAB — Transfer A Register to B Register — Timing: 1 Cycle



The contents of the A Register are placed in the B Register.

Indexing: No
Indirect Addressing: No
Registers Altered: B

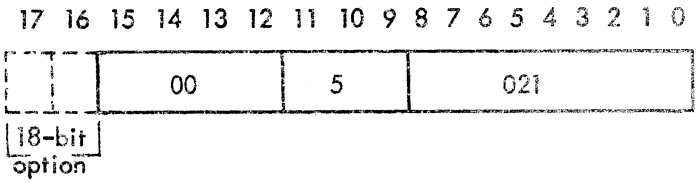
TAX — Transfer A Register to X Register — Timing: 1 Cycle



The contents of the A Register are placed in the X Register.

Indexing: No
Indirect Addressing: No
Registers Altered: X

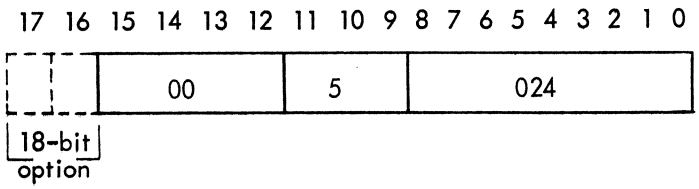
TBA — Transfer B Register to A Register — Timing: 1 Cycle



The contents of the B Register are placed in the A Register.

Indexing: No
Indirect Addressing: No
Registers Altered: A

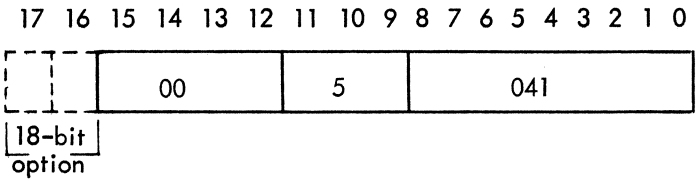
TBX — Transfer B Register to X Register — Timing: 1 Cycle



The contents of the B Register are placed in the X Register

Indexing: No
Indirect Addressing: No
Registers Altered: X

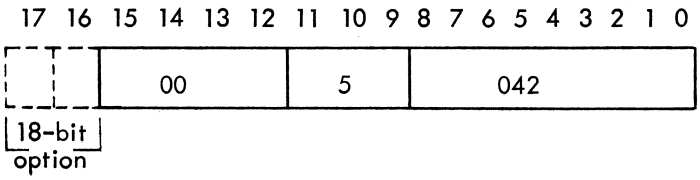
TXA — Transfer X Register to A Register — Timing: 1 Cycle



The contents of the X Register are placed in the A Register.

Indexing: No
Indirect Addressing: No
Registers Altered: A

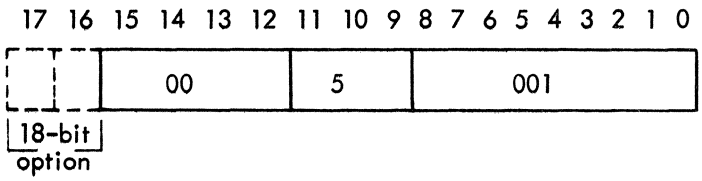
TXB — Transfer X Register to B Register — Timing: 1 Cycle



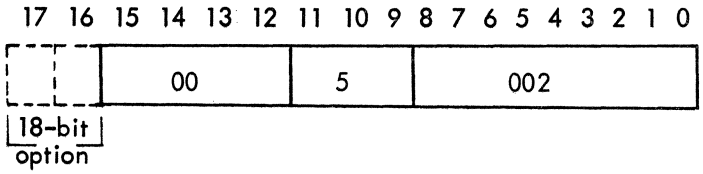
The contents of the X Register are placed in the B Register

Indexing: No
Indirect Addressing: No
Registers Altered: B

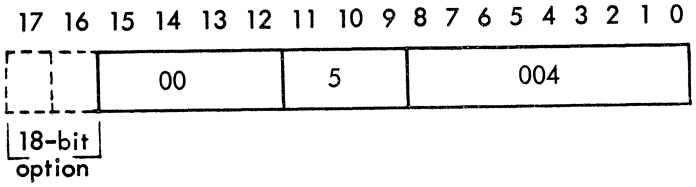
TZA — Transfer Zero to A Register — Timing: 1 Cycle



TZB — Transfer Zero to B Register — Timing: 1 Cycle



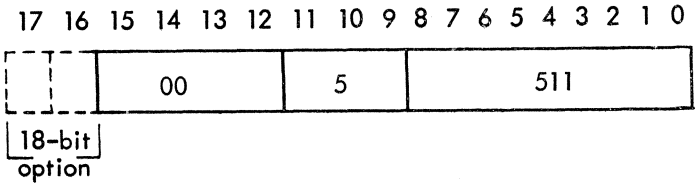
TZX — Transfer Zero to X Register — Timing: 1 Cycle



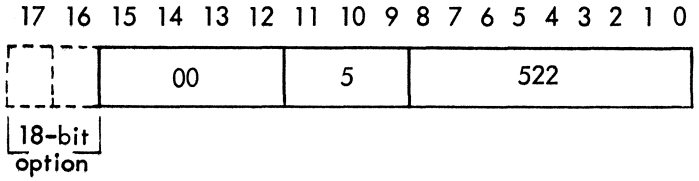
The A (B, X) Register is cleared to zero.

Indexing: No
Indirect Addressing: No
Registers Altered: A (B, X)

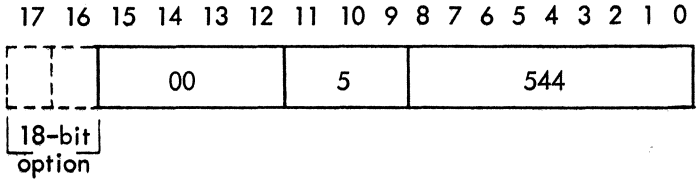
AØFA — Add Overflow to A Register — Timing: 1 Cycle



AØFB Add Overflow to B Register Timing: 1 cycle



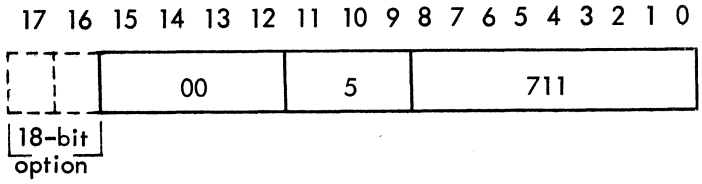
AØFX Add Overflow to X Register Timing: 1 cycle



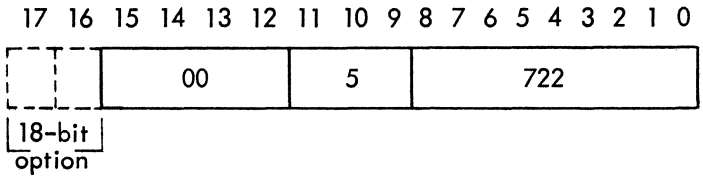
The contents of the overflow indicator, OF, are added to the A (B, X) Register, mod 2^{16} (2^{18}). The sum is placed in the A (B, X) Register. The overflow flip-flop does not change.

Indexing: No
Indirect Addressing: No
Registers Altered: A (B, X)

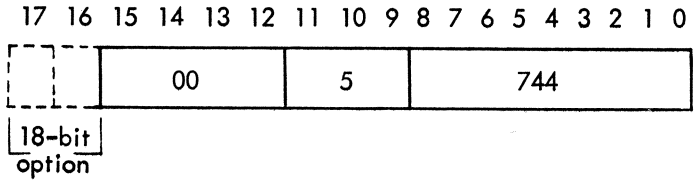
SØFA Subtract Overflow from A Register Timing: 1 cycle



SØFB Subtract Overflow from B Register Timing: 1 cycle



SØFX Subtract Overflow from X Register Timing: 1 cycle



The contents of the Overflow indicator, OF, are subtracted from the A (B,X) Register, mod 2^{16} (2^{18}). The Overflow flip-flop does not change.

Indexing: No
Indirect Addressing: No
Registers Altered: A (B,X)

3.3 DOUBLE-WORD INSTRUCTIONS

Double-word instructions may be either addressing or non-addressing. The instructions of the double-word addressing group are:

Jump
Jump-and-Mark
Execute
Extended Addressing (optional)
Byte (optional)

The instruction in the double-word non-addressing group is:

Immediate

3.3.1 Double-Word Addressing Instructions

For double-word addressing instructions, the second word is contained in the memory location following the instruction word. The second word may contain an operand or an address. The address may be either indirect or direct. The general flow chart for double-word instructions is shown in Figure 3-8.

Bits 0 through 8 determine the conditions for execution of the instruction. The condition is tested if the corresponding bit is equal to one. For example, if bit 0 equals 1, the instruction will examine the status of the Overflow flip-flop. If Overflow is set, the command will be executed. If Overflow is not set, the next instruction in sequence will be executed.

3.3.1.1 Jump Instruction Group. For the jump instruction group, the address field a contains a set of nine flags which define the logical conditions for execution of the jump function. The jump address is contained in the second word of the double-word instruction. Table G-5(a), in Appendix G, summarizes the logical condition associated with each bit in the address field. The jump condition is the logical-AND of all ones in the field. Thus, there are 512 possible combinations but

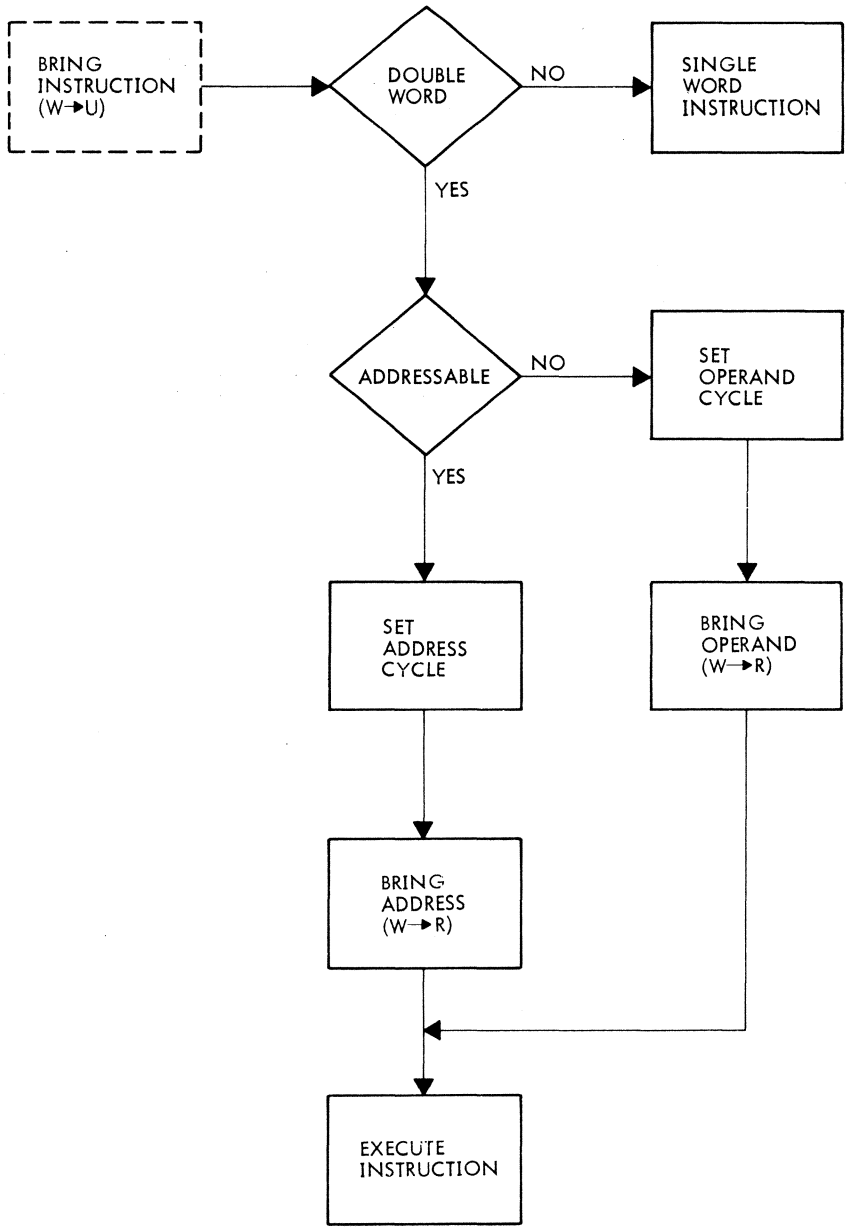


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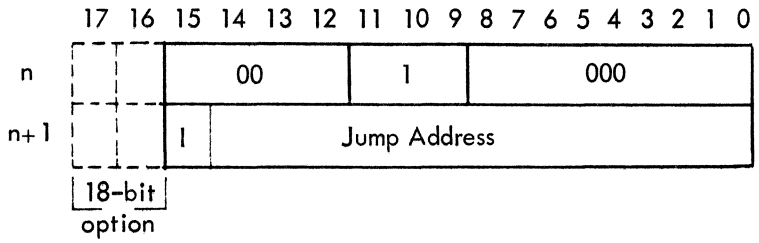
Fig. 3-8 Double Word Instruction, General Flow

not all are useful. The most useful conditional jump instructions are contained in the mnemonic instruction repertoire recognized by the DAS assembler, summarized in Table G-5(b). The general flow for jump instruction is shown in Figure 3-9.

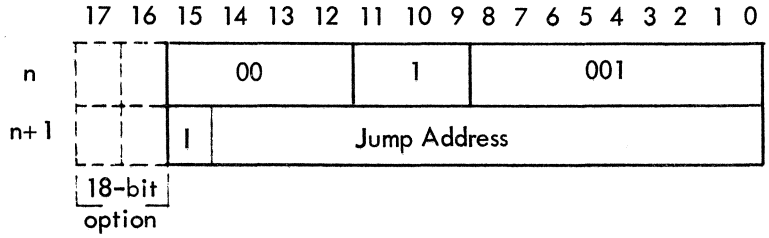
JMP — Jump Unconditionally — Timing: 2 cycles



The next instruction executed is at the Jump Address.

Indexing: No
Indirect Addressing: Yes
Registers Altered: P

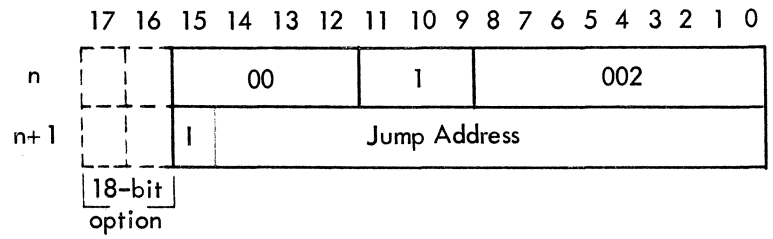
JØF — Jump if Overflow Indicator Set — Timing: 2 cycles



If the Overflow indicator, OF, is set, the next instruction executed is at the Jump Address. If the Overflow indicator is not set, the next instruction in sequence is executed. The Overflow indicator is reset upon execution of the JØF instruction.

Indexing: No
Indirect Addressing: Yes
Registers Altered: OF (reset), P

JAP — Jump if A Register Positive — Timing: 2 cycles



If the contents of the A Register are positive or zero, the next instruction executed is at the Jump Address. If the A Register is negative, the next instruction is sequence is executed.

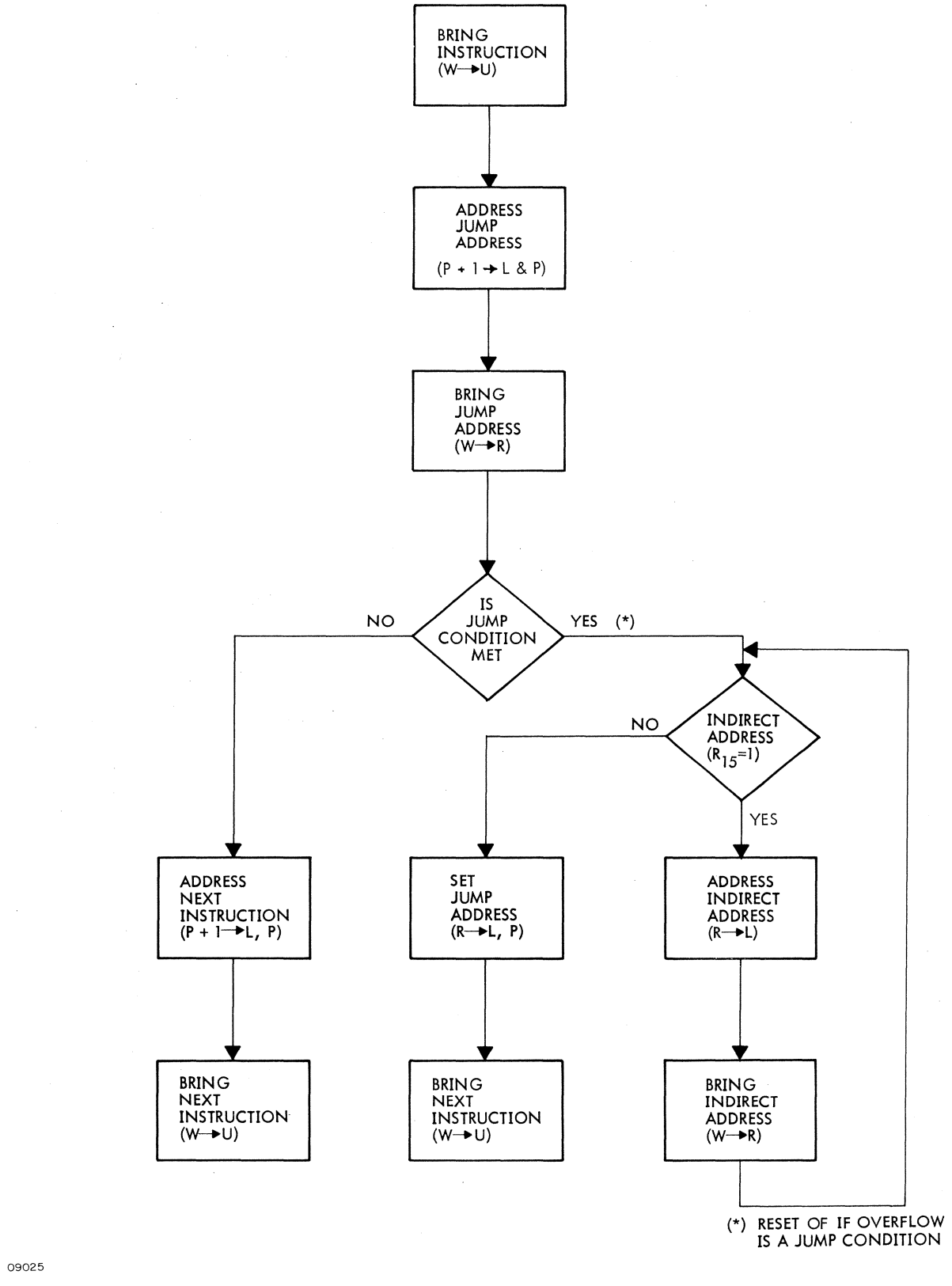
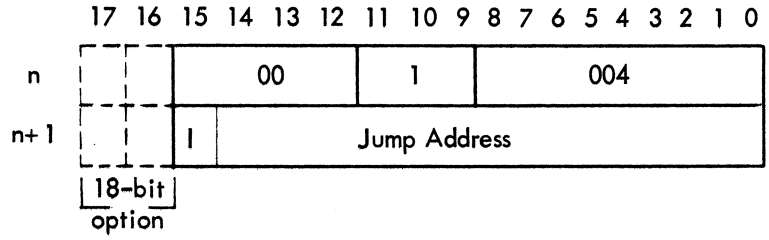


Fig. 3-9 Jump Instruction, General Flow

Indexing: No
Indirect Addressing: Yes
Registers Altered: P

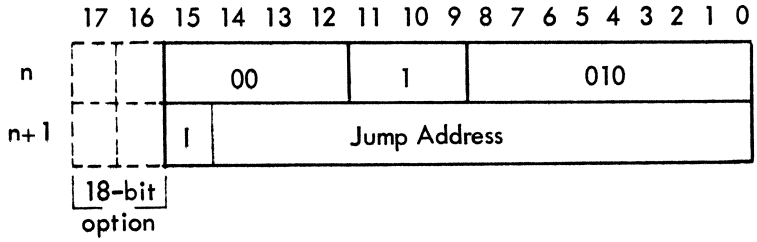
JAN — Jump if A Register Negative — Timing: 2 cycles



If the A Register is negative, the next instruction executed is at the Jump Address. If the A Register is positive, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: P

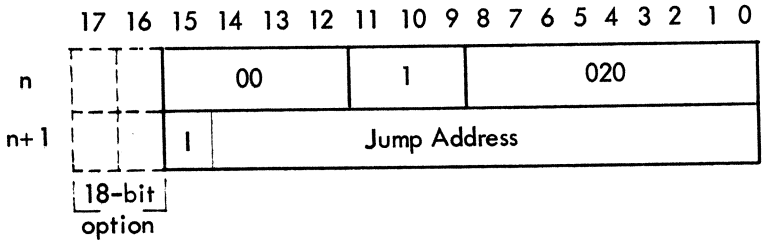
JAZ — Jump if A Register Zero — Timing: 2 Cycles



If the A Register is zero, the next instruction executed is at the Jump Address. If the A Register is not zero, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: P

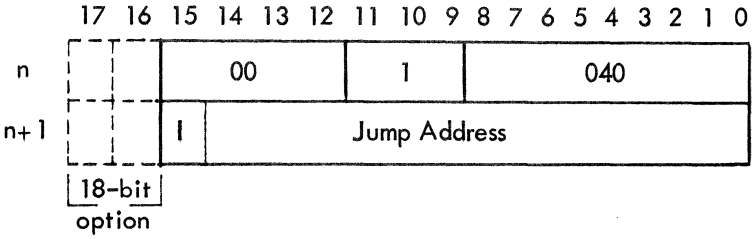
JBZ — Jump if B Register Zero — Timing: 2 Cycles



If the B Register is zero, the next instruction executed is at the Jump Address. If the B Register is not zero, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: P

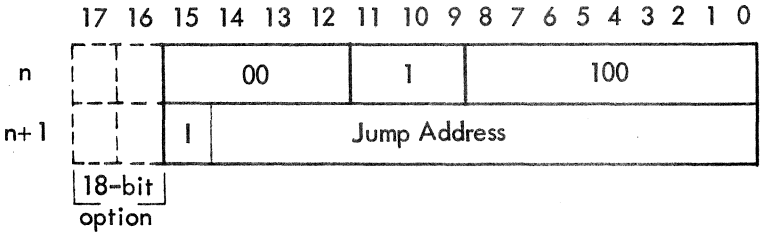
JXZ — Jump if X Register Zero — Timing: 2 Cycles



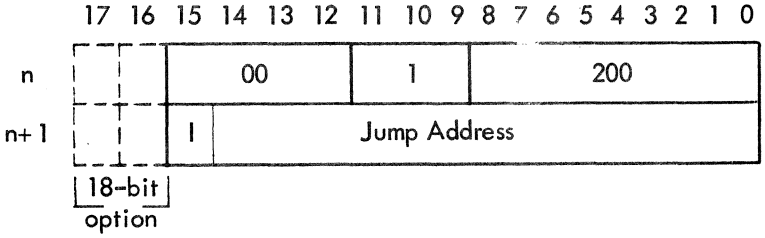
If the Index Register X is zero, the next instruction executed is at the Jump Address. If the Register is not zero, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: P

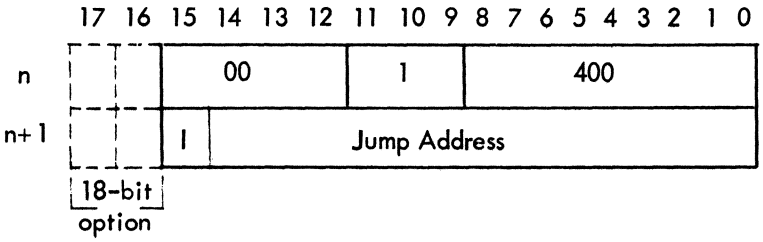
JSS1 — Jump if Sense Switch 1 Set — Timing: 2 Cycles



JSS2 — Jump if Sense Switch 2 Set — Timing: 2 Cycles



JSS3 Jump if Sense Switch 3 Set Timing: 2 Cycles

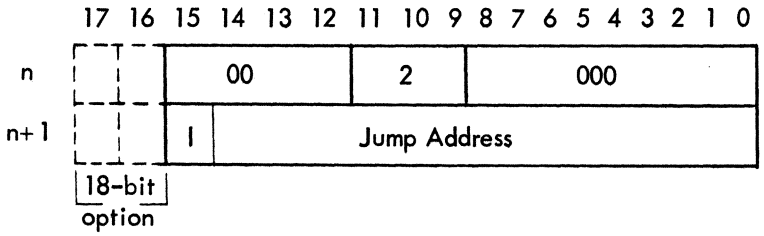


If Sense Switch 1 (2, 3) is set, the next instruction executed is at the Jump Address. If the Sense Switch being tested is not set, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: P

3.3.1.2 Jump and Mark Instruction Group. For the Jump and Mark group of instructions, the address field a defines the same set of logical conditions specified for the Jump group. These conditions are summarized in Table G6(a) in Appendix G. Thus, there are 512 possible combinations, but not all are useful. The most convenient instructions are contained in the mnemonic instruction repertoire recognized by the DAS assembler. These are summarized in Table G6(b).

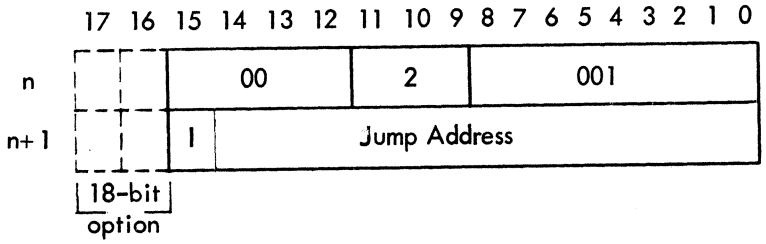
JMPM Jump and Mark Unconditionally Timing: 3 Cycles



The contents of the instruction counter, P, are stored at the Jump Address. The next instruction executed is at the Jump Address plus one.

Indexing: No
Indirect Addressing: Yes
Registers Altered: Jump Address, P

JØFM Jump and Mark if Overflow Set Timing: 3 Cycles



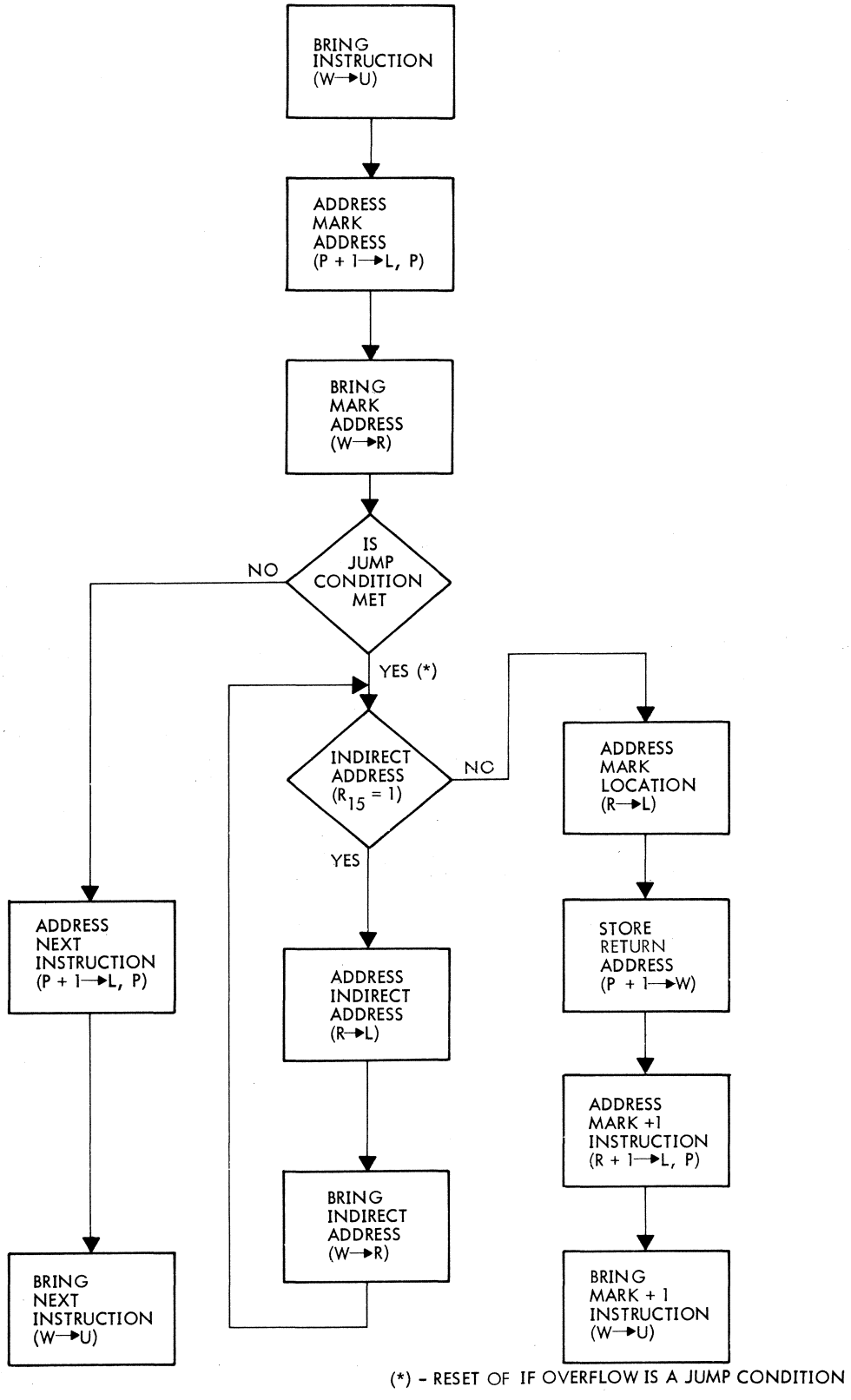
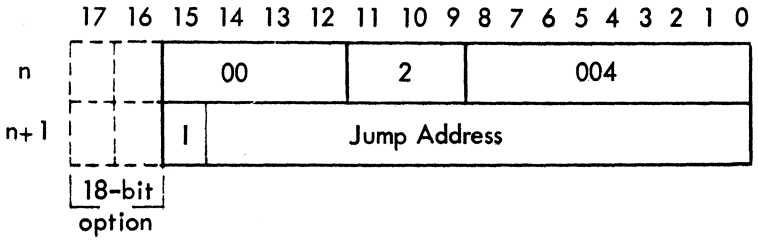


Fig. 3-10 Jump-and-Mark Instruction, General Flow

If the overflow indicator, OF, is set, the contents of the instruction counter (P) are stored at the Jump Address, and the instruction at the Jump Address-plus-one is executed. If the overflow indicator is not set, the next instruction in sequence is executed. The overflow indicator is reset upon execution of the JOFM instruction.

Indexing: No
Indirect Addressing: Yes
Registers Altered: Jump Address, P, OF (reset)

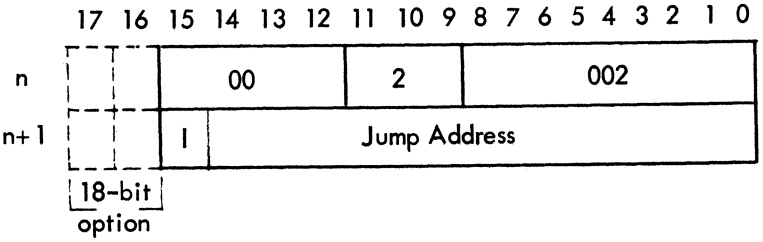
JANM — Jump and Mark if A Register Negative — Timing: 3 Cycles



If the A Register is negative, the contents of the instruction counter (P) are placed at the Jump Address, and the instruction at the Jump Address plus one is executed. If the A Register is positive, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: Jump Address, P

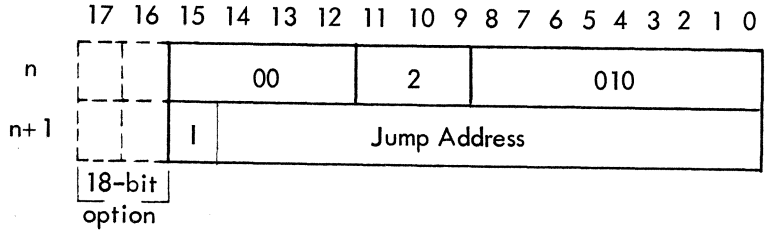
JAPM — Jump and Mark if A Register Positive — Timing: 3 Cycles



If the A Register is positive or zero, the contents of the instruction counter (P) are placed at the Jump Address, and the instruction at the Jump Address plus one is executed. If the A Register is negative, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: Jump Address, P

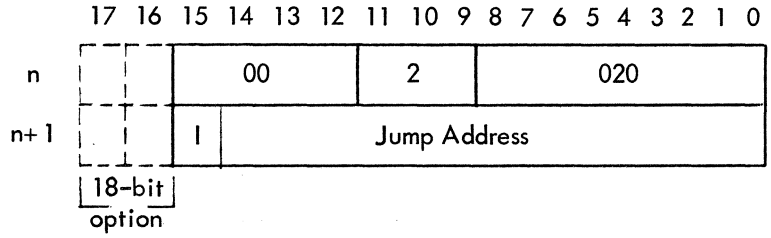
JAZM Jump and Mark if A Register Zero Timing: 3 Cycles



If the A Register is zero, the instruction counter (P) is placed at the Jump Address and the instruction at the Jump Address plus one is executed. If the A Register is not zero, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: Jump Address, P

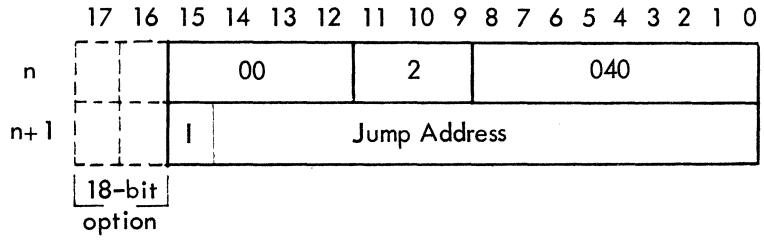
JBZM Jump and Mark if B Register Zero Timing: 3 Cycles



If the B Register is zero, the contents of the instruction counter (P) are placed at the Jump Address, and the instruction at the Jump Address plus one is executed. If the B Register is not zero, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: Jump Address, P

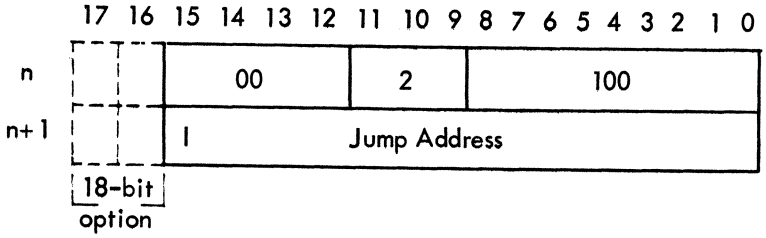
JXZM Jump and Mark if X Register Zero Timing: 3 Cycles



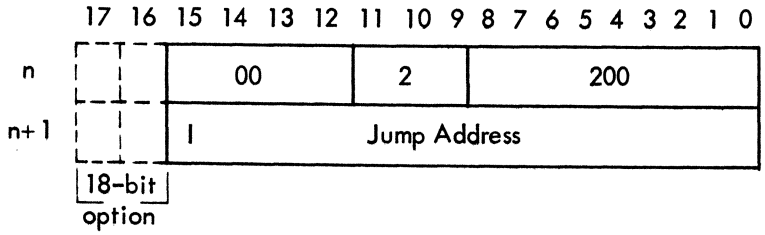
If the X Register is zero, the contents of the instruction counter (P) are placed at the Jump Address, and the instruction at the Jump Address plus one is executed. If the X Register is not zero, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: Jump Address, P

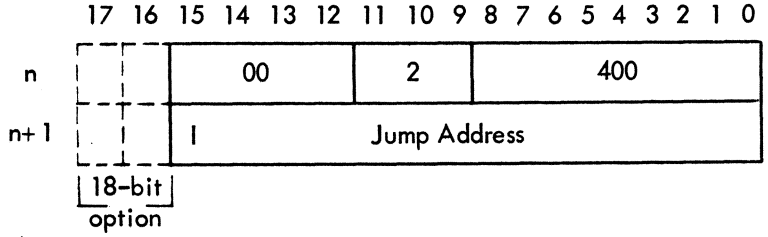
JS1M — Jump and Mark if Sense Switch 1 Set — Timing: 3 Cycles



JS2M — Jump and Mark if Sense Switch 2 Set — Timing: 3 Cycles



JS3M — Jump and Mark if Sense Switch 3 Set — Timing: 3 Cycles



If Sense Switch 1 (2, 3) is set, the instruction counter (P) is placed at the Jump Address, and the instruction at the Jump Address plus one is executed. If the tested Sense Switch is not set, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: Jump Address, P

3.3.1.3 Execute Instruction Group. For the Execute group of instructions, the address field a contains a set of nine flags which define the logical conditions for executing an instruction contained at the effective execution address. The execution address is contained in the second word of the double-word instruction. Table G7(a), Appendix G, summarizes the logical conditions associated with each bit in the address field. The execute condition is the logical-AND of all "1's" in the a field. The most useful of the 512 possible execute instructions are contained in the mnemonic instruction repertoire recognized by the DAS assembler, summarized in Table G7(b). Figure 3-11

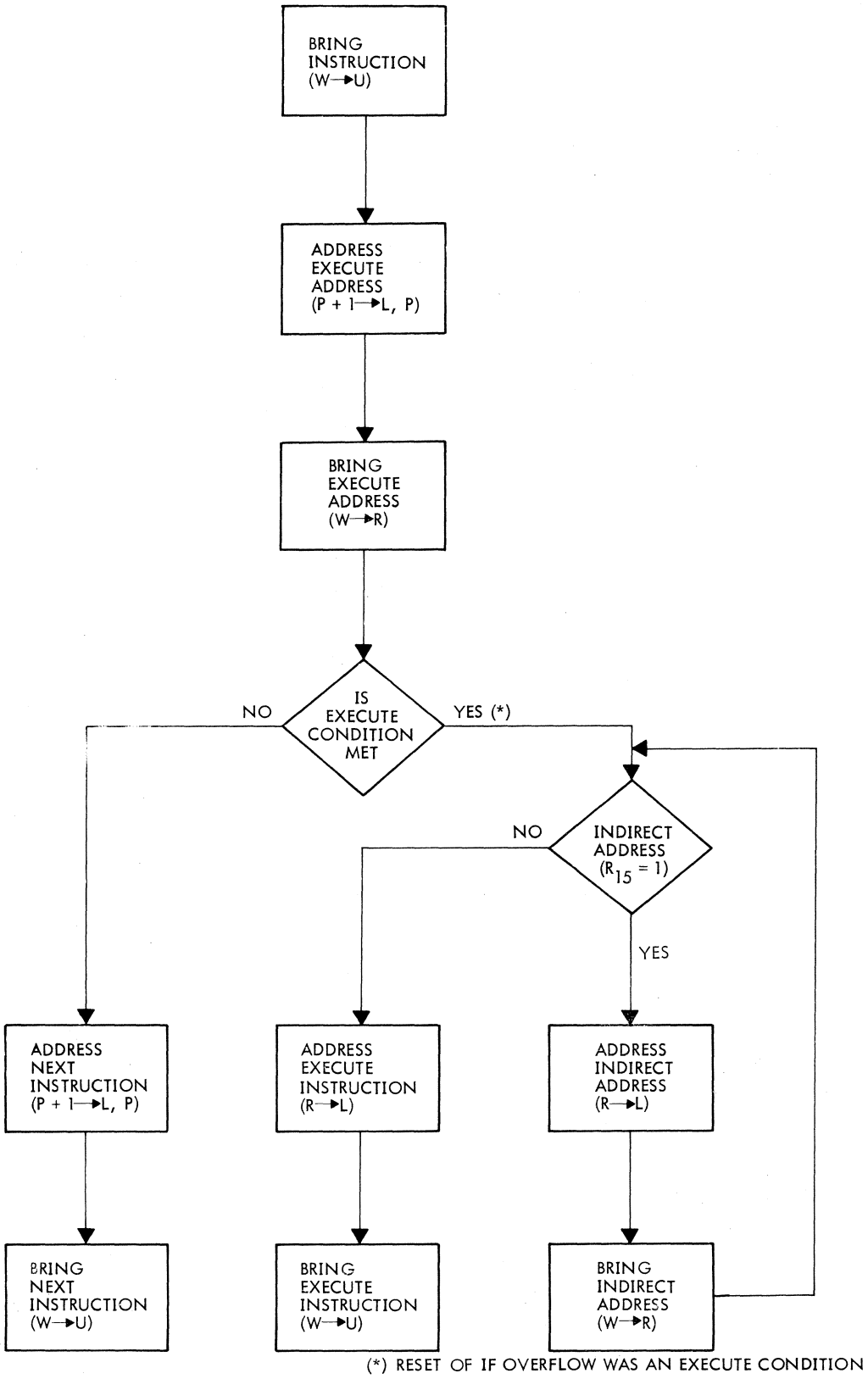


Fig. 3-11 Execute Instruction, General Flow

illustrates the general flow for the execute instructions.

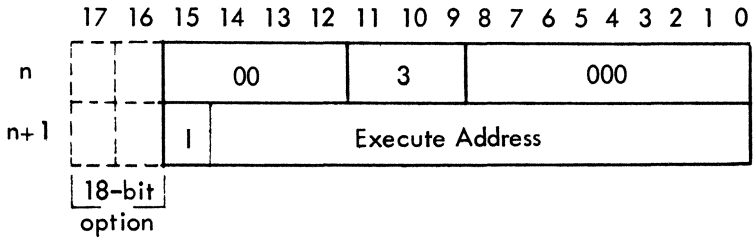
It is important to note that only single-word instructions should be executed. The single-word instruction groups are:

LOAD/STORE
ARITHMETIC
LOGICAL
CONTROL
SHIFT
REGISTER CHANGE

If the execute is attempted on double-word instructions, erroneous operation will occur. The double-word instruction groups are:

JUMP
JUMP AND MARK
EXECUTE
EXTENDED ADDRESSING
BYTE (optional)
IMMEDIATE

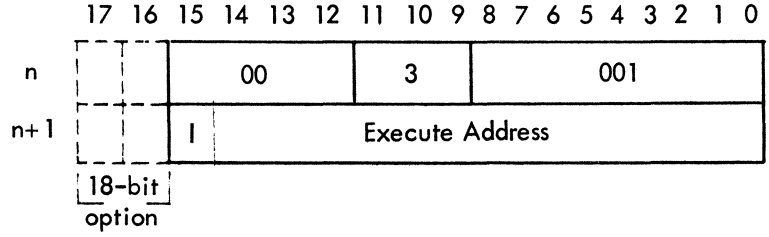
XEC — Execute Unconditionally — Timing: 2 Cycles



The instruction located at the Execute Address is executed and then the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: None

XØF — Execute if Overflow Set — Timing: 2 Cycles

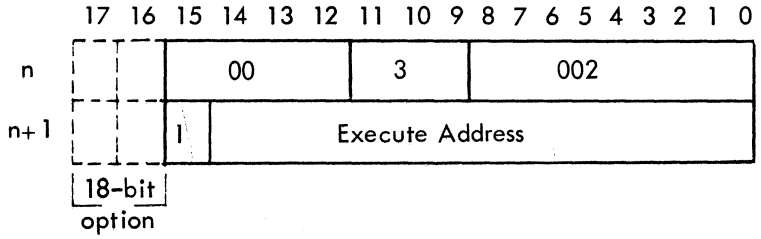


If the overflow indicator OF is set, the instruction at the Execute Address is executed, and then the next instruction in sequence is executed.

If the overflow indicator is not set, the next instruction in sequence is executed. Execution of the XØF instruction resets the overflow indicator.

Indexing: No
Indirect Addressing: Yes
Registers Altered: OF (reset)

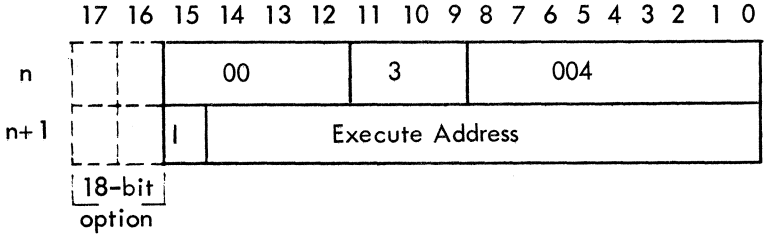
XAP — Execute if A Register Positive — Timing: 2 Cycles



If the A Register is positive or zero, the instruction at Execute Address is executed, and then the next instruction in sequence is executed. If the A Register is negative, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: None

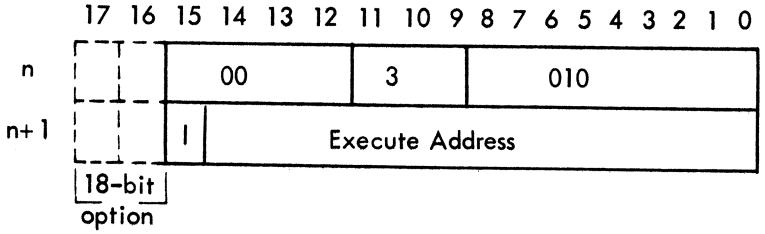
XAN — Execute if A Register Negative — Timing: 2 Cycles



If the A Register is negative, the instruction at the Execute Address is executed, and then the next instruction in sequence is executed. If the A Register is positive, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: None

XAZ — Execute if A Register Zero — Timing: 2 Cycles

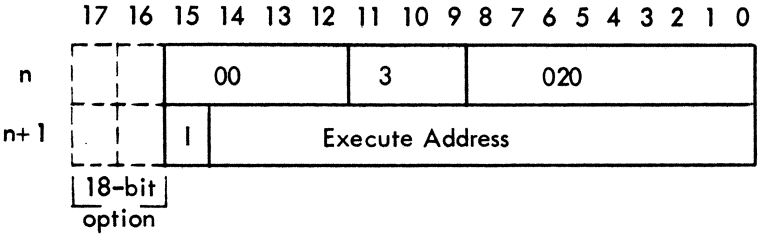


If the A Register is zero, the instruction at the Execute Address is executed, and then the next instruction in sequence is executed.

If the A Register is not zero the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: None

XBZ — Execute if B Register Zero — Timing: 2 Cycles

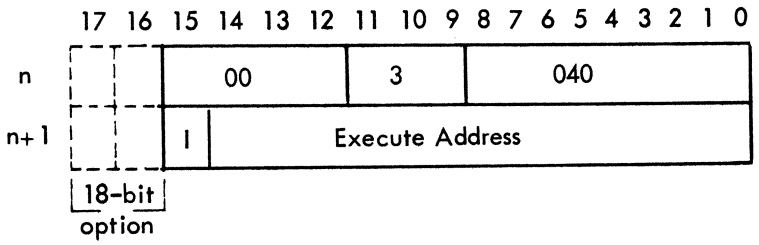


If the B Register is zero, the instruction at the Execute Address is executed, and then the next instruction in sequence is executed.

If the B Register is not zero, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: None

XXZ — Execute if X Register Zero — Timing: 2 Cycles

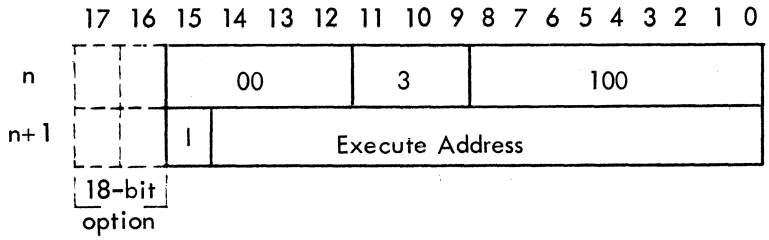


If the Index Register (X) is zero, the instruction at the Execute Address is executed, and then the next instruction in sequence is executed.

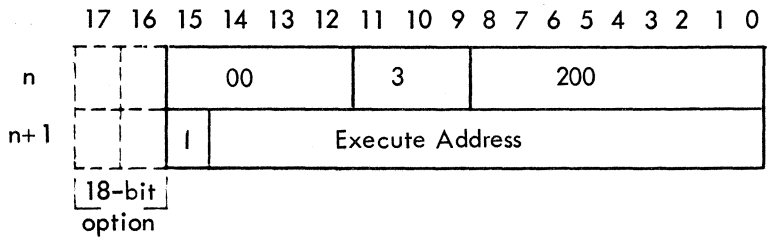
If the Index Register is not zero, the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: None

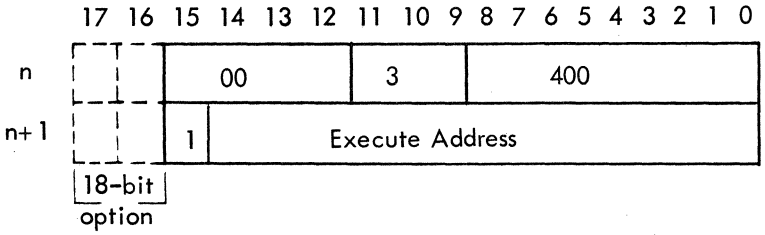
XSI — Execute if Sense Switch 1 — Timing: 2 Cycles



XS2 — Execute if Sense Switch 2 — Timing: 2 Cycles



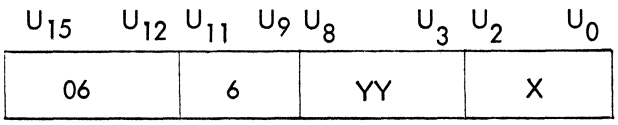
XS3 — Execute if Sense Switch 3 — Timing: 2 Cycles



If Sense Switch -1, (2, 3) is set, the instruction at the Execute Address is executed and then the next instruction in the sequence is executed. If the Sense Switch tested is not set, the next instruction is executed.

Indexing: No
Indirect Addressing: Yes
Registers Altered: None

3.3.1.4 Extended Addressing Instruction Group (optional). The Extended Address Mode instructions are similar in format to the Immediate Instructions. However, the second word of the double-word instruction contains the effective address. The address can be indirect or direct. It is determined by bit 15 of the second word.

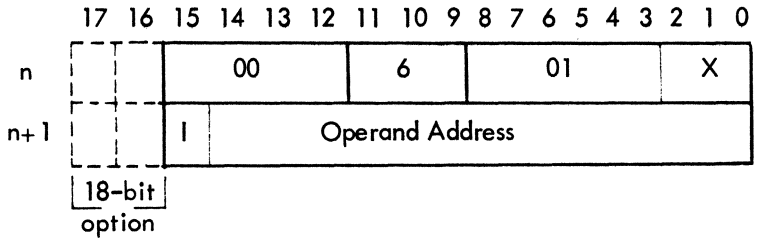


OP CODE ADDRESS MODE

YY equals any single word instruction in the OP CODE.

If X =	ADDRESS MODE	EFFECTIVE ADDRESS
0	Immediate	Second word contains operand
1	Relative to P	Contents of second word + (P Register + 1)
2	Indexed with X	Contents of second word + X Register
3	Indexed with B	Contents of second word + B Register
4	Direct or Indirect	Contents of second word is the direct address if Bit 15 is 0. Contents of second word is an indirect address if Bit 15 is a 1.

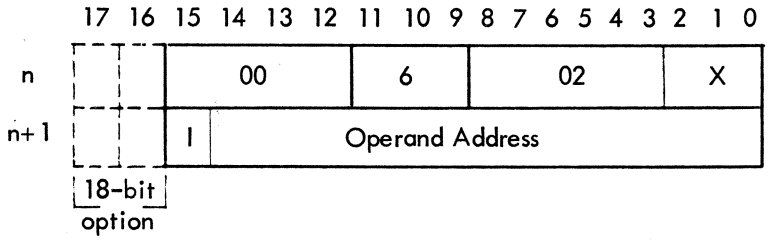
LDAE Load A Register Extended Timing: 3 Cycles



The contents of the memory location as addressed by the Operand Address at location n + 1 are placed in the A Register.

Indexing: Yes
Indirect Addressing: Yes
Register Altered: A

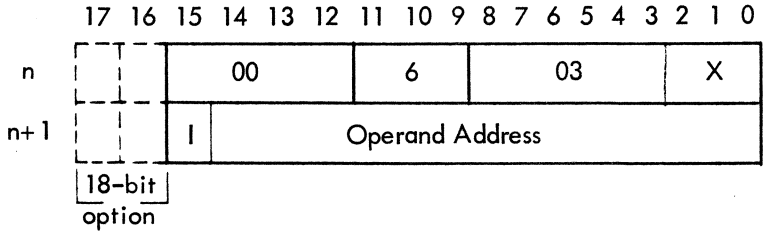
LDBE — Load B Register Extended — Timing: 3 Cycles



The contents of the memory location as addressed by the Operand Address at location n + 1 are placed in the B Register.

Indexing: Yes
Indirect Addressing: Yes
Register Altered: B

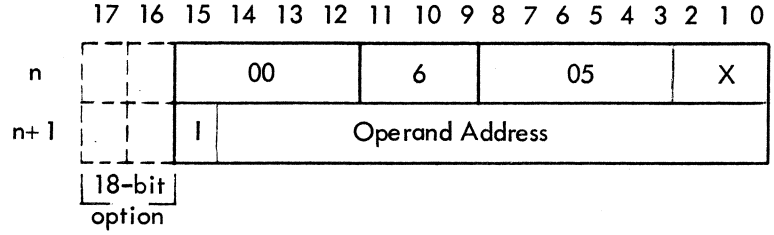
LDXE — Load X Register Extended — Timing: 3 Cycles



The contents of the memory location as addressed by the Operand Address at location n + 1 are placed in the X Register.

Indexing: Yes
Indirect Addressing: Yes
Register Altered: X

STAE — Store A Register Extended — Timing: 3 Cycles

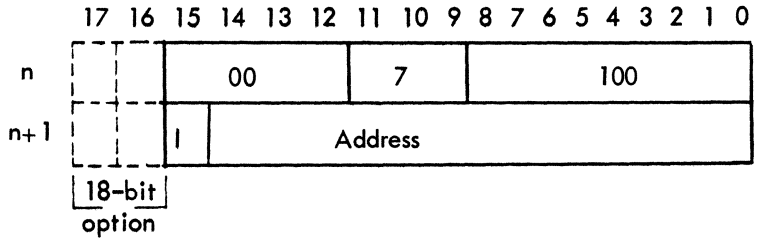


The contents of the A Register are stored in the memory location as addressed by the Operand Address at location n - 1.

Indexing: Yes
Indirect Addressing: Yes
Register Altered: Memory

3.3.1.5 Byte Instruction Group (Optional). The optional Byte instruction group provides a set of five commands for selectively loading, storing or comparing the bits of the A Register. Bit selection is controlled by a mask in the B Register. The address field a specifies the operation to be performed. Table G9, Appendix G, summarizes the byte instructions. Figures 3-12 and 3-13 illustrate the general flow for two of these operations.

SLA — Selective Load A Register — Timing: 2 Cycles



The contents of The effective memory address are selectively loaded into the bit positions of the A Register. If B Register bit $B_i = 1$, the contents of A_i are replaced by M_i. If $B_i = 0$, A_i is unaltered. The following table summarizes the logical operations performed.

Operand Bits			Results
A_i	B_i	M_i	A_i
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Indexing: No
Indirect Addressing: Yes
Registers Altered: A

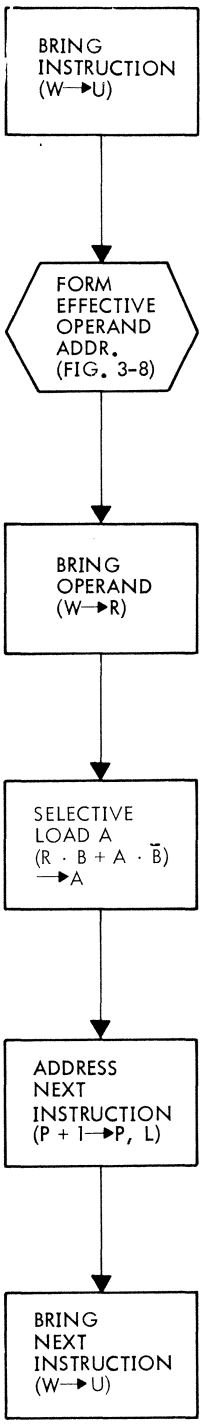


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Fig. 3-12 Selective Load A, General Flow

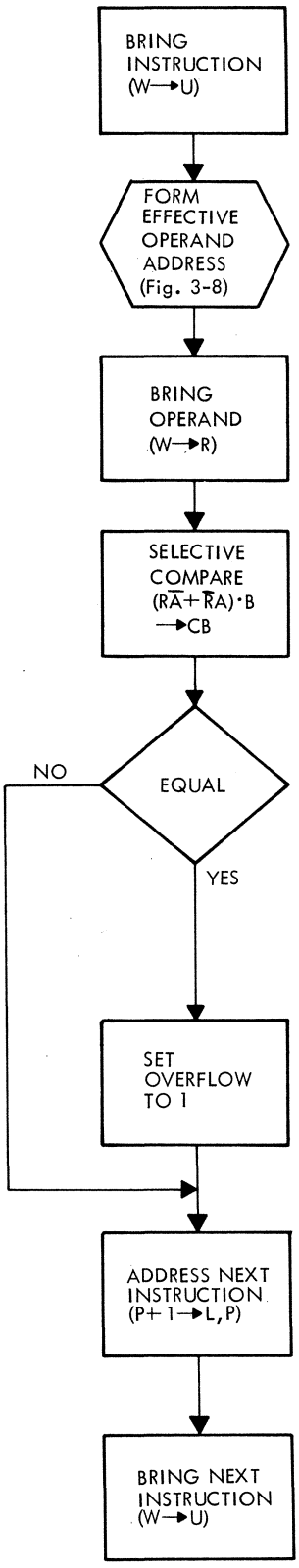
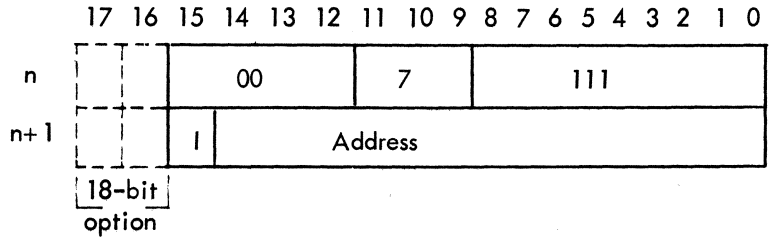


Fig. 3-13 Selective Compare Equal/Selective Compare Not Equal, General Flow

SSA — Selective Store A Register — Timing: 2 Cycles

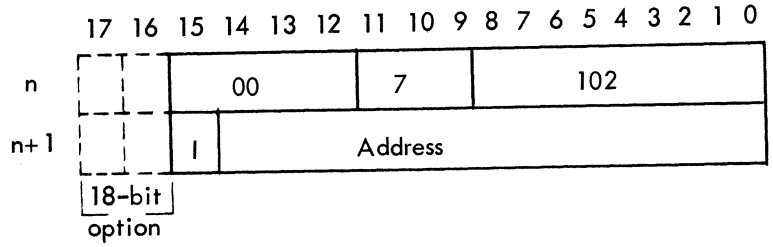


The contents of the A Register are selectively stored in the effective memory address. If the B Register bit $B_i = 1$, the contents of M_i are replaced by A_i. If $B_i = 0$, then M_i is unaltered. The following table summarizes the logical operations performed:

Operand Bits			Results
A_i	B_i	M_i	M_i
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Indexing: No
Indirect Addressing: Yes
Registers Altered: Memory

SLAC — Selective Load A Register Complement — Timing: 2 Cycles

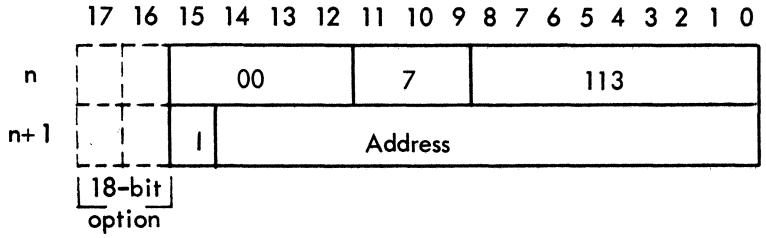


The complement of the contents of the effective memory address is selectively loaded into the bit positions of the A Register. If B Register bit $B_i = 1$, the contents of A_i are replaced by the complement of M_i. If $B_i = 0$, then A_i is unaltered. The following table summarizes the logical operations performed:

Operand Bits			Results
A_i	B_i	M_i	A_i
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Indexing: No
Indirect Addressing: Yes
Registers Altered: A

SSAC Selective Store A Register Complement Timing: 2 Cycles

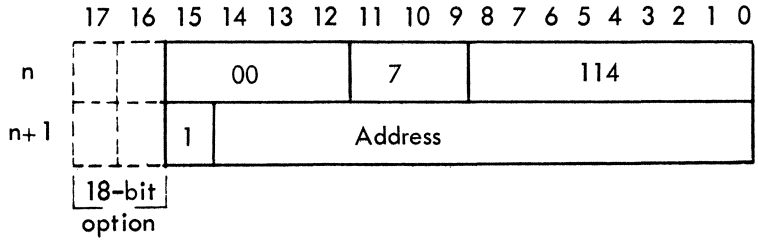


The complement of the contents of A Register is selectively stored in the effective memory address. If B Register bit $B_i = 1$, the contents of M_i are replaced by the complement of A_i. If $B_i = 0$, M_i is unaltered. The following table summarizes the logical operations performed.

Operand Bits			Results
A_i	B_i	M_i	M_i
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Indexing: No
Indirect Addressing: Yes
Registers Altered: Memory

SCAE — Selective Compare A Register Equal — Timing: 2 Cycles



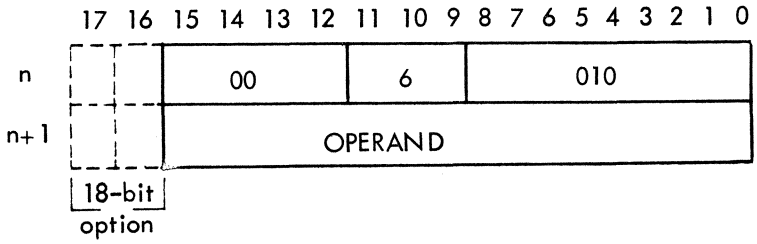
The contents of the A Register are selectively compared for equality with the contents of the effective memory address. Ones in the B Register specify the bits to be compared. If all selected bits in A are equal to the corresponding bits in the effective memory address, the overflow indicator (OF) is set.

Indexing: No
Indirect Addressing: Yes
Registers Altered: OF

3.3.2 Double-Word Non-Addressing Instructions

The double-word non-addressing instructions consist of the Immediate instruction group. The operand for the immediate instruction is contained in the second word of the double-word instruction. Address modification is not permitted for this group of instructions. The immediate instruction group codes are summarized in Table G10, Appendix G.

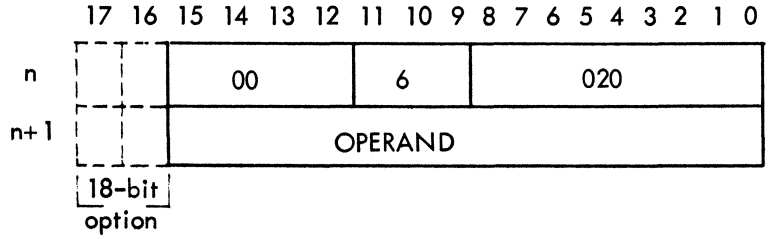
LDAI — Load A Register Immediate — Timing: 2 Cycles



The contents of the OPERAND at location n + 1 are placed in the A Register.

Indexing: No
Indirect Addressing: No
Registers Altered: A

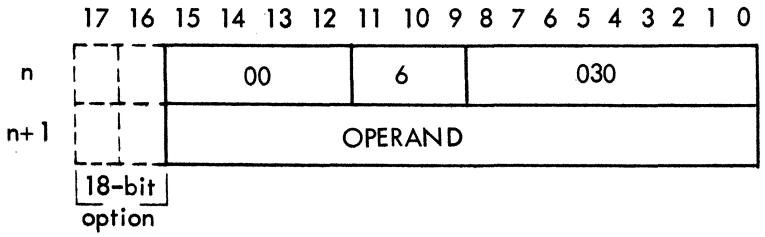
LDBI — Load B Register Immediate — Timing: 2 Cycles



The contents of the OPERAND at location n + 1 are placed in the B Register.

Indexing: No
Indirect Addressing: No
Registers Altered: B

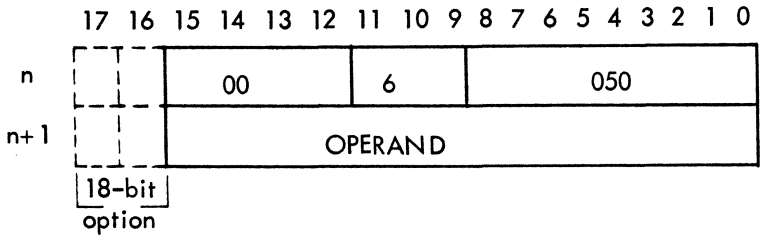
LDXI — Load X Register Immediate — Timing: 2 Cycles



The contents of the OPERAND at location n + 1 are placed in the X Register.

Indexing: No
Indirect Addressing: No
Registers Altered: X

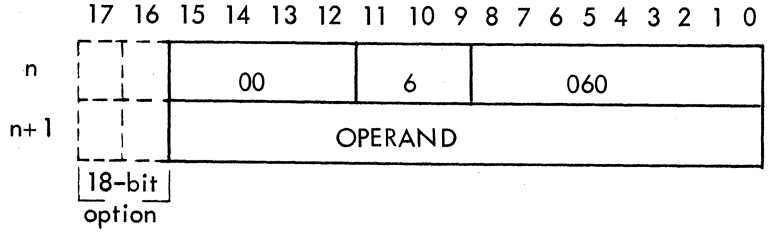
STAI — Store A Register Immediate — Timing: 2 Cycles



The contents of the A Register are placed in the OPERAND at location n + 1.

Indexing: No
Indirect Addressing: No
Registers Altered: OPERAND

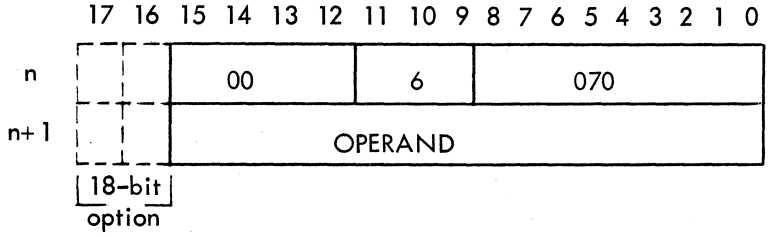
STBI — Store B Register Immediate — Timing: 2 Cycles



The contents of the B Register are placed in the OPERAND at location n + 1.

Indexing: No
Indirect Addressing: No
Registers Altered: OPERAND

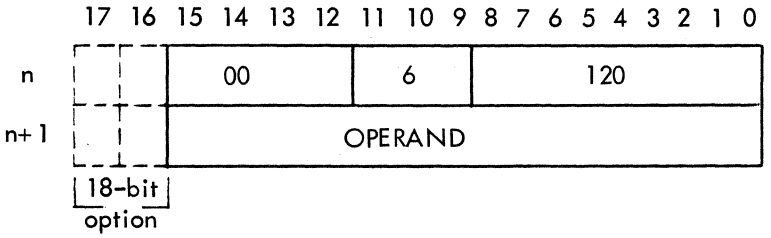
STXI — Store X Register Immediate — Timing: 2 Cycles



The contents of the Index Register are placed in the OPERAND at location n + 1.

Indexing: No
Indirect Addressing: No
Registers Altered: OPERAND

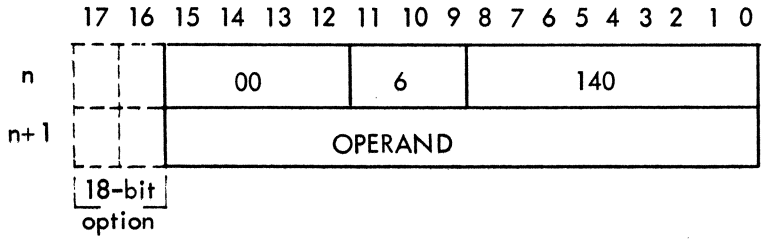
ADDI — Add Immediate — Timing: 2 Cycles



The contents of the A Register are added to the contents of the OPERAND at location n + 1. The sum is placed in the A Register. After execution, if (A) $\geq 2^{15}$ (2^{17}) or $< -2^{15}$ (-2^{17}), the overflow indicator (OF) is set.

Indexing: No
Indirect Addressing: No
Registers Altered: A, OF

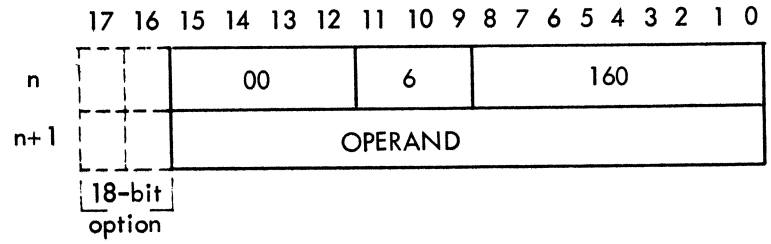
SUBI — Subtract Immediate — Timing: 2 Cycles



The contents of the OPERAND at location n + 1 are subtracted from the A Register. The difference is placed in the A Register. After execution, if (A)$\geq 2^{15}$ (2^{17}) or$< -2^{15}$ (-2^{17}), the overflow indicator (OF) is set.

Indexing: No
Indirect Addressing: No
Registers Altered: A, OF

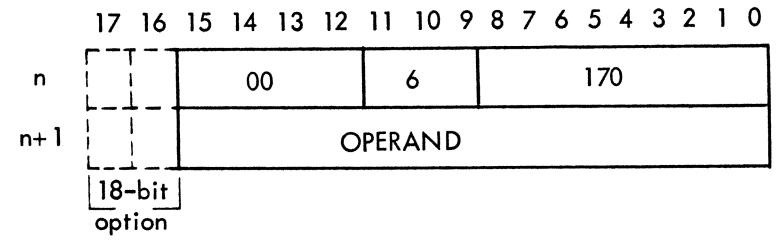
MULI — Multiply Immediate (Optional) — Timing: 10 Cycles (16 Bit)
14 Cycles (18 Bit)



The contents of the B Register are multiplied by the contents of the OPERAND at location n + 1. The product is placed in the A and B Registers with the most-significant half of the product in the A Register, and the least-significant half in the B Register. The sign of the product is contained in the sign position of the A Register. The sign position of the B Register is set to zero.

Indexing: No
Indirect Addressing: No
Registers Altered: A, B

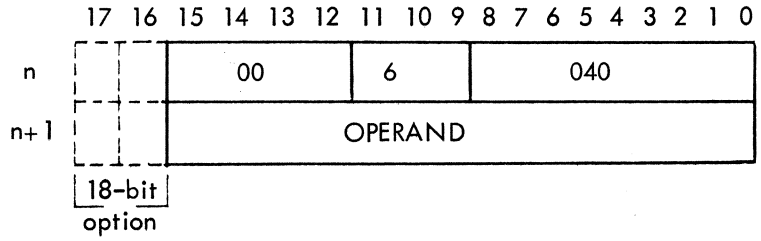
DIVI — Divide Immediate (Optional) — Timing: 10 - 14 Cycles (16 Bits)
11 - 16 Cycles (18 Bits)



The contents of the A and B Registers are divided by the contents of the OPERAND at location n + 1. The quotient is placed in the B Register, and the remainder is placed in the A Register. If $\frac{(A, B)}{M} \geq 1$ the overflow indicator (OF) is set.

Indexing: No
Indirect Addressing: No
Registers Altered: A, B, OF

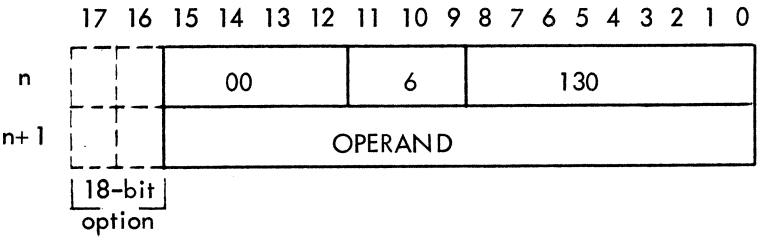
INRI — Increment and Replace Immediate — Timing: 3 Cycles



The contents of the OPERAND at location n + 1 are incremented by one, Mod 2^{16} (2^{18}). After execution, if (n + 1)$\geq 2^{15}$ (2^{17}), the overflow indicator (OF) is set.

Indexing: No
Indirect Addressing: No
Registers Altered: OPERAND, OF

ERAI — Exclusive-OR Immediate — Timing: 2 Cycles

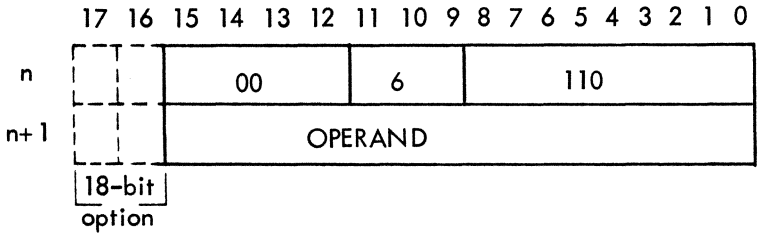


An exclusive-OR is performed between the contents of the OPERAND at location n + 1 and the A Register, and the result is placed in the A Register. If the same bit position of the OPERAND and the A Register contain a zero, or if both bit positions contain a one, the result is set to zero, If the contents of the same bit position of the OPERAND and the A Register are not equal; i.e. one contains a one and the other a zero, the result is set to one. The following table summarizes the logical operations performed:

OPERAND		RESULT
Ai	OPERAND i	Ai
0	0	0
0	1	1
1	0	1
1	1	0

Indexing: No
Indirect Addressing: No
Registers Altered: A

ØRAI — Inclusive-OR Immediate — Timing: 2 Cycles

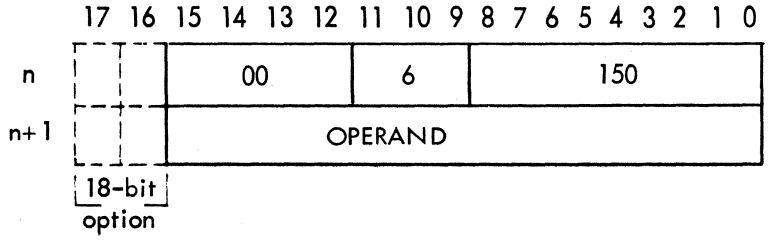


An inclusive-OR is performed between the contents of the OPERAND and the A Register. The result is placed in the A Register. If either the OPERAND or the A Register contains a one in the same bit position, a one is placed in the result in the A Register. The following table summarizes the logical operations performed:

OPERAND		RESULT
Ai	OPERAND i	Ai
0	0	0
0	1	1
1	0	1
1	1	1

Indexing: No
Indirect Addressing: No
Registers Altered: A

ANAI — AND Immediate — Timing: 2 Cycles



A logical-AND is performed between the contents of the OPERAND and the A Register. The result is placed in the A Register. If the same bit position of the OPERAND and the A Register contain a one, the result is set to one; otherwise, the result is set to zero. The following table summarizes the logical operations performed:

OPERATION		RESULT
Ai	OPERAND i	Ai
0	0	0
0	1	0
1	0	0
1	1	1

Indexing: No
Indirect Addressing: No
Registers Altered: A

SECTION IV
DATA 620 INPUT / OUTPUT SYSTEM

SECTION IV
DATA 620 INPUT/OUTPUT SYSTEM

4.1 INTRODUCTION

This section describes the operation and instruction set of the computer input/output system which includes the data transfer, external control, program sense, and program interrupt facilities.

The DATA 620 input/output system is designed to facilitate integration of the computer into an overall system. Refer to the Interface Reference Manual for detailed information required for special interface designs.

A wide selection of optional peripheral devices is also available. The basic complement of standard peripherals for the DATA 620 is described in Section VI.

4.2 ORGANIZATION

As shown in the block diagram, Figure 2-1, the I/O Section of the computer communicates with the operational registers and the memory through the internal C Bus. Data and control signals are transmitted to and from external peripheral devices through the I/O Bus.

4.2.1 Overall Operation

The overall organization of the DATA 620 I/O System, including a typical set of peripheral devices, is shown in Figure 4-1. Standard or special peripheral devices are in parallel on the I/O Bus. Any number of logical devices, up to a total of 64, may be added.

Two types of I/O operations may be performed: program control and automatic control. Program-controlled information transfers between the Central Processor and the external devices to be executed are:

a. External control. An external control code may be transmitted, under program control, from the Central Processor to an external device.

b. Program sense. The Central Processor can sense the status of a selected external line under program control.

c. Single-word transfer to/from A and B Registers. A single word may be transferred to or from the A and B Registers under program control.

d. Single-word transfer to/from memory. A single word may be transferred to or from any memory location under program control.

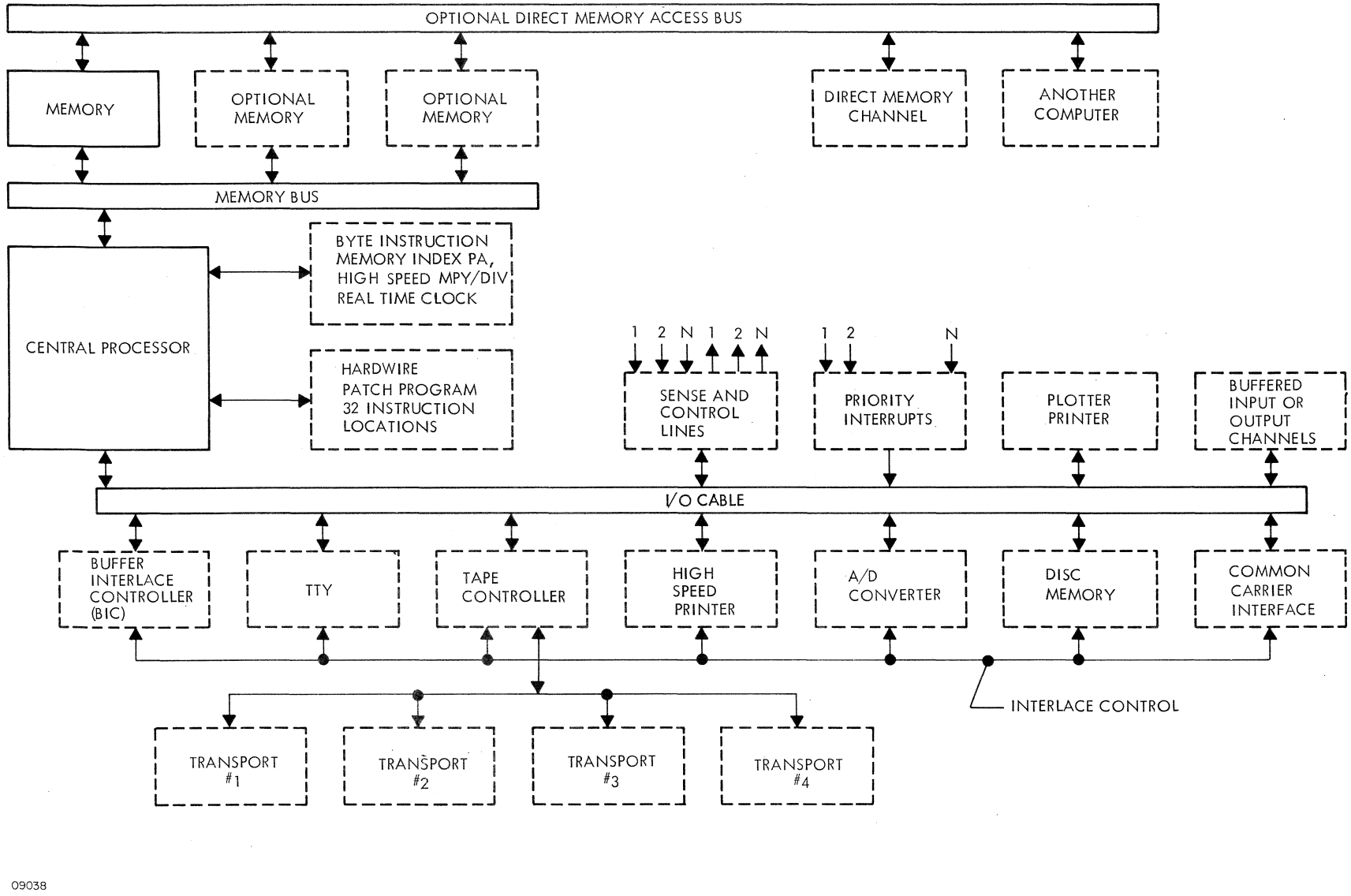


Fig. 4-1 DATA 620 I/O System Organization

The following types of automatically controlled information transfers between the Central Processor and the external devices may be executed independently of the program:

a. Program interrupt. An external device may force the program to execute an instruction at a specified location in memory.

b. Buffer Interlace Controller (BIC) transfer to/from memory. Blocks of words may be transferred to or from sequential memory locations under control of an optional Buffer Interlace Controller (BIC). Devices controlled by the BIC may also be operated under program control (single-word transfers).

c. Interlace data transfers. Single words may be transferred to or from memory by a special interface controller which uses the control signals available on the I/O Bus.

4.2.2 Input/Output (I/O) Bus.

A typical organization of peripheral devices on the I/O Bus is shown in Figure 4-1. The I/O Bus consists of the E Bus, plus a set of control lines. The E Bus contains 16 (or 18) pairs of bi-directional lines which transmit control codes, addresses, and data between the Central Processor and the peripheral devices connected, in parallel, to this bus.

Information transfers are synchronized by peripheral controllers; these controllers may, in turn, control one or more peripheral devices. The Central Processor communicates directly with all peripheral controllers under program control. It may determine when a device is ready to send or receive information by sensing associated sense lines, or it may be notified by means of a program interrupt. Standard Priority Interrupt and Sense Line Controllers are available, or special controllers may be provided.

Where block transfers of data, independent of, and concurrent with, internal operations are required (such as from tapes, drums, commutators, etc.) the Buffer Interlace Controller may be provided. This element contains hardware registers which automatically generate the proper memory addresses for successive data transfers to or from the Central Processor memory, directly to or from the device through its controller.

This type of operation uses the program trap facilities of the Computer. The trap sequence temporarily halts the program, without altering the program sequence, while the trapped I/O transfer occurs. Special interface designs may also take advantage of the trap facilities to control I/O transfers.

4.2.3 Input/Output Operations

During information transfers over the I/O Bus, the E lines may carry control codes, addresses or data, depending upon which type of operation is being performed. Table 4-1 defines the I/O control line signals used to synchronize all input/output operations. Table 4-2 summarizes the signals present on the E Bus during the program-controlled I/O operations.

Table 4-1
I/O CONTROL LINE SIGNALS

CONTROL LINE	SIGNAL NAME	FUNCTION
Function Ready	FRYX-I	Indicates that the E Bus contains external control information.
Data Ready	DRYX-I	Indicates that the E Bus contains the data.
Sense Response (Sent back to computer)	SERX-I	Indicates logical state of line designated by sense line address on E Bus.
Interrupt Request	IURX-I	Indicates a demand from the Interrupt module to force program to take one instruction from location specified by address on E Bus. This Address will be placed on E Bus when IUAX-I becomes true.
Interrupt Acknowledge	IUAX-I	Indicates that external interrupt demand is being acknowledged. Address is placed on E Bus and removed when IUAX-I goes false.
Trap Output	TPØX-I	Indicates that a Buffer Interlace Controller (or equivalent) is requesting a data transfer from memory.
Trap Input	TPIX-I	Indicates that a Buffer Interlace Controller (or equivalent) is requesting data to be transferred to memory.
Interrupt Clock	IUCX-I	1.1-mc pulse on party line for providing clock to the Interrupt module. This clock may also be used in any interface design.
Priority Out	PRIX-I	Priority line used with interrupt and Buffer Interlace Controller modules for priority determination.
Priority In	PR4X-I	Priority Line returned to computer for permitting console interrupt.
Priority 2 and 3	PR(N)X-I	Intermediate priority lines that are used on the I/O bus for allowing flexible priority assignments along the

Table 4-1 (cont'd)
I/O CONTROL LINE SIGNALS

CONTROL LINE	SIGNAL NAME	FUNCTION
		Party line.
System Reset	SYRT-I	Reset line for initializing peripheral controllers. Energized by Console RESET switch.
Interrupt Jump	IUJP-I	Indicates that instruction at interrupt location is a Jump (2-word) instruction.

4.2.4 I/O Cable Adapter Card

The I/O Cable Adapter is a standard VersaLOGIC module (VL121) designed to facilitate interfacing with the DATA 620 I/O Bus. Typical examples illustrating its use are given in the Interface Reference Manual. This card simplifies the use of many types of I/O interfaces.

4.3 PROGRAM CONTROL FUNCTIONS

Interfacing functions fall into two major categories: programmed operations, and automatic operations. The programmed operations are: External Control (single-bit out), Sense Operations (testing a single bit), Data Transfer In (full-word inputs), and Data Transfers Out (full-word outputs). The following paragraphs describe the programmed operations and examples of their use. The I/O instruction group is summarized in Table G-11, Appendix G.

4.3.1 External Control

The External Control instruction is a single word, non-addressing instruction. It places a function code, contained in Bits 0-8, on the E Bus to effect a control operation on an external device.

EXC External Control Timing: 1 cycle

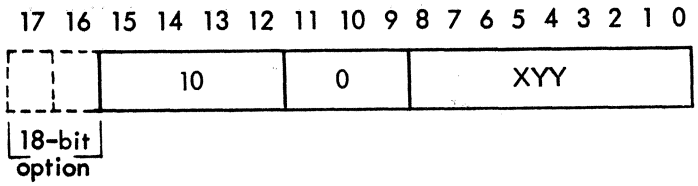


Table 4-2
SUMMARY OF E BUS SIGNALS DURING FRY TIME

OPERATION	BITS GENERATED BY DATA 620						BITS GENERATED BY DATA 620 I/O INSTRUCTION				
	EB15-1	EB14-1	EB13-1	EB12-1	EB11-1	EB10-1, EB09-1	EB08-1	EB07-1	EB06-1	EB05-1 to EB00-1	Function
Output from Memory	0	1	0	0	0	Unused	Note 1	0	0	Device Address ($00-63_{10}$)	Data Out
Output from A Register								0	1		
Output from B Register											
Input to Memory	0	0	1	0	0	Unused	Note 1	0	0	Device Address ($00-63_{10}$)	Data In
Input to A Register								0	1		
Input to B Register								1	0		
Sense state of External Device	0	0	0	1	0	Unused	Function Code			Device Address ($00-63_{10}$)	Sense
Send function code to External Device	0	0	0	0	1	Unused	Function Code			Device Address ($00-63_{10}$)	External Control 100XXX
Send Aux. Function code to External Device	1	0	0	0	0	Unused	Function Code			Device Address	External Control 104XXX

Note 1: If EB08-1 is TRUE, selected register in computer is cleared.
If EB08-1 is FALSE, selected register in computer is not cleared.
Bits EB06-1 to EB08-1 generally ignored by I/O Controller:

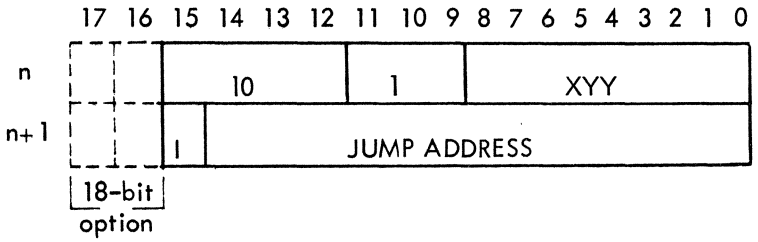
The nine bits represented by XYY are placed on the E Bus for transmission to the I/O controllers. The device address is contained in the YY portion of the data, and the X portion of the data contains the function to be performed by the selected device.

Indexing: No
Indirect Addressing: No
Registers Altered: None

4.3.2 Program Sense

The sense instruction is a double-word, addressing instruction which senses the logical state of an external line. Figure 4-2 shows the execution of this instruction.

SEN — Program Sense — Timing: 2.25 cycles



The nine bits represented by XYY are placed in the Party Line I/O Bus and represent the condition to be tested. X defines a specific line within device YY. The associated peripheral controller replies with either a true or false condition.

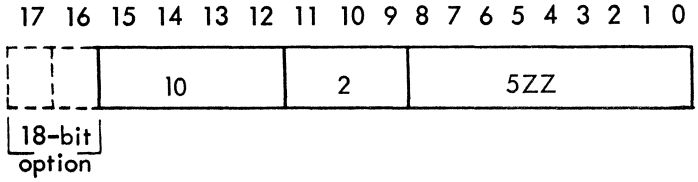
If a true condition is received by the DATA 620, a jump is made to the Jump Address. If a false condition is received the next instruction in sequence is executed.

Indexing: No
Indirect Addressing: No
Registers Altered: P

4.3.3 Data Transfer In

Two types of Data Transfer In instructions are provided: input to operational registers, and input directly to memory. The first type of input instruction is a single-word, non-addressing class instruction; the second type of input instruction is a double-word, addressing class instruction.

CIA — Clear and Input to A Register — Timing: 2 cycles



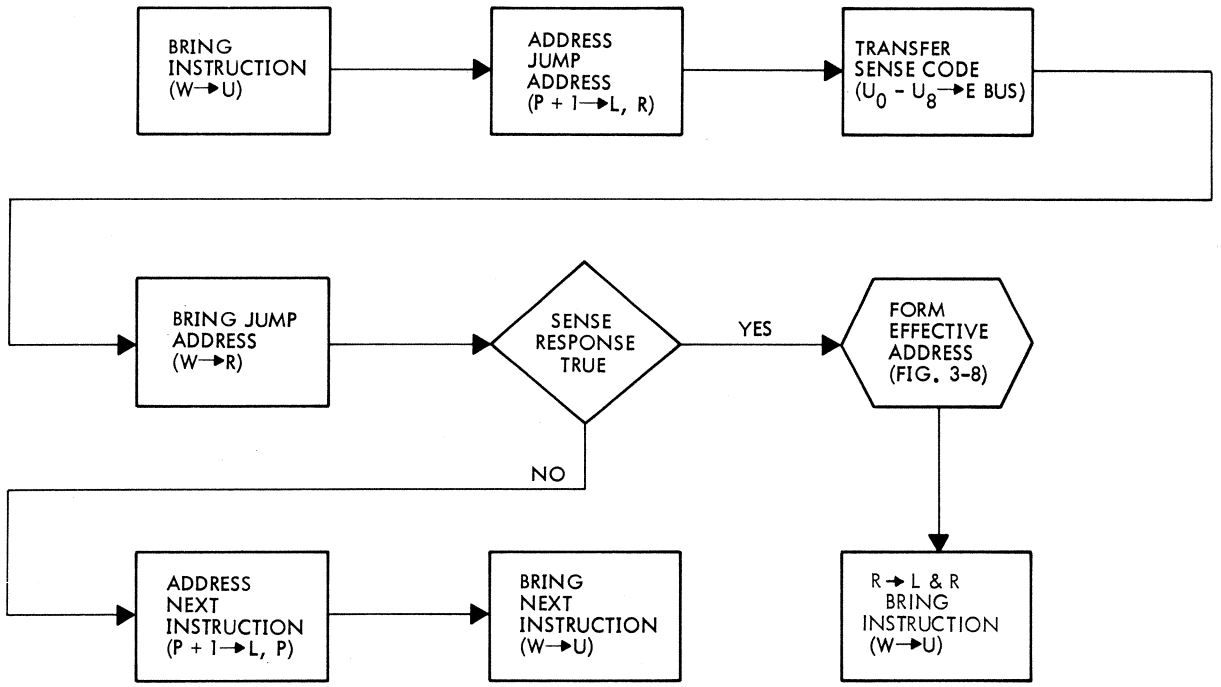
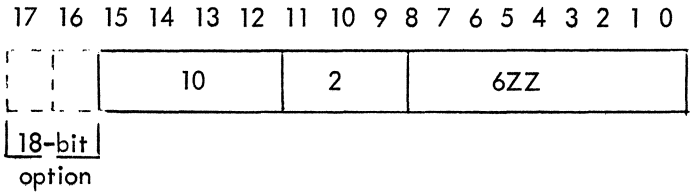


Fig. 4-2 Sense Instruction, General Flow

The A Register is cleared and a data word from the selected device, ZZ, is transferred into the A Register.

Indexing: No
Indirect Addressing: No
Registers Altered: A

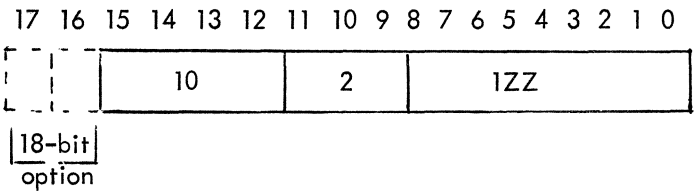
CIB — Clear and Input to B Register — Timing: 2 cycles



The B Register is cleared and a data word from the selected device, ZZ, is transferred to the B Register.

Indexing: No
Indirect Addressing: No
Registers Altered: B

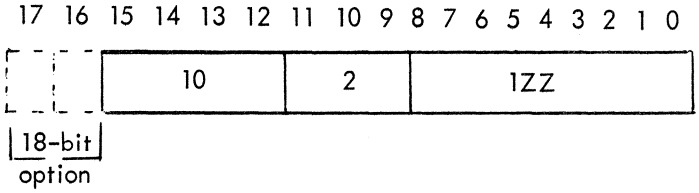
INA — Input to A Register — Timing: 2 cycles



A data word from the selected device, ZZ, is inclusively-ORed with the contents of the A Register.

Indexing: No
Indirect Addressing: No
Registers Altered: A

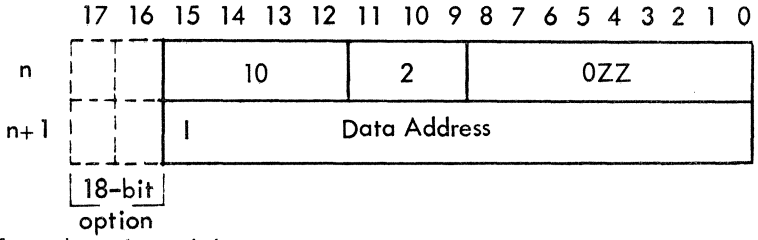
INB — Input to B Register — Timing: 2 cycles



A data word from the selected device, ZZ, is inclusively-ORed with the contents of the B Register.

Indexing: No
Indirect Addressing: No
Registers Altered: B

IME — Input to Memory — Timing: 3 cycles



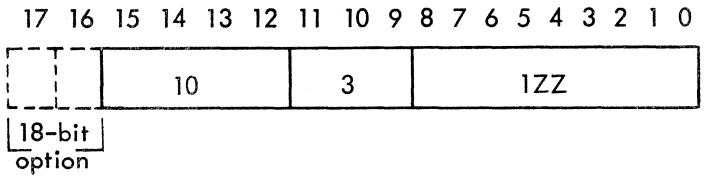
A data word from the selected device, ZZ, is placed in the effective memory address. Figure 4-3 shows the execution of this instruction.

Indexing: No
Indirect Addressing: No
Registers Altered: Memory

4.3.4 Data Transfer Out

Two types of Data Transfer Out instructions are provided: output from operational registers, and output from memory. The first type of output instruction is a single-word, non-addressing class instruction; the second type is a double-word, addressing class instruction.

ØAR — Output from A Register — Timing: 2 cycles



The contents of the A Register are transferred to the selected device, ZZ.

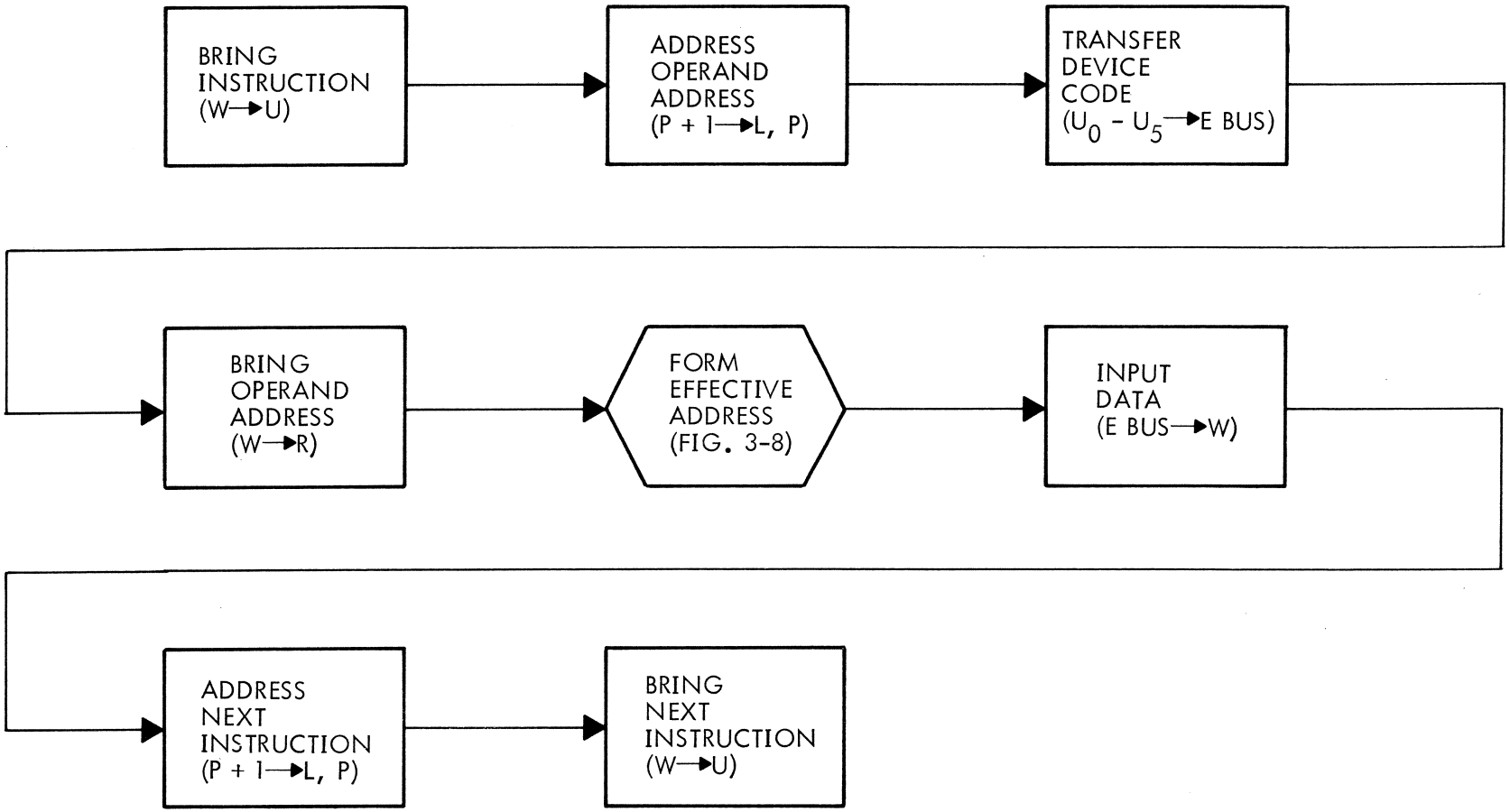
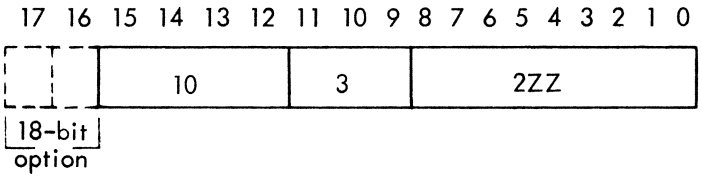


Fig. 4-3 Input to Memory, General Flow

Indexing: No
Indirect Addressing: No
Registers Altered: None

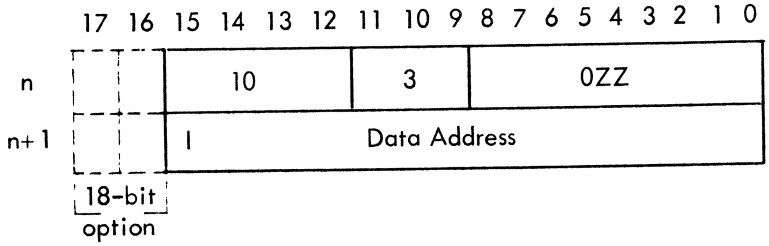
ØBR — Output from B Register — Timing: 2 cycles



The contents of the B Register are transferred to the selected device, ZZ.

Indexing: No
Indirect Addressing: No
Registers Altered: None

ØME — Output from Memory — Timing: 3 cycles



The contents of the effective memory address are transferred to the selected device, ZZ.

Indexing: No
Indirect Addressing: No
Registers Altered: None

4.4 AUTOMATIC CONTROL FUNCTIONS

Two types of computer timing sequences are provided to automatically transfer control and information signals between the I/O and the DATA 620:

a. An interrupt timing sequence is initiated when the DATA 620 recognizes an external interrupt signal. This sequence forces the computer to execute an instruction at the memory location specified by interrupt logic through the E Bus.

b. A trap timing sequence is initiated when an external device signals that it wishes to transfer a word to or from memory. The external device must supply the memory address of the word through the E Bus. This sequence delays the internal program sequence for the time required to execute the I/O transfer (2.7 μsec).

The devices that demand either of these automatic sequences must first establish a priority to resolve two or more simultaneous demands for service. The priorities of devices demanding service are determined every 1.8 μsec, and are clocked by the Interrupt Clock (refer to Table 4-1).

The basic computer has two built-in priority devices, both of which are internal program interrupts. The power failure interrupt is permanently wired for the highest priority. Unless power failure (scanned every 1.8 μsec) is detected, the computer will service interrupt or trap requests from the I/O Cable on a priority basis. If no requests are being received, the computer will accept a request from the console interrupt switch which is permanently wired for the lowest priority.

Priority assignment for devices on the I/O Cable is optional and is a part of the system definition. Priorities may be fixed, for any given configuration, by properly connecting priority lines in the I/O Cable. Priorities can be altered if the definition changes.

4.4.1 Program Interrupt

The DATA 620 has a multi-level interrupt system with single-execute, on/off and selective arm/disarm capability. Each interrupt line is assigned a unique memory destination address which is the first of a pair of locations. The system is modular and expandable in sets of eight levels. Two sets of eight are grouped to form sixteen. Each group of eight or sixteen has a unique device address. Two interrupts are provided, as standard, with the minimum machine configuration. The first and highest priority is connected to the power failure protection system. The second and lowest priority is connected to the console interrupt pushbutton. An interrupt response to an external signal can be accomplished as quickly as two memory cycle periods.

Each interrupt line has an enable/disable flip-flop which is addressable and set by interrupt control instructions. If signals exist on one or more interrupt lines, the highest-priority line is recognized and the corresponding memory destination address is transmitted to the DATA 620 after the current instruction is executed.

The program can maintain the hardware order of priority levels, or re-order to meet dynamic queueing. For each group the order is determined by a 16-bit mask word transferred by the program to the arm/disarm flip-flops in the interrupt system. The action initiated by the interrupt subroutine causes the interrupting device to remove its requesting signal.

An acknowledgement of an interrupt causes the instruction located at the destination address to be executed. The instruction can be any of the DATA 620 repertoire. This technique permits the interrupts to be of the "single execute" type, whereby single-instruction responses to external signals can be serviced in one instruction period. A real-time clock can be implemented with an interrupt line and an external pulse generator. An automatic data channel can be implemented with as few as two interrupt lines. If the executed instruction is a jump, the interrupt system is automatically inhibited permitting the inhibit to be terminated under program control. While in the inhibit mode, the interrupt subroutine may selectively enable and disable levels, and then enable the system permitting the selected levels to interrupt the level being processed.

4.4.2 Interlace Data Transfers

Interlace data transfers may be performed concurrently with internal program operation. This type of operation uses the computer trap timing sequence to delay the program for three cycles (5.4 μsec), while a word is transferred between memory and a peripheral device. The transfer is controlled by the external device which must transmit the memory address of the data word, and must synchronize the operation using the signals transmitted over the I/O Control lines (Table 4-1). The maximum interlace transfer rate is 202,000 words per second.

The general trap sequence flow is shown in Figure 4-4. The maximum computer delay in acknowledging a trap request is 5.4 μsec. However, the time delay experienced by a specific controller in receiving acknowledgement to a trap request may be extended by the time required for the Central Processor to service higher-priority requests.

Special peripheral controllers designed for system applications (such as A/D and D/A converters, etc.) may utilize the trap facilities of the computer to implement automatic I/O operations (refer to the Interlace Reference Manual for detailed design information). A standard Buffer Interlace Controller is also available (refer to paragraph 6.2) for use with all standard DATA 620 peripheral equipments. Special system devices may also be interfaced for interlace operations under control of this unit.

4.5 DIRECT MEMORY ACCESS AND OVERLAP CONTROL (OPTIONAL)

Complex data systems frequently require data buffering and multiple simultaneous communications. Functional processing may be time-phased. For example, during one phase the system may be in "data acquisition and quick look" and in another phase, be in "data analysis". During the "data acquisition" phase, maximum throughput is required. During "data analysis", the highest-possible processing rates are desired. These abilities can be best obtained if the memory complex is modular and can service multiple purposes. The Direct Memory Access and Overlap Control option provides this capability.

Direct Memory Access and Overlap Control (DMA) provides an additional memory hub, priority and control logic, and a memory bus. The additional memory hub makes available the W Register, the L Register, and memory control signals on lines isolated from the primary memory bus. Priority and control logic gives the DMA priority over the DATA 620 when both units simultaneously access a memory module. The additional memory bus provides a facility for system devices to communicate with the memory module over an independent bus. A second DATA 620 can be connected to this memory bus. An overlap control option must be added to each memory module. The DMA enables the memory modules to operate simultaneously in the general-purpose memory modes of: Read/Write, Read/Modify Write, Clear/Write, and half-cycle Read or Write.

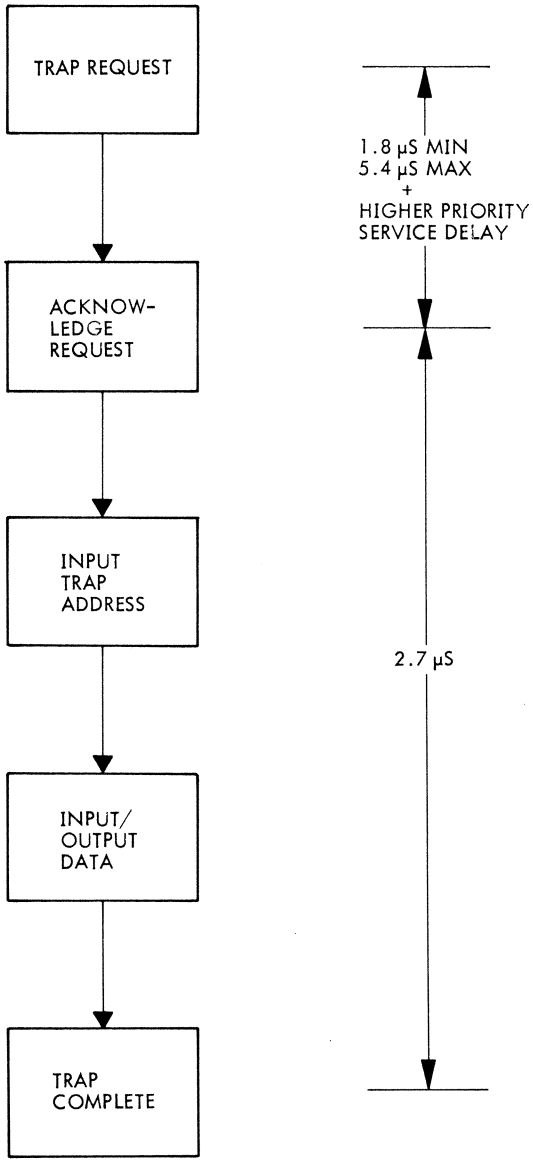


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Fig. 4-4 Trap Sequence, General Flow

SECTION V
CONTROL CONSOLE OPERATION

SECTION V
CONTROL CONSOLE OPERATION

5.1 CONTROLS AND INDICATORS

The DATA 620 Control Console (Fig. 5-1) provides controls and displays required for operator communication with the computer. Control Console facilities are of two kinds: register displays, and control switches. The contents of all operational registers in the computer, including the Instruction Register, are continuously displayed in binary-octal form. Indicators are also switches which permit independent control over each bit in the registers. The functions and applications of the register displays are summarized in Table 5-1. During normal operation (RUN mode) the displays are active; however, the register entry and reset switches are deactivated to prevent accidental alteration of the register contents.

Control switches permit the operator to manually alter normal program operation. These switches, described in Table 5-1, provide considerable control flexibility and are useful for maintenance, troubleshooting, and program debugging. The Sense switch controls are also useful in normal program operation to allow selection, by the operator, of particular program sequences to be executed.

Table 5-1
CONTROLS AND INDICATORS

CONTROL OR INDICATOR	FUNCTION
A REGISTER	Illuminated switch/indicators continuously display contents of the A Register. RESET switch shows state of overflow flip-flop. Pressing switch enters a "1" into corresponding bit position. Pressing RESET switch clears register, except the overflow bit. The overflow bit is set or reset by execution of the Set Overflow (or arithmetic condition) and Reset Overflow instructions.
B REGISTER	Illuminated switch/indicators continuously show contents of the B Register. Pressing switch enters a "1" into corresponding position. Pressing RESET switch clears entire register.
INSTRUCTION REGISTER	Illuminated switch/indicators continuously show the current instruction being held in the Instruction (U) Register during execution. Pressing switch enters a "1" into corresponding bit position. Pressing RESET switch clears entire register.

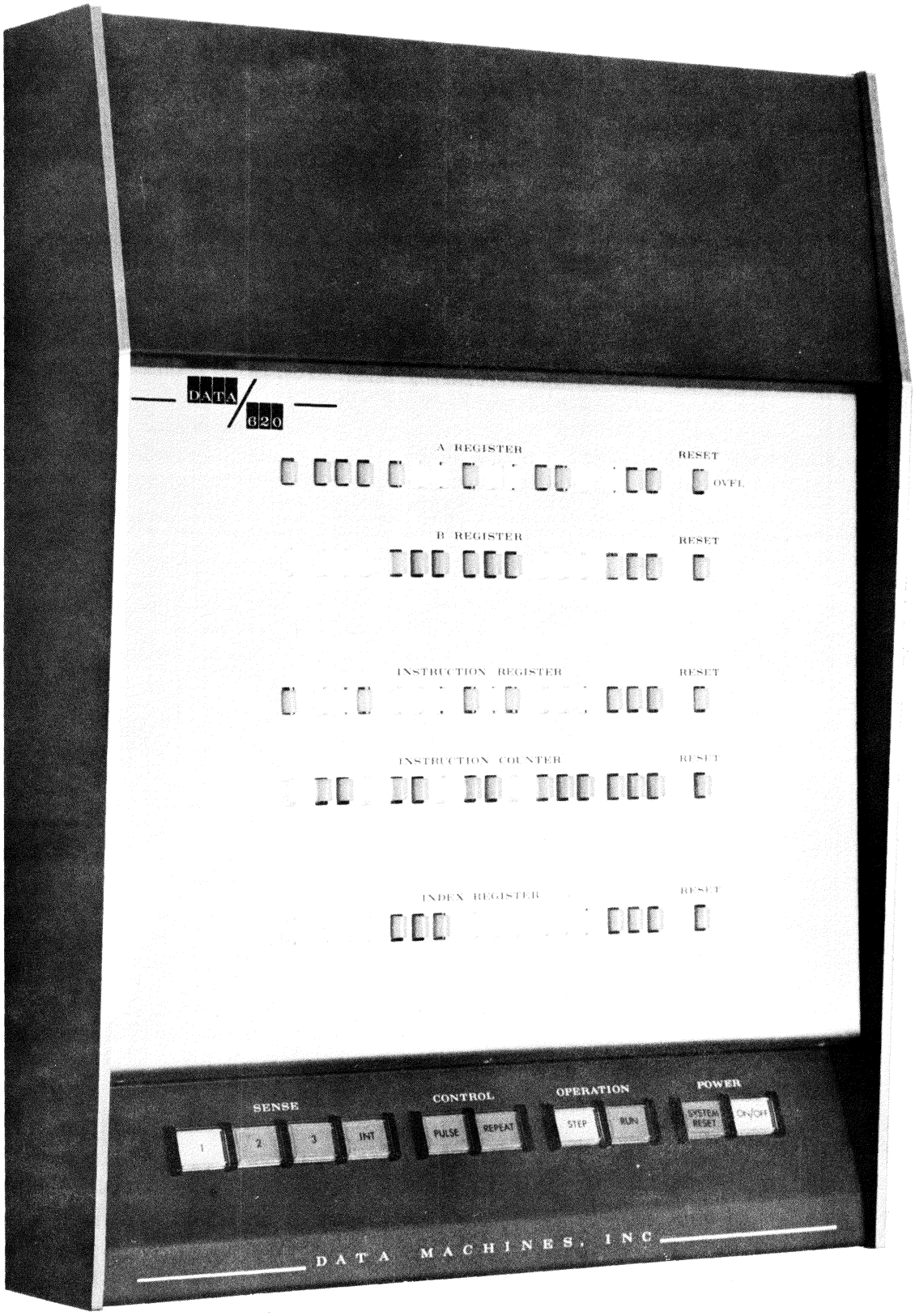


Fig. 5-1 Control Console

Table 5-1 (cont'd)
CONTROLS AND INDICATORS

CONTROL OR INDICATOR	FUNCTION
INSTRUCTION COUNTER	Illuminated switch/indicators continuously show memory location of the next instruction to be executed when the computer is halted. Pressing switch enters a "1" into corresponding bit position. Pressing RESET switch clears entire register.
INDEX REGISTER	Illuminated switch/indicators continuously show contents of the Index (X) Register. Pressing switch enters a "1" into corresponding bit position. Pressing RESET switch clears entire register.
POWER ON/OFF	Alternate-action switch/indicator turns memory and logic power supplies on and off. This switch also controls Teletype Controller power. Switch indicator lights when memory and computer power are both on; indicator is turned off when memory power is turned off.
SYSTEM RESET	Momentary-contact switch/indicator permits manual reset following memory temperature overload condition and is used to initialize computer and peripheral equipment. Indicator lights when memory power has been automatically turned off by over-temperature in the memory. Pressing this switch restores power to the memory and turns indicator off. POWER ON indicator is turned on when temperature overload circuit is reset by this switch.
RUN	Momentary-contact switch/indicator sets computer to normal mode of operation. Indicator is turned off and operation is halted when STEP switch is pressed or a program HALT instruction is executed.
STEP	Momentary-contact switch/indicator permits operation to be halted and the program to be executed one instruction at a time. Pressing this switch in the RUN mode stops operation, turns RUN indicator off, and turns STEP indicator on. INSTRUCTION REGISTER display indicates next instruction to be executed when STEP switch is pressed. PROGRAM COUNTER display indicates location of next instruction to be executed after the instruction contained in Instruction Register is executed. Normal operation is started and STEP indicator is turned off when RUN switch is pressed.

Table 5-1 (cont'd)
CONTROLS AND INDICATORS

CONTROL OR INDICATOR	FUNCTION
REPEAT	Alternate-action switch/indicator permits manual repeat of an instruction in Instruction Register. Pressing STEP switch executes instruction and advances Program Counter; however, contents of the Instruction Register are left unchanged. Switch and indicator on the Control Console are activated only when the STEP switch is on (operation halted); however, Maintenance Panel connections can activate Repeat mode during RUN conditions (for maintenance purposes).
SENSE SWITCHES 1, 2, 3	Alternate-action switch/indicators permit manual program control whenever the sense switch Jump, or Jump-and-Mark, or Execute instructions (JSS1, JSS2, JSS3, JS1M, JS2M, JS3M, XS1, XS2, XS3) are performed. The indicated Jump and Execute operations are performed only if the corresponding Sense Switch is ON.
INTERRUPT	Momentary-contact switch permits operator to manually interrupt the current program sequence and force the next instruction to be taken from a fixed memory location. Operations from that point are determined by the program.

5.2 MANUAL OPERATIONS

Control Console operation is simple and may be understood by reference to Table 5-1 and Figure 5-1. The following paragraphs describe typical operating sequences which illustrate normal use of the computer.

5.2.1 Power Control

The POWER ON switch supplies ON/OFF power to computer logic, memory, and controller logic. Memory power is automatically turned off (and the internal power fail interrupt is generated) if the temperature sensor in the memory detects an overload condition. When this occurs, the POWER RESET lamp is turned on and the POWER ON lamp is turned off (note that computer power is still on even though the lamp is off). Memory power may be re-applied when the temperature has returned to normal by either pressing the POWER RESET switch, or by turning the POWER ON switch off and then on again.

5.2.2 Manual Program Entry and Execution

When the computer is halted (STEP mode), programs and data may be read from memory and entered into memory, and a pre-stored program may be manually executed.

To load words into memory (either instructions or data), set up the desired word in the A, B, or X Register. Set up the appropriate store-type instruction (STA, STB, STX) with the desired operand address in the Instruction (U) Register and press the STEP switch to execute the store operation.

To display the contents of any memory cell in the A, B, or X Register displays, set up the appropriate load-type instruction (LDA, LDB, LDX) with the proper memory address in the Instruction Register; then press the STEP switch to load the selected word into the register.

To manually execute a program stored in memory, set up the starting location of the program in the Program Counter. When the STEP switch is pressed, the instruction contained in the Instruction Register is executed, and the instruction of the selected location is transferred to the Instruction Register. Repeated operation of the STEP switch will then step through the program one instruction at a time. All operations such as multi-level indirect addressing will be performed for each instruction each time the STEP switch is operated. Note that I/O instructions that involve an asynchronous device which transfers data in a block (such as magnetic tape or the Teletype) generally cannot be operated in a single-step mode.

5.2.3 Instruction Repeat

In the STEP mode, the Instruction Register contains the next instruction to be executed when STEP is pressed. The Program Counter contains the location of the next instruction to be transferred to the Instruction Register after the current instruction is executed.

In some cases, it is desirable to manually execute an instruction several times. When the REPEAT switch is on, Instruction Register loading, when STEP is pressed, is inhibited even though the Instruction Counter is advanced each time. This mode is particularly useful for loading words into sequential memory locations, or for displaying the contents of sequential memory cells.

To load a group of sequential memory cells, set up the appropriate store-type instruction (STA, STB, STX) in the Instruction Register with the Relative Address mode in the M Field and the base address in the A Field. Repeated operation of the STEP switch will store the contents of either A, B, or X into sequential memory locations. The word loaded on each step may be changed by entering the desired value into the operational register for each step.

To display the contents of a group of sequential memory cells, set up the appropriate load-type instruction (LDA, LDB, LDX) in the Instruction Register, in the relative address mode, with the base address in the Instruction Register and the A Field = 0. The contents of the sequential locations will be displayed in the selected operational register with each operation of the STEP switch.

5.2.4 Sense Switches

The sense switches allow the operator to dynamically alter a program sequence in either the RUN or STEP mode. The three sense switches provide a logical-AND function with bits 6-8 of the instruction word, and consequently can be used for various logical branches set up on the Console.

5.2.5 Manual Interrupt

If the INTERRUPT switch is pressed while the program is in the RUN mode, a program interrupt signal is generated. This signal breaks the normal program sequence for one cycle and forces execution of an instruction at a fixed location. If the instruction at the fixed location is not a jump or halt, the normal program sequence is resumed. A Jump-and-Mark instruction is used to transfer to a special interrupt routine. This interrupt is particularly useful for troubleshooting operations and may also be used for handling emergency conditions detected by the operator.

SECTION VI
PERIPHERAL EQUIPMENT

SECTION VI
PERIPHERAL EQUIPMENT

6.1 GENERAL

A wide variety of standard peripheral devices are available, providing broad flexibility in adapting the computer system to any set of requirements. Table 6-1 summarizes characteristics of the basic optional peripherals available.

The following paragraphs present general descriptive material and application information for the basic peripheral group. Additional information on the device controllers is contained in individual reference manuals for the units.

6.2 BUFFER INTERLACE CONTROLLER

The Model 620-15 Buffer Interlace Controller (BIC) is an optional accessory for the DATA 620 computer. The BIC controls transfer of data blocks between the memory and peripheral I/O devices, concurrent with program operations in the DATA 620. Full 16/18-bit word transfers can be controlled at rates up to 202,000 words per second.

The BIC is attached to the I/O Cable and generates the addresses and timing signals that control transfer of data words, through the I/O Bus, between a selected device and the DATA 620 memory. Any number of peripheral devices may be controlled by the BIC, limited to a maximum of 64 device numbers which may be assigned to all peripheral equipments (including the BIC). Multiple Buffer Interlace Controllers, with arbitrary priority assignments, may be used on the I/O Cable permitting concurrent data transfers to and from several peripheral devices.

6.2.1 Description

A block diagram of the BIC is shown in Figure 6-1. There are two major functional elements: the Buffer Address Control which maintains the current and final memory addresses for transferred data words, and the Sequence Control which synchronizes data transfer. The BIC sends and receives timing and control signals to and from peripheral controllers through the B Cable.

The BIC is connected to the I/O Cable in the same manner as any other peripheral controller. A typical scheme for connecting peripheral controllers and multiple BIC's is shown in Figure 6-2. The BIC's and peripheral controllers are connected to the I/O Cable in parallel, using standard cables and connectors. An arbitrary number of peripheral devices may be controlled by a BIC by attaching them to the B Cable. All standard 620-series peripheral controllers may be adapted for operation with the BIC. Note that an adapted peripheral controller may be operated directly under program control whenever it is not selected by the BIC.

To perform an operation, the BIC is initialized, under program control, with the Initial and final addresses of the block of data to be transferred; then the desired peripheral device is selected and

Table 6-1
STANDARD DATA 620 PERIPHERALS

MODEL NO.	ITEM	SOFTWARE
620-60	First TTY unit added to computer, ASR-33 with adapter. Reads at 10 cps, punches and types at 10 cps. Operates on- or off-line.	I/O Driver
620-60-1	Second and each additional ASR-33 TTY unit with adapter. Reads 25 cps, types and punches at 10 cps.	I/O Driver
620-61	First TTY unit added to computer, ASR-35 with adapter. Reads at 10 cps, punches and types at 10 cps. Operates on- or off-line.	I/O Driver
620-61-1	Second and each additional ASR-35 TTY unit with adapter. Reads, types, and punches at 10 cps.	I/O Driver
620-11	Byte processing instruction set	DAS
620-13	Real-time clock	I/O Driver
620-15	Buffer Interlace Controller, and one device adapter	I/O Driver
620-15-1	Additional Buffer Interlace Controller device adapter	N/A
620-20	Buffered output channel, 16/18-bit parallel	I/O Driver (Special)
620-21	Buffered input channel, 16/18-bit parallel	I/O Driver (Special)
620-22	Gated input channel, 16/18-bit parallel	I/O Driver (Special)
620-23	Gated output channel, 16/18-bit parallel	I/O Driver (Special)
620-25	Eight external sense lines	N/A
620-26	Eight external control lines	N/A
620-27	Eight priority interrupt lines with arm/disarm facility	N/A
620-30	Magnetic tape control unit and one transport. Includes assembly/disassembly register, IBM-compatible, operates at 45 ips. Dual density, 556 and 800 bpi.	I/O Driver

Table 6-1 (cont'd)
STANDARD DATA 620 PERIPHERALS

MODEL NO.	ITEM	SOFTWARE
620-31	Magnetic tape control unit and master transport to control up to three slaves. Includes assembly/disassembly register, operates at 45 ips. Dual-density 556 and 800 bpi. IBM-compatible.	I/O Driver
620-31-1	Slave transport for model 620-31	I/O Driver
620-32	Magnetic tape control unit and one transport. Includes assembly/disassembly register, IBM-compatible, operates at 75 ips. Dual-density 556 and 800 bpi.	I/O Driver
620-33	Magnetic tape control unit and master tape transport to control up to three slaves. Includes assembly/disassembly register, operates at 75 ips. IBM-compatible, dual-density 556 and 800 bpi.	I/O Driver
620-33-1	Slave transport for model 620-33.	I/O Driver
620-34	Magnetic tape control unit and one transport. Includes assembly/disassembly register, IBM-compatible, operates at 120 ips, dual-density 556 and 800 bpi.	I/O Driver
620-35	Magnetic tape control unit and master tape transport to control up to three slaves. Includes assembly/disassembly register, operates at 120 ips. IBM-compatible. Dual-density 556 and 800 bpi.	I/O Driver
620-35-1	Slave transport for model 620-35.	I/O Driver
620-41	Disc memory master control unit and one disc file. Up to 256K, 16-bit words of storage.	I/O Driver
620-50	Card reader and adapter, 90 CPM.	I/O Driver
620-52	Card punch and adapter, 100 CPM.	I/O Driver
620-56	High-speed Line Printer, 120 columns, 600 LPM, buffered.	I/O Driver
620-57	Medium-speed Line Printer, 120 columns, 300 LPM, buffered.	I/O Driver
620-58	Paper tape reader and adapter. Reads at 300 cps. Reads 5-, 7-, or 8-level tape.	I/O Driver

Table 6-1 (cont'd)
STANDARD DATA 620 PERIPHERALS

MODEL NO.	ITEM	SOFTWARE
620-59	Paper tape punch and adapter. Punches at 60 cps. Punches 5-, 7-, or 8-level tape.	I/O Driver
620-59-1	Paper tape system with common controller. Includes models 620-58 and 620-59.	I/O Driver
620-62	Full duplex interface to Bell 103 Data Set.	I/O Driver
620-70	Model 503 Oscilloscope adapter, 256 x 256 addressable points (without oscilloscope).	I/O Driver
620-75	Digital plotter. Plots at 300 increments per second.	Output Driver and Plot Routines

STANDARD SOFTWARE

DAS . . . Symbolic Assembler
Maintain . . . Maintenance Program
AID . . . On-line diagnostic & utility
Correct . . . Correction of Symbolic programs
FORTRAN . . . ASA Basic FORTRAN
Programmed Arithmetic
Elementary Functions

started by the DATA 620. The BIC then controls data transfers at the rate required by the peripheral device. When the block transfer is complete, the BIC automatically terminates the transfer operation. To handle abnormal conditions such as illegal stops, or situations where the number of words to be transferred is not known in advance, BIC transfers may also be terminated by a signal from the peripheral device.

The BIC is provided with two sense functions to permit testing for proper connection of a selected device, and for an abnormal stop condition.

The BIC is applicable in all types of block I/O operations. Typical uses include control of magnetic tape units, card readers and punches, discs and drums, analog-to-digital converters, etc.

6.2.2 Programming

The Buffer Interlace Controller provides the programmer with the capability of transferring a block of data by specifying the first and final memory addresses of the block, selecting the peripheral device, and starting the transfer. Once initiated, data block transfer is carried out without further program attention.

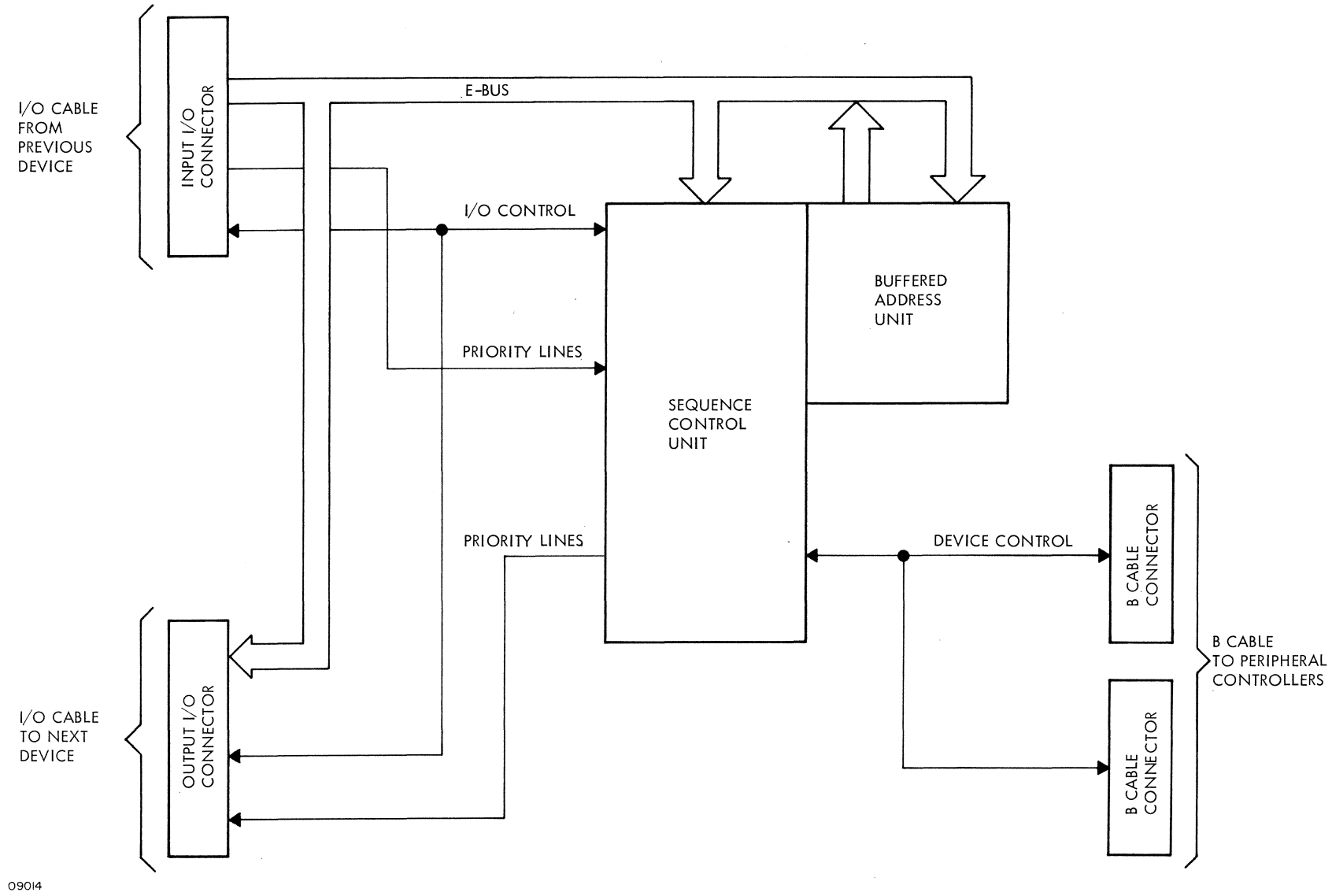


Fig. 6-1 Buffer Interlace Controller, Block Diagram

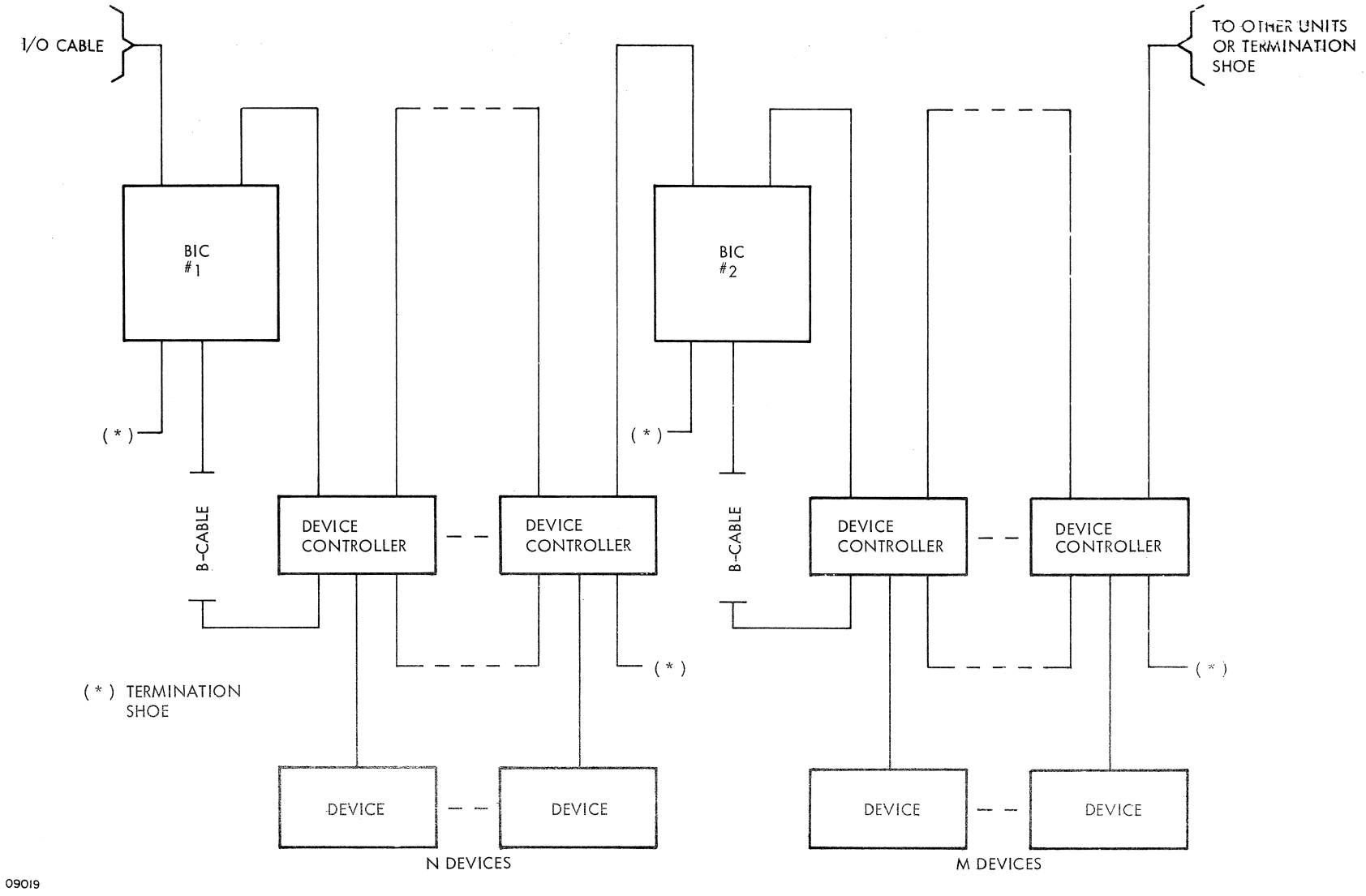


Fig. 6-2 Multiple BIC Cable Connections

There are 15 specific instructions associated with the BIC. These instructions consist of the following:

a. External Control . . . . . 2 instructions

b. Transfer . . . . . 11 instructions

c. Sense . . . . . 2 instructions

Table H-2, Appendix H, lists the instruction codes reserved for use with the first Buffer Interlace Controller added to the computer. Where multiple BIC's are attached to the cable, additional codes are assigned at the time of system definition. An example of programming for the Buffer Interlace Controller is given in Appendix B.

6.3 TELETYPE UNITS AND INTERFACE

6.3.1 ASR-33 Teletype

The ASR-33 Teletype is a standard input/output device. The unit with its controller provides the DATA 620 system with an operator's station with paper tape read and punch, page printing, and keyboard input capability. The ASR-33 may be used in an off-line mode for the listing or generation of paper tapes and in an on-line mode as programmed from the DATA 620.

6.3.2 ASR-33 Teletype Controller

The ASR-33 Teletype Controller (TTC) is connected to the I/O Cable and synchronizes the transfer of information between the ASR-33 and the DATA 620. The controller may be adapted to operate under control of the Model 620-15 Buffer Interlace Controller, permitting information transfer to and from the ASR-33 to be interlaced with program operations. Data transfer under DATA 620 control may be programmed any time the TTC is not operating with the BIC. The data transfer rate depends upon the selected mode of operation.

The TTC operates in four modes: high-speed input (25 cps), low-speed input (10 cps), keyboard input, and low-speed output (10 cps). The mode is specified by the Function Code (bits 6-8) of an External Control (EXC) instruction. The modes and the corresponding Function Codes are summarized in Table 6-2.

Print suppression is provided in the high-speed input mode. Paper tape punching is selected by manually actuating a switch on the ASR-33. To generate an output paper tape from the DATA 620, the operator must manually select the punch and the program must select low speed output mode.

The organization of the ASR-33 Teletype Controller is shown in Figure 6-4. There are two main functional elements, in addition to the line transmitters and receivers used for communication with the I/O and B Cables: (1) the T Register which buffers eight-bit data characters to and from the ASR-33, and; (2) the Timing and Control circuits which synchronize the character transfers. When the controller is operated under program control, the DATA 620 exchanges the data characters by executing the appropriate instruction after sensing that the T Register is ready. When the controller is operated under BIC control, it signals that the T Register is ready to exchange a character with the DATA 620 memory by issuing a transfer request through the B Cable. The BIC then automatically

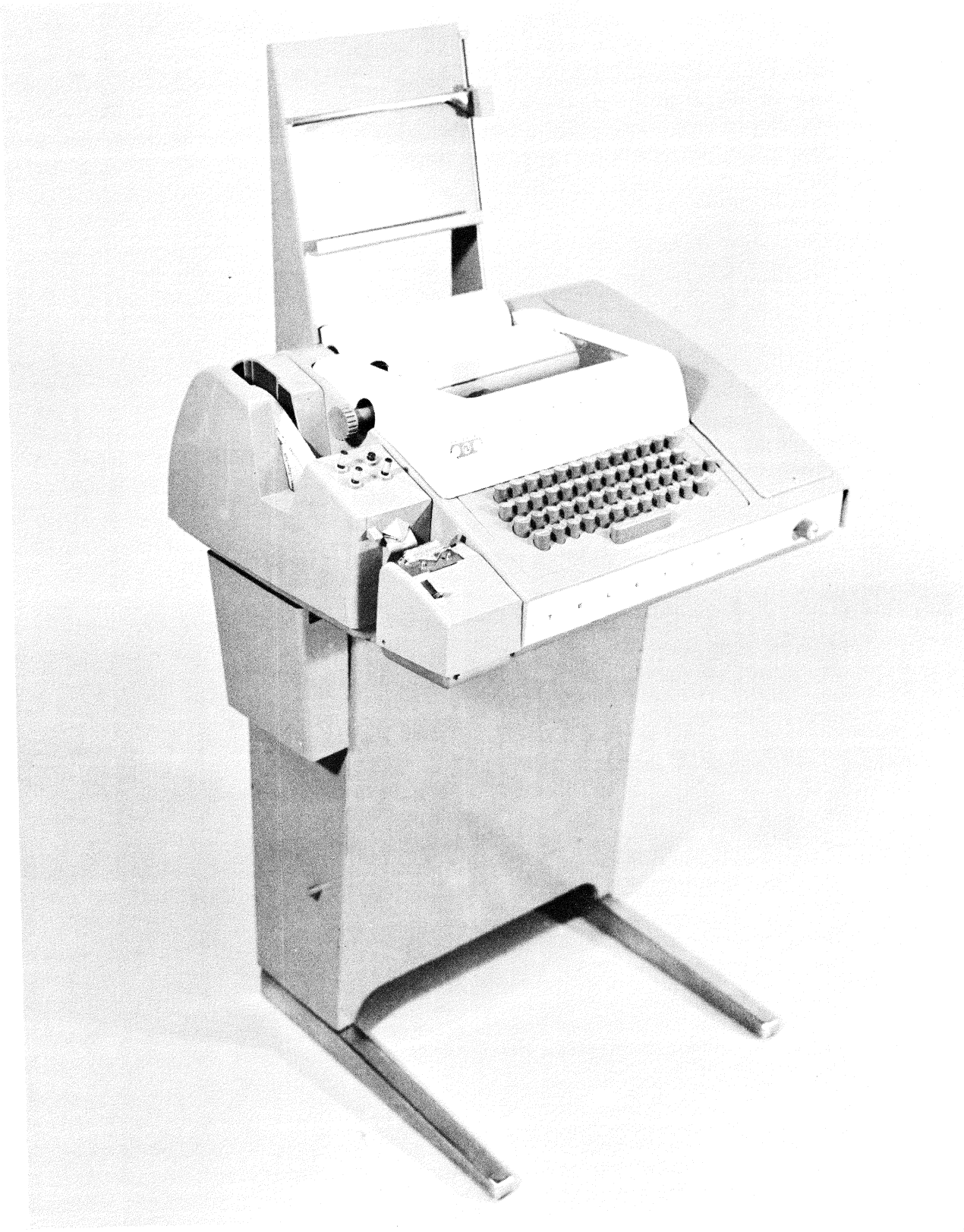


Fig. 6-3 ASR-33 Teletype

addresses the DATA 620 and controls transfer of a character between the memory and the T Register. The controller will be disconnected from the BIC if the requested data block is satisfied or if a read operation is terminated by the ASR-33 (as for an out-of-tape condition).

Table H3, Appendix H, lists the instruction codes reserved for the first TTC added to the system. Where multiple Teletypes are used, additional codes are assigned at the time of system definition. An example of programming techniques for the Teletype is given in Appendix B.

Table 6-2
TTC MODES

MODE	EXC COMMAND FUNCTION CODE			
	Bit 8	Bit 7	Bit 6	Octal
High Speed Input	0	0	0	0
Low Speed Input	0	0	1	1
Keyboard Input	0	1	0	2
Low Speed Output	0	1	1	3
Off/Initialize	1	0	0	4

6.4 CARD READER

The Model 620-50 Card Reader (Figure 6-5) reads standard 80-column punched cards. The card reader is connected to the DATA 620 I/O Cable for operation under program control. The interface includes the external control, sense, and device address decoding and information-gating logic. The Card Reader option may be adapted to operate under BIC control. The full twelve bits of each column are read, permitting the DATA 620 to read either Hollerith-coded or row or column binary data. Utility programs are supplied with the Card Reader. Principal characteristics of the Card Reader are listed below:

DIMENSIONS

18" long, 10-3/4" wide, 8-1/2" high
Weight: approximately 25 lbs.

MECHANICAL

Speed: 90 cards per minute
Read Mechanism: Star Wheels
Hopper Capacity: 500 cards

ENVIRONMENT

40°F to 98°F, 20% to 80% relative humidity

TIMING REQUIREMENTS

7 msec per column

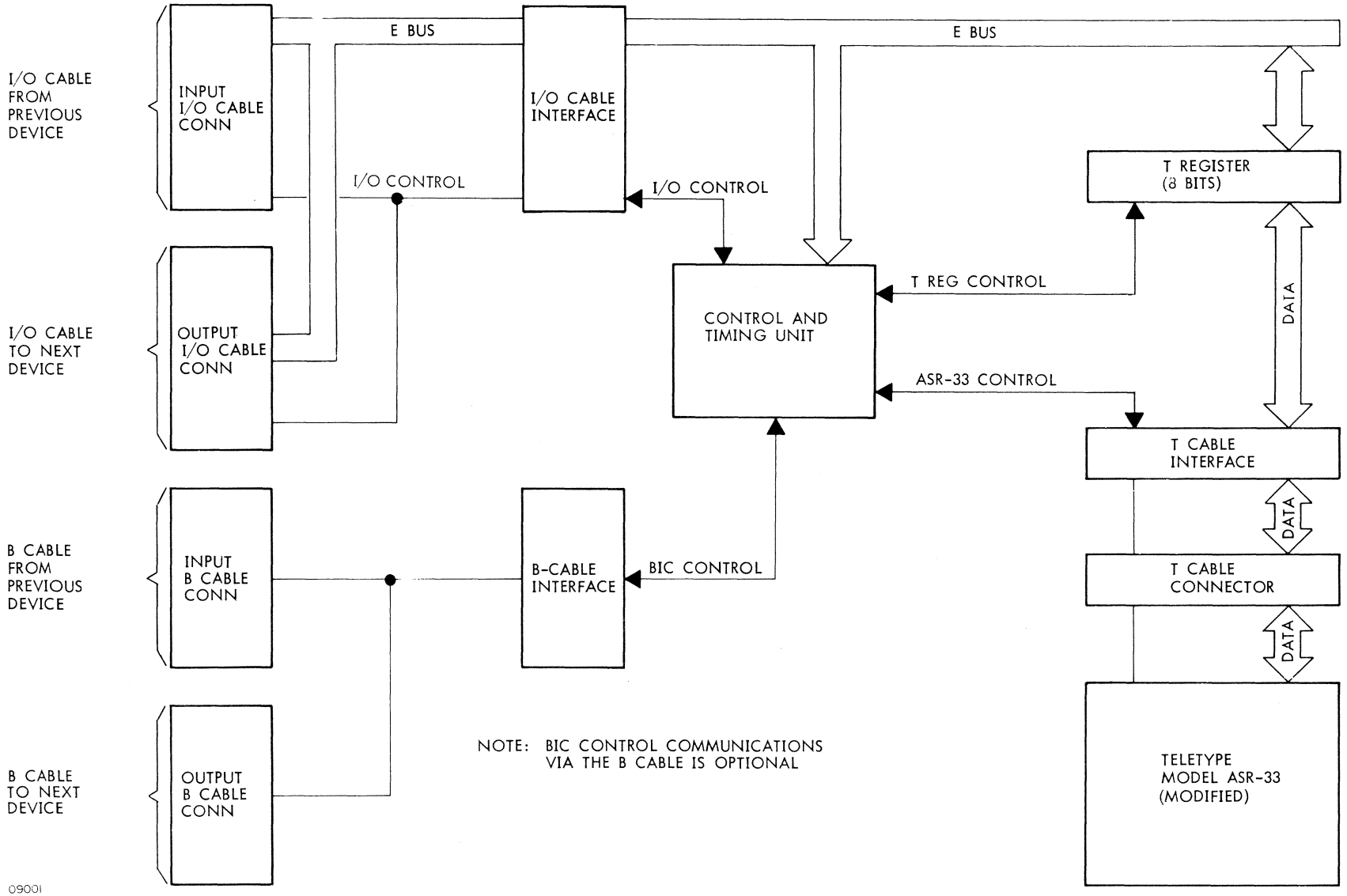


Fig. 6-4 Model 620-60 ASR-33 Teletype Controller, Block Diagram

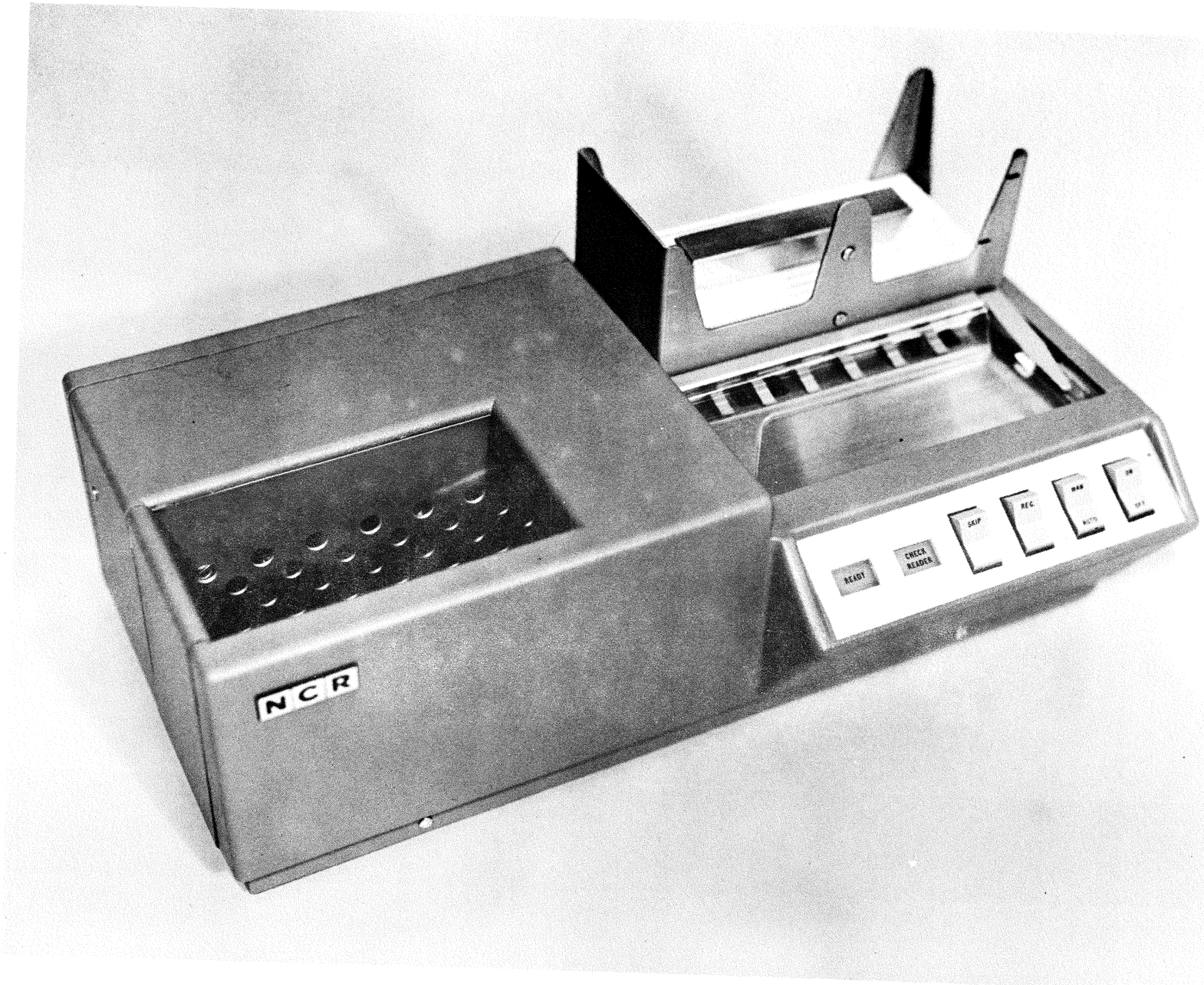


Fig. 6-5 Model 620-50 Card Reader

The controller requires 17 percent of a Model 620-91 connector drawer. The power required is 25 watts for the controller and 150 watts for the Card Reader. The Card Reader option is supplied with a 20-foot cable between the controller and the Card Reader.

The following 10 instructions are associated with the Card Reader:

External Control . . . . . 2 instructions

Transfer . . . . . 5 instructions

Sense . . . . . 3 instructions

Table H-4, Appendix H, lists the instruction codes reserved for use with the first card unit added to the computer. If multiple Card Readers are attached, additional codes will be assigned at the time of system definition.

6.5 BUFFERED INPUT/OUTPUT CHANNELS

The Model 620-21 Buffered Input Channel and the Model 620-20 Buffered Output Channel accept or transmit data, in the parallel mode, to and from the computer through the I/O Bus. Each optional channel is normally operated under program control. Each channel includes transfer instructions, sense lines, and select lines. The channels accept information at the maximum program-control input rate. Output rate is determined by the receiving device.

Each input/output channel is implemented using standard VersaLOGIC modules. Typical applications for these channels might be: (1) output at holding register for D/A Converters, or (2) input buffering for an ADC or switches. A detailed description of the interface may be found in the Interface Reference Manual.

The following six instructions are associated with each input or output channel:

Transfer . . . . . 5 instructions

Sense . . . . . 1 instruction

Table H-6, Appendix H, lists the instruction codes for use with the Buffered Input Channel, and Table H-8 lists the instruction codes for the Buffered Output Channel. The device addresses for the units will be assigned as they are added to the Cable.

6.6 GATED INPUT/OUTPUT CHANNELS

The Model 620-22 Gated Input Cahnnel, and Model 620-23 Gated Output Channel accept or transmit data, in the parallel mode, to and from the computer through the I/O Bus. This optional channel is normally operated under program control and differs from the Buffered Channels in that there is no logic buffering. Each channel includes transfer instructions, sense lines, and select lines. The channels accept information at the maximum program-control input rate. Output rate is determined by the receiving device.

Each input/output channel is implemented using standard VersaLOGIC modules. Typical applications for these channels would be:

- output devices with logic buffering
- displays
- other computers.

The interface is described, in detail, in the Interface Reference Manual.

The following six instructions are associated with each Gated Input Channel:

Transfer . . . . . 5 instructions

Sense . . . . . 1 instruction

The four instructions associated with each Gated Output Channel are as follows:

Transfer . . . . . 3 instructions

Sense . . . . . 1 instruction

Tables H-5 and H-7 in Appendix H list the instruction codes to be used with the Gated Input and Gated Output Channels. Device addresses for the units will be assigned as the units are added to the Cable.

6.7 SENSE LINES

The Model 620-25 Sense Lines are discrete inputs which may be tested by the computer. These lines are available as options in sets of eight lines per module. Up to 512 Sense Lines can be addressed, each with a unique address. All DATA 620 peripheral options include Sense Lines required.

Each Sense Line module is made up of standard VersaLOGIC cards. Sense Lines can be operated in combination with interrupt lines to permit more than one device to share an interrupt line.

There is one double-word addressing instruction associated with each Sense Line. If a signal exists on the Sense Line addressed by the instruction, the computer jumps to the effective address; otherwise, the program continues at location L +2.

6.8 EXTERNAL CONTROL LINES

The Model 620-26 External Control Lines are discrete outputs which may be used under program control. These lines are available as options in sets of eight lines per module. Up to 512 External Control Lines may be addressed, each with a unique address which can be used for control. All DATA 620 peripheral options include required external control lines. External Control Lines may be used for selecting units for operation or for controlling functions such as alarms, etc.

There is one single-word non-addressing instruction associated with each External Control Line. During a program sequence, an External Control (EXC) instruction is executed to output a 450-nsec pulse on the addressed line.

6.9 PRIORITY INTERRUPTS

6.9.1 General Description

Interrupts are available, in four standard options, as listed below:

Option	No. of Interrupts	Type of Interrupt
Model 620-27	8	dc
Model 620-27A	8	ac
Model 620-27B	16	dc
Model 620-27C	16	ac

The dc-type of interrupt can service level-type interrupt requests which can be maintained until acknowledged. The ac-type of interrupt has a latching register for storing pulse-type interrupt requests until serviced. Each interrupt line has a unique pair of memory addresses or locations assigned for 16 interrupts in a module; 32 consecutive memory locations are reserved for interrupt instructions. This block may be located in memory by using combinations of two bits for address generation.

When an interrupt is received, the interrupt module presents an interrupt request to the DATA 620 if the module is enabled and has priority. When the computer responds with an interrupt acknowledge, the module places the first address of the pair of locations associated with the requesting interrupt line on the E Bus. The DATA 620 then executes the instruction contained at the addressed location. The instruction executed may be any one of the DATA 620 repertoire.

If the interrupt address contains a Jump-and-Mark instruction, further interrupt processing is inhibited. This is accomplished by the DATA 620 which disables the interrupt modules with the Interrupt Jump signal, IUJP. The modules are then enabled under program control.

Features and characteristics of this option are described in the following paragraphs.

6.9.2 Clear AC Interrupt Register

When using the ac interrupt option, it is desirable to be able to clear the module of unserviced interrupts. This is done by the clear ac command (refer to Table H-1). The ac interrupt register is also cleared by the INITIALIZE command or by means of the DATA 620 console SYSTEM RESET pushbutton.

6.9.3 Interrupt Signal

An interrupt signal for the dc interrupt is a level of -12 V, (0 V on the I/O Cable). For the ac type, the interrupt signal is a positive-going transition from -12 V to 0 V (0 to -6 V on the I/O Cable). Interrupt signals may originate at spare lines in the I/O Cable, or from lines connected through an auxiliary input cable connector.

6.9.4 Priorities

The relative priorities of the interrupt lines are established by hardware but are easily changed by moving jumpers on a terminal strip in the module. The standard order of priorities ranks the interrupt line IL00 as highest, with descending priority for ascending line number.

The priority of the interrupt module relative to other devices is established either by physical placement on the I/O Cable, or by a priority line wiring technique (refer to the Interface Reference Manual). Normally, the system priorities are (in descending order):

- Power Fail Interrupt (not on the I/O Cable)
- Real Time Clock
- Buffer Interlace Controller(s)
- Interrupt Module(s)
- Console Interrupt (not on the I/O Cable)

6.9.5 Interrupt Addresses

Each interrupt line has a unique pair of memory addresses associated with it. (Two address locations are required for possible use with double-word instructions.) An interrupt module with 16 interrupts is assigned a block of 32 consecutive memory addresses. The location of the block is determined during system design but may be easily changed by moving jumpers in the module. Two extra line driver elements are provided to drive any pair of higher-order E Bus lines. Thus, for a module with 16 interrupts, the interrupt address generator drives EB00 through EB04, while the extra line drivers can drive any E Bus line above EB04.

6.9.6 Hardware

Each standard interrupt option requires one standard VersaLOGIC card bin and two I/O connectors (104-pin Concoa). The interrupt module connects only to the DATA 620 I/O Cable.

6.9.7 Programming

The interrupt module is a bilateral device which receives mask words and external control commands from the DATA 620 and, in return, sends memory addresses associated with particular interrupts. The four external control commands and three output transfer commands associated with an interrupt module are listed in Table H-1.

6.10 HIGH-SPEED PAPER TAPE READER

The Model 620-58 Paper Tape Reader reads 5-, 7-, or 8-level paper tape at 300 characters per second. The reader is available by itself, or in combination with the Model 620-59 Paper Tape Punch, to form a high-speed paper tape input/output system (Model 620-59-1).

The reader inputs data in an 8-bit character format (leading zeros for 5- and 7-level tape) and can be operated in a continuous or step-read mode. The step-read mode, with one character for each read command, is particularly useful in real-time applications.

Options include spoolers or fan-fold bins for improved tape handling, and an adapter to permit operation with a Buffer Interlace Controller.

Refer to Table H-9 for applicable codes to operate the reader.

6.11 HIGH-SPEED PAPER TAPE PUNCH

The Model 620-59 Paper Tape Punch perforates 5-, 7-, or 8-level paper tape at 60 characters per second. The punch is available by itself or in combination with the Model 620-58 Paper Tape Reader to form a high-speed paper tape input/output system (Model 620-59-1).

The punch accepts data in a 5-, 7-, or 8-bit character format and operates in a single-step mode. Either roll or fan-fold tape may be used; the punch will hold 1000 feet of either. A take-up spooler or fan-fold bin is provided to accumulate the tape as it is punched.

Options include a 120-cps perforating rate and an adapter to permit operation with a Buffer Interlace Controller.

Refer to Table H-9 for applicable codes to operate the punch.

6.12 MAGNETIC TAPE UNIT (120-IPS)

The Model 620-34 Magnetic Tape Control Unit and Transport is a complete operating unit with power supplies, read/write electronics, control electronics, enclosure, and operators' control panel. It provides tape speeds of 120 ips with dual packing density of 556 and 800 bpi.

The Magnetic Tape Control Unit allows flexible interfacing between the DATA 620 I/O Bus and the Magnetic Tape Transport, allowing the standard tape unit commands to be performed by the user. The unit contains two 16- or 18-bit word buffers. (The Magnetic Tape unit will work with either 16- or 18-bit computers.) The Magnetic Tape Control Unit requires only seven inches of rack space and consumes only 75 watts (approximately). The unit is supplied with a 25-foot cable for connection to the Tape Transport.

The double-word buffering allows the computer an average servicing rate of 32 kc for high density (800 bpi), and 22 kc for low density (556 bpi). In the 18-bit version both BCD and binary modes allow three characters per word. The 16-bit model allows two characters per word BCD (right-justified) and three characters per word in the binary mode (leftmost character has four bits of information).

The Model 620-34 Tape System may be connected to a Model 620-15 Buffer Interlace Controller (BIC). When operating in the optional BIC mode, less than 3.6 microseconds are required to service the tape unit buffer. The remaining time (either 30 μsec or 45 μsec) is available for concurrent computation or additional input/output.

6.12.1 Description

Specifications for the Model 620-34 120-ips Magnetic Tape System are as follows:

SPECIFICATION	CHARACTERISTICS
Tape Speed:	120 ips
Tape Width and Thickness:	1/2 inch wide, 1.5-mil by 2400 feet (Ampex types 832, 838) or 1.0-mil by 3600 feet
Tape Reels:	10-1/2 inch IBM or NAB type
Packing Densities:	556, 800 bpi (two front panel selectable densities)
Standard Recording Formats:	7-track, NRZ, 3/4 inch IRG (IBM compatible)
Rewind Speed:	120 seconds maximum (for 2400 feet of tape)
Start/Stop Time:	3.8 milliseconds maximum
Turn-around Time:	11 milliseconds maximum
Instantaneous Speed Variation:	120 ips ± 2%
Interchannel Time Displacement at 120 ips:	3.9 microseconds (with any 1/2 inch, 1.5-mil tape)
Input Voltage and Frequency:	115 V ± 10%, 60 ± 2 cps, 1.2 KVA
Operating Environment:	Ambient temperature: +40° to +100°F (5°C to 38°C) Relative humidity: 20% to 80% (with no condensation)

6.12.2 Operating Controls

The 620-34 Magnetic Tape System operating and remote controls are designed to accept tape input control signals, provide output control signals, and acknowledge signals to the computer equipment. All

required tape command interlocks are provided to ensure that erroneous command sequences will not cause tape damage or any other malfunction. Controls also include the logic for Rewind to Load Point, File Protect and other computer-oriented functions. An operator control panel is supplied with the unit for local operation and indication. Indicators show the status of the system under both "local" and "remote" command conditions.

Power Switch and Indicator

In the ON position, the transport and its control logic is activated. In the OFF position, the transport and its control logic is deactivated and all power to the transport is off.

Remote Switch and Indicator

When this momentary switch is pressed, the remote indicator lights up "white". When in remote, if select to the transport is true, the remote indicator lights up "red". When in remote and when select is true, all input and output lines to the transport are enabled, the local state is reset and the local indicator is turned off.

Local Switch and Indicator

When this momentary switch is pressed (and "transport ready" is true), the transport is conditioned to accept control commands generated by the local switches only. The remote state is reset and remote indicator turned off. When power is first applied, or "transport ready" is false, the transport is automatically set to the local state.

Stop Switch

When this momentary contact switch is pressed, the tape is unconditionally stopped and the transport set to local state.

Forward to Load Point Switch

This momentary switch is used in normal operation when a new file reel is mounted. When the switch is pressed, tape is automatically loaded into the vacuum chambers, driven in the forward direction, and stopped automatically at the load point. If the tape is already loaded and the switch is then pressed, the tape will be driven in the forward direction. This switch is enabled only in the local state.

Reverse Switch

When this momentary contact switch is pressed, the tape is driven in the reverse direction and stops automatically at the load point. If the tape is at the load point and the switch is pressed, the tape is driven in the reverse direction to the physical beginning of the tape.

Rewind to Load Point Switch

When this momentary switch is pressed, the tape is driven at rewind speed in the reverse direction until it stops automatically at the load point. If the tape is at the load point and the switch is pressed, the command is ignored. This switch is enabled only in the local state.

High/Low Density Switch and Indicator

This switch selects one of two density modes. Provisions are made to indicate the mode selected.

File Protect Indicator

When this indicator is illuminated, no writing is permitted on the tape unit. It is on when: (a) no file is mounted, or (b) a file reel is mounted which does not have a write enable ring.

6.12.3 Tape Format

The Tape Format is standard IBM 729-2 format with 3.75-inches from load point to first record gap, 3/4-inch record gap, and 3.7-inch end-of-record to file mark gap. Longitudinal check character gap is three missing characters.

Two types of parity checking are used, longitudinal and lateral. Longitudinal parity is always even (in either the BCD or binary modes). Even parity means if there is an even number of bits in the record for that channel, a zero will be written in the corresponding longitudinal parity character. If an odd number of bits exists, a one will be written in the check character. With lateral parity, one parity bit is carried with each character. Even parity is used for the BCD mode and odd parity for the binary mode.

6.12.4 Programming

There are eight External Control and eight Sense instructions used by the tape controller. These are described below and are summarized in Table H-10 of Appendix H.

6.12.4.1 External Control Instructions. The computer uses the following eight different external control commands (EXC) to control the operation of the Magnetic Tape System:

Read One Record Binary

This command sets the tape unit in the forward direction. The characters are read serially and form words in one of the two word buffers. After the first word is formed, the word is transferred to the second word buffer and the buffer-ready flip-flop is set. This flip-flop may be tested by a sense command. The information is transferred to the computer by an input instruction or through the use of the optional BIC. The parity error flip-flop is set if any character exhibits lateral parity error or the longitudinal parity check does not compare. If a file mark is detected, the file mark flip-flop is set. This may be tested by a sense instruction.

Read One Record BCD

Same as Read One Record Binary, except even parity is used for lateral parity checking.

Forward One Record

Same as Read command except no information is transferred to the computer. This command allows the tape unit to be moved forward one record without using computer time.

Write One Record Binary

This command places the Magnetic Tape unit in forward drive and starts writing after 3.8 milliseconds. Before writing, an output command must be given to load the word buffer. Whenever the buffers detect that no data is available for writing, a normal stop sequence is initiated. This involves writing longitudinal parity and spacing for end-of-record gap. The tape unit always stops with writing head 0.225 inches from the next start-of-record.

Care must be taken in writing after a backspace command. This restriction is due to the spacing of an end-of-file character. Before writing, a tape unit must have gone forward one record unless the backspace command did not detect a file mark.

Write One Record BCD

This command is the same as the write binary command except that even parity is written. The Magnetic Tape Driver subroutine translates the ASCII characters to IBM-compatible form. In the 18-bit version, three characters are written per word; two are used in the 16-bit version.

Write File Mark

This instruction writes the file mark character (0001111) with the required 3.7-inch gap in front of it. No data is transferred with this instruction. Even parity is used and the longitudinal parity character is the same as the file mark character.

Backspace One Record

This command allows the tape unit to backspace one record. The record may be data or a file mark character. No data is transferred during this command.

Rewind

This command rewinds the tape unit to the Load Point.

6.12.4.2 Sense commands. The following eight Sense commands are available with the Model 620-34 Magnetic Tape System:

Sense Parity

This command tests the parity error flip-flop or the longitudinal parity character to determine if a reading error has occurred. This command should be used at the conclusion of each forward movement of the tape unit. Checking this command during tape reading determines if parity has been read to that point in time. The parity flip-flop remains set until the next command is given to the Magnetic Tape Unit.

Sense Buffer Ready

A true condition indicates that the buffer contains information to be read, if in the input mode, or that the buffer is ready to receive data, if in the output mode. This flip-flop is reset after the action is performed by the computer.

Sense Tape Unit Ready

A true condition indicates that the tape unit is ready, stopped, and in the remote mode. The Tape Unit Ready Sense will indicate a TRUE condition if the tape unit is rewinding (see Sense Rewinding).

Sense High Density

A true condition indicates the tape unit is selected in the high density mode (800 bpi), and a false condition indicates a low density mode (556 bpi).

Sense End of Tape

A true condition indicates the Magnetic Tape has passed the EOT photosensitive tape mark located on the tape. The flip-flop is set when the EOT passes by and is reset with a rewind command.

Sense Beginning of Tape

A true signal indicates the tape is positioned at the photosensitive Load Point mark.

Sense Rewinding

A true condition indicates the tape unit is rewinding. (Note: the rewinding signal will not become true for approximately 5 μsec after a rewind command.)

Sense File Mark

When an end-of-file mark sequence is detected, the end-of-file mark flip-flop is set and may be tested by this command. An end-of-file mark may be detected by either a read command or the forward command. The flip-flop is reset with any Magnetic Tape command.

APPENDIX A
DATA 620 NUMBER SYSTEM

DATA 620 NUMBER SYSTEM

Binary numbers in the DATA 620 are represented in 2's-complement form. Single-precision numbers are 15 bits plus sign (16-bit configuration) or 17 bits plus sign (18-bit configuration). The sign bit occupies the most-significant bit position (15 or 17). A "0" in the sign position denotes a positive number; a "1" in the sign position denotes a negative number. The negative of a positive number is represented in 2's-complement form.

The 2's-complement of a number may be found in either of two ways:

a. Take the 1's-complement of the number (i.e., complement each bit); add "1" in the least-significant bit position. Example:

+9	0000000000001001
1's-complement	1111111111110110
	+ 1
2's-complement (-9)	1111111111110111

b. For an n-bit number (including sign) subtract it from 2^{n+1}. Example:

2^{n+1}	10000000000000000
-(+9)	-0000000000001001
-9	1111111111110111

It is generally convenient to express binary numbers by their octal equivalent. This conversion is easily performed by grouping the binary bits by threes, starting with the least-significant bit. Thus, in the 18-bit configuration, numbers may be expressed by six full octal digits (000000-777777_8).

In the 16-bit configuration, the range of octal numbers is less than six full digits (000000-177777_8). The octal equivalents for the above examples are:

Decimal	Octal
+9	000011_8
-9	177767_8

The range of numbers in the DATA 620 is from -2^{15} to $+2^{15}-1$ for the 16-bit configuration and -2^{17} to $+2^{17}-1$ for the 18-bit configuration. The zero minus 1 and plus/minus full-scale numbers for the 16-bit configuration are:

Binary	Octal	Decimal	
0111111111111111	077777_8	+32,767	+ Full Scale
0000000000000000	000000	0	0
1111111111111111	177777_8	-1	-1
1000000000000000	100000_8	-32,768	- Full Scale

The negative of the octal equivalent number is found by subtracting the number from 177777_8 and adding 1 in the least-significant digit (subtract from777777_8 for the 18-bit configuration). Example:

	177777_8
-(9)	-000011_8
	+1
(-9)	177767_8

In performing addition or subtraction, it is possible for the results to exceed the ± full scale range of the machine. For example:

Decimal	Octal	
+21,980	052734_8	
+11,843	$+027103_8$	
33,823	102037_8	-31,713

The negative result is in error. The same type of error occurs if the sum of the two negative numbers exceeds the minus full-scale range:

Decimal	Octal	
-21,980	125044_8	
(+)-11,843	150675_8	
-33,823	(1)075741	31,803

Note that the carry out of the most-significant octal digit position is generally lost. However, to inform the Programmer that the true result of an addition/subtraction falls outside the range of the machine, an overflow indicator is provided. The overflow indicator is set if the sign bit changes when two numbers of the same sign are added together (where the sign of the subtrahend is changed in subtraction).

In multiplication, a double-length product is formed in the arithmetic registers (A or B). Since the product cannot exceed 32-bits (36-bits in the 18-bit configuration), overflow will never occur as the result of a multiply. The sign of the product is automatically determined.

Example:

Decimal	Octal
21,980	052734
X 11,843	027103
65,940	200624
87,920	52734
175,840	454404
21,980	125670
21,980	
260,299,140	001741000224
	A B

The double-length result is accumulated in the A and B registers.

In division, an overflow (underflow) can occur if the divisor is less than or equal to the dividend.

APPENDIX B
PROGRAMMING EXAMPLES

PROGRAMMING EXAMPLES

PROCEDURE TO BOOTSTRAP PROGRAM INTO MEMORY

a. Manually enter, through the control console, the 10-instruction "Bootstrap Loader" sequence.

b. Set console registers as follows:

(AR) = 10101010 10101010 binary

(BR) = 0

(XR) = Storage address of program

(IC) = Entry address of "Bootstrap Loader" sequence

c. Position the paper tape containing the program in the ASR33/35 Teletype paper tape reader. The first frame containing data should be at the read position. The format of this paper tape is such that each two successive 8-bit frames make up a word.

d. RUN. The tape will feed completely through the reader. When this happens press the STEP switch, set (IC)= storage address of program, and RUN. The first four instructions of this program must be as follows:

PI	SEN 100	P2	SENSE BUFFER READY
	JMP	P1	REPEAT
P2	SEL 400		SELECT TTY OFF
	HLT		

e. JMPM Read.

```
READ , ENTR ,          ENTRY POINT FOR READ ROUTINE
     , SEL  ,0         SELECT HI SPEED TTY INPUT
B1   , SEN  ,0100,B2   GO TO B2 WHEN BUFFER READY
     , JMP  ,B1        BUFFER BUSY - WAIT UNTIL FREE
B2   , LRLB ,8         TOP 8 BITS ROTATED TO RIGHT
     , LSRB ,8         CLEAR THESE BITS
     , LRLB ,8         POSITION FOR INPUT
     , INB  ,          INPUT TO B RESGISTER
     , LRLA ,1         SHIFT (ROTATIONAL) A LEFT 1 BIT
     , JAP  ,B1        GET SECOND HALF OF DATA WORD
     , STB  ,0,1       STORE ASSEMBLED WORD IN CORE
     , IXR  ,          INCREMENT X REGISTER
     , JMP  ,B1        PROCESS NEXT WORD OF INPUT
```

CALLING SEQUENCES

The following pages illustrate two program sequences for calling subroutines. The first sequence shows a parameter being passed to the subroutine through a register. This sequence has a single return from the called subroutine. The second sequence shows the subroutine parameters being provided following the Jump-and-Mark instruction. This sequence also contains multiple returns from the called subroutine.

```
*  PROGRAM WITH SUBROUTINE CALLING SEQUENCES



     , LDB  ,PAR              PLACE PARAMETER IN B
     , CALL ,SUB1             PERFORM JMPM TO SUBROUTINE SUB1
     , STA  ,TEMP            STORE RESULT IN TEMP, RESULT RETURNED
*                            IN THE A REGISTER


     , CALL ,SUB2,(PAR1)*,(PAR2)      CALL ON SUBROUTINE
     , JMP  ,ERR                      JUMP TO ERROR RETURN RTN
     , LDX  ,C1              NORMAL RETURN - PICK UP VALUE



* SUBROUTINE SUB1
*
SUB1 , ENTR ,                ENTRY POINT TO SUBROUTINE
     , TZA  ,                ZERO A REGISTER
     , LRLA ,3               PLACE THREE HIGH ORDER BITS OF
*                            B IN A AND RETURN TO CALLING PROGRAM
     , RETU*,SUB1
```

```
*  SUBROUTINE SUB2.  THE ARGUMENTS ARE THE ADDRESS OF
*  PARAMETER PAR1, WITH AN INDIRECT FLAG, AND THE
*  ADDRESS OF PARAMETER PAR2, WITHOUT AN INDIRECT FLAG.



SUB2 , ENTR ,              ENTRY POINT TO THE SUROUTIN
     , LDA* ,SUB2          LOAD INDIRECT THROUGH ADDRESS OF
*                          PARAMETER PAR1.  THIS IS ALSO AN
*                          INDIRECT FLAGGED ITEM, SO WE GET THE
*                          VALUE OF PAR1 TO THE A REGISTER
     , INR  ,SUB2          POINT TO ADDRESS OF PAR2
     , LDX* ,SUB2          GET ADDRESS OF PARAMETER 2 TO X
     , LDB  ,0,1           GET VALUE OF PAR2 TO THE B REGISTER
     , MERG ,031           MERGE (LOGICAL OR) A AND B, RESULT TO A
     , JAZ  ,*+2           ERROR CONDITION - NOT ANY BITS
     , INR  ,SUB2
     , INR  ,SUB2          POINT AT NORMAL OR ERROR RETURN
     , RETU*,SUB2          BACK TO ERROR OR NORMAL RETURN
```

```
* SQFN
* PURPOSE ...
* TEST A REGISTER SIGN.  IF ZERO TAKE FIRST ERROR
*  RETURN, IF NEGATIVE TAKE SECOND ERROR RETURN,
*  OTHERWISE TAKE NORMAL RETURN AFTER NORMALIZING
*  CONTENT OF A REGISTER AND ADDING PARAMETER VALUE
*  LOCATED IN CELL 'Y' TO COUN.  ALSO RESERVE
*  A CELL IN COMMON FOR COUN.
     , ORG ,03000
*                          BEGIN ROUTINE AT 3000 OCTAL
SQFN , ENTR ,              ENTRY POINT
     , LDA* ,SQFN          GET VALUE OF ARGUMENT
     , INR  ,SQFN          SET TO ERROR RETURN 1
     , JAZ* ,SQFN          ERROR TYPE 1
     , INR  ,SQFN
     , JAN* ,SQFN          ERROR TYPE 2
     , INR  ,SQFN          SET FOR NORMAL RETURN
     , CALL ,SQFN          PERFORM SQUARE ROOT FUNCTION
     , LDA  ,COUN          GET VALUE
     , ADD  ,0,1           INDEX SET BY RTN SQFN
     , STA  ,COUN
     , USE  ,COMN          USE THE COMMON LOC COUNTER
COUN , BSS  ,1             DEFINE AN AREA IN COMMON FOR COUNT
     , USE  ,PREV          RESET LOC COUNTER
     , RETU*,SQFN          NORMAL RETURN
     , MORE ,              ANOTHER INPUT TAPE MAY FOLLOW
     , END  ,BEGN          NO MORE - EXECUTE AT BEGN
```

```
*   SQN ROUTINE
*   PURPOSE...
*   SQUARE ROOT NORMALIZE A (KNOWN POSITIVE) NUMBER IN
*   THE A REGISTER AND RECORD THE NUMBER OF 2 PLACE
*   SHIFTS RQD.  THIS IS PLACED IN COUN.  NORMAL RANGE
*   IS 1/4 .LE. (CONTENT OF A) .LE. 1
SQN   , ENTR ,                    ENTRY POINT
      , DECR ,02                  PUT -1 (ALL BITS) IN B
      , STB  ,COUN
      , TZB  ,                    ZERO B REGISTER
      , LLRL ,2
      , INR  ,COUN
      , JIF  ,AP+BZ,*-4+16        IF A POSITIVE AND B ZERO
AP    , EQU  ,02
BZ    , EQU ,020
*                                 BOTH CONDITIONS MUST BE MET
*                                 A POSITIVE AND B ZERO
      , LLRL ,16-2                EFFECT A ROTATE RIGHT 2
      , RTN* ,SQN                 DONE
*
*
*
*   ANOTHER VERSION FOLLOWS
*
*
SQN   , ENTR ,
      , DECR ,02
      , STB  ,COUN
      , TZB  ,
      , LLRL ,2
      , JIF  ,020,*-4             IF B = 0
      , RETU*,SQN
```

```
*     SAMPLE OF DATA 620 PROGRAMMING USING CONDITIONAL
*     ASSEMBLY FEATURES
*
P     , SET  ,0100
Q     , SET  ,0200        INITIAL VALUES OF FLAG VALUES
      , ORG  ,06000         ORIGIN PROGRAM AT 6000 OCTAL
BEGN  , LDA  ,=3            PLACE A THREE IN THE A REGISTER
      , INCR ,02+04         SOURCE OF ZERO TO B AND X, B = X = 1.
      , STA  ,INTL          SET INITIAL COUNT AT 3
      , IFT  ,P,,Q          IF P NOT EQUAL Q (PREV SET VALUES P AND Q)
      , LDA  ,P             A = CONTENT OF P
      , IFT  ,P,,Q          IF P NOT EQUAL Q
      , STA  ,Q             IF UNEQUAL WE RESET Q EQUAL TO P
*
*
      , NOP ,             LEAVE SPACE OF ONE WORD
CYCL  , LDX  ,=7            PLACE A SEVEN IN X
      , TZA ,               ZERO THE A
      , STA ,TBL,1          ZERO TO TBL+CONTENT OF X
SPCL  , BEGI,0100           SET UP POINTERS
      , USE ,SPCL           SET UP AT 0100
      , DATA,1
      , USE  ,PREV          BACK AGAIN
      , STB ,TBM,1          ONE TO TBM+CONTENT OF X
      , DXR ,               DECREMENT X REGISTER
      , CPB ,               PERFORM TWOS COMPLIMENT OF B
      , IBR ,
      , JXZ ,*+4            SKIP OUT WHEN X IS ZERO
      , JMP ,CYCL+2         BACK AGAIN
      , IBR  ,              B = 2
      , STB  ,TBM           TABLE TBM LAST WORD IS A 2
      , STA  ,TBL           ZERO LAST WORD OF TABLE TBL
      , CALL ,PROC,(TBL),(TBM),(ERR)*
      , INCR ,07            TURN ON ALL REGISTERS, SET AS 1 FOR
*                           A FLAG
      , HLT  ,
ERR   , DATA ,(ERST)        ADDRESS OF ERROR STOP
      , USE  ,COMN          ERROR STOP IN COMMON AREA
ERST  , DECR ,07            ERROR INDICATOR, ALL LIGHTS ON
      , HLT  ,
      , LDA* ,PROC
      , JMP  ,FIRS          BACK AGAIN AFTER ERROR
INTL  , BSS  ,1
TBL   , DATA ,0
      , DUP  ,7             MAKE SEVEN COPIES OF NEXT LINE
      , DATA ,0
TBM   , NULL ,              DEFINE LABEL HERE
      , DUP  ,4,2           DUPLICATE NEXT 2 LINES FOUR TIMES
      , PZE  ,1
      , MZE  ,1
      , USE  ,PREV          BACK TO UPPER MEMORY
```

```
P     , SET  ,5
R     , SET  ,(TBL-TBM)     IF TBL FIRST IN CORE THIS IS NEG
      , SMRY ,              DO NOT SHOW DETAILS EXCEPT ASSEMBLED
*                           CODE - PROCESS TBL, TBM TESTING
      , IFT  ,R,0,0         IF R NEGATIVE
      , GOTO ,N1
      , GOTO ,N2
N1    , NULL ,
Q     , SET  ,P+1
      , GOTO ,N3
N2    , CONT ,
Q     , SET  ,P
      , GOTO ,N4
N3    , NOP  ,              INCLUDED IF TABLE TBL FIRST IN MEMORY
N4    , ORG  ,P*01000+050   SET UP ORIGIN
FIRS , HLT  ,
      , DETL ,
      , JMP  ,BEGN
      , DATA ,'PAGE NO.';0
      , END  ,BEGN
```

APPENDIX C
TABLE OF POWERS OF TWO

Table of Powers of Two

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125

APPENDIX D
OCTAL-DECIMAL INTEGER CONVERSION TABLE

OCTAL-DECIMAL INTEGER CONVERSION TABLE

0000 to 0777 (Octal)	0000 to 0511 (Decimal

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0315	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

1000 to 1777 (Octal)	0512 to 1023 (Decimal)

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0614	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

OCTAL-DECIMAL INTEGER CONVERSION TABLE

	0	1	2	3	4	5	6	7
2000	1024	1025	1026	1027	1028	1029	1030	1031
2010	1032	1033	1034	1035	1036	1037	1038	1039
2020	1040	1041	1042	1043	1044	1045	1046	1047
2030	1048	1049	1050	1051	1052	1053	1054	1055
2040	1056	1057	1058	1059	1060	1061	1062	1063
2050	1064	1065	1066	1067	1068	1069	1070	1071
2060	1072	1073	1074	1075	1076	1077	1078	1079
2070	1080	1081	1082	1083	1084	1085	1086	1087
2100	1088	1089	1090	1091	1092	1093	1094	1095
2110	1096	1097	1098	1099	1100	1101	1102	1103
2120	1104	1105	1106	1107	1108	1109	1110	1111
2130	1112	1113	1114	1115	1116	1117	1118	1119
2140	1120	1121	1122	1123	1124	1125	1126	1127
2150	1128	1129	1130	1131	1132	1133	1134	1135
2160	1136	1137	1138	1139	1140	1141	1142	1143
2170	1144	1145	1146	1147	1148	1149	1150	1151
2200	1152	1153	1154	1155	1156	1157	1158	1159
2210	1160	1161	1162	1163	1164	1165	1166	1167
2220	1168	1169	1170	1171	1172	1173	1174	1175
2230	1176	1177	1178	1179	1180	1181	1182	1183
2240	1184	1185	1186	1187	1188	1189	1190	1191
2250	1192	1193	1194	1195	1196	1197	1198	1199
2260	1200	1201	1202	1203	1204	1205	1206	1207
2270	1208	1209	1210	1211	1212	1213	1214	1215
2300	1216	1217	1218	1219	1220	1221	1222	1223
2310	1224	1225	1226	1227	1228	1229	1230	1231
2320	1232	1233	1234	1235	1236	1237	1238	1239
2330	1240	1241	1242	1243	1244	1245	1246	1247
2340	1248	1249	1250	1251	1252	1253	1254	1255
2350	1256	1257	1258	1259	1260	1261	1262	1263
2360	1264	1265	1266	1267	1268	1269	1270	1271
2370	1272	1273	1274	1275	1276	1277	1278	1279

	0	1	2	3	4	5	6	7
2400	1280	1281	1282	1283	1284	1285	1286	1287
2410	1288	1289	1290	1291	1292	1293	1294	1295
2420	1296	1297	1298	1299	1300	1301	1302	1303
2430	1304	1305	1306	1307	1308	1309	1310	1311
2440	1312	1313	1314	1315	1316	1317	1318	1319
2450	1320	1321	1322	1323	1324	1325	1326	1327
2460	1328	1329	1330	1331	1332	1333	1334	1335
2470	1336	1337	1338	1339	1340	1341	1342	1343
2500	1344	1345	1346	1347	1348	1349	1350	1351
2510	1352	1353	1354	1355	1356	1357	1358	1359
2520	1360	1361	1362	1363	1364	1365	1366	1367
2530	1368	1369	1370	1371	1372	1373	1374	1375
2540	1376	1377	1378	1379	1380	1381	1382	1383
2550	1384	1385	1386	1387	1388	1389	1390	1391
2560	1392	1393	1394	1395	1396	1397	1398	1399
2570	1400	1401	1402	1403	1404	1405	1406	1407
2600	1408	1409	1410	1411	1412	1413	1414	1415
2610	1416	1417	1418	1419	1420	1421	1422	1423
2620	1424	1425	1426	1427	1428	1429	1430	1431
2630	1432	1433	1434	1435	1436	1437	1438	1439
2640	1440	1441	1442	1443	1444	1445	1446	1447
2650	1448	1449	1450	1451	1452	1453	1454	1455
2660	1456	1457	1458	1459	1460	1461	1462	1463
2670	1464	1465	1466	1467	1468	1469	1470	1471
2700	1472	1473	1474	1475	1476	1477	1478	1479
2710	1480	1481	1482	1483	1484	1485	1486	1487
2720	1488	1489	1490	1491	1492	1493	1494	1495
2730	1496	1497	1498	1499	1500	1501	1502	1503
2740	1504	1505	1506	1507	1508	1509	1510	1511
2750	1512	1513	1514	1515	1516	1517	1518	1519
2760	1520	1521	1522	1523	1524	1525	1526	1527
2770	1528	1529	1530	1531	1532	1533	1534	1535

2000 to 2777 (Octal)	1024 to 1535 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
3000	1536	1537	1538	1539	1540	1541	1542	1543
3010	1544	1545	1546	1547	1548	1549	1550	1551
3020	1552	1553	1554	1555	1556	1557	1558	1559
3030	1560	1561	1562	1563	1564	1565	1566	1567
3040	1568	1569	1570	1571	1572	1573	1574	1575
3050	1576	1577	1578	1579	1580	1581	1582	1583
3060	1584	1585	1586	1587	1588	1589	1590	1591
3070	1592	1593	1594	1595	1596	1597	1598	1599
3100	1600	1601	1602	1603	1604	1605	1606	1607
3110	1608	1609	1610	1611	1612	1613	1614	1615
3120	1616	1617	1618	1619	1620	1621	1622	1623
3130	1624	1625	1626	1627	1628	1629	1630	1631
3140	1632	1633	1634	1635	1636	1637	1638	1639
3150	1640	1641	1642	1643	1644	1645	1646	1647
3160	1648	1649	1650	1651	1652	1653	1654	1655
3170	1656	1657	1658	1659	1660	1661	1662	1663
3200	1664	1665	1666	1667	1668	1669	1670	1671
3210	1672	1673	1674	1675	1676	1677	1678	1679
3220	1680	1681	1682	1683	1684	1685	1686	1687
3230	1688	1689	1690	1691	1692	1693	1694	1695
3240	1696	1697	1698	1699	1700	1701	1702	1703
3250	1704	1705	1706	1707	1708	1709	1710	1711
3260	1712	1713	1714	1715	1716	1717	1718	1719
3270	1720	1721	1722	1723	1724	1725	1726	1727
3300	1728	1729	1730	1731	1732	1733	1734	1735
3310	1736	1737	1738	1739	1740	1741	1742	1743
3320	1744	1745	1746	1747	1748	1749	1750	1751
3330	1752	1753	1754	1755	1756	1757	1758	1759
3340	1760	1761	1762	1763	1764	1765	1766	1767
3350	1768	1769	1770	1771	1772	1773	1774	1775
3360	1776	1777	1778	1779	1780	1781	1782	1783
3370	1784	1785	1786	1787	1788	1789	1790	1791

	0	1	2	3	4	5	6	7
3400	1792	1793	1794	1795	1796	1797	1798	1799
3410	1800	1801	1802	1803	1804	1805	1806	1807
3420	1808	1809	1810	1811	1812	1813	1814	1815
3430	1816	1817	1818	1819	1820	1821	1822	1823
3440	1824	1825	1826	1827	1828	1829	1830	1831
3450	1832	1833	1834	1835	1836	1837	1838	1839
3460	1840	1841	1842	1843	1844	1845	1846	1847
3470	1848	1849	1850	1851	1852	1853	1854	1855
3500	1856	1857	1858	1859	1860	1861	1862	1863
3510	1864	1865	1866	1867	1868	1869	1870	1871
3520	1872	1873	1874	1875	1876	1877	1878	1879
3530	1880	1881	1882	1883	1884	1885	1886	1887
3540	1888	1889	1890	1891	1892	1893	1894	1895
3550	1896	1897	1898	1899	1900	1901	1902	1903
3560	1904	1905	1906	1907	1908	1909	1910	1911
3570	1912	1913	1914	1915	1916	1917	1918	1919
3600	1920	1921	1922	1923	1924	1925	1926	1927
3610	1928	1929	1930	1931	1932	1933	1934	1935
3620	1936	1937	1938	1939	1940	1941	1942	1943
3630	1944	1945	1946	1947	1948	1949	1950	1951
3640	1952	1953	1954	1955	1956	1957	1958	1959
3650	1960	1961	1962	1963	1964	1965	1966	1967
3660	1968	1969	1970	1971	1972	1973	1974	1975
3670	1976	1977	1978	1979	1980	1981	1982	1983
3700	1984	1985	1986	1987	1988	1989	1990	1991
3710	1992	1993	1994	1995	1996	1997	1998	1999
3720	2000	2001	2002	2003	2004	2005	2006	2007
3730	2008	2009	2010	2011	2012	2013	2014	2015
3740	2016	2017	2018	2019	2020	2021	2022	2023
3750	2024	2025	2026	2027	2028	2029	2030	2031
3760	2032	2033	2034	2035	2036	2037	2038	2039
3770	2040	2041	2042	2043	2044	2045	2046	2047

3000 to 3777 (Octal)	1536 to 2047 (Decimal)

OCTAL-DECIMAL INTEGER CONVERSION TABLE

4000 to 4777 (Octal)	2048 to 2559 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
4000	2048	2049	2050	2051	2052	2053	2054	2055
4010	2056	2057	2058	2059	2060	2061	2062	2063
4020	2064	2065	2066	2067	2068	2069	2070	2071
4030	2072	2073	2074	2075	2076	2077	2078	2079
4040	2080	2081	2082	2083	2084	2085	2086	2087
4050	2088	2089	2090	2091	2092	2093	2094	2095
4060	2096	2097	2098	2099	2100	2101	2102	2103
4070	2104	2105	2106	2107	2108	2109	2110	2111
4100	2112	2113	2114	2115	2116	2117	2118	2119
4110	2120	2121	2122	2123	2124	2125	2126	2127
4120	2128	2129	2130	2131	2132	2133	2134	2135
4130	2136	2137	2138	2139	2140	2141	2142	2143
4140	2144	2145	2146	2147	2148	2149	2150	2151
4150	2152	2153	2154	2155	2156	2157	2158	2159
4160	2160	2161	2162	2163	2164	2165	2166	2167
4170	2168	2169	2170	2171	2172	2173	2174	2175
4200	2176	2177	2178	2179	2180	2181	2182	2183
4210	2184	2185	2186	2187	2188	2189	2190	2191
4220	2192	2193	2194	2195	2196	2197	2198	2199
4230	2200	2201	2202	2203	2204	2205	2206	2207
4240	2208	2209	2210	2211	2212	2213	2214	2215
4250	2216	2217	2218	2219	2220	2221	2222	2223
4260	2224	2225	2226	2227	2228	2229	2230	2231
4270	2232	2233	2234	2235	2236	2237	2238	2239
4300	2240	2241	2242	2243	2244	2245	2246	2247
4310	2248	2249	2250	2251	2252	2253	2254	2255
4320	2256	2257	2258	2259	2260	2261	2262	2263
4330	2264	2265	2266	2267	2268	2269	2270	2271
4340	2272	2273	2274	2275	2276	2277	2278	2279
4350	2280	2281	2282	2283	2284	2285	2286	2287
4360	2288	2289	2290	2291	2292	2293	2294	2295
4370	2296	2297	2298	2299	2300	2301	2302	2303

	0	1	2	3	4	5	6	7
4400	2304	2305	2306	2307	2308	2309	2310	2311
4410	2312	2313	2314	2315	2316	2317	2318	2319
4420	2320	2321	2322	2323	2324	2325	2326	2327
4430	2328	2329	2330	2331	2332	2333	2334	2335
4440	2336	2337	2338	2339	2340	2341	2342	2343
4450	2344	2345	2346	2347	2348	2349	2350	2351
4460	2352	2353	2354	2355	2356	2357	2358	2359
4470	2360	2361	2362	2363	2364	2365	2366	2367
4500	2368	2369	2370	2371	2372	2373	2374	2375
4510	2376	2377	2378	2379	2380	2381	2382	2383
4520	2384	2385	2386	2387	2388	2389	2390	2391
4530	2392	2393	2394	2395	2396	2397	2398	2399
4540	2400	2401	2402	2403	2404	2405	2406	2407
4550	2408	2409	2410	2411	2412	2413	2414	2415
4560	2416	2417	2418	2419	2420	2421	2422	2423
4570	2424	2425	2426	2427	2428	2429	2430	2431
4600	2432	2433	2434	2435	2436	2437	2438	2439
4610	2440	2441	2442	2443	2444	2445	2446	2447
4620	2448	2449	2450	2451	2452	2453	2454	2455
4630	2456	2457	2458	2459	2460	2461	2462	2463
4640	2464	2465	2466	2467	2468	2469	2470	2471
4650	2472	2473	2474	2475	2476	2477	2478	2479
4660	2480	2481	2482	2483	2484	2485	2486	2487
4670	2488	2489	2490	2491	2492	2493	2494	2495
4700	2496	2497	2498	2499	2500	2501	2502	2503
4710	2504	2505	2506	2507	2508	2509	2510	2511
4720	2512	2513	2514	2515	2516	2517	2518	2519
4730	2520	2521	2522	2523	2524	2525	2526	2527
4740	2528	2529	2530	2531	2532	2533	2534	2535
4750	2536	2537	2538	2539	2540	2541	2542	2543
4760	2544	2545	2546	2547	2548	2549	2550	2551
4770	2552	2553	2554	2555	2556	2557	2558	2559

5000 to 5777 (Octal)	2560 to 3071 (Decimal)

	0	1	2	3	4	5	6	7
5000	2560	2561	2562	2563	2564	2565	2566	2567
5010	2568	2569	2570	2571	2572	2573	2574	2575
5020	2576	2577	2578	2579	2580	2581	2582	2583
5030	2584	2585	2586	2587	2588	2589	2590	2591
5040	2592	2593	2594	2595	2596	2597	2598	2599
5050	2600	2601	2602	2603	2604	2605	2606	2607
5060	2608	2609	2610	2611	2612	2613	2614	2615
5070	2616	2617	2618	2619	2620	2621	2622	2623
5100	2624	2625	2626	2627	2628	2629	2630	2631
5110	2632	2633	2634	2635	2636	2637	2638	2639
5120	2640	2641	2642	2643	2644	2645	2646	2647
5130	2648	2649	2650	2651	2652	2653	2654	2655
5140	2656	2657	2658	2659	2660	2661	2662	2663
5150	2664	2665	2666	2667	2668	2669	2670	2671
5160	2672	2673	2674	2675	2676	2677	2678	2679
5170	2680	2681	2682	2683	2684	2685	2686	2687
5200	2688	2689	2690	2691	2692	2693	2694	2695
5210	2696	2697	2698	2699	2700	2701	2702	2703
5220	2704	2705	2706	2707	2708	2709	2710	2711
5230	2712	2713	2714	2715	2716	2717	2718	2719
5240	2720	2721	2722	2723	2724	2725	2726	2727
5250	2728	2729	2730	2731	2732	2733	2734	2735
5260	2736	2737	2738	2739	2740	2741	2742	2743
5270	2744	2745	2746	2747	2748	2749	2750	2751
5300	2752	2753	2754	2755	2756	2757	2758	2759
5310	2760	2761	2762	2763	2764	2765	2766	2767
5320	2768	2769	2770	2771	2772	2773	2774	2775
5330	2776	2777	2778	2779	2780	2781	2782	2783
5340	2784	2785	2786	2787	2788	2789	2790	2791
5350	2792	2793	2794	2795	2796	2797	2798	2799
5360	2800	2801	2802	2803	2804	2805	2806	2807
5370	2808	2809	2810	2811	2812	2813	2814	2815

	0	1	2	3	4	5	6	7
5400	2816	2817	2818	2819	2820	2821	2822	2823
5410	2824	2825	2826	2827	2828	2829	2830	2831
5420	2832	2833	2834	2835	2836	2837	2838	2839
5430	2840	2841	2842	2843	2844	2845	2846	2847
5440	2848	2849	2850	2851	2852	2853	2854	2855
5450	2856	2857	2858	2859	2860	2861	2862	2863
5460	2864	2865	2866	2867	2868	2869	2870	2871
5470	2872	2873	2874	2875	2876	2877	2878	2879
5500	2880	2881	2882	2883	2884	2885	2886	2887
5510	2888	2889	2890	2891	2892	2893	2894	2895
5520	2896	2897	2898	2899	2900	2901	2902	2903
5530	2904	2905	2906	2907	2908	2909	2910	2911
5540	2912	2913	2914	2915	2916	2917	2918	2919
5550	2920	2921	2922	2923	2924	2925	2926	2927
5560	2928	2929	2930	2931	2932	2933	2934	2935
5570	2936	2937	2938	2939	2940	2941	2942	2943
5600	2944	2945	2946	2947	2948	2949	2950	2951
5610	2952	2953	2954	2955	2956	2957	2958	2959
5620	2960	2961	2962	2963	2964	2965	2966	2967
5630	2968	2969	2970	2971	2972	2973	2974	2975
5640	2976	2977	2978	2979	2980	2981	2982	2983
5650	2984	2985	2986	2987	2988	2989	2990	2991
5660	2992	2993	2994	2995	2996	2997	2998	2999
5670	3000	3001	3002	3003	3004	3005	3006	3007
5700	3008	3009	3010	3011	3012	3013	3014	3015
5710	3016	3017	3018	3019	3020	3021	3022	3023
5720	3024	3025	3026	3027	3028	3029	3030	3031
5730	3032	3033	3034	3035	3036	3037	3038	3039
5740	3040	3041	3042	3043	3044	3045	3046	3047
5750	3048	3049	3050	3051	3052	3053	3054	3055
5760	3056	3057	3058	3059	3060	3061	3062	3063
5770	3064	3065	3066	3067	3068	3069	3070	3071

OCTAL-DECIMAL INTEGER CONVERSION TABLE

	0	1	2	3	4	5	6	7
6000	3072	3073	3074	3075	3076	3077	3078	3079
6010	3080	3081	3082	3083	3084	3085	3086	3087
6020	3088	3089	3090	3091	3092	3093	3094	3095
6030	3096	3097	3098	3099	3100	3101	3102	3103
6040	3104	3105	3106	3107	3108	3109	3110	3111
6050	3112	3113	3114	3115	3116	3117	3118	3119
6060	3120	3121	3122	3123	3124	3125	3126	3127
6070	3128	3129	3130	3131	3132	3133	3134	3135
6100	3136	3137	3138	3139	3140	3141	3142	3143
6110	3144	3145	3146	3147	3148	3149	3150	3151
6120	3152	3153	3154	3155	3156	3157	3158	3159
6130	3160	3161	3162	3163	3164	3165	3166	3167
6140	3168	3169	3170	3171	3172	3173	3174	3175
6150	3176	3177	3178	3179	3180	3181	3182	3183
6160	3184	3185	3186	3187	3188	3189	3190	3191
6170	3192	3193	3194	3195	3196	3197	3198	3199
6200	3200	3201	3202	3203	3204	3205	3206	3207
6210	3208	3209	3210	3211	3212	3213	3214	3215
6220	3216	3217	3218	3219	3220	3221	3222	3223
6230	3224	3225	3226	3227	3228	3229	3230	3231
6240	3232	3233	3234	3235	3236	3237	3238	3239
6250	3240	3241	3242	3243	3244	3245	3246	3247
6260	3248	3249	3250	3251	3252	3253	3254	3255
6270	3256	3257	3258	3259	3260	3261	3262	3263
6300	3264	3265	3266	3267	3268	3269	3270	3271
6310	3272	3273	3274	3275	3276	3277	3278	3279
6320	3280	3281	3282	3283	3284	3285	3286	3287
6330	3288	3289	3290	3291	3292	3293	3294	3295
6340	3296	3297	3298	3299	3300	3301	3302	3303
6350	3304	3305	3306	3307	3308	3309	3310	3311
6360	3312	3313	3314	3315	3316	3317	3318	3319
6370	3320	3321	3322	3323	3324	3325	3326	3327

	0	1	2	3	4	5	6	7
6400	3328	3329	3330	3331	3332	3333	3334	3335
6410	3336	3337	3338	3339	3340	3341	3342	3343
6420	3344	3345	3346	3347	3348	3349	3350	3351
6430	3352	3353	3354	3355	3356	3357	3358	3359
6440	3360	3361	3362	3363	3364	3365	3366	3367
6450	3368	3369	3370	3371	3372	3373	3374	3375
6460	3376	3377	3378	3379	3380	3381	3382	3383
6470	3384	3385	3386	3387	3388	3389	3390	3391
6500	3392	3393	3394	3395	3396	3397	3398	3399
6510	3400	3401	3402	3403	3404	3405	3406	3407
6520	3408	3409	3410	3411	3412	3413	3414	3415
6530	3416	3417	3418	3419	3420	3421	3422	3423
6540	3424	3425	3426	3427	3428	3429	3430	3431
6550	3432	3433	3434	3435	3436	3437	3438	3439
6560	3440	3441	3442	3443	3444	3445	3446	3447
6570	3448	3449	3450	3451	3452	3453	3454	3455
6600	3456	3457	3458	3459	3460	3461	3462	3463
6610	3464	3465	3466	3467	3468	3469	3470	3471
6620	3472	3473	3474	3475	3476	3477	3478	3479
6630	3480	3481	3482	3483	3484	3485	3486	3487
6640	3488	3489	3490	3491	3492	3493	3494	3495
6650	3496	3497	3498	3499	3500	3501	3502	3503
6660	3504	3505	3506	3507	3508	3509	3510	3511
6670	3512	3513	3514	3515	3516	3517	3518	3519
6700	3520	3521	3522	3523	3524	3525	3526	3527
6710	3528	3529	3530	3531	3532	3533	3534	3535
6720	3536	3537	3538	3539	3540	3541	3542	3543
6730	3544	3545	3546	3547	3548	3549	3550	3551
6740	3552	3553	3554	3555	3556	3557	3558	3559
6750	3560	3561	3562	3563	3564	3565	3566	3567
6760	3568	3569	3570	3571	3572	3573	3574	3575
6770	3576	3577	3578	3579	3580	3581	3582	3583

6000	3072
to	to
6777	3583
(Octal)	(Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
7000	3584	3585	3586	3587	3588	3589	3590	3591
7010	3592	3593	3594	3595	3596	3597	3598	3599
7020	3600	3601	3602	3603	3604	3605	3606	3607
7030	3608	3609	3610	3611	3612	3613	3614	3615
7040	3616	3617	3618	3619	3620	3621	3622	3623
7050	3624	3625	3626	3627	3628	3629	3630	3631
7060	3632	3633	3634	3635	3636	3637	3638	3639
7070	3640	3641	3642	3643	3644	3645	3646	3647
7100	3648	3649	3650	3651	3652	3653	3654	3655
7110	3656	3657	3658	3659	3660	3661	3662	3663
7120	3664	3665	3666	3667	3668	3669	3670	3671
7130	3672	3673	3674	3675	3676	3677	3678	3679
7140	3680	3681	3682	3683	3684	3685	3686	3687
7150	3688	3689	3690	3691	3692	3693	3694	3695
7160	3696	3697	3698	3699	3700	3701	3702	3703
7170	3704	3705	3706	3707	3708	3709	3710	3711
7200	3712	3713	3714	3715	3716	3717	3718	3719
7210	3720	3721	3722	3723	3724	3725	3726	3727
7220	3728	3729	3730	3731	3732	3733	3734	3735
7230	3736	3737	3738	3739	3740	3741	3742	3743
7240	3744	3745	3746	3747	3748	3749	3750	3751
7250	3752	3753	3754	3755	3756	3757	3758	3759
7260	3760	3761	3762	3763	3764	3765	3766	3767
7270	3768	3769	3770	3771	3772	3773	3774	3775
7300	3776	3777	3778	3779	3780	3781	3782	3783
7310	3784	3785	3786	3787	3788	3789	3790	3791
7320	3792	3793	3794	3795	3796	3797	3798	3799
7330	3800	3801	3802	3803	3804	3805	3806	3807
7340	3808	3809	3810	3811	3812	3813	3814	3815
7350	3816	3817	3818	3819	3820	3821	3822	3823
7360	3824	3825	3826	3827	3828	3829	3830	3831
7370	3832	3833	3834	3835	3836	3837	3838	3839

	0	1	2	3	4	5	6	7
7400	3840	3841	3842	3843	3844	3845	3846	3847
7410	3848	3849	3850	3851	3852	3853	3854	3855
7420	3856	3857	3858	3859	3860	3861	3862	3863
7430	3864	3865	3866	3867	3868	3869	3870	3871
7440	3872	3873	3874	3875	3876	3877	3878	3879
7450	3880	3881	3882	3883	3884	3885	3886	3887
7460	3888	3889	3890	3891	3892	3893	3894	3895
7470	3896	3897	3898	3899	3900	3901	3902	3903
7500	3904	3905	3906	3907	3908	3909	3910	3911
7510	3912	3913	3914	3915	3916	3917	3918	3919
7520	3920	3921	3922	3923	3924	3925	3926	3927
7530	3928	3929	3930	3931	3932	3933	3934	3935
7540	3936	3937	3938	3939	3940	3941	3942	3943
7550	3944	3945	3946	3947	3948	3949	3950	3951
7560	3952	3953	3954	3955	3956	3957	3958	3959
7570	3960	3961	3962	3963	3964	3965	3966	3967
7600	3968	3969	3970	3971	3972	3973	3974	3975
7610	3976	3977	3978	3979	3980	3981	3982	3983
7620	3984	3985	3986	3987	3988	3989	3990	3991
7630	3992	3993	3994	3995	3996	3997	3998	3999
7640	4000	4001	4002	4003	4004	4005	4006	4007
7650	4008	4009	4010	4011	4012	4013	4014	4015
7660	4016	4017	4018	4019	4020	4021	4022	4023
7670	4024	4025	4026	4027	4028	4029	4030	4031
7700	4032	4033	4034	4035	4036	4037	4038	4039
7710	4040	4041	4042	4043	4044	4045	4046	4047
7720	4048	4049	4050	4051	4052	4053	4054	4055
7730	4056	4057	4058	4059	4060	4061	4062	4063
7740	4064	4065	4066	4067	4068	4069	4070	4071
7750	4072	4073	4074	4075	4076	4077	4078	4079
7760	4080	4081	4082	4083	4084	4085	4086	4087
7770	4088	4089	4090	4091	4092	4093	4094	4095

7000	3584
to	to
7777	4095
(Octal)	(Decimal)

APPENDIX E
OCTAL-DECIMAL FRACTION CONVERSION TABLE

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	.100	.125000	.200	.250000	.300	.375000
.001	.001953	.101	.126953	.201	.251953	.301	.376953
.002	.003906	.102	.128906	.202	.253906	.302	.378906
.003	.005859	.103	.130859	.203	.255859	.303	.380859
.004	.007812	.104	.132812	.204	.257812	.304	.382812
.005	.009765	.105	.134765	.205	.259765	.305	.384765
.006	.011718	.106	.136718	.206	.261718	.306	.386718
.007	.013671	.107	.138671	.207	.263671	.307	.388671
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	.017578	.111	.142578	.211	.267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	.312	.394531
.013	.021484	.113	.146484	.213	.271484	.313	.396484
.014	.023437	.114	.148437	.214	.273437	.314	.398437
.015	.025390	.115	.150390	.215	.275390	.315	.400390
.016	.027343	.116	.152343	.216	.277343	.316	.402343
.017	.029296	.117	.154296	.217	.279296	.317	.404296
.020	.031250	.120	.156250	.220	.281250	.320	.406250
.021	.033203	.121	.158203	.221	.283203	.321	.408203
.022	.035156	.122	.160156	.222	.285156	.322	.410156
.023	.037109	.123	.162109	.223	.287109	.323	.412109
.024	.039062	.124	.164062	.224	.289062	.324	.414062
.025	.041015	.125	.166015	.225	.291015	.325	.416015
.026	.042968	.126	.167968	.226	.292968	.326	.417968
.027	.044921	.127	.169921	.227	.294921	.327	.419921
.030	.046875	.130	.171875	.230	.296875	.330	.421875
.031	.048828	.131	.173828	.231	.298828	.331	.423828
.032	.050781	.132	.175781	.232	.300781	.332	.425781
.033	.052734	.133	.177734	.233	.302734	.333	.427734
.034	.054687	.134	.179687	.234	.304687	.334	.429687
.035	.056640	.135	.181640	.235	.306640	.335	.431640
.036	.058593	.136	.183593	.236	.308593	.336	.433593
.037	.060546	.137	.185546	.237	.310546	.337	.435546
.040	.062500	.140	.187500	.240	.312500	.340	.437500
.041	.064453	.141	.189453	.241	.314453	.341	.439453
.042	.066406	.142	.191406	.242	.316406	.342	.441406
.043	.068359	.143	.193359	.243	.318359	.343	.443359
.044	.070312	.144	.195312	.244	.320312	.344	.445312
.045	.072265	.145	.197265	.245	.322265	.345	.447265
.046	.074218	.146	.199218	.246	.324218	.346	.449218
.047	.076171	.147	.201171	.247	.326171	.347	.451171
.050	.078125	.150	.203125	.250	.328125	.350	.453125
.051	.080078	.151	.205078	.251	.330078	.351	.455078
.052	.082031	.152	.207031	.252	.332031	.352	.457031
.053	.083984	.153	.208984	.253	.333984	.353	.458984
.054	.085937	.154	.210937	.254	.335937	.354	.460937
.055	.087890	.155	.212890	.255	.337890	.355	.462890
.056	.089843	.156	.214843	.256	.339843	.356	.464843
.057	.091796	.157	.216796	.257	.341796	.357	.466796
.060	.093750	.160	.218750	.260	.343750	.360	.468750
.061	.095703	.161	.220703	.261	.345703	.361	.470703
.062	.097656	.162	.222656	.262	.347656	.362	.472656
.063	.099609	.163	.224609	.263	.349609	.363	.474609
.064	.101562	.164	.226562	.264	.351562	.364	.476562
.065	.103515	.165	.228515	.265	.353515	.365	.478515
.066	.105468	.166	.230468	.266	.355468	.366	.480468
.067	.107421	.167	.232421	.267	.357421	.367	.482421
.070	.109375	.170	.234375	.270	.359375	.370	.484375
.071	.111328	.171	.236328	.271	.361328	.371	.486328
.072	.113281	.172	.238281	.272	.363281	.372	.488281
.073	.115234	.173	.240234	.273	.365234	.373	.490234
.074	.117187	.174	.242187	.274	.367187	.374	.492187
.075	.119140	.175	.244140	.275	.369140	.375	.494140
.076	.121093	.176	.246093	.276	.371093	.376	.496093
.077	.123046	.177	.248046	.277	.373046	.377	.498046

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000000	.000000	.000100	.000244	.000200	.000488	.000300	.000732
.000001	.000003	.000101	.000247	.000201	.000492	.000301	.000736
.000002	.000007	.000102	.000251	.000202	.000495	.000302	.000740
.000003	.000011	.000103	.000255	.000203	.000499	.000303	.000743
.000004	.000015	.000104	.000259	.000204	.000503	.000304	.000747
.000005	.000019	.000105	.000263	.000205	.000507	.000305	.000751
.000006	.000022	.000106	.000267	.000206	.000511	.000306	.000755
.000007	.000026	.000107	.000270	.000207	.000514	.000307	.000759
.000010	.000030	.000110	.000274	.000210	.000518	.000310	.000762
.000011	.000034	.000111	.000278	.000211	.000522	.000311	.000766
.000012	.000038	.000112	.000282	.000212	.000526	.000312	.000770
.000013	.000041	.000113	.000286	.000213	.000530	.000313	.000774
.000014	.000045	.000114	.000289	.000214	.000534	.000314	.000778
.000015	.000049	.000115	.000293	.000215	.000537	.000315	.000782
.000016	.000053	.000116	.000297	.000216	.000541	.000316	.000785
.000017	.000057	.000117	.000301	.000217	.000545	.000317	.000789
.000020	.000061	.000120	.000305	.000220	.000549	.000320	.000793
.000021	.000064	.000121	.000308	.000221	.000553	.000321	.000797
.000022	.000068	.000122	.000312	.000222	.000556	.000322	.000801
.000023	.000072	.000123	.000316	.000223	.000560	.000323	.000805
.000024	.000076	.000124	.000320	.000224	.000564	.000324	.000808
.000025	.000080	.000125	.000324	.000225	.000568	.000325	.000812
.000026	.000083	.000126	.000328	.000226	.000572	.000326	.000816
.000027	.000087	.000127	.000331	.000227	.000576	.000327	.000820
.000030	.000091	.000130	.000335	.000230	.000579	.000330	.000823
.000031	.000095	.000131	.000339	.000231	.000583	.000331	.000827
.000032	.000099	.000132	.000343	.000232	.000587	.000332	.000831
.000033	.000102	.000133	.000347	.000233	.000591	.000333	.000835
.000034	.000106	.000134	.000350	.000234	.000595	.000334	.000839
.000035	.000110	.000135	.000354	.000235	.000598	.000335	.000843
.000036	.000114	.000136	.000358	.000236	.000602	.000336	.000846
.000037	.000118	.000137	.000362	.000237	.000606	.000337	.000850
.000040	.000122	.000140	.000366	.000240	.000610	.000340	.000854
.000041	.000125	.000141	.000370	.000241	.000614	.000341	.000858
.000042	.000129	.000142	.000373	.000242	.000617	.000342	.000862
.000043	.000133	.000143	.000377	.000243	.000621	.000343	.000865
.000044	.000137	.000144	.000381	.000244	.000625	.000344	.000869
.000045	.000141	.000145	.000385	.000245	.000629	.000345	.000873
.000046	.000144	.000146	.000389	.000246	.000633	.000346	.000877
.000047	.000148	.000147	.000392	.000247	.000637	.000347	.000881
.000050	.000152	.000150	.000396	.000250	.000640	.000350	.000885
.000051	.000156	.000151	.000400	.000251	.000644	.000351	.000888
.000052	.000160	.000152	.000404	.000252	.000648	.000352	.000892
.000053	.000164	.000153	.000408	.000253	.000652	.000353	.000896
.000054	.000167	.000154	.000411	.000254	.000656	.000354	.000900
.000055	.000171	.000155	.000415	.000255	.000659	.000355	.000904
.000056	.000175	.000156	.000419	.000256	.000663	.000356	.000907
.000057	.000179	.000157	.000423	.000257	.000667	.000357	.000911
.000060	.000183	.000160	.000427	.000260	.000671	.000360	.000915
.000061	.000186	.000161	.000431	.000261	.000675	.000361	.000919
.000062	.000190	.000162	.000434	.000262	.000679	.000362	.000923
.000063	.000194	.000163	.000438	.000263	.000682	.000363	.000926
.000064	.000198	.000164	.000442	.000264	.000686	.000364	.000930
.000065	.000202	.000165	.000446	.000265	.000690	.000365	.000934
.000066	.000205	.000166	.000450	.000266	.000694	.000366	.000938
.000067	.000209	.000167	.000453	.000267	.000698	.000367	.000942
.000070	.000213	.000170	.000457	.000270	.000701	.000370	.000946
.000071	.000217	.000171	.000461	.000271	.000705	.000371	.000949
.000072	.000221	.000172	.000465	.000272	.000709	.000372	.000953
.000073	.000225	.000173	.000469	.000273	.000713	.000373	.000957
.000074	.000228	.000174	.000473	.000274	.000717	.000374	.000961
.000075	.000232	.000175	.000476	.000275	.000720	.000375	.000965
.000076	.000236	.000176	.000480	.000276	.000724	.000376	.000968
.000077	.000240	.000177	.000484	.000277	.000728	.000377	.000972

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000400	.000976	.000500	.001220	.000600	.001464	.000700	.001708
.000401	.000980	.000501	.001224	.000601	.001468	.000701	.001712
.000402	.000984	.000502	.001228	.000602	.001472	.000702	.001716
.000403	.000988	.000503	.001232	.000603	.001476	.000703	.001720
.000404	.000991	.000504	.001235	.000604	.001480	.000704	.001724
.000405	.000995	.000505	.001239	.000605	.001483	.000705	.001728
.000406	.000999	.000506	.001243	.000606	.001487	.000706	.001731
.000407	.001003	.000507	.001247	.000607	.001491	.000707	.001735
.000410	.001007	.000510	.001251	.000610	.001495	.000710	.001739
.000411	.001010	.000511	.001255	.000611	.001499	.000711	.001743
.000412	.001014	.000512	.001258	.000612	.001502	.000712	.001747
.000413	.001018	.000513	.001262	.000613	.001506	.000713	.001750
.000414	.001022	.000514	.001266	.000614	.001510	.000714	.001754
.000415	.001026	.000515	.001270	.000615	.001514	.000715	.001758
.000416	.001029	.000516	.001274	.000616	.001518	.000716	.001762
.000417	.001033	.000517	.001277	.000617	.001522	.000717	.001766
.000420	.001037	.000520	.001281	.000620	.001525	.000720	.001770
.000421	.001041	.000521	.001285	.000621	.001529	.000721	.001773
.000422	.001045	.000522	.001289	.000622	.001533	.000722	.001777
.000423	.001049	.000523	.001293	.000623	.001537	.000723	.001781
.000424	.001052	.000524	.001296	.000624	.001541	.000724	.001785
.000425	.001056	.000525	.001300	.000625	.001544	.000725	.001789
.000426	.001060	.000526	.001304	.000626	.001548	.000726	.001792
.000427	.001064	.000527	.001308	.000627	.001552	.000727	.001796
.000430	.001068	.000530	.001312	.000630	.001556	.000730	.001800
.000431	.001071	.000531	.001316	.000631	.001560	.000731	.001804
.000432	.001075	.000532	.001319	.000632	.001564	.000732	.001808
.000433	.001079	.000533	.001323	.000633	.001567	.000733	.001811
.000434	.001083	.000534	.001327	.000634	.001571	.000734	.001815
.000435	.001087	.000535	.001331	.000635	.001575	.000735	.001819
.000436	.001091	.000536	.001335	.000636	.001579	.000736	.001823
.000437	.001094	.000537	.001338	.000637	.001583	.000737	.001827
.000440	.001098	.000540	.001342	.000640	.001586	.000740	.001831
.000441	.001102	.000541	.001346	.000641	.001590	.000741	.001834
.000442	.001106	.000542	.001350	.000642	.001594	.000742	.001838
.000443	.001110	.000543	.001354	.000643	.001598	.000743	.001842
.000444	.001113	.000544	.001358	.000644	.001602	.000744	.001846
.000445	.001117	.000545	.001361	.000645	.001605	.000745	.001850
.000446	.001121	.000546	.001365	.000646	.001609	.000746	.001853
.000447	.001125	.000547	.001369	.000647	.001613	.000747	.001857
.000450	.001129	.000550	.001373	.000650	.001617	.000750	.001861
.000451	.001132	.000551	.001377	.000651	.001621	.000751	.001865
.000452	.001136	.000552	.001380	.000652	.001625	.000752	.001869
.000453	.001140	.000553	.001384	.000653	.001628	.000753	.001873
.000454	.001144	.000554	.001388	.000654	.001632	.000754	.001876
.000455	.001148	.000555	.001392	.000655	.001636	.000755	.001880
.000456	.001152	.000556	.001396	.000656	.001640	.000756	.001884
.000457	.001155	.000557	.001399	.000657	.001644	.000757	.001888
.000460	.001159	.000560	.001403	.000660	.001647	.000760	.001892
.000461	.001163	.000561	.001407	.000661	.001651	.000761	.001895
.000462	.001167	.000562	.001411	.000662	.001655	.000762	.001899
.000463	.001171	.000563	.001415	.000663	.001659	.000763	.001903
.000464	.001174	.000564	.001419	.000664	.001663	.000764	.001907
.000465	.001178	.000565	.001422	.000665	.001667	.000765	.001911
.000466	.001182	.000566	.001426	.000666	.001670	.000766	.001914
.000467	.001186	.000567	.001430	.000667	.001674	.000767	.001918
.000470	.001190	.000570	.001434	.000670	.001678	.000770	.001922
.000471	.001194	.000571	.001438	.000671	.001682	.000771	.001926
.000472	.001197	.000572	.001441	.000672	.001686	.000772	.001930
.000473	.001201	.000573	.001445	.000673	.001689	.000773	.001934
.000474	.001205	.000574	.001449	.000674	.001693	.000774	.001937
.000475	.001209	.000575	.001453	.000675	.001697	.000775	.001941
.000476	.001213	.000576	.001457	.000676	.001701	.000776	.001945
.000477	.001216	.000577	.001461	.000677	.001705	.000777	.001949

APPENDIX F
DATA 260 INSTRUCTIONS (ALPHABETICAL ORDER)

APPENDIX F
DATA 620 INSTRUCTIONS (ALPHABETICAL ORDER)

Mnemonic	Octal	Description	Wds/Inst	Time Cycles	Indirect Address	Page
ADD	120000	Add to A Register	1	2	yes	3-10
ADDI	006120	Add to A Register Immediate	2	2	no	3-54
ANA	150000	AND to A Register	1	2	yes	3-13
ANAI	006150	AND to A Register Immediate	2	2	no	3-58
AØFA	005511	Add OF to A Register	1	1	no	3-27
AØFB	005522	Add OF to B Register	1	1	no	3-28
AØFX	005544	Add OF to X Register	1	1	no	3-28
ASLA	004200+n	Arithmetic Shift Left A n places	1	1+.25n	no	3-19
ASLB	004000+n	Arithmetic Shift Left B n places	1	1+.25n	no	3-20
ASRA	004300+n	Arithmetic Shift Right A n places	1	1+.25n	no	3-19
ASRB	004100+n	Arithmetic Shift Right B n places	1	1+.25n	no	3-19
CIA	102500	Clear and Input to A Register	1	2	no	4-7
CIB	102600	Clear and Input to B Register	1	2	no	4-9
CPA	005211	Complement A Register	1	1	no	3-24
CPB	005222	Complement B Register	1	1	no	3-24
CPX	005244	Complement X Register	1	1	no	3-24
DAR	005311	Decrement A Register	1	1	no	3-23
DBR	005322	Decrement B Register	1	1	no	3-23
DIV*	170000	Divide AB Register 16-bit	1	10-14	yes	3-11
		18-bit	1	11-16		
DIVI*	006170	Divide AB Register Immediate 16-bit	2	10-14	no	3-55
		18-bit		11-16		
DXR	005344	Decrement X Register	1	1	no	3-23
ERA	130000	Exclusive OR to A Register	1	2	yes	3-12
ERAI	006130	Exclusive OR to A Register Immediate	2	2	no	3-56
EXC	100000	External Control Function	1	1	no	4-5
HLT	000000	Halt	1	1	no	3-14
IAR	005111	Increment A Register	1	1	no	3-22
IBR	005122	Increment B Register	1	1	no	3-22
IME	102000	Input to Memory	2	3	no	4-10
INA	102100	Input to A Register	1	2	no	4-9
INB	102100	Input to B Register	1	2	no	4-10
INR	040000	Increment and Replace	1	3	yes	3-7
INRI	006040	Increment and Replace Immediate	2	3	no	3-56
IXR	005144	Increment X Register	1	1	no	3-22
JAN	001004	Jump if A Register NEGATIVE	2	2	yes	3-33
JANM	002004	Jump and mark if A Register NEGATIVE	2	2-3	yes	3-37
JAP	001002	Jump if A Register POSITIVE	2	2	yes	3-31
JAPM	002002	Jump and Mark if A Register POSITIVE	2	2-3	yes	3-37
JAZ	001010	Jump if A Register ZERO	2	2	yes	3-33
JAZM	002010	Jump and Mark if A Register	2	2-3	yes	3-38
JBZ	001020	Jump if B Registers ZERO	2	2	yes	3-33

Mnemonic	Octal	Description	Wds/Inst	Time Cycles	Indirect Address	Page
JBZM	002020	Jump and Mark if B Register ZERO	2	2-3	yes	3-38
JMP	001000	Jump UNCONDITIONALLY	2	2	yes	3-31
JMPM	002000	Jump and Mark if UNCONDITIONALLY	2	3	yes	3-35
JØF	001001	Jump if Overflow ON	2	2	yes	3-31
JØFM	002001	Jump and Mark if Overflow ON	2	3	yes	3-35
JS1M	002100	Jump and Mark if Sense Switch L I ON	2	2-3	yes	3-39
JS2M	002200	Jump and Mark if Sense Switch L 2 ON	2	2-3	yes	3-39
JS3M	002400	Jump and Mark if Sense Switch 3 ON	2	2-3	yes	3-39
JSS1	001100	Jump if Sense Switch I ON	2	2	yes	3-34
JSS2	001200	Jump if Sense Switch 2 ON	2	2	yes	3-34
JSS3	001400	Jump if Sense Switch 3 ON	2	2	yes	3-35
JXZ	001040	Jump X Register ZERO	2	2	yes	3-34
JXZM	002040	Jump and Mark X Register ZERO	2	203	yes	3-38
LASL	004400+n	Long Arithmetic Shift Left n places	1	1 + .50n	no	3-20
LASR	004500+n	Long Arithmetic Shift Right n places	1	1 + .50n	no	3-20
LDA	010000	Load A Register	1	2	yes	3-2
LDAE	006010	Load A Register Extended	2	3	yes	3-45
LDAI	006010	Load A Register Immediate	2	2	no	3-52
LDB	020000	Load B Register	1	2	yes	3-6
LDBE	006020	Load B Register Extended	2	3	yes	3-46
LDBI	006020	Load B Register Immediate	2	2	no	3-53
LDX	030000	Load X Register	1	2	yes	3-6
LDXE	006030	Load X Register Extended	2	3	yes	3-46
LDXI	006030	Load X Register Immediate	2	2	no	3-53
LLRL	00444+n	Long Logical Rotate Left n places	1	1 + .50n	no	3-18
LLSR	004540+n	Long Logical Rotate Left n places	1	1 + .50n	no	3-18
LRLA	004240+n	Logical Rotate Left A n places	1	1 + .25n	no	3-17
LRLB	004040+n	Logical Rotate Left B n places	1	1 + .25n	no	3-18
LSRA	004340+n	Logical Shift Right A n places	1	1 + .25n	no	3-17
LSRB	004140+n	Logical Shift Right B n places	1	1 + .25n	no	3-17
MUL*	160000	Multiply B Register 16-Bit	1	10	yes	3-11
		18-Bit		11		3-11
MULI*	006160	Multiply B Register Immediate 16-Bit	2	10	no	3-62
		18-Bit		14		3-55
NØP	00500	No Operation	1	1	no	3-14
ØAR	103100	Output from A Register	1	2	no	4-10
ØBR	103200	Output from B Register	1	2	no	4-12
ØME	103000	Output from Memory	2	3	no	4-12
ØRA	110000	Inclusive OR to A Register	1	2	yes	3-12
ØRAI	006110	Inclusive OR to A Register Immediate	2	2	no	3-57
RØF	007400	Reset Overflow	1	1	no	3-15
SCAE	007114	Selective Compare A Equal	2	2	yes	3-52
SEN	101000	Sense Input/Output Lines	2	2.25	no	4-7
SLA*	007100	Selective Load A Register	2	2	yes	3-47
SLAC*	007102	Selective Load A Complement	2	2	yes	3-50
SØF	007401	Set Overflow	1	1	no	3-15
SØFA	005711	Subtract OFLO from A Register	1	1	no	3-28
SØFB	005722	Subtract OFLO from B Register	1	1	no	3-28

Mnemonic	Octal	Description	Wds/Inst	Time Cycles	Indirect Address	Page
SØFX	005744	Subtract OFLO from X Register	1	1	no	3-29
SSA*	007111	Selective Store A Register	2	2	yes	3-50
SSAC*	007113	Selective Store A Complement	2	2	yes	3-51
STA	050000	Store A Register	1	2	yes	3-6
STAE	006050	Store A Register Extended	2	3	yes	3-46
STAI	006050	Store A Register Immediate	2	2	no	3-53
STB	060000	Store B Register	1	2	yes	3-7
STBI	006060	Store B Register Immediate	2	2	no	3-54
STX	070000	Store X Register	1	2	yes	3-7
STX1	006070	Store X Register Immediate	2	2	no	3-60
SUB	140000	Subtract from A Register	1	2	yes	3-10
SUBI	006140	Subtract from A Register Immediate	2	2	no	3-55
TAB	005012	Transfer A to B Register	1	1	no	3-25
TAX	005014	Transfer A to X Register	1	1	no	3-25
TBA	005021	Transfer B to A Register	1	1	no	3-25
TBX	005024	Transfer B to X Register	1	1	no	3-26
TXA	005041	Transfer X to A Register	1	1	no	3-26
TXB	005042	Transfer X to B Register	1	1	no	3-26
TZA	005001	Transfer Zero to A Register	1	1	no	3-27
TZB	005002	Transfer Zero to B Register	1	1	no	3-27
TZX	005004	Transfer Zero to X Register	1	1	no	3-27
XAN	003004	Execute A Register Negative	2	2	yes	3-41
XAP	003002	Execute A Register Positive	2	2	yes	3-41
XAZ	003010	Execute A Register Zero	2	2	yes	3-43
XBZ	003020	Execute B Register Zero	2	2	yes	3-43
XEC	003000	Execute UNCONDITIONALLY	2	2	yes	3-41
XØF	003001	Execute Overflow SET	2	2	yes	3-41
XS1	003100	Execute Sense Switch 1 Set	2	2	yes	3-44
XS2	003200	Execute Sense Switch 2 SET	2	2	yes	3-44
XS3	003400	Execute Sense Switch 3 SET	2	2	yes	3-44
XXZ	003040	Execute X Register Zero	2	2	yes	3-43

APPENDIX G
DATA 620 INSTRUCTIONS (BY TYPE)

TABLE G-1
SINGLE-WORD ADDRESSED INSTRUCTIONS

TABLE G-1(a)
LOAD/STORE INSTRUCTION GROUP

OP CODE OCTAL	MNEMONIC	INSTRUCTION	TIMING (CYCLES)
01	LDA	Load A Register	2
02	LDB	Load B Register	2
03	LDX	Load X Register	2
05	STA	Store A Register	2
06	STB	Store B Register	2
07	STX	Store X Register	2

TABLE G-1(b)
ARITHMETIC INSTRUCTION GROUP

OP CODE OCTAL	MNEMONIC	INSTRUCTION		TIMING (CYCLES)
04	INR	Increment and Replace		3
12	ADD	Add Memory to A		2
14	SUB	Subtract Memory from A		2
16	MUL(*)	Multiply	16-bit	10
			18-bit	11
17	DIV(*)	Divide	16-bit	10-14
			18-bit	11-15

* Optional Instructions

TABLE G-1(c)
LOGICAL INSTRUCTION GROUP

OP CODE		INSTRUCTION	TIMING (CYCLES)
OCTAL	MNEMONIC		
11	ØRA	Inclusive OR, Memory and A	2
13	ERA	Exclusive OR, Memory and A	2
15	ANA	AND Memory and A	2

TABLE G-1(d)
ADDRESSING MODES FOR SINGLE WORD ADDRESSED INSTRUCTIONS

m FIELD			ADDRESSING MODE	OPERATION
11	10	9		
0	X	X	Direct	Combine bits 9, 10 with a field (0-8) to form effective address (0000 - 2047).
1	0	0	Relative	Add a field (bits 0-8) to contents of P to form effective address (Mod 2^{15}).
1	0	1	Index (X Register)	Add a field (bits 0-8) to contents of X to form effective address (Mod 2^{15}).
1	1	0	Index (B Register)	Add a field (bits 0-8) to contents of B to form effective address (Mod 2^{15}).
1	1	1	Indirect	a field (bits 0-8) specifies location of an address word.

TABLE G-2

CONTROL INSTRUCTION GROUP CODES
(SINGLE-WORD, NON-ADDRESSABLE)

OP CODE		m	a		TIMING
OCTAL	MNEMONIC	FIELD	FIELD	INSTRUCTION	(CYCLES)
00	HLT	0	XXX	Halt	1
00	NØP	5	000	No Operation	1
00	RØF	7	400	Reset Overflow	1
00	SØF	7	401	Set Overflow	1

TABLE G-3
SHIFT INSTRUCTION GROUP

TABLE G-3(a)
INSTRUCTION FORMAT

OCTAL	OCTAL	a FIELD								
OP CODE	m FIELD	U_8	U_7	U_6	U_5	U_4	U_3	U_2	U_1	U_0
00	4	0 = A or B 1 = A & B	0 = B 1 = A	0=Left 1 = rt.	0 = Arith. 1 = logical rotate	SHIFT COUNT (0 - 31)				

TABLE G-3(b)
INSTRUCTION FORMAT

U	U	U	U	MNEMONIC	SHIFT INSTRUCTION	TIMING (CYCLES)
0	0	0	0	ASLB	Arithmetic Shift B Left	1 + .25n
0	0	0	1	LRLB	Logical Rotate B Left	"
0	0	1	0	ASRB	Arithmetic Shift B Right	"
0	0	1	1	LSRB	Logical Shift B Right	"
0	1	0	0	ASLA	Arithmetic Shift A Left	"
0	1	0	1	LRLA	Logical Rotate A Left	"
0	1	1	0	ASRA	Arithmetic Shift A Right	"
0	1	1	1	LSRA	Logical Shift A Right	"
1	0	0	0	LASL	Long Arithmetic Shift A, B Left	1 +.50n
1	0	0	1	LARL	Long Logical Rotate A, B Registers Left	1 +.50n
1	0	1	0	LASR	Long Arithmetic Shift A, B Right	1 +.50n
1	0	1	1	LLSR	Long Logical Shift, A, B Registers	1 +.50n
1	1	0	0		Invalid	
1	1	0	1		Invalid	
1	1	1	0		Invalid	
1	1	1	1		Invalid	

TABLE G-4
REGISTER CHANGE INSTRUCTION
GROUP

TABLE G-4(a)
INSTRUCTION FORMAT

CLASS CODE	m FIELD	a FIELD						TYPE OF TRANSFER
		SOURCE					DEST.	
OCTAL	OCTAL	U_8 U_7	U_6	U_5	U_4	U_3	U_2 U_1 U_0	
00	5	0 0 0 1 1 0 1 1		X	B	A	X B A	Transfer Unchanged Transfer Incremented Transfer Complemented Transfer Decremented

Note: Multiple source transfer results in Inclusive-OR; Multiple source complemented results in complement Inclusive-OR

TABLE G-4(b)
REGISTER CHANGE INSTRUCTION CODES

Class Code FIELD OCTAL	MNEMONIC	REGISTER CHANGE INSTRUCTION	TIMING
0 0 1	TZA	Transfer Zero to A Register	1
0 0 2	TZB	Transfer Zero to B Register	1
0 0 4	TZX	Transfer Zero to X Register	1
0 1 2	TAB	Transfer A Register to B Register	1
0 1 4	TAX	Transfer A Register to X Register	1
0 2 1	TBA	Transfer B Register to A Register	1
0 2 4	TBX	Transfer B Register to X Register	1
0 4 1	TXA	Transfer X Register to A Register	1
0 4 2	TXB	Transfer X Register to B Register	1
1 1 1	IAR	Increment A Register	1
1 2 2	IBR	Increment B Register	1
1 4 4	IXR	Increment X Register	1
3 1 1	DAR	Decrement A Register	1
3 2 2	DBR	Decrement B Register	1
3 4 4	DXR	Decrement X Register	1
5 1 1	AØFA	Add Overflow to A Register	1
5 2 2	AØFB	Add Overflow to B Register	1
5 4 4	AØFX	Add Overflow to X Register	1
7 1 1	SØFA	Subtract Overflow from A Register	1
7 2 2	SØFB	Subtract Overflow from B Register	1
7 4 4	SØFX	Subtract Overflow from X Register	1

TABLE G-5
JUMP INSTRUCTION GROUP

TABLE G-5(a)
INSTRUCTION FORMAT

OP CODE OCTAL	m FIELD OCTAL	a FIELD								
		U_8	U_7	U_6	U_5	U_4	U_3	U_2	U_1	U_0
0 0	1	SS3 ON	SS2 ON	SS1 ON	X=0	B=0	A=0	A 0	A 0	OF=1

NOTE: Jump condition is logical AND of all a Field bits

TABLE G-5(b)
JUMP INSTRUCTION CODES

a FIELD OCTAL	MNEMONIC	JUMP INSTRUCTION	TIMING (CYCLES)
0 0 0	JMP	Jump Unconditionally	2
0 0 1	JØF	Jump If Overflow Set	2
0 0 2	JAP	Jump If A Register Positive	2
0 0 4	JAN	Jump If A Register Negative	2
0 1 0	JAZ	Jump If A Register Zero	2
0 2 0	JBZ	Jump If B Register Zero	2
0 4 0	JXZ	Jump If X Register Zero	2
1 0 0	JSS1	Jump If Sense Switch 1 Set	2
2 0 0	JSS2	Jump If Sense Switch 2 Set	2
3 0 0	JSS3	Jump If Sense Switch 3 Set	2

TABLE G-6
JUMP AND MARK INSTRUCTION GROUP

TABLE G-6(a)
INSTRUCTION FORMAT

OP CODE OCTAL	m FIELD OCTAL	a FIELD								
		U_8	U_7	U_6	U_5	U_4	U_3	U_2	U_1	U_0
00	1	SS3	SS2	SS1	X=0	B=0	A=0	A 0	A 0	OF=1

NOTE: Jump and Mark condition is logical-AND of all a Field bits

TABLE G-6(b)
JUMP AND MARK INSTRUCTION CODES

a FIELD OCTAL	MNEMONIC	JUMP AND MARK INSTRUCTIONS	TIMING (CYCLES)
000	JMPM	Jump and Mark Unconditionally	2
001	JØFM	Jump and Mark if Overflow Set	2 (3 if Jump)
002	JANM	Jump and Mark if A Register Negative	2 (3 if Jump)
003	JAPM	Jump and Mark if A Register Positive	2 (3 if Jump)
010	JAZM	Jump and Mark if A Register Zero	2 (3 if Jump)
020	JBZM	Jump and Mark if B Register Zero	2 (3 if Jump)
040	JXZM	Jump and Mark if X Register Zero	2 (3 if Jump)
100	JS1M	Jump and Mark if Sense Switch 1 On	2 (3 if Jump)
200	JS2M	Jump and Mark if Sense Switch 2 On	2 (3 if Jump)
400	JS3M	Jump and Mark if Sense Switch 3 On	2 (3 if Jump)

TABLE G-7
EXECUTE INSTRUCTION GROUP

TABLE G-7(a)
INSTRUCTION FORMAT

OP CODE OCTAL	m FIELD OCTAL	a FIELD								
		U_8	U_7	U_6	U_5	U_4	U_3	U_2	U_1	U_0
0 0	3	SS3 ON	SS2 ON	SS1 ON	X=0	B=0	A=0	A 0	A 0	OF=1

NOTE: Execute Condition is logical-AND of all a Field bits. Executed instruction must be single work

TABLE G-7(a)
INSTRUCTION FORMAT

a FIELD OCTAL	MNEMONIC	EXECUTE INSTRUCTION	TIMING (CYCLES)
000	XEC	Execute Unconditionally	2
001	XØF	Execute if Overflow Set	2
002	XAP	Execute if A Register Positive	2
004	XAN	Execute if A Register Negative	2
010	XAZ	Execute if A Register Zero	2
020	XBZ	Execute if B Register Zero	2
040	XXZ	Execute if X Register Zero	2
100	XS1	Execute if Sense Switch 1	2
200	XS2	Execute if Sense Switch 2	2
400	XS3	Execute if Sense Switch 3	2

TABLE G-8
AUTO INDEX INSTRUCTION GROUP

TABLE G-8(a)
INSTRUCTION FORMAT

OP CODE OCTAL	MNEMONIC	m FIELD OCTAL	a FIELD U8	a FIELD U7 U6	a FIELD U5	a FIELD U4 U3 U2 U1 U0	INSTRUCTION	TIMING (CYCLES)
	IRJZ			0 0			Increment Replace & Jump if Zero	3 (4 if Jump)
00	IRJN	7	0	0 1	1	INDEX LOCATION ($0-37_8$)	Increment Replace & Jump if not Zero	3 (4 if Jump)
	DRJZ			1 0			Decrement Replace & Jump if Zero	3 (4 if Jump)
	DRJN			1 1			Decrement Replace & Jump if Not Zero	3 (4 if Jump)

TABLE G-8(b)
AUTO INDEX INSTRUCTION CODES

a FIELD	MNEMONIC	INSTRUCTION	TIMING (CYCLES)
0, 40 + L	IRJZ	Increment Replace and Jump if Zero	3 (4 if Jump)
1, 40 + L	IRJN	Increment Replace and Jump if Not Zero	3 (4 if Jump)
2, 40 + L	DRJZ	Decrement Replace and Jump if Zero	3 (4 if Jump)
3, 40 + L	DRJN	Decrement Replace and Jump if Not Zero	3 (4 if Jump)

TABLE G-9
BYTE INSTRUCTION GROUP (*)

OP CODE		m FIELD	a FIELD	INSTRUCTION	TIMING (CYCLES)
OCTAL	MNEMONIC	OCTAL	OCTAL		
00	SLA	7	000	Selective Load A Register	2
00	SSA	7	011	Selective Store A Register	2
00	SCAE	7	014	Selective Load A Register Complement	2
00	SSAC	7	025	Selective Store A Register Complement	2

(*) Optional

TABLE G-10
IMMEDIATE INSTRUCTION GROUP

OP CODE		m FIELD	a FIELD		TIMING
OCTAL	MNEMONIC	OCTAL	OCTAL	INSTRUCTION	(CYCLES)
00	LDAI	6	010	Load A Immediate	2
00	LDBI	6	020	Load B Immediate	2
00	LDXI	6	030	Load X Immediate	2
00	INRI	6	040	Increment and Replace Immediate	2
00	STAI	6	050	Store A Immediate	2
00	STBI	6	060	Store B Immediate	2
00	STXI	6	070	Store X Immediate	2
00	ØRAI	6	110	Inclusive OR Immediate	2
00	ADDI	6	120	Add Immediate	2
00	ERAI	6	130	Exclusive OR Immediate	2
00	SUBI	6	140	Subtract Immediate	2
00	MULI (*)	6	160	Multiply Immediate	10
00	DIVI (*)	6	170	Divide Immediate	10-14
00	ANAI	6	150	AND Immediate	2

(*) Optional

TABLE G-11
INPUT/OUTPUT INSTRUCTION GROUP

OP CODE		m FIELD	a FIELD	INSTRUCTION	TIMING
OCTAL	MNEMONIC	OCTAL	OCTAL		(CYCLES)
10	EXC	0	XZZ	External Control	1
10	SEN	1	XZZ	Program Sense	2
10	IME	2	0ZZ	Input to Memory	3
10	INA	2	1ZZ	Input to A	2
10	INB	2	2ZZ	Input to B	2
10	CIA	2	5ZZ	Clear and Input to A	2
10	CIB	2	6ZZ	Clear and Input to B	2
10	ØME	3	0ZZ	Output from Memory	2
10	ØAR	3	1ZZ	Output from A	2
10	ØBR	3	2ZZ	Output from B	2

X - Mode or logical unit number

Z - Device number

TABLE G-12
EXTENDED ADDRESS INSTRUCTION GROUP

OP CODE		m FIELD	a FIELD	INSTRUCTION	TIMING
OCTAL	MNEMONIC	OCTAL	OCTAL		(CYCLES)
00	LDAE	6	01X	Load A Register Extended	3
00	LDBE	6	02X	Load B Register Extended	3
00	LDXE	6	03X	Load X Register Extended	3
00	STAE	6	05X	Store A Register Extended	3

APPENDIX H
DATA 620 RESERVED INSTRUCTION CODES

Table H-1
INTERRUPT MODULE RESERVED INSTRUCTION CODES

The following instruction codes are for use with the first Interrupt Module. Device addresses 40_8 through 47_8 are reserved for Interrupt Modules.

MNEMONIC	OCTAL	FUNCTION
A. EXTERNAL CONTROL		
EXC 140*	100140	CLEAR ac Register
EXC 240	100240	ENABLE Interrupt Module
EXC 440	100440	INHIBIT Interrupt Module
EXC 540	100540	INITIALIZE Interrupt Module
B. TRANSFER		
ØME 40	103040	LOAD MASK from Memory
ØAR 40	103140	LOAD MASK from A Register
ØBR 40	103240	LOAD MASK from B Register
C. SENSE		
NONE		

*Ac option only.

Table H-2
BIC RESERVED INSTRUCTION CODES

The following instruction codes are for use with the first Buffer Interlace Controller. Device addresses 20_8 through 27_8 are reserved for BIC's.

MNEMONIC	OCTAL	FUNCTION
A. EXTERNAL CONTROL		
EXC 020	1000020	ACTIVATE ENABLE
EXC 021	1000021	INITIALIZE
B. TRANSFER		
ØAR 20	103120	LOAD INITIAL Register from A
ØBR 20	103220	LOAD INITIAL Register from B
ØME 20	103020	LOAD INITIAL Register from memory
ØAR 21	103121	LOAD FINAL Register from A
ØBR 21	103221	LOAD FINAL Register from B
ØME 21	103021	LOAD FINAL Register from memory
INA 20	102120	READ INITIAL Register into A
INB 20	102220	READ INITIAL Register into B
IME 20	102020	READ INITIAL Register into memory
CIA 20	102520	READ INITIAL Register into cleared A
CIB 20	102620	READ INITIAL Register into cleared B
C. SENSE		
SEN 20	101020	Sense BIC NOT BUSY
SEN 21	101021	Sense ABNORMAL DEVICE STOP

Table H-3
TELETYPE RESERVED INSTRUCTION CODES

The following instruction codes are for use with the first Teletype. Device addresses 00_8 through 07_8 are reserved for Teletypes.

MNEMONIC	OCTAL	FUNCTION
A. EXTERNAL CONTROL		
EXC 000	100000	Select HIGH SPEED INPUT
EXC 100	100100	Select LOW SPEED INPUT
EXC 200	100200	Select KEYBOARD INPUT
EXC 300	100300	Select LOW SPEED OUTPUT
EXC 400	100400	Select TTY OFF
B. TRANSFER		
ØAR 00	103100	Transfer A Register to TTY Buffer
ØBR 00	103200	Transfer B Register to TTY Buffer
ØME 00	103000	Transfer Memory to TTY Buffer
INA 00	102100	Transfer TTY Buffer to A Register
INB 00	102200	Transfer TTY Buffer to B Register
IME 00	102000	Transfer TTY Buffer to Memory
CIA 00	102500	Transfer TTY Buffer to cleared A Register
CIB 00	102600	Transfer TTY Buffer to cleared B Register
C. SENSE		
SEN 000	101000	Sense TTY NOT BUSY
SEN 100	101100	Sense TTY BUFFER READY
SEN 300	101300	Sense TTY READER READY

Table H-4
90 CPM CARD READER RESERVED INSTRUCTION CODES

The following instruction codes are for use with the 90 CPM Card Reader. For additional Card Readers, device addresses will be assigned at the time of system definition.

MNEMONIC	OCTAL	FUNCTION
A. EXTERNAL CONTROL		
EXC 230	100230	Read One Card
EXC 630	100630	Step Read One Character
B. TRANSFER		
INA 30	102130	Transfer to A Register
INB 30	102230	Transfer to B Register
IME 30	102030	Transfer to Memory
CIA 30	102530	Transfer to A Register Cleared
CIB 30	102630	Transfer to B Register Cleared
C. SENSE		
SEN 130	101130	Sense Character Ready
SEN 230	101230	Sense Reader Not Busy
SEN 630	101630	Sense Reader Ready

Table H-5
GATED INPUT CHANNEL RESERVED INSTRUCTION CODES

The following instruction codes are for use with the Gated Input Channel. Device addresses for additional input channels will be assigned at the time of system definition.

MNEMONIC	OCTAL	FUNCTION
A. EXTERNAL CONTROL		
NONE		
B. TRANSFER		
INA 60	102160	Input from Channel to A Register
INB 60	102260	Input from Channel to B Register
IME 60	102060	Input from Channel to Memory
CIA 60	102560	Input from Channel to cleared A Register
CIB 60	102660	Input from Channel to cleared B Register
C. SENSE		
SEN 460	101460	Sense Transfer In Request

Table H-6
BUFFER INPUT CHANNEL RESERVED INSTRUCTION CODES

The following instruction codes are for use with the Buffer Input Channel. Device addresses for additional input channels will be assigned at the time of system definition.

MNEMONIC	OCTAL	FUNCTION
A. EXTERNAL CONTROL		
NONE		
B. TRANSFER		
INA 62	102162	Input from Channel to A Register
INB 62	102262	Input from Channel to B Register
IME 62	102062	Input from Channel to Memory
CIA 62	102562	Input from Channel to Cleared A Register
CIB 62	102662	Input from Channel to Cleared B Register
C. SENSE		
SEN 462	101462	Sense Transfer In Request

Table H-7
GATED OUTPUT CHANNEL RESERVED INSTRUCTION CODES

The following instruction codes are for use with the Gated Output Channel. Device addresses for additional output channels will be assigned at the time of system definition.

MNEMONIC	OCTAL	FUNCTION
A. EXTERNAL CONTROL		
NONE		
B. TRANSFER		
ØAR 60	103160	Output from A Register through Channel
ØBR 60	103260	Output from B Register through Channel
ØME 60	103060	Output from Memory through Channel
C. SENSE		
SEN 260	101260	Sense Data Request

Table H-8

BUFFER OUTPUT CHANNEL RESERVED INSTRUCTION CODE

The following codes are for use with the Buffer Output Channel. Device addresses for additional Output Channels will be assigned at the time of system definition.

MNEMONIC	OCTAL	FUNCTION
A. EXTERNAL CONTROL		
NONE		
B. TRANSFER		
ØAR 62	103162	Output from A Register through Channel
ØBR 62	103262	Output from B Register through Channel
ØME 62	103062	Output from Memory through Channel
C. SENSE		
SEN 262	101262	Sense Data Request

Table H-9
HIGH SPEED PAPER TAPE I/O RESERVED INSTRUCTION CODES

The following instruction codes are for use with the Paper Tape I/O unit. For additional units, device addresses will be assigned at the time of system definition. If only a reader or a punch is attached, use only those codes which apply.

MNEMONIC	OCTAL	FUNCTION
A. EXTERNAL CONTROL		
EXC 037	100037	CONNECT PUNCH to BIC
EXC 437	100437	STOP READER
EXC 537	100537	START READER
EXC 637	100637	PUNCH BUFFER
EXC 737	100737	READ ONE CHARACTER
B. TRANSFER		
OAR 37	103137	LOAD BUFFER from A Register
OBR 37	103237	LOAD BUFFER from B Register
OME 37	103037	LOAD BUFFER from Memory
INA 37	102137	READ BUFFER into A Register
INB 37	102237	READ BUFFER into B Register
IME 37	102037	READ BUFFER into Memory
CIA 37	102537	READ BUFFER into cleared A Register
CIB 37	102637	READ BUFFER into cleared B Register
C. SENSE		
SEN 537	101537	Sense BUFFER READY

Table H-10
MAGNETIC TAPE UNIT RESERVED INSTRUCTION CODES

The following instruction codes are for use with the first MTU. Device addresses 10_8 through 13_8 are reserved for MTU's.

MNEMONIC	OCTAL	FUNCTION
A. EXTERNAL CONTROL		
EXC 010	100010	READ ONE RECORD BINARY
EXC 110	100110	READ ONE RECORD BCD
EXC 210	100210	WRITE ONE RECORD BINARY
EXC 310	100310	WRITE ONE RECORD BCD
EXC 410	100410	WRITE FILE MARK
EXC 510	100510	FORWARD ONE RECORD
EXC 610	100610	BACKSPACE ONE RECORD
EXC 710	100710	REWIND
B. TRANSFER		
ØAR	103110	LOAD BUFFER from A Register
ØBR	103210	LOAD BUFFER from B Register
ØME	103010	LOAD BUFFER from Memory
INA	102110	READ BUFFER into A Register
INB	102210	READ BUFFER into B Register
IME	102010	READ BUFFER into Memory
CIA	102510	READ BUFFER into cleared A Register
CIB	102610	READ BUFFER into cleared B Register
C. SENSE		
SEN 010	101010	Sense PARITY ERROR
SEN 110	101110	Sense BUFFER READY
SEN 210	101210	Sense MTU READY
SEN 310	101310	Sense FILE MARK
SEN 410	101410	Sense HIGH DENSITY
SEN 510	101510	Sense END OF TAPE
SEN 610	101610	Sense BEGINNING OF TAPE
SEN 710	101710	Sense REWINDING

APPENDIX I
STANDARD CHARACTER CODES

APPENDIX I
DATA 620 STANDARD BCD CODES

SYMBOL	ASCII	PRINTER	MAG TAPE	HOLLERITH
@	300	00	32	0-2-8
A	301	01	61	12-1
B	302	02	62	12-2
C	303	03	63	12-3
D	304	04	64	12-4
E	305	05	65	12-5
F	306	06	66	12-6
G	307	07	67	12-7
H	310	10	70	12-8
I	311	11	71	12-9
J	312	12	41	11-1
K	313	13	42	11-2
L	314	14	43	11-3
M	315	15	44	11-4
N	316	16	45	11-5
O	317	17	46	11-6
P	320	20	47	11-7
Q	321	21	50	11-8
R	322	22	51	11-9
S	323	23	22	0-2
T	324	24	23	0-3
U	325	25	24	0-4

SYMBOL	ASCII	PRINTER	MAG TAPE	HOLLERITH
V	326	26	25	0-5
W	327	27	26	0-6
X	330	30	27	0-7
Y	331	31	30	0-8
Z	332	32	31	0-9
[	333	33	75	12-5-8
\	334	34	36	0-6-8
]	335	35	55	11-5-8
↑	336	36	17 (Note)	7-8
←	337	37	20	2-8
blank	240	40	20	No Punch
!	241	41	52	11-2-8
"	242	42	35	0-5-8
#	243	43	37	0-7-8
$	244	44	53	11-3-8
%	245	45	57	11-7-8
&	246	46	77	12-7-8
'	247	47	14	4-8
(	250	50	34	0-4-8
)	251	51	74	12-4-8
*	252	52	54	11-4-8
+	253	53	60	12
,	254	54	33	0-3-8

Note: End of File for Mag Tape

SYMBOL	ASCII	PRINTER	MAG TAPE	HOLLERITH
-	255	55	40	11
.	256	56	73	12-3-8
/	257	57	21	0-1
0	260	60	12	0
1	261	61	01	1
2	262	62	02	2
3	263	63	03	3
4	264	64	04	4
5	265	65	05	5
6	266	66	06	6
7	267	67	07	7
8	270	70	10	8
9	271	71	11	9
:	272	72	15	5-8
;	273	73	56	11-6-8
<	274	74	76	12-6-8
=	275	75	13	3-8
>	276	76	16	6-8
?	277	77	72	12-2-8

TELETYPE CHARACTER CODES

Teletype Character	620 Internal Code	Teletype Character	620 Internal Code
0	260	Y	331
1	261	Z	332
2	262	blank	240
3	263	!	241
4	264	'	242
5	265	#	243
6	266	$	244
7	267	%	245
8	270	&	246
9	271	'	247
A	301	(	250
B	302	)	251
C	303	*	252
D	304	+	253
E	305	,	254
F	306	–	255
G	307	.	256
H	310	/	257
I	311	:	272
J	312	;	273
K	313		274
L	314	=	275
M	315		276
N	316	?	277
O	317	@	300
P	320		333
Q	321		334
R	322		335
S	323		336
T	324		337
U	325	Rub Out	377
V	326	NUL	200
W	327	SOM	201
X	330	EOA	202

Teletype Character	620 Internal Code	Teletype Character	620 Internal Code
EOM	203	TAPE AUX ON	222
EOT	204	X-OFF	223
WRU	205	TAPE OFF AUX	224
RU	206	ERROR	225
BEL	207	SYNC	226
FE	210	LEM	227
H TAB	211	SO	230
LINE FEED	212	S1	231
V TAB	213	S2	232
FORM	214	S3	233
RETURN	215	S4	234
SO	216	S5	235
SI	217	S6	236
DCO	220	S7	237
X-ON	221		

APPENDIX J
AUTO INDEX INSTRUCTION GROUP

APPENDIX J
AUTO INDEX INSTRUCTION GROUP

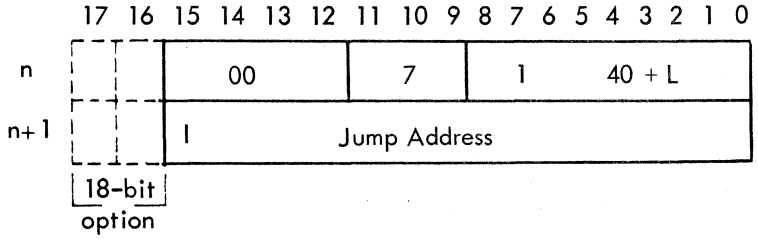
The Auto Index Instruction Group (optional) uses the first 32_{10} (37_8) words of memory as pointers or counters. Four instructions are provided for altering and testing the contents of these memory locations. The address field a specifies the index memory location and the type of indexing and logical test to be performed. Table G8(a), Appendix G, summarizes the control functions specified by the address field. Table G8(b) summarizes the auto index instructions. The general flow for this instruction group is shown in Fig. 3-12.

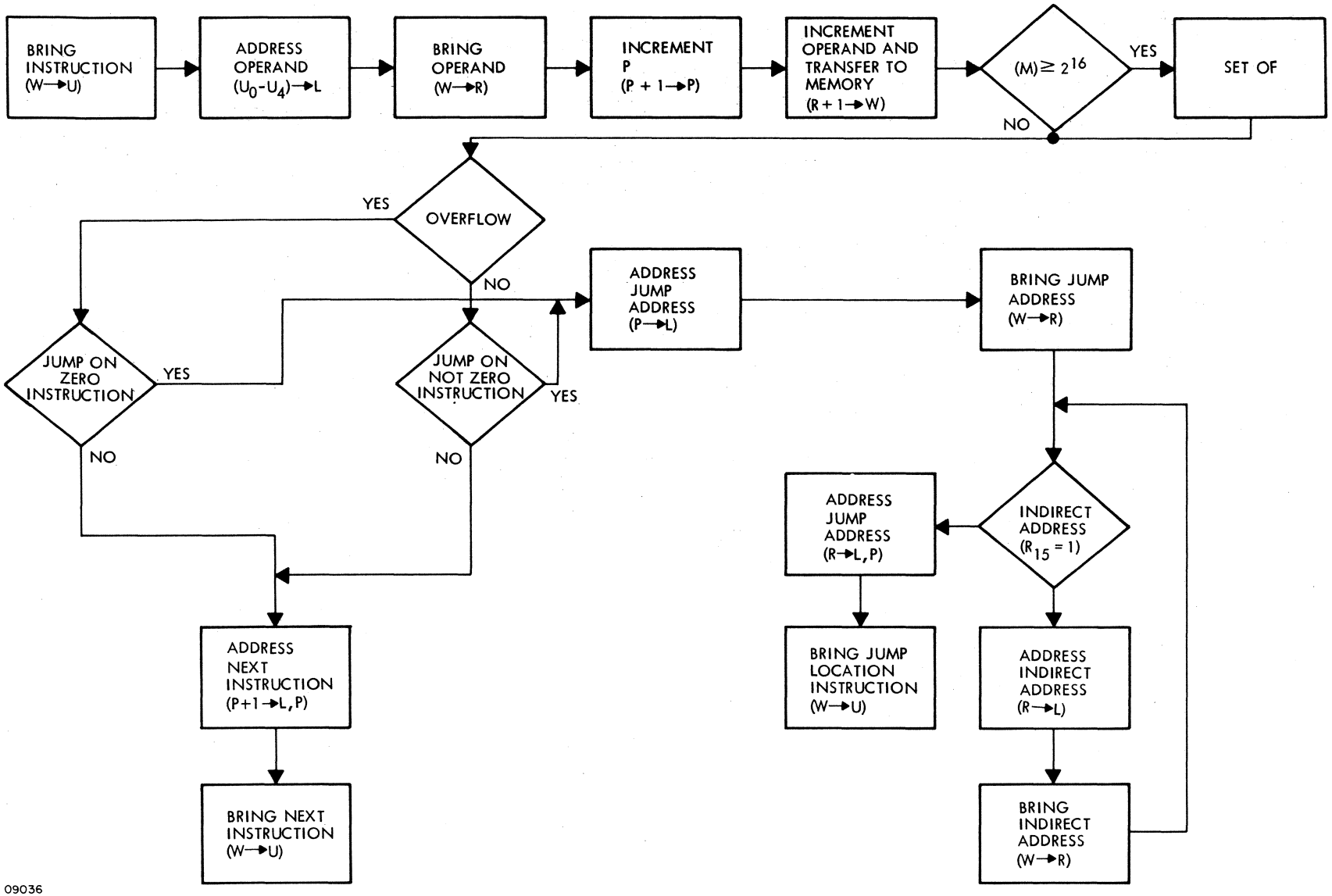
IRJZ — Increment Replace and Jump if Zero — Timing: 3 Cycles (No Jump), 4 Cycles (Jump)

The contents of L (L = 0 to 37_8) is incremented by one, Mod 2^{16}, and the sum is placed in L. If the sum is zero, a jump is executed to the Jump Address. If the sum is not zero, the next instruction in the sequence is executed. After execution, if (M) 2^{15} (2^{17}), the overflow indicator (OF) is set.

Indexing: No
Indirect Addressing: Yes
Registers Altered: L, P, OF

IRJN — Increment Replace and Jump if Not Zero — Timing: 3 Cycles (No Jump), 4 Cycles (Jump)



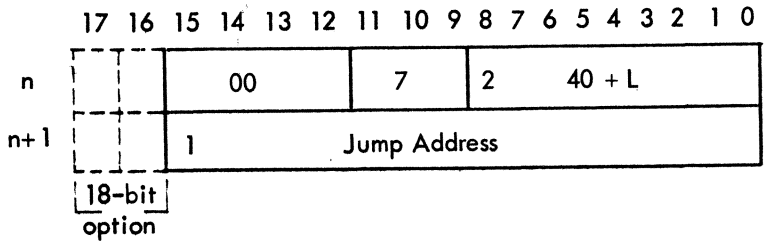


Auto Instruction, Increment/Jump, General Flow

The contents of L (L = 0 to 37_8) are incremented by one Mod 2^{16} and the sum is placed in L. If the sum is not zero a jump to the Jump Address is executed. If the sum is zero, the next instruction in sequence is executed. After execution, if (M) $\geq 2^{15}$ (2^{17}) the overflow indicator (OV) is set.

Indexing: No
Indirect Addressing: Yes
Registers Altered: L, P, OV

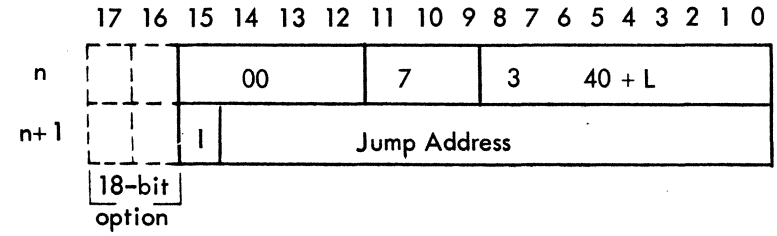
DRJZ — Decrement Replace and Jump if Zero — Timing: 4 Cycles (No Jump)
5 Cycles (Jump)



The contents of L (L = 0 to 37_8) are incremented by one, Mod 2^{15} (2^{17}), and the difference is placed in L. If the difference is zero, a jump is executed to the Jump Address. If the difference is not zero, the next instruction in sequence is executed. After execution, if (M) $> -2^{15}$ (-2^{17}) the overflow indicator (OF) is set.

Indexing: No
Indirect Addressing: Yes
Registers Altered: L, P, OF

DRJN — Decrement Replace and Jump if Not Zero — Timing: 4 Cycles (No Jump)
5 Cycles (Jump)



The contents of L (L = 0 to 37_8) are decremented by one, Mod 2^{15} (2^{17}), and the difference is placed in L. If the difference is not zero a jump is executed to the Jump Address. If the difference is zero, the next instruction in sequence is executed. After execution, if (M) $> -2^{15}$ (-2^{17}), the overflow indicator (OF) is set.

Indexing: No
Indirect Addressing: Yes
Registers Altered: L, P, OF

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