

WANG

3403

**4200 - SERIES
VS WORKSTATIONS**

Models:

4210

4220

**Customer Engineering
Product Maintenance Manual**

741-1302

PREFACE

This microfiche document is the Standard Maintenance (STD) Manual for the Wang 4210 and 4220 Workstations. It is organized in accordance with the approved STD outline established at the Field/Home Office Publications meetings conducted on September 14th and 15th, 1982. The scope of this manual reflects the type of maintenance philosophy selected for this product (swap unit, printed circuit assembly chip level or any combination thereof).

This manual provides the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot and repair the Wang 4210 and 4220 Workstations. It will be updated on a regular schedule.

Third Edition (August 1984)

This edition of the 4210/4220 Workstation STD manual obsoletes document number 729-1302-A. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as Product Update Bulletins (PUBs) or subsequent editions.

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WARNING

Do not open the switching Power Supply under any circumstance. Extremely dangerous voltage and current levels (in excess of 300 volts and unlimited current) are present within the Power Supply. Do not attempt to repair the switching Power Supply; it is field replaceable only. After powering the unit down and disconnecting the ac power plug from the wall outlet, allow one minute before removing the Power Supply to provide adequate time for any residual voltage to drain through the bleeder resistors.

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CHAPTER

1

**INTRO-
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CHAPTER 1 INTRODUCTION

1.1 SCOPE AND PURPOSE OF MANUAL

This manual contains installation, operation and maintenance information for the 4210 Local VS Workstation and the 4220 Remote VS Workstation (Figure 1-1). These workstations are supported in the field on a board-swap basis. This manual meets the support requirements by detailing maintenance tasks, functional theory and parts replacement to the same level.

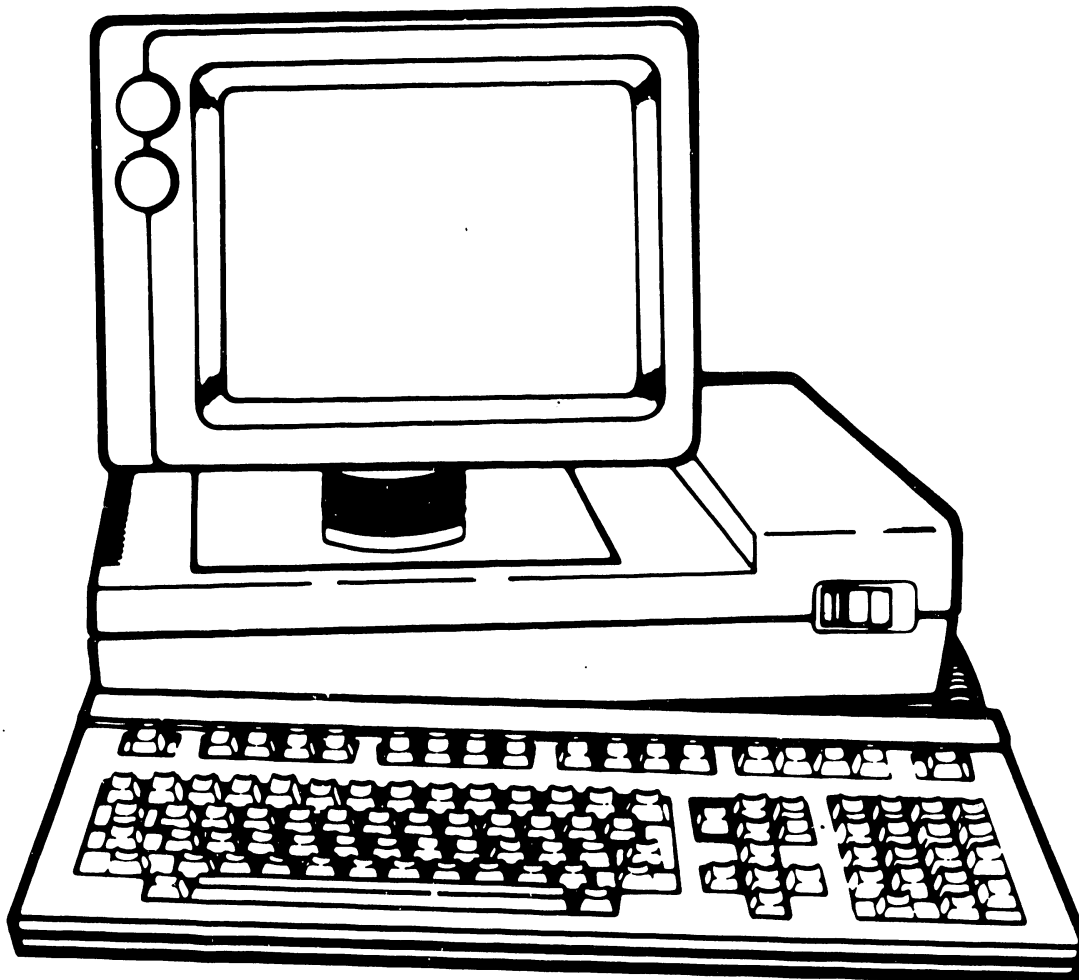


Figure 1-1. 4210/4220 Workstation

1.2 APPLICABLE DOCUMENTATION

1.2.1 PUBLICATIONS

Publications relating to the 4210 and 4220 Workstations and their installation, operation and use on VS systems are listed in Table 1-1.

Table 1-1. Related Publications

PUBLICATION	ORDER NUMBER
VS-100 Maintenance Manual	729-0871-A, -A1
VS 95 Maintenance Manual	729-1224-A, -A1
VS-50/60/80 Central Processor Preliminary Hardware Manual	729-0822
VS 25/45 Maintenance Manual	729-1032-B
VS Input/Output Processor Manual	729-0824
22V17 WS/Printer/AWS I/O Processor PSN	729-0932
Site Planning Guide	700-5978
VS System Administrative Reference for O/S 60	800-1144-01
VS O/S Release 60 Software Bulletin	800-3111
CE Documentation Control & Processing Catalog/Index	729-0000-C
Corporate Literature Catalog	700-7647

1.2 APPLICABLE DOCUMENTATION, continued1.2.1 PUBLICATIONS, continued

Ordering addresses for publications appear below:

Address For User Manuals Address For CE Manuals
(Prefix 700-, 800-): (Prefix 729-):

WANG LABS, INC.

Supplies Division

M/S 1711

c/o Order Entry Dept.

800 Chelmsford St.

Lowell, MA 01851

WANG LABS, INC.

Order Entry Dept.

M/S 8220

c/o (Your Area Rep.)

437 So. Union Street

Lawrence, MA 01843

1.2.2 DIAGNOSTICS

The 4210 and 4220 Workstations use Built-In Test (BIT) diagnostic PROMs to isolate malfunctions in a defective assembly or board. On-line diagnostics are also available in the VS diagnostic test operating system (DTOS). Table 1-2 lists the part numbers and current revisions for the BIT PROMs along with the documentation part numbers for those packages.

Table 1-2. Diagnostics

	<u>4210 BIT PROM</u>	<u>4220 BIT PROM</u>
	<u>DIAGNOSTICS</u>	<u>DIAGNOSTICS</u>
Package P/N	195-2536-3	195-2700-3
Document P/N	760-1114-A	760-1193
Document Rev.	93B8	9380
Software P/N	702-0247	702-0271
Software Rev.	53B8	5380
PROM P/N	378-8043	378-8047

1.3 DESCRIPTION

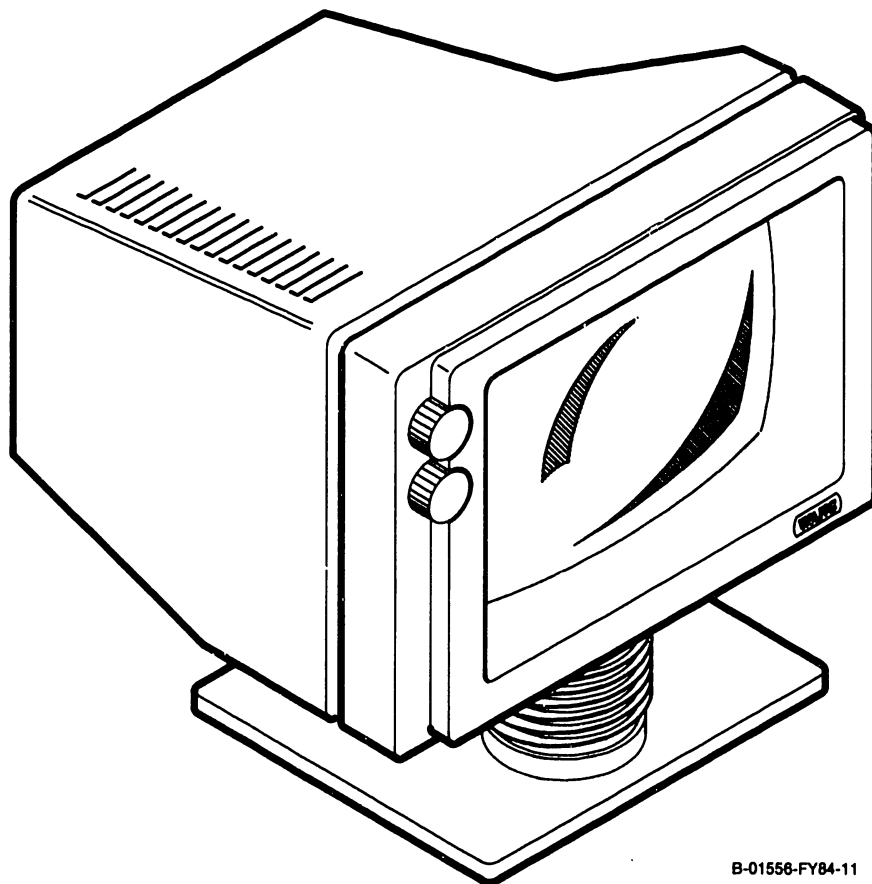
The 4210 and 4220 Workstations are the first in a series of modular, easy-to-service workstations offered by Wang for VS customers. The 4210 and 4220 models find their application in the VS product line, as replacements for the 2246S/C and 2246R workstations, respectively. In addition to the functions normally associated with these earlier workstations, the 4210 provides the added capability of bit-mapped graphics. The 4220 offers a special graphics mode called character set graphics.

The workstations are Z-80 based and modular in design, comprising three basic components which operate together to provide the workstation functions. The modular approach allows greatly simplified methods of service to be employed in the field, as well as supporting the ergonomic design principles typical of Wang equipment.

1.3 DESCRIPTION, continued

1.3.1 VIDEO MONITOR

Figure 1-2 shows the Monitor used with the 4210/4220 Workstation. Note that this is the same Monitor used with the Wang Professional Computer. The unit provides an 80 column by 25 row, 12-inch diagonal, green-on-black viewing screen, with the cathode ray tube (CRT) and associated electronics housed in a two-piece enclosure. Altogether, the self-contained Monitor sits atop a pedestal attached by means of a ball-joint fitting. This allows the Monitor, and hence the viewing screen, to be tilted to suit the operator. The pedestal fits into a depression in the cover of the Electronics Base.



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Figure 1-2. Monitor

1.3 DESCRIPTION, continued

1.3.1 VIDEO MONITOR continued

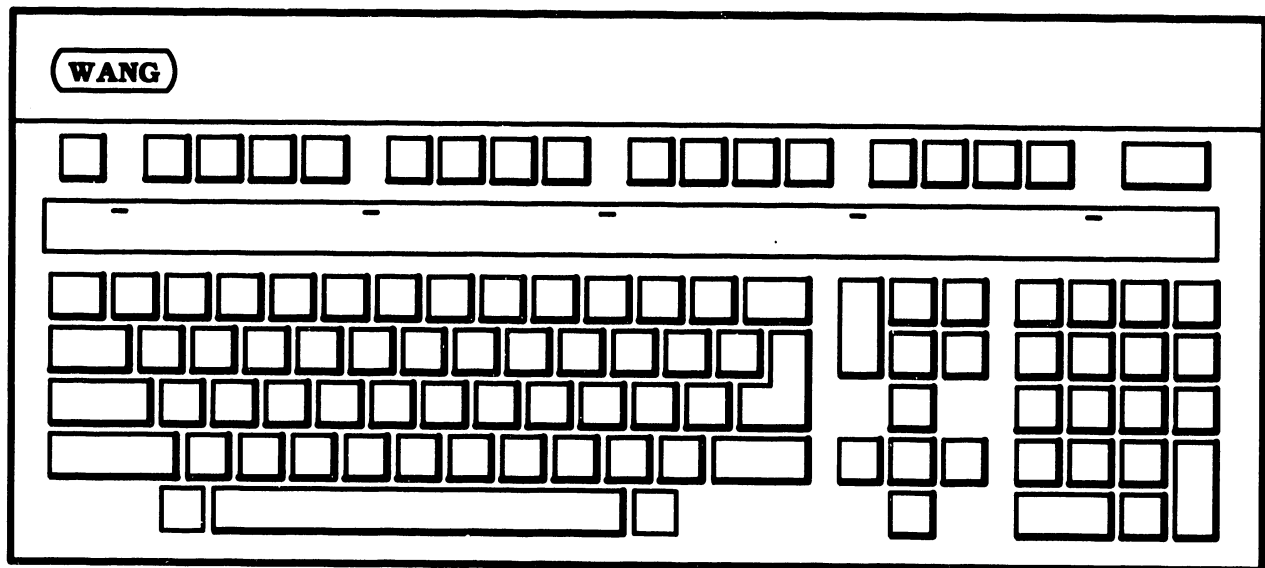
Brightness and contrast controls are placed in the upper left corner of the unit, with the brightness control on top and the contrast control below. The contrast control is functional in the 4220, but has no effect on the display in the 4210 Workstation.

Internally, the Monitor uses one of two printed circuit assemblies (PCAs) to process and display incoming video and synchronization signals. In early production units the 8244 PCA was used. Current production units, however, use the 8344 PCA. The Monitor has no internal power supply of its own, but relies on a +12 Vdc input from the Electronics Base.

A dual cable connects the Monitor to the Electronics Base, with one of the cables connecting power between the units and the other carrying the video and synchronization signals. The dual cable is terminated on both ends with a molded 3-pin DIN connector for the power cable and a molded 8-pin DIN connector for the video cable. The cables connect to the Monitor on its underside, through two access holes in the cover. The DIN sockets are mounted directly to the internal Monitor PCA.

1.3 DESCRIPTION, continued1.3.2 KEYBOARD

The 4210/4220 Workstation uses the low-profile, universal serial Keyboard in use in other current Wang products, including the Wang Professional Computer (Figure 1-3).



B-01558-FY84-13

Figure 1-3. Low-Profile Serial Keyboard

1.3 DESCRIPTION, continued

1.3.2 KEYBOARD continued

The low-profile serial Keyboard is a separate, detachable unit containing 101 keys and a programmable speaker. The Keyboard offers 16 programmable function keys, a HELP key, four cursor control keys (north, south, east and west arrows), as well as a calculator-style key pad. Standard word processing edit keys are also supported (e.g., INSERT, DELETE, MOVE, COPY).

The Keyboard is attached to the Electronics Base through a coil-cord emanating from the right rear corner of the Keyboard, and terminated in a 4-pin DIN connector. The Keyboard can thus be freely moved to suit the operator's preference.

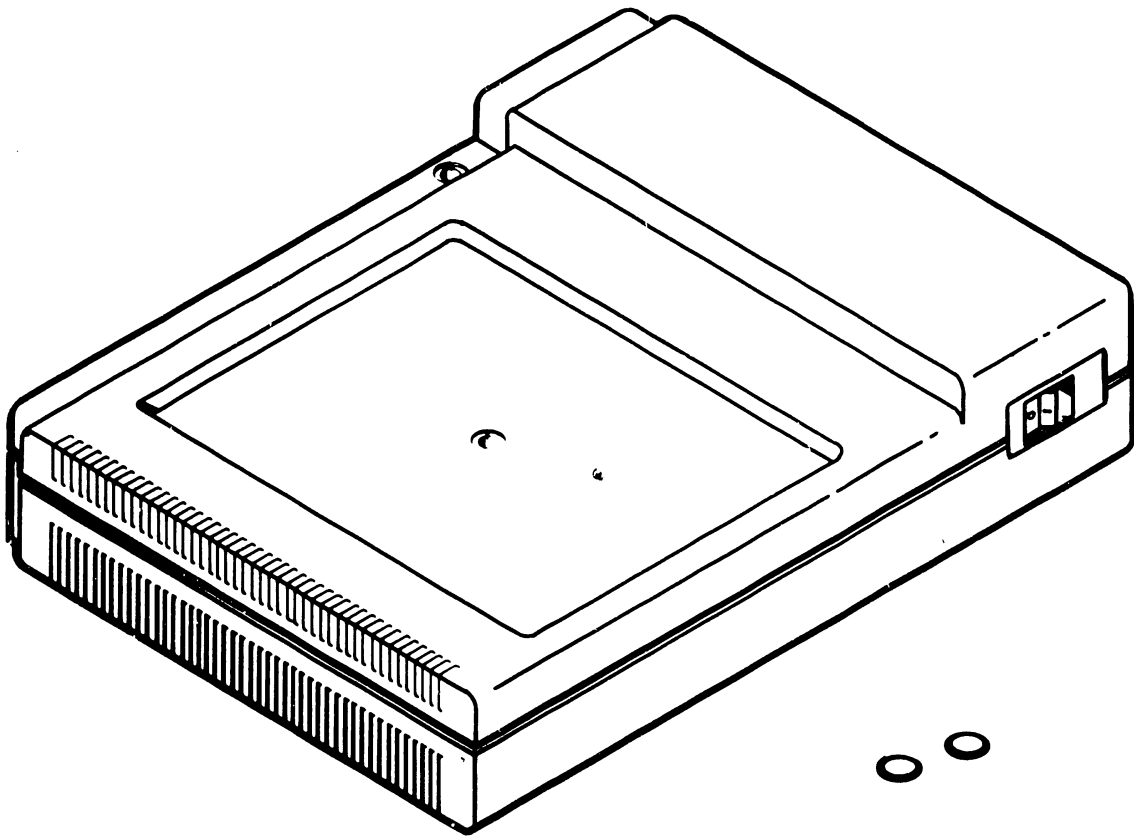
An additional feature of this Keyboard is a series of six light-emitting diode (LED) indicators. Five of these are placed above the section of typewriter keys, and one is built into the LOCK key. These LEDs are used to display information relative to the Built-In Test (BIT) diagnostics. The BIT is described in detail in Chapter 4 of this manual. The LED in the LOCK key is also used to indicate, during normal operation, that the caps-lock feature is active.

Communication between the Keyboard and the Electronics Base is in serial format at 62.5k baud. The Keyboard itself is microprocessor based, using an 8031 CPU with PROM-based microcode.

1.3 DESCRIPTION, continued

1.3.3 ELECTRONICS BASE

The Electronics Base houses the main logic PCAs associated with either the 4210 or 4220 Workstation, along with an 80-Watt Harris Switching Power Supply (Figure 1-4).



B-01556-FY84-21

Figure 1-4. Electronics Base

1.3 DESCRIPTION, continued

1.3.3 ELECTRONICS BASE, continued

The power supply is field replaceable only, and is not intended to be serviced in the field. The unit supplies +5 Vdc and +12 Vdc potentials to the operating circuitry of the workstation, and incorporates a built-in ventilating fan, ac line fuse, ac power cord connector, 115V/230V switch and ac power on/off (1/0) switch in one easy-to-replace package. The unit is mechanically fastened to the base with only two screws.

The exterior of the electronics base and the enclosed power supply are identical in both workstation models. The PCA loading of the base differentiates the 4210 from the 4220 Workstation.

1.3.3.1 4210 Electronics Base

The 4210 Electronics Base houses two PCAs which carry out workstation logic functions. The two PCAs are the 210-8264 CPU PCA (on top), and the 210-8263 Bit Map PCA (on bottom).

The front edge of the PCAs are secured in capture slots in the front of the base, and the connector headers at the rear of the PCAs interlock with each other and the edge of the base bottom and cover. The PCAs are spaced in the center by a support/spacer rod which fits between the PCAs, seated against the upper and lower parts of the base. The rod also provides support for the physical weight of the Monitor which is placed atop the Electronics Base.

1.3.3 ELECTRONICS BASE, continued

1.3.3.1 4210 Electronics Base, continued

The 8264 CPU PCA contains the Z-80 CPU, 64k bytes of main memory with parity, a standard Wang 928 serial data link and a 4k PROM containing the Built-In Test (BIT) power-up diagnostic. Workstation operating software (microcode) is downline loaded from the system host CPU and stored in main memory. The unit features software-loadable fonts which are also downline loaded from the system host. The connector header mounted on the rear of the PCA contains the DATA LINK BNC/TNC connectors for cable connection to the host.

The 8263 Bit Map PCA contains the Z-80 dual serial input/output device (DSIO), configured as a dual-port asynchronous receiver/transmitter (DART). One of the ports is used to interface CPU communications in parallel with the serial format required for the Keyboard. The second port is reserved for the RS-232C connector provided on the connector header at the rear edge of this PCA. The RS-232C port is not currently supported.

Also included on the 8263 Bit Map PCA are two planes or pages of screen memory, each arranged in a 16k x 16-bit format for a total of 32k bytes per page. The screen memory addressing logic, the CRT controller logic and other support logic are also on this PCA. At the rear of the PCA, a metal connector header carries an RS-232C connector and DIN connectors for the Keyboard and Monitor cables. The two PCAs are connected with a 50-conductor ribbon cable.

1.3.3.2 4220 Electronics Base

All circuitry for the 4220 Workstation logic functions is contained on the 210-8277 Remote Workstation Electronics PCA in the 4220 Electronics Base. The front edge of the PCA is secured in capture slots in the front of the base, and the connector header at the rear of the PCA interlocks with the edge of the base bottom and cover. A support rod fits in the center of the PCA and seats against the upper and lower parts of the base to provide support for the physical weight of the Monitor which is placed atop the Electronics Base.

The 8277 PCA contains the Z-80 CPU, 64k bytes of main memory with parity, two 4k PROMs for a total of 8k of PROM space containing the Built-In Test (BIT) power-up diagnostic and bootstrap microcode, 4k of display RAM and 4k of font RAM. A Motorola 6845 CRT controller (CRTC) device is used to develop synchronization signals for the Monitor. Workstation software (microcode) as well as the microcode required to service an attached parallel printer is downline loaded from the host CPU and stored in main memory. The unit features software-loadable fonts which are also downline loaded from the system host.

The unit also uses a Z-80 dual serial input/output (DSIO) device dedicated to the telecommunications task, while another DSIO device services the Keyboard interface and an auxiliary RS-232C port. A Centronics-compatible parallel printer interface is also provided. The header mounted on the rear of the PCA contains

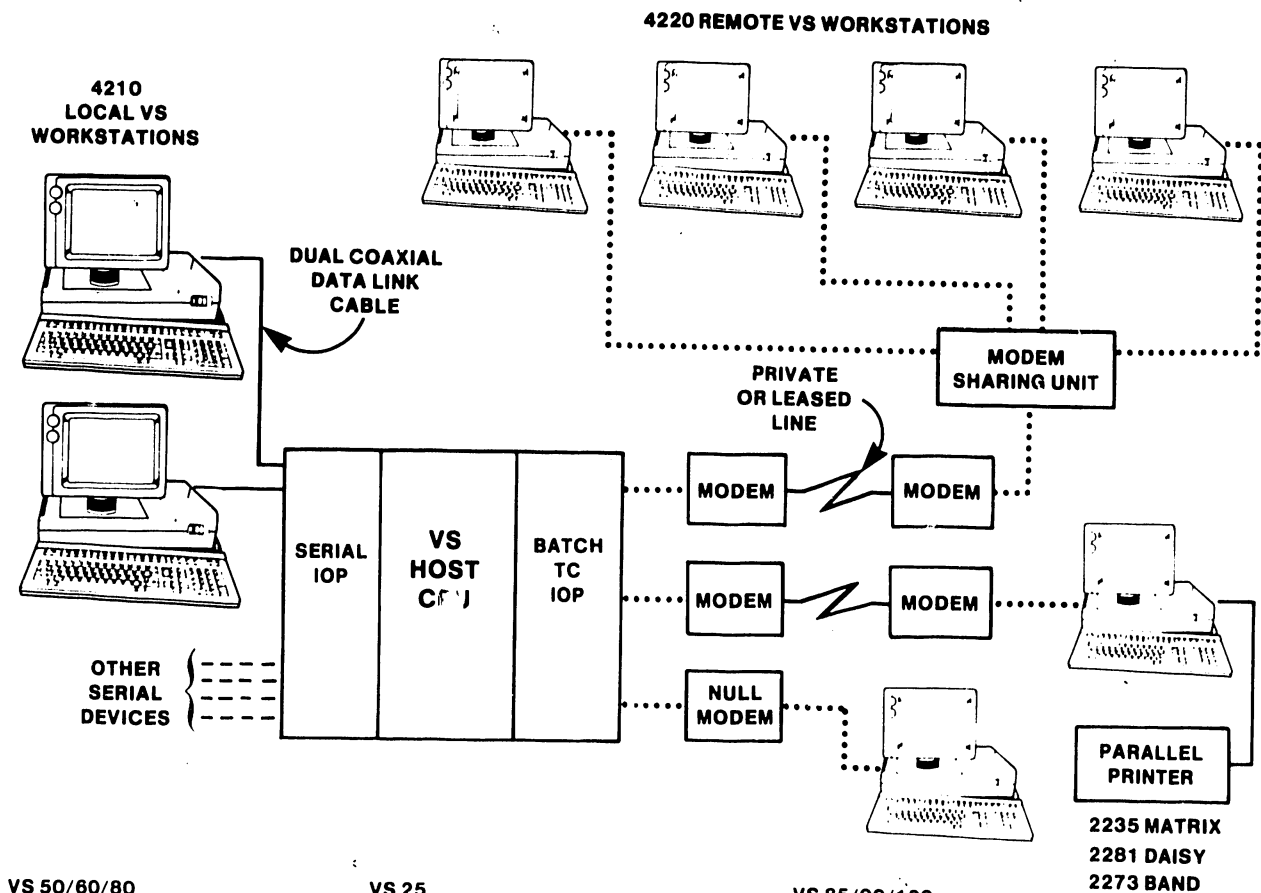
connectors required for the Keyboard, Monitor, RS-232C and the 36-pin parallel printer connections.

1.4 SYSTEM APPLICATIONS

1.4.1 4210 WORKSTATION SYSTEM APPLICATIONS

The 4210 Local VS Workstation is designed as a replacement for the familiar 2246S/C workstation in the VS product line. The 4210 Workstation supports the full range of data processing functions available on VS systems, as well as supporting word processing on VS systems with appropriate software. In the word processing mode, the 4210 appears as a 32k workstation to the host CPU. Communication with the host CPU is over a dual coaxial cable using a standard 928 data link arrangement.

Figure 1-5 is a representative VS system showing the host CPU with the appropriate input/output processor (IOP) for the 4210 local workstation. In the VS 50/60/80, 4210 workstations communicate with the host CPU via a 22V17 extended serial IOP designed for use with serial devices such as workstations and printers. In the VS 90/100, the appropriate serial IOP is the 22V27.



VS 50/60/80

SERIAL IOP: 22V17-1, 2
 -1 = 8 PORT, 16 EXTENDED
 -2 = 16 PORT, 32 EXTENDED
 BATCH TC IOP: 22V06-1, -2, -3
 -1 = 1 PORT
 -2 = 2 PORT
 -3 = 3 PORT

VS 25

SERIAL I/O DEVICE ADAPTER
 210-7906-A
 SINGLE PORT TC DEVICE ADAPTER
 210-8337-A
 RS-232C

VS 85/90/100

SERIAL IOP: 22V27-1, 2
 -1 = 8 PORT
 -2 = 16 PORT
 BATCH TC IOP: 22V26-1, -2, -3
 -1 = 1 PORT
 -2 = 2 PORT
 -3 = 3 PORT

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Note: Disk drives, tape drives, and other elements of a VS system are not shown.

Figure 1-5. 4210 System Applications

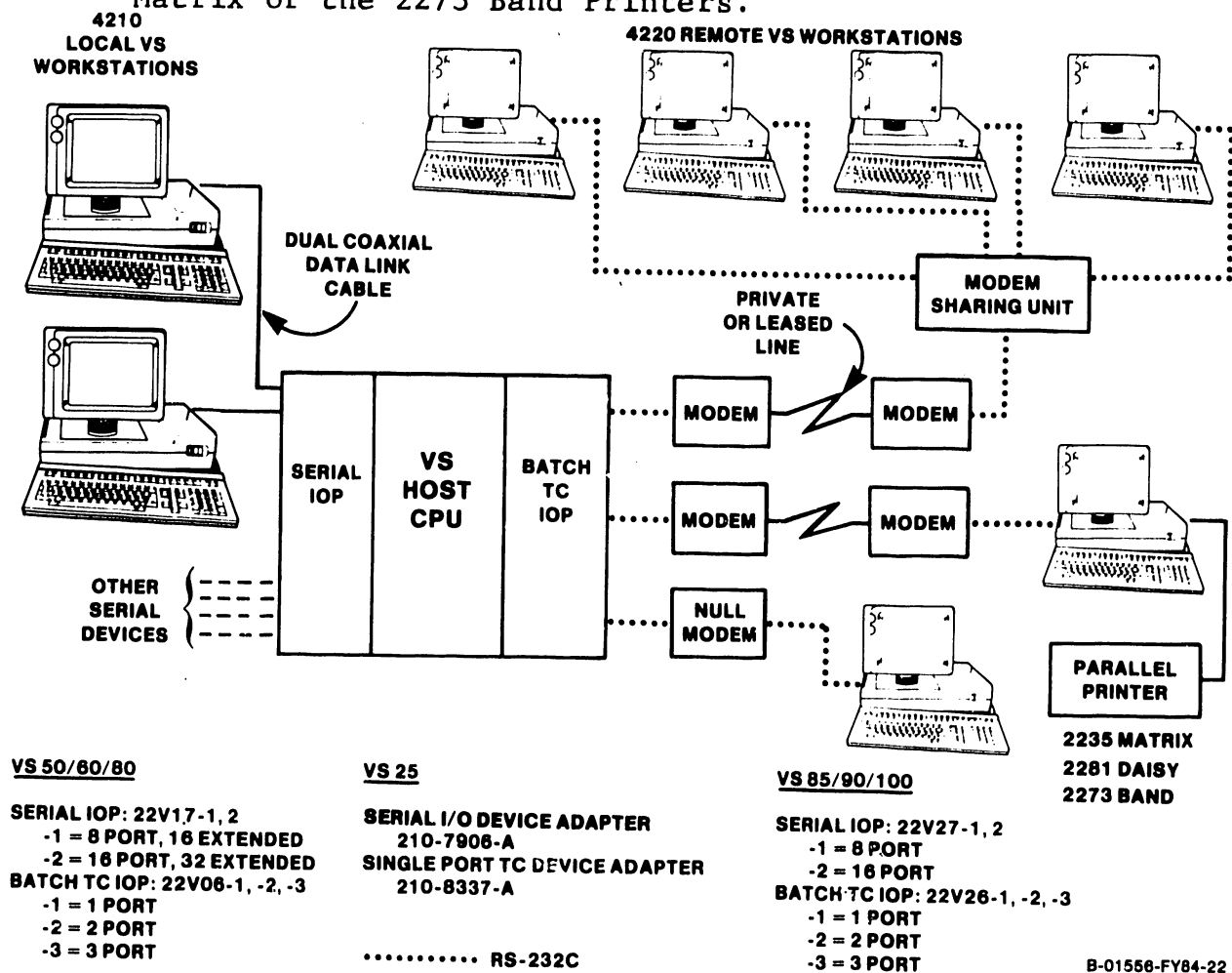
1.4.2 4220 SYSTEM APPLICATIONS

The 4220 Remote VS Workstation is designed as a replacement for the familiar 2246R workstation in the VS product line. The 4220 Workstation supports a wide range of data processing functions but does not support word processing.

Communication with the host CPU is carried out via telecommunications, using the workstation in conjunction with an appropriate modem to effect the communications link. Thus, 4220 workstations geographically remote from a host CPU appear as locally connected units. Mechanical/electrical interface between the workstation and the modem is RS-232C format.

Functioning as a stand-alone remote workstation, the 4220 includes a built-in communications controller with a full duplex, asynchronous or synchronous serial interface. The workstation can be programmed to support a variety of line protocols including HDLC and IBM 2780/3780 emulation. Currently, however, system microcode supports only bisynchronous protocol at 9600 baud.

Figure 1-5 is a representative VS system showing the host CPU with the appropriate input/output processor (IOP) for the 4220 Remote Workstation. In the VS 50/60/80, 4220 workstations communicate with the host CPU via a 22V06 batch TC IOP designed for use with remote telecommunicating devices. In the VS 90/100, the appropriate batch TC IOP is the 22V26. The figure also shows a 4220 Workstation connected locally via a null modem. Parallel printers which can be used with 4220 Workstation include the 2281 Daisy, the 2235 Matrix or the 2273 Band Printers.



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Figure 1-5. 4220 System Applications

Specifications for the 4210 and 4220 Workstations are given in Table 1-3.

Table 1-3. Workstation Specifications

PARAMETER	DESCRIPTION																
CRT:	12-inch diagonal, green on black, 80 column x 25 row, 24 rows supported by software																
4210 Data Link:	4.275 Mbps, serial asynchronous																
4220 TC Data Rates Supported (baud):	300, 600, 1200, 2400, 4800, 9600, 19.2k (Set at 9600 by current system microcode)																
4220 Protocols Supported:	BSC (Bisynchronous) currently supported by system microcode																
Keyboard Interface:	62.5k baud, asynchronous																
Microprocessor:	Z-80																
Line Tolerance:	<table border="0"> <thead> <tr> <th colspan="2">Volts</th> <th colspan="2">Hertz</th> </tr> <tr> <th>Min.</th> <th>Nom.</th> <th>Max.</th> <th>Frequency</th> </tr> </thead> <tbody> <tr> <td>90</td> <td>115</td> <td>132</td> <td>47 - 63</td> </tr> <tr> <td>180</td> <td>230</td> <td>264</td> <td>47 - 63</td> </tr> </tbody> </table>	Volts		Hertz		Min.	Nom.	Max.	Frequency	90	115	132	47 - 63	180	230	264	47 - 63
Volts		Hertz															
Min.	Nom.	Max.	Frequency														
90	115	132	47 - 63														
180	230	264	47 - 63														
Power Requirements:	100 Watts maximum, 80 Watts typical																
Ambient Operating Temperature:	60°F to 90°F (16°C to 32°C)																
Relative Humidity:	20% to 80% (non-condensing)																
Monitor Dimensions & Weight:	<table border="0"> <thead> <tr> <th>Height</th> <th>Width</th> <th>Depth</th> <th>Weight</th> </tr> <tr> <th><u>in. (cm)</u></th> <th><u>in. (cm)</u></th> <th><u>in. (cm)</u></th> <th><u>lb. (kg)</u></th> </tr> </thead> <tbody> <tr> <td>11.5</td> <td>13.0</td> <td>10.8</td> <td>15.0</td> </tr> <tr> <td>(29.2)</td> <td>(33.0)</td> <td>(27.4)</td> <td>(6.8)</td> </tr> </tbody> </table>	Height	Width	Depth	Weight	<u>in. (cm)</u>	<u>in. (cm)</u>	<u>in. (cm)</u>	<u>lb. (kg)</u>	11.5	13.0	10.8	15.0	(29.2)	(33.0)	(27.4)	(6.8)
Height	Width	Depth	Weight														
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11.5	13.0	10.8	15.0														
(29.2)	(33.0)	(27.4)	(6.8)														
Keyboard Dimensions & Weight:	<table border="0"> <thead> <tr> <th>Height</th> <th>Width</th> <th>Depth</th> <th>Weight</th> </tr> <tr> <th><u>in. (cm)</u></th> <th><u>in. (cm)</u></th> <th><u>in. (cm)</u></th> <th><u>lb. (kg)</u></th> </tr> </thead> <tbody> <tr> <td>1.7</td> <td>18.3</td> <td>7.8</td> <td>4.5</td> </tr> <tr> <td>(4.3)</td> <td>(46.5)</td> <td>(19.8)</td> <td>(2.0)</td> </tr> </tbody> </table>	Height	Width	Depth	Weight	<u>in. (cm)</u>	<u>in. (cm)</u>	<u>in. (cm)</u>	<u>lb. (kg)</u>	1.7	18.3	7.8	4.5	(4.3)	(46.5)	(19.8)	(2.0)
Height	Width	Depth	Weight														
<u>in. (cm)</u>	<u>in. (cm)</u>	<u>in. (cm)</u>	<u>lb. (kg)</u>														
1.7	18.3	7.8	4.5														
(4.3)	(46.5)	(19.8)	(2.0)														
Electronics Base Dimensions & Weight:	<table border="0"> <thead> <tr> <th>Height</th> <th>Width</th> <th>Depth</th> <th>Weight</th> </tr> <tr> <th><u>in. (cm)</u></th> <th><u>in. (cm)</u></th> <th><u>in. (cm)</u></th> <th><u>lb. (kg)</u></th> </tr> </thead> <tbody> <tr> <td>4.1</td> <td>19.0</td> <td>14.1</td> <td>6.5</td> </tr> <tr> <td>(10.5)</td> <td>(48.8)</td> <td>35.3)</td> <td>(2.9)</td> </tr> </tbody> </table>	Height	Width	Depth	Weight	<u>in. (cm)</u>	<u>in. (cm)</u>	<u>in. (cm)</u>	<u>lb. (kg)</u>	4.1	19.0	14.1	6.5	(10.5)	(48.8)	35.3)	(2.9)
Height	Width	Depth	Weight														
<u>in. (cm)</u>	<u>in. (cm)</u>	<u>in. (cm)</u>	<u>lb. (kg)</u>														
4.1	19.0	14.1	6.5														
(10.5)	(48.8)	35.3)	(2.9)														

The 4210/4220 Workstations are supported on the following operating system releases:

<u>4210</u>	<u>4220</u>
5.1.73	5.1.73
5.3.90	5.3.90
6.11.xx	6.20
6.20	

1.7 OPTIONS

Currently, there is no optional equipment available for the 4210 or 4220 Workstation.

CHAPTER

2

THEORY

OF

OPERA-

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CHAPTER 2
THEORY OF OPERATION

This chapter contains block level theory of operation discussions for major subassemblies of the 4210 and 4220 workstations. The equipment is covered in the subsections of this chapter as listed below.

Section 2.1	Monitor
Section 2.2	Keyboard
Section 2.3	4210 Electronics Base
Section 2.4	4220 Electronics Base

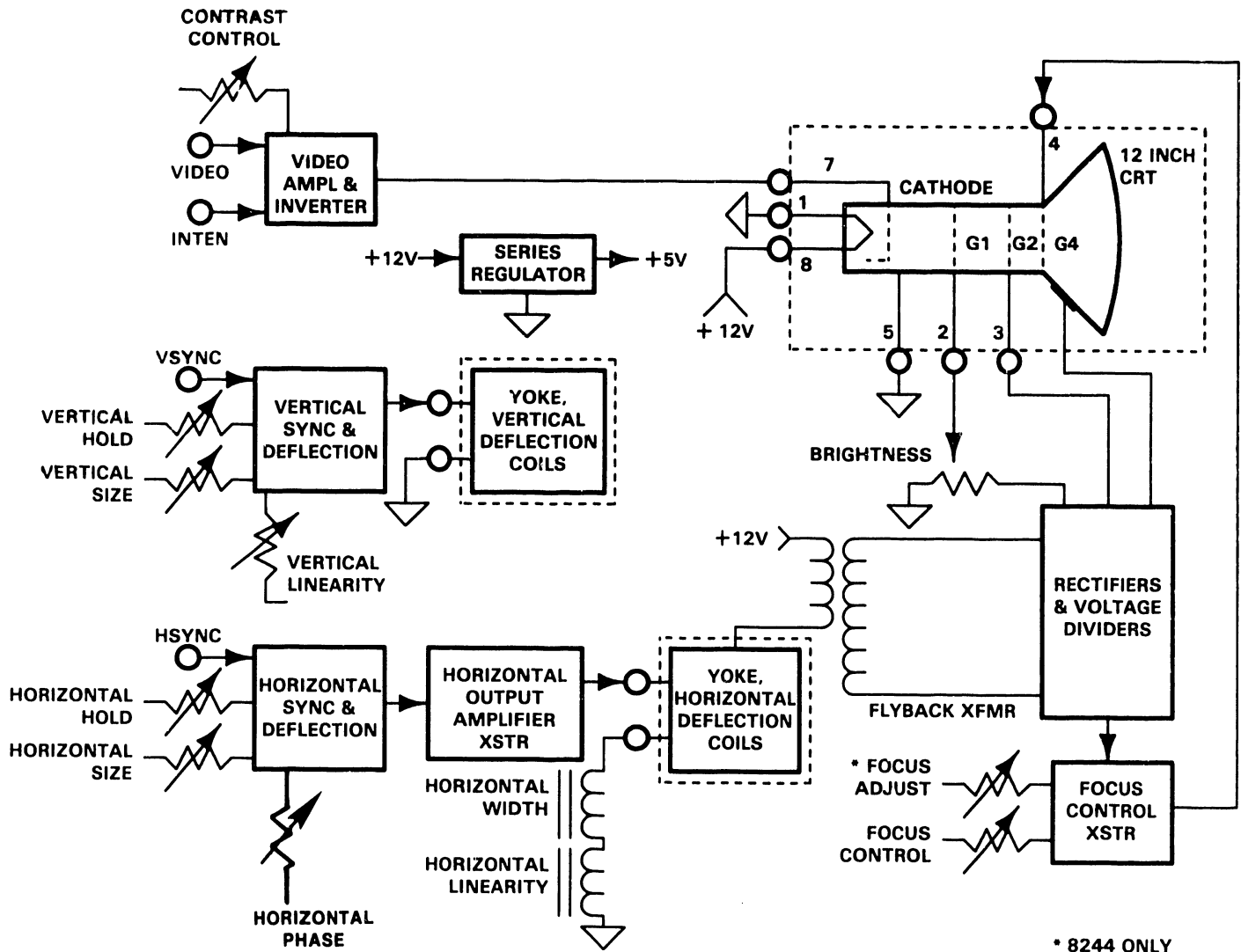
2.1 MONITOR

Refer to Figure 2-1 for the following discussion.

The Monitor unit contains a 12-inch green-on-black CRT with a Monitor PCA to process video and synchronization signals. The CRT screen has a capacity of 25 lines with 80 characters per line for a total of 2000 characters displayed.

The Monitor PCA receives +12 Vdc from the switching power supply in the Electronics Base via one lead of the Monitor power cable assembly. The +12 Vdc directly supplies the higher current horizontal deflection circuitry and the CRT filament. A series regulator is used to derive a +5 Vdc supply from the +12 Vdc input for the logic devices on the Monitor PCA.

2.1 MONITOR, continued



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Figure 2-1. Monitor PCA Block Diagram

2.1 MONITOR, continued

Input signals to the Monitor PCA include VIDEO, HSYNC, VSYNC and INTEN which are generated on the Bit Map PCA in the 4210, or the Remote Workstation Electronics PCA in the 4220. These signals are applied to the Monitor PCA via the eight-pin monitor video cable, buffered and then presented to the appropriate circuits on the PCA.

The VIDEO input is applied to a common-emitter stage in the video amplifier and inverter which provides amplification and inversion of the incoming video signal. The amplified and inverted video drives the cathode of the 12-inch (diagonal) CRT.

A special portion of the video amplifier and inverter receives the INTEN signal, which is used to intensify or highlight selected characters on the CRT screen. The INTEN signal causes the CRT cathode voltage to decrease, causing an increase in intensity for the instant that the INTEN signal is present. The front-panel contrast control adjusts the extent to which the circuit reacts to the INTEN signal. Intensification in the 4210 is achieved through software, so the contrast control has no effect on the 4210 display.

The horizontal sync (HSYNC) input is applied to the horizontal sync and deflection circuitry, comprising a horizontal processor device followed by a driver and, finally, the horizontal output amplifier. The horizontal phase and horizontal hold adjustments are inputs to the horizontal sync and deflection device and provide for a

2.1 MONITOR, continued

phase- and frequency-stable horizontal deflection ramp to be fed to the output stage.

The horizontal output transistor feeds the horizontal deflection coils of the yoke with a sawtooth-type deflection waveform. The current in the yoke windings develops an electro-magnetic field for deflecting the CRT electron beam in the horizontal direction. Adjustments for horizontal width and horizontal linearity form part of the total horizontal deflection coil load.

At horizontal retrace (flyback), the current field in the horizontal deflection coils of the yoke collapses and the resultant energy is stepped up by the flyback transformer. On the secondary side of the flyback transformer are separate windings which feed diode rectifiers and associated voltage divider circuits. Anode operating potential, focus (G4), G1 and G2 voltages are all derived from these rectifier and voltage divider circuits.

The vertical sync (VSYNC) input is applied to the vertical sync and deflection circuitry. Vertical processing is performed wholly by a vertical processor device which develops the final vertical sawtooth waveform that drives the vertical deflection coils of the yoke. Vertical hold, vertical size and vertical linearity adjustments are all inputs to the vertical sync and deflection device.

2.2 KEYBOARD

This section provides an overview of Keyboard operations as well as a functional block diagram level of theory discussion. For the following discussion refer to Figures 2-2 and 2-3.

2.2.1 KEYBOARD OVERVIEW

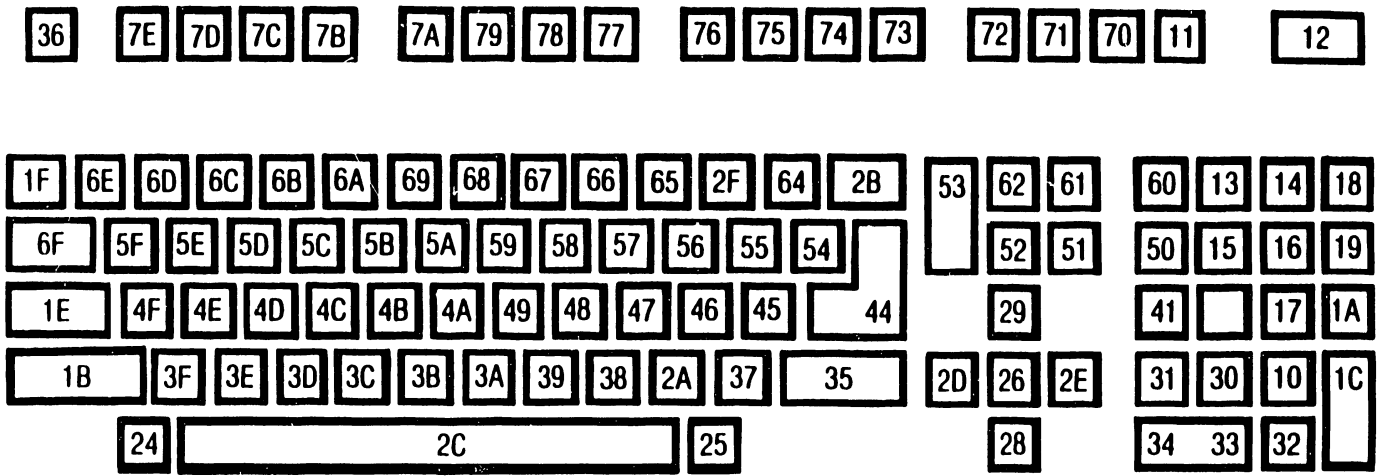
The detached Keyboard contains a dedicated 8031 microprocessor that accepts commands from the Z-80 in the Electronics Base while sending both Keyboard status data and keystroke data back to the Z-80. This communication occurs between the serial I/O port of the 8031 in the Keyboard and a Z-80 serial I/O located in the Electronics Base. The Z-80 SIO is a dual channel device. The Keyboard uses one channel and communicates in full-duplex mode.

Pressing a key causes the Keyboard to send a 7-bit keystroke code to the Z-80 in the Electronics Base. Every key has its own unique keystroke code, which is arbitrary and bears no relationship to any of the various character codes. In addition to the keystroke codes produced when they are pressed, the left and right SHIFT keys also generate different codes, called release codes, when they are released.

The release code for any key is identical to its keystroke code, but with high-order bit 7 set (i.e., keystroke code plus '80'). Special Keyboard commands establish release codes for up to five other designated keys or, alternately, for all of the keys on the Keyboard.

2.2 KEYBOARD, continued

2.2.1 KEYBOARD OVERVIEW, continued



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Figure 2-2. Keycode Assignments

2.2 KEYBOARD, continued

2.2.1 KEYBOARD OVERVIEW, continued

The LOCK and SHIFT keys have transmittable codes that allow maximum flexibility at the host system. The LOCK key has an LED (bit 0) for a visual indication that the key is engaged. The host system decodes the LOCK key transmittal code and returns a code back to the Keyboard through the 8031 to light the LOCK LED.

The left and right SHIFT keys have make and break codes in the Keyboard default scheme. When either SHIFT key is depressed, it will transmit its own X/Y code (make code). When the SHIFT key is released, a break code will be transmitted. When a shift condition is sensed, the host system will append an '80' bit to all keys until it sees the break code for the shift key.

Any key on the Keyboard is a potential repeat key. If the Keyboard is programmed to generate a release code for a particular key, the Z-80 in the Electronics Base can assume that the key remains down (or pressed) between the time it receives the keystroke code and the time it receives the corresponding release code. When a program monitoring the Keyboard recognizes a pressed key in this way, it can decide whether the key will repeat, and at what rate.

Figure 2-2 shows keystroke code assignments for the standard Keyboard. There are some possible keystroke codes and their corresponding release codes that are not produced by any key. One of

2.2 KEYBOARD, continued2.2.1 KEYBOARD OVERVIEW, continued

these, code '01', is used as a query response byte, which is always followed by one or more status bytes. When the Z-80 makes an inquiry by sending one of the query control byte sequences, it continues to accept Keyboard input until it receives the '01' query response byte and then accepts the appropriate number of status bytes before resuming normal Keyboard input.

A 4-conductor cable fitted with a 4-pin DIN connector carries power and interface signals between the Keyboard interface and the detached Keyboard. The Keyboard connector and 4-pin DIN connector signals are shown in Table 2-1.

Table 2-1

<u>CONNECTOR PIN NO.</u>	<u>DIN PLUG PIN NO.</u>	<u>SIGNAL</u>
1	N/C	Negative lead to 8-ohm speaker
2		Positive lead to 8-ohm speaker
3	1	Ground
4	2	Serial data output to Keyboard
5	4	5 Vdc power
6	3	Serial data input from Keyboard

LED control commands are used to turn on individual LEDs as well as to turn all LEDs on and off. The Keyboard LEDs are used to indicate diagnostic errors. The LED status command allows the host system to read the LED status at any time. The Keyboard is initialized with all LEDs off.

2.2 KEYBOARD, continued

2.2.1 KEYBOARD OVERVIEW, continued

N-key rollover exists between all encoded keys on the Keyboard. When a key is depressed while other keys are held down, the Keyboard will be able to output the latest keycode. Two 8-bit switchbanks on the Keyboard identify the particular Keyboard configuration.

The Keyboard interface in the Electronics Base is designed around a Z-80 dual serial input/output (DSIO) device operating at 62.5K baud. On power-up or system reset, hardware initializes the DSIO to transmit and receive serial protocol that consists of one start bit (cleared to zero), an 8-bit data word (least significant bit first), and two stop bits (set to one), without parity.

2.2.2 KEYBOARD THEORY OF OPERATION

Refer to Figure 2-3 for the following discussion.

The 8031 device is a single-component 8-bit microprocessor that contains 128 x 8-bit internal RAM memory, an internal oscillator and timing circuit for data synchronization, and a full duplex serial port UART. The 8031 device requires one supply voltage (+5 volts) for operation. Keyboard data is either sent or received across the full-duplex Keyboard interface.

2.2 KEYBOARD, continued

2.2.2 KEYBOARD THEORY OF OPERATION, continued

A 4 MHz crystal-generated clock is to synchronize the 8031 with various other components located on the board. This clock is necessary since only power and data are transmitted from the Electronics Base.

The 8031 uses its port zero lines as both the data and the address bus in a multiplexed bus scheme. Lines D0 - D7 in Figure 2-3 identify the shared bus. Signal ALE (address latch enable) enables the address latch when the bus is in the address mode, thus storing an address in the latch. The address latch addresses the EPROM while signal PSEN (program store enable) enables the EPROM to read the instruction at that address onto the bus, which is now in data mode. The EPROM stores 8031 operational routines.

At power-up, the reset circuit sets the 8031 program counter to zero and the 8031 starts executing its initialization code from the EPROM. The initialization routine performs the following tasks:

- o configure internal UART to 62.5K baud
- o configure line protocol (1 start bit, 8 data bits, 2 stop bits)
- o load zeros to sound generator
- o clear LEDs
- o set up the internal timers

After initialization, the 8031 starts its X axis scan routine, continuously polling port 1 for an input from the X/Y matrix. The Keyboard keys are

2.2 KEYBOARD, continued

2.2.2 KEYBOARD THEORY OF OPERATION, continued

laid out in a 16 x 8 X/Y matrix for a total of 128 possible configurations. Not all configurations are used. The 8031 supplies three scan lines (A8, A9, A10) to the two 3-to-8 decoders. The three scan lines count in binary from zero to 7 for each of the two decoders, thus causing a strobe to occur sequentially from X_0 to X_{15} .

The Y lines in the matrix are the return lines to the 908 device. When a key is depressed, the capacitive reactance is sensed by the 908 device and the 908 device translates the sense to a TTL level for the 8031. Upon receipt of the input from the 908, the 8031 reads the 908 input again to confirm the original read. The 8031 now looks in an internal table for the keycode that matches the Y location from the 908 device and the X location from the 3-to-8 decoders. These are the codes shown in Figure 2-2.

The keycode is then sent to the 8031's internal UART where it is serialized. A start bit and two stop bits are added and the serial stream is transmitted to the Electronics Base. After transmission of the last bit in the stream, the 8031 UART generates an internal interrupt which causes the 8031 to resume its X axis scanning routine.

The X portion of the X/Y matrix also serves to read the settings of the two on-board switchbanks. Each one of the switches is connected on one side to one of the X lines.

2.2 KEYBOARD, continued

2.2.2 KEYBOARD THEORY OF OPERATION, continued

Each X line is normally pulled up to 5V. The other side of each switch is connected to one common transistor. When an X line is strobed (brought low) and its switch is closed, the strobe is coupled through the switch to the transistor and the transistor changes state.

This pulse is applied to the 8031 as an interrupt at P_3^2 , and the 8031 registers the switch closure in an internal register dedicated to holding the switch settings. When an X line is strobed (brought low) and its switch is open, the transistor is unaffected and no interrupt occurs. The switch setting scan routine occurs after each X/Y matrix read routine. The switch settings can be read from the 8031's internal register anytime the Z-80 in the Electronics Base issues a query command.

Communication from the Z-80 in the Electronics Base to the 8031 in the Keyboard occurs as follows. The command to the Keyboard is received by the 8031's internal UART, the start and stop bits are stripped and the command is located in a table in the 8031. The starting address of the routine associated with that command is put on the address bus, and the 8031 executes code from the EPROM to satisfy the particular routine.

The six LEDs located on the Keyboard PCB are under the control of the Z-80 CPU in the Electronics Base. The Z-80 CPU sends LED data serially to the 8031 in the Keyboard. The 8031 strips the start and stop bits and converts the serial data to parallel data. The LED data is

2.2 KEYBOARD, continued

2.2.2 KEYBOARD THEORY OF OPERATION, continued

then placed on port zero lines P_0 - P_7 and latched in the tri-state LED latch. The 8031 enables the LED latch, thus driving the LEDs with the data from the Z-80 in the Electronics Base. Any low output from the LED latch will illuminate the associated LED.

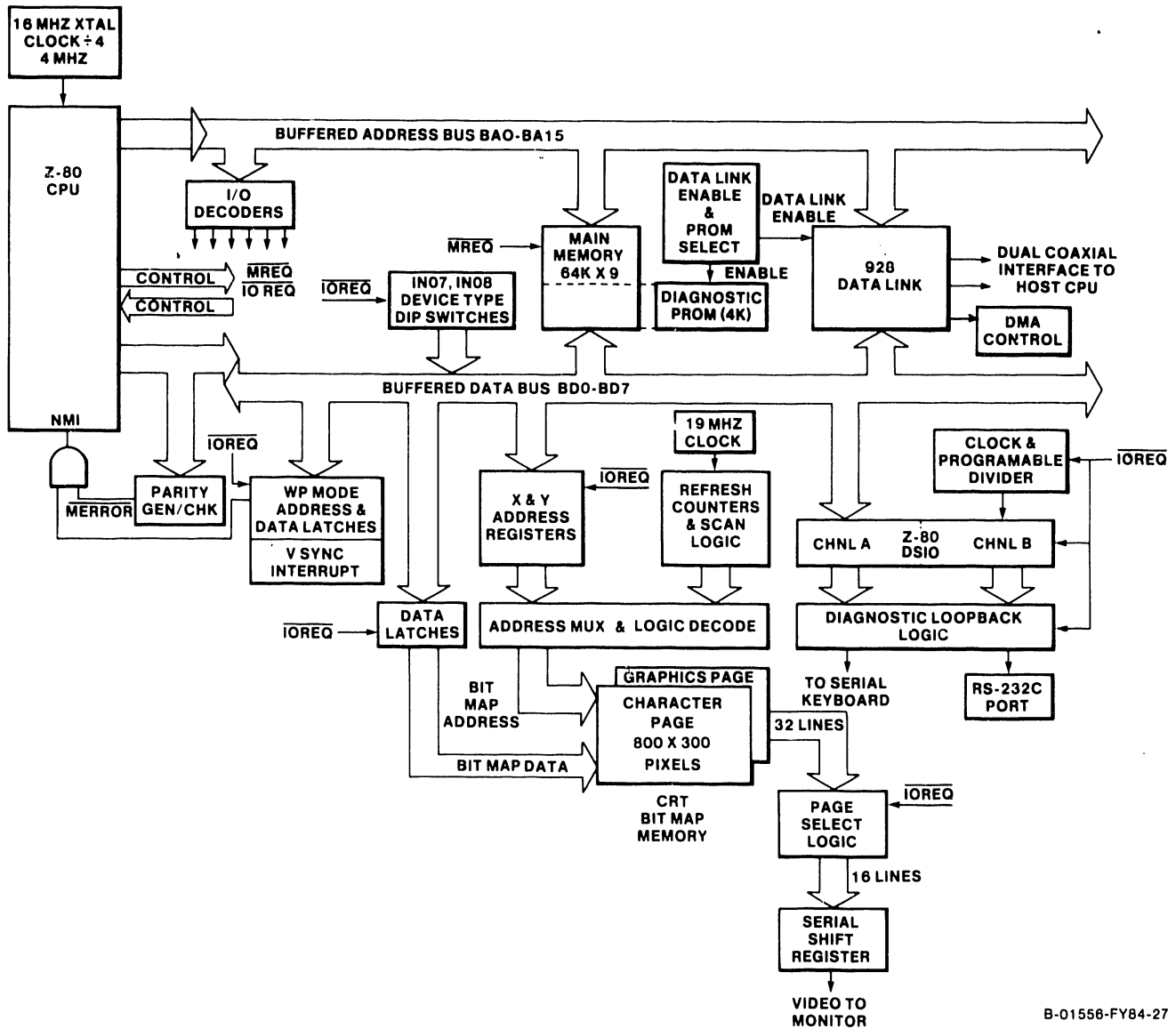
A programmable sound generator device provides the Keyboard with its beep and click sounds. Upon receipt of a beep or click command from the Z-80 in the Electronics Base, the associated routine is called from the EPROM. The 8031 receives the appropriate data for the sound generator from the EPROM. This includes the data required to load the sound generator's attenuation and frequency registers to produce the desired sound. The data is latched from the data bus and then applied to the sound generator. A common operational amplifier is used to drive the speaker.

2.3 4210 ELECTRONICS BASE

The 4210 Electronics Base houses two PCAs which carry out the main logic functions of the workstation. The two PCAs are the 210-8264 CPU PCA and the 210-8263 Bit Map PCA. Refer to Figure 2-4. Details of each of the functional blocks of the PCAs are given in the sections that follow.

2.3 4210 ELECTRONICS BASE, continued

2.3.1 210-8264 CPU PCA, continued



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Figure 2-4. 4210 Functional Block Diagram

2.3 4210 ELECTRONICS BASE, continued

2.3.1 210-8264 CPU PCA

The 8264 CPU PCA contains the Z-80 CPU, 64k bytes of main memory with parity, a standard Wang 928 serial data link and a 4k PROM containing the Built-In Test (BIT) power-up diagnostics. The connector header mounted on the rear of the PCA contains the DATA LINK BNC/TNC connectors for cable connections to the host CPU.

2.3.1.1 Z-80 Central Processor Unit (CPU)

Bus operations are controlled by the Z-80A CPU. The CPU receives sequential instructions from Main Memory over the data bus. It assigns device access and tasks based on these instructions and communicates with workstation logic through the data, address, and control buses.

CPU signals are sequenced according to both its internal instruction set and instructions received from main memory over the data bus. The CPU requires a single, +5 Vdc supply and employs a 4 MHz clock as its time base.

Bi-directional data flow is accomplished by an 8-bit, tri-state data bus. The CPU transmits address information through a 16-bit, tri-state address bus. A reset line initializes the CPU and the six control-output lines. The six control-output lines are:

M1, CPU Fetch Cycle: Active during the first (fetch) cycle of each instruction-request cycle, and during special interrupt cycles.

2.3.1 210-8264 CPU PCA, continued

2.3.1.1 Z-80 (CPU), continued

MREQ, Memory Request: Active when the CPU accesses memory to fetch either an instruction or data.

IORQ, Input/Output Request: Becomes active to indicate either an input or an output to a peripheral device during the interrupt-acknowledge cycles.

RD, Read: When active, indicates that the CPU will input data while performing a memory-access or I/O instruction.

WR, Write: When active, indicates that the CPU will output data while performing a memory-access or I/O instruction.

RFSH, Refresh: During an M1 (memory period 1) cycle, the CPU outputs an address for memory refresh. RFSH confirms the active presence of that address.

In addition to the control-output lines, there are three CPU input control lines. These lines are:

BUSRQ, Bus Request: Becomes active when an outside device requests bus access. BUSRQ input causes the CPU to switch its address, data, and status lines into a high-impedance state to accommodate the outside device.

2.3.1 210-8264 CPU PCA, continued

2.3.1.1 Z-80 (CPU), continued

BUSAK, Bus Acknowledge: Becomes active to indicate that the CPU has complied with a BUSRQ.

WAIT: Becomes active to request the CPU to extend the current memory access or I/O cycle as long as the WAIT is present.

2.3.1.2 CPU Interrupts

The workstation employs Z-80 interrupt mode 2. A mode 2 interrupt is the most powerful mode in the Z-80 CPU control set in that it allows for an indirect call to any location in memory. In this mode, the CPU forms a 16-bit memory address where the upper eight bits are the content of the interrupt page register (I register) in the CPU. The low order eight bits are supplied by the interrupting peripheral.

The address thus formed points to the first two bytes in a table where the address of the appropriate service routine is located. The CPU automatically obtains the starting address and performs a CALL to this address, thus servicing the peripheral. After the routine is complete, the contents of the program counter are retrieved from the stack and the program continues from where it left off before the interrupt.

2.3.1 210-8264 CPU PCA, continued

2.3.1.2 CPU Interrupts, continued

A non-maskable interrupt (unconditional entrance to the program) is generated for the following conditions:

- o Parity error in main memory
- o OUT instruction in the range of '00' to '07'*
- o IN instruction in the range of '00' to '07'*
- o Vertical sync (VS), at periodic rate of 16.69 milliseconds*
- o Write to CRT memory called by WP workstation microcode*

* Only if in WP Mode, as defined by an OUT 09 with D0 = 1. WP Mode operation allows software such as Word Processing, which is based on character memory 'C000'-'FFFF,' to be executed in the bit-mapped graphics workstation. See section 2.3.2.2 for details.

2.3.1.3 Main Memory

Main memory consists of 64k bytes of dynamic RAM with one bit of parity for each byte of memory. Physically, memory is implemented with nine 64k x 1 bit devices.

Main RAM can be accessed by both the CPU and the Data Link. (The Data Link is a DMA path.) Row Address Select (RAS) and Column Address Select (CAS) logic is employed to address main memory. RAS and CAS lines enable 16-bit addresses to be processed in 8-bit, half-address form, permitting

2.3.1 210-8264 CPU PCA, continued

2.3.1.3 Main Memory, continued

16-bit main memory addresses to be written and read by the 8-bit Z-80 CPU. RAS/CAS logic transfers high and low-order address bits through the same device pins at different times.

RAS/CAS cycles are required whenever main memory is addressed. Main memory is addressed during these operations:

- o CPU instruction fetch/refresh cycle
- o CPU data read
- o CPU data write
- o DMA transfer

2.3.1.4 Main Memory Parity Checking

Memory parity logic is one of two parity generation/detection circuits. The other circuit is part of the Data Link. Memory parity logic generates and tests for even parity on all data transfers leaving or entering the CPU through the data bus. During a CPU write, each parity bit is calculated and stored in main memory.

The parity line is checked on each CPU read. If a Memory Parity Error is detected, the error is noted in the the CPU status register. Such an error is also indicated in this register during a CRT control memory write. The Data Link also tests memory parity before generating its own line parity during a host CPU Read command.

2.3.1 210-8264 CPU PCA, continued

2.3.1.4 Main Memory Parity Checking, continued

A detected memory parity error immediately freezes the CRT display and selects the diagnostic PROM. The LOCK LED on the Keyboard blinks to indicate memory parity error to the user. This condition can be cleared only through a Z-80A RESET. In the 4210, a RESET can only be accomplished by cycling ac power to the workstation.

Following workstation restart, the diagnostic built-in test (BIT) runs and the usual power-up checks ensue. If the memory parity error was a soft error, the workstation will pass the BIT and be ready for operation again. Parity detection circuitry is also tested, by forcing bad parity to be written and then reading back the same data location.

2.3.1.5 Programmable Read-Only Memory (PROM)

At power-up, the bottom 4k bytes of main memory are masked by the diagnostic PROM through the action of the data link enable and PROM select logic. Sequential testing of different groups of logic is performed to verify the integrity of the terminal. During this phase, the data link is disabled. Upon successful completion of the tests, PROM is deselected and the data link is enabled. At this point, conventional data link downloading commences as though the terminal had just been powered-up.

2.3.1 210-8264 CPU PCA, continued

2.3.1.6 Data Link

The Data Link permits workstation memory to be loaded or read by the master. The host CPU can write new memory instructions into workstation memory; it can also record (archive) information entered by the workstation onto a common disk. The workstation CPU is disabled when the host CPU uses the Data Link. During this time, Direct Memory Access (DMA) logic, rather than the CPU, synchronizes memory read/write operations. DMA logic does not support CRT memory transfers.

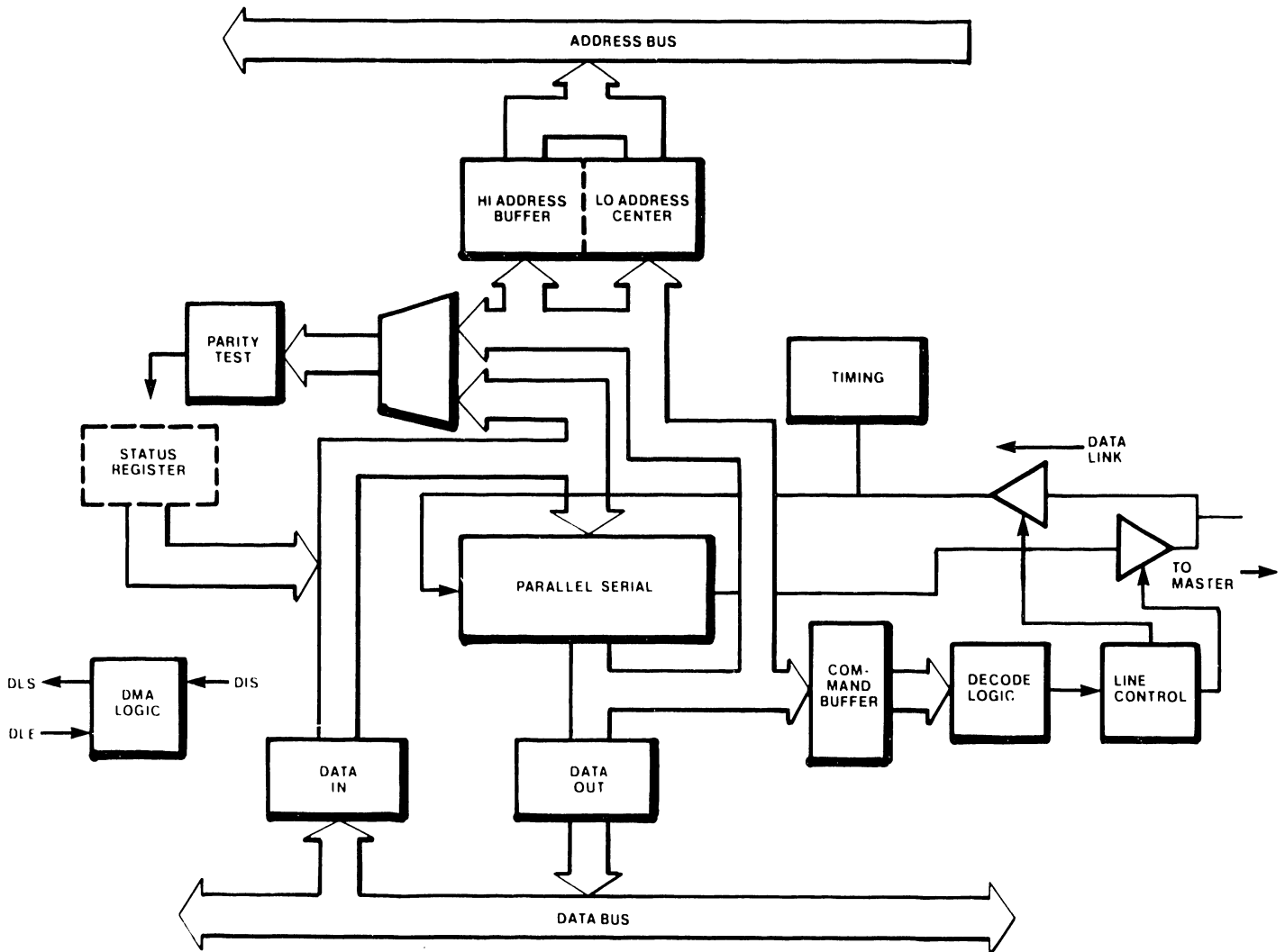
The data link (Figure 2-5) permits the host CPU to transfer data at high speed between its main memory (or disk) and main memory in its peripheral subsystems. In particular, the host CPU uses this link to load programs into workstations, store documents produced at workstations, and to feed high-speed printers.

Each workstation is connected to the host CPU separately, through a radial bus structure. All transmissions are controlled by the host CPU.

Data is transferred directly between memories using DMA logic. Data transfer is carried out in a serial, asynchronous, byte-oriented format using a half-duplex line. The transmission line itself is a balanced pair of coaxial cables operating at 4M baud. The actual data transfer rate is approximately 260k bytes per second.

2.3.1 210-8264 CPU PCA, continued

2.3.1.6 Data Link, continued



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Figure 2-5. Data Link Block Diagram

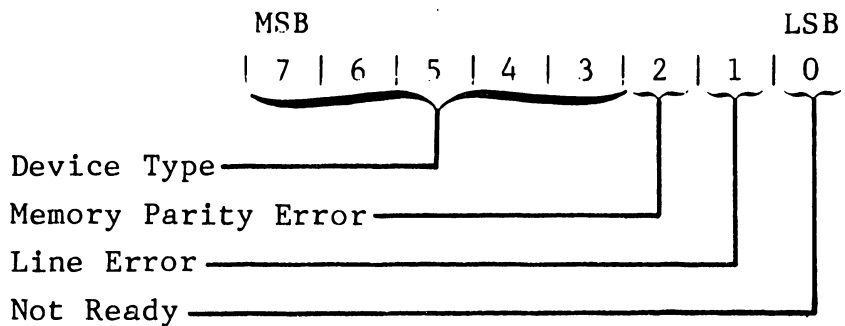
2.3.1.6 Data Link, continued

2.3.1.6.1 Data Link Commands

Six Data Link commands permit the host CPU to:

- o Check Slave STATUS and ID
- o Initiate Slave Operation (RESTART)
- o Load Slave Memory (WRITE - 2 commands)
- o Store Slave Data (READ - 2 commands)

STATUS and ID commands send Slave status and ID to the host CPU on command. The STATUS read is the method a host CPU uses to interrogate a slave. Eight bits of information are transmitted from the slave as shown below:



These are further defined below:

Not Ready: a high level indicates to the host CPU that the slave is not running.

Line Error: a high level indicates to the host CPU that the slave has detected a parity error during a transmission from the host CPU to the slave.

2.3.1.6 Data Link, continued

2.3.1.6.1 Data Link Commands, continued

Main Parity Error: a high level indicates the slave has detected a parity error in its own memory. In on-line applications, this bit would not be seen because the data link would be disabled and the boot (diagnostic) PROM would be enabled through NMI.

Device Type: defines the type of slave on the data link by reading device type DIP switches.

Further Data Link commands include:

RESTART commands reset the Slave CPU on command from the host CPU.

WRITE and READ commands may each transfer either 1 byte or 256 bytes. A one-byte command transfers a single DMA cycle. A 256-byte command transfers a single page of data.

WRITE DATA (1 byte) commands the Slave to receive data (one DMA cycle) from the host CPU on command.

WRITE BYTE (256 bytes) commands the Slave to receive data (one page) from the host CPU on command.

READ DATA (1 byte) commands the Slave to send data (one DMA cycle) to the host CPU on command.

READ BYTE (256 bytes) commands the Slave to send data (one page) to the host CPU on command.

2.3.1.6 Data Link, continued

2.3.1.6.2 Data Path Logic Function, continued

The data path defines the path by which information bytes are transferred between the serial data link and the data bus, address bus, command register, or status register.

The workstation portion of the data link normally monitors the serial, half-duplex transmission line. The first "1" detected by the differential line receiver causes a timing circuit to count out the eleven-bit intervals needed for a byte transfer. When the last bit of the serial/parallel shift register has been loaded, line parity is tested, the first byte of information is loaded into a command register, and, in some cases, a DMA bus request is initiated. Since stray line noise may start the timing circuits, three bits in the first byte are checked for a special header character. The remaining bits can be decoded to indicate a command if and only if the header is correct.

After the first byte has been transmitted, data link operation depends on the decoded command. A Data Transfer command (Read or Write) loads the next two bytes into the high and low address registers, respectively. The low address register is a counter that increments the DMA byte address following each transfer. A 256-byte transfer command ends when the address counter overflows. For Write operations, a data byte(s) immediately follows the low half of the address.

2.3.1.6 Data Link, continued

2.3.1.6.2 Data Path Logic Function, continued

For Read operations, line-control logic must reverse the half-duplex line before data can be sent to the host CPU. An 8 microsecond delay provides time for the line to quiet before data is transmitted.

Non-data commands (Status and Restart) do not transfer an address. Restart generates a 1.8 microsecond reset pulse to the workstation CPU. Status causes a Data Link Status Word to be transmitted to the host CPU after a line reversal. The host CPU monitors each command during its execution and clears the Data Link when the command has been completed.

2.3.1.6.3 Timing Logic Function

Timing is normally enabled to receive data. Timing logic recognizes the start bit preceding each byte and determines when the entire byte has been received. It also provides bit timing when information is transmitted to the host CPU. During Read and Status commands, timing logic clears timing during line reversal and maintains continuous timing while transmitting.

2.3.1.6.4 Line Control

Line control ensures that the Data Link is ready to receive command inputs from the host CPU when the Data Link is not in use, determines that the line is quiet before reversing the half-duplex

2.3.1.6 Data Link, continued

2.3.1.6.4 Line Control, continued

line, generates and checks line parity on each byte and clears the Data Link both after each command and in the event of a line failure. Line Control logic interlocks the Data Line Drivers and Receivers to ensure that the Workstation does not transmit into itself. Line Drivers are disabled until they are required to transmit data or status to the host CPU during a specific command.

2.3.1.6.5 Command Decode Logic Function

This function decodes and validates commands from the host CPU after a valid command (three-bit header) has been recognized.

2.3.1.6.6 Bus Requests and DMA Operation

Bus Requests are generated by the Data Link when a non-processor device requires direct memory access (DMA) for a data transfer. DMA transfers typically move blocks of data between main memory and mass storage devices. DMA operations have a higher priority than CPU operations due to real-time requirements.

Before a DMA device can use the bus it must gain control of the bus from the CPU. The CPU permits it to do so by recognizing the presence of a Bus Request and disabling its own bus inputs and outputs as soon as its current machine cycle has been completed. The CPU indicates when the cycle

2.3.1.6 Data Link, continued

2.3.1.6.6 Bus Requests/DMA Operation, continued

is complete by asserting Bus Acknowledge. The DMA device now has control of the bus for as long as Bus Request remains asserted.

Since CPU bus-control logic is not available to supply data transfer timing or to initiate refresh cycles during a DMA operation, separate DMA bus timing must be provided by the DMA device. This occurs automatically by applying low order address bits during RAS cycles. During a 256-byte transfer, all memory locations get refreshed by the byte counter.

DMA Enables permit selected devices to place DMA addresses and data onto the system bus. DMA Enables also ensure that only the selected device is allowed to control the main memory write control lines.

2.3.1.7 I/O Decoders

The Z-80 uses IN and OUT instructions to transfer data to and from input/ output devices. These instructions, combined with the assertion of IOREQ, distinguish memory addresses from the addresses of I/O ports. The Z-80 design allows for 256 discrete I/O ports to be assigned using the eight least significant bits of the address bus (A0 - A7). The I/O decoders decode these address lines to provide single chip enable lines for each I/O address. The I/O port assignments for the 4210 workstation are shown in Table 2-2.

2.3.2 210-8263 BIT MAP PCA

The 8263 Bit Map PCA contains the Z-80 dual serial input/output (DSIO) device, which, in the 4210 is configured as a dual asynchronous receiver/ transmitter (DART). One of the DSIO ports is used to interface CPU communications in parallel format with the serial format required for the Keyboard. The second port of the DSIO is reserved for future support of the RS-232C connector provided on the connector header at the rear edge of this PCA.

Also included on the 8263 Bit Map PCA are two planes or pages of screen memory, each arranged in a 16k x 16-bit format for a total of 32k bytes per page. The screen memory addressing logic, the CRT controller logic and other support logic are also on this PCA. At the rear of the PCA, a metal connector header carries an RS-232C connector and DIN connectors for the Keyboard and Monitor cables. This PCA interconnects with the CPU PCA via a 50-conductor ribbon cable.

2.3.2.1 CRT Screen Memory

The CRT screen (video refresh) memory comprises two 32K-byte pages of I/O mapped memory, where each bit of each byte is a pixel displayed on the screen. In the 4210, LSB is displayed first. The bytes are addressed on the screen as a matrix or an array of 100 bytes in the horizontal direction and 300 lines in the vertical direction. A format of 800 pixels horizontal and

2.3.2 210-8263 BIT MAP PCA, continued

2.3.2.1 CRT Screen Memory, continued

300 pixels vertical is thus implemented in the 4210, placing this system in the medium resolution range of graphics workstations.

The X and Y address registers specify the byte address that is written to with data from the data latches. These address registers have the added feature of enabling/disabling auto-incrementing/decrementing X and/or Y addresses.

The CRT bit map memory data is latched off the data bus by the data latches. This data determines whether the particular pixels in a byte, addressed by the address logic, will be on or off. The refresh counters and scan logic provide refresh timing for the two 32k-byte pages of DRAM CRT bit map memory. A 19 Mhz clock provides the timing base for this circuit. The address multiplexer and logic decode circuitry differentiates the addresses for the graphics page of memory and the character page of memory.

A 16 line bus transfers data from each of the two pages of CRT bit map memory, providing both pages of data to the page select logic. The page select logic allows any combination of data to be forwarded to the serial shift register for serialization. This could be either one of the pages separately, both or neither. The serial shift register serializes the data for use by the video monitor.

2.3.2 210-8263 BIT MAP PCA, continued

2.3.2.1 CRT Screen Memory, continued

An interrupt at the beginning of vertical retrace allows implementation of a blinking cursor by software. Note that only one level of video is displayed and that the attribute memory used in many Wang workstations is not found in the 4210. Split cycle memory access allows for flicker-free display when updating screen.

2.3.2.2 WP Mode Operation

To run word processing, a character-based code, on the bit-mapped workstation, a scheme called WP Mode is used. When enabled, WP Mode causes operations such as writing to screen memory, or reads and writes to the parallel keyboard to be captured and an NMI generated. The VS code decides which operation the WP code was trying to perform and emulates it on the bit-mapped screen or serial keyboard.

For example, the WP code encounters an OUT 00 (Sound Keyboard Clicker) and executes it. With WP Mode interrupts enabled (OUT 09 data = 01), an NMI is generated causing the Z-80 to jump to location '0066'. At the same time, the contents of the address and data bus, and a bit indicating that an OUT in the range of 00-07 was executed, are latched. At location '0066' a routine exists in the VS code to perform the following tasks:

- o Read WP Mode Status Latch: IN-09 data = 02 indicates that an OUT in the range of 00-07 was executed.

2.3.2 210-8263 BIT MAP PCA, continued

2.3.2.2 WP Mode Operation, continued

- o Read Low Address Byte: IN 0A data = 00 indicates the operation was an OUT 00.

- o Emulate clicker OUT 00 by sending the appropriate command to the serial keyboard to generate a click with its sound generator.

- o Return to WP Code.

A similar procedure is used when WP code writes to screen memory. By sampling the status, address and data latches, the NMI routine can write the appropriate character to the screen in bit map memory and again return to WP code at the end of the operation.

When in WP Mode, writes to main memory above 'C000' are inhibited. This gives the NMI routine the ability to read the location and decide if the character already exists there. If it does (which is often the case), time is saved by not having to duplicate the character in bit mapped memory. Thus, the serial keyboard and bit mapped memory remain transparent to the WP code.

An OUT 0D will reset the WP Mode Interrupt Latch, and it is issued just prior to Enable WP Mode OUT 09 (D0 = 1).

2.3.2 210-8263 BIT MAP PCA, continued

2.3.2.3 Dual Serial Input/Output (DSIO) Device

The Z-80 DSIO serves the function of serial-to-parallel, parallel-to-serial conversion and is optimized through software to carry out communication with the serial detached Keyboard. This function is carried out by channel A of the two channel device, and channel A is assigned priority over channel B. Channel B supports the RS-232C connector found on the rear of this PCA.

The Z-80 DSIO shares the Z-80 8-bit data bus from which it receives both data and commands. Data from the DSIO is also transferred on the data bus. The C/D line state determines whether the data on the bus at any instant is data (C/D low) or a command (C/D high). The data or command is routed to the appropriate channel by the B/A select line (low = channel A, high = channel B).

The following signals are exercised by the Z-80 to control the DSIO functions:

- o CE, Chip Enable: A low at this input enables the DSIO to accept command or data inputs from the CPU during a write cycle, or to transmit data to the CPU during a read cycle.

- o M1, Machine Cycle 1: When M1 is active (low) and RD is also active (low), the Z-80 is fetching an instruction from memory. When M1 is active while IORQ is active, the DSIO recognizes this as an interrupt acknowledge.

2.3.2 210-8263 BIT MAP PCA, continued

2.3.2.3 DSIO, continued

- o IORQ, Input/Output Request: This signal is used with B/A, C/D, CE and RD to transfer commands and data between the Z-80 CPU and the DSIO. When CE, RD and IORQ are all active, the channel selected by B/A transfers data to the CPU (a read operation). When CE and IORQ are active but RD is not active, the channel selected by B/A is written to by the CPU with either data or control information as specified by C/D.

- o RD, Read Cycle Status: An active state on this line indicates a memory or I/O read operation is in progress. RD is used with B/A, CE and IORQ to transfer data from the DSIO to the CPU.

- o INT, Interrupt Request: This line is pulled low when the DSIO is requesting an interrupt.

A clock and programmable divider provide the time base for the DSIO, and is used to derive the selected baud rate as described in the following section. Loopback logic is provided to allow for diagnostic testing of the DSIO without an external loopback being required.

2.3.2 210-8263 BIT MAP PCA, continued

2.3.2.4 Telecommunications

Channel B of the Z-80 DSIO supports the RS-232C I/O port on the rear of this PCA. Inputs and outputs to/from the port are listed below:

INPUTS

Receive Data (RXDB)
 Clear to Send (CTSB)
 Carrier Detect (DCDB)
 Receive/Transmit Clock (RXTXCB)
 (Ring Indicator [RIB] input not active)

OUTPUTS

Transmit Data (TXDB)
 Data Terminal Ready (DTRB)
 Request to Send (RTSB)

The interrupt line to the Z-80 is shared with the Keyboard (channel A) which has the higher priority. Baud rates for the transmit/receive clock are selected by OUT 3C with D0-D2 and the DSIO X16 or X64 clock modes. Table 2-2 is the baud rate table for the DSIO.

Table 2-2. 4210 Baud Rate Table

BAUD	OUT 3C D=	DSIO CLOCK MODE
75	7	X64
150	6	X64
300	5	X64
600	4	X64
1200	3	X64
2400	2	X64
4800	1	X64
9600	0	X64
19200	2	X16

2.3 4210 ELECTRONICS BASE, continued

2.3.3 SUMMARY OF IN/OUT COMMANDS

The IN/OUT commands of the 4210 Workstation are summarized in Table 2-3.

Table 2-3. Summary of 4210 IN/OUT Commands

COMMAND	DESCRIPTION
IN07	Primary switchbank defining slave device type
IN08	Secondary switchbank defining slave device type
IN09	Read WP Mode Interrupt Status Register BD0=1, Mem Write occurred to CRT MEM (C000-FFFF) BD1=1, an OUT in the range of 00-07 occurred BD2=1, an IN in the range of 00-07 occurred BD3=1, VS is latched (16 ms)
IN0A	Read Low Address Byte (WP Mode)*
IN0B	Read High Address Byte (WP Mode)*
IN0C	Read Data Bus Register (WP Mode)*
IN28	Read a byte from bit mapped memory at location pointed to by the X and Y and page select registers
IN38	Read DSIO channel A data
IN39	Read DSIO channel B data
IN3A	Read DSIO channel A control registers
IN3B	Read DSIO channel B control registers
OUT 09	BD0=0, Disable WP Mode Interrupts BD0=1, Enable WP Mode Interrupts
OUT 0D	Clear WP Mode Interrupts
OUT OE**	BD0=0, Set memory write to correct parity BD0=1, Set all memory writes to the wrong parity BD1=0, Ensures that the data link will remain enabled and that the diagnostic PROM will remain disabled when a parity error in main memory occurs. BD1=1, A Main Memory parity error will cause the Data Link to be disabled and the diagnostic PROM will be enabled.

2.3 4210 ELECTRONICS BASE, continued

2.3.3 SUMMARY OF IN/OUT COMMANDS, continued

Table 2-3. 4210 IN/OUT Commands, con't.

COMMAND	DESCRIPTION
OUT OE**	(continued)
	BD2=0, Disable Horizontal Sync Interrupt
	BD2=1, Enable Horizontal Sync Interrupt
	BD3=0, Disable X-Register Carry Interrupt
	BD3=1, Enable X-Register Carry Interrupt
	BD4=0, Disable Y-Register Carry Interrupt
	BD4=1, Enable Y-Register Carry Interrupt
	BD5, Unused
	BD6=0, Set PROM Select F/F
	BD6=1, Reset PROM Select F/F
	BD7=0, Reset Data Link Enable F/F
	BD7=1, Set Data Link Enable F/F
OUT 28	Write to bit map memory at location pointed to by X and Y registers.
OUT 29	Load X Register
OUT 2A	Load Y Register (High Byte)
OUT 2B	Load Y Register (Low Byte)
OUT 2C	X/Y Register Control: Each IN28 and OUT28 instruction provide clocking to the X and Y registers. BD0 = 0 Decrement X, D0=1 Increment X BD1 = 0 Decrement Y, D1=1 Increment Y BD2 = 0 Allow X register to count up/down BD2 = 1 Inhibit count of X register BD3 = 0 Allow Y register to count up/down BD3 = 1 Inhibit count of Y register
OUT 2D	BD0 = 0 Select Bank B for Reads and Writes BD0 = 1 Select Bank A for Reads and Writes
OUT 2F	BD1, BDO = 00 Blank Display 01 Display Bank A 10 Display Bank B 11 Display A & B

- 2.3 4210 ELECTRONICS BASE, continued
 2.3.3 SUMMARY OF IN/OUT COMMANDS, continued

Table 2-3. 4210 IN/OUT Commands, con't.

OUT 38	Write DSIO Channel A Data
OUT 39	Write DSIO Channel B Data
OUT 3A	Write DSIO Channel A Control Word
OUT 3F	Write DSIO Channel B Control Word
OUT 3C	BDO-BD2 = 0-7 Selects Baud Rate for RS-232C Port (See Table 2-1)
OUT 3F	BDO=0, Reset loopback F/F BDO=1, Set loopback F/F Loopback F/F provides an internal loopback connection for the serial keyboard and the RS-232C port. This is used by diagnostics.

* Latched at each WP Mode Interrupt

** Note: OUT OE also resets MPE (main memory parity error flip-flop).

2.4 4220 ELECTRONICS BASE

All circuitry for the 4220 Workstation logic functions is contained on a single PCA in the 4220 Electronics Base, the 210-8277 PCA. Figure 2-6 illustrates the architecture employed in the 4220 Workstation.

The 8277 PCA contains the Z-80 CPU, 64k bytes of main memory with parity, an 8k PROM containing the BIT power-up diagnostic and bootstrap micro-code, 4k of display RAM and 4k of font RAM. The display and font RAM is directly addressed by the CPU. A Motorola 6845 CRT controller (CRTC)

2.4 4220 ELECTRONICS BASE, continued

device is used to develop synchronization signals for the Monitor, as well as addressing the 4k of display RAM and 4k of font RAM.

The unit also uses a dual serial input/output (DSIO) device dedicated to telecommunications, while another DSIO services the Keyboard interface and the additional RS-232C port. Additional logic supports the Centronics-compatible printer interface port. The connector header mounted on the rear of the PCA contains connectors required for Keyboard, Monitor, printer and RS-232C connections.

2.4.1 Z-80 CENTRAL PROCESSOR UNIT (CPU)

Bus operations are controlled by the Z-80A CPU. The CPU receives sequential instructions from Main Memory over the data bus. It assigns device access and tasks based on these instructions and communicates with workstation logic through the data, address, and control buses.

CPU signals are sequenced according to both the CPU's internal instruction set and instructions received from main memory over the data bus. The CPU requires a single, +5 Vdc supply and employs a 4 MHz clock as its time base.

Bi-directional data flow is accomplished by an 8-bit, tri-state data bus. The CPU transmits address information through a 16-bit, tri-state address bus. A reset line initializes the CPU and the six control-output lines. The six control-output lines are:

2.4 4220 ELECTRONICS BASE, continued

2.4.1 Z-80 CPU, continued

- o M1, CPU Fetch Cycle: This line is active during the first cycle (fetch cycle) of each instruction-request cycle, and during the special interrupt cycles.
- o MREQ, Memory Request: Active when the CPU accesses memory to fetch either an instruction or data.
- o IORQ, Input/Output Request: Becomes active to indicate either an input or an output to a peripheral device during the interrupt-acknowledge cycles.
- o RD, Read: When active, indicates that the CPU will input data while performing a memory-access or I/O instruction.
- o WR, Write: When active, indicates that the CPU will output data while performing a memory-access or I/O instruction.
- o RFSH, Refresh: During an M1 (memory period 1) cycle, the CPU outputs an address for memory refresh. RFSH confirms the active presence of that address.

In addition to the control-output lines, there are three CPU input control lines:

2.4 4220 ELECTRONICS BASE, continued

2.4.1 Z-80 CPU, continued

- o BUSRQ, Bus Request: Becomes active when an outside device requests bus access. BUSRQ input causes the CPU to switch its address, data, and status lines into a high-impedance state to accommodate the outside device. In the 4220, no outside devices have access to the CPU data bus and this line is not used.
- o BUSRQ, Bus Request: Becomes active when an outside device requests bus access. BUSRQ input causes the CPU to switch its address, data, and status lines into a high-impedance state to accommodate the outside device. In the 4220, no outside devices have access to the CPU data bus and this line is not used.
- o BUSAK, Bus Acknowledge: Becomes active to indicate that the CPU has complied with a BUSRQ. As with BUSRQ, this line is not used in the 4220.
- o WAIT: Becomes active to request the CPU to extend the current memory access or I/O cycle as long as the WAIT is present.

2.4.2 CPU INTERRUPTS

The workstation employs Z-80 interrupt mode 2 for all interrupts except parity error. A mode 2 interrupt is the most powerful mode in the Z-80 CPU control set in that it allows for an indirect call to any location in memory. In this mode, the CPU forms a 16-bit memory address where the

2.4 4220 ELECTRONICS BASE, continued

2.4.2 CPU INTERRUPTS, continued

upper eight bits are the content of the interrupt page register (I register) in the CPU. The low order eight bits are supplied by the interrupting peripheral.

The address thus formed points to the first two bytes in a table where the address of the appropriate service routine is located. The CPU automatically obtains the starting address and performs a CALL to this address, thus servicing the peripheral. After the routine is complete, the contents of the program counter are retrieved from the stack and the program continues from where it left off before the interrupt.

The interrupt priority is shown in Table 2-4, with highest priority first. A non-maskable interrupt (unconditional entrance to the program) is generated only for a parity error in main memory.

Table 2-4 Interrupt Priority

1. Keyboard (auxiliary SIO channel A)
2. Auxiliary serial port (aux. SIO channel B)
3. Receive (SIO channel A)
4. Transmit (SIO channel B)
5. CTC Timer (channel 0)
6. CTC Timer (channel 1)
7. Printer acknowledge (CTC channel 2)
8. Video Logic (CTC channel 3)

2.4 4220 ELECTRONICS BASE, continued

2.4.3 MAIN MEMORY

Main memory consists of 64k bytes of dynamic RAM with one bit of parity for each byte of memory. Physically, memory is implemented with nine 64k x 1 bit devices.

Main RAM is accessed by the CPU by Row Address Select (RAS) and Column Address Select (CAS) logic. RAS and CAS lines enable 16-bit addresses to be processed in 8-bit, half-address form, permitting 16-bit main memory addresses to be written and read by the 8-bit Z-80 CPU. RAS/CAS logic transfers high and low-order address bits through the same device pins at different times. The RAS/CAS scheme is implemented by the DRAM controller logic.

RAS/CAS cycles are required any time main memory is addressed. Main memory is addressed during these operations:

- o CPU instruction fetch/refresh cycle
- o CPU data read
- o CPU data write

2.4.4 MAIN MEMORY PARITY CHECKING

Memory parity logic generates and then tests for even parity on all data transfers leaving or entering the CPU through the data bus. During a CPU write, each parity bit is calculated and stored in main memory.

2.4 4220 ELECTRONICS BASE, continued

2.4.4 MAIN MEMORY PARITY CHECKING, continued

The parity line is checked on each CPU read. If a Memory Parity Error is detected, a non-maskable interrupt is sent to the CPU and the error is noted in the CPU status register. A detected memory parity error immediately freezes the CRT display and generates all zeroes on the data bus. This condition is interpreted by the CPU as a string of continuous NOP instructions which disable the CPU while maintaining the necessary Memory Refresh cycles.

The CPU can escape from the disabling NOPs through a Z-80A RESET. Reset can be accomplished either by accessing diagnostic PROM or cycling ac power.

2.4.5 PROGRAMMABLE READ-ONLY MEMORY (PROM)

At power-up, the bottom 8k bytes of main memory (0000 to 1FFF) are masked by the PROM. Sequential testing of different groups of logic is performed to verify the integrity of the terminal. During this phase, the RS-232C telecommunications port is disabled and no communication with the host CPU can occur. Upon successful completion of the tests, bootstrap microcode is loaded from the PROM into workstation main memory, PROM is deselected and conventional downloading of workstation microcode from the host CPU can commence. PROM is automatically selected upon power-up, reset or main memory parity error. PROM can be deselected via bit 3 of I/O address '70' (see section 2.4.13).

2.4 4220 ELECTRONICS BASE, continued

2.4.6 CHIP SELECTS

Each of the major devices on the Remote Workstation Electronics PCA has a unique chip select line used to enable the device, under control of the Z-80 CPU. The select lines are decoded from low order address lines A0 through A7.

2.4.7 VIDEO DISPLAY

The video display logic provides the following features:

- o 80 character by 25 row, green on black display
- o 18.8 kHz horizontal scan rate
- o resolution 800 horizontal x 300 vertical (medium resolution)
- o TTL video input
- o recommended character 8x10 dots in a 10x12 character cell

The character font provides an 8-bit by 16-row memory for each character. The last two rows for each character are unused in the 10x12 character cell. The 8 bits of each row are centered in the 10 dots across the character cell, with the outer dots normally blanked. In character set graphics mode, these normally blanked outer dots are smeared outward to fill the entire character cell.

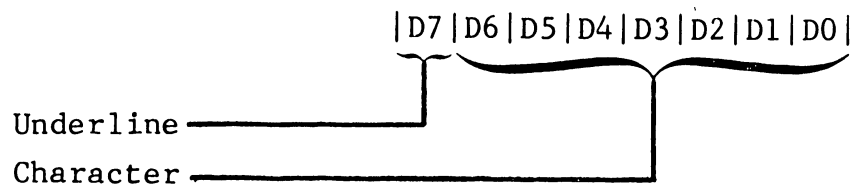
The display RAM indicates to the font RAM which characters are to be displayed on the screen and how they are to be displayed. Each character is defined by two bytes as follows:

2.4 4220 ELECTRONICS BASE, continued

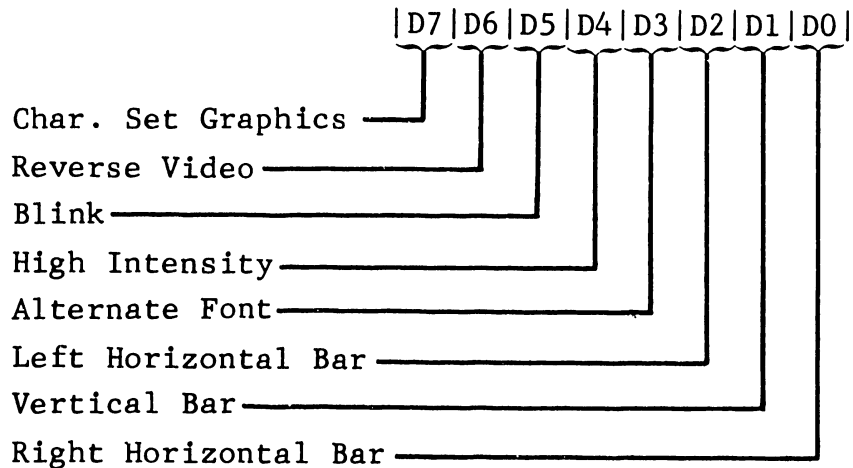
2.4.7 VIDEO DISPLAY, continued

Byte 1 (character):

The first byte indicates which character is to be displayed. During display, this is the most significant bit of the font memory address. The format of this byte is illustrated below.

Byte 2 (attributes):

The second byte defines the attributes of the character to be displayed. The format of this byte is shown below.



2.4 4220 ELECTRONICS BASE, continued

2.4.7 VIDEO DISPLAY, continued

Bit 7 enables character set graphics. This causes the 8-bit wide character to expand horizontally to fill the 10-bit wide character cell. Figure 2-7 illustrates the normal 8 x 12 area defined by the font and shows how columns 2 and 7 are expanded to the edges of the character cell with character set graphics.

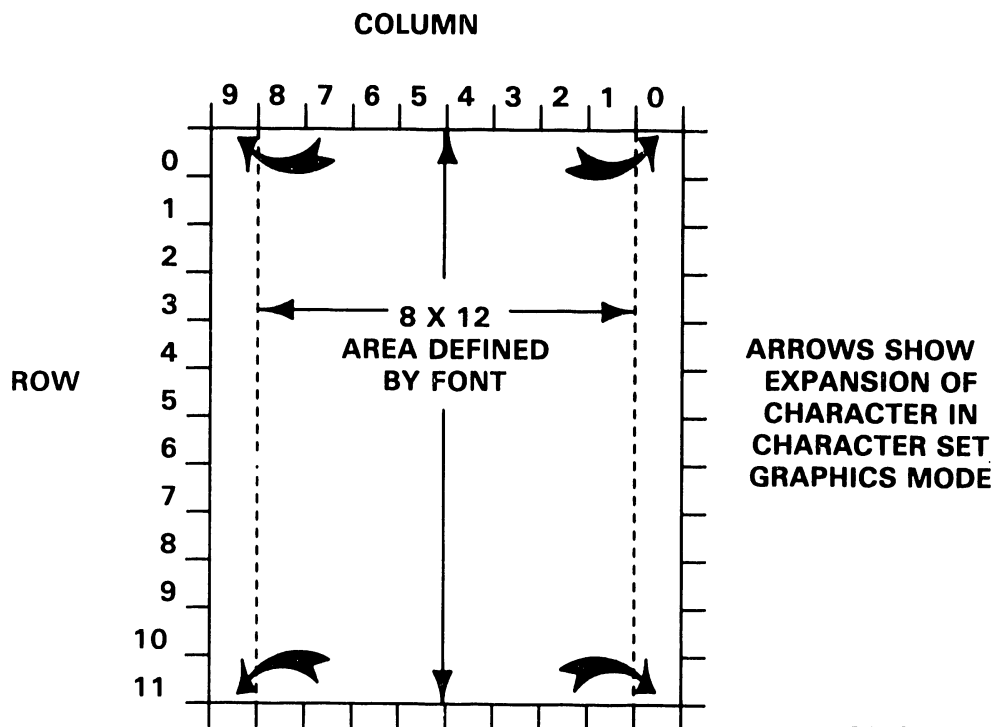
Continuing with byte 2, the attributes information, bit 6 enables reverse video for that character cell. Bit 5 when set causes that character to blink at a fixed rate of 32 times the field period. Bit 4 enables high intensity.

Bit 3, when set, enables the alternate font memory. The underline is programmed in this application to row 11.

Bits 0, 1 and 2 are used to enable the box graphics elements. Bit 2 enables the left horizontal bar, bit 1 the vertical bar, and bit 0 the right horizontal bar. These are implemented as illustrated in Figure 2-8.

2.4 4220 ELECTRONICS BASE, continued

2.4.7 VIDEO DISPLAY, continued



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Figure 2-7. 10 x 12 Character Cell

2.4 4220 ELECTRONICS BASE, continued

2.4.7 VIDEO DISPLAY, continued

The cursor is not shown in Figure 2-8. It is programmed to be a blinking solid line, filling rows 10 and 11. Two blink modes are available at 16 times or 32 times the field period. The cursor behaves as a high intensity field.

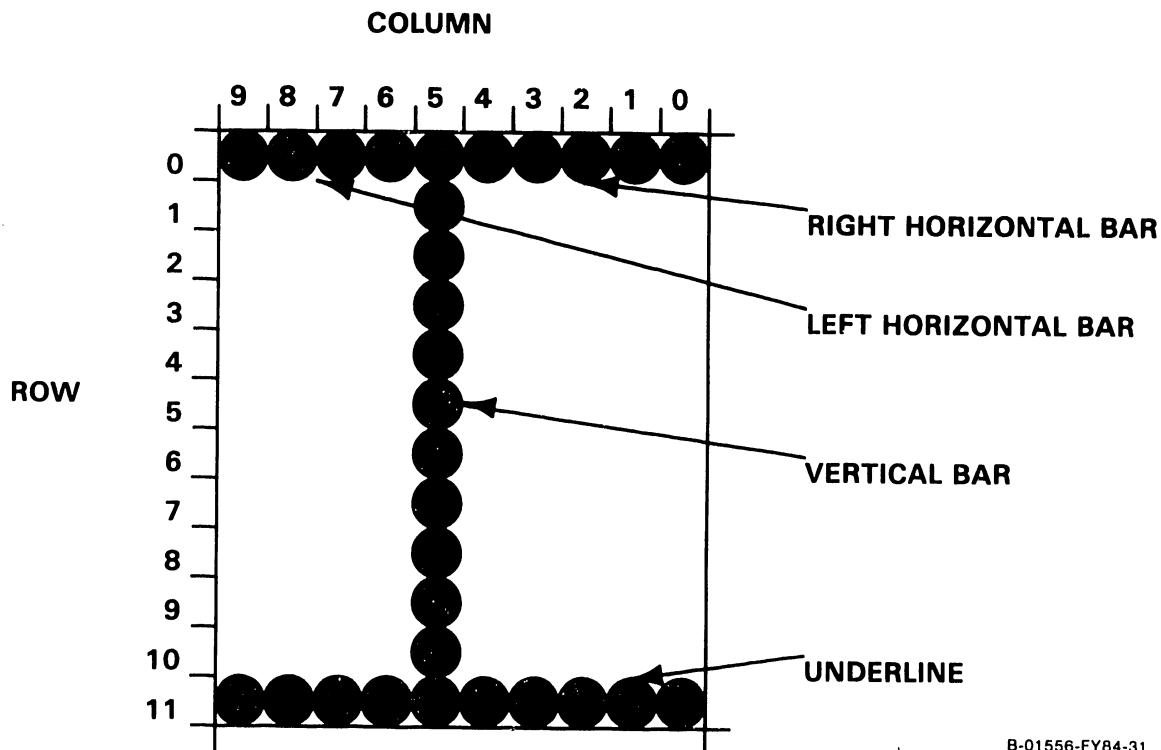


Figure 2-8. Box Graphics

2.4 4220 ELECTRONICS BASE, continued

2.4.8 CRTC OPERATION

The 6845 CRT Controller (CRTC) device provides HSYNC and VSYNC (horizontal and vertical) sync timing for the monitor using constants in special internal registers called initialization registers. The CRTC maintains 14-bit addresses for reading display and font RAM via the video bus. It also maintains cursor movements and blink rate information.

Table 2-5 summarizes the I/O addresses used by the Z-80 to access the video logic, including those which are internal to the CRTC. A more detailed functional description of each follows.

Table 2-5. Video Interface Registers

I/O ADDRESS (HEX)	DATA	FUNCTION
'30'	Points to a control register	Address Register
'31'	See Table 2-4	Initialization Register
'70'	See Section 2.4.13	Status Register

Selecting I/O address ('00') sets the video display mode. When this mode is set the processor has access to CRT memory, thus locking out the CRT. This function is cleared by selecting I/O address ('00') again.

2.4 4220 ELECTRONICS BASE, continued

2.4.8 CRTC OPERATION, continued

Display RAM is set by selecting I/O address ('10'). When this mode is set, display and font RAM are enabled. Selecting I/O address ('10') again clears this function and main memory is enabled.

Upon power-up, video display and display RAM default to clear (reset).

2.4.8.1 Initialization Registers

There are 18 initialization registers in the CRTC containing video parameters, all of which are accessed by writing to the same I/O address ('31'). The CRTC has an internal pointer which contains the address of one of the other 18 registers. This register is accessed by writing to I/O address ('30') where the data is the register desired. Table 2-6 is a list of initialization commands.

2.4.8.2 Display Control Registers

There are 14 address bits used to access display and font memory. The display memory is accessed using binary addresses, not row/column as in many Wang workstations. The Z-80 software is responsible for keeping track of where one row ends and the next begins when updating the display. The 14-bit display address space is assigned as shown in Table 2-7.

2.4.8 CRTC OPERATION, continued

2.4.8.2 Display Control Registers, continued

Bits D3 and D2 of status output register '70' are used in conjunction with display and font memory. (Refer to section 2.4.13 for more details on status register '70'.) An active display memory enable bit (D3) causes the top 8k of main memory to be masked by CRT memory. D3 is active any time CRT memory is read or written. An active hog mode bit (D2) blanks the CRT display and allows the CPU unlimited access to CRT memory.

Table 2-6. CRTC Initialization Registers

INITIALIZATION REGISTER	VALUE (HEX)	FUNCTION
IR0	'65'	Horizontal Total
IR1	'50'	Horizontal Displayed
IR2	'57'	Horizontal Sync Position
IR3	'4F'	Sync Width
IR4	'19'	Vertical Total
IR5	'04'	Vertical Total Adjust
IR6	'19'	Vertical Displayed
IR7	'19'	Vertical Sync Position
IR8	'10'	Interlace Mode & Skew Register
IR9	'0B'	Maximum Scan Line Address
IR10	'6A'	Cursor Start
IR11	'0B'	Cursor End
IR12	'**'	High Order Start Address
IR13	'**'	Low Order Start Address
IR14	'**'	High Order Cursor Address
IR15	'**'	Low Order Cursor Address
IR16	NA	High Order Light Pen Address
IR17	NA	Low Order Light Pen Address

**Programmable

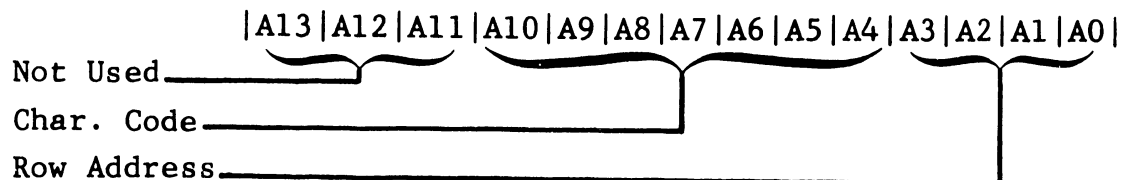
2.4.8 CRTC OPERATION, continued

2.4.8.2 Display Control Registers, continued

Table 2-7. Display Memory Address Assignments

FROM (HEX)	TO (HEX)	FUNCTION	BYTES
E000	E7FF	Character RAM	2K
E800	EFFF	Attribute RAM	2K
F000	F7FF	Font (1st)	2K
F800	FFFF	Font (2nd)	2K

When addressing the font memory, address bits are assigned as follows:



2.4.9 TELECOMMUNICATIONS

The main telecommunications (TC) interface for the workstation is handled by a dual serial input/output (DSIO) device. The addresses assigned to the DSIO are listed in Table 2-6.

The Z-80 DSIO shares the Z-80 8-bit data bus from which it receives both data and commands. Data from the DSIO is also transferred on the data bus. The state of the C/D line determines whether the data on the bus at any instant is data (C/D low) or a command (C/D high). The data or command is routed to the appropriate channel by the B/A select line (low = channel A, high = channel B).

2.4 4220 ELECTRONICS BASE, continued

2.4.9 TELECOMMUNICATIONS, continued

The following signals are exercised by the Z-80 to control the DSIO functions:

- o CE, Chip Enable: A low at this input enables the DSIO to accept command or data inputs from the CPU during a write cycle, or to transmit data to the CPU during a read cycle.
- o M1, Machine Cycle 1: When M1 is active (low) and RD is also active (low), the Z-80 is fetching an instruction from memory. When M1 is active while IORQ is active, the DSIO recognizes this as an interrupt acknowledge.
- o IORQ, Input/Output Request: This signal is used with B/A, C/D, CE and RD to transfer commands and data between the Z-80 CPU and the DSIO. When CE, RD and IORQ are all active, the channel selected by B/A transfers data to the CPU (a read operation). When CE and IORQ are active but RD is not active, the channel selected by B/A is written to by the CPU with either data or control information as specified by C/D.
- o RD, Read Cycle Status: An active state on this line indicates a memory or I/O read operation is in progress. RD is used with B/A, CE and IORQ to transfer data from the DSIO to the CPU.
- o INT, Interrupt Request: This line is pulled low when the DSIO is requesting an interrupt.

2.4 4220 ELECTRONICS BASE, continued

2.4.9 TELECOMMUNICATIONS, continued

The DSIO used for the main TC interface uses channel A for receive and channel B for transmit to allow full duplex operation. Channel A transmit and channel B receive pins are unused in this application but are tied together for diagnostic purposes. Diagnostic loopback logic is also provided to allow for thorough diagnostic testing without an external loopback being provided. Pin assignments for the DSIO are shown in Table 2-8.

Synchronous or asynchronous mode for the main TC interface is selected via jumper J11. Asynchronous mode is selected by shorting position 1 with 2. Synchronous mode is selected by shorting positions 2 with 3. While operating synchronously the clock is generated externally by an attached modem. When asynchronous mode is used the baud rate is selected via baud rate switch SW2. Refer to Table 2-8 for switch settings. Other capabilities include optional NRZI encoding/decoding of serial data. Control of this function is described more fully in section 2.4.13.

Table 2-7. Main DSIO Interface Addresses

I/O ADDRESS	READ/WRITE	FUNCTION
'40'	Read/Write	Channel A Data
'41'	Read/Write	Channel B Data
'42'	Read/Write	Channel A Control
'43'	Read/Write	Channel B Control

2.4 4220 ELECTRONICS BASE, continued

2.4.9 TELECOMMUNICATIONS, continued

Table 2-8. Main DSIO Pin Assignments

SIGNAL	INPUT/ OUTPUT	FUNCTION
TxCA	Input	9600 Baud Clock
RxCA	Input	Internal/External Receiver Clock
TxDA	Output	Looped Back to RxDB
RxDA	Input	Received Data from Modem
RTSA	Output	Not Used
DTRA	Output	Not Used
CTSA	Input	Ring Indicator from Modem
DCDA	Input	Carrier Detect from Modem
W/RDYA	Output	Not used
TxCB	Input	Internal/External Transmit Clock
RxCB	Input	9600 Baud Clock
TxDB	Output	Data Transmitted to Modem
RxDB	Input	Looped Back from TxDA
RTSB	Output	Request To Send to Modem
DTRB	Output	Data Terminal Ready to Modem
CTSB	Input	Clear To Send from Modem
DCDB	Input	Data Set Ready from Modem
W/RDYB	Output	Not Used

2.4 4220 ELECTRONICS BASE, continued

2.4.9 TELECOMMUNICATIONS, continued

Table 2-9. SW2 Baud Rate Selection

SWITCH SECTION			BAUD RATE
2	3	4	
0	0	0	External Clock
0	0	1	19,200
0	1	0	9,600
0	1	1	4,800
1	0	0	2,400
1	0	1	1,200
1	1	0	600
1	1	1	300

Note: 0 = OFF, 1 = ON

2.4.10 COUNTER/TIMER CIRCUIT (CTC)

The CTC device provides general purpose timing capability for the workstation software, as well as an input mechanism for interrupts from other functions. Using I/O addresses '50' through '53,' the clock/trigger inputs are tied to the following hardware interrupt functions: print acknowledge (channel 2), and vertical retrace (channel 3) (see Table 2-10). The zero count outputs are unconnected.

Table 2-10. CTC I/O Addresses

I/O ADDRESS	READ WRITE	FUNCTION
'52'	Write	CTC Chnl 2 (Print Acknowledge)
'53'	Write	CTC Chnl 3 (Vsync, Timer)

2.4 4220 ELECTRONICS BASE, continued

2.4.11 AUXILIARY DSIO

Table 2-11 gives the I/O addresses for the auxiliary DSIO while Table 2-12 indicates the connections to the second DSIO in the workstation. Channel A is dedicated to the serial keyboard interface. This asynchronous link operates at 62.5k baud and requires only receive and transmit data signals. The receive and transmit clocks are tied together and a 1 MHz clock is provided. To interface at the proper baud rate, channel A is operated in the X16 clock mode.

Channel B of the auxiliary DSIO provides for an additional TC interface. This RS-232C channel can be configured for either synchronous or asynchronous operation, with clock generated externally or internally, as selected by DIP switch SW1. Refer to Table 2-13 for switch settings.

Diagnostic loopback logic is provided to allow for thorough diagnostic testing without an external loopback being provided.

Table 2-11. Auxiliary DSIO I/O Addresses

I/O ADDRESS	READ/WRITE	FUNCTION
'60'	Read/Write	Channel A Data
'61'	Read/Write	Channel B Data
'62'	Read/Write	Channel A Control
'63'	Read/Write	Channel B Control

2.4 4220 ELECTRONICS BASE, continued

2.4.11 AUXILIARY DSIO, continued

Table 2-12. Auxiliary DSIO Pin Assignments

SIGNAL	INPUT/OUTPUT	FUNCTION
Channel A (Keyboard):		
TxCA	Input	1 MHz Clock (16 times 62.5 Kbaud)
RxCA	Input	1 MHz Clock
TxDA	Output	Keyboard Data Out
RxDA	Input	Keyboard Data In
RTSA	Output	Not used
DTRA	Output	Not used
CTSA	Input	Not used
DCDA	Input	Not used
W/RDYA	Output	Not used
Channel B (Auxiliary RS-232C Port):		
TxCB	Input	External/Internal Clock
RxCB	Input	Tied to TxCB
TxDB	Output	Data Transmitted
RxDB	Input	Received Data
RTSB	Output	Request To Send
DTRB	Output	Data Terminal Ready
CTSB	Input	Clear To Send
DCDB	Input	Data Set Ready
W/RDYB	Output	Not Used

2.4 4220 ELECTRONICS BASE, continued

2.4.11 AUXILIARY DSIO, continued

Table 2-13. SW1 Baud Rate Selection
(Auxiliary RS-232C Port)

SWITCH SECTION			BAUD RATE
3	2	1	
0	0	0	External Clock
0	0	1	19,200
0	1	0	9600
0	1	1	4800
1	0	0	2400
1	0	1	1200
1	1	0	600
1	1	1	300

Note: 0 = OFF, 1 = ON

2.4.12 PARALLEL PRINTER INTERFACE

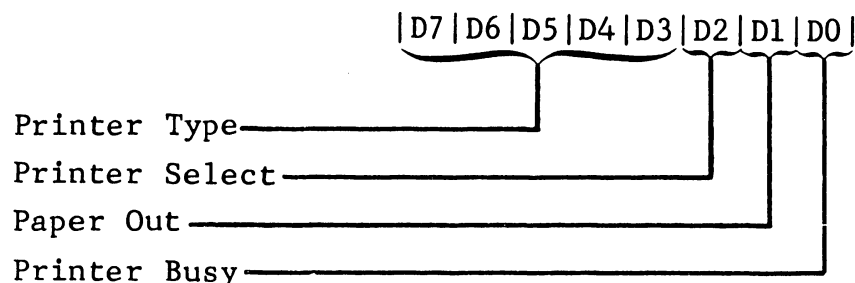
I/O addresses '71' and '72' are used for a parallel, Centronics-type interface. Data to be sent to the printer is written to address '72', whereupon the necessary printer strobe signal is generated and sent to the printer. The printer acknowledge signal returned by the printer is sent to CTC channel 2, and can be used to trigger an interrupt.

I/O address '71' is read to obtain various printer status flags: printer busy, paper out, and printer selected. Additional bits in this register read in the values from DIP switch SW2, sections 9-5 (D7-D3), which are used to define the type of printer connected to the port. The

2.4 4220 ELECTRONICS BASE, continued

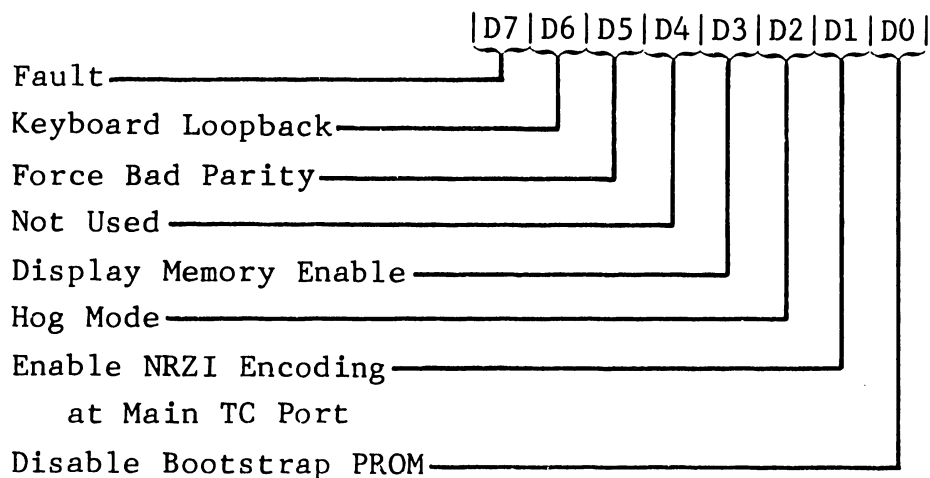
2.4.12 PARALLEL PRINTER INTERFACE, continued

printer status register ('71') flags are arranged as shown below.



2.4.13 OTHER HARDWARE FUNCTIONS

I/O addresses '70' and '73' are status registers dedicated to providing hardware functions not covered in the various LSI functions. These include the PROM enable/disable and TC functions such as NRZI encoding enable/disable. These output flags are set using the status output register (I/O address '70') which is organized as shown below. This register is cleared at power-up to enable the PROM.



2.4 4220 ELECTRONICS BASE, continued

2.4.13 OTHER HARDWARE FUNCTIONS, continued

The fault bit (D7) drives an on-board LED which acts as an indicator for the diagnostic code. When D7 is active the LED is off, indicating that the diagnostic was passed. A blinking LED indicates the diagnostic is running. When D7 is inactive the LED is on, indicating an error was found by the diagnostic.

The Keyboard loopback bit (D6) is inactive when a loopback is in effect and active when normal communication between the Keyboard and the CPU is in effect. An active force bad parity bit (D5) forces bad parity to be written to test the parity generation and checking circuits.

Bits D3 and D2 are used in conjunction with display and font memory. Refer to section 2.4.8.2 for broader coverage of this subject. An active display memory enable bit (D3) causes the top 8k of main memory to be masked by CRT memory. D3 is active any time CRT memory is read or written. An active hog mode bit (D2) blanks the CRT display and allows the CPU unlimited access to CRT memory.

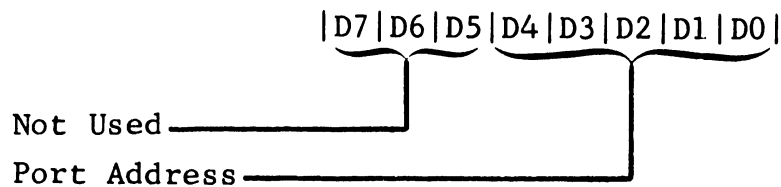
An active bit D1 enables NRZI coding at the main TC port of the work station. Bit D0 masks the lower 8k of main memory with the PROM.

The status input register (I/O address '73') is a read-only port, which brings in the settings of certain sections of on-board DIP switches SW1 and

2.4 4220 ELECTRONICS BASE, continued

2.4.13 OTHER HARDWARE FUNCTIONS, continued

SW2 to determine the port address of the workstation. These settings are hardware dedicated as shown below. D6-D0 corresponds to switch SW1 sections 10 to 4 respectively. D7 corresponds to switch S2 position 1.



2.4.14 SUMMARY OF 4220 I/O ADDRESSES

Table 2-14 summarizes I/O addresses.

Table 2-14. 4220 I/O Addresses

I/O ADDRESS	FUNCTION
'00'	Video Display Mode
'10'	Display RAM
'20'	Not Used
'30'	CRT Select
'40'	DSIO Select
'50'	CTC Select
'60'	Keyboard Select
'70'	Status Select

CHAPTER

3

OPERA-

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CHAPTER 3 OPERATION

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CHAPTER 3 OPERATION

This chapter provides information pertaining to the 4210/4220 Workstation operator controls and indicators, initial control settings, initial turn-on procedures, and normal and emergency shut-down procedures.

3.1 CONTROLS AND INDICATORS

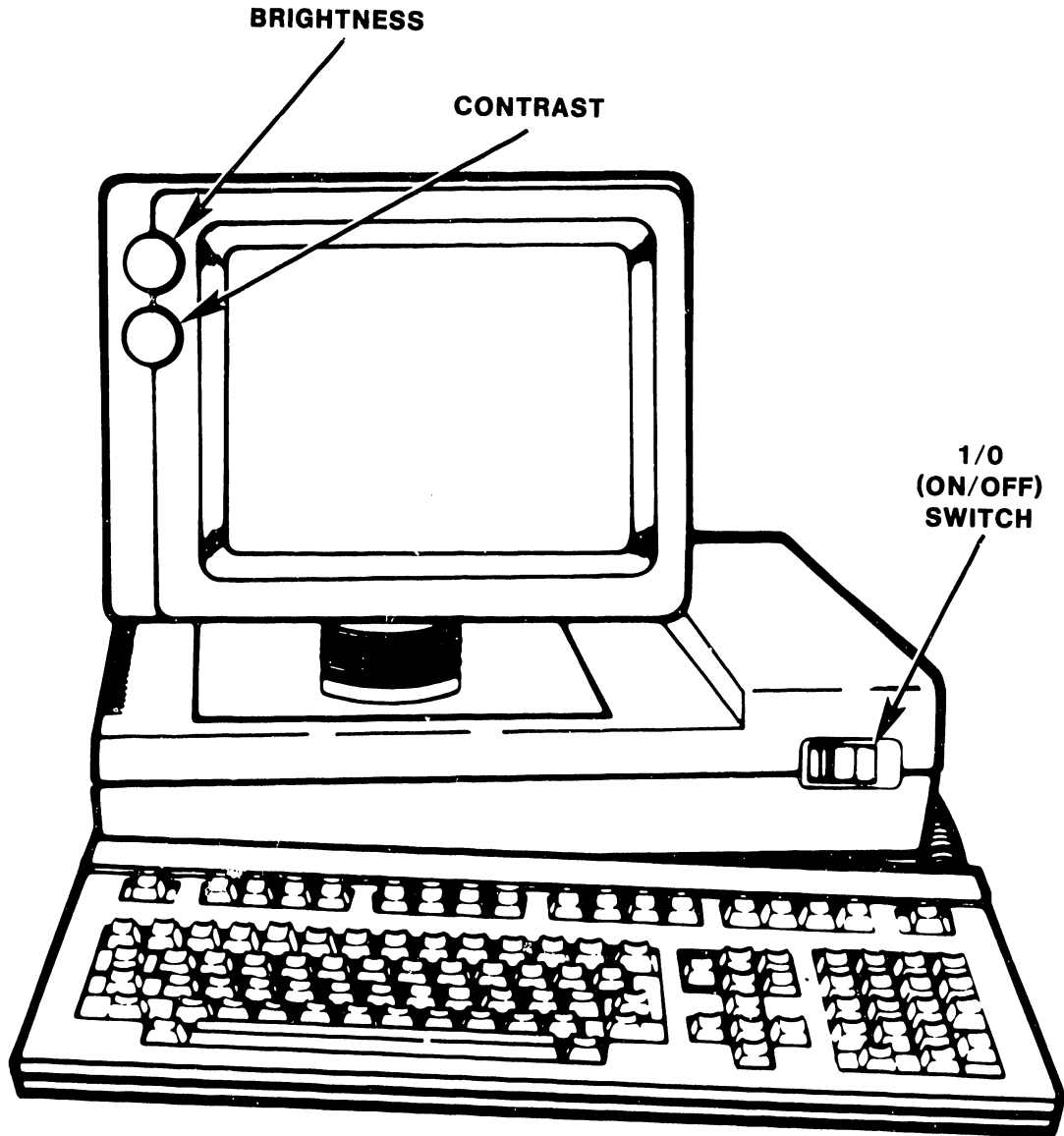
The controls and indicators of the 4210/4220 Workstation are shown in Figure 3-1 and discussed below. The Keyboard is discussed in section 3.2.

- o 1/0 (On/Off) Switch - Turns ac input power to the workstation on (1) or off (0).

- o Brightness Control - The Brightness control sets the brightness of all displayed characters, affecting normal and highlighted characters equally.

- o Contrast Control - The Contrast control does not affect the 4210 Workstation display. In the 4220 Workstation, Contrast controls the change in brightness between normal and highlighted characters.

3.1 CONTROLS AND INDICATORS, continued

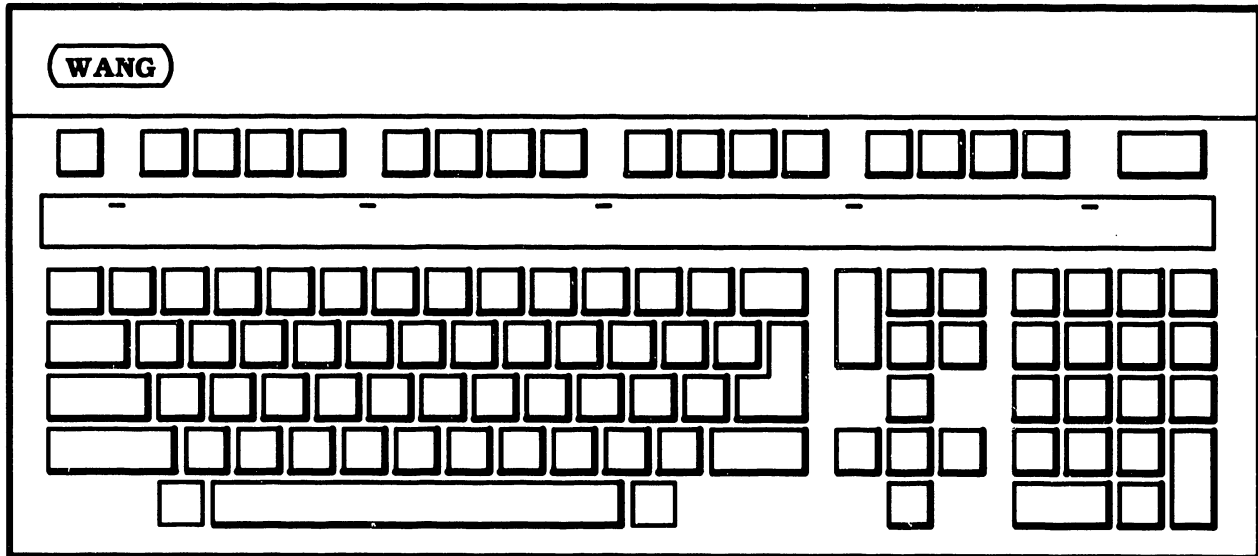


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Figure 3-1. Workstation Controls and Indicators

3.2 KEYBOARD

The workstation is equipped with the low profile, serial keyboard currently used in many other Wang products (Figure 3-2).



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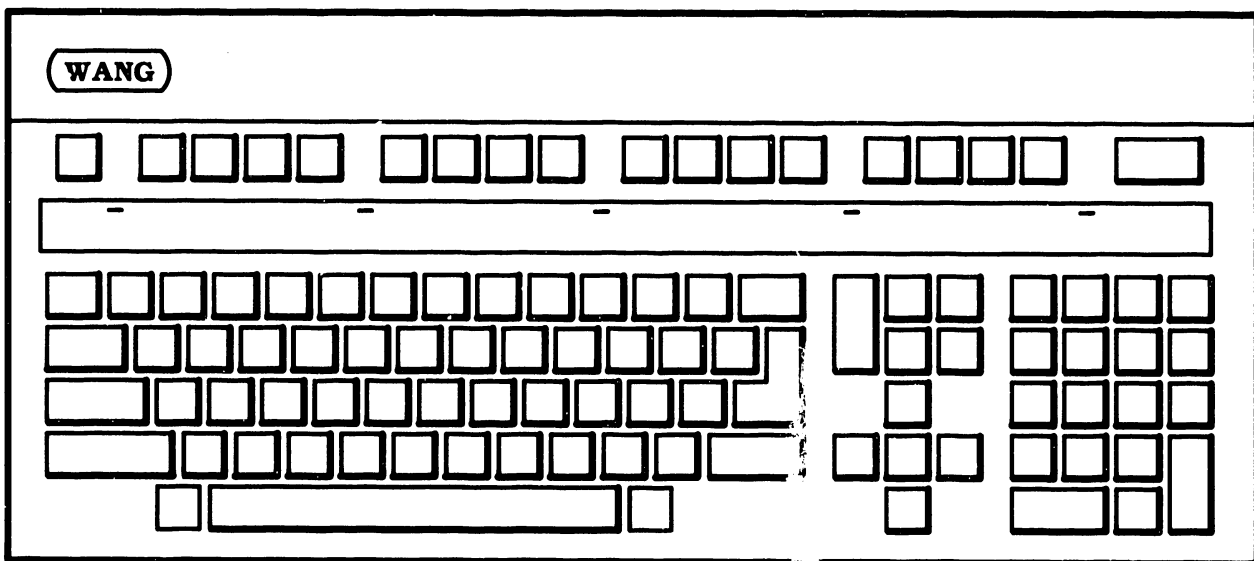
The Keyboard features the conventional typewriter format, cursor control and editing keys, and special function keys. The special function keys are those normally associated with Wang WP systems (INDENT, FORMAT, SRCH, COMMAND, etc.) and those normally associated with data processing systems (Program Function keys). The Keyboard is also equipped with a numeric keypad at the extreme right.

The following paragraphs describe the actions associated with each group of keys. For convenience, the keyboard has been divided into four zones as described below.

3.2 KEYBOARD, continued

Zone 1 - Typewriter Keyboard: Similar to a standard typewriter, this zone contains the alphanumeric characters, the special purpose characters such as @ # \$ % and the arithmetic operators (+ - * / =). Also included are the TAB, GL, RETURN and SHIFT keys which perform the following WP functions:

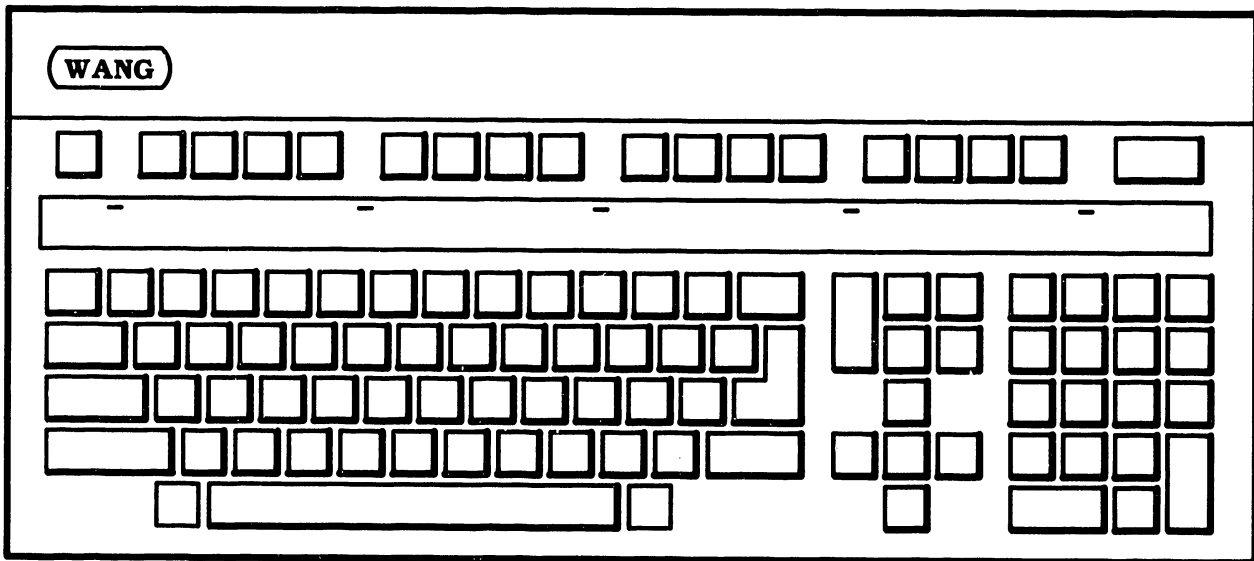
- o TAB sets the format line zone and advances the cursor through successive zones on the screen to facilitate table creation.
- o GL (glossary) is a useful function in Word Processing whereby repeatedly used text may be created once, stored on disk and retrieved again with two keystrokes, GL followed by the glossary number.
- o RETURN terminates the present text line and repositions the cursor at the beginning of the next line.



ZONE 1

3.2 KEYBOARD, continued

Zone 2 - Cursor Control and Editing Keys: This zone contains editing keys (INSERT and DELETE), location keys (NEXT SCRN and PREV SCRN), and cursor control keys which control movement of the cursor in the indicated direction, up, down, right, left and home (top left corner of screen).

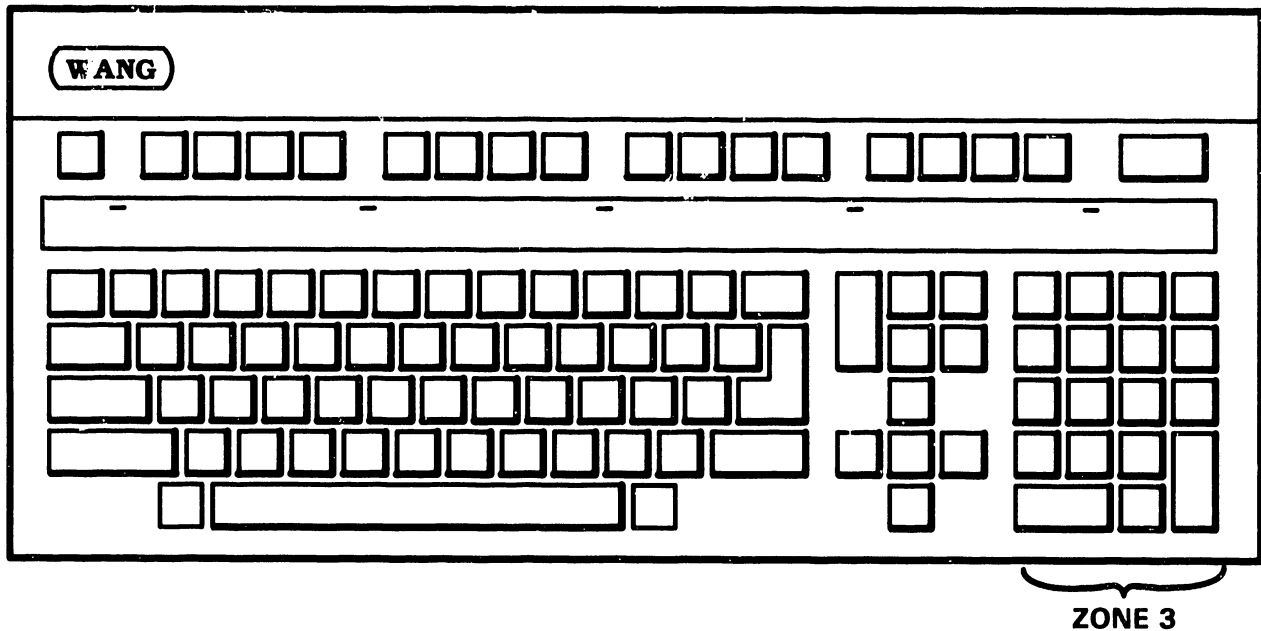


ZONE 2

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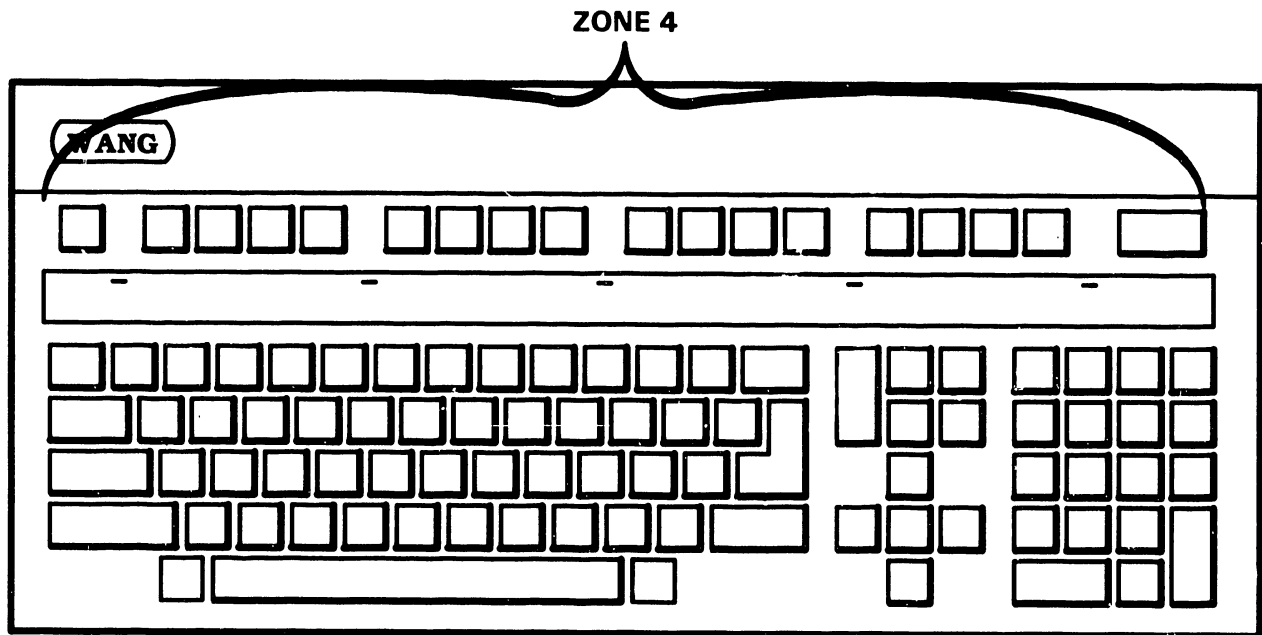
3.2 KEYBOARD, continued

Zone 3 - Numeric Keypad: The keys in the numeric zone allow rapid entry of numeric characters, grouped here for convenience. Digits can be entered by using the numeric keys in either the numeric or the alphanumeric zone. In addition to the standard ten numeric keys are arithmetic operator keys (+, -, x, divide-by) and PRINT, ERASE, RETURN and decimal point (.) keys used in data processing.



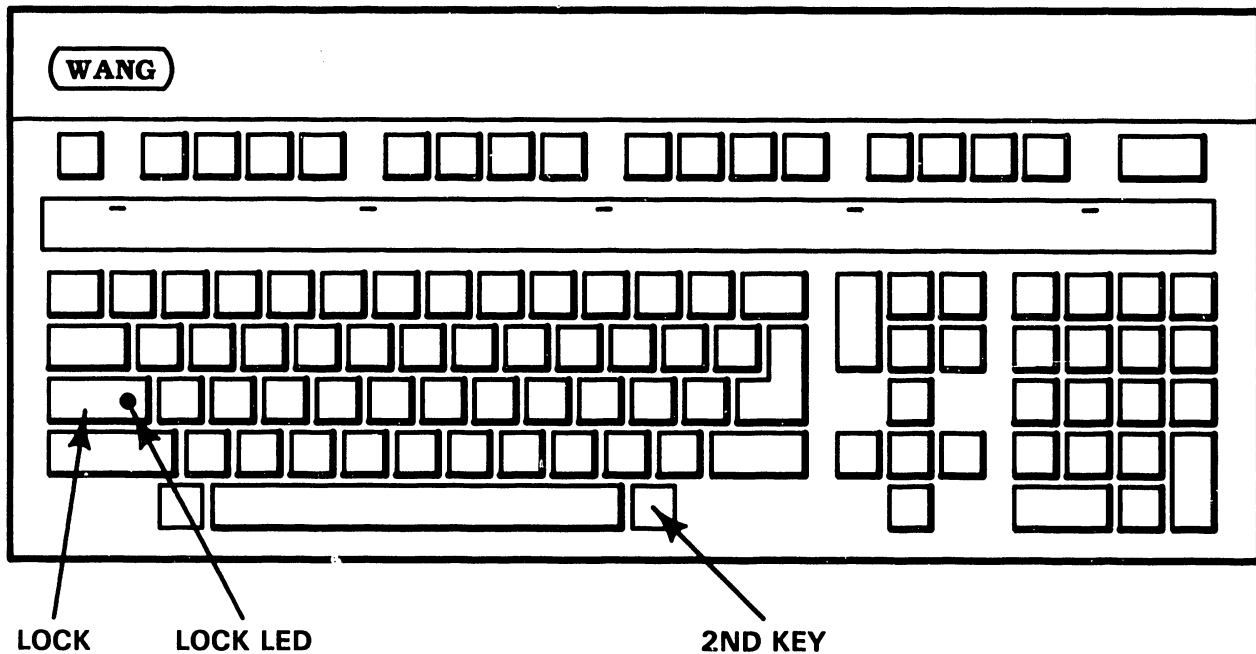
3.2 KEYBOARD, continued

Zone 4 - Special Function Keys: Across the top of the Keyboard are 16 Special Function keys. These keys provide the special Word Processing functions which simplify document creation and revision. For example, the CENTER key automatically centers a line of text, the MOVE key allows any amount of consecutive text to be moved within a document, and the REPLC key allows a character-defined sequence to be replaced with another within a document. For data processing, these keys can call any of 16 special Program Functions (PF1 through PF16).



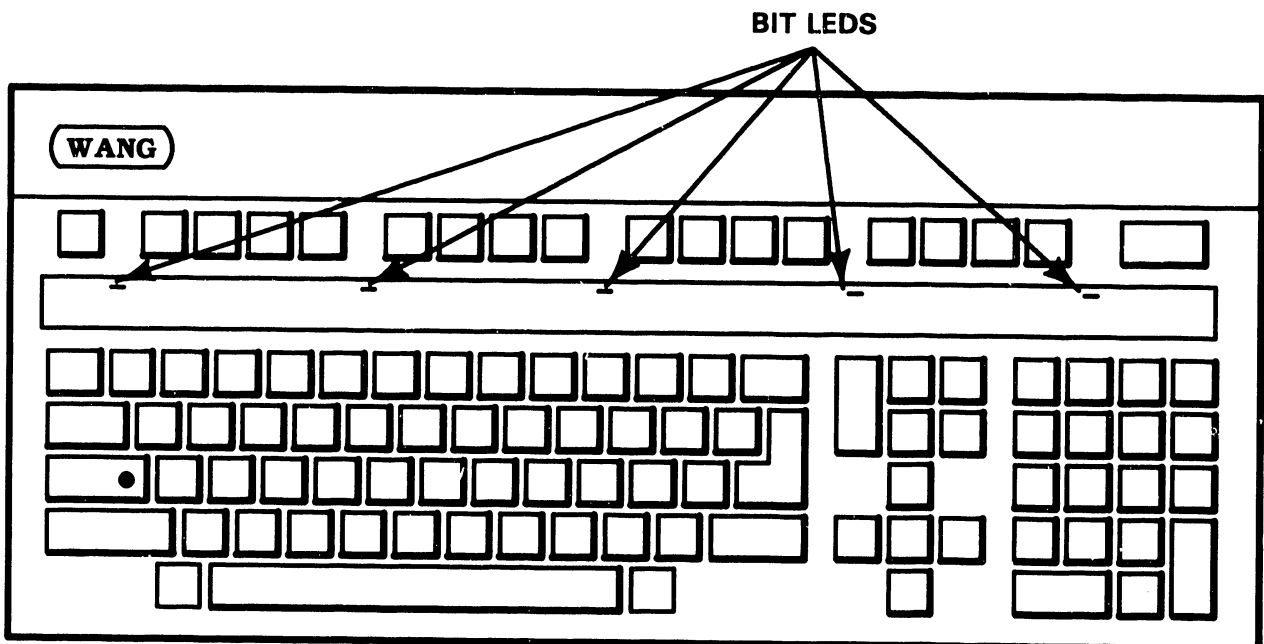
3.2 KEYBOARD, continued

The shift LOCK key acts as a caps-lock feature, allowing letters to be capitalized but not causing the numeric/symbolic characters to be upshifted. When the shift LOCK key is pressed, an LED built into the key is illuminated. Pressing either SHIFT key unshifts the keyboard and extinguishes the LED. The Keyboard allows characters to be underlined and all displayable characters can be made to repeat. A "2ND" key is present which allows special operating features of the workstation to be exercised. Refer to section 3.6 for a description of these features.



3.2 KEYBOARD, continued

Located across the function strip on the Keyboard are five LEDs. These LEDs are software programmable and are used to denote diagnostic error codes during system power-on, when the Built-In Test (BIT) is running.



3.3 INITIAL CONTROL SETTINGS

The only initial setting that requires attention is the external 115V/230V Power Supply switch detailed in Chapter 4 (Installation) of this manual.

3.4 4210 WORKSTATION INITIAL TURN-ON PROCEDURE

Prior to turning on the workstation, ensure that all packing materials (tape, plastic wrap, etc.) are removed from the unit. Inspect the unit to ensure that all cables are properly attached and verify the ac input voltage switch setting as described in Chapter 4.

The following procedure is recommended for initial system turn-on:

Set the I/O switch on the front of the Electronics Base to the 1 (on) position. When power is first applied the following actions will ensue:

- o The workstation's internal fan starts
- o A short beep sounds
- o The BIT begins to run
- o the Keyboard LEDs flash on and off in accordance with the BIT
- o The monitor begins to display various test patterns, although this may not be visible if the CRT has not warmed up sufficiently. See Chapter 4 for details on the BIT.

3.4 4210 TURN-ON PROCEDURE, continued

after successful completion of the BIT, the host CPU will execute the IPL (Initial Program Load) sequence. When the IPL is completed, the Monitor will display the LOGON screen. If the unit is not on line, the ID field message of the BIT will appear on the first line of the CRT.

3.5 4220 WORKSTATION INITIAL TURN-ON PROCEDURE

3.5.1 INITIAL TURN-ON

To turn on the 4220 Workstation, simply press 1 (on) on the 1/0 (on/off) switch on the front panel of the Electronics Base.

When power is first applied the following actions will ensue:

- o The workstation's internal fan starts
- o A short beep sounds
- o The BIT (Built-In Test) begins to run. (Refer to Chapter 4 for details on the 4220 BIT.)
- o the Keyboard LEDs will flash on and off
- o The monitor will display the power-up screen (Figure 3-2), although this won't be visible until the CRT has warmed up sufficiently.

- 3.5 4220 TURN-ON PROCEDURE, continued
3.5.1 INITIAL TURN-ON, continued

WS # 00 (ROUTING ADDRESS)	BISYNC RDLP 6.12.00 (BOOTLOADING REVISION #)
4220R POWER UP	
REV 5380 (DIAGNOSTICS REVISION #)	WANG VS

During microcode down-loading:

WS # 00	LOADING MC 06.10.00 - 2200	BISYNC RDLP 6.12.00
(MICROCODE REVISION #)	(CURRENT LOADING ADDRESS)	

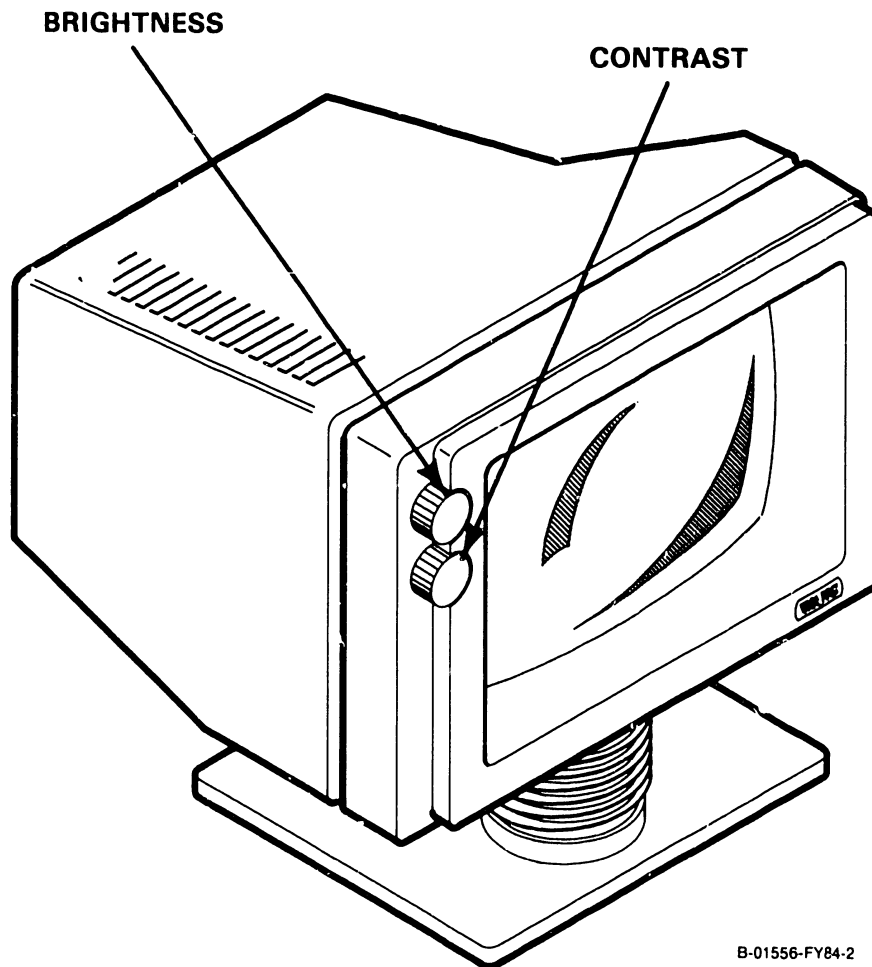
Note: Entries enclosed in parentheses () are not displayed on the 4220 power up screen. They are shown to identify screen entries only.

Figure 3-2. 4220 Power Up Screen

3.5 4220 TURN-ON PROCEDURE, continued

3.5.1 INITIAL TURN-ON, continued

If the power-up screen does not appear, adjust the Brightness and Contrast controls at the upper left edge of the Monitor front panel.



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3.5 4220 TURN-ON PROCEDURE, continued

3.5.1 INITIAL TURN-ON, continued

After successful completion of the BIT, the host CPU can execute the IPL (Initial Program Load) sequence once the connection from the host to the remote site has been activated. See section 3.5.2 for information on that procedure.

Once the host-to-remote-site connection has been activated, the microcode is transferred to the workstation in 2k blocks, and a message on the first line of the CRT screen will display the microcode version that is being loaded.

```
WS # 00  LOADING MC 06.10.00 - 2200      BISYNC RDLP 6.12.00
```

(MICROCODE REVISION #)

(CURRENT LOADING ADDRESS)

Note: Entries enclosed in parentheses () are not displayed on the 4220 power up screen. They are shown to identify screen entries only.

3.5 4220 TURN-ON PROCEDURE, continued

3.5.1 INITIAL TURN-ON, continued

The address of the current block being loaded is also shown. Additionally, the five Keyboard LEDs across the Keyboard function strip will count, in binary, the number of 2k block transfers that have been completed. The left-most LED is considered the MSB and the right-most LED, the LSB for the binary counting scheme.

If for any reason the host CPU fails to download the workstation microcode, the HELP key may be pressed to send an unsolicited interrupt to the host. The interrupt should start the downloading process.

When the IPL is completed, the Monitor will display the LOGON screen.

3.5.2 CONNECTING AND ACTIVATING THE REMOTE SITE

In its normal operating mode, the 4220 Remote Workstation does not appear to the operator to be a telecommunicating device and, therefore, no special operator instructions apply other than to establish a connection between the remote site and the host CPU. If the remote station is connected to the host CPU by a leased line, simply call the host CPU operating personnel to request activation of the remote workstation.

3.5 4220 TURN-ON PROCEDURE, continued

3.5.2 CONNECTING AND ACTIVATING THE REMOTE SITE, continued

If the remote station is set up for dial-up connection to the host CPU, perform the following procedure to establish communication between the workstation and the host CPU.

- o Dial the telephone number associated with the VS host CPU to which you will communicate. Establish contact with the appropriate operating personnel and explain that you are initiating a 4220 Remote Workstation.
- o At the instruction of the host CPU operator, press the DATA button on the remote modem. At this point, you will lose voice contact.
- o Upon hearing a clear dial tone, the operator at the host CPU site will press the local modem's DATA button, thus establishing telecommunications service.

3.6 SPECIAL OPERATING FEATURES

The 4210 and 4220 Workstations employ the "2ND" key to call up special operating features unique to each unit. The features are secondary functions of other keys on the Keyboard. The 4220 Workstation displays messages regarding operation of the attached printer and a communication link failure message. The following sections detail these features.

3.6 SPECIAL OPERATING FEATURES, continued

3.6.1 4210 "2ND" KEY SPECIAL FEATURES

- o 2ND, PF2 (PAGE) - Turns display of the graphics page of CRT memory on or off with successive presses of 2ND, PF2 (PAGE).
- o 2ND, PF3 (CENTER) - Turns display of the text page of CRT memory on or off with successive presses of 2ND, PF3 (CENTER).
- o 2ND, ERASE - Erases the contents of the graphics page of CRT memory.
- o 2ND, PF5 (FORMAT) - Places the workstation in the setup mode for setting the audio prompt and clicker volume. Pressing PF16 clears the setup mode. Operation of the 4210 setup mode is described below.

The setup mode is entered by pressing in sequence, 2ND, PF5 (FORMAT). The CRT screen will be cleared of the previous display, which is replaced by a graphics display of a bell, and a finger pushing a key. The bell represents the volume of the audio prompt, while the finger pushing the key represents the volume of the clicker. A setup mode cursor at the bottom of the CRT screen can be moved (with the east/west cursor keys) under either the bell or the finger pushing the key, indicating which volume adjustment is active. The volume adjustment is made with the cursor north/south keys. The previous display screen, although preempted by the setup mode screen, continues to be updated while in the setup mode.

3.6 SPECIAL OPERATING FEATURES, continued

3.6.1 4210 "2ND" KEY SPECIAL FEATURES, continued

To adjust the volume of either the audio prompt or the clicker proceed as follows:

- o Enter the setup mode by pressing in sequence 2ND, PF5 (FORMAT). (This can be done anytime after the workstation microcode has been down-loaded from the host CPU.)
- o Using the cursor east/west keys, move the setup mode cursor under the bell to adjust the audio prompt volume or under the finger pushing the key to adjust the clicker volume.
- o Use the cursor north key to step the selected graphics display toward the top of the screen (higher in volume) or use the cursor south key to step the selected graphics display toward the bottom of the screen (lower in volume).
- o Press PF16 to return to the previous display.

3.6.2 4220 "2ND" KEY SPECIAL FEATURES

- o 2ND, PF13 (CANCEL) - Restarts the workstation as if just powered on, except that the diagnostics are not performed.

3.6 SPECIAL OPERATING FEATURES, continued

3.6.2 4220 "2ND" KEY SPECIAL FEATURES, continued

- o 2ND, PF5 (FORMAT) - Places the workstation in setup mode for setting the audio prompt and clicker volume, and selecting/deselecting the type-ahead and receive/transmit features. Pressing PF16 clears setup mode. Operation of the 4220 setup mode is described below.

The setup mode is entered by pressing in sequence, 2ND, PF5 (FORMAT). The CRT screen will be cleared of the previous display, which is replaced by a reverse video field showing the setup options and connected printer type as shown below.

BELL	CLICKER	TYPE-	RECEIVE/	
VOLUME	VOLUME	AHEAD	TRANSMIT	PRINTER =

In addition, symbols representing each option appear above the option names. A special setup mode cursor also appears over one of the option names and can be moved over any one of the options by using the cursor east/west keys. Placing the cursor over an option selects that option to be modified, either in volume for the audio prompt and clicker, or on/off as with the type-ahead and receive/transmit features. The option is modified with the cursor north/south keys.

3.6 SPECIAL OPERATING FEATURES, continued

3.6.2 4220 "2ND" KEY SPECIAL FEATURES, continued

To adjust/select any of the setup options, proceed as follows:

- o Enter the setup mode by pressing in sequence 2ND, PF5 (FORMAT). (This can be done anytime after the workstation microcode has been downloaded from the host CPU.)
- o Using the cursor east/west keys, move the setup cursor over the option to be adjusted/selected.
- o Use the cursor north/south keys to adjust/select the option. For audio prompt and clicker volume, pressing the north key steps the volume to the next higher level. Pressing the south key lowers the volume to the next lower level. For the type-ahead and receive/transmit features, pressing the north key enables the option, pressing the south key disables the option.
- o Press PF16 to return to the previous display.

Descriptions of the type-ahead and receive/transmit options follow.

Type-ahead - The type-ahead feature allows the user to enter data from the keyboard while, at the same time, executing data I/O to and from the host CPU. For the user knowledgeable of the next screens, this eliminates waiting for the screens to change.

3.6 SPECIAL OPERATING FEATURES, continued

3.6.2 4220 "2ND" KEY SPECIAL FEATURES, continued

Receive/Transmit - This feature uses the two left-most Keyboard LEDs to signal the user of data received from and transmitted to the host CPU. The farthest left LED indicates a received data stream from the host to the workstation; the next LED (2nd from the left) indicates a transmitted data stream from workstation to host.

The 'PRINTER =' field displays the printer type that the rear panel DIP switches are set for using one of the following designations: LC MATRIX, MATRIX, DAISY, BAND.

3.6.3 4220 PRINTER TO WORKSTATION MESSAGES

Attention required-type messages associated with an attached printer are displayed on the line 25 of the workstation connected to the printer. The message initially blinks on and off. Pressing the RESET key cancels the blinking and servicing the printer clears the message.

Table 3-1 identifies the four possible messages that can be issued by the printers used with the 4220 Workstation, and the conditions under which they are issued. Note that these messages are displayed at the remote workstation only, and that at the host CPU, only the general assistance-required message will appear.

3.6 SPECIAL OPERATING FEATURES, continued

3.6.3 4220 PRINTER/WORKSTATION MESSAGES, con't

PRINTER	CONDITION			
	OFFLINE	PAPER LOW	MALFUNCTION	POWER OFF
Band	ID# 00	01	02	03
Daisy	00	00	02	00
Matrix/ Low Cost Matrix	00	00	02	00

ID#	MESSAGE
00	Assistance Required for Attached Printer (Offline)
01	Assistance Required for Attached Printer (Paper Low)
02	Assistance Required for Attached Printer (Malfunction)
03	Assistance Required for Attached Printer (Power Off)

3.6.4 4220 COMMUNICATION LINK FAILURE MESSAGE

If the communication link to the host CPU is lost, the 4220 Workstation will display one of two messages on the 25th line of the CRT screen. The message displayed depends upon the type of communication link failure sensed by the workstation as follows:

COMMUNICATION LINK FAILURE TO HOST SYSTEM

or

4220R REMOTE WORKSTATION DEACTIVATED

3.7 NORMAL SHUT-DOWN PROCEDURE

Before turning off the workstation, be sure to LOGOFF (PF16). Turn off the workstation by setting the I/O power switch to the 0 (off) position.

3.8 EMERGENCY SHUT-DOWN PROCEDURE

In case of an emergency situation when the normal shut-down procedure cannot be used, proceed as follows:

- o Set the I/O (on/off) switch to the 0 (off) position.

- o Remove the ac power plug from the outlet.

CHAPTER

4

INSTAL-

LATION

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CHAPTER 4 INSTALLATION

This chapter contains information required to properly install the 4210 and 4220 Workstation. The 4210 Workstation is shipped with all internal switches preset for proper operation, eliminating the need for CE personnel to disassemble units of the workstation during the installation process. Switch setting information usually found here will be found in Chapter 5: Maintenance for the 4210.

4.1 INSTALLATION SITE CHECK

4.1.1 ENVIRONMENTAL

The environment in which the workstations operate can greatly affect their performance. Considerations of temperature, humidity and cleanliness are discussed below.

4.1.1.1 Temperature Considerations

The recommended operating temperature range for the workstation is from 60°F to 80°F (15°C to 27°C), but a range from 50°F to 90°F (10°C to 32°C) is allowable. Since nearly all locations are heated, low outside temperatures are usually not a problem. High temperatures can be a problem, however, in locations that do not have air conditioning. If the system is used where temperatures exceed the maximum specified, component failure rates may increase, resulting in costly downtime.

4.1.1 ENVIRONMENTAL, continued

4.1.1.1 Temperature Considerations, continued

If an air conditioning unit is already installed or if one is to be installed, such equipment must be powered on a power line separate from the one connecting to the workstation. If separate power is not used, data errors can occur when the air conditioner is in use.

Air conditioning also removes moisture and dust from the air by lowering the humidity. Lower humidity levels along with static build-up from carpets and synthetic clothing can impart a static electrical charge on operating personnel. When the operator comes in contact with the unit, resultant static discharge can cause unit failures.

4.1.1.2 Humidity Considerations

The recommended relative-humidity range is from 35% to 65%. Humidifiers or dehumidifiers should be installed to increase or decrease the humidity as required. If carpeting is to be installed, be sure it is a non-static variety. If existing carpeting is not of the non-static type, it will either have to be treated with a non-static spray or an electrically conductive mat must be installed to prevent a static charge build-up. Carpets treated with non-static spray should be thoroughly cleaned before the first treatment, and they should be retreated at least once every three months thereafter. If an electrically conductive mat is used, it should be installed under the unit's operating area and must be properly connected to an earth ground.

4.1.1 ENVIRONMENTAL, continued

4.1.1.3 Cleanliness Considerations

Dust can accumulate within the workstation since it contains no air filters. Dirt and grease form a film that prevents proper heat dissipation from components and can also create a leakage path for signals. To prevent this type of failure, all air conditioning, heating and ventilating units should have air filters installed; these filters should be cleaned or replaced regularly.

4.1.2 ELECTRICAL SERVICE CONSIDERATIONS

The workstation is designed to operate domestically with a 115V, 60 Hz power source, or internationally with a 230V, 50 Hz power source. The source outlet should not be electrically connected to other equipment capable of generating voltage fluctuations on the power line (such as paper shredders, electrical stamp machines/staplers, coffee makers, etc.)

The workstation is outfitted with a three-wire power cord, designed for connection to a standard grounded outlet (NEMA 5-15IG receptacle).

4.1.3 EQUIPMENT POSITIONING

Equipment positioning is limited by the following cable lengths:

- o A maximum of 2000 feet from the 4210 Workstation to the host CPU.

4.1 INSTALLATION SITE CHECK, continued

4.1.3 EQUIPMENT POSITIONING, continued

- o A maximum of 50 feet from the 4220 Workstation to its modem if it is remote from the host CPU.

- o A maximum of 50 feet from the 4220 Workstation to the host CPU if it is connected locally via a null modem.

Other than the above considerations, no special requirements apply with respect to positioning the workstation except for common-sense considerations of user convenience and non-interference with traffic flow.

4.2 UNPACKING AND INSPECTION

4.2.1 INSPECTION UPON ARRIVAL

When the equipment arrives, immediately locate the packing slip and note the work order number. Verify the equipment model and serial number as listed on the packing slip.

Before opening the container, inspect it carefully for signs of damage (crushed edges, puncture holes, tears, etc.) If damage is noted, promptly file a claim with the carrier and notify the factory:

WLI DISTRIBUTION CENTER
Department #90
Quality Assurance Department
Tewksbury, MA 01876

4.2 UNPACKING AND INSPECTION, continued

4.2.1 INSPECTION UPON ARRIVAL, continued

State the nature and extent of damage and make arrangements for replacement equipment if necessary. Be certain to include the following information:

WORK ORDER # _____
CUSTOMER NAME _____
CUSTOMER # _____
MODEL # _____
SERIAL # _____

4.2.2 UNPACKING

The 4210/4220 Workstation comes packaged in three containers: one each for the 12-inch Monitor, the Keyboard and the Electronics Base. Each unit is considered separately in the following sections.

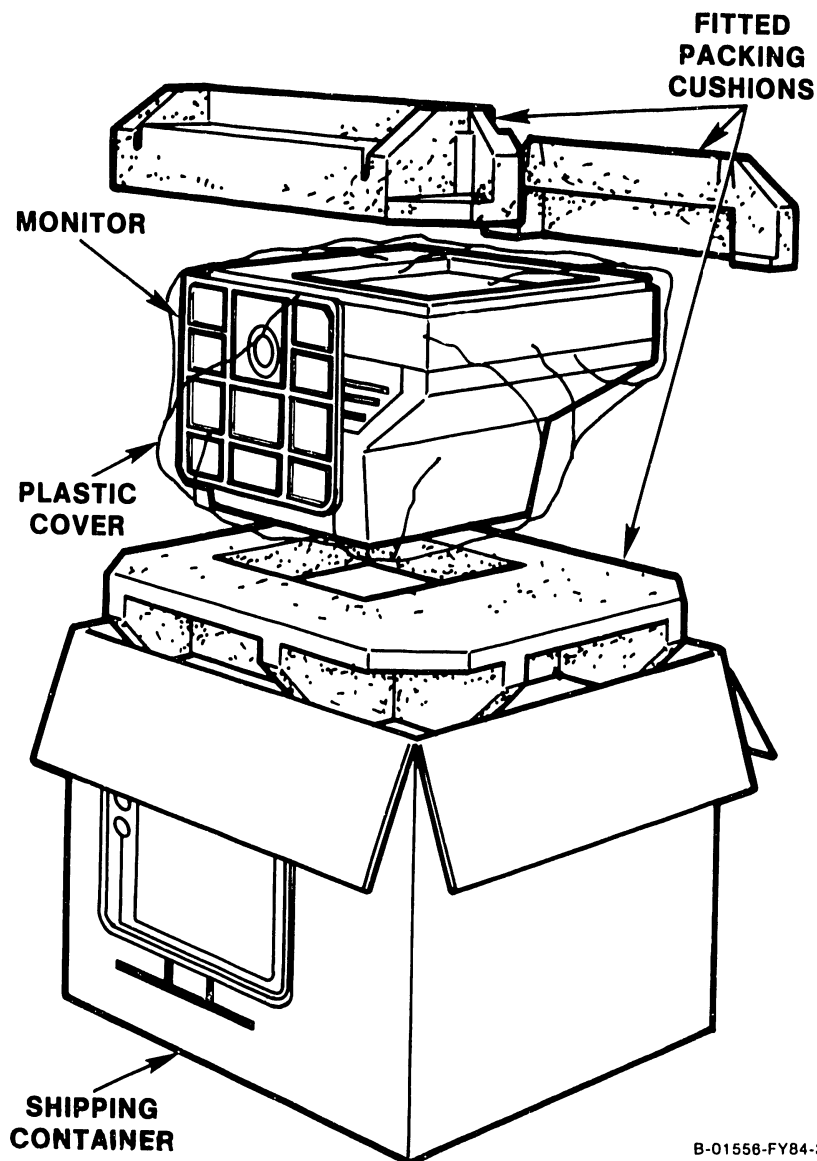
4.2.2.1 Unpacking the Monitor

Refer to Figure 4-1 and the following procedure to unpack the Monitor. Save all packing material until the unit performs satisfactorily.

4.2.2 UNPACKING, continued

4.2.2.1 Unpacking the Monitor, continued

- o Cut the tape sealing the top of the shipping container, being careful not to penetrate so deeply as to contact the contents. Open the shipping container.
- o Remove the fitted packing cushions.
- o Lift the Monitor out of the shipping container and remove the plastic wrapping.



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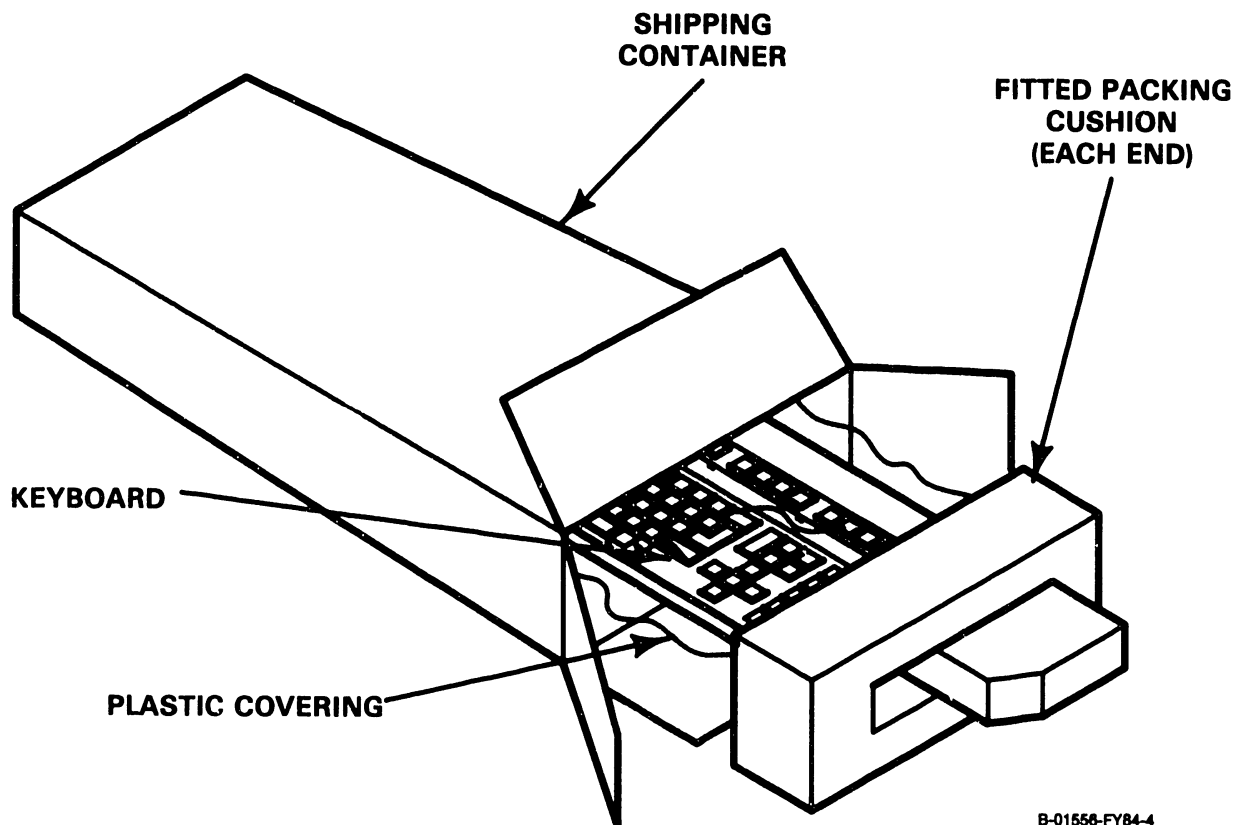
Figure 4-1 Unpacking the Monitor

4.2.2 UNPACKING, continued

4.2.2.2 Unpacking the Keyboard

Refer to Figure 4-2 and the following procedure to unpack the Keyboard. Save all packing material until the unit has been found to function satisfactorily.

- o Cut the tape sealing the end of the shipping container, being careful not to penetrate so deeply as to contact the contents. Open the shipping container.
- o Slide the Keyboard out of the shipping container and remove the plastic wrapping.



B-01556-FY84-4

Figure 4-2. Unpacking the Keyboard

4.2.2 UNPACKING, continued

4.2.2.3 Unpacking the Electronics Base

Refer to Figure 4-3 and the following procedure to unpack the Electronic Base. Save all packing material until the unit has been found to function satisfactorily.

- o Cut the tape sealing the top of the shipping container, being careful not to penetrate so deeply as to contact the contents. Open the shipping container.
- o Lift the base out of the shipping container along with its fitted packing cushions and the cable bag (taped to the base wrapping).
- o Remove the packing cushions and plastic wrapping from around the Electronics Base.

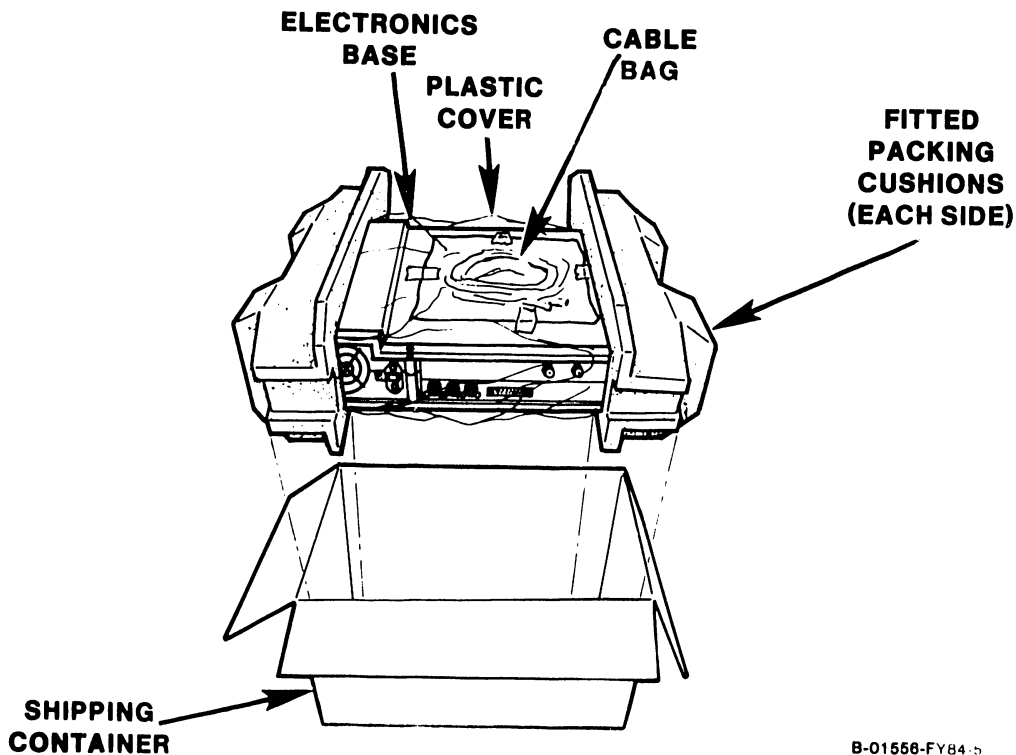


Figure 4-3. Unpacking the Electronics Base

4.3 WORKSTATION INSTALLATION PROCEDURES

Workstation installation procedures are presented under three major subject headings as follows:

Section 4.4: 4210 Installation Procedures

This section details installation procedures unique to the 4210 Workstation.

Section 4.5: 4220 Installation Procedures

This section details installation procedures unique to the 4220 Workstation.

Section 4.6: Common Installation Procedures

This section details installation procedures common to both the 4210 and 4220 Workstation.

First, proceed to the section dealing with the procedures unique to workstation you are installing. Next, perform the common installation procedures. After the common installation procedures have been performed, proceed to the post-installation procedures in section 4.7.

4.4 4210 WORKSTATION INSTALLATION PROCEDURES

The following subsections detail the installation procedures for the 4210 Workstation:

Section 4.4.1 4210 Switch Settings

Section 4.4.2 4210 System Interconnections

4.4.1 4210 SWITCH SETTINGS

The 4210 Workstation is shipped with all internal switches preset for proper operation. This eliminates the need for CE personnel to disassemble

4.4 4210 INSTALLATION PROCEDURES, continued

4.4.1 4210 SWITCH SETTINGS, continued

the Base unit and Keyboard at installation in order to access the internal switches. Switch settings are given in section 5.7 and are for reference only, as may be required when setting up a replacement 8264 CPU board or Keyboard.

Refer to section 4.6: Common Installation Procedures, for instructions on setting the external 115V/230V Power Supply switch on the rear of the Electronics Base.

4.4.2 4210 SYSTEM INTERCONNECTIONS

4.4.2.1 Workstation to Host CPU Cable

The standard interconnecting cable supplied for connecting the 4210 Workstation to the host CPU is a 25-foot, dual coaxial cable with a BNC/TNC connector pair at each end. The standard cable, part number 220-0148, is packed with the 4210 Electronics Base. The distance between the workstation and the host CPU can be extended from the standard 25 feet to 2000 feet by using optional dual coaxial cables available under the following part numbers:

<u>LENGTH (FT.)</u>	<u>PART NUMBER</u>
50	120-2300-1
100	120-2300-2
150	120-2300-3
---	----
---	----
---	----
2000	120-2300-40

4.4.2 4210 SYSTEM INTERCONNECTIONS, continued

4.4.2.2 Connecting the 4210 to the Host CPU

Connect a dual coaxial cable from the DATA LINK connectors on the rear of the 4210 Electronics Base, to the serial IOP dual BNC/TNC connector panel of the host CPU. Refer to Figure 4-4. These connections are a BNC/TNC pair and can only be connected BNC to BNC, TNC to TNC. The length of this cable is not to exceed 2000 feet.

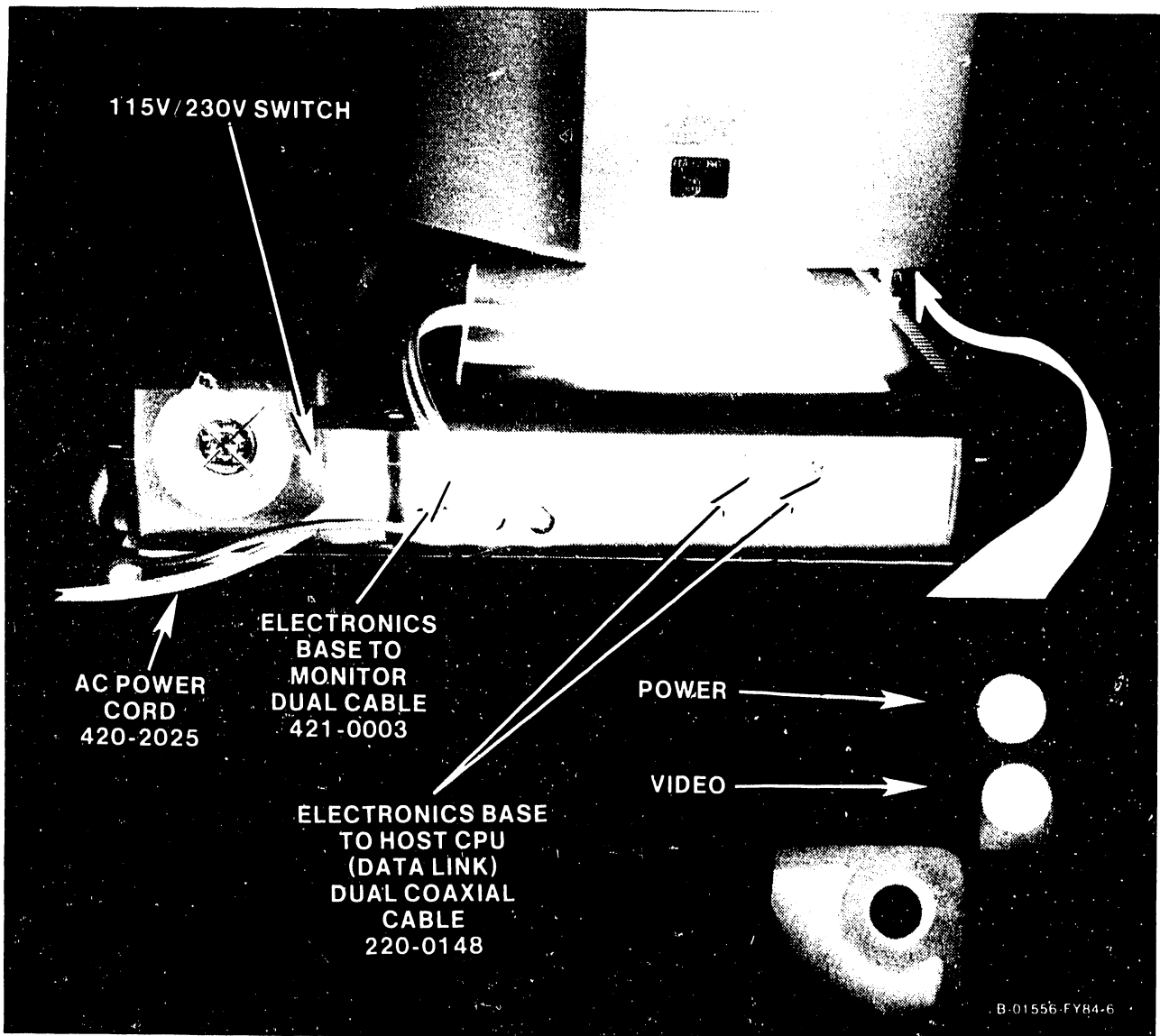


Figure 4-4. 4210 Workstation Interconnections

4.4.2 4210 SYSTEM INTERCONNECTIONS, continued

4.4.2.3 RS-232 Telecommunications Port

The 4210 Workstation provides a standard 25-pin, RS-232C connector on the rear of the Electronics Base. At this time, however, the telecommunications function is not supported.

4.4.2.4 Other Connections

The interconnection of the Monitor, Keyboard and Electronics Base is detailed in section 4.6, Common 4210/4220 Installation Procedures.

4.5 4220 WORKSTATION INSTALLATION PROCEDURES

The following subsections detail the installation procedures for the 4220 Workstation:

Section 4.5.1 4220 Switch Settings

Section 4.5.2 4220 System Interconnections

4.5.1 4220 SWITCH SETTINGS

The 4220 Workstation has two 10-section switch-banks, SW1 and SW2, located on the rear of the Remote Workstation Electronics PCA. Both switches are located so that they are accessible through cut-outs in the connector header, and the header is silkscreened to make switch identification easy. The switches used to set a variety of workstation operating parameters are covered separately in the following sections.

4.5 4220 INSTALLATION PROCEDURES, continued4.5.1 4220 SWITCH SETTINGS, continued

Note that the silkscreen on the connector header identifies the switch sections from SW1 section 1, to SW2 section 10, consecutively, as sections 1 through 20. The switches themselves, however, are each numbered 1 through 10, and the number markings on the switches can also be read through the cut-outs in the connector header. In the following subsections, the silkscreened switch section number is used in identifying the switch sections.

4.5.1.1 Main TC Port Switch Settings and Jumper

Jumper J11 selects either synchronous or asynchronous operation of the main TC port. Currently, only synchronous operation is supported and the jumper is set as shown below for synchronous operation at the factory. The asynchronous setting is given for reference.

Synchronous: J11-2 to J11-3

Asynchronous: J11-1 to J11-2

Switch sections SW2-12, 13, and 14 are used to select either the external clock input as required for synchronous operation, or one of seven baud rates possible for asynchronous operation. Currently, only synchronous operation is supported and the switches must be set as

4.5.1 4220 SWITCH SETTINGS, continued

4.5.1.1 Main TC Port Switch Settings and Jumper

shown below for synchronous operation. Asynchronous baud rate settings are given for reference.

SW2 SWITCH SECTION

<u>12</u>	<u>13</u>	<u>14</u>	<u>BAUD RATE</u>
DOWN	DOWN	DOWN	External Clock*
DOWN	DOWN	UP	19,200
DOWN	UP	DOWN	9600
DOWN	UP	UP	4800
UP	DOWN	DOWN	2400
UP	DOWN	UP	1200
UP	UP	DOWN	600
UP	UP	UP	300

*This setting required for synchronous operation per current software support.

4.5.1.2 Auxiliary TC Port Switch Settings

The auxiliary TC port can be configured for synchronous operation with an external clock or for asynchronous operation at one of seven baud rates. The selections are made with SW1 sections 1, 2 and 3. At this time, the auxiliary TC port is not supported and the switch settings below are given for reference only.

4.5.1 4220 SWITCH SETTINGS, continued

4.5.1.2 Auxiliary TC Switch Settings, continued

SW1 SWITCH SECTION

<u>1</u>	<u>2</u>	<u>3</u>	<u>BAUD RATE</u>	
DOWN	DOWN	DOWN	External (Synchronous)	Clock
UP	DOWN	DOWN	19,200	
DOWN	UP	DOWN	9,600	
UP	UP	DOWN	4,800	
DOWN	DOWN	UP	2,400	
UP	DOWN	UP	1,200	
DOWN	UP	UP	600	
UP	UP	UP	300	

Note: OFF position of SW1 switch sections is up.

4.5.1.3 Parallel Printer Switch Settings

The 4220 Workstation will currently support one of three parallel printers, either the 2281 Daisy, the 2235 Matrix or the 2273 Band printer. Rear panel switches SW2 16, 17, 18 and 19 are read by workstation microcode to determine the type of printer attached to the workstation. Set the switches as shown below and illustrated in Figure 4-5 to identify the type of printer attached to the workstation. If no printer is attached, these switches can be disregarded.

SW2 SWITCH SECTION

<u>16</u>	<u>17</u>	<u>18</u>	<u>19</u>	<u>PRINTER TYPE</u>
DOWN	UP	DOWN	DOWN	2281WR Daisy
DOWN	UP	DOWN	UP	2235R Matrix
DOWN	DOWN	DOWN	DOWN	2221/2231 Matrix
DOWN	DOWN	UP	DOWN	2273V-1/2 Band

4.5.1 4220 SWITCH SETTINGS, continued

4.5.1.4 Workstation Device Address Switch Settings

There are 32 device addresses associated with each TC IOP on the VS system for device polling and selection activity. Switch SW1 sections 8, 7, 6, 5 and 4 are used to identify the device address for the 4220 Workstation in binary as shown below. SW1-8 is considered MSB and SW1-4 LSB in the binary numbering scheme, with a total of 32 possible combinations (0 - 31). Some examples are also shown below. Set the switches in accordance with the device address of the workstation as assigned by the host VS system operating personnel.

SECTION

DEVICE

<u>ADDRESS</u>	<u>8(MSB)</u>	<u>7</u>	<u>6</u>	<u>5</u>	<u>4(LSB)</u>
00	DOWN	DOWN	DOWN	DOWN	DOWN
01	DOWN	DOWN	DOWN	DOWN	UP
06	DOWN	DOWN	UP	UP	DOWN
31	UP	UP	UP	UP	UP
NUM.WEIGHT	16	8	4	2	1

4.5.1.5 Other Switch Settings

Refer to section 4.6, Common 4210/4220 Installation Procedures, for instructions on setting the external 115V/230V Power Supply switch on the rear of the Electronics Base.

4.5.2 4220 SYSTEM INTERCONNECTIONS

4.5.2.1 Workstation to Modem Cable

The standard interconnecting cable supplied for connecting the 4220 Workstation to a modem or null modem is a 25-foot RS-232C cable with standard RS-232C connectors at each end. The distance between the workstation and the modem can be increased to a maximum of 50 feet by using an optional 50-foot cable. The part numbers of both the 25 and 50-foot cables are shown below.

25-Foot RS-232C Cable, P/N 120-2227-25

50-Foot RS-232C Cable, P/N 120-2227-50

4.5.2 4220 SYSTEM INTERCONNECTIONS, continued

4.5.2.2 Connecting the 4220 to the Modem

Connect an RS-232C cable from the Main TC RS-232C connector on the rear of the 4220 Electronics Base, to the modem or null modem used with the workstation (Figure 4-6).

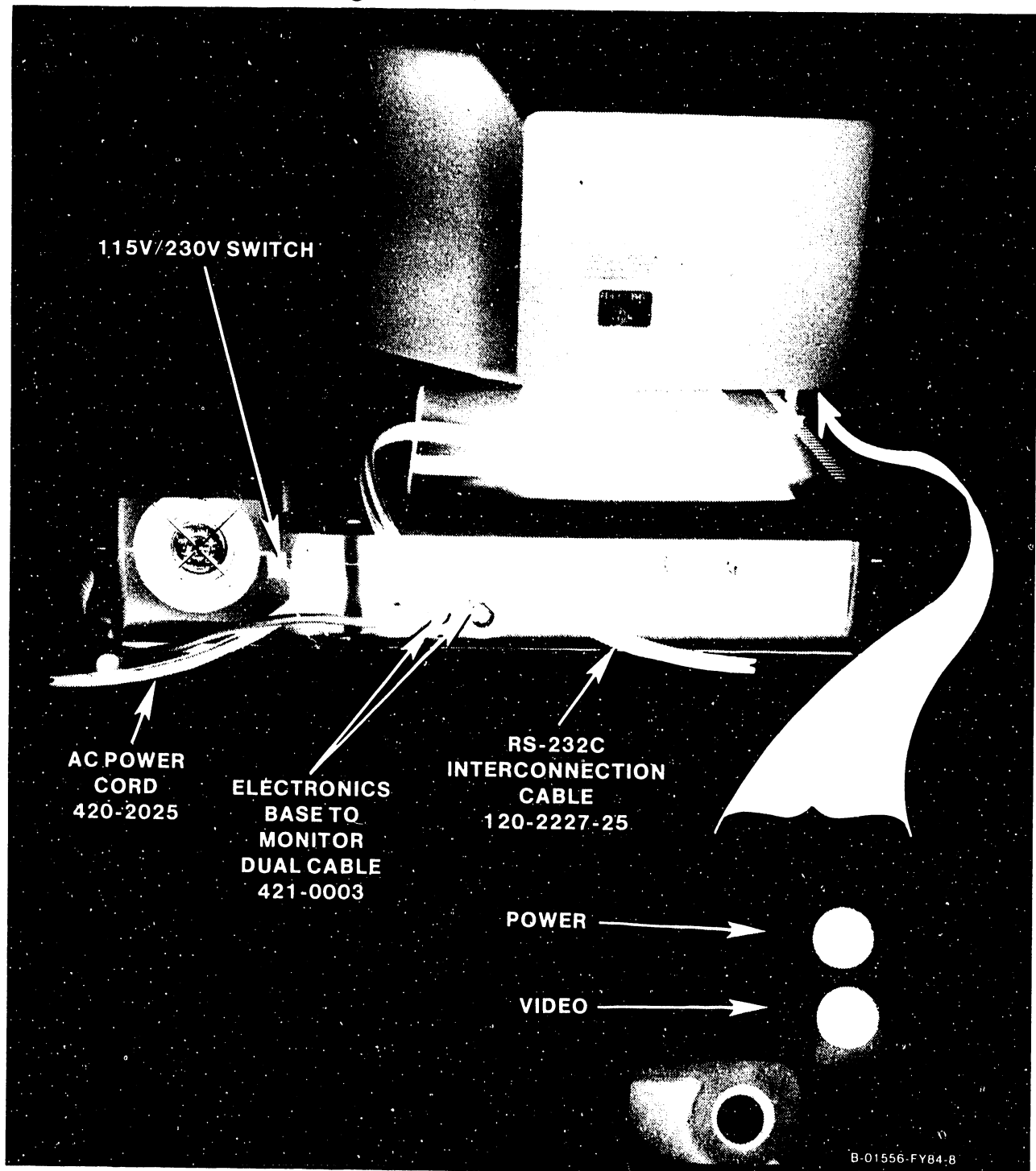
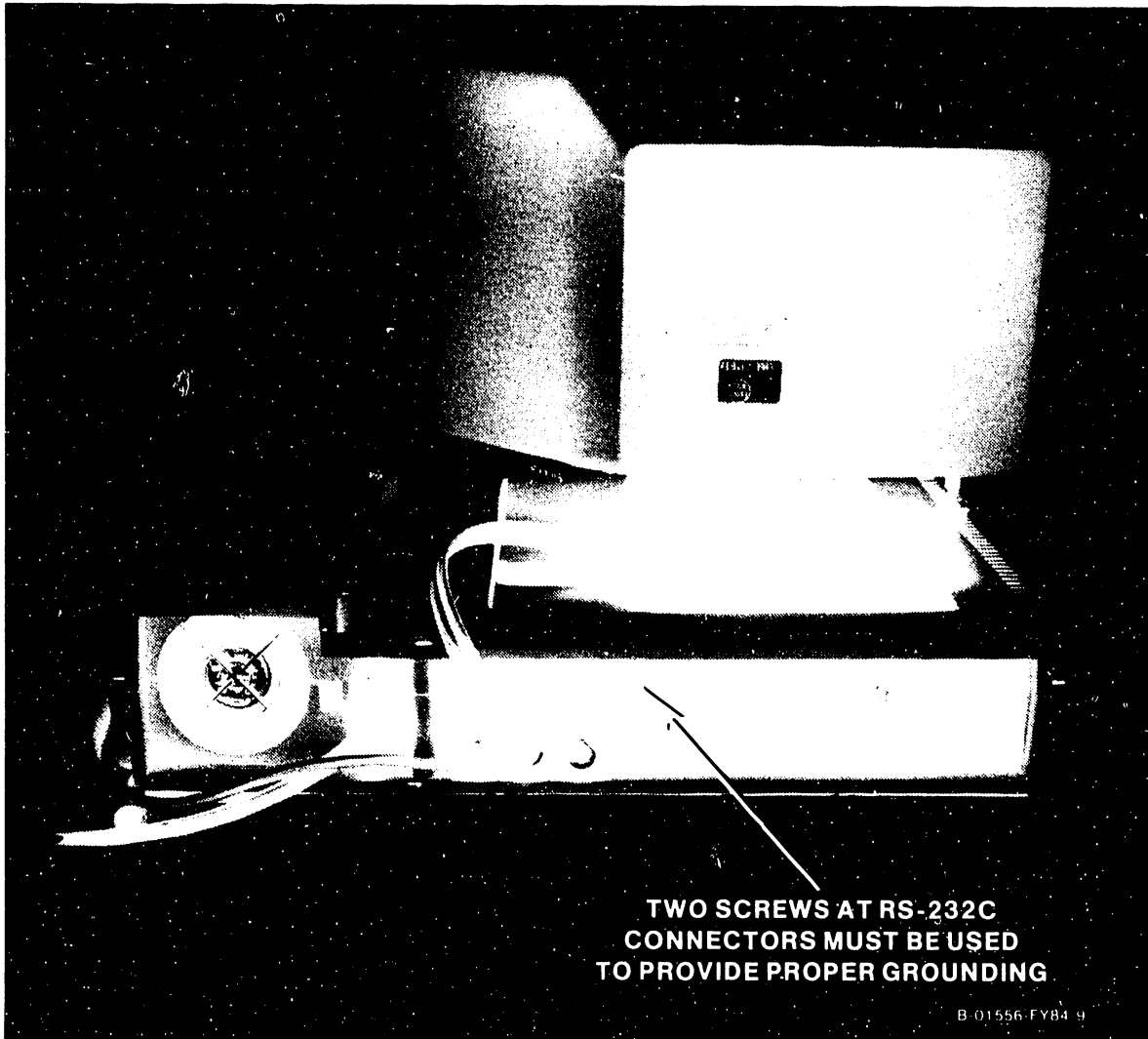


Figure 4-6. 4220 Workstation Interconnections

4.5.2 4220 SYSTEM INTERCONNECTIONS, continued

4.5.2.2 Connecting the 4220 to the Modem, cont'd

Secure each connector with two screws. The two screws which secure the RS-232C connector to the TC port must be used in the 4220 Workstation to provide proper ground connection. The length of this cable is not to exceed 50 feet.



4.5.2 4220 SYSTEM INTERCONNECTIONS, continued

4.5.2.3 Auxiliary RS-232 Telecommunications Port

The 4220 Workstation provides an auxiliary RS-232C connector on the rear of the Electronics Base. At this time, however, the auxiliary TC port is not supported.

4.5.2.4 Printer Connection

A Centronics-compatible printer interface connector is provided on the rear of the Electronics Base for connection to any one of the following parallel printers:

2235 Matrix

2281 Daisy

2273 Band

Be sure to identify the printer type by setting the associated switches properly as defined in section 4.5.1.3. Secure the printer cable (not supplied) to the 36-pin Printer connector with two screws.

4.5.2.5 Other Connections

The interconnection of the Monitor, Keyboard and Electronics Base is detailed in section 4.6, Common Installation Procedures.

4.6 COMMON WORKSTATION INSTALLATION PROCEDURES

This section details installation procedures common to both the 4210 and 4220 Workstations. After completing these procedures, proceed to section 4.7 for post-installation checks.

4.6.1 115V/230V POWER SUPPLY SWITCH

The setting of the 115V/230V Power Supply switch ensures that the Power Supply is set for the ac voltage in use at the installation site. This is an easily accessible switch on the rear of the Electronics Base and is described below.

CAUTION

Applying power to the workstation with an incorrectly set Power Supply switch will damage the switching Power Supply. Warning stickers are placed over the I/O switch on the front of the Electronics Base and over the power cord receptacle on the rear of the Electronics Base to alert installation personnel to check the Power Supply switch setting before applying power to the unit.

The workstation, powered from a single power supply in the Electronics Base, can be used with domestic power of 115 Vac at 60 Hz, or internationally with power of 230 Vac at 50 Hz. Switching between the two types of power is accomplished by means of a single switch accessible on the rear of the Electronics Base.

4.6 COMMON INSTALLATION PROCEDURES, continued

4.6.1 115V/230V POWER SUPPLY SWITCH, continued

- o Slide the 115V/230V switch either up or down so that the power at the installation site is readable on the switch, either 115V or 230V.

- o Remove the warning sticker over the power cord receptacle on the rear of the Electronics Base unit.

- o Remove the warning sticker over the I/O (on/off) switch on the front of the Electronics Base.

4.6 COMMON INSTALLATION PROCEDURES, continued

4.6.2 WORKSTATION INTERCONNECTING CABLES

The cables required to interconnect the Monitor, Keyboard and Electronics Base are supplied with the workstation. Information regarding these cables is given below.

Electronics Base-to-Monitor Dual Cable:

Description: Monitor Power, 3-Pin DIN each end.

Monitor Video, 8-Pin DIN each end.

Packed With: Electronics Base

Length: 2 feet

Part Number: 421-0003

Keyboard-to-Electronics Base:

Description: 4-Pin DIN one end, hard-wired internally to Keyboard; coiled

Packed With: Keyboard

Length: 1 ft, retracted

Part Number: 220-0305

Electronics Base-to-AC Power:

Description: 3-Prong male one end, 3-Prong female other end

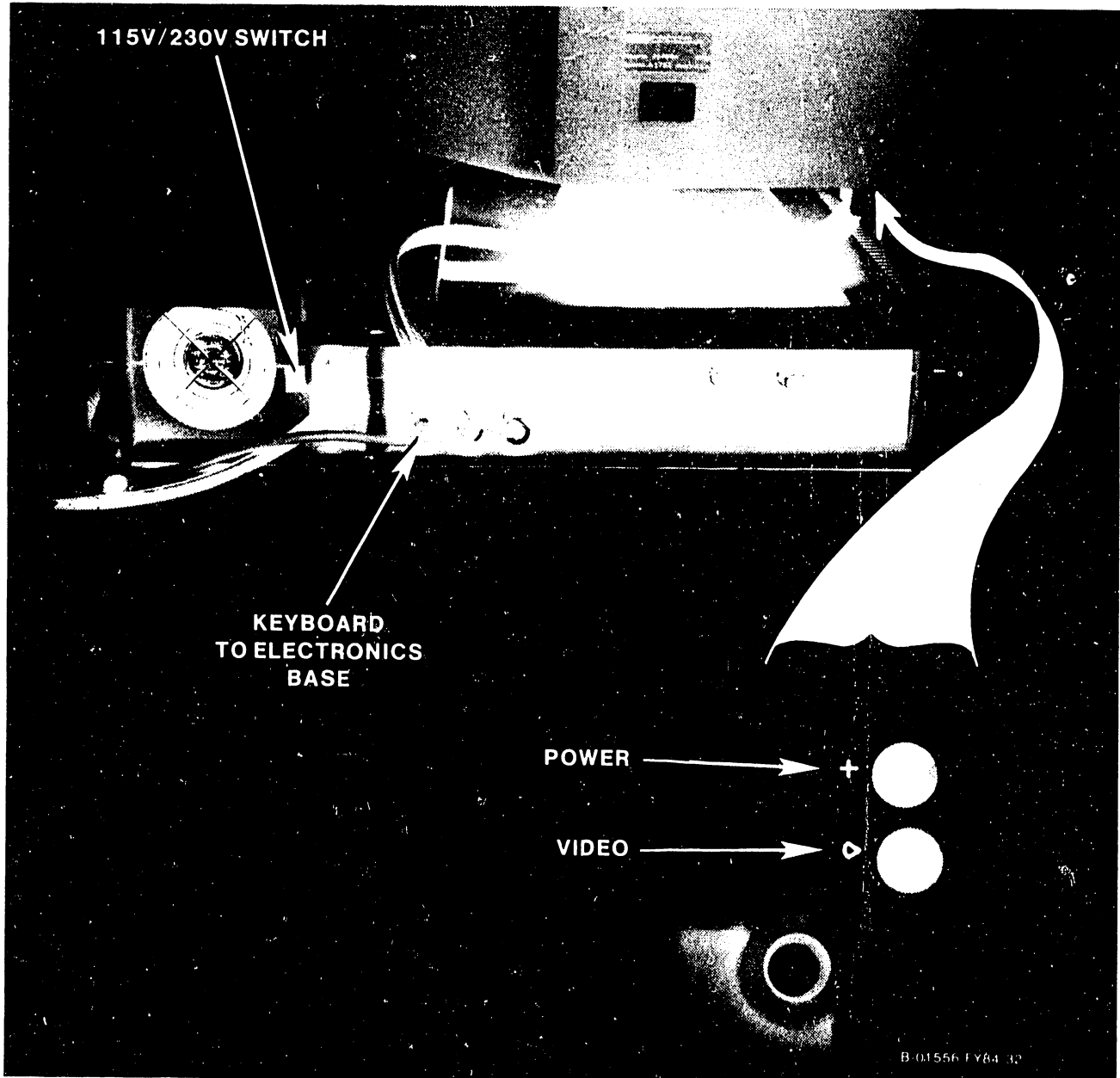
Packed With: Electronics Base

Length: 6 feet

Part Number: 420-2025

4.6 COMMON INSTALLATION PROCEDURES, continued
4.6.3 INTERCONNECTING THE MONITOR, KEYBOARD AND ELECTRONICS BASE

- o Insert the Keyboard 4-pin DIN plug into the KYBD connector on the rear of the Electronics Base.
- o Place the Monitor on its top and locate the power and video connectors on its underside. These connectors are identified by symbols as shown below.

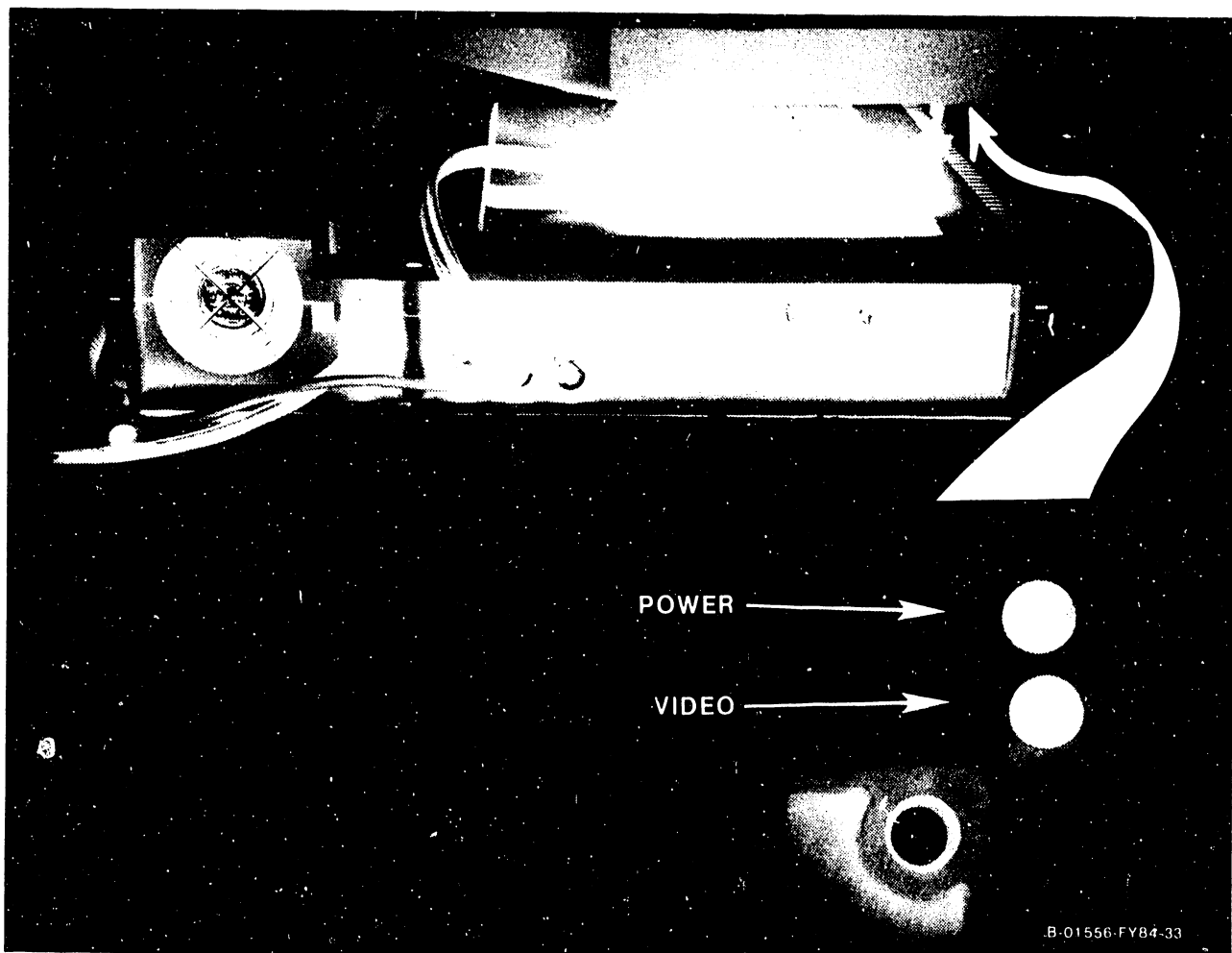


4.6 COMMON INSTALLATION PROCEDURES, continued
4.6.3 INTERCONNECTING THE MONITOR, KEYBOARD AND
BASE, continued

NOTE

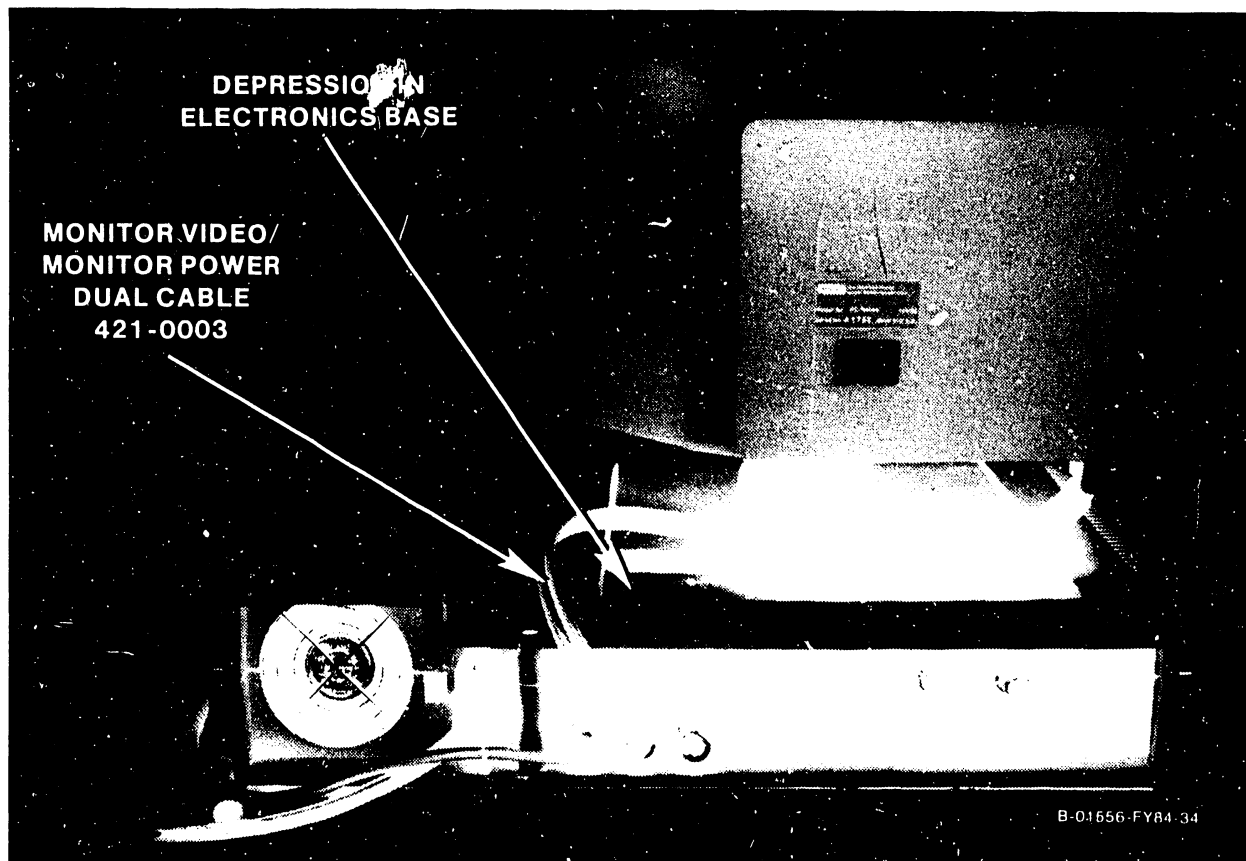
In the following steps, make certain that the cable connectors are fully seated by pushing them in to the full extent of their travel.

- o Insert the Monitor video 8-pin DIN plug into the video connector on the underside of the Monitor.
- o Insert the Monitor power 3-pin DIN plug into the power connector on the underside of the Monitor.



4.6 COMMON INSTALLATION PROCEDURES, continued
4.6.3 INTERCONNECTING THE MONITOR, KEYBOARD AND
BASE, continued

- o Place the Monitor platform in the depression in the top of the Electronics Base, cables toward the rear of the Electronics Base.
- o Insert the Monitor video 8-pin DIN plug into the VIDEO connector on the rear of the Base.
- o Insert the Monitor power 3-pin DIN plug into the PWR CRT connector on the rear of the Base.
- o Plug the female end of the power cord into its receptacle on the rear of the Electronics Base. Secure with two screws. Do not over-tighten. Plug the ac power cord into a suitable outlet.



4.7 POST-INSTALLATION CHECKS

4.7.1 SYSTEM SOFTWARE COMPATIBILITY

Microcode for the 4210 is supported on the following operating systems:

<u>4210</u>	<u>4220</u>
5.1.73	5.1.73
5.3.90	5.3.90
6.11	6.20
6.20	

Microcode File Name: @4210WM Version: 06.01.00
 @MC4220R Version: 06.10.00

4.7.2 SYSGEN CONSIDERATIONS (4210 ONLY)

With operating system 06.10.XX or above, the 4210 Workstation can be entered as device type 4210WM on the serial IOP screen of the GENEDIT menu.

4.7.3 4210 WORKSTATION TURN-ON

To turn on the 4210 Workstation, simply press 1 (on) on the 1/0 (on/off) switch on the front panel of the Electronics Base. When power is first applied, the following actions will ensue:

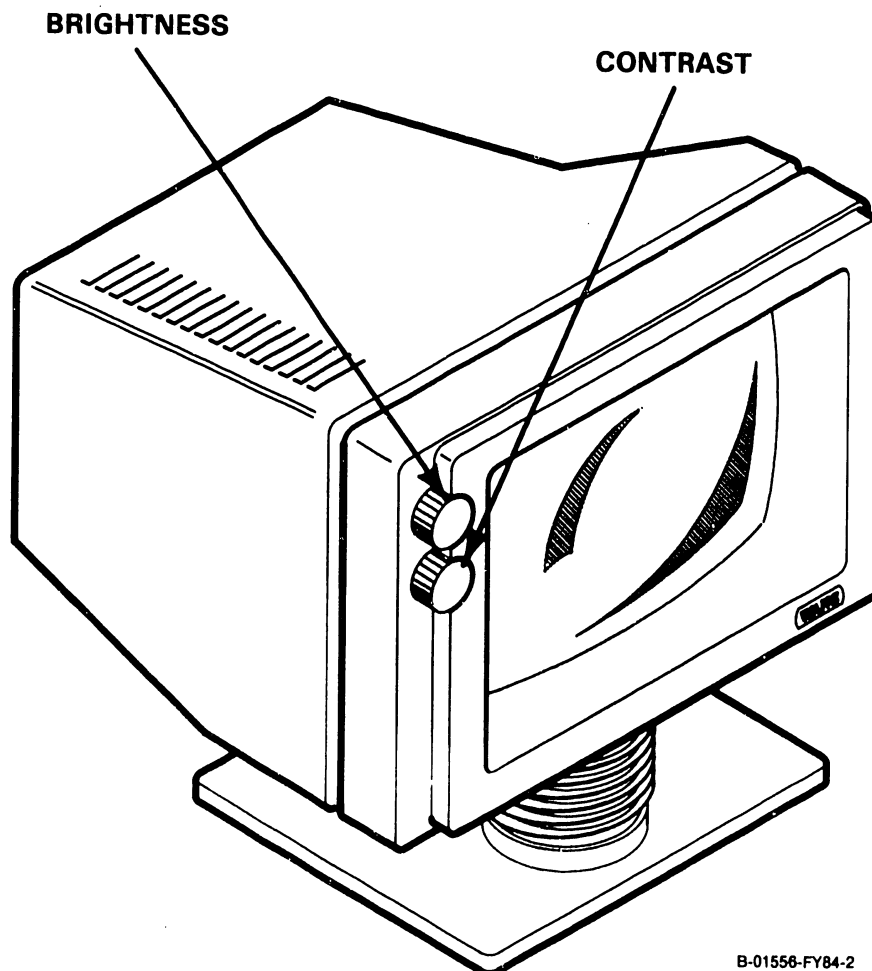
- o The workstation's internal fan starts
- o A short beep sounds
- o The BIT (Built-In Test) begins to run
- o the Keyboard LEDs will flash on and off

4.7 POST-INSTALLATION CHECKS, continued

4.7.3 4210 WORKSTATION TURN-ON, continued

- o The monitor will begin to display various test patterns, although this may not be visible if the CRT has not warmed up sufficiently. Refer to section 4.8 for details on the 4210 BIT.

After completing the BIT, the host CPU will execute the IPL (Initial Program Load) sequence. When the IPL is completed, the Monitor will display the LOGON screen. If the LOGON screen does not appear, adjust the Brightness and Contrast controls at the upper left edge of the Monitor front panel.



4.7 POST-INSTALLATION CHECKS, continued

4.7.3 4210 WORKSTATION TURN-ON, continued

NOTE: If the LOGON screen does not appear, refer to Chapter 8 of this manual for troubleshooting procedures.

After the LOGON screen has been obtained, the unit can be turned over to the customer.

4.7.4 4220 WORKSTATION TURN-ON

To initially turn on the 4220 Workstation, simply press 1 (on) on the I/O (on/off) switch on the front panel of the Electronics Base.

When power is first applied the following actions will ensue:

- o The workstation's internal fan starts
- o A short beep sounds
- o The BIT (Built-In Test) begins to run. (Refer to section 4.9 for details on the 4220 BIT.)
- o the Keyboard LEDs will flash on and off
- o The monitor will display the power-up screen (Figure 4-7), although this won't be visible until the CRT has warmed up sufficiently. (If the power-up screen does not appear, adjust the Brightness and Contrast controls at the upper left edge of the Monitor front panel.

4.7 POST-INSTALLATION CHECKS, continued

4.7.4 4220 WORKSTATION TURN-ON, continued

After successfully completing the BIT, the host CPU can execute the IPL (Initial Program Load) sequence once the connection from the host to the remote site has been activated. Chapter 3 details that procedure.

Once the host to remote site connection has been activated, the microcode is transferred to the workstation in 2k blocks, and a message on the first line of the CRT screen will display the microcode version that is being loaded (see Figure 4-7).

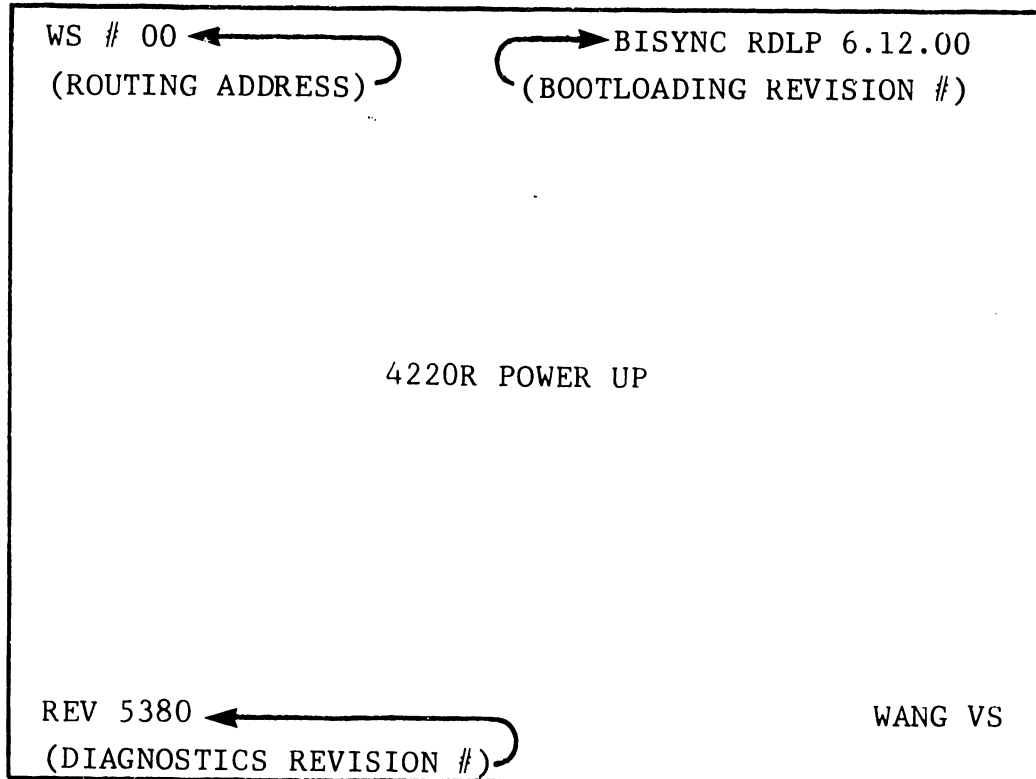
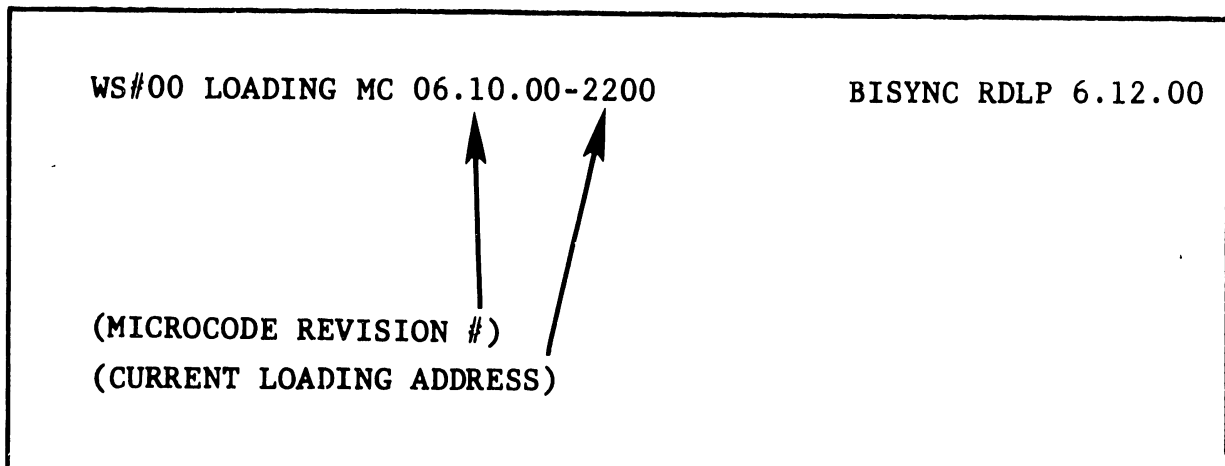


Figure 4-7a 4220 Power Up Screen

4.7 POST-INSTALLATION CHECKS, continued

4.7.4 4220 WORKSTATION TURN-ON, continued

During microcode down-loading:



Note: Entries enclosed in parentheses () are not displayed on the 4220 power up screen. They are shown here to identify screen entries only.

Figure 4-7b. 4220 Power Up Screen

The address of the current block being loaded is also shown. Additionally, the five Keyboard LEDs across the Keyboard function strip will count, in binary, the number of 2k block transfers that have been completed. The left-most LED is considered the MSB and the right-most LED, the LSB for the binary counting scheme.

If for any reason the host CPU fails to download the workstation microcode, the HELP key may be pressed to send an unsolicited interrupt to the host. The interrupt should start the downloading process.

4.7 POST-INSTALLATION CHECKS, continued

4.7.4 4220 WORKSTATION TURN-ON, continued

When the IPL is completed, the Monitor will display the LOGON screen.

NOTE: If either the power-up or LOGON screen does not appear, refer to Chapter 8 for troubleshooting procedures.

After the LOGON screen has been obtained, the unit can be turned over to the customer.

4.8 4210 POWER-UP DIAGNOSTICS

4.8.1 DESCRIPTION

The 4210 Workstation BIT program resides in a 4k PROM at location L10 on the 8264 CPU PCA. The BIT can be used for fault isolation to the board or subassembly level. In addition to the built-in test, a CRT display which aids in evaluating the CRT alignment is resident in the PROM.

The BIT runs certain tests automatically each time the workstation is powered on (section 4.8.4.1), and error messages resulting from failed tests are displayed on the Monitor CRT (section 4.8.6). Test status and results can also be determined by the state of the Keyboard LEDs (section 4.8.5).

In addition to the tests that run automatically at each power-up, other modes are included which are selected by entering the appropriate key-strokes after power-up of the workstation (sections 4.8.4.2 through 4.8.4.7).

4.8 4210 POWER-UP DIAGNOSTICS, continued

4.8.2 REVISION HISTORY AND ORDERING INFORMATION

Initial Release Date: April 11, 1983

Package Part Number: 195-2536-3

Documentation Revision: 93B8

Documentation Part Number: 760-1114-A

Software Revision: 53B8

Software Part Number: 702-0247-A

PROM Part Number: 378-8043-A

4.8.3 TESTS IN THE PROGRAM

The following tests are provided in the BIT:

<u>#</u>	<u>NAME OF TEST</u>	<u>HARDWARE TESTED</u>
2	Checksum test	Check diagnostic PROM
3	Parity gen. test	Parity generation and detection
4	MACHO (Main Mem.) test	Main memory
5	DART (SIO) test	DART
6	CRT RAM control test	CRT RAM access logic
7	MACHO (CRT Mem.) test	CRT memory
8	WP latch test	WP mode circuit
9	TC loopback test	TC drivers
A	Keyboard test	Keyboard
B	Video circuit test	Check video controllers

4.8.4 OPERATING INSTRUCTIONS

The following sections describe the currently supported modes of the 4210 Workstation BIT and how to implement them.

4.8 4210 POWER-UP DIAGNOSTICS, continued

4.8.4 OPERATING INSTRUCTIONS, continued

When power is initially applied to the unit, it will idle for two seconds waiting for the CANCEL key to be pressed. If CANCEL is not pressed within two seconds of power-up, normal power-up mode will be entered (section 4.8.4.1).

If CANCEL is pressed within two seconds of power-up, the operator will have an additional two seconds to press a key associated with one of the other modes (sections 4.8.4.2 through 4.8.4.7) thus entering that mode. If an additional key is not pressed to select one of the other BIT modes, normal power-up mode will be entered.

4.8.4.1 Normal Power-Up

The normal power-up sequence performs tests 2 through 8 as listed in section 4.8.3, essentially testing all circuitry visible to the CPU. If an error is found, testing stops and an error indication is given on the CRT (section 4.8.6) and on the Keyboard (section 4.8.5), and IPL is inhibited. If the unit is good, the host CPU will down-load workstation microcode and the LOGON screen will appear.

4.8.4.2 Skip BIT

This mode allows the unit to be used if it has a non-fatal hardware fault. No testing is performed, and the host processor can IPL the unit.

4.8.4 OPERATING INSTRUCTIONS, continued

4.8.4.2 Skip BIT, continued

To skip the BIT:

- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
- o Within two seconds after pressing CANCEL, press INDENT. The LOGON screen will appear.

This provision allows the normal power-up test to repeat indefinitely, as long as no errors are detected.

4.8.4.3. Loop-On-BIT

To loop on the BIT:

- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
- o Within two seconds after pressing CANCEL, press PAGE.

If an error is found, testing stops and an error indication is given on the CRT (section 4.8.6) and on the Keyboard (section 4.8.5). To cancel the test, shut unit off (1/0 switch to 0).

4.8.4.4 Video Test Pattern

This mode presents a pattern on the Monitor's CRT screen for verifying that the video controller logic in the Electronics Base is functional. The pattern can also be used to verify/correct the video alignment of the Monitor. This use of the

4.8.4 OPERATING INSTRUCTIONS, continued

4.8.4.4 Video Test Pattern, continued

pattern is discussed in Chapter 5 along with the video alignment procedure.

During the video pattern display, no testing is performed.

To display the BIT video pattern:

- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
- o Within two seconds after pressing CANCEL, press CENTER.
- o Press CENTER to step between the three available test patterns.

NOTE: While in this test, pressing the HELP key will release the unit to the operating system for IPL.

4.8.4.5 External Loopback

This test allows complete checkout of the telecommunications (TC) circuitry in the Electronics Base, thus allowing TC faults to be isolated between the workstation and external TC equipment. TC operation is presently not supported on the 4210 Workstation.

The test requires a standard RS-232 loopback connector (WLI P/N 420-1040) to be connected to the RS-232 connector on the rear panel of the Electronics Base unit. Once the test is initiated, it continuously loops and the pass count is

4.8.4 OPERATING INSTRUCTIONS, continued

4.8.4.5 External Loopback, continued

displayed on the second line of the CRT in hexadecimal notation. If an error is found, testing stops and an error indication is given on the CRT (section 4.8.6), and the Keyboard LEDs display the failed test number (section 4.8.5).

Additionally, the pass count freezes, displaying the number of times the test was run before the error occurred.

To run the external loopback test:

- o Install an RS-232C loopback connector (P/N 420-1040) on the RS-232C port on the rear of the workstation.
- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
- o Within two seconds after pressing CANCEL, press FORMAT.

To cancel a test, shut unit off (I/O switch to 0).

4.8.4.6 Keyboard Test

Selection of this test clears the CRT for display of the hexadecimal keycode of any key the operator presses. The test displays the keycode exactly as it is received.

4.8.4 OPERATING INSTRUCTIONS, continued

4.8.4.6 Keyboard Test, continued

To run the Keyboard test:

- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
- o Within two seconds after pressing CANCEL, press SEARCH.
- o Press any key and compare the CRT display with the hexadecimal code assigned to that key as shown in Table 4-1.

To cancel a test, shut unit off (I/O switch to 0).

4.8.4.7 Summary of Operator-Invoked BIT Functions

<u>FUNCTION</u>	<u>PRESS</u>
Skip BIT	CANCEL, INDENT
Loop on BIT	CANCEL, PAGE
Video Pattern	CANCEL, CENTER
External Loopback	CANCEL, FORMAT
Keyboard	CANCEL, SEARCH

4.8 4210 POWER-U. DIAGNOSTICS, continued

4.8.4 OPERATING INSTRUCTIONS, continued

Table 4-1. Universal Serial Keyboard
Hex (XY) Codes

CODE	COMMENT	CODE	COMMENT	CODE	COMMENT	CODE	COMMENT
00		20	Int'l	40	5 (P)	60	+ (P)
01	Query Response	21	Int'l	41	4 (P)	61	Prev
02		22	Int'l	42	Unusable	62	Insert
03		23	Int'l	43	Unusable	63	Unusable
04		24	Control	44	Return	64	=
05		25	2nd	45	'	65	0
06		26	Home	46	;	66	9
07		27	Unusable	47	L	67	8
08		28	S Cursor	48	K	68	7
09		29	N Cursor	49	J	69	6
0A		2A	.	4A	H	6A	5
0B		2B	Backspace	4B	G	6B	4
0C		2C	Space bar	4C	F	6C	3
0D		2D	W Cursor	4D	D	6D	2
0E		2E	E Cursor	4E	S	6E	1
0F		2F	-	4F	A	6F	Tab
10	3 (P)	30	2 (P)	50	7 (P)	70	Blank Key
11	Go to	31	1 (P)	51	Next	71	Sub/super
12	Cancel	32	Period (P)	52	Delete	72	Command
13	- (P)	33	Unusable	53	Execute	73	Move
14	Multiply (P)	34	0 (P)	54	Glossary	74	Copy
15	8 (P)	35	Rt. Shift	55]	75	Replace
16	9 (P)	36	Help	56	P	76	Search
17	6 (P)	37	/	57	O	77	Stop
18	Divide (P)	38	,	58	I	78	Note
19	Print	39	M	59	U	79	Merge
1A	Erase	3A	N	5A	Y	7A	Format
1B	Left Shift	3B	B	5B	T	7B	Dec Tab
1C	Return (P)	3C	V	5C	R	7C	Center
1D	Int'l	3D	C	5D	E	7D	Page
1E	Lock	3E	X	5E	W	7E	Indent
	1F		Back Tab	3F	Z	5F	Q
7F	Unused						

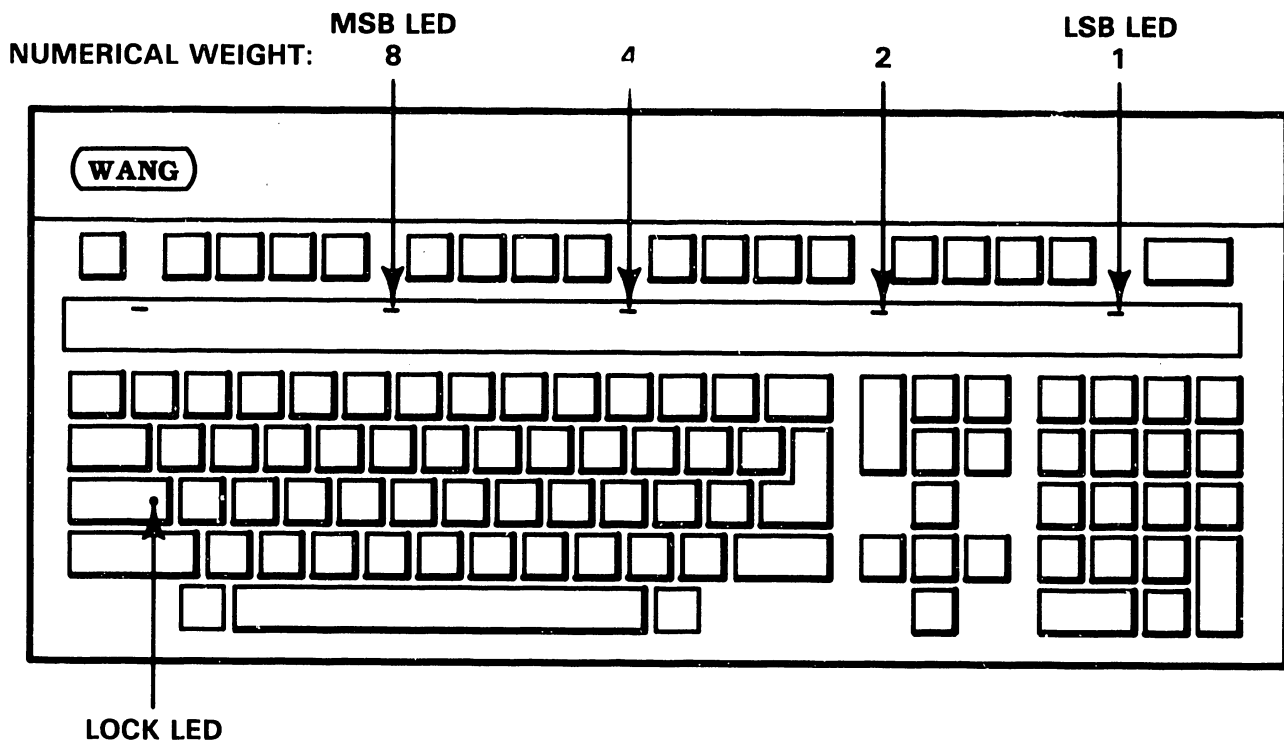
NOTES

- o Keys marked "Unusable" are in defined locations.
- o The codes 00 to 0F are reserved for control functions. These codes cannot be sent by pressing a key on the keyboard.
- o Codes marked "Int'l" are reserved for the International keyboard and exist only on the universal expanded keyboard.
- o The keyboard defaults to having the left and right shift keys generate make and break codes. The break code will be the x/y value of the depressed key OR-ed with an 80 bit.

4.8 4210 POWER-UP DIAGNOSTICS, continued4.8.5 KEYBOARD LED DISPLAYS

The Keyboard contains light-emitting diodes (LEDs) used by the BIT program for displaying BIT testing status. Five of these LEDs are between the program function/edit key row and the top key row of the standard typewriter keys. A sixth LED is built into the shift LOCK key.

Referring to the diagram below, the four right-most LEDs along the top of the Keyboard display, in binary, the number of the test being run. The rightmost LED is the LSB while the LED fourth from the right is the MSB in the binary numbering scheme. The test numbers are listed in section 4.8.3.



4.8 4210 POWER-UP DIAGNOSTICS, continued4.8.5 KEYBOARD LED DISPLAYS, continued

The table below outlines how the LEDs are used to convey the current status of the BIT program.

<u>BIT PROGRAM STATUS</u>	<u>LED ACTIVITY</u>
Initial 2-second delay after turn-on (waiting for CANCEL to be pressed):	LSB LED lit
Next 2-second delay after CANCEL is pressed (as above):	Left-most LED lit
During testing in any mode:	LEDs display test number in binary, lsb & msb per diagram above, see section 4.8.3 for test numbers
Error detected in any test:	LEDs display failed test number as above, LOCK LED blinks at approx. 1 - 2/second rate
All tests completed without error:	LEDs extinguished

4.8.6 CRT DISPLAY SCREEN STANDARDS

4.8.6.1 ID Field

Before testing starts and immediately following any test that modifies the screen, the BIT will clear the screen and display the ID field. The ID field will be displayed on the top line of the screen and has the following format:

R 5320 07 xx 08 xx

"R" indicates that this is the revision line, and that the digits following are the revision number of the BIT.

5320

is the 4-digit revision number of the BIT.

07 xx 08 xx

07 and 08 are the DIP switches readable by software on the CPU PCA and xx are the values read.

4.8.6.2 Messages for Errors Detected During BIT

When an error is detected during a BIT test, the screen will be cleared, the ID field displayed and the error message displayed with the following format:

4.8.6 CRT DISPLAY SCREEN STANDARDS, continued

4.8.6.2 Messages for Errors Detected During BIT

ERR xx BOARD bb cc dd ee hhll

"ERR" indicates an error has occurred and that the information on the rest of the line is error information.

xx BOARD

xx are the last two digits of the PC board number most likely to have caused the error. xx is "KE" if the keyboard is indicated as the failed item.

bb cc dd ee hhll

The contents of the Z80 B, C, D, E and HL registers, respectively. 'ee' represents error code where the first digit of the code is the test number failed (also shown on the Keyboard LEDs) and the second is the error number in the particular test.

4.8.6.3 Examples of CRT Displays

R 5320 07 00 08 05

Typical ID field showing revision of the BIT PROM, switch setting 00 for IN07 and 05 for IN08.

4.8.6 CRT DISPLAY SCREEN STANDARDS, continued

4.8.6.3 Examples of CRT Displays, continued

```
R 5320    07 00    08 05
```

```
ERR  KE BOARD 00 00 00 5B 0000
```

Typical BIT error message showing a failure of test 5, the keyboard test, and indicating a failure of the Keyboard.

```
R 5320    07 00    08 05
```

```
0001
```

```
ERR  63 BOARD 00 00 00 95 0000
```

Typical BIT error message showing a failure of test 9, the external loopback test, and indicating a failure of the 8263 board. The pass counter shows the failure occurred the first time through the test.

4.8.6 CRT DISPLAY SCREEN STANDARDS, continued

4.8.6.4 Memory Parity Errors Detected On-Line, continued

The workstation also checks memory parity during on-line operation. If a memory parity error is detected, control is passed to the BIT which freezes the contents of the screen. This is immediately evidenced by the cursor which stops flashing. Additionally, the LOCK LED on the Keyboard blinks at approximately 1 - 2/second.

4.9 4220 POWER-UP DIAGNOSTICS

4.9.1 DESCRIPTION

The 4220 Workstation BIT program resides in a 4k PROM at location L37 on the 8277 Remote Workstation Electronics PCA. The BIT can be used for fault isolation to the board or subassembly level. In addition to the built-in test; a CRT display which aids in evaluating the character attribute logic is resident in the PROM.

The BIT runs certain tests automatically each time the workstation is powered on (section 4.9.4.1), and error messages resulting from failed tests are displayed on the Monitor CRT (section 4.9.6). Test status and results can also be determined by the state of the Keyboard LEDs (section 4.9.5). Additionally a diagnostic LED on the Remote Workstation Electronics PCA indicates the status of the diagnostic testing: in progress, passed or failed (section 4.9.7).

4.9 4220 POWER-UP DIAGNOSTICS, continued

4.9.1 DESCRIPTION, continued

In addition to the tests that run automatically at each power-up, other modes are included which are selected by entering the appropriate key-strokes after power-up of the workstation (sections 4.9.4.2 through 4.9.4.8).

Also included is a special burn-in mode which automatically loops through the power-up tests for as long as the unit is powered on and passes the tests (section 4.9.4.10).

4.9.2 REVISION HISTORY AND ORDERING INFORMATION

Initial Release Date: August 10, 1983
 Package Part Number: 195-2700-3
 Documentation Revision: 9380
 Documentation Part Number: 760-1193
 Software Revision: 5380
 Software Part Number: 702-0271
 PROM Part Number: 378-8047

4.9.3 TESTS IN THE PROGRAM

The following tests are provided in the BIT:

<u>NO.</u>	<u>NAME OF TEST</u>	<u>HARDWARE TESTED</u>
01	Initialization	Keyboard SIO Interface
02	PROM Checksum	Diagnostic and IPL PROMs
03	Parity generating test	Parity generation and detection

4.9 4220 POWER-UP DIAGNOSTICS, continued

4.9.3 TESTS IN THE PROGRAM, continued

<u>NO.</u>	<u>NAME OF TEST</u>	<u>HARDWARE TESTED</u>
04	Main memory test	Main memory (8 kB to 64 kB)
05	CRT memory	CRT memory (56 kB to 64 kB)
06	Low memory test	Main memory (0 to 8 kB)
07	CTC timer operation	CTC
08	CTC interrupt priority	CTC
09	Keyboard asynch. port	Keyboard asynchronous serial line
0A	Main RS-232C port	Data transfer using polling (internal loopback)
0B	Main RS-232C port	Data transfer using interrupts (internal loopback)
0C	Main RS-232C port	Data transfer using polling (external loopback)
0D	Main RS-232C port	Data transfer using interrupts (external loopback)
0E	Aux. RS-232C port	Data transfer using polling (external loopback)
0F	Aux. RS-232C port	Data transfer using interrupts (external loopback)
10	Attributes test	Video Monitor
11	Keyboard test	Keyboard

Note: Tests 10 and 11 are transparent to the operator, and do not display an error message.

4.9.4 OPERATING INSTRUCTIONS

The following sections describe the currently supported modes of the 4220 Workstation BIT and how to implement them.

4.9 4220 POWER-UP DIAGNOSTICS, continued

4.9.4 OPERATING INSTRUCTIONS, continued

When power is initially applied to the unit, it will idle for two seconds waiting for the CANCEL key to be pressed. If CANCEL is not pressed within two seconds of power-up, normal power-up mode will be entered (section 4.9.4.1).

If CANCEL is pressed within two seconds of power-up, the operator will have an additional two seconds to press a key associated with one of the other modes (4.9.4.2 through 4.9.4.8), thus entering that mode. If an additional key is not pressed to select one of the other BIT modes, normal power-up mode will be entered.

A special burn-in mode can be entered by installing loopback connectors on the Keyboard connector the Main TC connector and the Auxiliary TC connector. This mode loops on the power-up tests as long as the unit is powered on and passes the tests (section 4.9.4.10).

4.9.4.1 Normal Power-Up

The normal power-up sequence performs the tests listed in section 4.9.3, with the exception of the external loopback tests, the character attribute test and the Keyboard test, thus testing all circuitry visible to the CPU. If an error is found, testing stops and an error indication is given on the CRT (section 4.9.6) and on the Keyboard (section 4.9.5), the Keyboard emits three beeps and IPL is inhibited. If the

4.9.4 OPERATING INSTRUCTIONS, continued

4.9.4.1 Normal Power-Up, continued

unit is good and the host to workstation connection is active, the host CPU will down-load workstation microcode and the LOGON screen will appear.

4.9.4.2 Skip BIT

This mode allows the unit to be used if it has a non-fatal hardware fault. No testing is performed, and the host processor can IPL the unit.

To skip the BIT:

- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
- o Within two seconds after pressing CANCEL, press INDENT. Microcode down-loading will commence and then the LOGON screen will appear.

4.9.4.3 Loop on BIT

This provision allows the normal power-up test to repeat indefinitely, as long as no errors are detected. This mode does not run an external loopback test on either the Main TC port or the Auxiliary TC port. A loop count is flashed briefly on the CRT after each pass through the test program.

4.9.4 OPERATING INSTRUCTIONS, continued

4.9.4.3 Loop on BIT, continued

To loop on the BIT:

- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
- o Within two seconds after pressing CANCEL, press PAGE.

If an error is found, testing stops and an error indication is given on the CRT (section 4.9.6) and on the Keyboard (section 4.9.5) and the Keyboard emits three beeps. To cancel the test, shut unit off (I/O switch to 0).

4.9.4.4 Keyboard SIO Test

This test verifies operation of the keyboard asynchronous port using both polling and vectored interrupt modes to transfer data. The test runs continuously once selected. The Keyboard is not required to be connected for the test and can be either connected or not without any effect on the test. No indication is given on the CRT while the test is running.

To run the Keyboard SIO test:

- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
- o Within two seconds after pressing CANCEL, press NOTE.

4.9.4 OPERATING INSTRUCTIONS, continued

4.9.4.4 Keyboard SIO Test, continued

If an error is found, testing stops and an error indication is given on the CRT (section 4.9.6) and on the Keyboard (section 4.9.5) and the Keyboard emits three beeps. To cancel the test, shut unit off (I/O switch to 0).

4.9.4.5 Main SIO Test

This test exercises channels A and B of the main SIO using both an internal and external loopback type of test. Full checkout of the main SIO is thus possible, allowing TC faults to be isolated to either the workstation or the associated modem. The test requires the installation of an external loopback connector in place of the modem on the Main TC port on the rear of the workstation.

Note that this test will indicate a failure if the Sync/Async jumper J11 for the main SIO is set for asynchronous operation. The error code will be 'C6.' Since the jumper should be in the synchronous position for proper operation with the host CPU, the test should run normally without having to reset the jumper at J11 to facilitate the test. (Section 4.5.1.1.)

To run the main SIO test:

- o Install an RS-232C loopback connector (P/N 420-1040) on the Main TC port on the rear of the workstation.

4.9.4 OPERATING INSTRUCTIONS, continued

4.9.4.5 Main SIO Test

- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and press CANCEL.
- o Within two seconds after pressing CANCEL, press FORMAT.

If an error is found, testing stops and an error indication is given on the CRT (section 4.9.6) and on the Keyboard (section 4.9.5) and the Keyboard emits three beeps. To cancel the test, shut unit off (1/0 switch to 0).

4.9.4.6 Auxiliary SIO Test

This test exercises external TC loopback circuitry only and requires an RS-232C loopback connector on the Auxiliary TC port on the rear of the workstation. The test isolates faults to either the workstation or the associated modem.

To run the auxiliary SIO test:

- o Install an RS-232C loopback connector (P/N 420-1040) on the Auxiliary TC port on the rear of the workstation.
- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
- o Within two seconds after pressing CANCEL, press MERGE.

If an error is found, testing stops and an error indication is given on the CRT (section 4.9.6) and on the Keyboard (section 4.9.5). To cancel the test, shut unit off (1/0 switch to 0).

4.9.4 OPERATING INSTRUCTIONS, continued

4.9.4.7 Character Attributes Test

This test exercises the video controller logic on the Remote Workstation Electronics board and on the Monitor board. Each line of the CRT screen is filled with hexadecimal characters and displays one of the available character attributes, normal, underline, blink, reverse video, high intensity, left horizontal bar, vertical bar, or right horizontal bar. Both primary and secondary fonts are exercised. No internal testing is performed with this test and no error messages are possible. Observe the screen and compare it with Figure 4-8 for diagnostic purposes.

```

1 UNDERLINE UNDERLINE UNDERLINE UNDERLINE UNDER
2 BLINK BLINK BLINK BLINK BLINK BLINK BLINK BLI
3 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
4 REVERSE VIDEO REVERSE VIDEO REVERSE VIDEO REV
5 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
6 HIGH INTENSITY HIGH INTENSITY HIGH INTENSITY
7 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
8 LEFT HORIZONTAL BAR LEFT HORIZONTAL BAR LEFT
9 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
10 VERTICAL BAR VERTICAL BAR VERTICAL BAR VERTIC
11 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
12 RIGHT HORIZONTAL BAR RIGHT HORIZONTAL BAR RIG
13 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
14 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
15 BLINK BLINK BLINK BLINK BLINK BLINK BLINK BLI
16 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
17 REVERSE VIDEO REVERSE VIDEO REVERSE VIDEO REV
18 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
19 HIGH INTENSITY HIGH INTENSITY HIGH INTENSITY
20 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
21 LEFT HORIZONTAL BAR LEFT HORIZONTAL BAR LEFT
22 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
23 VERTICAL BAR VERTICAL BAR VERTICAL BAR VERTIC
24 NORMAL NORMAL NORMAL NORMAL NORMAL NORMAL NOR
25 RIGHT HORIZONTAL BAR RIGHT HORIZONTAL BAR RIG

```

Note: Lines 1 through 12 = primary font
 Lines 13 through 25 = repeat of lines 1 through 12 in secondary font

Figure 4-8. 4220 Character Attributes Display Screen

4.9.4 OPERATING INSTRUCTIONS, continued

4.9.4.7 Character Attributes Test, continued

To run the character attributes test:

- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
- o Within two seconds after pressing CANCEL, press CENTER.

When the CRT is sufficiently warmed up, the hexadecimal characters on each line should have the attributes shown in Figure 4-8. To cancel the test, shut unit off (I/O switch to 0).

4.9.4.8 Keyboard Test

Selection of this test clears the CRT for display of the hexadecimal keycode of any key the operator presses. The test displays the keycode exactly as it is received.

To run the Keyboard test:

- o Power on the unit, wait for the LED adjacent to the CANCEL key to light and immediately press CANCEL.
- o Within two seconds after pressing CANCEL, press SEARCH.
- o Press any key and compare the CRT display with the hexadecimal code assigned to that key as shown in Table 4-1.

To cancel the test, shut unit off (I/O switch to 0).

4.9.4 OPERATING INSTRUCTIONS, continued

4.9.4.9 Summary of Operator-Invoked BIT Functions

<u>FUNCTION</u>	<u>PRESS</u>
Skip BIT	CANCEL, INDENT
Loop on BIT	CANCEL, PAGE
Keyboard SIO Test	CANCEL, NOTE
Main SIO Test	CANCEL, FORMAT
Auxiliary SIO Test	CANCEL, MERGE
Attributes Test	CANCEL, CENTER
Keyboard Test	CANCEL, SEARCH

4.9.4.10 Burn-In Mode

The burn-in mode provides a complete test of all serial input/output circuitry and also causes the loop on BIT function to be selected automatically. Upon power-up, the program looks at the Keyboard SIO port and, if it senses a loopback connection (pins 2 and 3 connected), it assumes that the Main and Auxiliary TC ports also have loopback connectors installed. It then proceeds with the burn-in mode tests, looping through all tests as long as power is applied to the unit and it passes the tests. A loop count is flashed briefly on the CRT after each pass through the test program.

To select the burn-in mode, proceed as follows:

- o Install loopback connectors on the Main and Auxiliary TC ports on the rear of the Electronics Base. The part number for the RS-232C loop-back connector is 420-1040.
- o Connect pins 2 and 3 of the Keyboard connector. Refer to Figure 8-3 for a diagram and pin assignments of this connector.

4.9.4 OPERATING INSTRUCTIONS, continued

4.9.4.10 Burn-In Mode, continued

- o Set the Main and Auxiliary TC port baud rates to 9600 by setting SW2 sections 12, 13 and 14 and SW1 sections 1, 2 and 3 as shown below:

MAIN TC PORT		AUXILIARY TC PORT	
<u>Switch SW2</u>	<u>Position</u>	<u>Switch SW1</u>	<u>Position</u>
Sec. 12	DCWN	Sec. 1	DOWN
Sec. 13	UP	Sec. 2	UP
Sec. 14	DOWN	Sec. 3	DOWN

- o Initiate operation of the test program by powering on the unit under test.

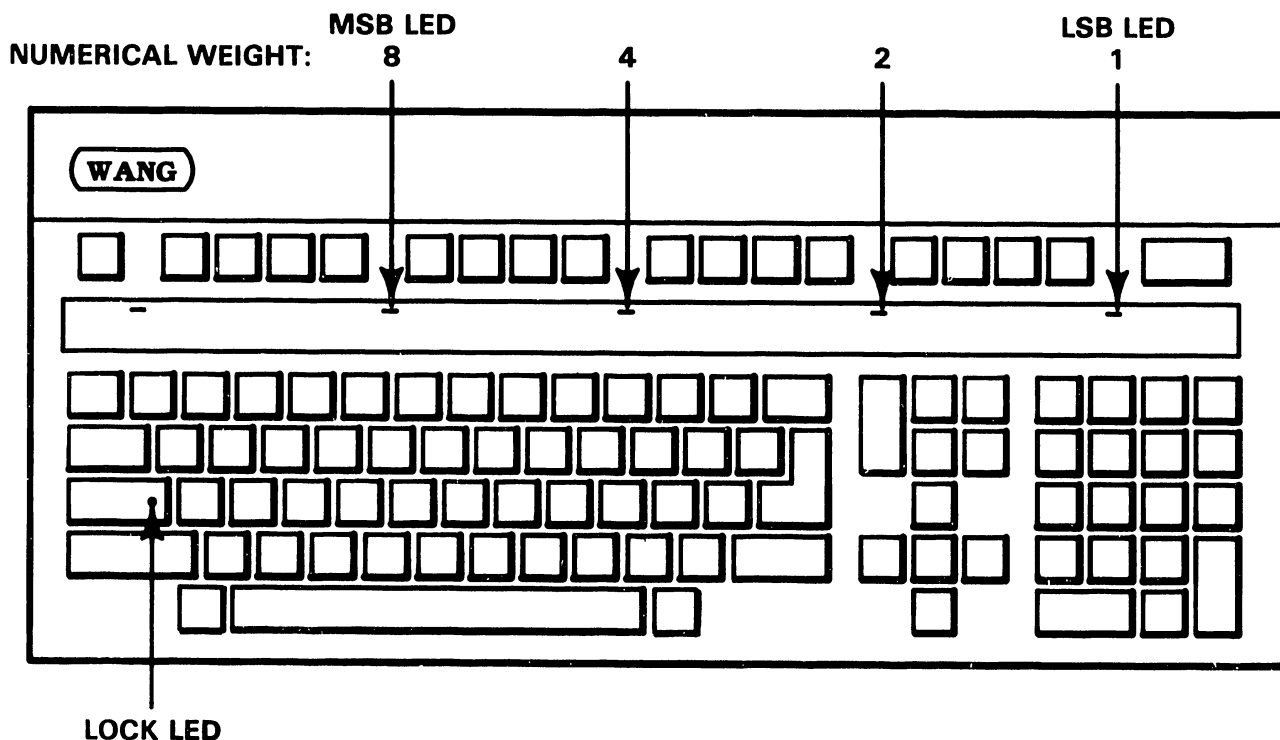
If an error is found, testing stops and an error indication is given on the CRT (section 4.9.6) and on the Keyboard (section 4.9.5) and the Keyboard emits three beeps. To cancel the test, shut unit off (I/O switch to 0).

4.9 4220 POWER-UP DIAGNOSTICS, continued

4.9.5 KEYBOARD LED DISPLAYS

The Keyboard contains light-emitting diodes (LEDs) used by the BIT program for displaying BIT testing status. Five of these LEDs are between the program function/edit key row and the top key row of the standard typewriter keys. A sixth LED is built into the shift LOCK key.

Referring to the diagram below, the four right-most LEDs along the top of the Keyboard display, in binary, the number of the test being run. The rightmost LED is the LSB while the LED fourth from the right is the MSB in the binary numbering scheme. The test numbers are listed in section 4.9.3.



4.9 4220 POWER-UP DIAGNOSTICS, continued4.9.5 KEYBOARD LED DISPLAYS, continued

The table below outlines how the LEDs are used to convey the current status of the BIT program.

<u>BIT PROGRAM STATUS</u>	<u>LED ACTIVITY</u>
Initial 2-second delay after turn-on (waiting for CANCEL to be pressed):	LSB LED lit
Next 2-second delay after CANCEL is pressed (as above):	No LEDs lit
During testing in any mode:	LEDs display test number in binary, lsb & msb per diagram above, see section 4.9.3 for test numbers
Error detected in any test:	LEDs display failed test number as above
All tests completed without error:	LEDs extinguished

4.9.6 CRT DISPLAY SCREEN STANDARDS4.9.6.1 CRT Display During Testing

During normal testing, no information is displayed on the CRT screen. Action of the BIT can be determined by the Keyboard LEDs as they display the number of the test currently running (section 4.9.5) and also by the state of the diagnostic LED on the 8277 PCA (section 4.9.7).

4.9.6 CRT DISPLAY SCREEN STANDARDS, continued

4.9.6.1 CRT Display During Testing, continued

The CRT will display information in the event of a detected error as described in the next section. Other than errors, the only CRT displays are the pass count when in the loop on BIT mode, the character attributes when in the attribute test and the keycodes when in the keycode test.

4.9.6.2 Messages for Errors Detected During BIT

When an error is detected during a BIT test, the error message will be displayed with the following format:

```
ERR 8277 BOARD aa bb dd ee hhll
```

"ERR" indicates an error has occurred and that the information on the rest of the line is error information.

```
8277 BOARD
```

8277 is the 4220 Workstation PC board number.

```
aa bb dd ee
```

aa represents bad data (data received). bb represents good data (data expected). dd represents the difference data (XOR of good and bad data). ee represents error code in hex where the first digit of the code is the test number failed (also shown on the Keyboard LEDs) and the second is the error number in the particular test. Table 4-2 gives a complete list of error codes and their meaning.

4.9.6 CRT DISPLAY SCREEN STANDARDS, continued

4.9.6.2 Messages for Errors Detected During BIT,
continued

hh11

hh11 represents the address in hex where a memory test error has occurred.

Note that if a specific entry on the error line is not applicable to a particular test, the contents of that entry will be zero.

Table 4-2. 4220 BIT Error Codes

ERROR CODE	DESCRIPTION
11	No character in Keyboard Receive Buffer
12	Keyboard SIO data error
21	Diagnostic PROM checksum error
22	IPL PROM checksum error
31	Memory data error
32	Unexpected NMI interrupt
33	No NMI interrupt
41	Main Mem. (8 to 64 kB) data error after memory fill
42	Main Mem. (8 to 64 kB) data error after single cell write
51	CRT Memory data error after memory fill
52	CRT Memory data error after single cell write
61	Main Mem. (0 to 8 kB) data error after memory fill
62	Main Mem. (0 to 8 kB) data error after single cell write
71	CTC Timer interrupt occurred too soon
72	No CTC Timer interrupt
81	No CTC priority interrupt for Channel 0

4.9.6 CRT DISPLAY SCREEN STANDARDS, continued
 4.9.6.2 Messages for Errors Detected During BIT,
 continued

Table 4-2. 4220 BIT Error Codes
 continued

ERROR CODE	DESCRIPTION
82	Unexpected CTC priority interrupt for Channel 3
83	No CTC priority interrupt for Channel 0
84	No CTC priority interrupt for Channel 1
85	Unexpected CTC priority interrupt for Channel 3
86	No CTC priority interrupt for Channel 0
87	No CTC priority interrupt for Channel 2
88	Unexpected CTC priority interrupt for Channel 3
89	No CTC priority interrupt for Channel 0
8A	No CTC priority interrupt for Channel 3
91	Keyboard Transmit Buffer not empty (TBE)
92	Character in Keyboard Receive Buffer
93	Keyboard Transmit Buffer not empty (TBE)
94	No character in Keyboard Receive Buffer (RCA)
95	Keyboard SIO data error
96	No Keyboard Transmit Buffer Empty (TBE) interrupt
97	No Keyboard Transmit Buffer Empty (TBE) interrupt
98	No Keyboard Receive Character Available (RCA) interrupt
9A	Keyboard SIO data error
A1	Main SIO Transmit Interrupt Pending active (internal)
A2	Main SIO Receive Interrupt Pending active (internal)

4.9.6 CRT DISPLAY SCREEN STANDARDS, continued
 4.9.6.2 Messages for Errors Detected During BIT,
 continued

Table 4-2. 4220 BIT Error Codes
 continued

ERROR CODE	DESCRIPTION
A3	Main SIO Receiver not in "hunt" mode (intern.)
A4	Main SIO Transmit Buffer not empty (TBE) (intern.)
A5	No "sync" characters from Main SIO Transmit port (internal)
A6	Main SIO Receiver remained in "hunt" mode (intern.)
A7	Main SIO Transmit Buffer not empty (TBE) (intern.)
A8	No character in Main SIO Receive Buffer (intern.)
A9	"Sync" character in Main SIO Receive Buffer (intern.)
AA	Main SIO data error (intern.)
B1	No Main SIO External Status interrupt (intern.)
B2	No Main SIO Status Affects Vector interrupt (SAV) (intern.)
B3	No Main SIO Transmit Buffer Empty (TBE) interrupt (intern.)
B4	No Main SIO Received Character Available (RCA) interrupt (intern.)
B5	"Sync" character received in Main SIO Receive Buffer (intern.)
B6	Main SIO data error (intern.)
B7	No Main SIO Receive Overrun interrupt (intern.)

4.9.6 CRT DISPLAY SCREEN STANDARDS, continued

4.9.6.2 Messages for Errors Detected During BIT,
continuedTable 4-2. 4220 BIT Error Codes
continued

ERROR CODE	DESCRIPTION
C1	Main SIO Transmit Interrupt Pending active (external)
C2	Main SIO Receive Interrupt Pending active (external)
C3	Main SIO Receiver not in "hunt" mode (external)
C4	Main SIO Transmit Buffer not empty (TBE) (external)
C5	No "sync" characters from Main SIO Transmit port (external)
C6	Main SIO Receiver remained in "hunt" mode (external)
C7	Main SIO Transmit Buffer not empty (TBE) (external)
C8	No character in Main SIO Receive Buffer (external)
C9	"Sync" character in Main SIO Receive Buffer (external)
CA	Main SIO data error (external)
D1	No Auxiliary SIO External Status interrupt (external)
D2	No Auxiliary SIO Status Affects Vector interrupt (external)
D3	No Auxiliary SIO Transmit Buffer Empty (TBE) interrupt (external)
D4	No Auxiliary SIO Received Character Available (RCA) interrupt (external)

4.9.6 CRT DISPLAY SCREEN STANDARDS, continued
 4.9.6.2 Messages for Errors Detected During BIT,
 continued

Table 4-2. 4220 BIT Error Codes
 continued

ERROR CODE	DESCRIPTION
D5	"Sync" character received in Auxiliary SIO Receive Buffer (external)
D6	Auxiliary SIO data error (external)
D7	No Auxiliary SIO Receive Overrun interrupt (external)
E1	Auxiliary SIO Transmit Interrupt Pending active (external)
E2	Auxiliary SIO Receive Interrupt Pending active (external)
E3	Auxiliary SIO Receiver not in "hunt" mode (external)
E4	Auxiliary SIO Transmit Buffer not empty (TBE) (external)
E5	No "sync" characters from Auxiliary SIO Transmit port (external)
E6	Auxiliary SIO Receiver remained in "hunt" mode (external)
E7	Auxiliary SIO Transmit Buffer not empty (TBE) (external)
E8	No character in Auxiliary SIO Receive Buffer (external)
E9	"Sync" character in Auxiliary SIO Receive Buffer (external)
EA	Auxiliary SIO data error (external)
F1	No Auxiliary SIO External Status interrupt (external)

- 4.9.6 CRT DISPLAY SCREEN STANDARDS, continued
 4.9.6.2 Messages for Errors Detected During BIT,
 continued

Table 4-2. 4220 BIT Error Codes
 continued

ERROR CODE	DESCRIPTION
F2	No Auxiliary SIO Status Affects Vector interrupt (SAV) (external)
F3	No Auxiliary SIO Transmit Buffer Empty (TBE) interrupt (external)
F4	No Auxiliary SIO Received Character Available (RCA) interrupt (external)
F5	"Sync" character received in Auxiliary SIO Receive Buffer (external)
F6	Auxiliary SIO data error (external)
F7	No Auxiliary SIO Receive Overrun interrupt (external)

4.9.6.3 Examples of CRT Displays

01

Position and format of pass counter displayed when loop on BIT mode is used.

4.9.6 CRT DISPLAY SCREEN STANDARDS, continued

4.9.6.3 Examples of CRT Displays, continued

```
ERR 8277 BOARD 00 00 00 C6 0000
```

Typical BIT error message showing a failure of test C, the Main TC port test, indicating a failure of the external loopback test on this port.

4.9.6.4 Memory Parity Errors

The workstation checks memory parity during the built-in test and during on-line operation. Memory parity errors result in the generation of a nonmaskable interrupt to the Z-80.

If a memory parity error is detected, and the source of the parity error is the test program, the number of the test where the NMI originated will be displayed on the Keyboard LEDs and the LOCK LED will blink.

If the source of the NMI interrupt is from the operating system, all Keyboard LEDs will be turned on and the LOCK LED will blink.

Also, in both cases the contents of the CRT screen will be underlined. The diagnostic LED on the 8277 board will be lit to indicate the failing status of the unit.

4.9 4220 POWER-UP DIAGNOSTICS, continued

4.9.7 DIAGNOSTIC LED

The diagnostic LED gives a visual indication of the status of the BIT, whether in progress, passed or failed. The LED can be viewed through the ventilation slots in the Electronics Base bottom, on the left side toward the front of the unit. The code is as follows:

LED Blinking = BIT is in progress

LED Off = BIT was passed

LED On = BIT was failed

CHAPTER

5

**MAINT-
ENANCE**

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CHAPTER 5 MAINTENANCE

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CHAPTER 5
PREVENTIVE AND CORRECTIVE MAINTENANCE

This chapter contains routine maintenance procedures required to align and adjust the 4210 and 4220 Workstations for best performance (section 5.3). Removal and reinstallation procedures are also included in sections 5.4, 5.5 and 5.6. Section 5.7 details switch settings for the CPU PCA in the 4210 Workstation, and the 4210/4220 Keyboard.

5.1 REQUIRED TOOLS, TEST EQUIPMENT AND ACCESSORIES

The following items are required to carry out the preventive and corrective maintenance activities described in this chapter or elsewhere in this manual.

<u>DESCRIPTION</u>	<u>PART NUMBER</u>
Wang CE Tool Kit	726-9401
Digital Multimeter	727-0119

5.2 PREVENTIVE MAINTENANCE

Preventive Maintenance should be performed on a regular basis to help prevent workstation equipment failures. The suggested plan for regular preventive maintenance follows.

5.2.1 ROUTINE SEMI-ANNUAL MAINTENANCE OR DURING AN UNSCHEDULED TROUBLE CALL

5.2.1.1 Cleaning

Remove power from the workstation and clean as follows:

- o Dust keyboard with a soft-bristled brush.
- o Clean the CRT screen, using a good quality glass cleaner and a soft, lint-free cloth.
- o Wipe exterior of workstation components, using a damp, lint-free cloth.
- o Vacuum dust from the ventilating slots in the Monitor cover and the Electronics Base cover, and from around the fan at the rear of the Electronics Base.

5.2.1.2 Checks and Adjustments

Power-on the workstation and proceed as follows:

- o Check the workstation power supply voltages, as described in section 5.3.1.
- o Check for proper character display. Perform the Monitor Alignment Procedure (section 5.3.2), if required.

5.2.1.3 Diagnostics

A routine check of the workstation internal functions is automatically performed by the Built-In Test (BIT) diagnostics each time the unit is powered up.

5.2.2 ANNUAL MAINTENANCE (SEMI-ANNUAL IN AN INDUSTRIAL ENVIRONMENT)

Check all cables and connectors for proper seating. Loose or damaged connectors should be repaired or replaced.

5.3 CORRECTIVE MAINTENANCE

This section contains adjustment and alignment procedures required in the units of the 4210 and 4220 Workstations. The tools, test equipment and accessories required for these procedures are listed in section 5.1. To access the components as directed in the procedures, refer to the removal and reinstallation procedures in sections 5.4, 5.5 or 5.6. Adjustment/alignment procedures included in this section are listed below.

<u>SECTION</u>	<u>PROCEDURE</u>
5.3.1	Voltage Checks
5.3.2	Monitor Alignment

5.3.1 VOLTAGE CHECKS

The 4210/4220 Workstation is powered by a single switching power supply in the Electronics Base unit which supplies +5 and +12 Vdc to the workstation components. In the 4210, a series-regulator device on the 8264 CPU board derives a -5 Vdc supply from the -12 Vdc power supply output. An identical device resides on the 8263 Bit Map PCA in the 4210, providing a -5 Vdc supply for that PCA. In the 4220, no -5 volt supply is used. To check the internal power supplies, proceed as described in the following sections.

5.3.1 VOLTAGE CHECKS, continued

5.3.1.1 4210 Voltage Checks

NOTE: No adjustments are to be performed in the field in the switching Power Supply. If the voltage outputs are not within tolerance, replace the power supply.

The table below lists voltages and respective tolerances as well as test point locations for the 4210 Workstation. Measure the following voltages on the 8264 CPU PCA, grounding your meter to J2-6 on that board in the 4210 Workstation.

<u>DC VOLTAGE</u>	<u>210-8264 BOARD TEST POINT</u>	<u>ACCEPTABLE TOLERANCE</u>
+ 5 Vdc	J2-3	+ 4.9 - + 5.1 Vdc
- 5 Vdc	VR1-2	- 4.9 - - 5.1 Vdc
+12 Vdc	J2-1	+11.8 - +12.2 Vdc
-12 Vdc	J2-8	-11.4 - -12.6 Vdc

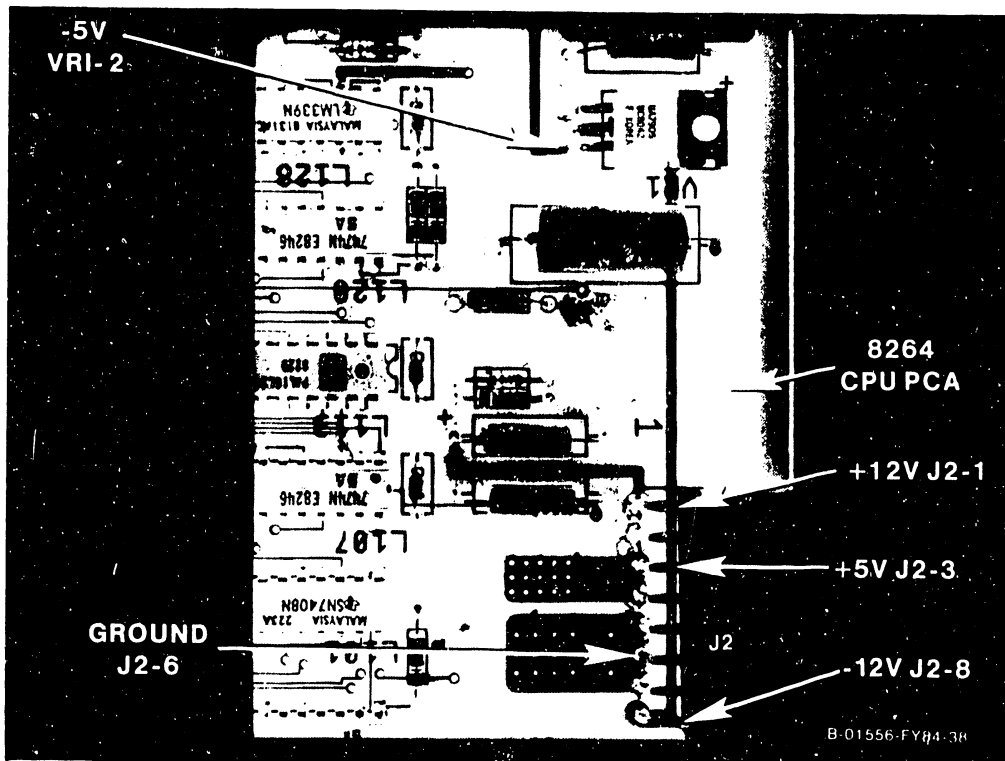


Figure 5-1. 4210 Power Supply Checks

5.3.1 VOLTAGE CHECKS, continued

5.3.1.2 4220 Voltage Checks

NOTE: No adjustments are to be performed in the field in the switching Power Supply. If the voltage outputs are not within tolerance, replace the power supply.

The table below lists voltages and respective tolerances as well as test point locations for the 4220 Workstation. Measure the following voltages on the 8264 CPU PCA, grounding your meter to J5-6 on that board in the 4210 Workstation.

DC VOLTAGE	210-827/ BOARD TEST POINT	ACCEPTABLE TOLERANCE
+ 5 Vdc	J5-4	+ 4.9 - + 5.1 Vdc
+12 Vdc	J5-1	+11.8 - +12.2 Vdc
-12 Vdc	J5-8	-11.4 - -12.6 Vdc

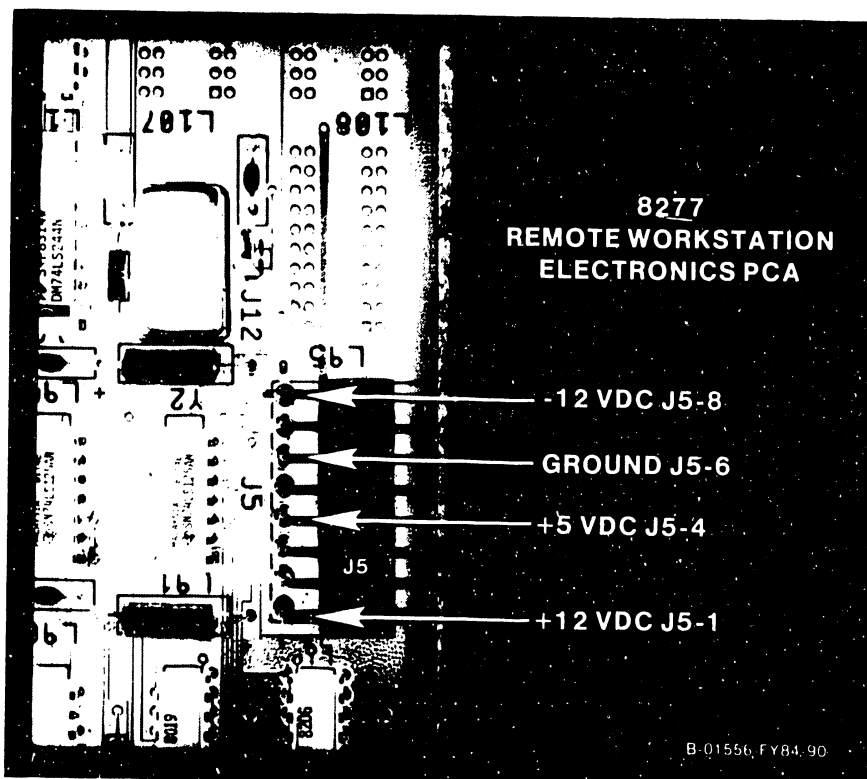


Figure 5-2. 4220 Power Supply Checks

5.3 CORRECTIVE MAINTENANCE, continued

5.3.2 MONITOR ALIGNMENT, DESCRIPTION OF SOFTWARE SUPPORT

Monitor alignment is carried out using either the Built-In Test (BIT) video pattern or with the on-line VS diagnostic test operating system (DTOS) series of test patterns. Monitor alignment with the BIT pattern allows for all adjustments except horizontal and vertical linearity. Alternatively, the DTOS, with its available grid and circle patterns, allows for the linearity to be set precisely and visually checked. Monitor alignment using BIT support is shown in section 5.3.3 while section 5.3.4 details the Monitor alignment using DTOS support.

5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT

The following alignment of the 4210/4220 Monitor is carried out with the support of the video pattern in the Built-In Test. Please note that the procedure does not cover Monitor linearity adjustments and that a complete alignment can be obtained with the support of the VS DTOS package, as detailed in section 5.3.4.

Pre-Alignment Conditions

- o Remove cover from Monitor (section 5.5).
- o Connect dual cable between Monitor and Electronics Base.

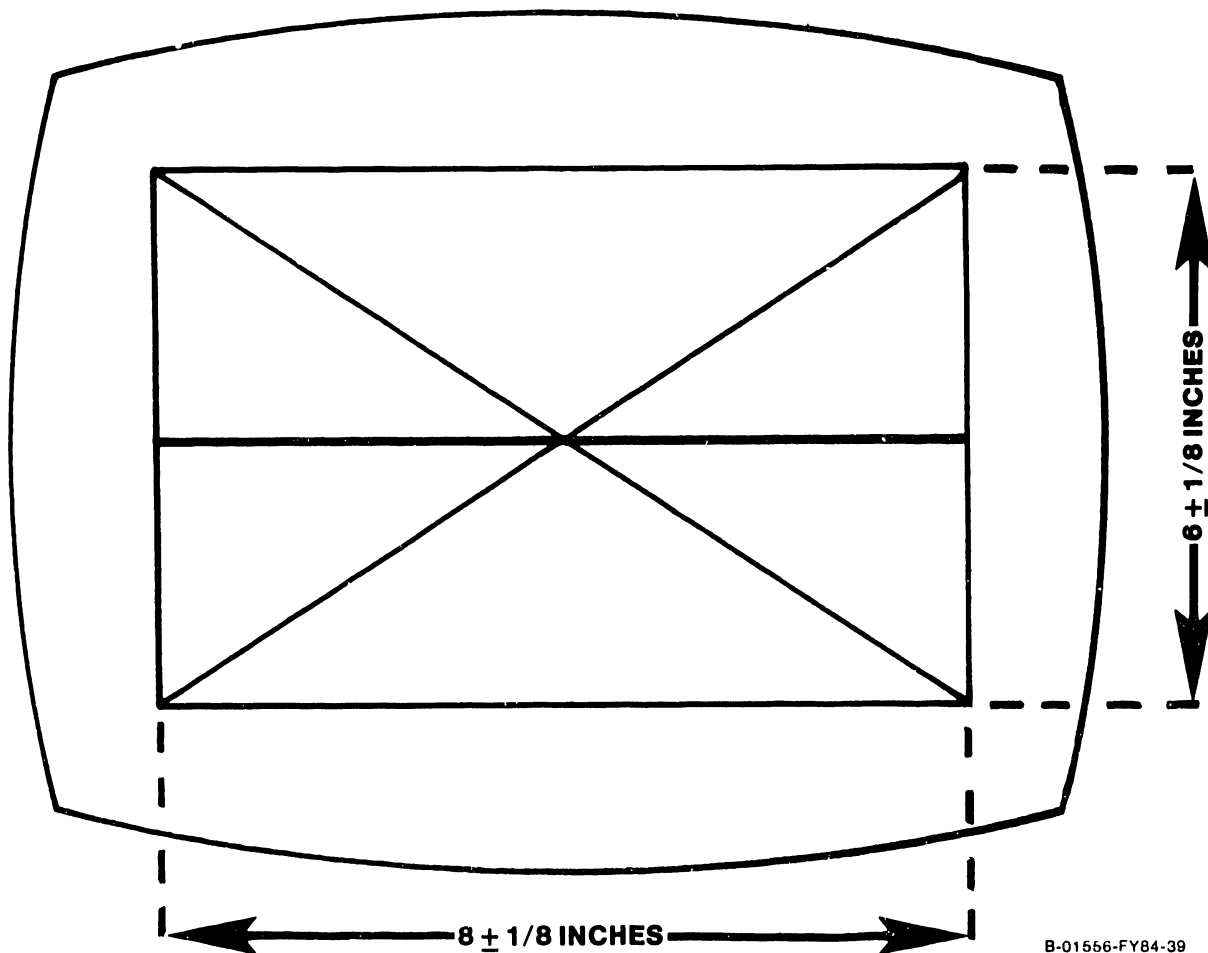
One of two Monitor PCAs will be found in the Monitor, either the 8244 PCA in early units or the 8344 PCA in later units. The two procedures that follow describe, in order, the 8244 unit and the 8344 unit.

5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.1 4210 Monitor Alignment

WARNING: High voltage is present in the vicinity of the Monitor PCA. Most adjustments will be made from the solder side of the PCA through labeled access holes. Use extreme caution in making these adjustments to prevent coming in contact with dangerous voltages.

The 4210 video pattern is shown in Figure 5-3.



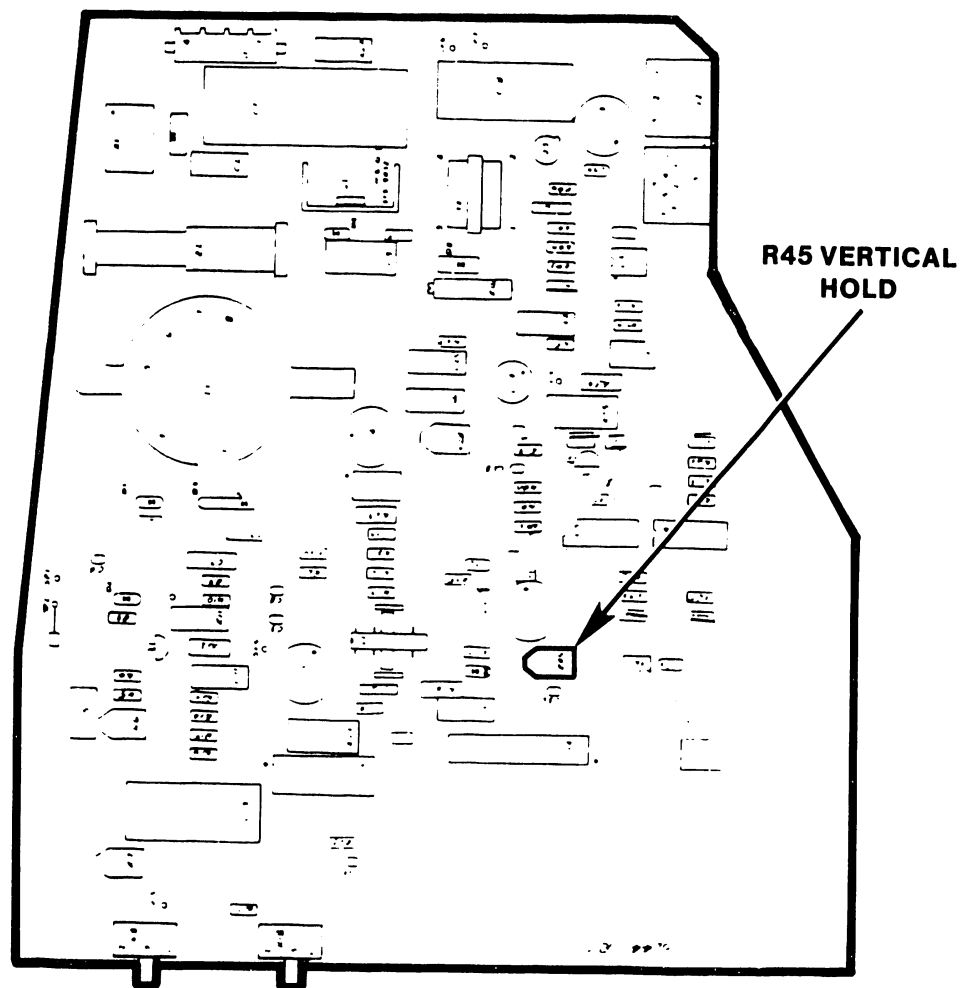
B-01566-FY84-39

Figure 5-3. Video Display Pattern of 4210 BIT

5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.1 4210 Monitor Alignment, continued

1. Set Workstation 1/0 switch to 1. Within two seconds, press in sequence CANCEL, CENTER.
2. Allow approximately five minutes for the Monitor to stabilize.
3. Adjust the Monitor Brightness control to display the video display pattern. Do not adjust Brightness so high as to cause raster display or blooming.
4. Adjust vertical hold control R45 to the center of its stable range.



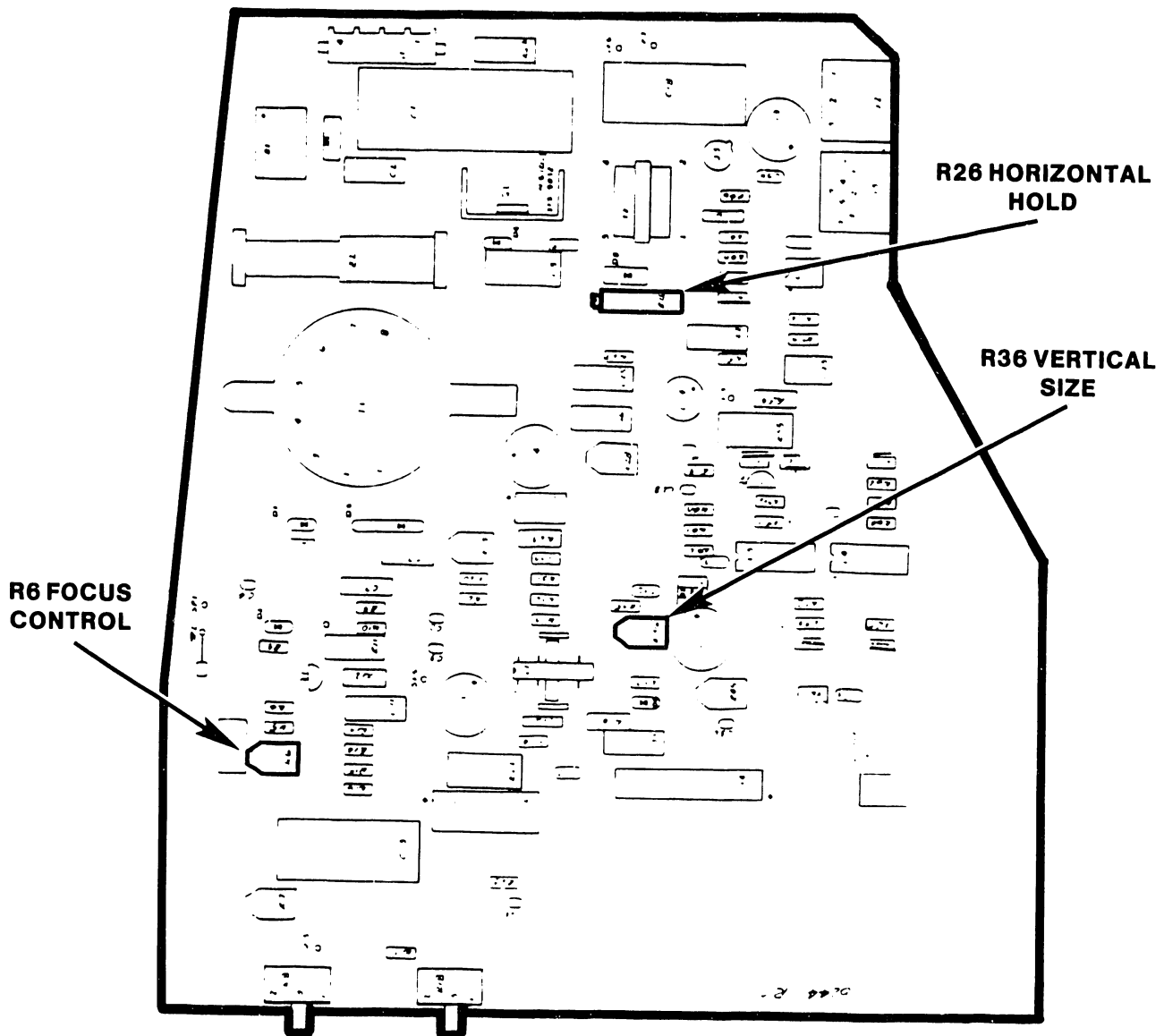
B-01556-FY84-40

Figure 5-4. 8244 Test Points and Adjustments

5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.1 4210 Monitor Alignment, continued

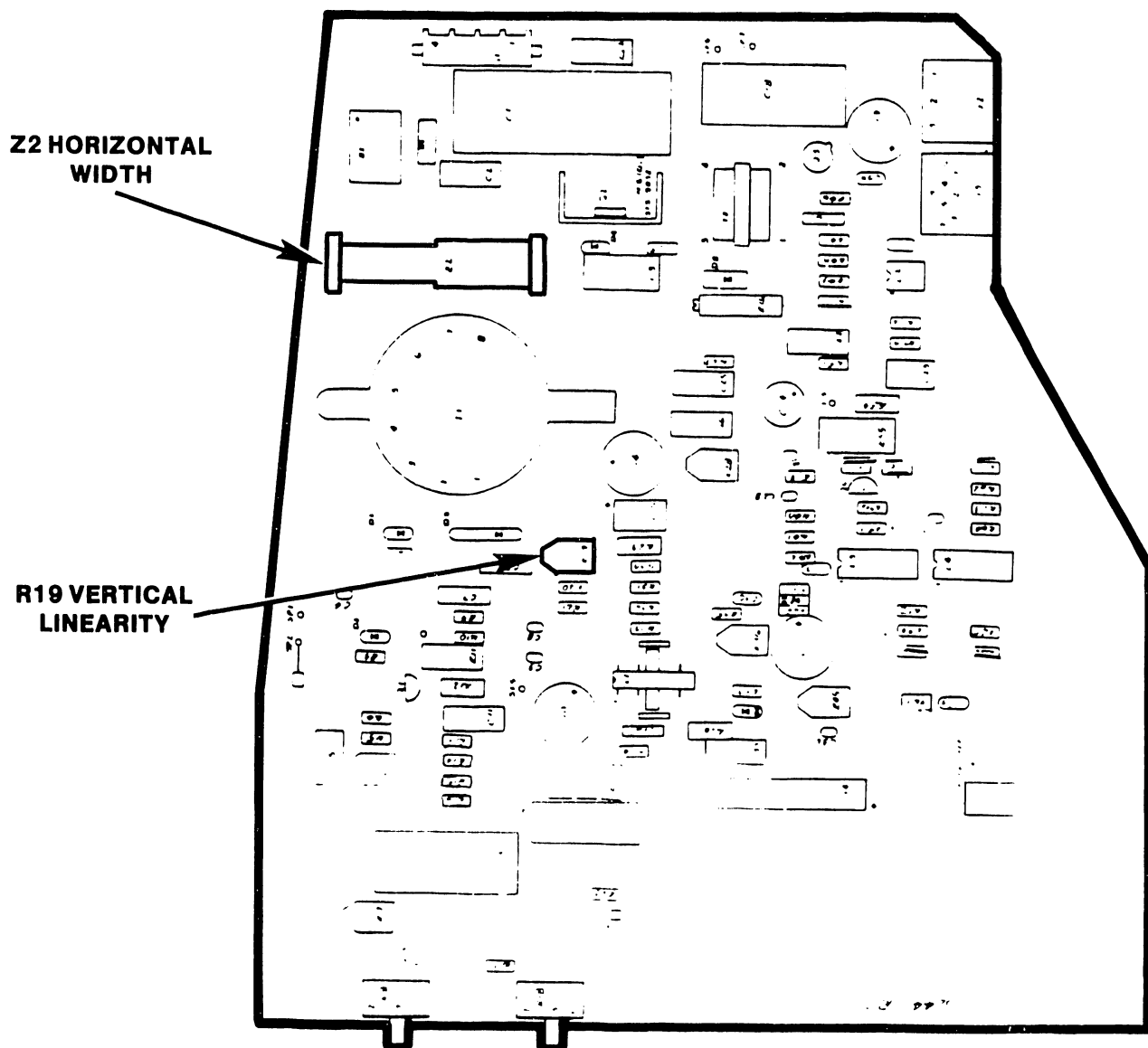
5. Adjust horizontal hold control R26 to the center of its stable range.
6. Adjust focus control R6 for the sharpest overall display pattern.
7. Adjust vertical size control R36 so that the display pattern is $6 \pm \frac{1}{8}$ inches ($15.2 \text{ cm} \pm 3 \text{ mm}$) high. Use a standard or metric scale.



5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.1 4210 Monitor Alignment, continued

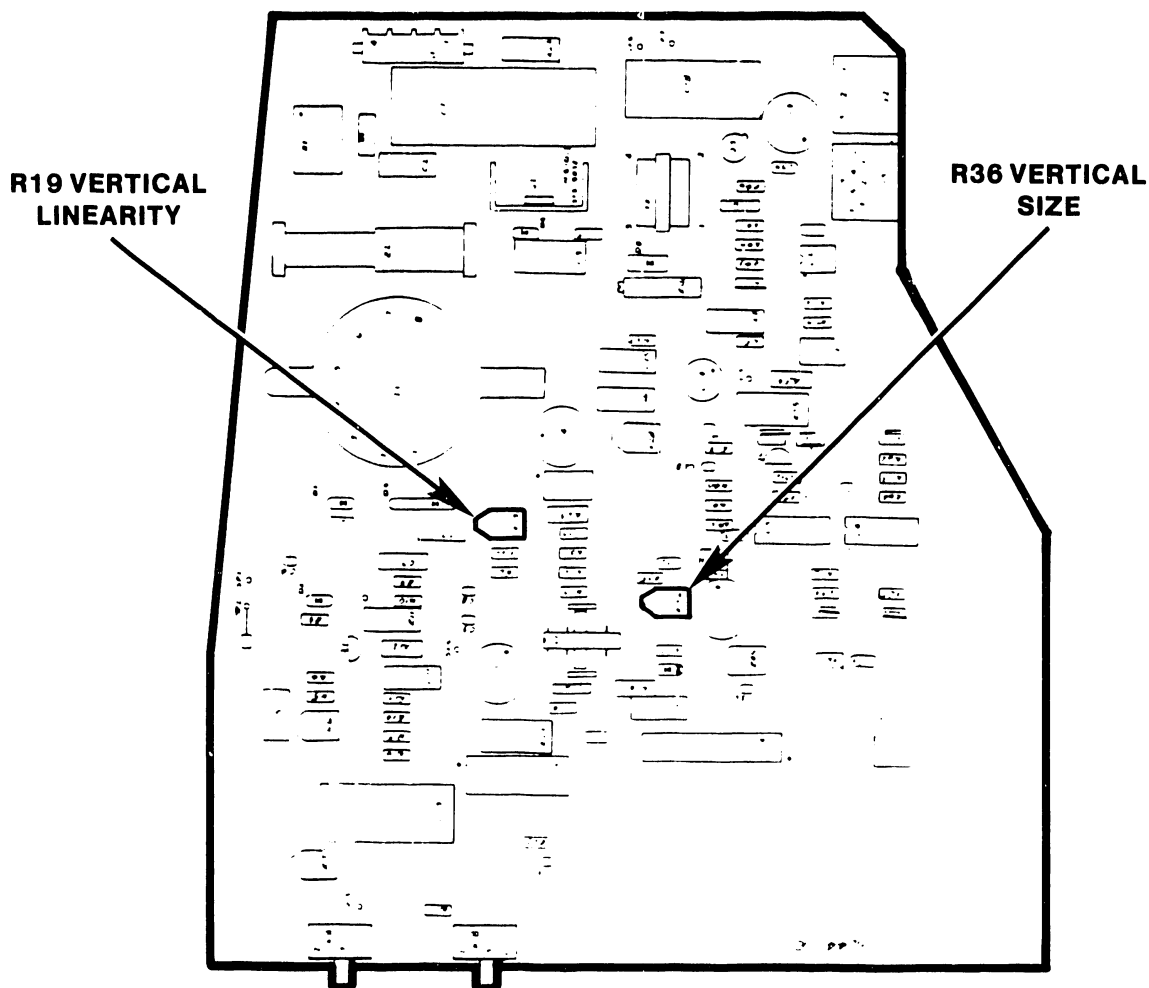
8. Adjust vertical linearity control R19 so that the squares at the top of the display are the same vertical size as the squares at the bottom of the display. This adjustment may affect the vertical height adjustment. Repeat step 7 if required.
9. Adjust horizontal width coil Z2 so that the display pattern is $8 \pm 1/8$ inches ($20.3 \text{ cm} \pm 3 \text{ mm}$) wide. Use a standard or metric scale.



5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.1 4210 Monitor Alignment, continued

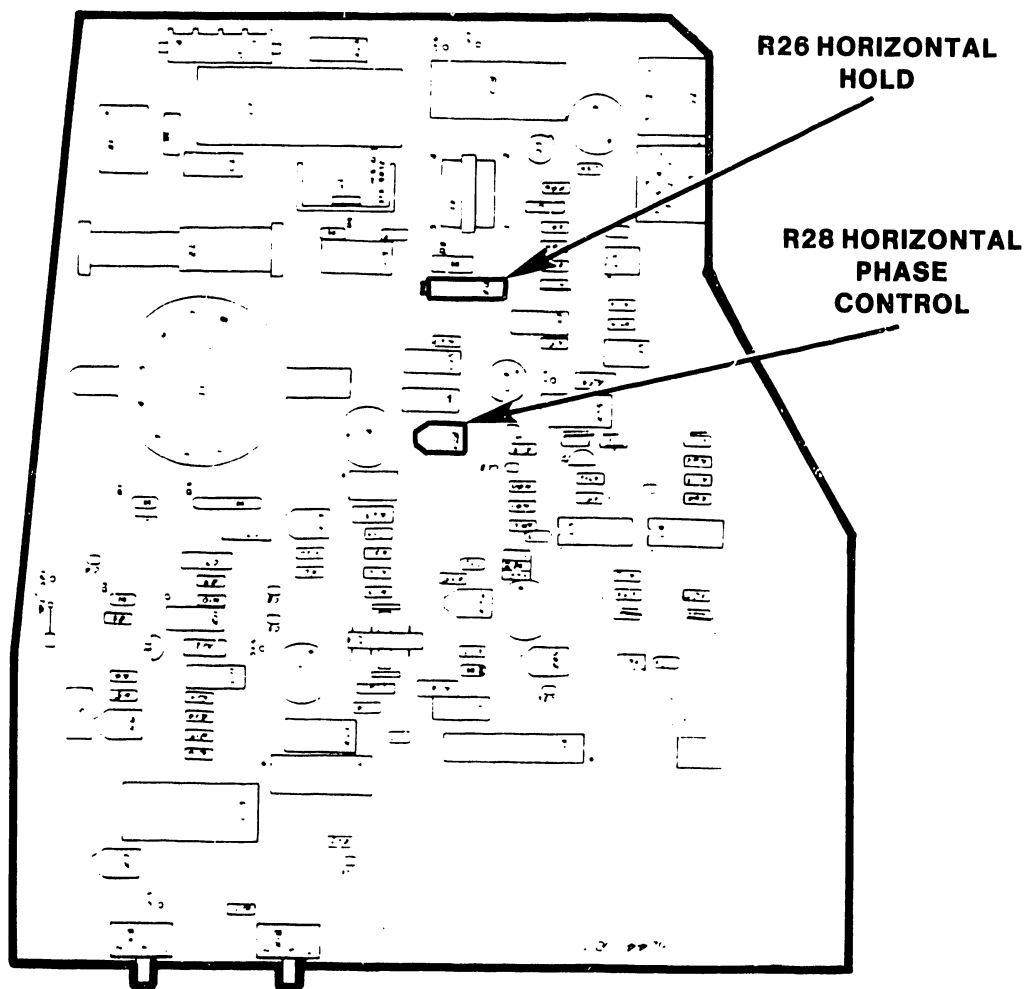
10. Adjust horizontal linearity control R19 so that the squares at the top of the display are the same vertical size as the squares at the bottom of the display. This adjustment may affect the vertical height adjustment. Repeat step 7 if necessary.
11. Select the circle alignment pattern in the Monitor alignment routine in the VS DTOS package. A visual check of the circles displayed should reveal no noticeable distortion, i.e. no egg-shaped or oblong forms. Repeat steps 7 through 11 if necessary.



5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.1 4210 Monitor Alignment, continued

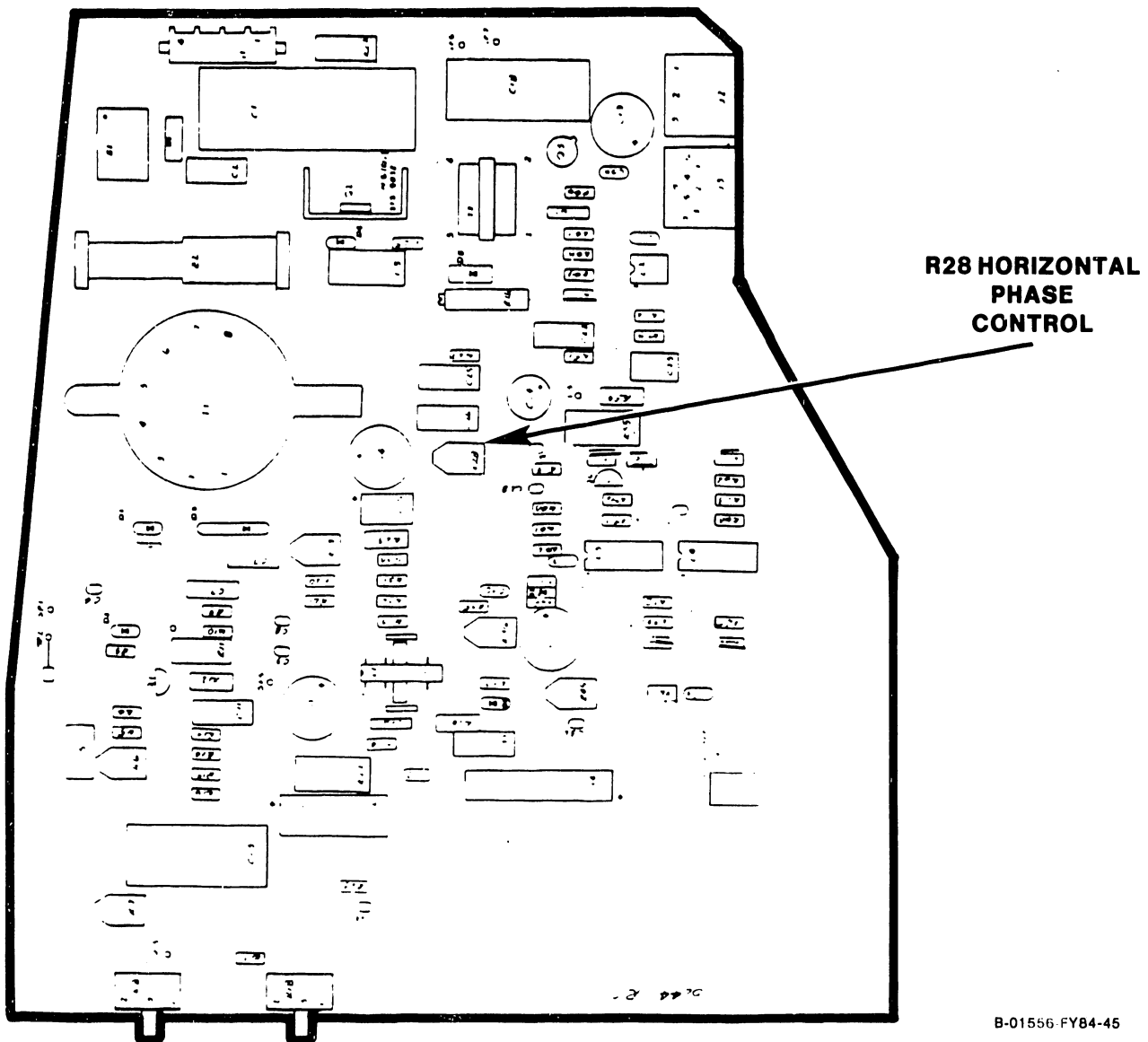
12. With the circle alignment pattern still selected, adjust the Brightness control to display the raster, but not so high as to cause blooming. Adjust horizontal phase control R28 completely counterclockwise.
13. Adjust horizontal hold control R26 clockwise so that the video pattern overlaps at the left edge of the display, and touches the left edge of the two left-most circles.



5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.1 4210 Monitor Alignment, continued

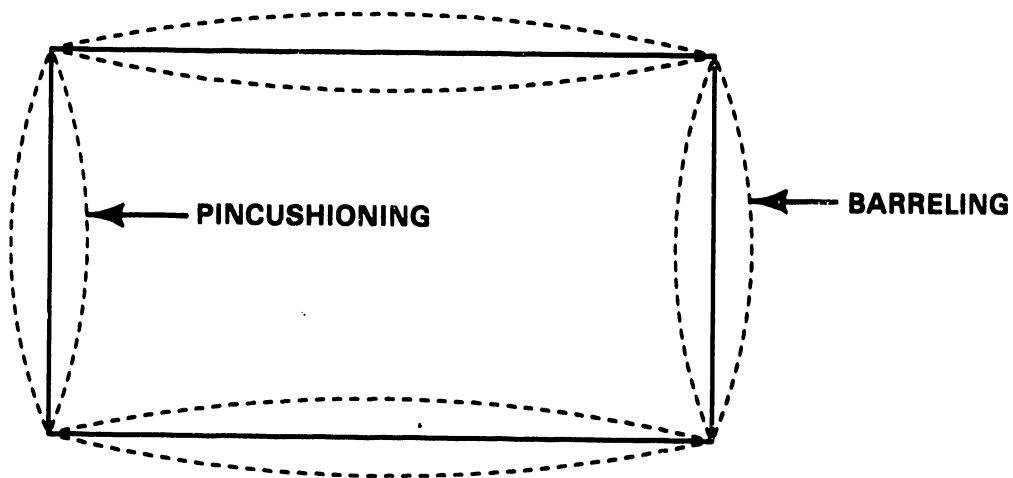
14. Adjust horizontal phase control R28 to center the display pattern in the raster. Return to the grid pattern and proceed with the next step.
15. Adjust the two tabs on the rear cover of the deflection yoke around the CRT neck one at a time to center the raster on the face of the CRT.



5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.1 4210 Monitor Alignment, continued

16. Using a non-metallic straight-edge (plastic ruler, envelope, etc.) for comparison, check each perimeter line of the video display pattern for pincushioning or barreling distortion (Figure 5-5a). The lines should be straight to within $\pm 1/16$ inch (1.5 mm).



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Figure 5-5.
Pincushioning/Barreling Correction

5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.1 4210 Monitor Alignment, continued

17. If either type of distortion exceeds $\pm 1/16$ inch (1.5 mm), adjustment of the magnets mounted on the posts around the perimeter of the deflection yoke is required (Figure 5-5b). Rotate the magnet closest to the area of greatest distortion to make the correction.

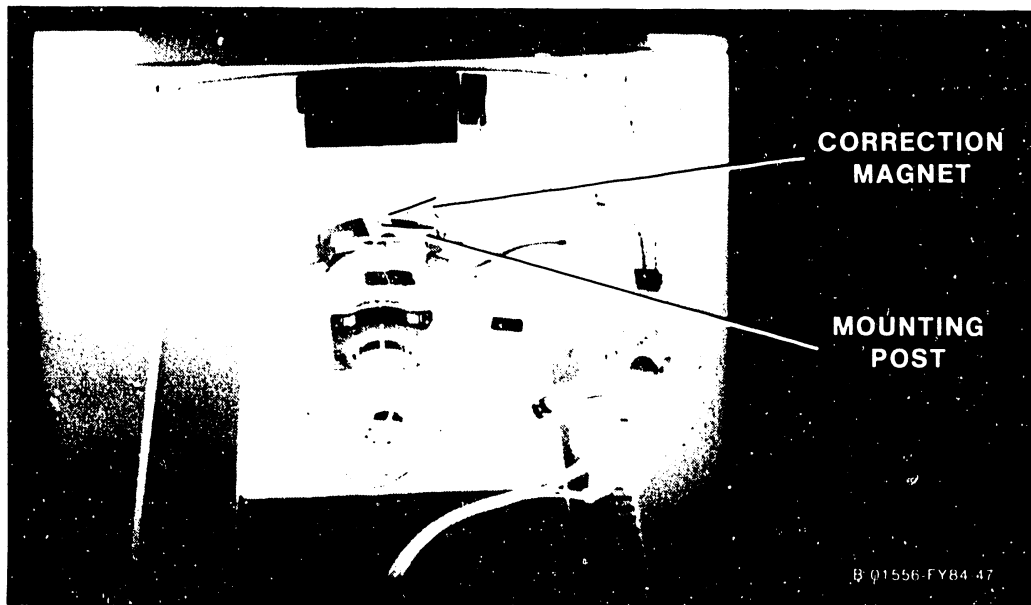


Figure 5-5b. Yoke Adjustments

5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.1 4210 Monitor Alignment, continued

18. If correction is not possible with the magnets mounted around the yoke, magnets can be added as required to correct the distortion. This generally involves replacing an existing magnet with one of a higher gauss value. The magnets, their color coding, and part numbers are listed below.

<u>MAGNET COLOR CODE</u>	<u>VALUE</u>	<u>PART NUMBER</u>
Green	Gauss 11	320-0126
Blue	Gauss 15	320-0128
White	Gauss 20	320-0127

If the above procedure does not bring the Monitor into tolerance, replacement is recommended. If the Monitor can be aligned satisfactorily, power off the workstation and reassemble the Monitor.

5.3.3.2 4220 Monitor Alignment

WARNING: High voltage is present in the vicinity of the Monitor PCA. Most adjustments will be made from the solder side of the PCA through labeled access holes. Use extreme caution in making these adjustments to prevent coming in contact with dangerous voltages.

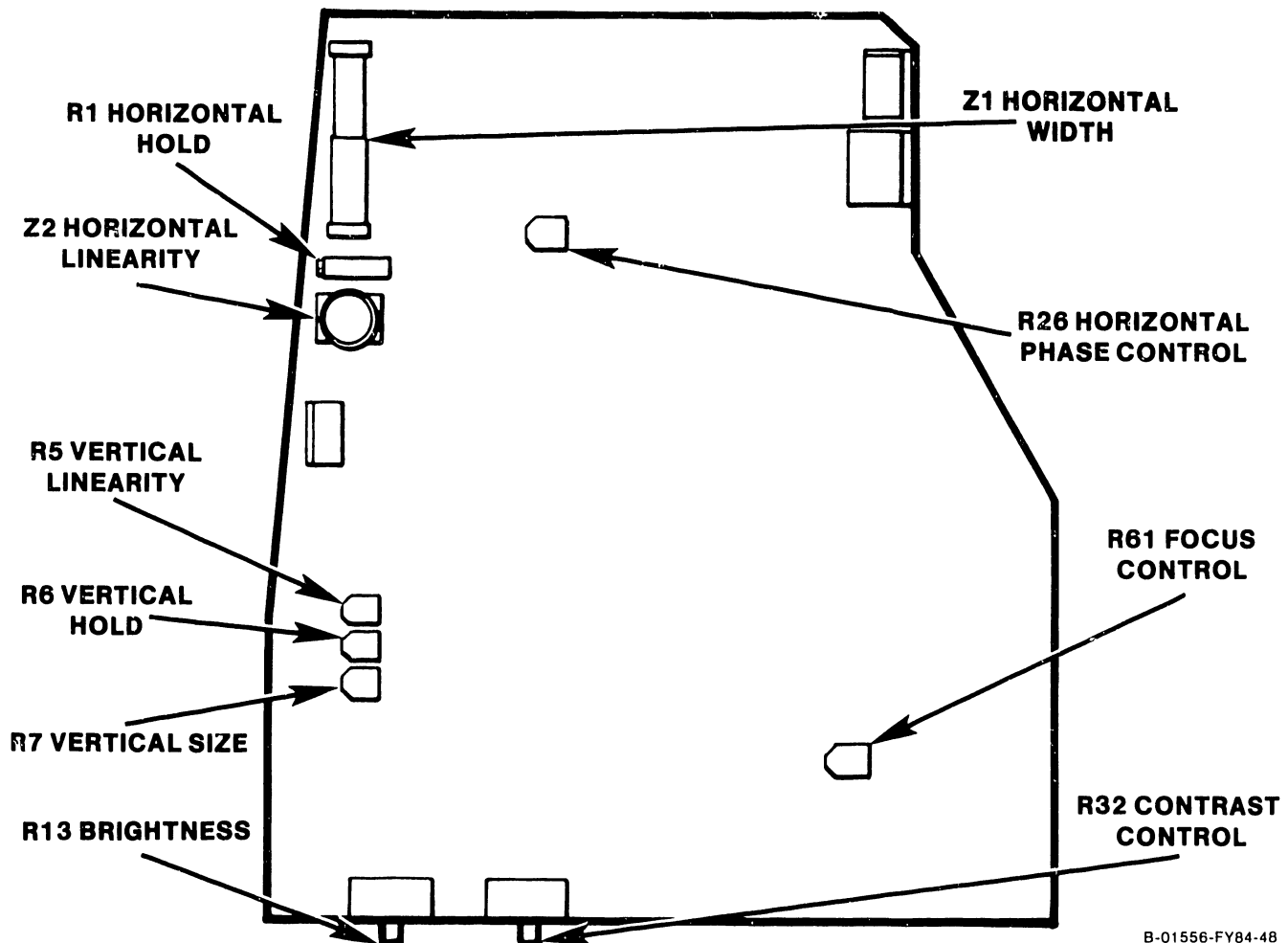
The 4220 will not display the same video pattern as the 4210, but a full screen of characters can be used for the following adjustments. Use the perimeter of the character block as a guide when instructed to use the perimeter of the display

5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.2 4220 Monitor Alignment, continued

pattern. In the following steps, the block of characters on the 4220 screen is referred to as a video display pattern, or simply display pattern.

1. Set Workstation I/O switch to 1. Within two seconds, press in sequence CANCEL, CENTER.
2. Allow approximately five minutes for the Monitor to stabilize.
3. Adjust the Monitor Brightness control to display the video display pattern. Do not adjust Brightness so high as to cause raster display or blooming.



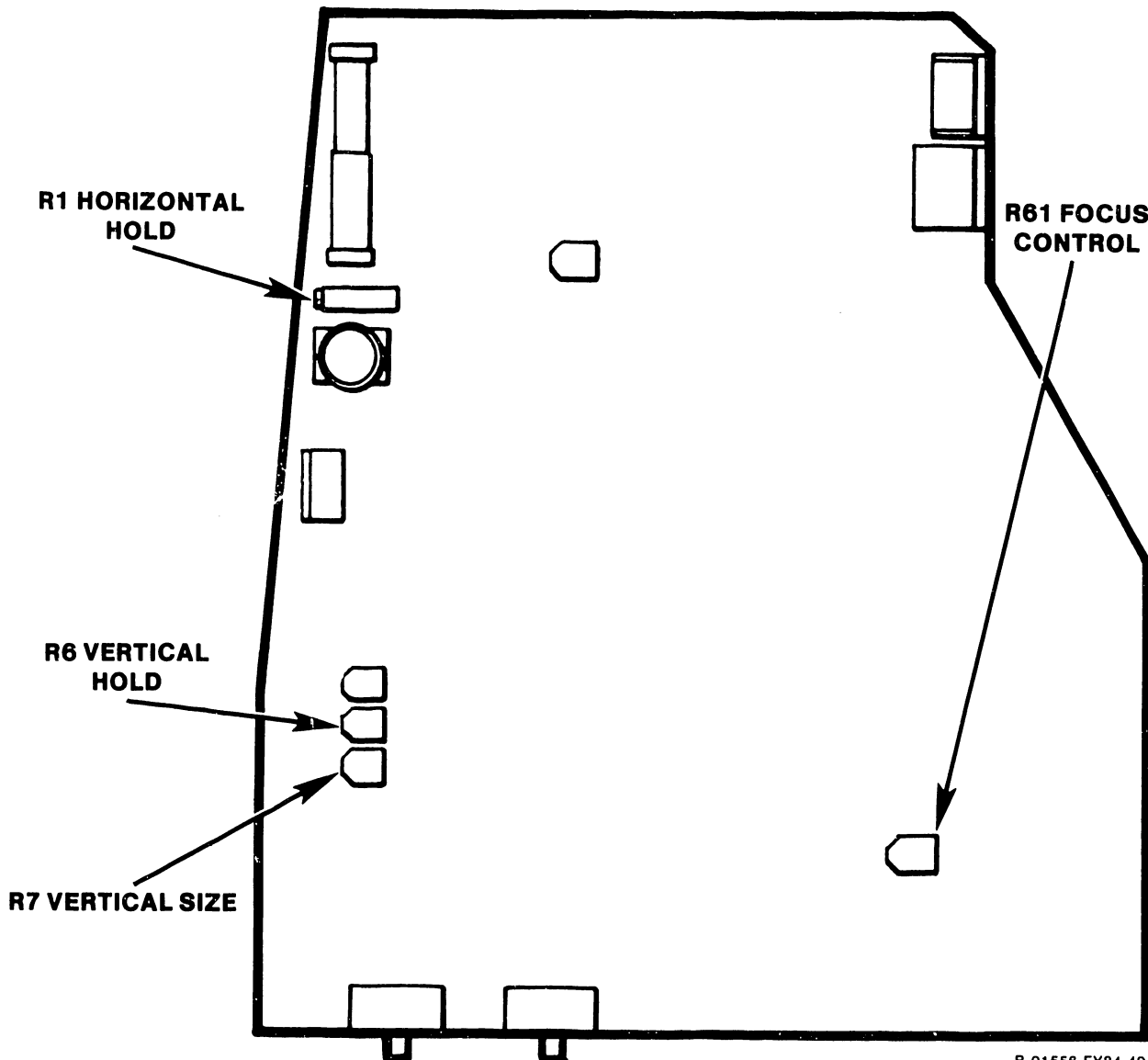
B-01556-FY84-48

Figure 5-6. 8344 Test Points and Adjustments

5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.2 4220 Monitor Alignment, continued

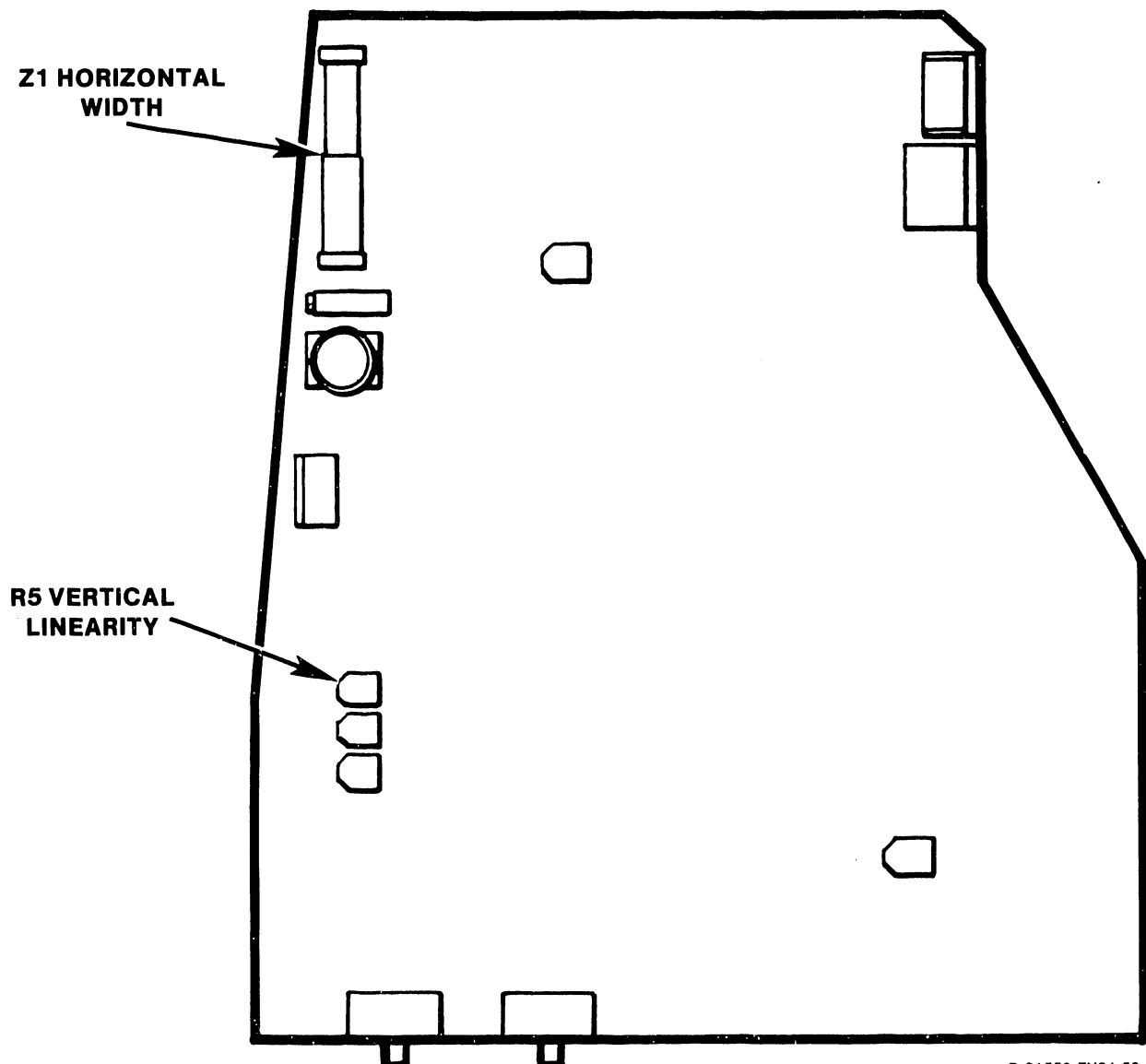
4. Adjust vertical hold control R6 to the center of its stable range.
5. Adjust horizontal hold control R1 to the center of its stable range.
6. Adjust focus control R61 for the sharpest overall display pattern.
7. Adjust vertical size control R7 so that the display pattern is $6 \pm 1/8$ inches ($15.2 \text{ cm} \pm 3 \text{ mm}$) high. Use a standard or metric scale.



5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.2 4220 Monitor Alignment, continued

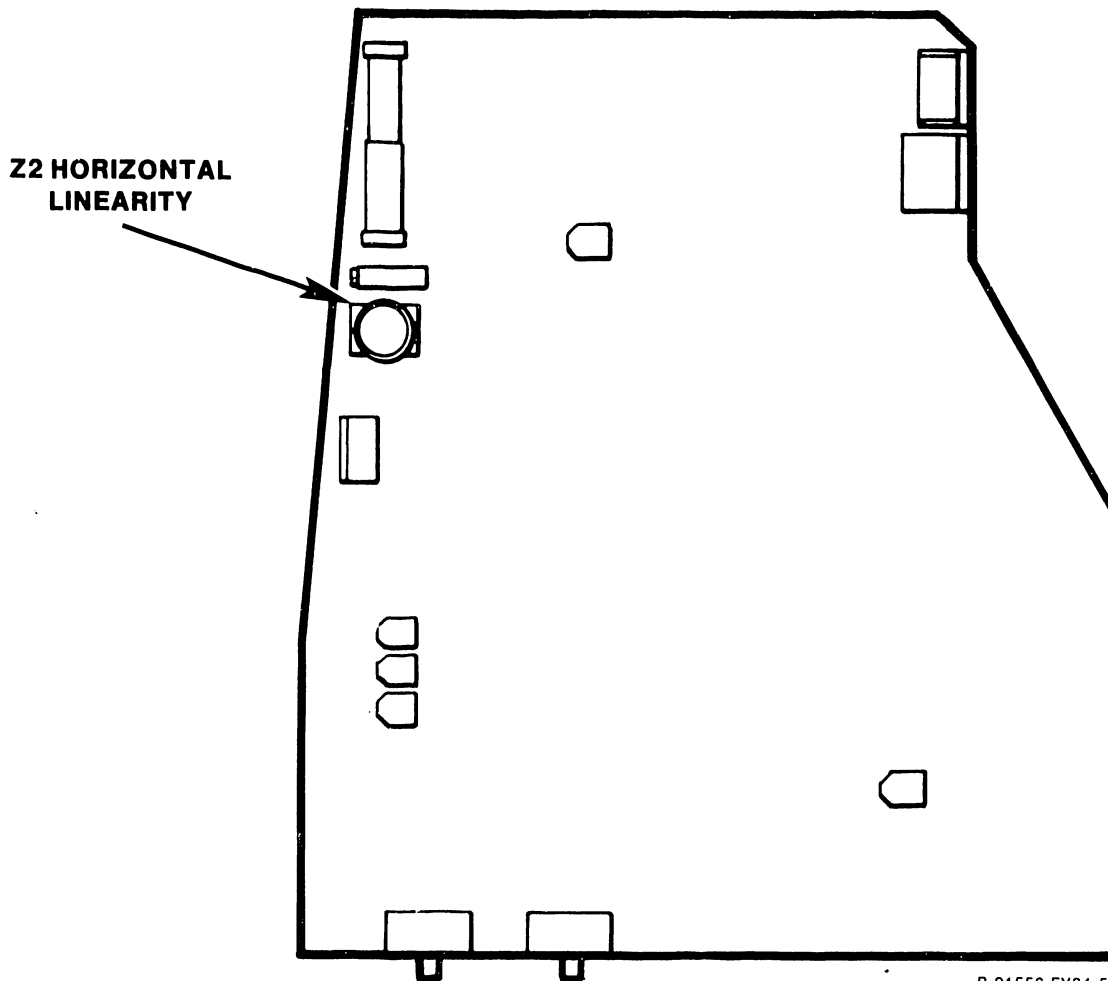
8. Adjust vertical linearity control R5 so that the squares at the top of the display are the same vertical size as the squares at the bottom of the display. This adjustment may affect the vertical height adjustment; repeat step 7 if required.
9. Adjust horizontal width coil Z1 so that the display pattern is $8 \pm 1/8$ inches ($20.3 \text{ cm} \pm 3 \text{ mm}$) wide. Use a standard or metric scale.



5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.2 4220 Monitor Alignment, continued

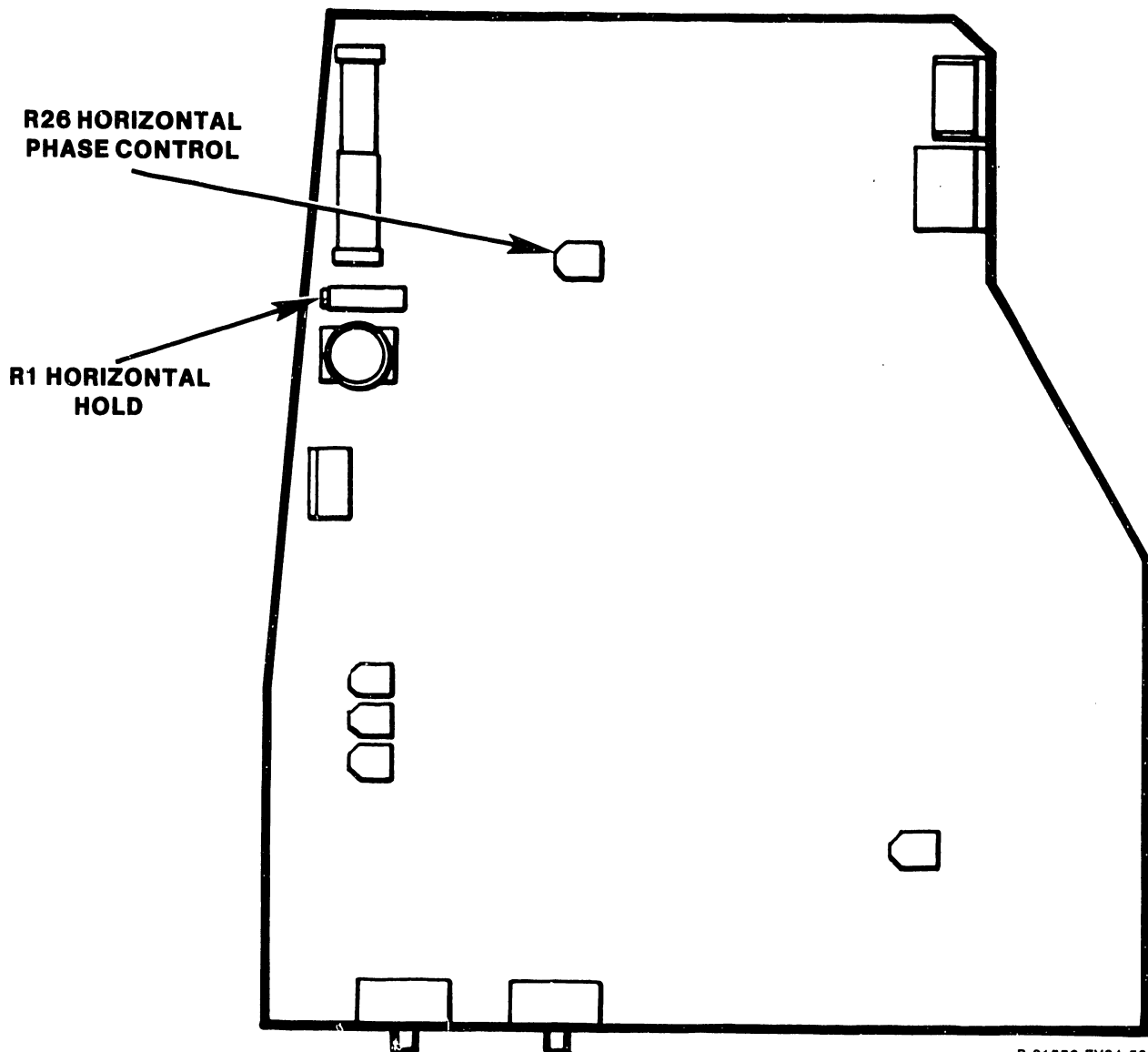
10. Adjust horizontal linearity coil Z2 so that the squares at the top of the display are the same horizontal size as the squares at the bottom of the display. This adjustment may affect the horizontal height adjustment; repeat step 9 if necessary.
11. Select the circle alignment pattern in the Monitor alignment routine in the VS DTOS package. A visual check of the circles displayed should reveal no noticeable distortion, i.e. no egg-shaped or oblong forms. Repeat steps 7 through 11 if necessary.



5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.2 4220 Monitor Alignment, continued

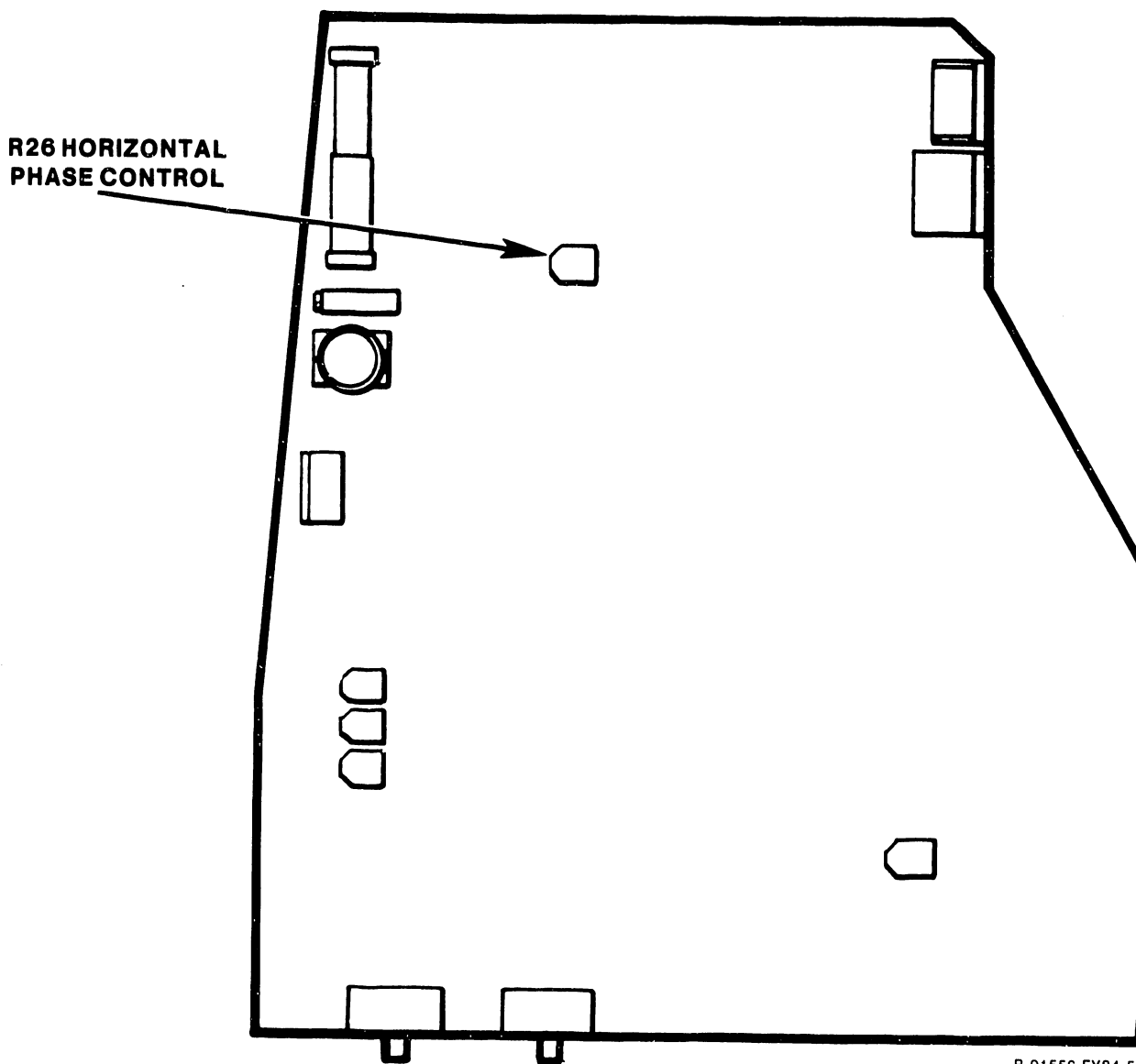
12. With the circle alignment pattern still selected, adjust the Brightness control to display the raster, but not so high as to cause blooming. Adjust horizontal phase control R26 completely counterclockwise.
13. Adjust horizontal hold control R1 clockwise so that the video pattern overlaps at the left edge of the display, and touches the left edge of the two left-most circles.



5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.2 4220 Monitor Alignment, continued

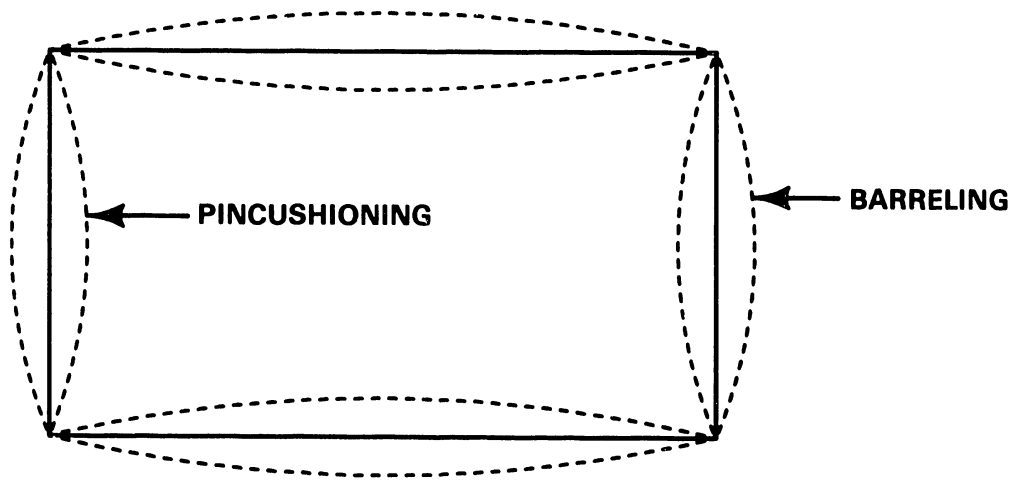
14. Adjust horizontal phase control R26 to center the display pattern in the raster. Return to the grid pattern and proceed with the next step.
15. Adjust the two tabs on the rear cover of the deflection yoke around the CRT neck one at a time to center the raster on the face of the CRT.



5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.2 4220 Monitor Alignment, continued

16. Using a non-metallic straight-edge (plastic ruler, envelope, etc.) for comparison, check each perimeter line of the video display pattern for pincushioning or barreling distortion (see below). The lines should be straight to within $\pm 1/16$ inch (1.5 mm).



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5.3.3 MONITOR ALIGNMENT USING BIT SUPPORT, cont.

5.3.3.2 4220 Monitor Alignment, continued

17. If either type of distortion exceeds $\pm 1/16$ inch (1.5 mm), adjustment of the magnets mounted on the posts around the perimeter of the deflection yoke is required. Rotate the magnet closest to the area of greatest distortion to make the correction.
18. If correction is not possible with the magnets mounted around the yoke, magnets can be added as required to correct the distortion. This generally involves replacing an existing magnet with one of a higher gauss value. The magnets, their color coding, and part numbers are listed below.

<u>MAGNET COLOR CODE</u>	<u>VALUE</u>	<u>PART NUMBER</u>
Green	Gauss 11	320-0126
Blue	Gauss 15	320-0128
White	Gauss 20	320-0127

If the above procedure does not bring the Monitor into tolerance, replacement is recommended. If the Monitor can be aligned satisfactorily, power off the workstation and reassemble the Monitor.

5.3 CORRECTIVE MAINTENANCE, continued

5.3.4 MONITOR ALIGNMENT USING DTOS SUPPORT

Alignment of the 4210/4220 Monitor can also be carried out using video patterns in the VS DTOS package.

Pre-Alignment Conditions

- o Remove cover from Monitor (section 5.5).
- o Connect dual cable between Monitor and Electronics Base.
- o Set workstation I/O switch to 1 (on). Allow approx. five minutes for the Monitor to stabilize.

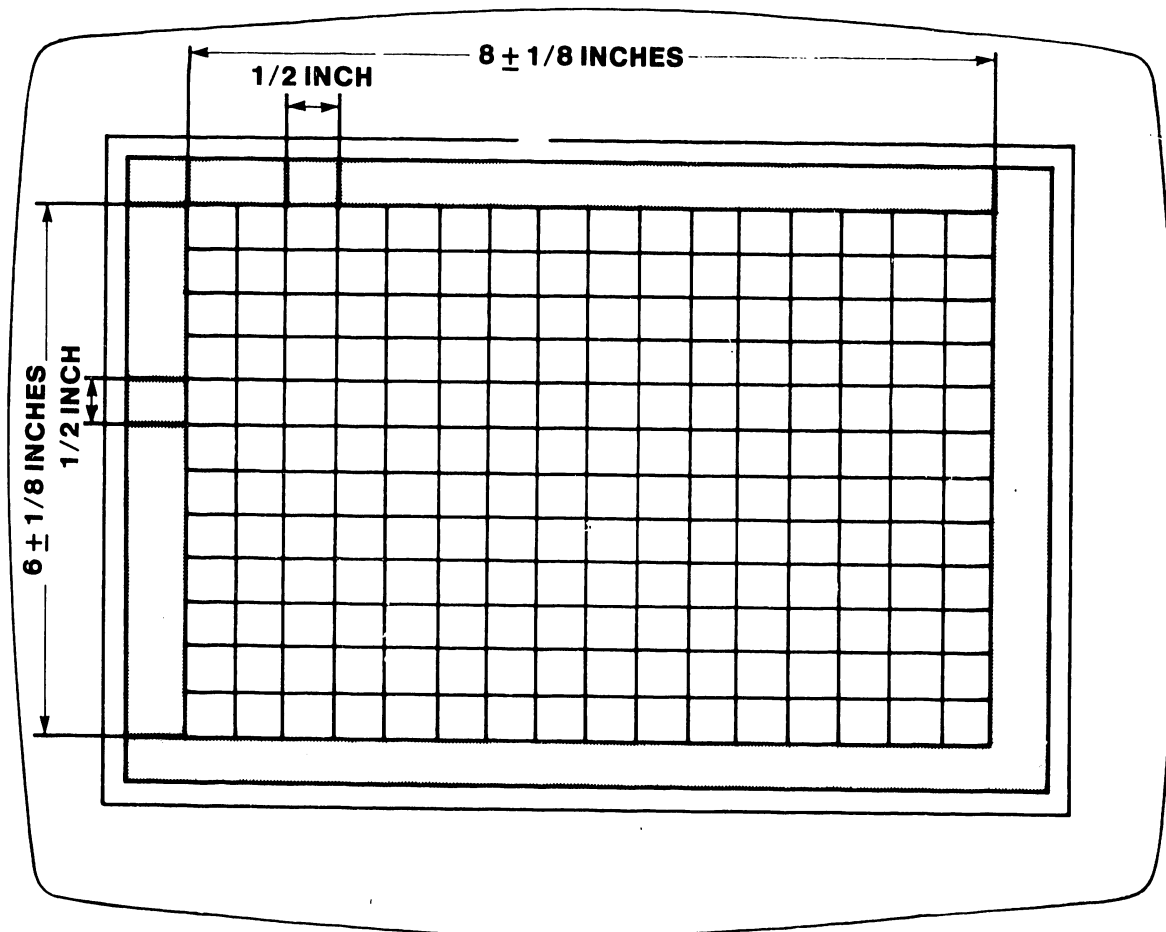
WARNING

High voltage is present in the vicinity of the Monitor PCA. Most adjustments will be made from the solder side of the PCA through labeled access holes. Use extreme caution in making these adjustments to prevent coming in contact with dangerous voltages.

5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.1 4210 DTOS Monitor Alignment

1. Select the Monitor alignment routine resident in the VS DTOS package. This routine contains four different patterns for use in aligning the Monitor. Only two patterns, the grid and the circle, will be used in the following procedure.
2. Select the grid alignment pattern (Figure 5-7) for display on the workstation Monitor.



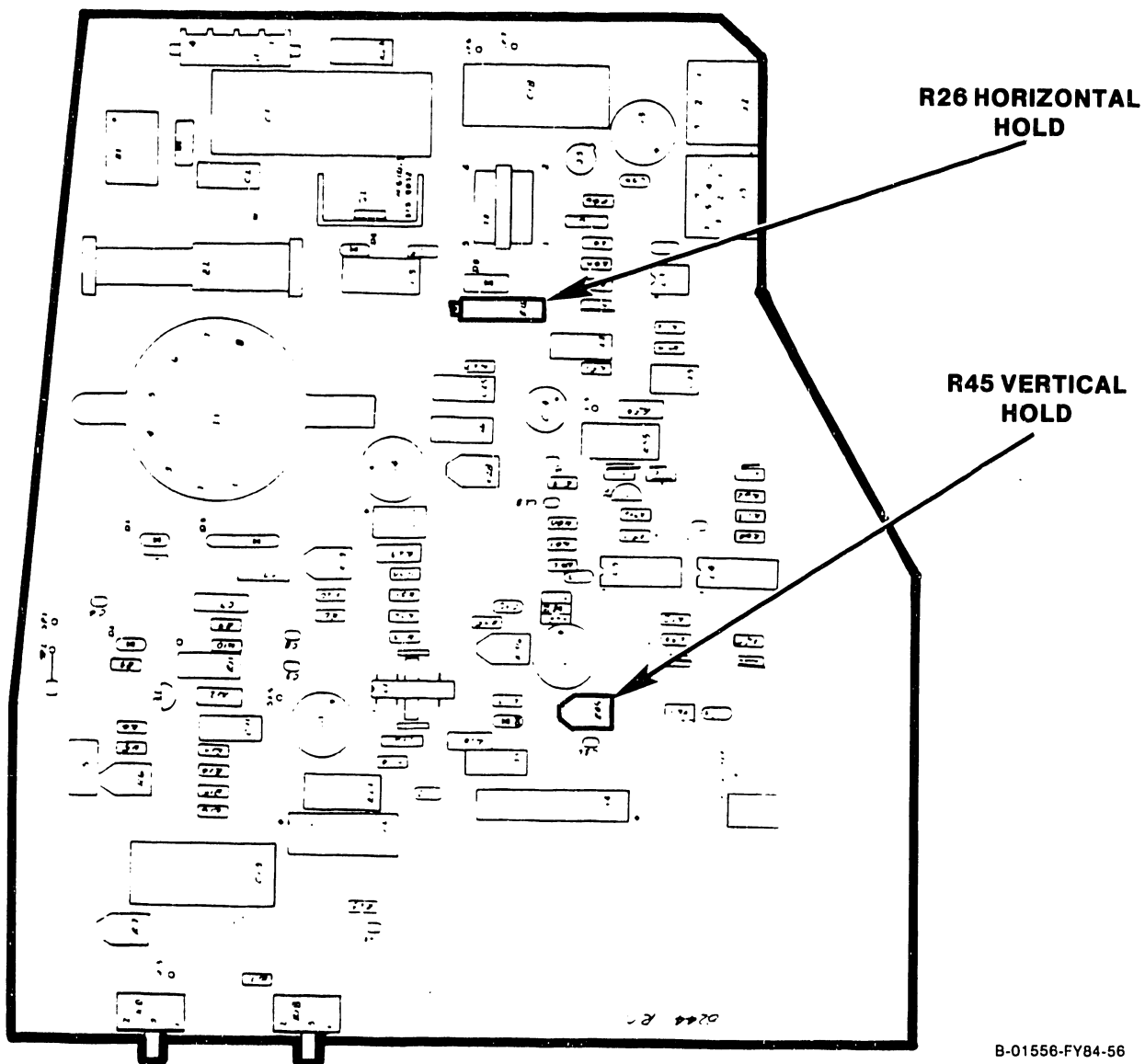
B-01556-FY84-55

Figure 5-7. VS DTOS Grid Display Pattern

5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.1 4210 DTOS Monitor Alignment, continued

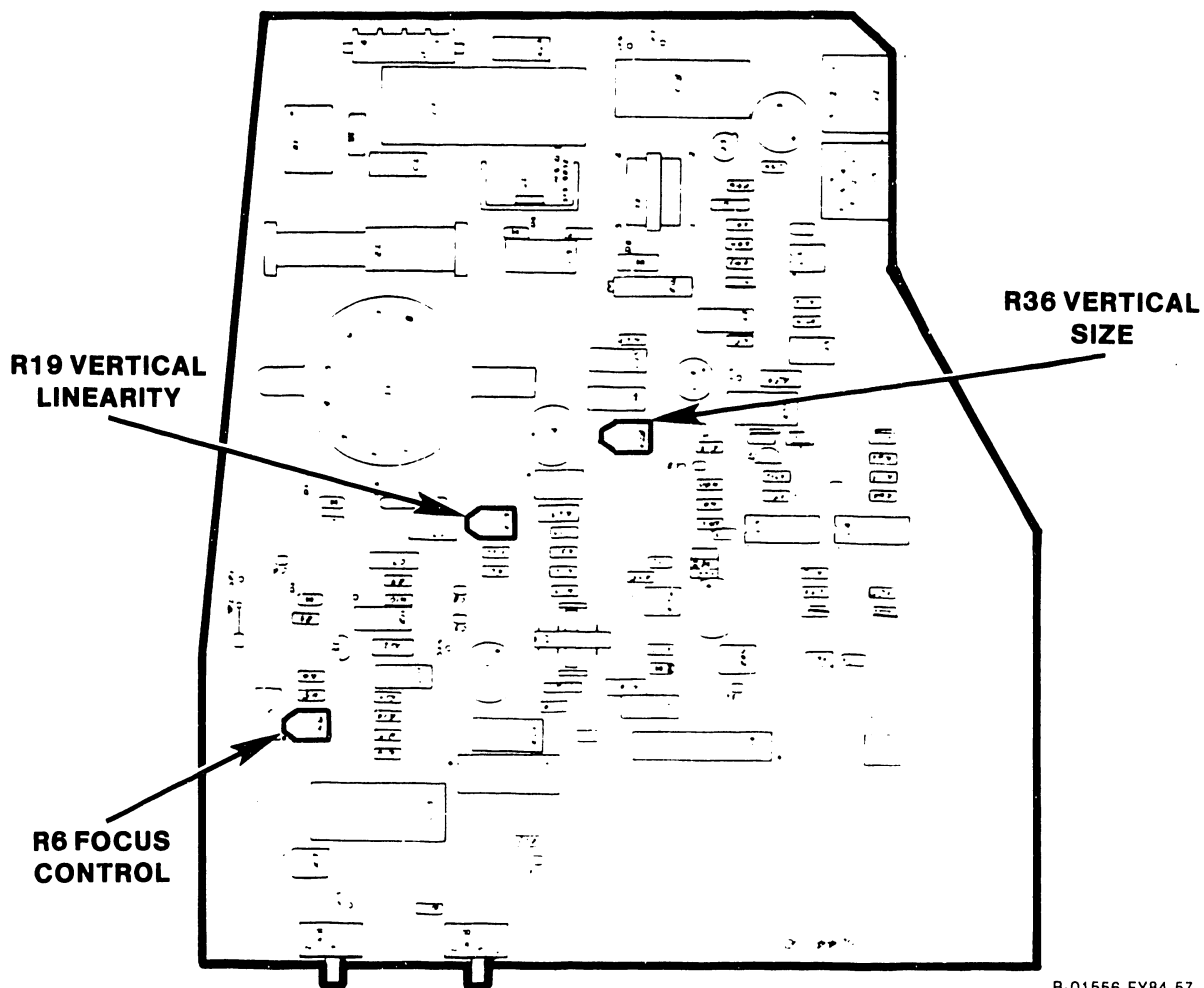
3. Adjust the Monitor brightness control to adequately display the grid alignment pattern. Do not adjust brightness so high as to cause display of the raster or cause blooming.
4. Adjust vertical hold control R45 to the center of its stable range.
5. Adjust horizontal hold control R26 to the center of its stable range.



5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.1 4210 DTOS Monitor Alignment, continued

6. Adjust focus control R6 for the sharpest overall display pattern.
7. Adjust vertical size control R36 so that the display pattern is $6 \pm 1/8$ inches ($15.2 \text{ cm} \pm 3 \text{ mm}$) high. Use a standard or metric scale.
8. Adjust vertical linearity control R19 so that the squares at the top of the display are the same vertical size as the squares at the bottom of the display. This adjustment may affect the vertical height adjustment. Repeat step 7 if required.



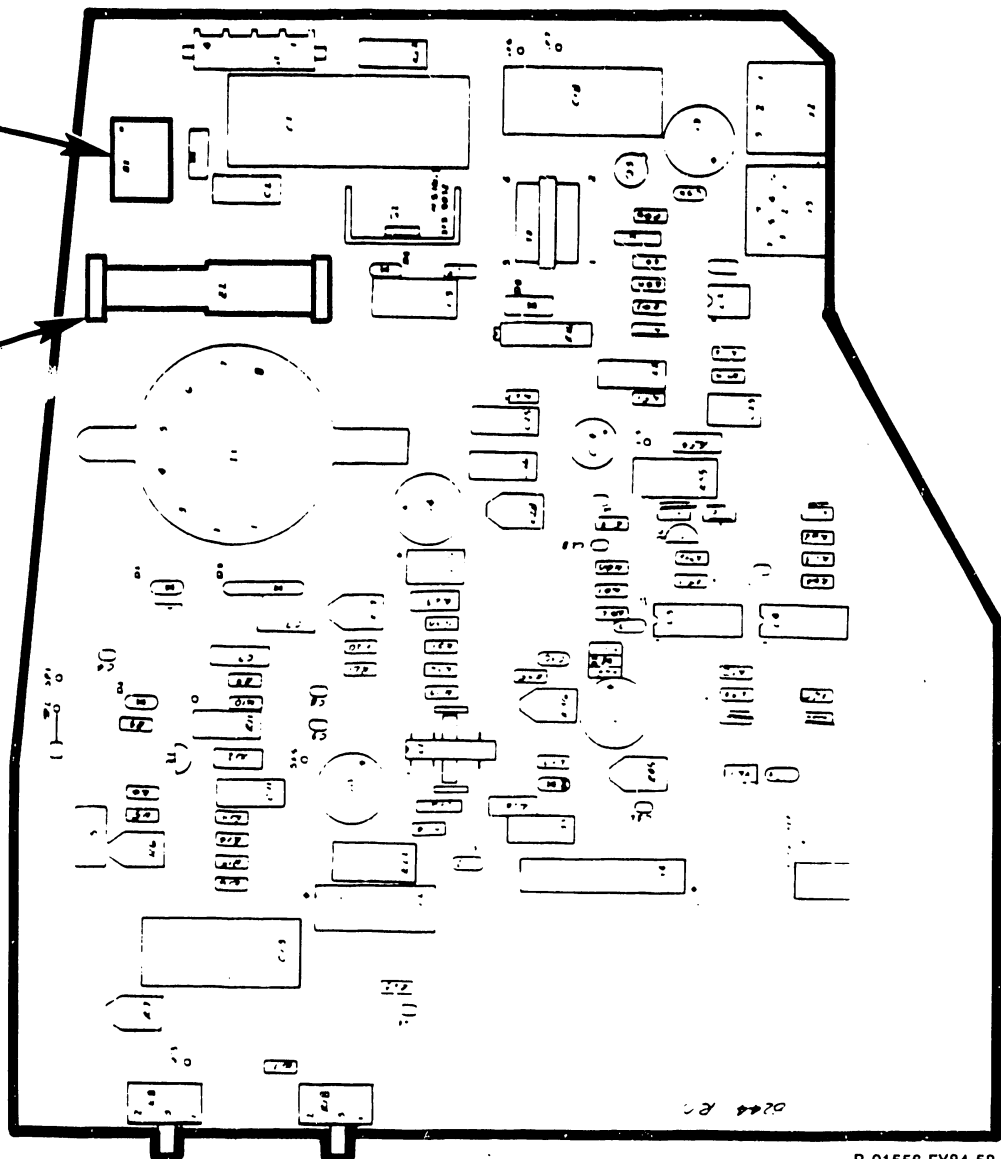
5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.1 4210 DTOS Monitor Alignment, continued

9. Adjust horizontal width coil Z2 so that the display pattern is $8 \pm 1/8$ inches ($20.3 \text{ cm} \pm 3 \text{ mm}$) wide. Use a standard or metric scale.
10. Adjust horizontal linearity coil Z1 so that the squares at the left of the display are the same horizontal size as the squares at the right of the display. This adjustment may affect the horizontal width adjustment. Repeat step 9 if required.

Z1 HORIZONTAL
LINEARITY

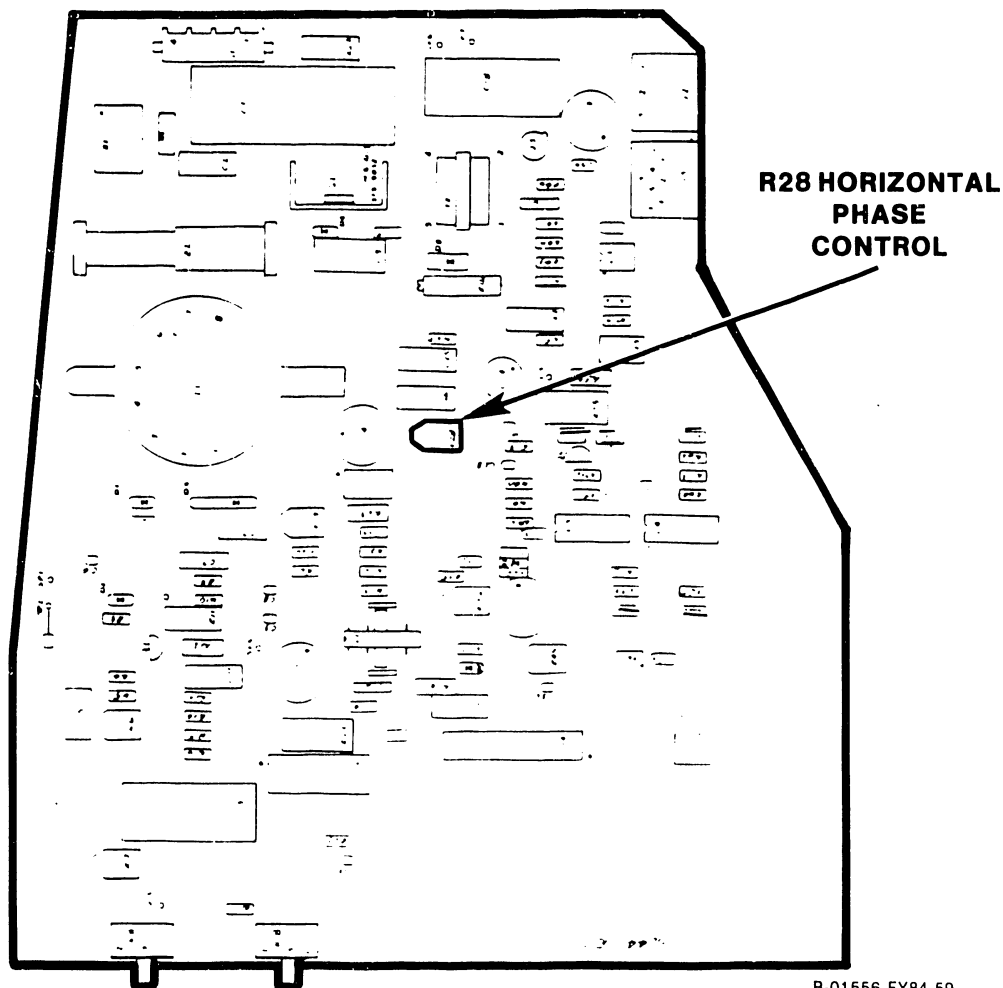
Z2 HORIZONTAL
WIDTH



5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.1 4210 DTOS Monitor Alignment, continued

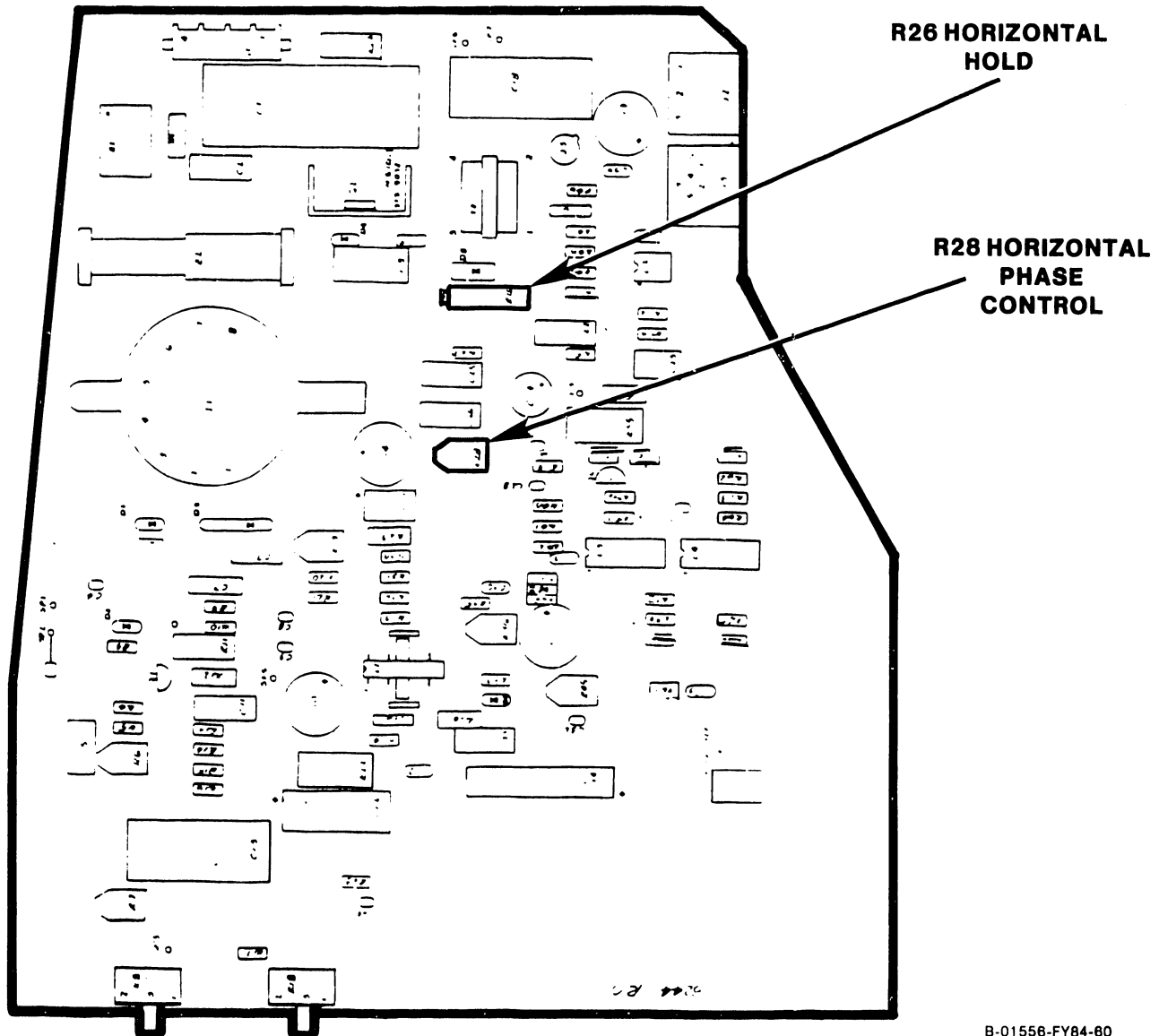
11. Select the circle alignment pattern in the Monitor alignment routine in the VS DTOS package. A visual check of the circles displayed should reveal no noticeable distortion, i.e., no egg-shaped or oblong forms. Repeat steps 7 through 11 if necessary.
12. With the circle alignment pattern still selected, adjust the Brightness control to display the raster, but not so high as to cause blooming. Adjust horizontal phase control R28 completely counterclockwise.



5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.1 4210 DTOS Monitor Alignment, continued

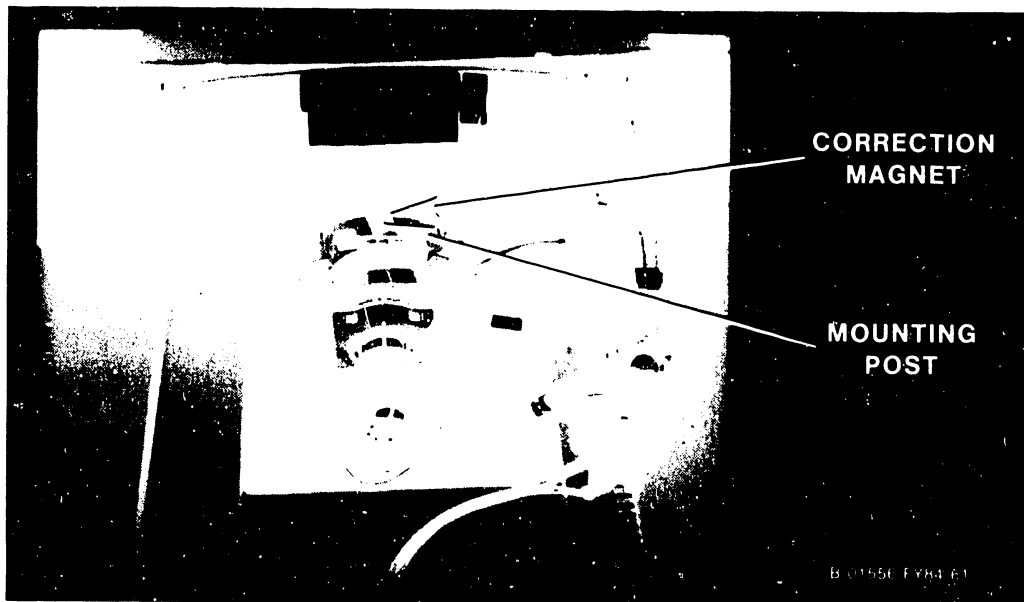
13. Adjust horizontal hold control R26 clockwise so that the video pattern overlaps at the left edge of the display, and touches the left edge of the two left-most circles.
14. Adjust horizontal phase control R28 to center the display pattern in the raster. Return to the grid pattern and proceed with the next step.



5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.1 4210 DTOS Monitor Alignment, continued

15. Adjust the two tabs on the rear cover of the deflection yoke around the CRT neck one at a time to center the raster on the face of the CRT.
16. Using a non-metallic straight-edge (plastic ruler, envelope, etc.) for comparison, check each perimeter line of the video display pattern for pincushioning or barreling distortion. The lines should be straight to within $\pm 1/16$ inch (1.5 mm).



5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.1 4210 DTOS Monitor Alignment, continued

17. If either type of distortion exceeds $\pm 1/16$ inch (1.5 mm), adjustment of the magnets mounted on the posts around the perimeter of the deflection yoke is required. Rotate the magnet closest to the area of greatest distortion to make the correction.
18. If correction is not possible with the magnets mounted around the yoke, magnets can be added as required to correct the distortion. This generally involves replacing an existing magnet with one of a higher gauss value. The magnets, their color coding and part numbers are listed below.

<u>MAGNET COLOR CODE</u>	<u>VALUE</u>	<u>PART NUMBER</u>
Green	Gauss 11	320-0126
Blue	Gauss 15	320-0128
White	Gauss 20	320-0127

If the above procedure does not bring the Monitor into tolerance, replacement is recommended. If the Monitor can be aligned satisfactorily, power off the workstation and reassemble the Monitor.

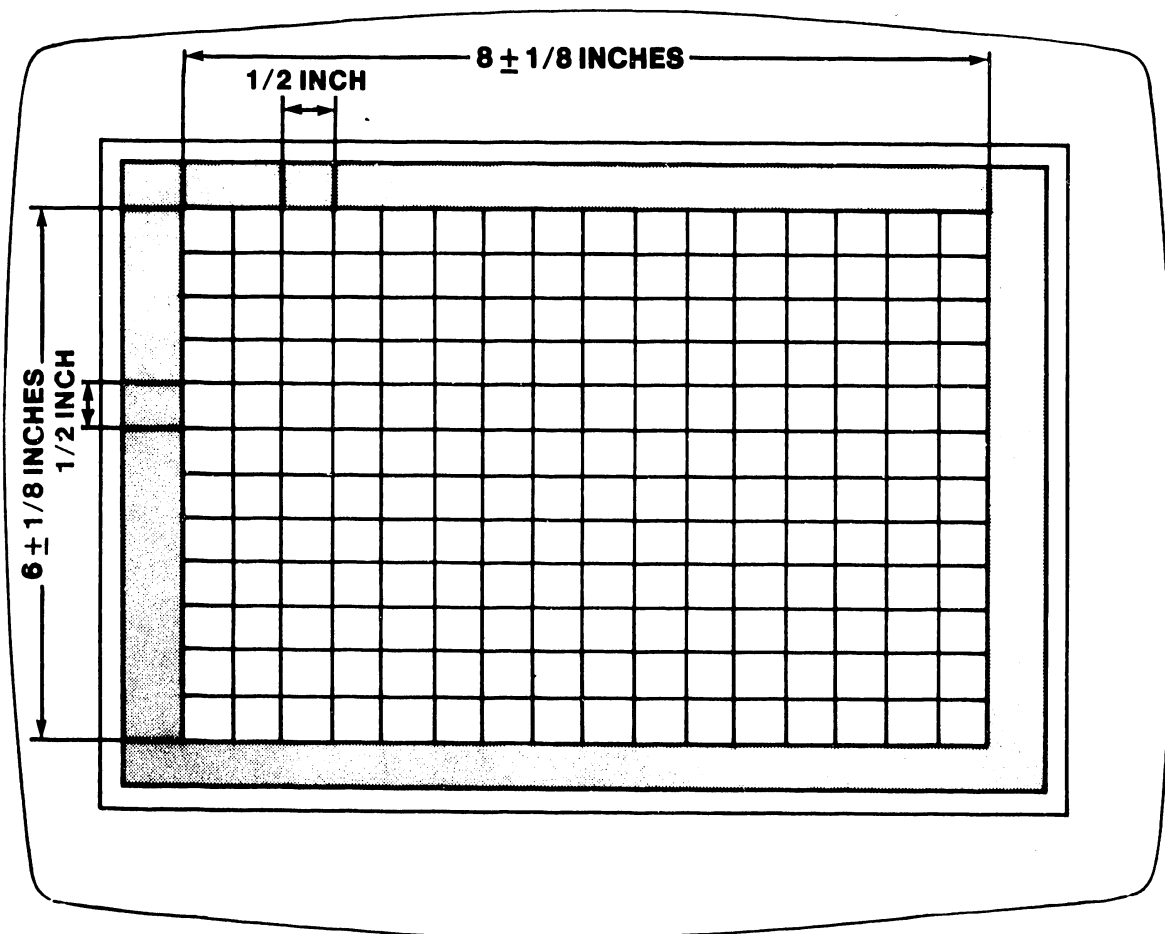
5.3.4.2 4220 DTOS Monitor Alignment

WARNING: High voltage is present in the vicinity of the Monitor PCA. Most adjustments will be made from the solder side of the PCA through labeled access holes. Use extreme caution in making these adjustments to prevent coming in contact with dangerous voltages.

5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.2 4220 DTOS Monitor Alignment

1. Select the Monitor alignment routine resident in the VS DTOS package. This routine contains four different patterns for use in aligning the Monitor. Only two patterns, the grid and the circle, will be used in the following procedure.
2. Select the grid alignment pattern for display on the workstation Monitor.



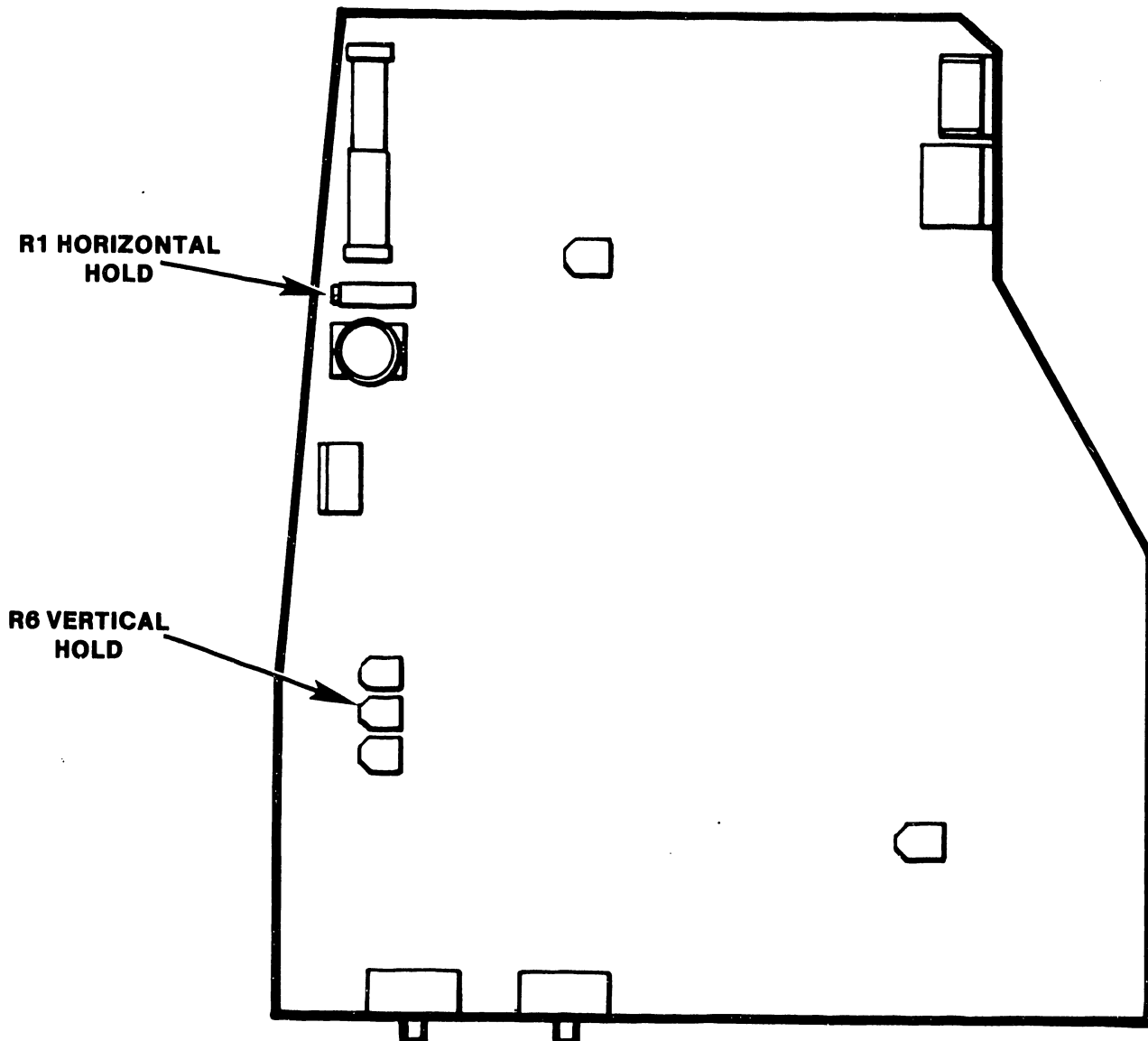
B-01556-FY84-82

Figure 5-9. VS DTOS Grid Display Pattern

5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.2 4220 DTOS Monitor Alignment, continued

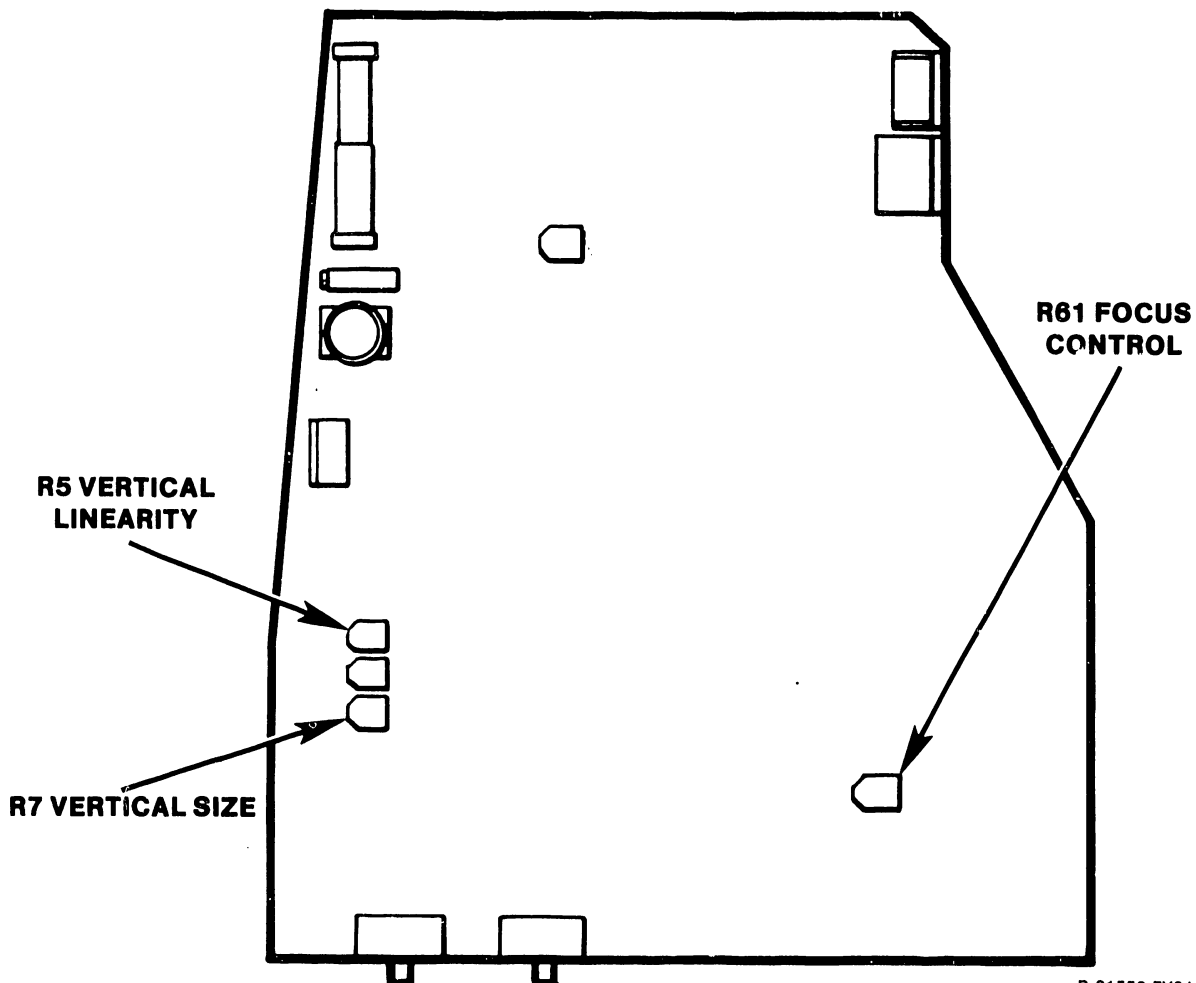
3. Adjust the Monitor brightness control to adequately display the grid alignment pattern. Do not adjust brightness so high as to cause display of the raster or cause blooming.
4. Adjust vertical hold control R6 to the center of its stable range.
5. Adjust horizontal hold control R1 to the center of its stable range.



5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.2 4220 DTOS Monitor Alignment, continued

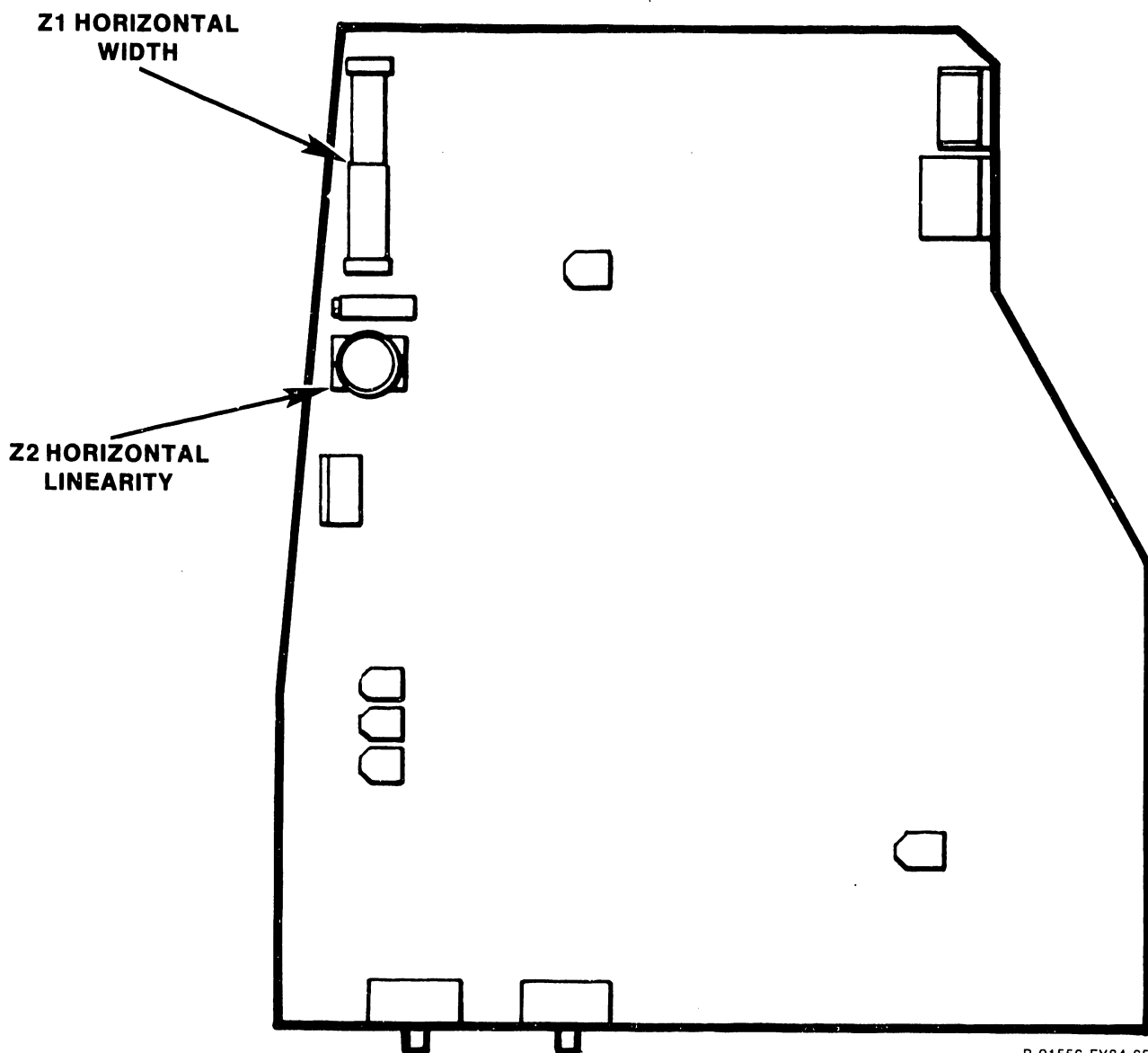
6. Adjust focus control R61 for the sharpest overall display pattern.
7. Adjust vertical size control R7 so that the display pattern is $6 \pm 1/8$ inches ($15.2 \text{ cm} \pm 3 \text{ mm}$) high. Use a standard or metric scale.
8. Adjust vertical linearity control R5 so that the squares at the top of the display are the same vertical size as the squares at the bottom of the display. This adjustment may affect the vertical height adjustment. Repeat step 7 if required.



5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.2 4220 DTOS Monitor Alignment, continued

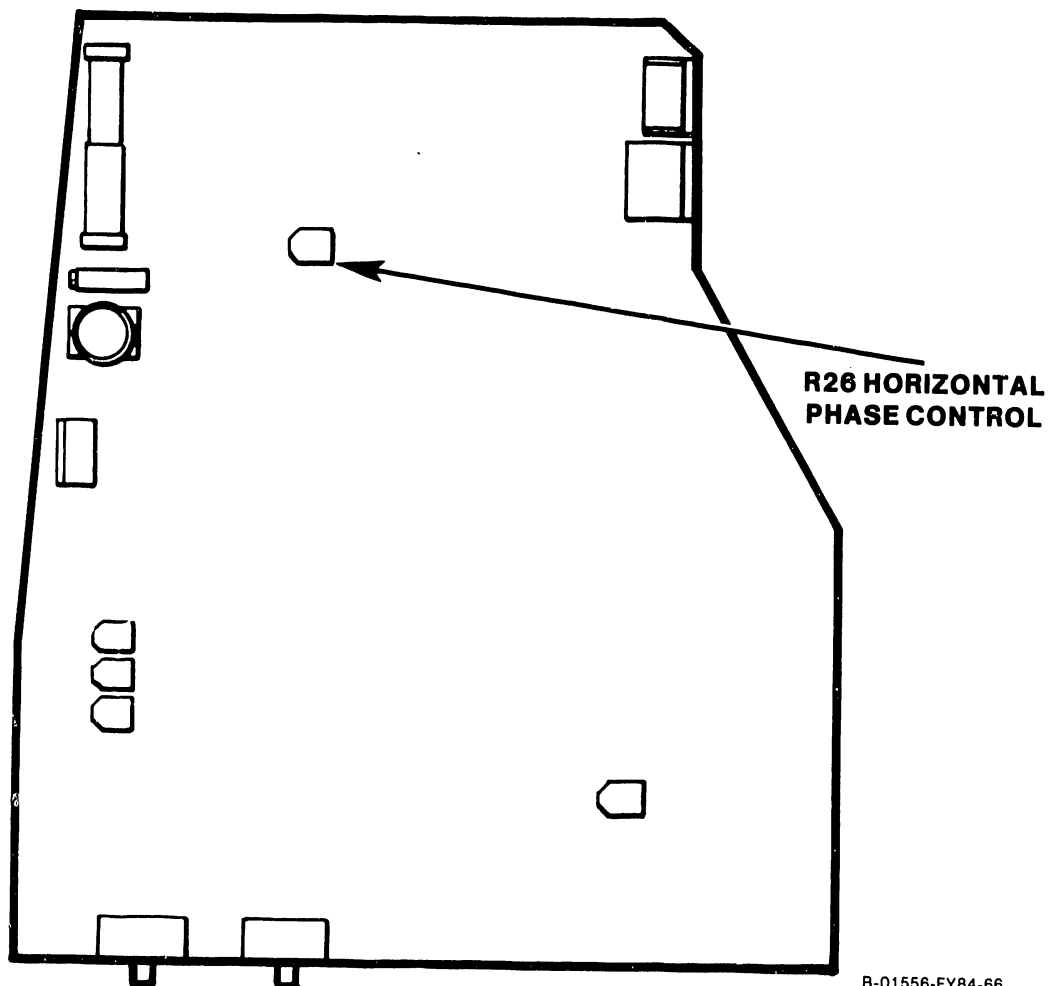
9. Adjust horizontal width coil Z1 so that the display pattern is $8 \pm 1/8$ inches ($20.3 \text{ cm} \pm 3 \text{ mm}$) wide. Use a standard or metric scale.
10. Adjust horizontal linearity coil Z2 so that the squares at the left of the display are the same horizontal size as the squares at the right of the display. This adjustment may affect the horizontal width adjustment. Repeat step 9 if required.



5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.2 4220 DTOS Monitor Alignment, continued

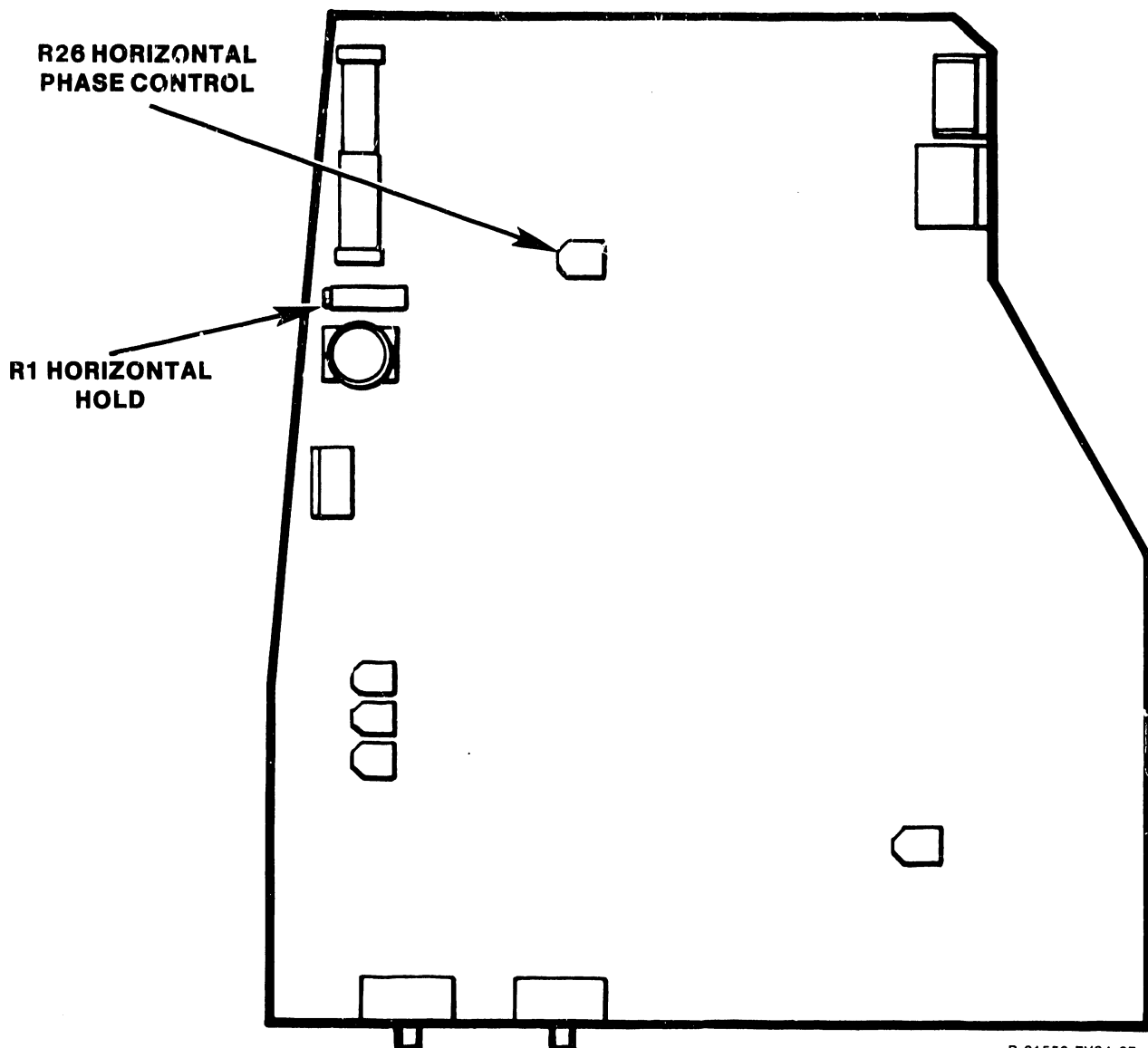
11. Select the circle alignment pattern in the Monitor alignment routine in the VS DTOS package. A visual check of the circles displayed should reveal no noticeable distortion, i.e., no egg-shaped or oblong forms. Repeat steps 7 through 11 if necessary.
12. With the circle alignment pattern still selected, adjust the Brightness control to display the raster, but not so high as to cause blooming. Adjust horizontal phase control R26 completely counterclockwise.



5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.2 4220 DTOS Monitor Alignment, continued

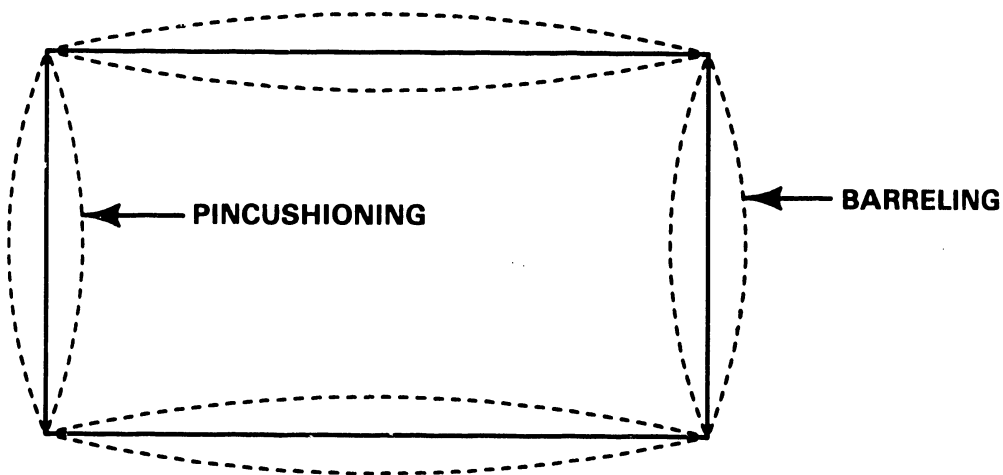
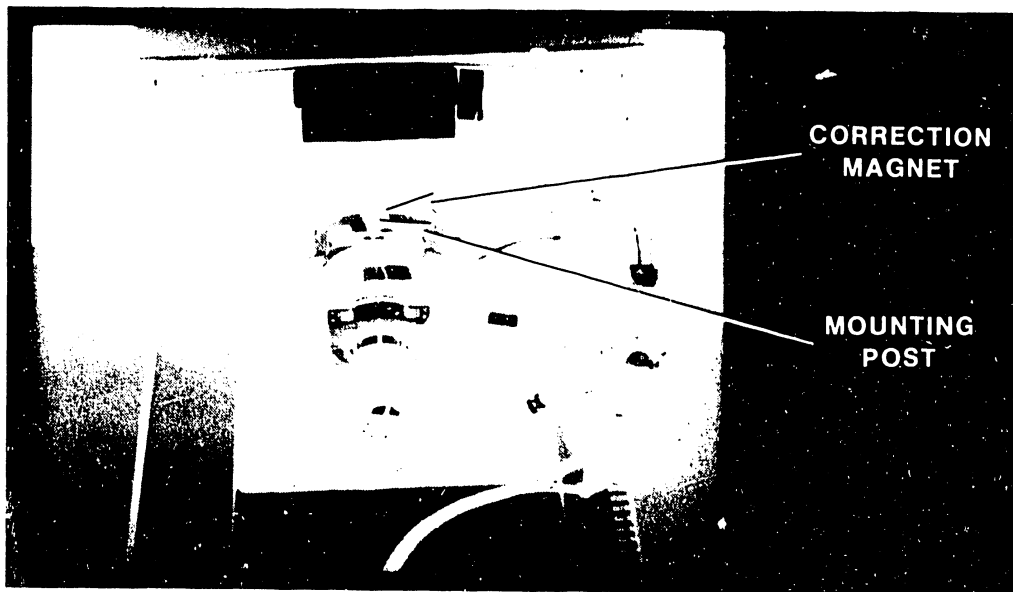
13. Adjust horizontal hold control R1 clockwise so that the video pattern overlaps at the left edge of the display, and touches the left edge of the two left-most circles.
14. Adjust horizontal phase control R26 to center the display pattern in the raster. Return to the grid pattern and proceed with the next step.



5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.2 4220 DTOS Monitor Alignment, continued

15. Adjust the two tabs on the rear cover of the deflection yoke around the CRT neck one at a time to center the raster on the face of the CRT.
16. Using a non-metallic straight-edge (plastic ruler, envelope, etc.) for comparison, check each perimeter line of the video display pattern for pincushioning or barreling distortion. The lines should be straight to within $\pm 1/16$ inch (1.5 mm).



5.3.4 DTOS MONITOR ALIGNMENT, continued

5.3.4.2 4220 DTOS Monitor Alignment, continued

17. If either type of distortion exceeds $\pm 1/16$ inch (1.5 mm), adjust the magnets mounted on the posts around the perimeter of the deflection yoke. Rotate the magnet closest to the area of greatest distortion to make the correction.
18. If correction is not possible with the magnets mounted around the yoke, magnets can be added as required to correct the distortion. This generally involves replacing an existing magnet with one of a higher gauss value. The magnets, their color coding and part numbers are listed below.

<u>MAGNET COLOR CODE</u>	<u>VALUE</u>	<u>PART NUMBER</u>
Green	Gauss 11	320-0126
Blue	Gauss 15	320-0128
White	Gauss 20	320-0127

If the above procedure does not bring the Monitor into tolerance, replacement is recommended. If the Monitor can be aligned satisfactorily, power off the workstation and reassemble the Monitor.

5.4 ELECTRONICS BASE REMOVAL/REINSTALLATION PROCEDURES

This section contains instructions regarding the removal and reinstallation of the major components of the Electronics Base, including the internal PCAs and Power Supply. Before attempting any of these procedures, complete the following set up procedures:

- o Set the workstation I/O switch to 0 (off) and remove the ac power cord from the ac outlet.
- o Disconnect the Monitor and Keyboard from the Electronics Base and move them out of the working area.
- o Disconnect the dual coaxial cable from the DATA LINK connectors on the rear of the Electronics Base.

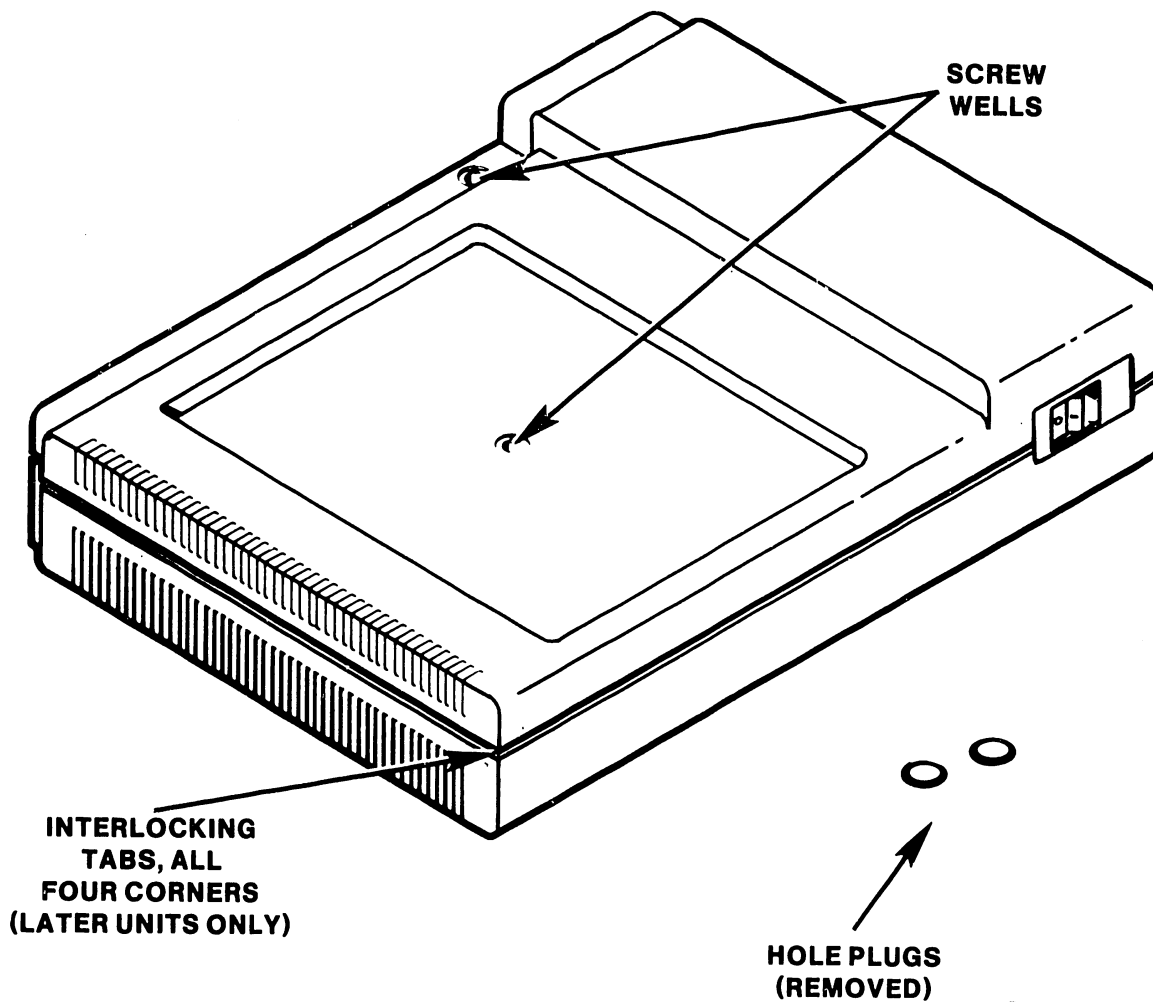
5.4.1 ELECTRONICS BASE COVER

Two types of base covers are presently in the field. Early units have covers equipped with a Velcro^R patch affixed to their front right corner. This patch interlocks with a mating patch of Velcro^R on the top of the Power Supply. Later units have covers with extensions that reach down into the base to interlock with the ventilation slots in each corner. The procedure below addresses both cover designs.

Velcro is a registered trademark of Velcro Industries, N.V.

5.4 BASE REMOVAL/REINSTALLATION, continued**5.4.1 ELECTRONICS BASE COVER, continued**

1. Referring to Figure 5-8, lift two decorative hole plugs out of the Electronics Base top cover.
2. Completely loosen, but do not remove, two phillips screws located in the screw wells under the hole plugs.



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Figure 5-8. Removing the Electronics Base Cover

5.4 BASE REMOVAL/REINSTALLATION, continued

5.4.1 ELECTRONICS BASE COVER, continued

NOTE: The connector headers on the rear edges of the internal PCAs interlock with each other and/or the cover and base parts of the Electronics Base unit. In the next step, be certain to separate the cover from the PCA(s) by holding the PCA connector header(s) in position when lifting the cover off.

3. On later units, use a small coin or flat-bladed screwdriver to disengage the cover extensions from the ventilation slots in each corner of the base. Push the interlocking tabs inward while pulling the corner away from the base.

5.4 BASE REMOVAL/REINSTALLATION, continued

5.4.1 ELECTRONICS BASE COVER, continued

4. Lift the cover off of the Electronics Base. On early units the front right corner of the cover is secured to the top of the Power Supply internally by a patch of Velcro^R and will offer some resistance when removing the cover.

To reinstall the Electronics Base cover, reverse the above procedure giving special attention to the following items:

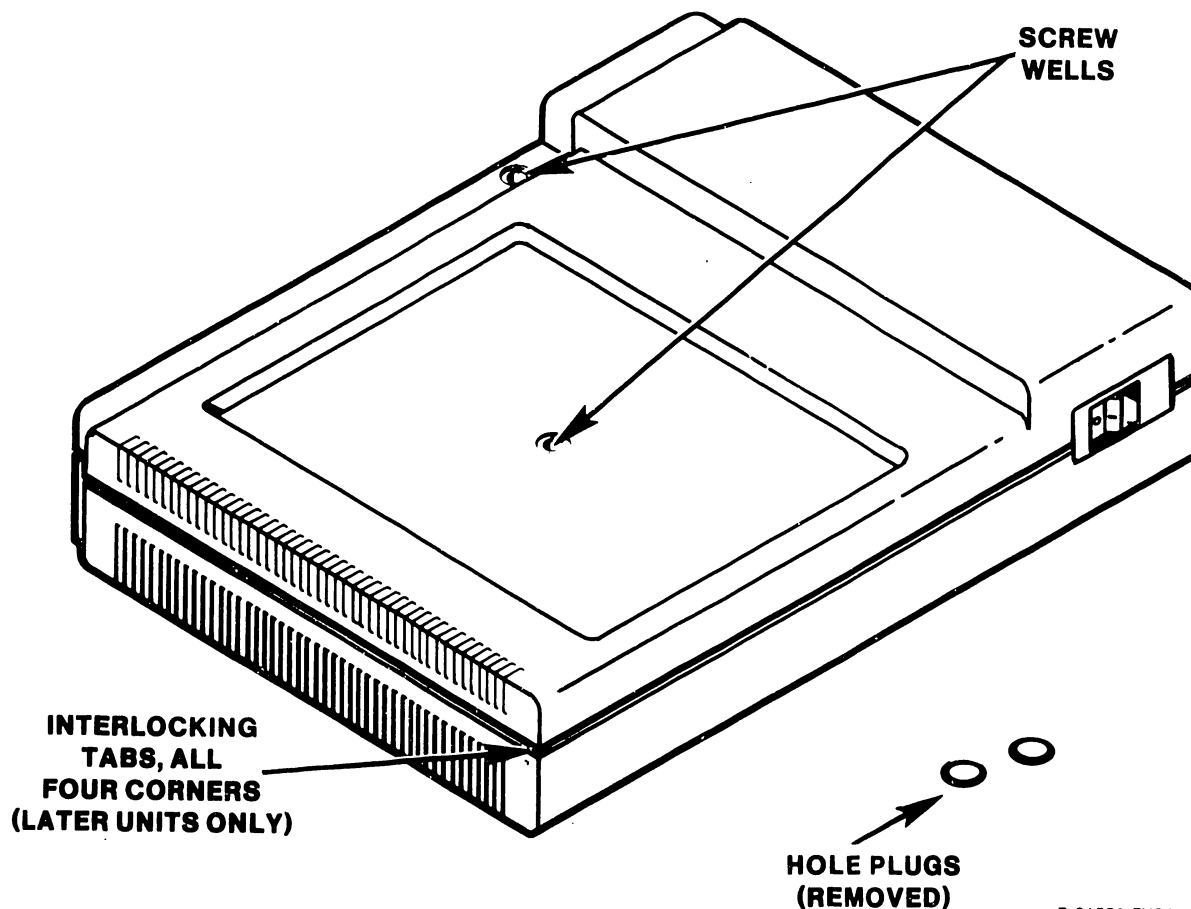
- o Check around the perimeter of the Electronics Base cover to make sure that the cover interlocks properly with the base, the PCA connector header(s) at the rear and the insert around the Power Supply I/O switch.
- o On later units, ensure that the cover extensions are interlocked in the ventilating slots in each corner of the base.
- o Do not over-tighten the cover screws when reinstalling the Electronics Base cover. Tighten the screws until they are just snug.
- o After the cover is installed and the screws are secured, press down on the front right corner of the cover to interlock the Velcro^R patch (early units).

5.4 BASE REMOVAL/REINSTALLATION, continued

5.4.2 POWER SUPPLY

WARNING: Do not open the switching Power Supply under any circumstance. Extremely dangerous voltage and current levels in excess of 300 volts and unlimited current are present within the Power Supply. Do not attempt to repair the switching Power Supply; it is field replaceable only. After powering the unit down and disconnecting the ac power plug from the wall outlet, allow one minute before removing the Power Supply to provide adequate time for residual voltage to drain through the bleeder resistors.

1. Remove the Electronics Base cover per section 5.4.1.



5.4 BASE REMOVAL/REINSTALLATION, continued

5.4.2 POWER SUPPLY

2. Referring to Figure 5-9, remove two screws securing the Power Supply to the Electronics Base, and lift the Power Supply out to the extent of its connecting harness.
3. Grasp the molex connector (not the harness wires) firmly and unplug the Power Supply harness from the PCA(s) in the base. Remove the Power Supply.

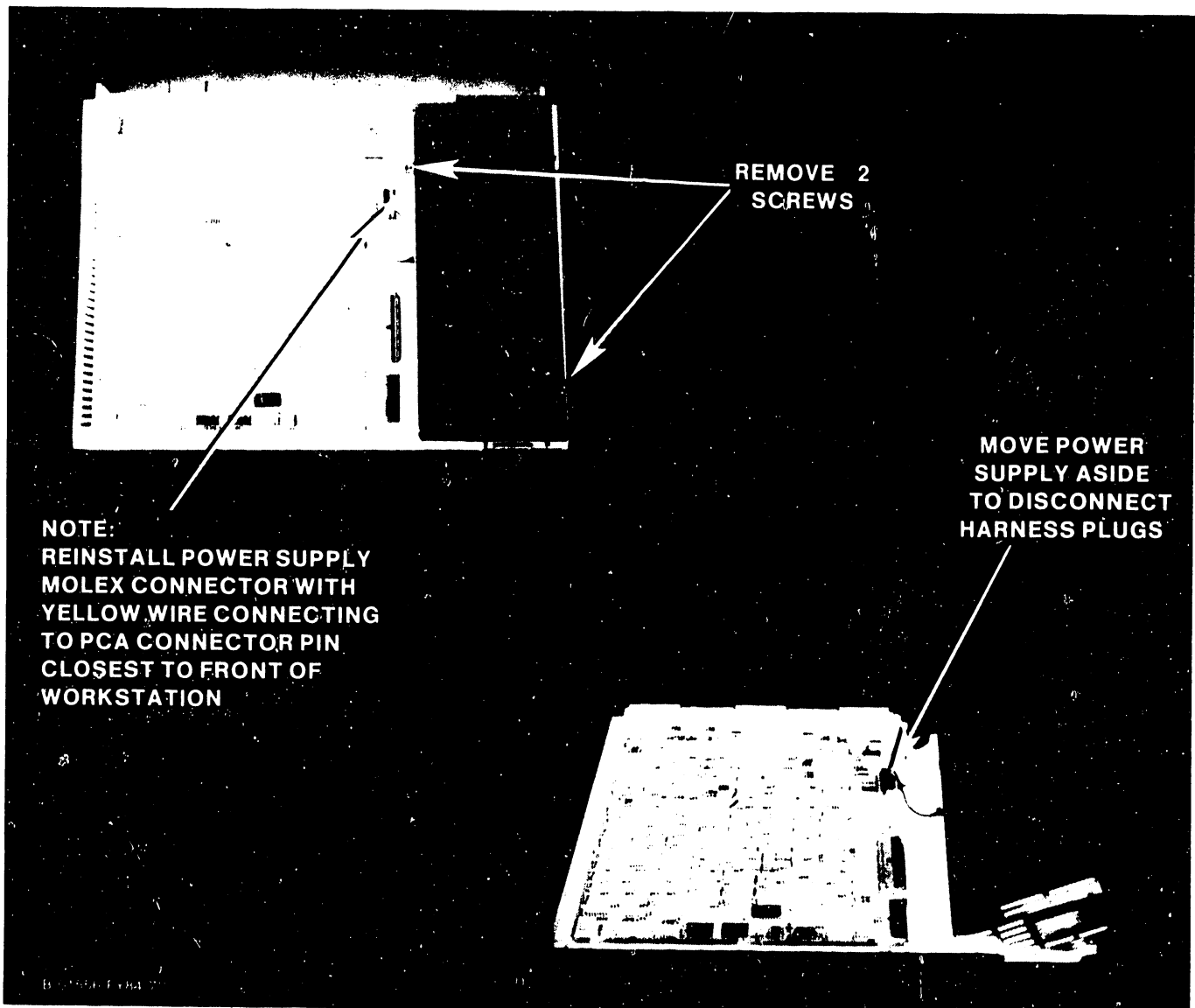


Figure 5-9. Removing the Power Supply

5.4 BASE REMOVAL/REINSTALLATION, continued

5.4.2 POWER SUPPLY, continued

To reinstall the Power Supply, reverse the removal procedure giving special attention to the following items:

- o Reconnect the Power Supply plug with the yellow wire to the pin closest to the front of the workstation. Ensure that the molex connectors mate with the pins on the PCAs correctly. Shifting the connectors to the left or right could seriously damage the PCAs.
- o If the Power Supply is being replaced, transfer the ac power cord from the original unit to the replacement. If the replacement Power Supply does not have a Velcro^R patch attached on the top front of its cover, install one (early units). The part number for this patch is 458-3309.
- o Replacement power supplies will also need to have the insert around the I/O switch installed. This is a snap-in type plastic insert which, in most cases, will not be able to be removed from the original unit without damage. Order an extra insert for each replacement power supply.
- o Do not over-tighten the Power Supply screws. Tighten until snug.

5.4 BASE REMOVAL/REINSTALLATION, continued
5.4.3 PRINTED CIRCUIT ASSEMBLIES (PCAs)

The following procedure addresses both the double board 4210 Workstation and the single board 4220 Workstation. The latter is similar to the 4210 except for the I/O ribbon cable, which is not used. When using this procedure for the 4220 Workstation, skip steps 3, 4 and 6.

1. Remove the Electronics Base cover per section 5.4.1.
2. Remove the switching Power Supply per section 5.4.2.
3. Press the locking arms on both sides of the I/O ribbon cable connector outward to disengage the cable from the connector on the top (8264 CPU) PCA. Disconnect the cable from the connector (Figure 5-10a).

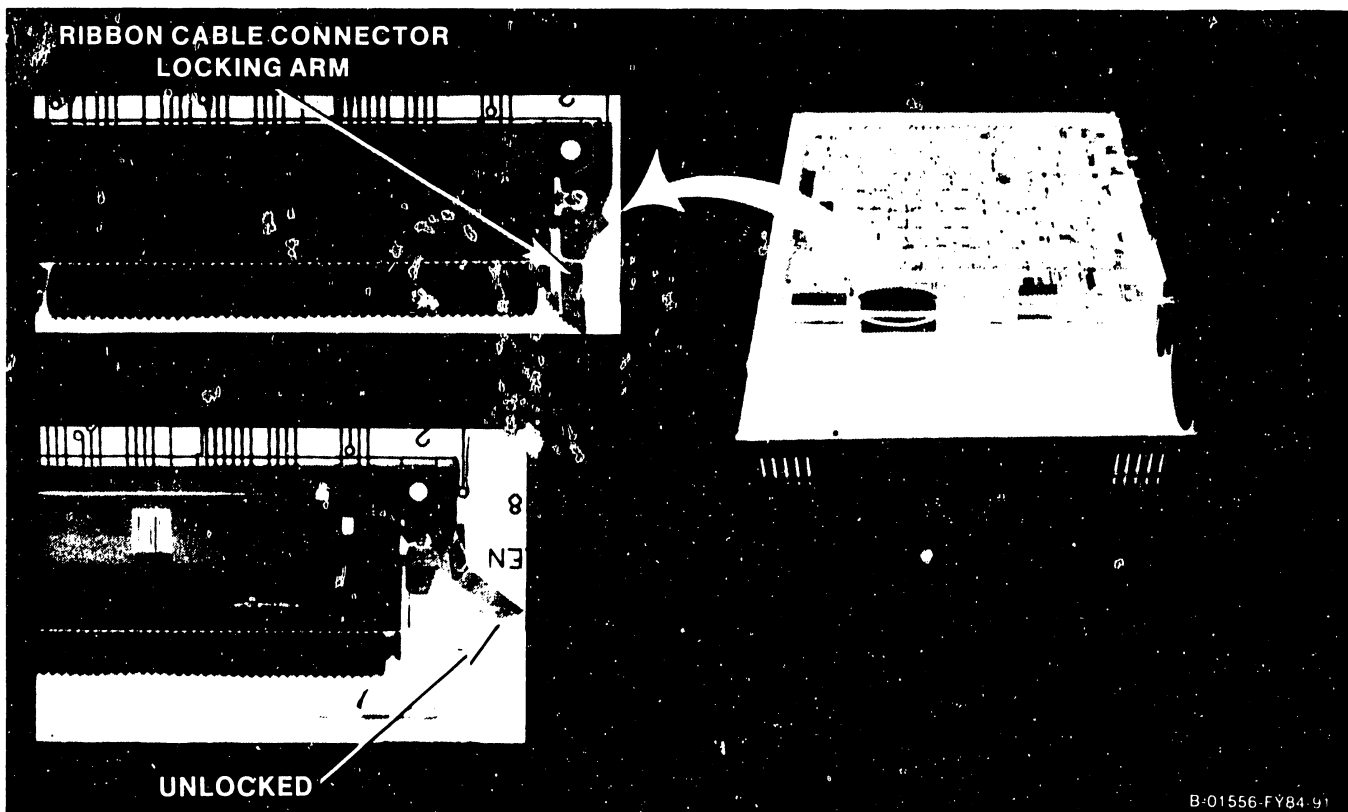


Figure 5-10. Removing the PCAs
(4210 Shown)

5.4 BASE REMOVAL/REINSTALLATION, continued
5.4.3 PRINTED CIRCUIT ASSEMBLIES, continued

4. Lift up the rear edge of the 8264 CPU PCA and move it rearward to disengage it from its capture slots in the front of the base.

CAUTION: Do not misplace the center support/spacer. It both supports the Monitor on top of the Electronics Base and maintains proper spacing of the PCAs within the Base.

5. Remove the center support/PCA spacer from its center hole in the lower PCA. Retain the support/spacer for reinstallation.

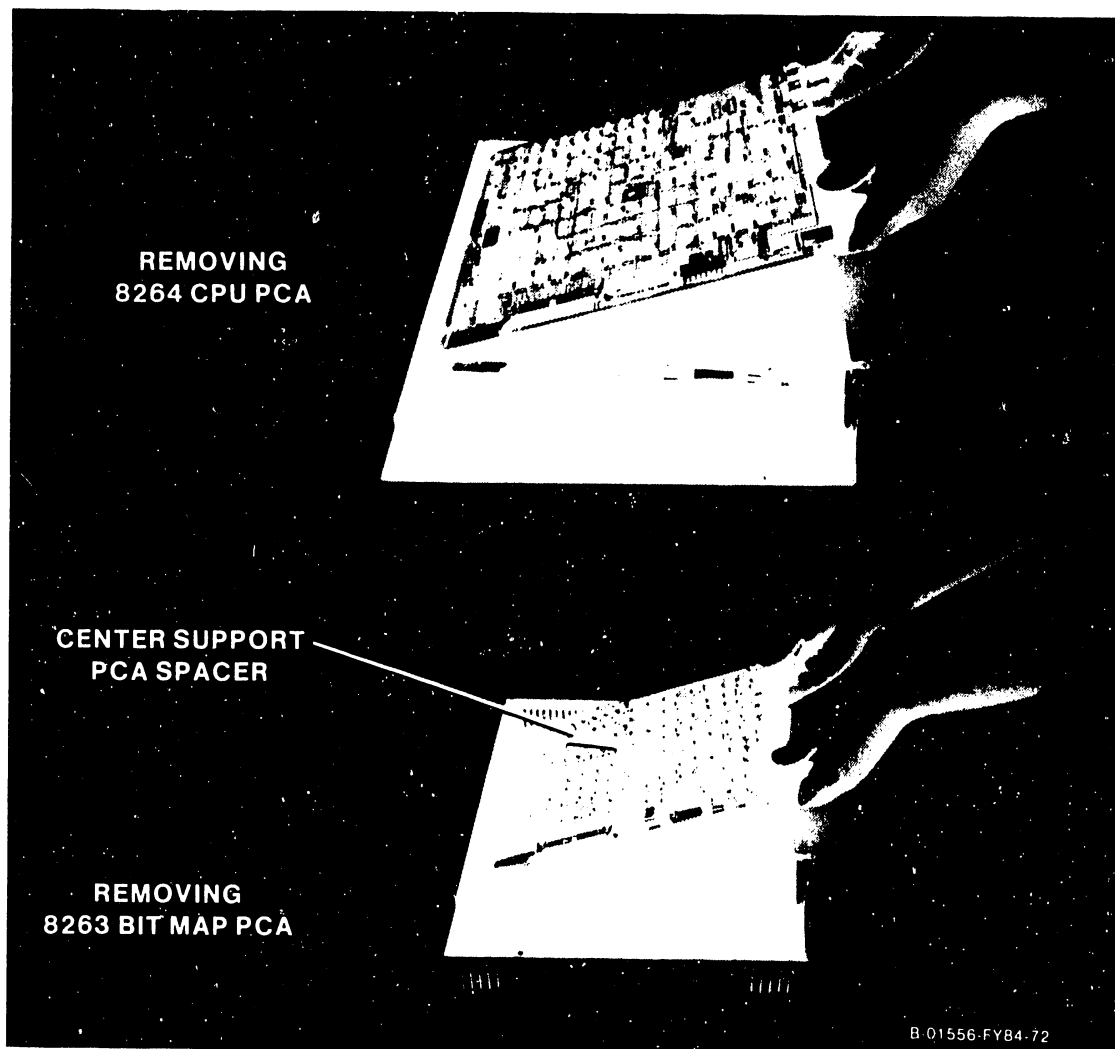
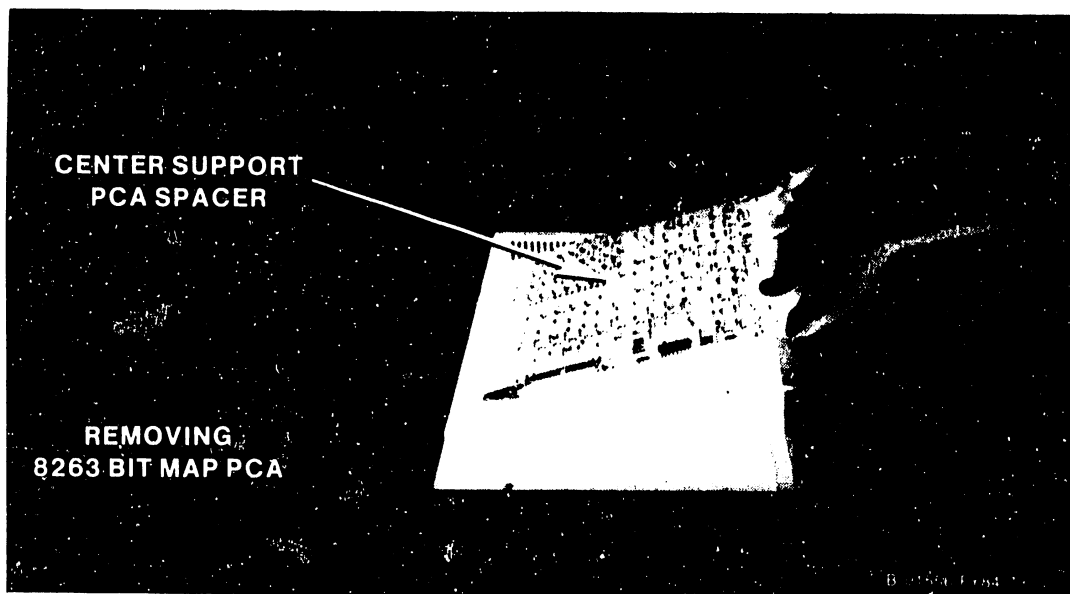


Figure 5-10b. Removing the PCAs

5.4 BASE REMOVAL/REINSTALLATION, continued

5.4.3 PRINTED CIRCUIT ASSEMBLIES, continued

6. Press the locking arms on both sides of the I/O ribbon cable connector outward to disengage the cable from the connector on the bottom (8263 Bit Map) PCA. Disconnect the cable from the connector.
7. Lift up the rear edge of the 8263 Bit Map PCA (4210) or the 8277 Remote Workstation Electronics PCA (4220) and move it rearward to disengage it from its capture slots in the front of the base.



5.4 BASE REMOVAL/REINSTALLATION, continued

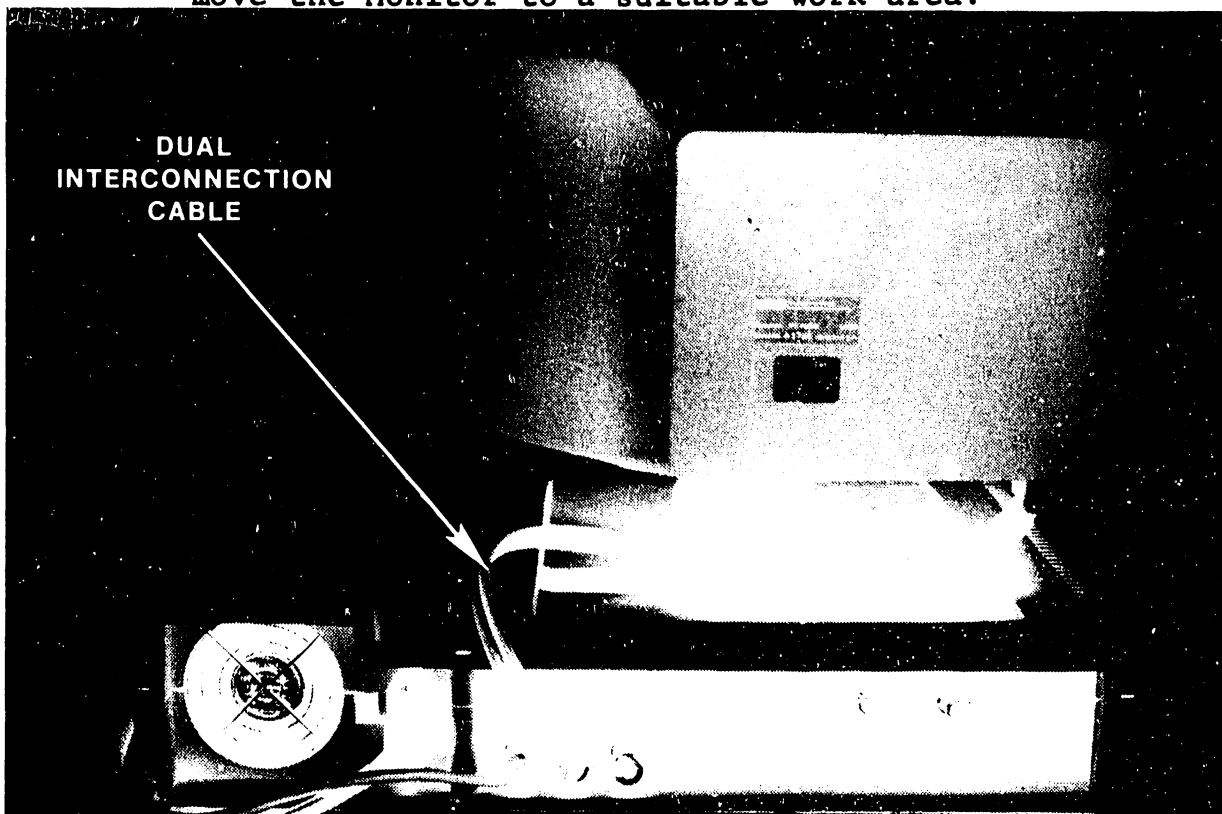
5.4.3 PRINTED CIRCUIT ASSEMBLIES, continued

To reinstall the PCAs, reverse the removal procedure, giving special attention to the reinstallation of the center support/spacer.

5.5 MONITOR REMOVAL/REINSTALLATION PROCEDURES

This section contains instructions for removal and reinstallation of the major components of the Monitor. Before attempting any of these procedures, make the following preparations:

- o Set the workstation I/O switch to 0 (off).
- o Disconnect the Monitor dual interconnection cable from the underside of the Monitor, and move the Monitor to a suitable work area.



5.5 MONITOR REMOVAL/REINSTALLATION, continued**5.5.1** **REMOVING THE MONITOR COVER**

1. Turn the monitor upside down, resting it on its top. Remove the two screws that hold the cover to the faceplate. Stand the monitor up on its pedestal (Figure 5-11).

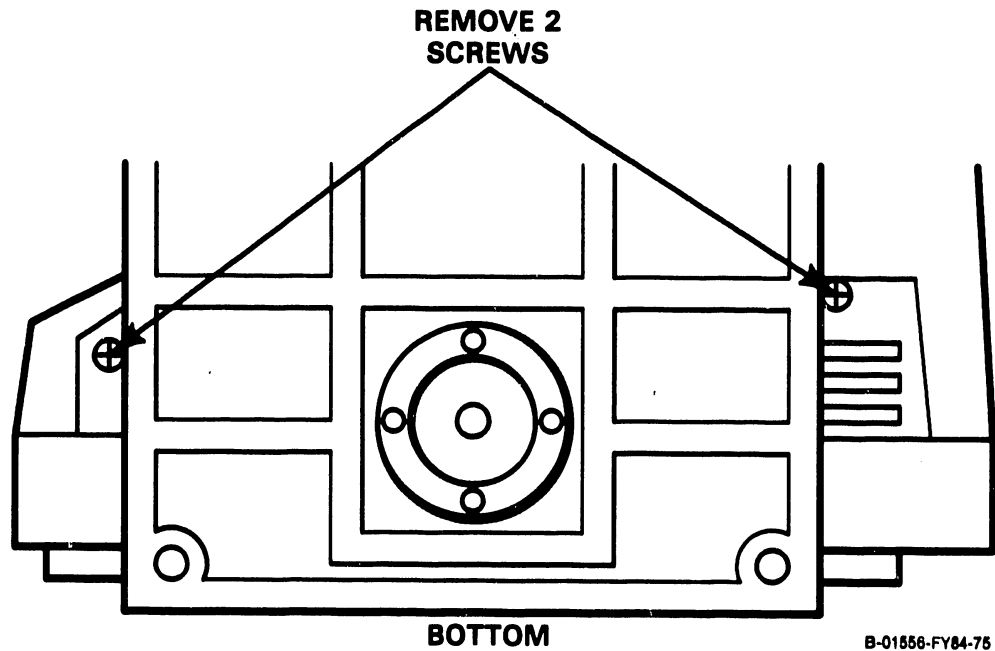


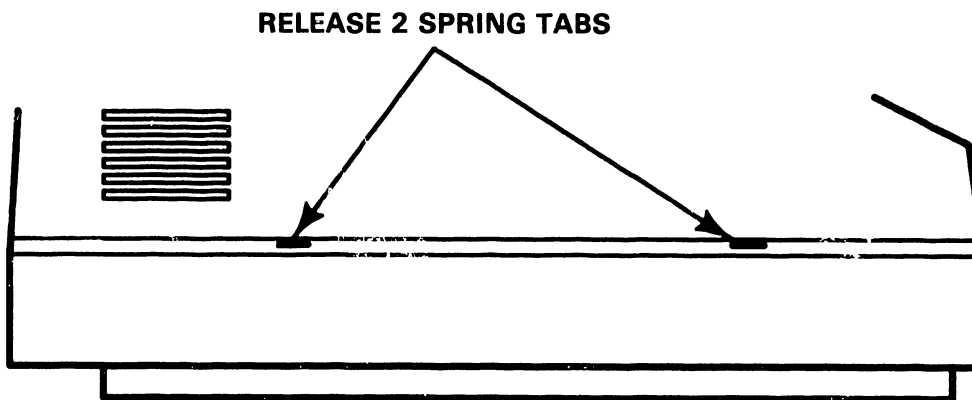
Figure 5-11a. Removing the Monitor Cover

5.5 MONITOR REMOVAL/REINSTALLATION, continued

5.5.1 REMOVING THE MONITOR COVER, continued

CAUTION: Do not twist the screwdriver while performing the Monitor cover removal in the next step, or the cover will be damaged.

2. Locate the two spring locking tabs on the top of the Monitor along the seam where the cover meets the faceplate.
3. Using a small, flat-blade screwdriver, push the right-hand spring tab down through its slot to free the cover on the right side.
4. Holding the right side of the cover free, push the left-hand spring tab down through its slot to free the cover on the left side.



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Figure 5-11b. Removing The Monitor Cover

5.5 MONITOR REMOVAL/REINSTALLATION, continued

5.5.1 REMOVING THE MONITOR COVER, continued

5. Remove the cover by pulling it straight back, clearing the neck of the CRT.

WARNING: Before proceeding with any further removal/reinstallation work inside the Monitor, perform the CRT Anode Discharge Procedure in section 5.5.2.

To reinstall the cover, reverse the removal procedure, with the exception of steps 2, 3 and 4. Simply slide the cover back in place, pressing it gently against the face plate, causing the spring tabs to lock in place.

5.5 MONITOR REMOVAL/REINSTALLATION, continued

5.5.2 CRT ANODE DISCHARGE PROCEDURE

Even with power removed, the Monitor cathode ray tube (CRT) can hold a charge of several thousand volts. To eliminate the risk of accidental CRT discharge which can result in serious injury, discharge the CRT anode as follows:

1. Attach one end of a length of insulated wire to the metal shaft of a plastic-handled, heavy-duty screwdriver.
2. Attach the other end of the wire to chassis ground.
3. Using a non-conductive tool such as a plastic alignment tool, carefully raise the edge of the rubber anode cap high enough to insert the screwdriver.
4. Taking care not to touch the metal shaft of the screwdriver or any metal part of the workstation, discharge the CRT anode by touching the anode clip with the grounded screwdriver.
5. After discharging the CRT, remove the grounding wire and reseal the rubber anode cap.

5.5.3 MONITOR PCA

1. Remove the cover per section 5.5.1.
2. Remove the Brightness and Contrast control knobs located on the front upper left of the Monitor by pulling them straight out.
3. Unplug the CRT cable connector from J1 located at the rear of the Monitor PCA.

5.5 MONITOR REMOVAL/REINSTALLATION, continued

5.5.3 MONITOR PCA, continued

4. Disconnect the FASTON clip from the retaining screw ground lug located at the top left side near the Brightness and Contrast potentiometers.
5. Disconnect the CRT socket connector.
6. Disconnect the high-voltage anode connector from the CRT.
7. Using a flat-bladed screwdriver with a long shaft, unscrew the Monitor PCA holding screw securing the PCA to the faceplate.
8. Remove the Monitor PCA.

To reinstall the Monitor PCA, reverse the removal procedure.

5.6 KEYBOARD REMOVAL/REINSTALLATION PROCEDURES

The removal/reinstallation procedure for the Keyboard cover is presented below.

1. Disconnect the Keyboard cable from its connector on the rear of the Electronics Base.
2. Referring to Figure 5-12, turn the Keyboard top down on a suitable work surface and remove two screws on the bottom.

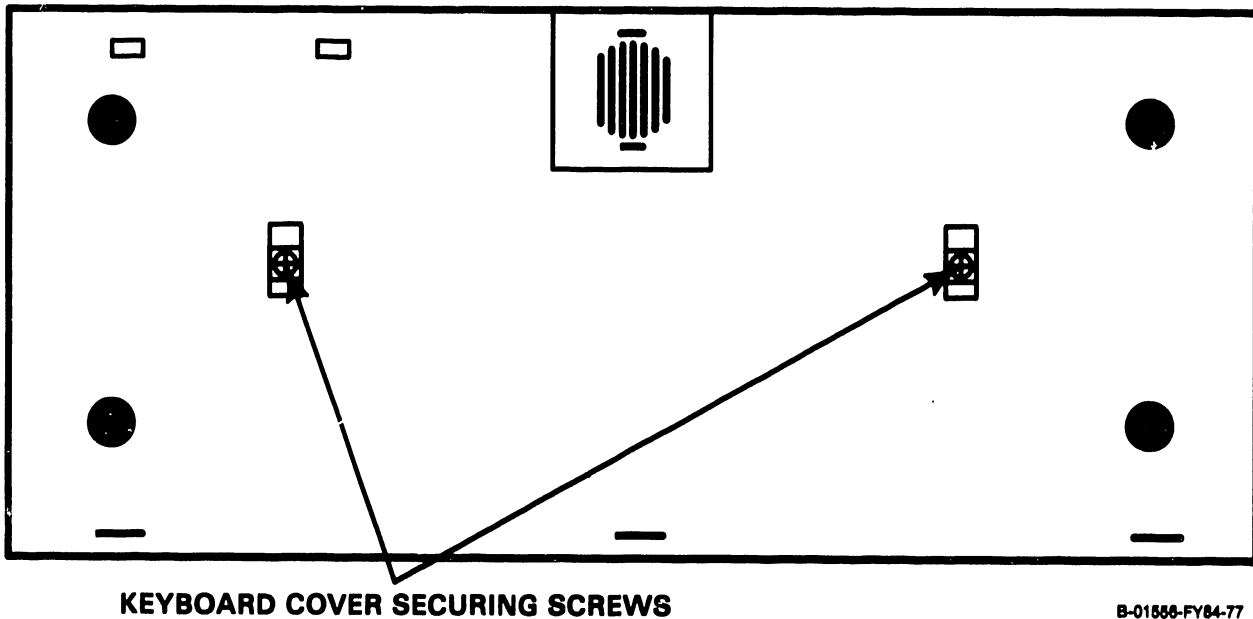


Figure 5-12. Removing the Keyboard Cover

5.6 KEYBOARD REMOVAL/REINSTALLATION, continued

3. Holding the top and bottom halves of the Keyboard together, turn the unit face up and place on the work surface.
4. Lift the top cover off of the Keyboard, being careful to retain the two circular collars around each of the screw holes.

To reinstall the Keyboard cover, reverse the removal procedure being sure that the circular collars around the Keyboard screw holes are in place.

5.7 SWITCH SETTINGS

The 4210 Workstation is shipped with all internal switches preset for proper operation. This eliminates the need for CE personnel to disassemble the Electronics Base unit and Keyboard at installation to access internal switches. The switch settings given in sections 5.7.1 and 5.7.2 are for reference only, as may be required when setting up a replacement 8264 CPU board or Keyboard. (Switch settings for the Keyboard are common to both the 4210 and 4220 Workstation.)

The setting of the 115V/230V Power Supply switch is required at installation to ensure that the Power Supply is set for the ac voltage in use at the installation site. Refer to section 4.3.1 in Chapter 4 for more information on the 115V/230V switch.

5.7 SWITCH SETTINGS, continued

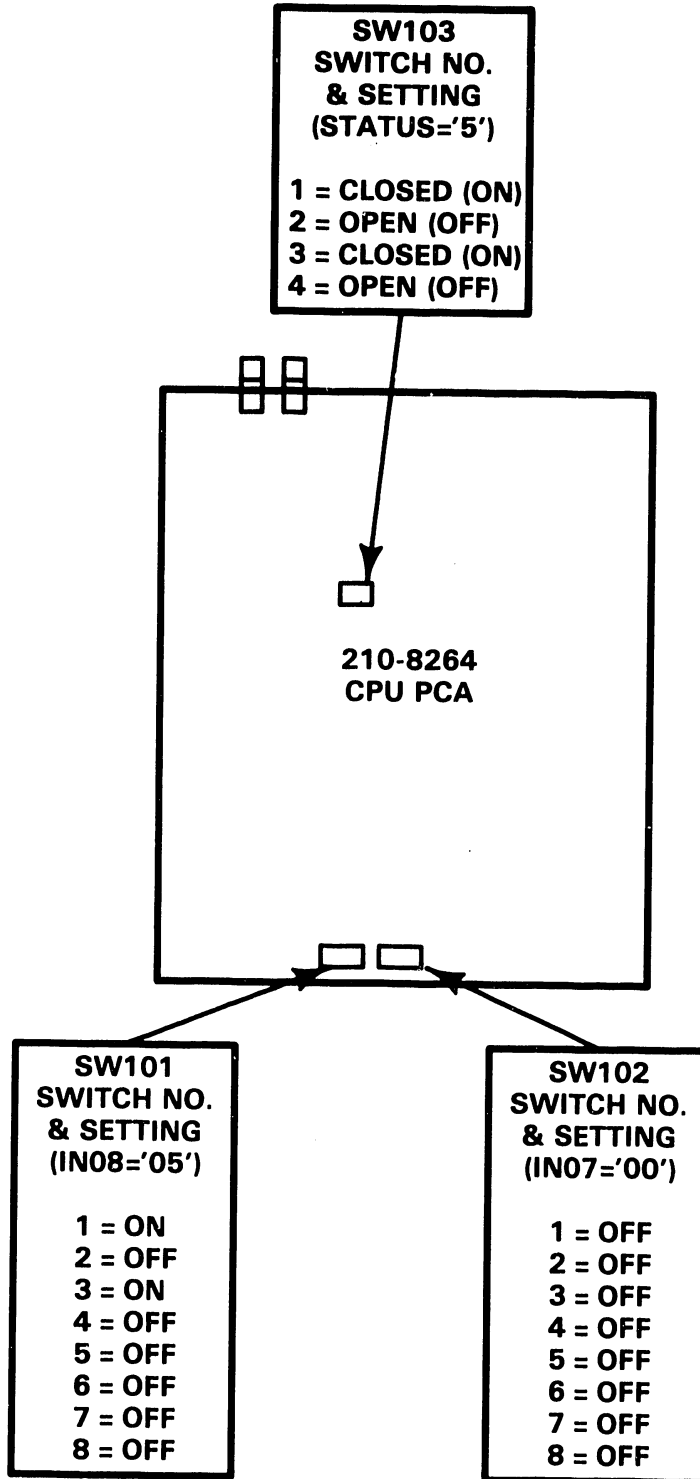
5.7.1 210-8264 CPU PCA SWITCH SETTINGS (4210)

The 210-8264 CPU Board contains three switches which must be set to define the type of terminal to the host system. These switches are SW102, SW101 and SW103 which are read during instructions IN07, IN08 and STATUS respectively. The required switch settings are shown below and illustrated in Figure 5-13.

SW102 SWITCH NO. & SETTING <u>(IN07 = '00')</u>	SW101 SWITCH NO. & SETTING <u>(IN08 = '05')</u>	SW103 SWITCH NO. & SETTING <u>(STATUS = '5')</u>
1 = OFF	1 = ON	1 = CLOSED (ON)
2 = OFF	2 = OFF	2 = OPEN (OFF)
3 = OFF	3 = ON	3 = CLOSED (ON)
4 = OFF	4 = OFF	4 = OPEN (OFF)
5 = OFF	5 = OFF	
6 = OFF	6 = OFF	
7 = OFF	7 = OFF	
8 = OFF	8 = OFF	

5.7 SWITCH SETTINGS, continued

5.7.2 KEYBOARD SWITCH SETTINGS (4210/4220)



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Figure 5-13. 210-8264 CPU PCA Switch Settings
(4210)

5.7 SWITCH SETTINGS, continued

5.7.2 KEYBOARD SWITCH SETTINGS (4210/4220)

The universal, low profile keyboard used with the 4210/4220 Workstations contains two 8-bit DIP switches totaling 16 bits in length. Each universal keyboard is assigned a 15-bit number (bits 0 - 14) that uniquely identifies it. The number codes for all models of the Keyboard are listed in Table 5-1. Models of the Keyboard which are available in expanded format are indicated in the table. The expanded universal keyboard of a particular language is defined by setting the most significant bit (bit 15).

5.7 SWITCH SETTINGS, continued
 5.7.2 KEYBOARD SWITCH SETTINGS (4210/4220)

KEYBOARD	SYMBOL	HEX SWITCH	BINARY SWITCH	EXPANDED AVAILABLE?
Qwerty:US Standard		0000	0000 0000 0000 0000	
Azerty	AZ	0001	0000 0000 0000 0001	
Canadian English	CE	0002	0000 0000 0000 0010	
Canadian French	CA	0003	0000 0000 0000 0011	
German	GE	0004	0000 0000 0000 0100	YES
Spanish Latin	SL	0005	0000 0000 0000 0101	
Swedish	SW	0006	0000 0000 0000 0110	YES
Swiss French	SF	0007	0000 0000 0000 0111	YES
Swiss German	SG	0008	0000 0000 0000 1000	YES
United Kingdom	UK	0009	0000 0000 0000 1001	
Danish	DA	000A	0000 0000 0000 1010	YES
Dutch	NL	000B	0000 0000 0000 1011	YES
Finnish	FI	000C	0000 0000 0000 1100	YES
Flemish	FL	000D	0000 0000 0000 1101	
Italian	IT	000E	0000 0000 0000 1110	
Norwegian	NO	000F	0000 0000 0000 1111	YES
South African	SE	0010	0000 0000 0001 0000	
Spanish/Catalag	SP	0011	0000 0000 0001 0001	
Finnish/Cyrillic	FC	0012	0000 0000 0001 0010	
Greek	GR	0013	0000 0000 0001 0011	
Portuguese	PO	0014	0000 0000 0001 0100	
Arabic	AR	0015	0000 0000 0001 0101	
Azerty/Cyrillic	AC	0016	0000 0000 0001 0110	
Cyrillic	CY	0017	0000 0000 0001 0111	
Czechoslovakia	CZ	0018	0000 0000 0001 1000	
Europe Parliament	EC	0019	0000 0000 0001 1001	
Hungarian	HU	001A	0000 0000 0001 1010	
IADB	IA	001B	0000 0000 0001 1011	
Icelandic	IC	001C	0000 0000 0001 1100	
Multilingual	MU	001D	0000 0000 0001 1101	
PAHO	PH	001E	0000 0000 0001 1110	
Polish	PD	001F	0000 0000 0001 1111	
Qwerty/Azerty	QA	0020	0000 0000 0010 0000	
Romanian	RO	0021	0000 0000 0010 0001	
Serbo-Croatian	SC	0022	0000 0000 0010 0010	
Turkish	TU	0023	0000 0000 0010 0011	
UN Azerty	UA	0024	0000 0000 0010 0100	
UN Qwerty	UQ	0025	0000 0000 0010 0101	
WHO French	WF	0026	0000 0000 0010 0110	
WHO Spanish	WS	0027	0000 0000 0010 0111	
World Lang.	WL	0028	0000 0000 0010 1000	
Arabic Latin	AL	0029	0000 0000 0010 1001	
Cyrillic/Latin	CL	002A	0000 0000 0010 1010	
Greek/Latin	GL	002B	0000 0000 0010 1011	

5.7 SWITCH SETTINGS, continued

5.7.2 KEYBOARD SWITCH SETTINGS (4210/4220)

The 4210/4220 Workstation uses the Qwerty: U.S. Standard Keyboard. Accordingly, its switches (SW1/SW2) must be set to hex 0000, that is, all switches set to the off position (Figure 5-14).

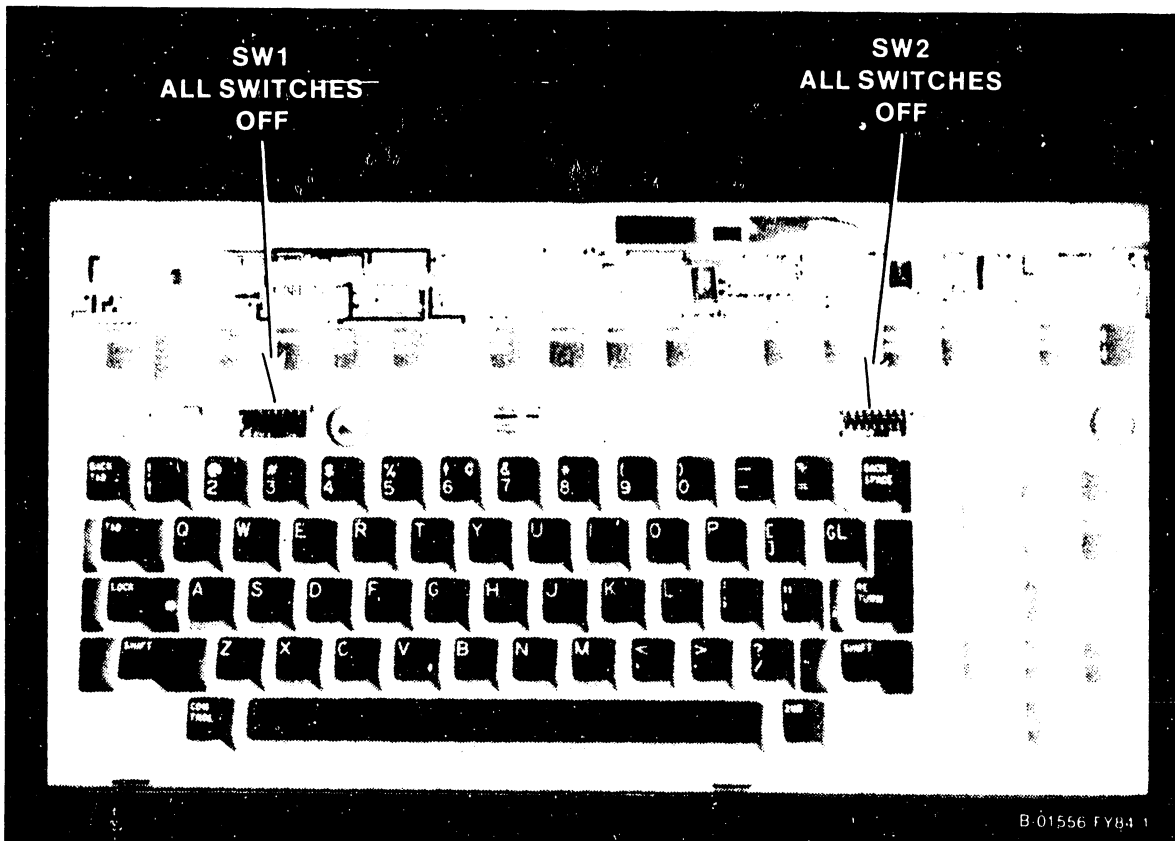


Figure 5-14. Keyboard Switch Settings
(4210/4220)

CHAPTER

6

SCHE-

MATICS

THE SCHEMATICS, WHEN AVAILABLE, ARE ON THE LAST FICHE IN THIS SET.

CHAPTER

7

ILLUSTRATED

PARTS

BREAKDOWN

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CHAPTER 7 ILLUSTRATED PARTS BREAKDOWN

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CHAPTER 7
ILLUSTRATED PARTS BREAKDOWN

This chapter contains illustrated parts breakdowns (IPBs) for the 4210 and 4220 Workstations. The illustrations identify the part numbers of subassemblies referred to throughout the manual in the various maintenance procedures. Some subassemblies are further broken down to identify piece parts for replacement purposes as may be necessary.

7.1 LIST OF ILLUSTRATED PARTS BREAKDOWNS

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Monitor Assembly	7-2	7-2
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7.2 CORPORATE END ITEM (CEI) NUMBERS

Corporate end item part numbers for the major units comprising the 4210 and 4220 Workstations are listed below and should be used when ordering complete assemblies for replacement in the field.

DESCRIPTION	PART NUMBER
4210 Electronics Base Assembly	177-7230
4220 Electronics Base Assembly	177-7229
4210 Monitor Assembly	279-0541*
4210 Keyboard Assembly	279-2042*

(*) Denotes an RSL item.

Table 7-1. Electronics Base Assembly
(Refer to Figure 7-1)

<u>LOC.</u>	<u>DESCRIPTION</u>	<u>P/N</u>
1	Decorative Hole Plugs	655-0293
2	Screw, #8-32 x 3/8, PH PHIL	650-4135
3	Top Cover	450-0917-XB
4	Screw, #8-32 x 2, PH PHIL	650-4643
5	I/O Interconnect Cable	220-3282*
6	CPU PCA	210-8264-A*
7	Bit Map PCA (4210)	210-8263-A*
	Remote WS Electronics PCA (4220)	210-8277-A*
8	Center Support, PCA Spacer	449-0674*
9	Screw, AC Power Cord Mounting	part of item 10
10	AC Power Cord (w/mtg screws item 9)	420-2025
11	Screw, #8-32 x 1/4, PH PHIL	650-4080
12	Washer (used with item 11)	
13	Switching Power Supply	725-2749-11*
14	Switch Insert	449-0676-XC*
15	Base Bottom	450-0916-XC
16	Foot, Self-Adhesive	655-0286

(*) Denotes an RSL item.

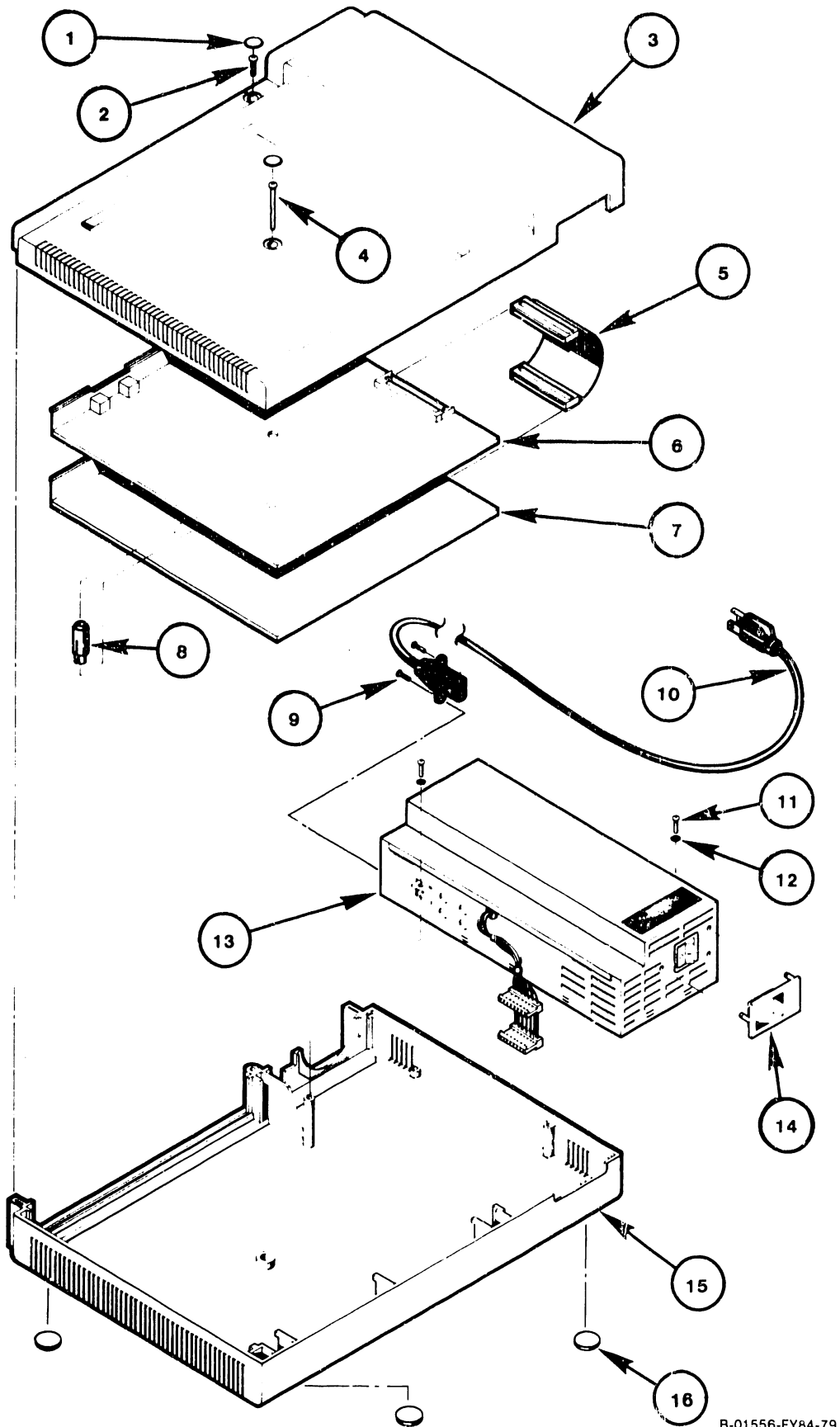
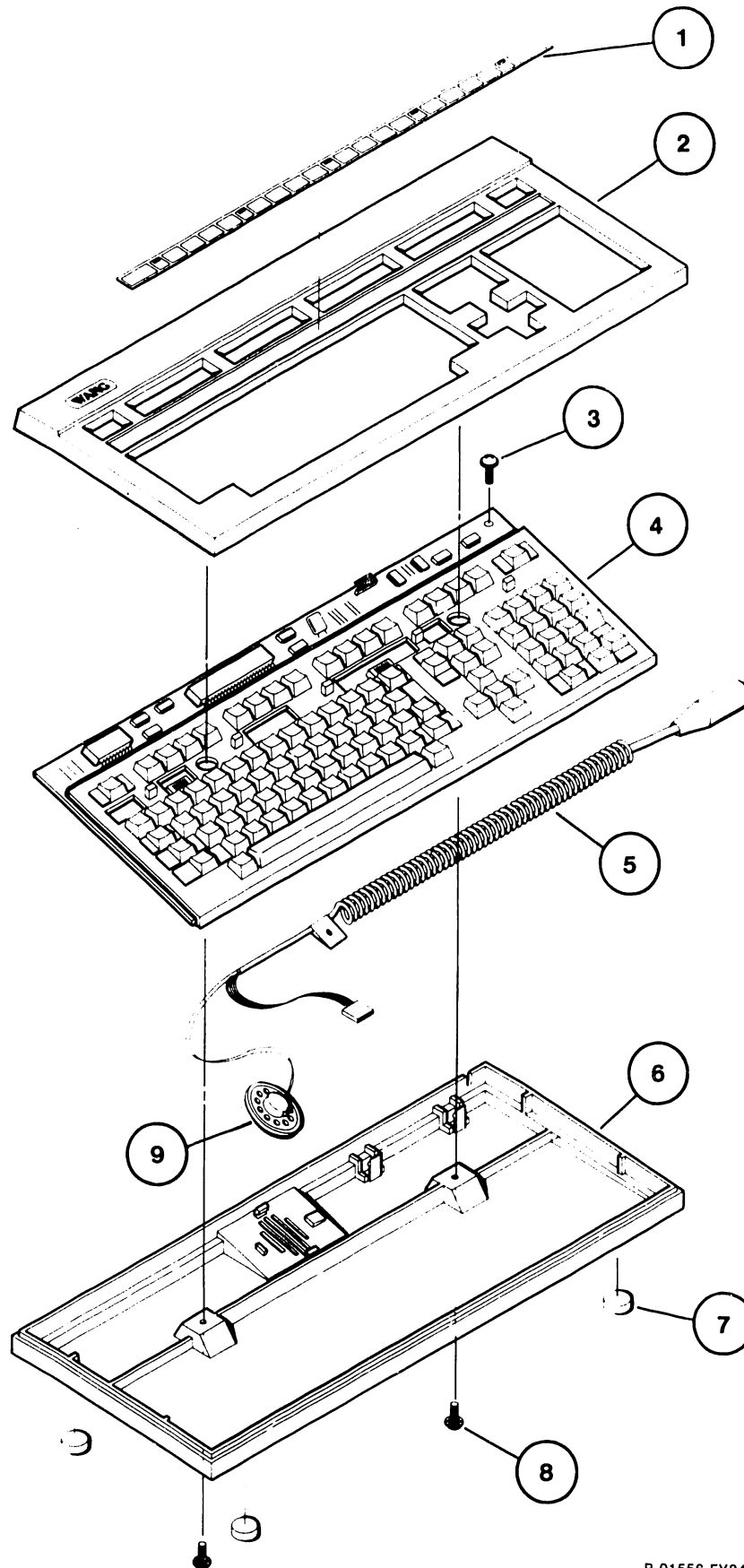


Figure 7-1. Electronics Base Assembly

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Table 7-2. Keyboard Assembly
(Refer to Figure 7-2)

<u>LOC.</u>	<u>DESCRIPTION</u>	<u>P/N</u>
	UNI/KBD-US (United States)	279-2042-US*
	UNI/KBD-UK (United Kingdom)	279-2042-UK*
	UNI/KBD-SL (Spanish-Latin American)	279-2042-SL*
	UNI/KBD-AZ (AZERTY)	279-2042-AZ*
	UNI/KBD-GE (German Expanded)	279-2042-GE*
1	Function Strip	615-2059
2	Cover, Top (Non-Expanded)	449-0608
	Cover, Top (Expanded)	449-0611
3	Screw, 8-32 X 3/8 PAN HD PHIL	650-4120
	Locknut (use with item 3)	652-0029
4	Keyboard, Universal (US)	725-2738-US
	Keyboard, Universal (UK)	725-2738-UK
	Keyboard, Universal (SL)	725-2738-SL
	Keyboard, Universal (AZ)	725-2738-AZ
	Keyboard, Universal Exp. (GE)	725-2739-GE
5	Cable Assembly	220-0305
6	Base, Keyboard	449-0607
7	Foot, Self Adhesive	655-0286
	Foot, Self Adhesive	655-0291
8	Screw, 8-32 X 1/2 Pan Hd Phil	650-4160
9	Speaker, Round 2-in., 8 Ohm	320-0306
	(*) Denotes an RSL item.	

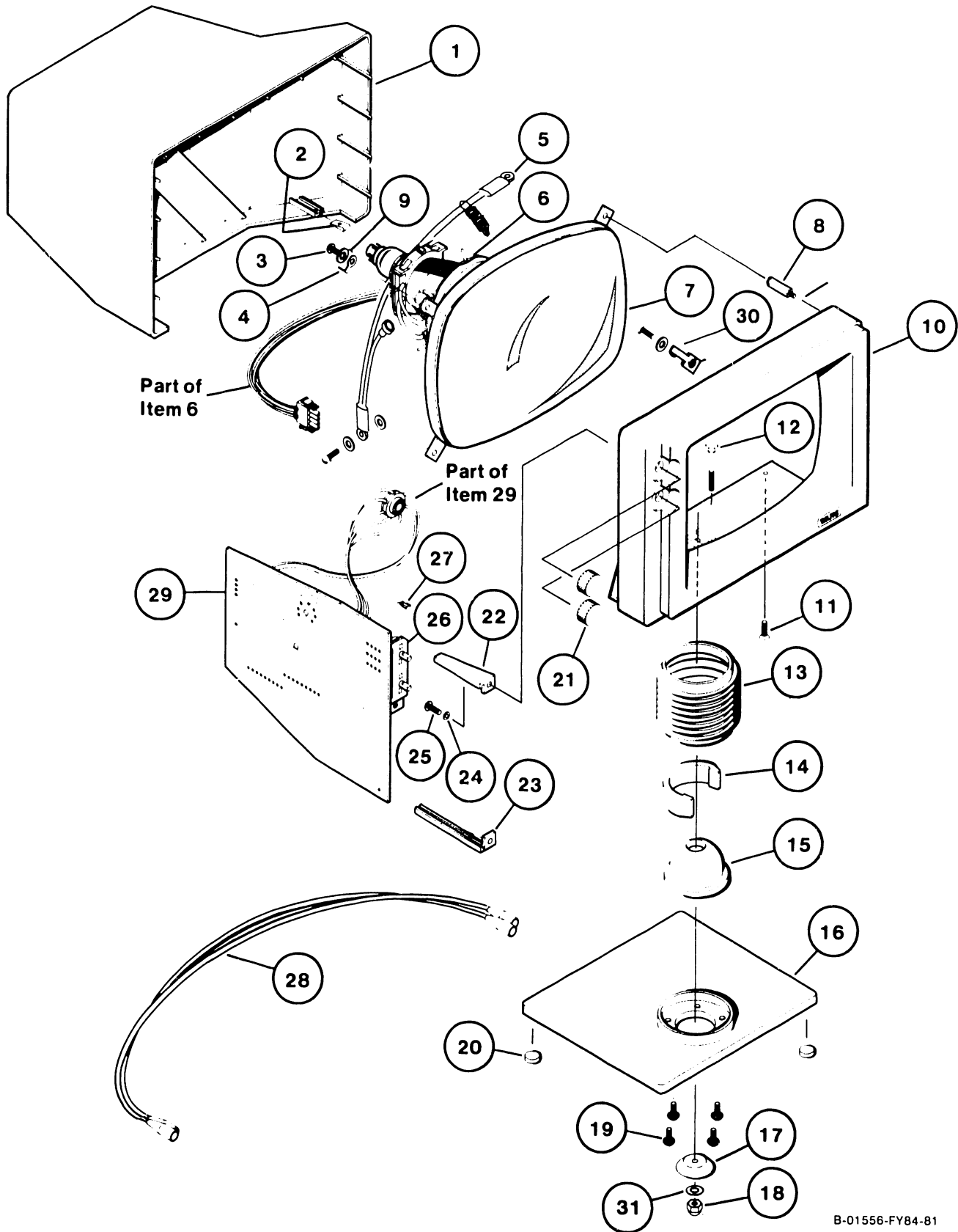


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Figure 7-2. Keyboard Assembly

Table 7-3. Monitor Assembly
(Refer to Figure 7-3)

<u>LOC.</u>	<u>DESCRIPTION</u>	<u>P/N</u>
1	Cover, Monitor	449-0630
2	Fastener, #8-32 U-Type	651-0268
3	Screw, 10-32 X 1/2 Truss Hd Phil	650-6160
4	Terminal Lug, Spade	654-0125
5	Grounding Cable Assembly (requires item 30 for installation)	220-1964
6	Yoke Assy (Less Magnets)	270-3289
	Magnet, 11 Gauss	320-0126
	Magnet, 20 Gauss	320-0127
	Magnet, 15 Gauss	320-0128
7	Tube, C/R 12-in. (Less Yoke Assy)	340-0111
8	Standoff, 3/8 Hex X 1-5/8-in. Long	462-0610
9	Washer	653-6000
10	Bezel, Monitor	449-0631
11	Screw, 8-32 X 3/8 Phil Hd Flt (White)	650-4121
12	Screw, 1/4-28 X 1-3/4 Hex	650-9077
13	Bellow, Sleeve	449-0635
14	Collar, Ball Joint	449-0626
15	Ball Joint	478-0805
16	Base, Monitor	449-0627
17	Cap Spring	449-0625
18	Stop Nut, 1/4-28	652-0064
19	Screw, 6-32 X 1/2 Pan Hd Phil	650-3160
20	Foot, 5/8 X 1/8 Self-Adhesive	655-0286
21	Knob	449-0596
22	Holder, PCB Upper	449-0629
23	Holder, PCB Lower	449-0628
24	Washer	653-4001
25	Screw, 8 X 1/2 Self Tap Pan Hd Phil	651-0052
26	Bracket (included w/item 29)	451-4985
27	Wire and Lug Assy (included w/item 29)	220-1263
28	Cable Assy, I/O	421-0001*
29	PCA, Monitor (early units)	210-8244*
	PCA, Monitor (later units)	210-8344*
30	Clip, Spring	452-2737
31	Washer	653-6006
32	Spring (included w/item 5)	465-1637
(*)	Denotes an RSL item.	



B-01556-FY84-81

Figure 7-3. Monitor Assembly

CHAPTER

8

**TROUBLE-
SHOOTING**

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CHAPTER 8 TROUBLESHOOTING

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CHAPTER 8 TROUBLESHOOTING

This chapter contains information directed toward diagnosis and repair of the 4210 and 4220 Workstations. Included are illustrations showing some of the key rear panel connectors of the Electronics Base, each of their pins and the signals associated with those pins. Also, a separate troubleshooting flowchart is given for each of the two models.

The flowcharts organize information included in other chapters of this manual in a logical sequence toward the end of isolating a field replaceable unit related to an observed symptom.

During the course of investigation, alignments or other procedures may be referred to as a means of verification or isolation. Following the flowchart through on these points will prevent replacement of field replaceable units where they only require alignment or some other adjustment.

Remember, no procedure can list every problem that could occur in even a very simple device. Use the troubleshooting flowchart as a guide in the systematic investigation, diagnosis and repair of failures in the 4210/4220 Workstation.

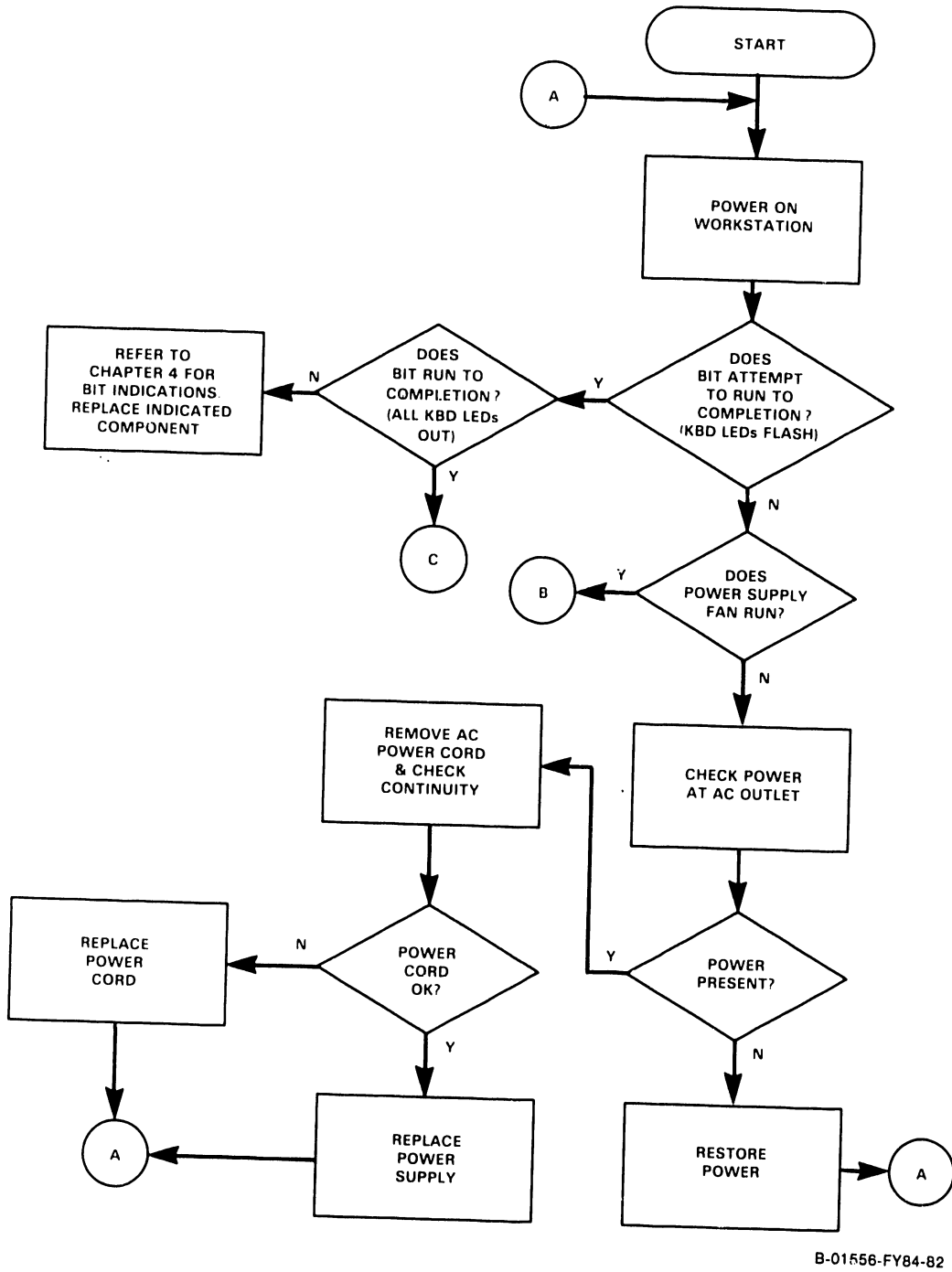
8.1 GENERAL TROUBLESHOOTING CHECKS

Before proceeding with the more in-depth troubleshooting outlined in other sections of this chapter, make a careful visual inspection of the workstation and check the items listed below.

- o Is the ac power cord securely plugged into its power outlet?
- o Are the VIDEO, PWR, and KYBD cables between the Monitor, Keyboard and Electronics Base securely connected to their respective connectors?
- o For the 4210, is the DATA LINK dual-coaxial cable from the workstation to the host CPU securely connected at both units?
- o For the 4220, is the RS-232C cable connector securely connected at the workstation and the modem?

8.2 TROUBLESHOOTING FLOWCHARTS

Figure 8-1 is the troubleshooting flowchart for the 4210 Workstation. Figure 8-2 is the troubleshooting flowchart for the 4220 Workstation.



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Figure 8-1. 4210 Workstation Troubleshooting Flowchart (Sheet 1 of 4)

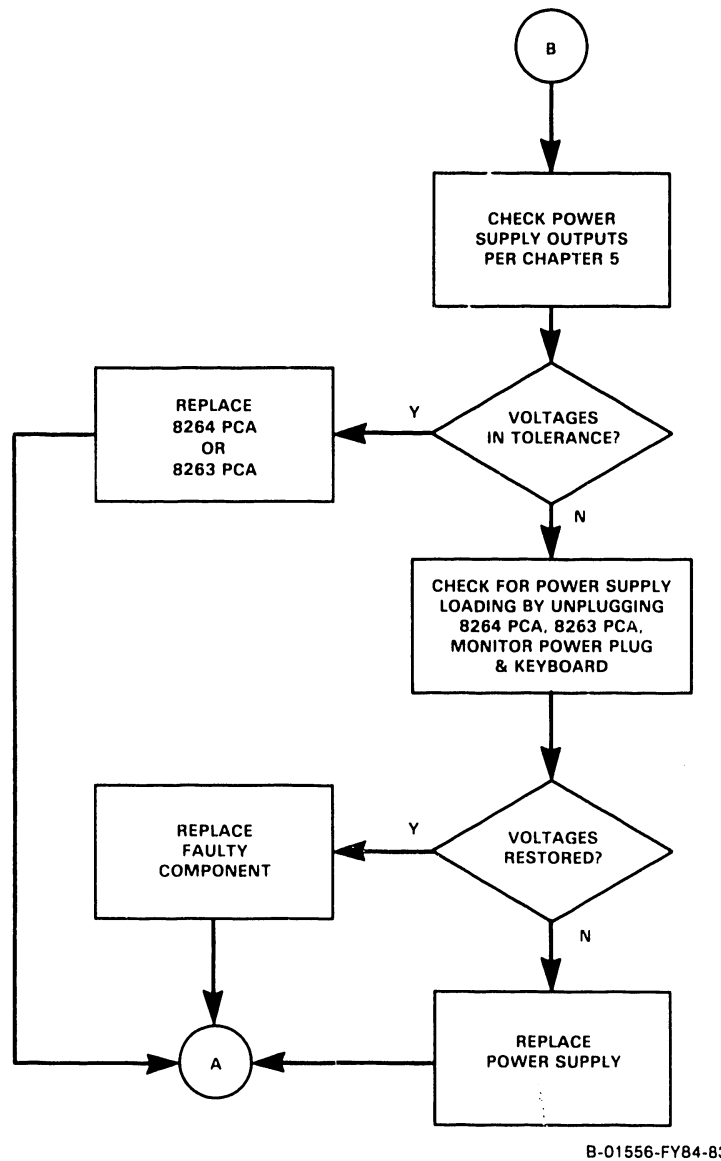
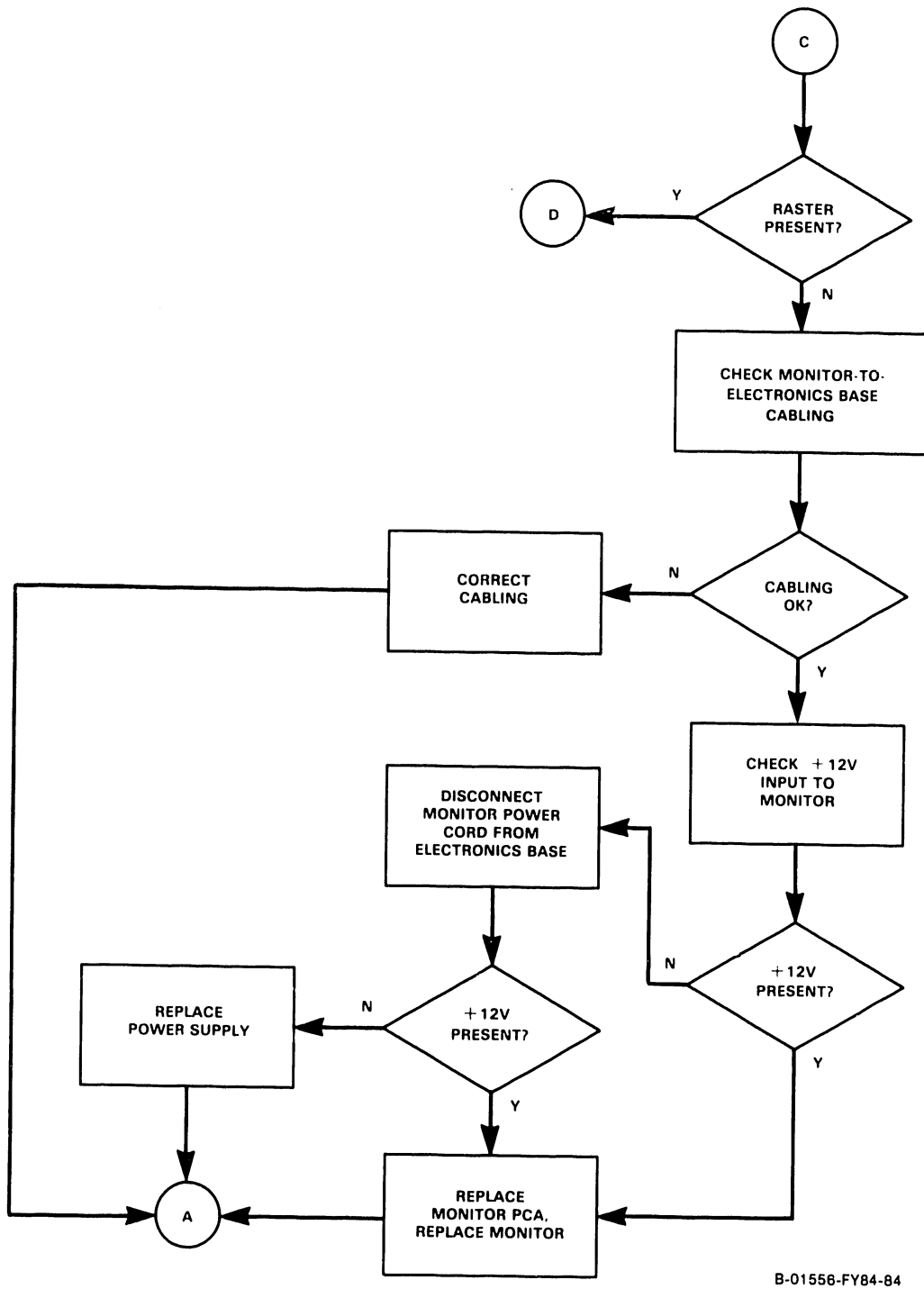
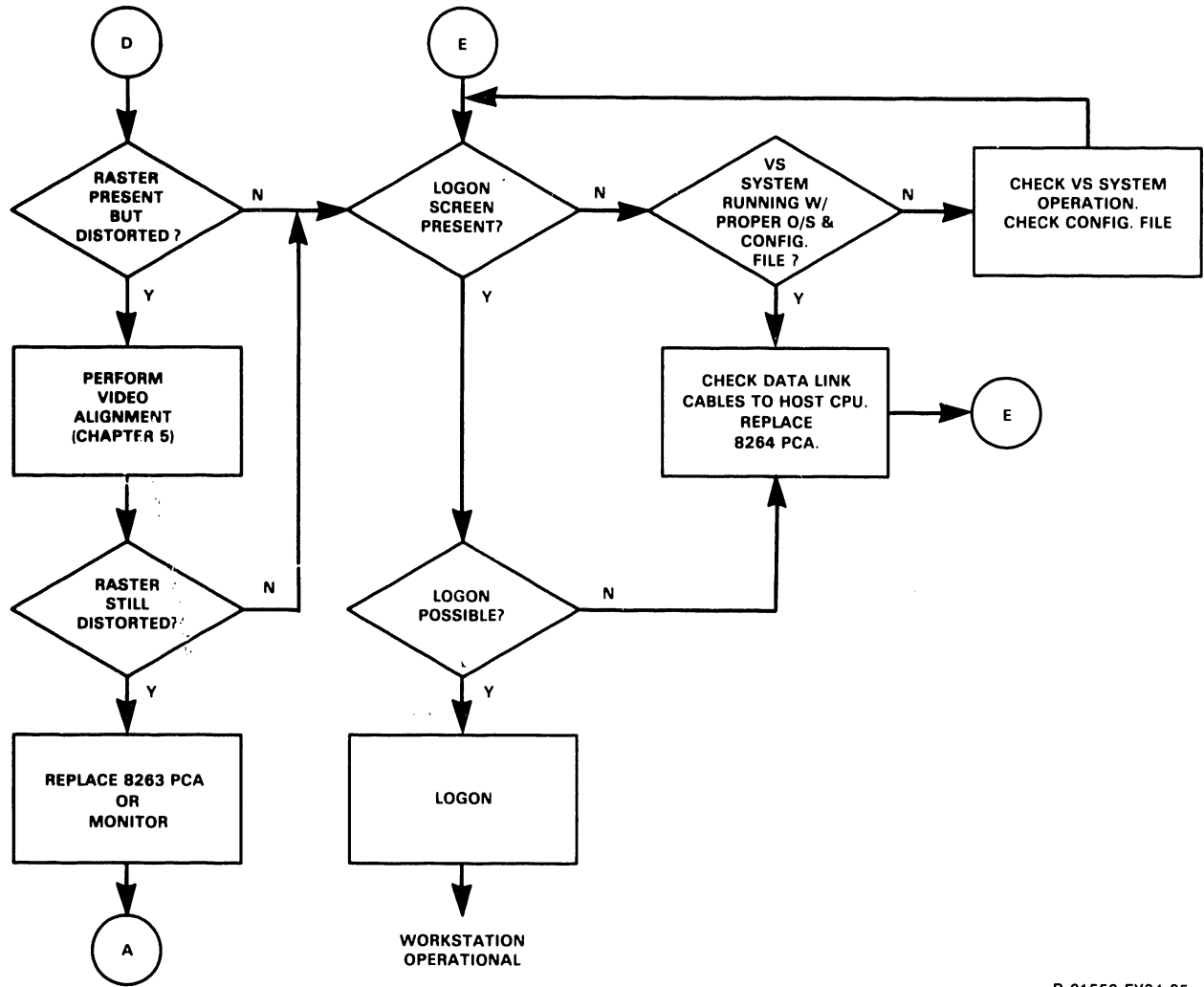


Figure 8-1. 4210 Workstation Troubleshooting
Flowchart (Sheet 2 of 4)



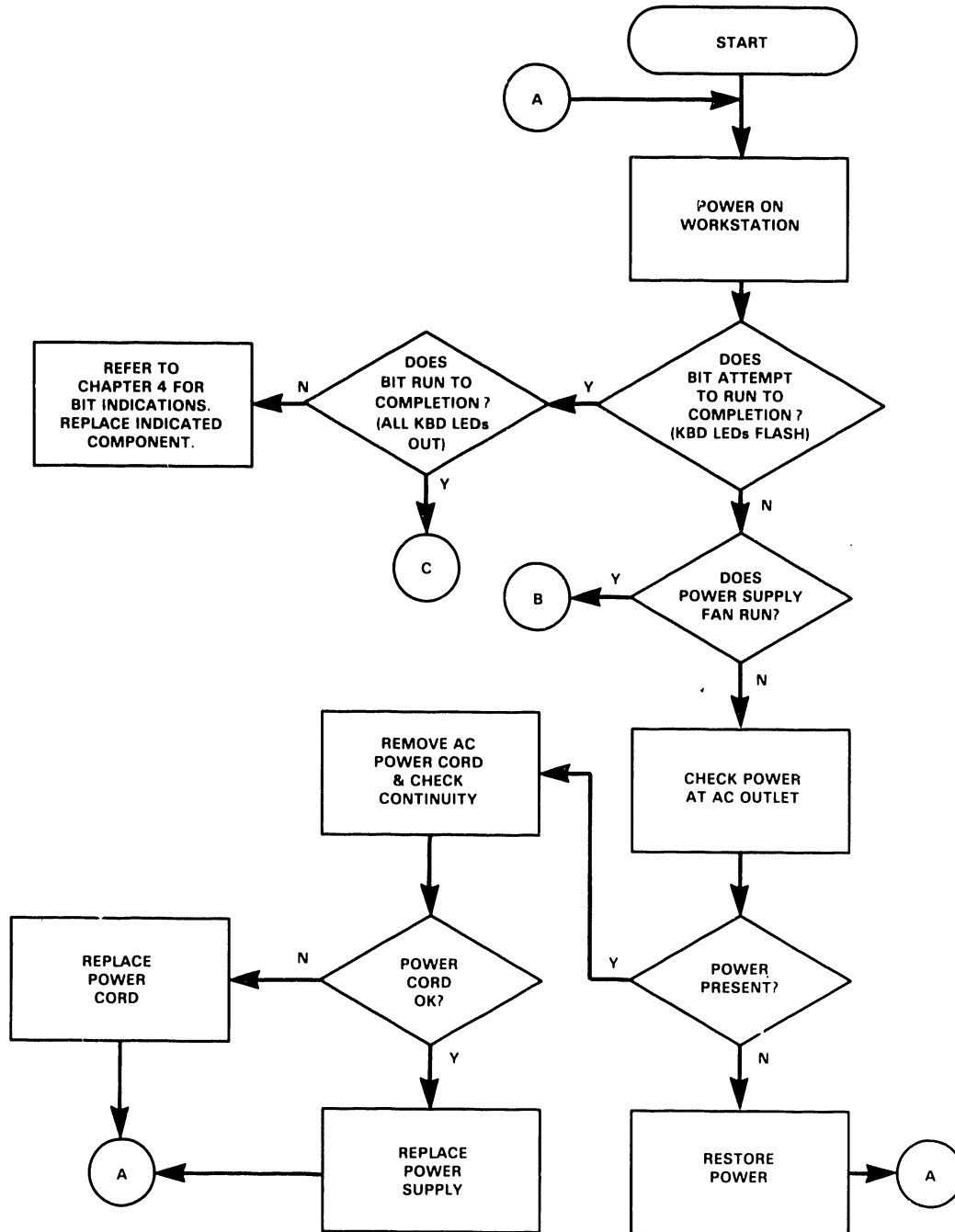
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Figure 8-1. 4210 Workstation Troubleshooting Flowchart (Sheet 3 of 4)



B-01556-FY84-85

Figure 8-1. 4210 Workstation Troubleshooting Flowchart (Sheet 4 of 4)



B-01556-FY84-86

Figure 8-2. 4220 Workstation Troubleshooting Flowchart (Sheet 1 of 4)

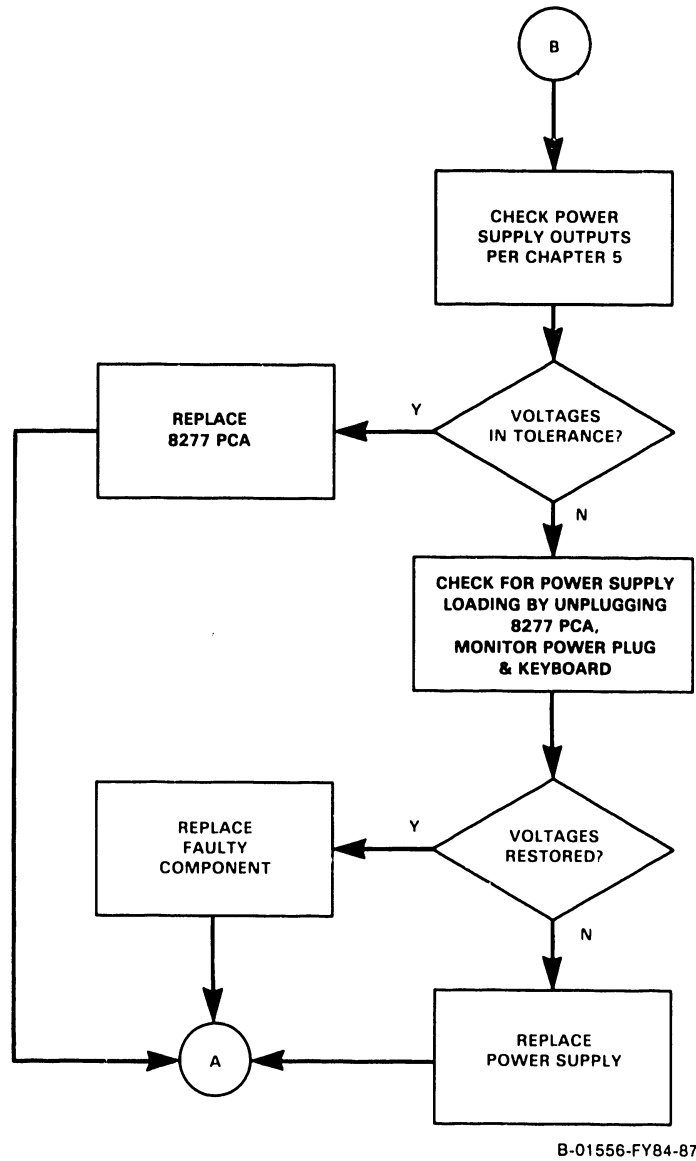
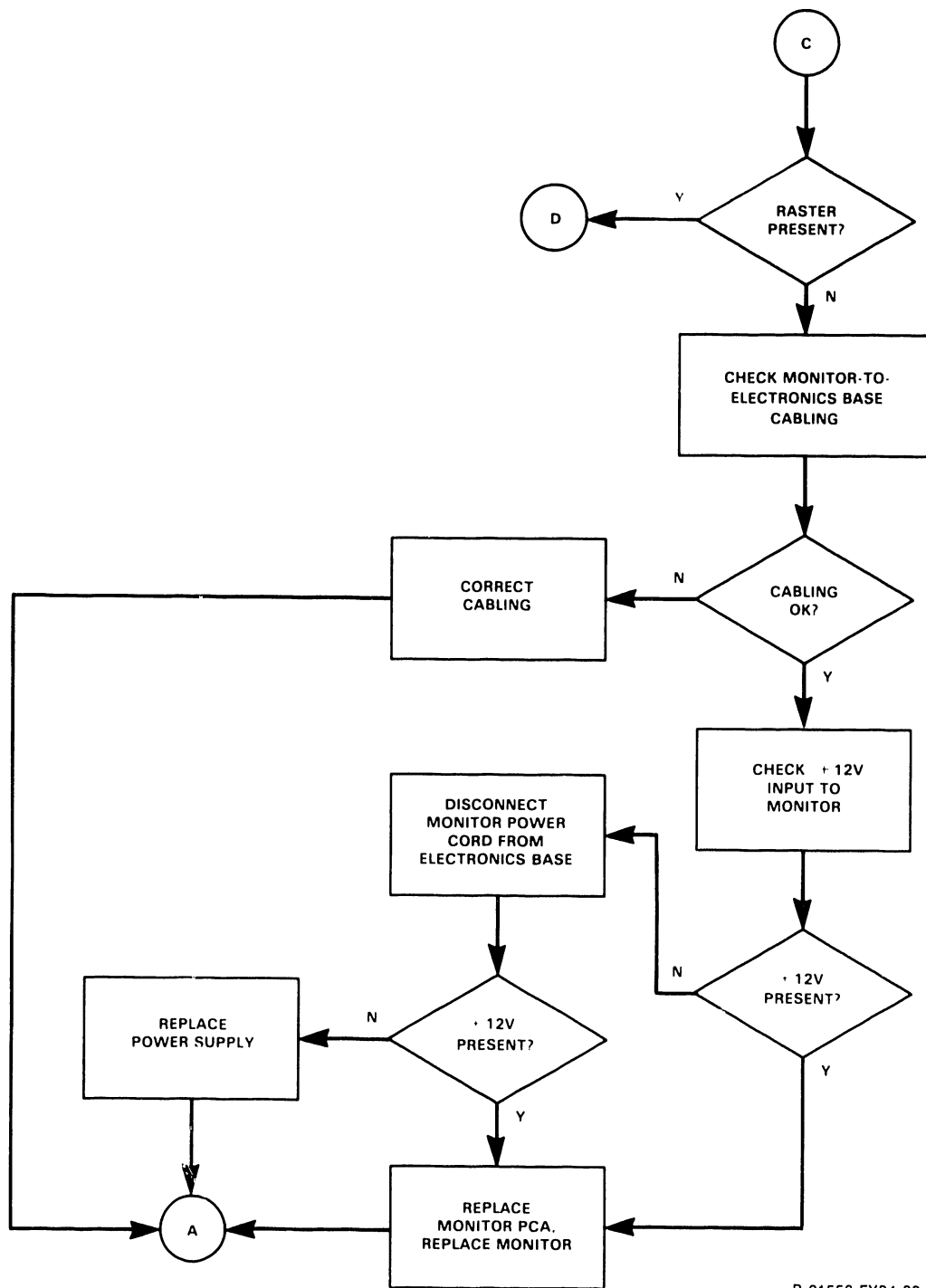
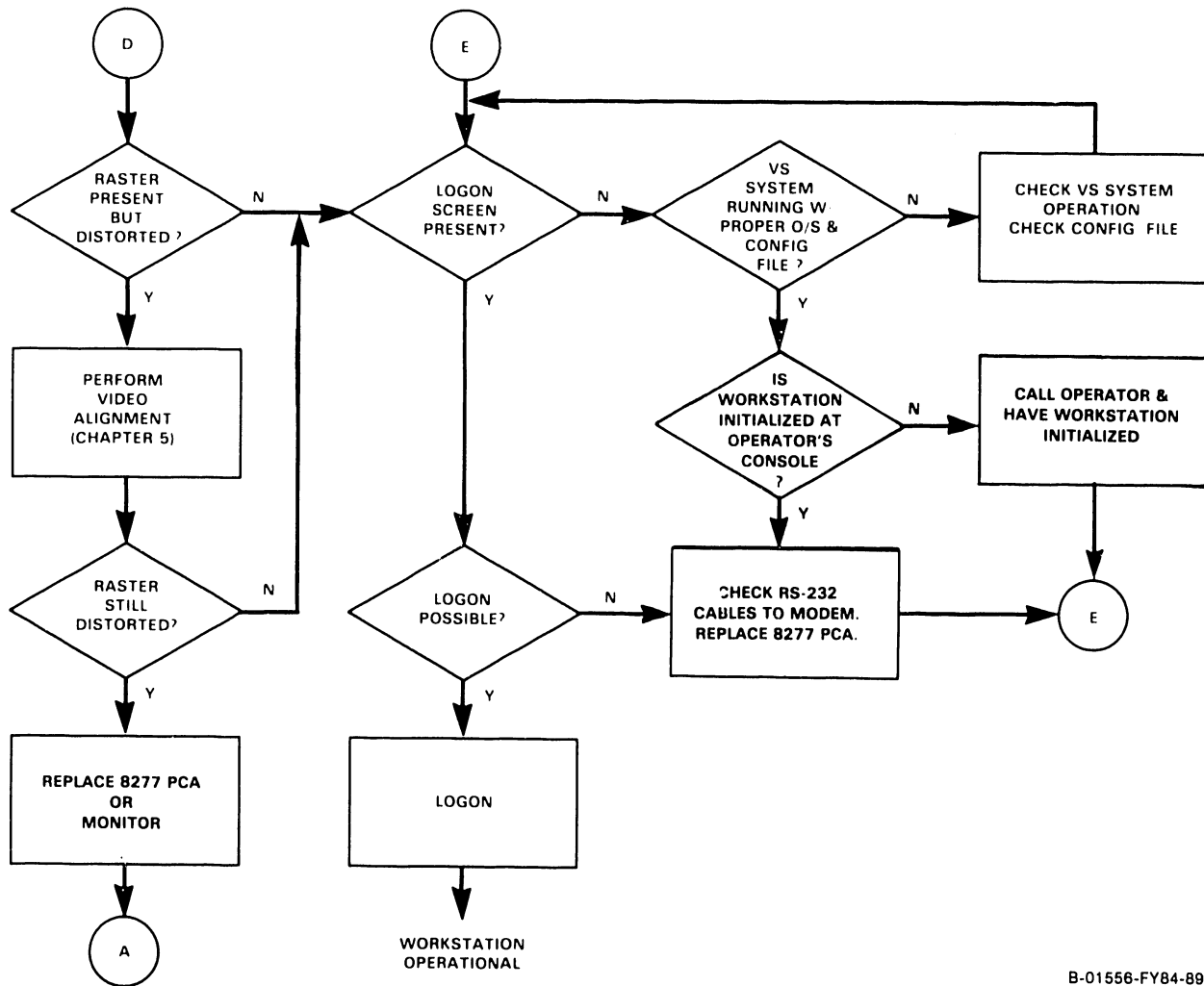


Figure 8-2. 4220 Workstation Troubleshooting
Flowchart (Sheet 2 of 4)



B-01556-FY84-88

Figure 8-2. 4220 Workstation Troubleshooting
Flowchart (Sheet 3 of 4)



B-01556-FY84-89

Figure 8-2. 4220 Workstation Troubleshooting Flowchart (Sheet 4 of 4)

8.3 MONITOR QUICK CHECKS

The VS diagnostic test operating system (DTOS) contains two video display patterns which are useful for quick evaluation of the Monitor's performance. These are the inverse video display and the circular alignment pattern.

Inverse Video Display Pattern

Select the inverse video display pattern of the DTOS Monitor alignment routine. All pixels on the CRT will be active (lit) except for those which display the words 'INVERSE VIDEO.' This display is useful in determining the condition of the high voltage circuits of the Monitor. Typical symptoms which may be observed with this full display are given below.

- o Blooming: Indicates possible failure of high voltage circuitry to maintain adequate current for full illumination of CRT phosphors.

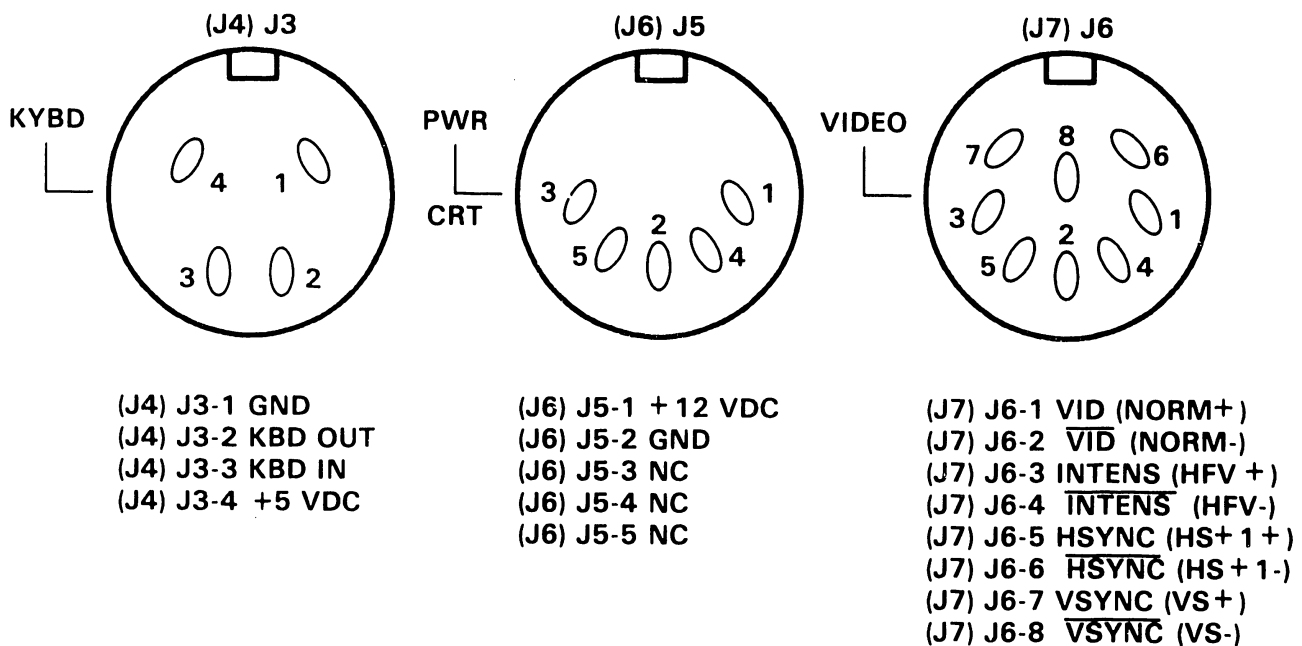
- o Noise or Breakup: Indicates possible high voltage arcing or other source of interference.

Circular Alignment Pattern

Select the circular alignment pattern of the DTOS Monitor alignment routine. Five circles of equal size will be displayed on the CRT. The circles are a good visual check of the linearity of the CRT display. If the circles are out of round or egg-shaped, the Monitor is in need of alignment. Refer to the alignment procedure in Chapter 5 of this manual.

8.4 PIN ASSIGNMENTS OF REAR PANEL CONNECTORS

Figures 8-3 and 8-4 illustrate some of the key rear panel connectors of the Electronics Base, each of their pins and the signals associated with those pins. The PWR, VIDEO and KYBD connectors are common to both the 4210 and 4220 Workstations as is the RS-232C connector.

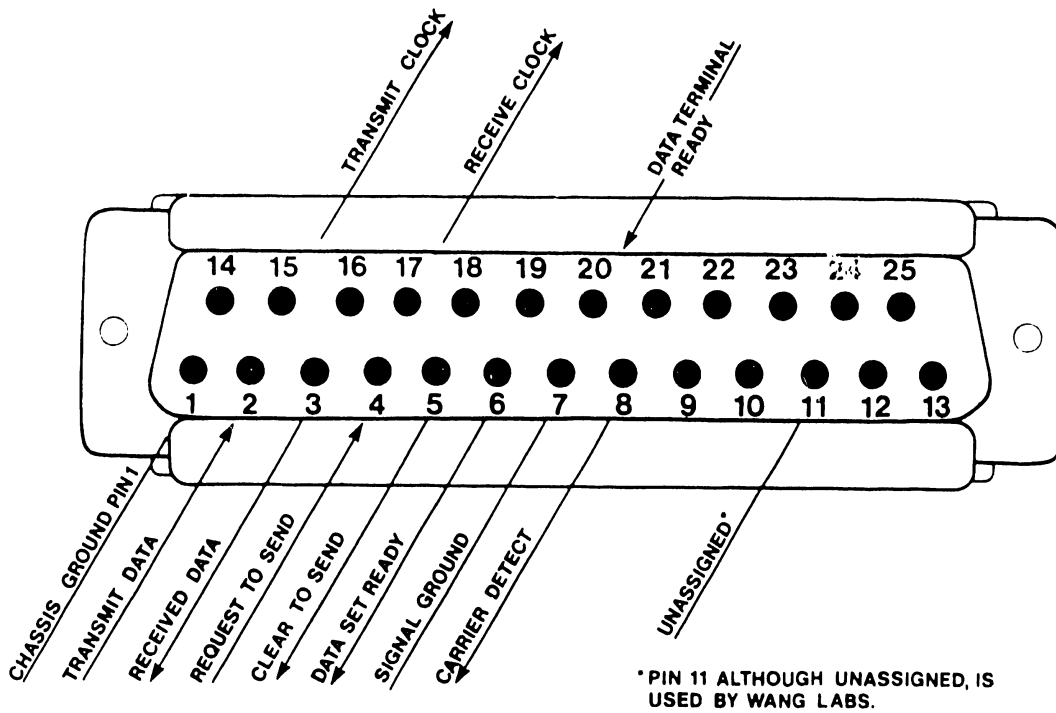


CONNECTORS VIEWED FROM REAR OF ELECTRONICS BASE.

4220 REFERENCE DESIGNATIONS AND ALTERNATIVE SIGNAL

NAMES ARE GIVEN IN PARENTHESES (4220)4210.

Figure 8-3. PWR, VIDEO and KYBD Connector
Pin Assignments



VIEWED FROM CABLE SIDE

PIN	EIA	CCITT	SIGNAL DESCRIPTION	SOURCE
1	AA	101	Protective Ground	
2	BA	103	Transmitted Data	DTE
3	BB	104	Received Data	DCE
4	CA	105	Request to Send	DTE
5	CB	106	Clear to Send	DCE
6	CC	107	Data Set Ready	DCE
7	AB	102	Signal Ground	
8	CF	109	Carrier Detect	DCE
9				
10				
11	SCA	120	Not Assigned	
12	SCF	122	Second. Carrier Detect	DCE
13	SCB	121	Second. Clear to Send	DCE
14	SBA	118	Second. Transmitted Data	DTE
15	DB	115	Transmit Clock	DCE
16	SBB	119	Secondary Received Data	DCE
17	DD	115	Receive Clock	DCE
18			Not Assigned	
19	SCA	120	Secondary Request to Send	DTE
20	CD	108.2	Data Terminal Ready	DTE
21	CG	110	Signal Quality Detector	DCE
22	CE	125	Ring Indicator	DCE
23	CH	111	Data Signal Rate Selector	DTE
23	CI	112	Data Signal Rate Selector	DCE
24	DA	113	Transmit Clock	DTE
25			Unassigned	

Figure 8-4. RS-232C Connector Pin Assignments

8.5 SWITCHING POWER SUPPLY OVERCURRENT TRIP

The switching power supply senses overcurrent conditions in the workstation and responds by shutting itself down momentarily and then recycling itself back on. If the overcurrent condition still exists, the cycle is repeated. The result is a distinctive repetitive clicking sound which emanates from the power supply in the event of a hard short in the workstation.

In the event of a condition such as this, check for shorts across the +5 and +12 Vdc lines in the workstation. Also, be sure that the power supply plug has been connected properly to the workstation PCAs. The yellow wire on the molex connector from the power supply must be connected to the PCA connector pin closest to the front of the workstation.

8.6 ITS-1 EIA INTERFACE TEST SET

8.6.1 DESCRIPTION

The model ITS-1 EIA Interface Test Set is a self-contained, pocket size test set that can be inserted between the Data Communication Equipment (DCE) or modem and Data Terminal Equipment (DTE). It permits the user to monitor the EIA RS-232 signals and isolate and identify sources of trouble.

8.6 ITS-1 EIA INTERFACE TEST SET, continued

8.6.1 DESCRIPTION, continued

The EIA Interface Test Set contains nine indicators which continuously monitor the level of the following interface signals:

- transmitted data
- data terminal ready
- data set ready
- request to send
- ring indicator
- clear to send
- received data
- signal quality detect
- carrier detect

Two indicators monitor the transmit and receive clock signals. Unlike the nine level indicators, the two clock signal indicators will not respond when only a dc level is present. The clock signal indicators will only turn on when there is an active clock signal present. Two additional uncommitted indicators are present for monitoring either positive or negative levels on any of the interface lines.

The Interface Test Set contains 24 switches which allow any of the interface signals except line one (Frame Ground) to be interrupted. These switches are physically located in the center of the front panel and functionally divide the test set into two halves. The upper half contains a cable and connector for connecting the test set to the DCE (data communications equipment) or modem. The indicators which monitor signals originating from the modem are also located on the upper half of the front panel. Likewise, the lower half of the test set contains a connector to which the DTE (workstation or CPU) can be connected. The indicators which monitor signals

8.6 ITS-1 EIA INTERFACE TEST SET, continued

8.6.1 DESCRIPTION, continued

originating from the DTE are also located on the lower half of the test set. Furthermore, the positive and negative test indicators are also located on the lower half of the test set. All indicators are labeled with both the standard EIA designation and the commonly used abbreviations.

Twenty-five pins are located both above and below the switches. These pins permit monitoring of any of the interface lines with either or both the positive and negative test indicators with jumpers supplied or probing with an external meter or oscilloscope. Both sets of pins are arranged in the same configuration and order as the pins in a standard EIA RS-232 female connector.

The Interface Test Set is housed in a sturdy plastic case with aluminum extrusions and hinge. A positive latch is provided on the cover to keep the test set closed securely when not in use. The front panel is photographically etched and overcoated to prevent the lettering from being scratched or marred during use. The unit is self-contained and is powered by two penlite (AA) batteries which provide over 100 hours of continuous operation. No power is consumed by the test set when it is not in use.

8.6 ITS-1 EIA INTERFACE TEST SET, continued

8.6.1 DESCRIPTION, continued

Table 8-1. EIA Interface Test Set Specifications
Level Indicators:

- transmitted data
- data terminal ready
- data set ready
- request to send
- ring indicator
- clear to send
- received data
- signal quality detect
- carrier detect

Activity Indicators:	Trans. Clk, Rec. Clk.
Indicator Threshold:	+ 3 volts
Indicator Input Impedance:	30,000 ohms
Power:	2 1.5 volt AA Batteries
Dimensions:	4.5"L x 3.6"W x 1.6"H
Weight:	12 oz.

8.6.2 MODEM CONTROL SIGNALS CHECKOUT

If the modem is suspected of causing trouble, the following control signals can be checked using an oscilloscope or an EIA Interface Test Set which provides test points and LEDs that indicate signal activity. The modem must be in the data mode when checking the control signals.

To check out the modem control signals, insert the EIA ITS-1 between the DCE and the DTE, using the cables and connectors provided. The following sections are divided according to the signals required for communication on the RS-232C link. They provide additional information required to determine proper signal activity on each pin of the RS-232C connector involved in the data communication. All pin numbers are given in reference to the standard RS-232C connector.

8.6.2 MODEM CONTROL SIGNALS CHECKOUT, continued

8.6.2.1 Ground

Pins 1 and 7 are chassis and signal ground respectively. Check for any noise on the ground circuits.

8.6.2.2 Pin 2, Transmitted Data (To DCE)

Signals on this circuit are generated by the DTE. Check to see if the workstation is transmitting data when in the transmit mode. The DTE will not transmit data unless the following signals are active:

- o Clear To Send: Active = +3V to +25V @ pin 5
- o Data Terminal Ready: Active = +3V to +25V @ pin 20
- o Data Set Ready: Active = +3V to +25V @ pin 6

8.6.2.3 Pin 3, Received Data (From DCE)

Signals on this circuit are generated by receiving DCE in response to data signals received from a remote DCE. This circuit is always held in the MARK state (-3V to -25V) when the Received Line Signal Detector (pin 8) is inactive (-3V to -25V).

8.6.2 MODEM CONTROL SIGNALS CHECKOUT, continued

8.6.2.4 Pin 4, Request To Send (To DCE)

The DTE presents an active signal (+3V to +25V) to this circuit when it intends to transmit data. After activating this signal, the DTE must wait for Clear To Send (pin 5) to activate before starting data transmission.

8.6.2.5 Pin 5, Clear To Send (From DCE)

This signal becomes active to indicate that the DCE is ready to transmit data. This circuit is activated (+3V to +25V) in response to an active Request To Send at pin 4, delayed approximately 50 to 200 msec depending on the type of modem and customer options selected.

8.6.2.6 Pin 6, Data Set Ready (From DCE)

The active condition (+3V to +25V) of this circuit indicates that the DCE is in data mode and is capable of receiving and transmitting data. The Data Terminal Ready signal at pin 20 must be active (+3V to +25V) during data mode. An inactive condition (-3V to -25V) indicates that the DCE is in talk, test, or on-hook mode.

8.6.2.7 Pin 8, Carrier Detect (From DCE)

The active condition (+3V to +25V) of this circuit indicates that the data carrier signal is above the receiver threshold for at least 47 ± 3 msec. This circuit is active during the receive

8.6.2 MODEM CONTROL SIGNALS CHECKOUT, continued

8.6.2.7 Pin 8, Carrier Detect (From DCE)

mode and will deactivate (-3V to -25V) and disable the receiver when the DTE is in the transmit mode or when Request To Send is activated.

8.6.2.8 Pin 15, Transmit Clock (From DCE)

The square wave signals on this circuit at 2000 Hz (for 2000 baud modem) or 2400 Hz (for 2400 baud modem) or 4800 Hz (for 4800 baud modem) are used to provide the DTE with signal element timing information for the transmitted data circuit. A timing signal will be present on this circuit in most cases when power is on in the DCE.

8.6.2.9 Pin 17, Receive Clock (From DCE)

The square wave signal on this circuit at 2000 Hz (2000 baud modem) or 2400 Hz (2400 baud modem) or 4800 Hz (4800 baud modem) rate is used to provide the DTE with receiver signal element timing information. The transition from active to inactive normally indicates the center of each signal element on the received data circuit. A timing signal will be present on this circuit when Carrier Detect (pin 8) is active for Bell data sets 201A and 201C.

8.6.2 MODEM CONTROL SIGNALS CHECKOUT, continued

8.6.2.10 Pin 20, Data Terminal Ready (To DCE)

The DTE must activate (+3V to +25V) this line for the DCE to go into the DATA mode. An inactive signal on this line will not allow the DCE to go into the data mode. An inactive state on this line which occurs during data transmission/reception will cause the DCE to drop the communication line.

8.7 RS-232C LOOPBACK CONNECTOR

An RS-232C loopback connector is available under part number 420-1040 and can be useful in troubleshooting the TC ports of either the 4210 or 4220 Workstation. The loopback connector is required to run the loopback test portion of the Built-In Test diagnostics in both workstations. Figure 8-5 shows the wiring of the connector. A loopback connector can be fashioned from an RS-232C connector by connecting the four jumpers shown in the figure to the specified terminals of the connector.

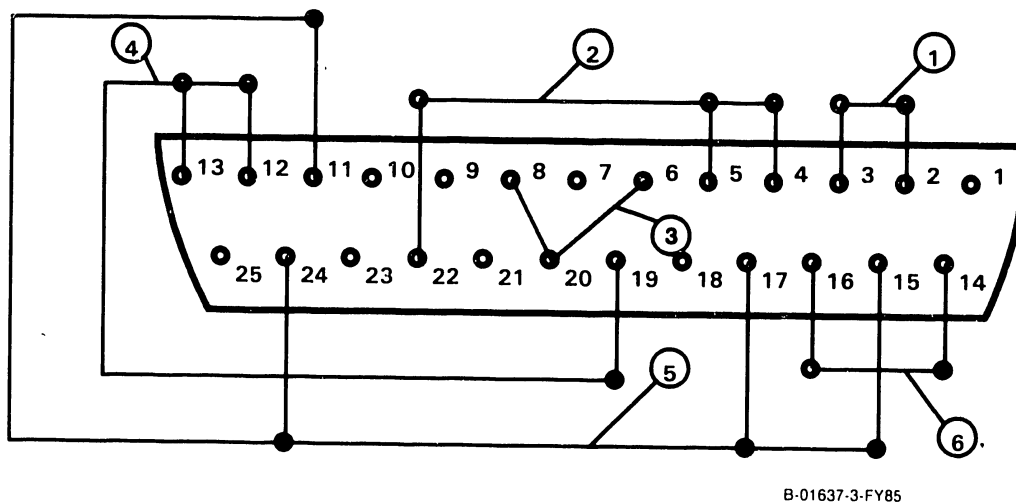


Figure 8-5. RS-232C Loopback Connector Wiring

CHAPTER

6

SCHE-

MATICS

TABLE OF CONTENTS

CHAPTER 6 SCHEMATICS

<u>Section</u>	<u>Title</u>	<u>Page</u>
6.1	<u>INTRODUCTION</u>	6-1

CHAPTER 6
SCHEMATICS

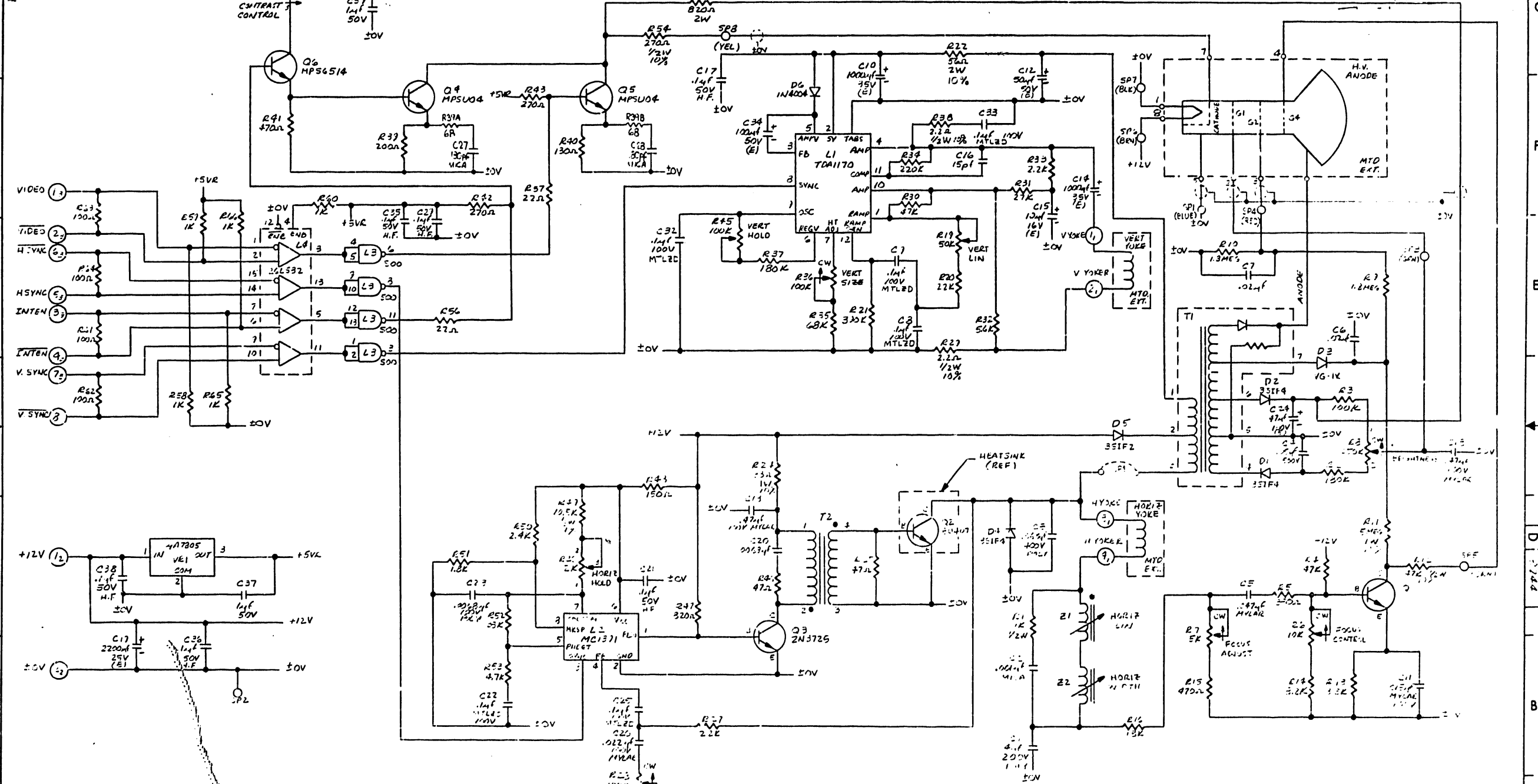
6.1 INTRODUCTION

Schematic diagrams for the component parts of the 4210 and 4220 Workstations are included in this chapter of the manual. The schematics reflect the latest revisions at the time of printing.

The following is a list of the schematics contained in this chapter, the titles, drawing numbers and revisions at time of printing.

<u>TITLE</u>	<u>DWG. NO.</u>	<u>REV.</u>	<u>COMMENTS</u>
Monitor PCA	210-8244	12	Common, Early Units
Bit Map PCA	210-8263	5	4210
CPU PCA	210-8264	6	4210
Remote Wkstn Electronics PCA	210-8277	7	4220
Monitor PCA	210-8344	6	Common, Later Units
Keyboard PCA	725-2786	2	Common

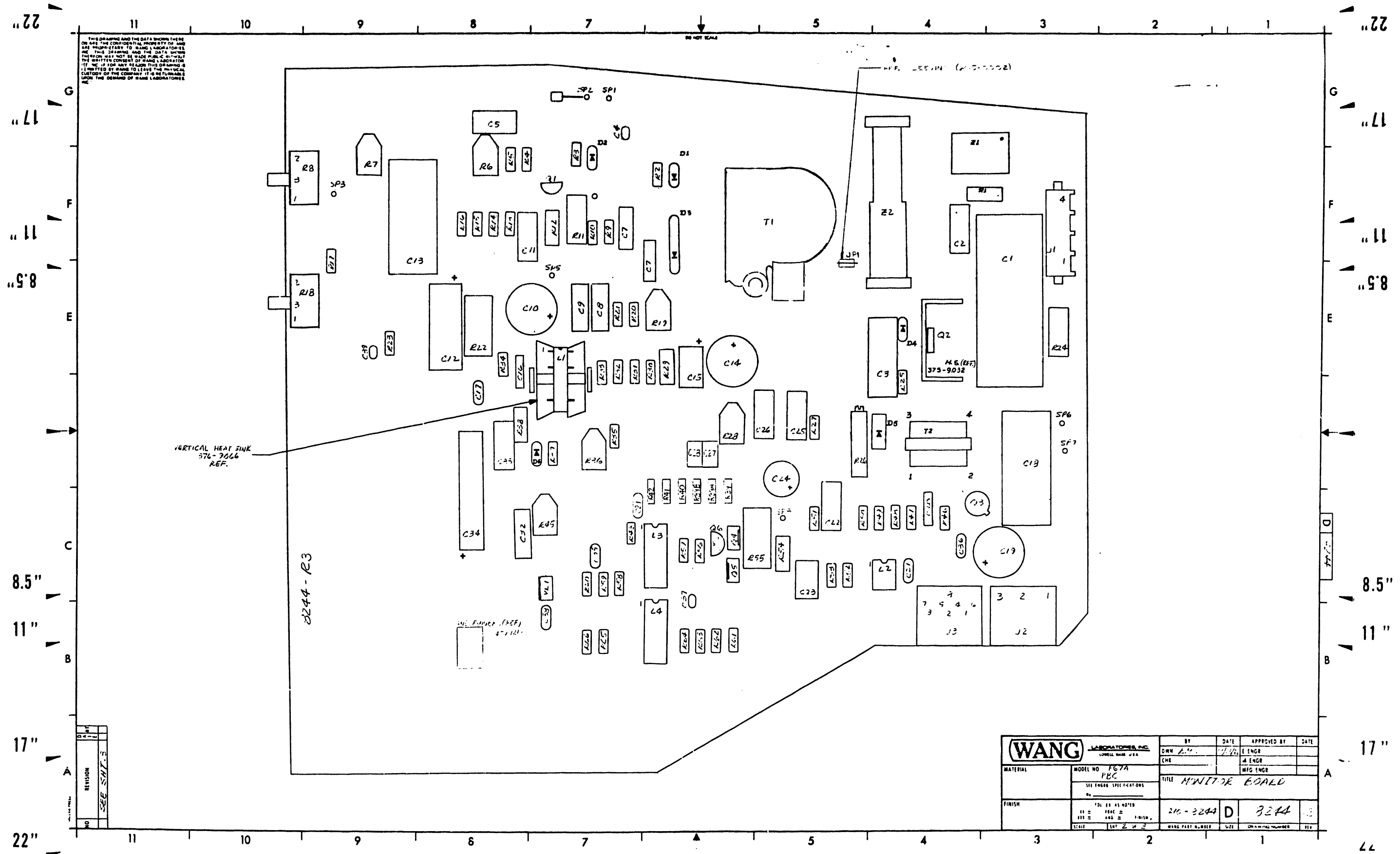
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REV	DATE	DESCRIPTION
1		ISSUED FOR FAB

WANG PART NO	DRAWING NO	DESCRIPTION	BY	DATE	APPROVED BY	DATE
			DWN		ENGR	
			CHK		M ENGR	
MATERIAL		MODEL NO	TITLE			
		SEE ENG SPECIFICATIONS	MONITOR BOARD			
FINISH		TO BE AS NOTED	210	5223	D	3/24
		SCALE	1/8" = 1"	WANG PART NUMBER	SIZE	DRAWING NUMBER

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VERTICAL HEAT SINK
576-7066
REF.

3244-R3

SEE FIGURE (REF)
4-1121

NO.	REVISION	DATE	BY
1	SEE SH-7-5		

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		BY CME	DATE 7/76	APPROVED BY M. ENGR	DATE
MATERIAL	MODEL NO. P67A PBC	TITLE MONITOR BOARD		MFG ENGR	
FINISH	101.00 AS NOTED 111.00 111.00	20-3244	D	3244	13
SCALE	1:1	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

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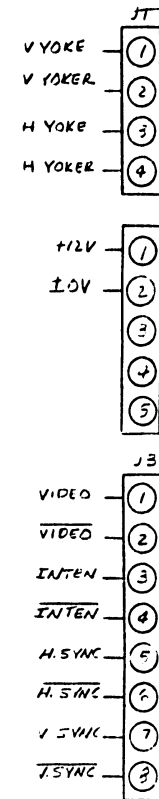
COMPONENT	TYPE	WL PART NO.
R1	1K 1/2W 5%	331-3011
R2,37	132K 1/4W 5%	330-5019
R3	100K 1/4W 5%	330-5011
R4,30	47K 1/4W 5%	330-4048
R5	330Ω 1/4W 5%	330-2034
R6	10K POT	336-1067
R7	5K POT	336-1068
R8	250K 2W POT	336-2048
R9,10	394K 1/4W 5%	330-6019
R11	154K 1W 10%	332-6015
R12	47K 1/2W 10%	331-4047
R13	3.3K 1/4W 5%	330-3037
R14	8.2K 1/4W 5%	330-3083
R15,41	470Ω 1/4W 5%	330-2048
R16	18K 1/4W 5%	330-4019
R17,54,57	22Ω 1/8W 5%	330-1023
R18	1K 2W POT	336-2047
R19	50K POT	336-1066
R20,27	22K 1/4W 5%	330-4023
R21	330K 1/4W 5%	330-5040
R22	56Ω 2W 1%	337-1056
R23	680Ω 1/4W 5%	330-2067
R24	33Ω 1W 10%	332-1033
R25,46	17Ω 1/4W 5%	330-1048
R26	2K TRIMP	336-2036
R29	120Ω POT	336-1062
R29,38	1.2K 1/4W 10%	331-0022
R31	27K 1/4W 5%	330-3023
R32	5.6K 1/4W 5%	330-3057
R33	2.2K 1/4W 5%	330-2028
R34	220K 1/4W 5%	330-5023
R35	29K 1/4W 5%	330-4067
R36,45	100K POT	336-1065
R37	200Ω 1/4W 5%	330-2020
R39A,39B	68Ω 1/4W 5%	330-1069
R40	130Ω 1/4W 5%	330-2014
R42,43	270Ω 1/4W 5%	330-3028
R47	320Ω 1/4W 5%	330-2028
R48	150Ω 1/4W 5%	330-2016
R49	10.5K 1/4W 1%	333-0112
R50	2.2K 1/4W 5%	330-2025
R51	1.3K 1/4W 5%	330-3017
R52	33K 1/4W 5%	330-4024

COMPONENT	TYPE	WL PART NO.
E53	47K 1/4W 5%	330-3048
R54	270Ω 1/4W 5%	331-2027
E55	270Ω 1/4W 5%	337-2083
R58-60,65,66	1K 1/4W 5%	330-3011
R61-64	100Ω 1/4W 5%	330-2011
C1	4μF 200V POLY	300-2413
C2	.001μF 500V MKT	300-5038
C3	.002μF 400V POLY	300-2076
C4	.05μF 500V	300-1946
C5	.047μF 50V	300-1962
C6,7	.02μF 140V	300-1916
C8,9,22,25,32,33	.1μF 100V MKT	300-2217
C10,14	1000μF 35V(1E)	300-3020
C11	.05μF 100V(1E)	300-2115
C12	50μF 50V(1E)	300-3010
C13,18	.47μF 100V(1E)	300-2247
C15	10μF 16V(1E)	300-3006
C16	15μF 500V	300-1015
C17,21,23,25,36,38	1μF 50V H.F.	300-1730
C19	220μF 25V(1E)	300-2021
C20	.0022μF 120V	300-1711
C25	.0047μF 100V	300-2067
C24	47μF 100V(1E)	300-2143
C26	.22μF 100V(1E)	300-2122
C27,28	150μF 50V MKT	300-1011
C29	100μF 50V(1E)	300-2052
C30	1μF 50V	300-1731
VR1	4A7805	374-0001
D1,7,4	3E1F4	330-2010
D3	VE1K	330-2017
D5	3E1F2	330-2012
D6	1N4004	330-1000

COMPONENT	TYPE	WL PART NO.
Q1	T80CMW-150V	375-1143
Q2	6U407	375-1057
Q3	2N3725	375-1027
Q4,5	MPSU04	375-1096
Q6	MPS6514	375-1062
T1	FLY BACK	410-0238
T2	KFMR DRIVER	410-1006
Z1	ADJUSTABLE	320-0107
Z2	WIDTH	320-0053
J1	4PIN CONN.	350-0215
J2	5PIN CONN.	350-0539
J3	8PIN CONN.	350-0542
JP1	15 GA BUS WIRE	600-2019
REF.	SLEEVING	605-0002
REF.	MT BRACKET	451-4785 AB
REF.	CRT GND STRIP	458-1217
REF.	HEAT SHRINK .1FT	605-0123
REF.	HEAT SHRINK .1FT	605-0143
REF.	20GA WIRE .1FT	600-1027
REF.	BRAID TUBULAR 1/32 ID .083 FT	420-0091
REF.	FLAT BRAID .1166 FT	420-0074

COMPONENT	TYPE	WL PART NO.
L1	TCA1170	376-2052
L2	M51711	376-2079
L3	1F500	376-2029
L4	1F500	376-2071

MNEMONIC	COORD.
H SYNC	1E11
H SYNC	1E11
H YOKE	1C4
H YOKE	1C4
INTEN	1E11
INTEN	1E11
VIDEO	1F11
VIDEO	1E11
V SYNC	1D11
V SYNC	1D11
V YOKE	1E4
V YOKE	1E4



NOTE: ALL RES ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

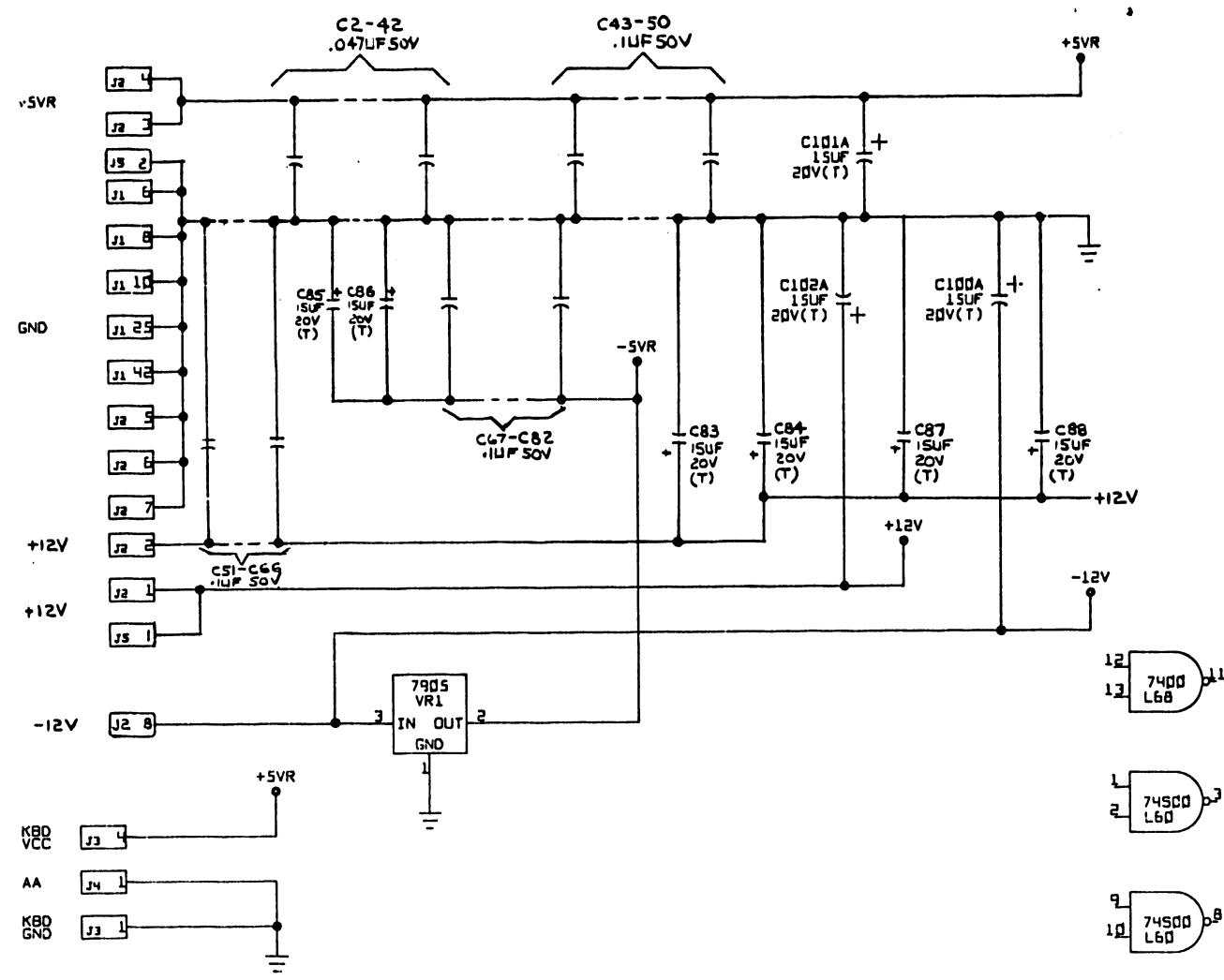
F-12V
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NO.	REVISION	DATE	BY	CHKD.	APPROVED
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3	REVISED PER	11/17/72	W.L.		
4	REVISED PER	11/17/72	W.L.		
5	REVISED PER	11/17/72	W.L.		
6	REVISED PER	11/17/72	W.L.		
7	REVISED PER	11/17/72	W.L.		
8	REVISED PER	11/17/72	W.L.		
9	REVISED PER	11/17/72	W.L.		
10	REVISED PER	11/17/72	W.L.		
11	REVISED PER	11/17/72	W.L.		
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13	REVISED PER	11/17/72	W.L.		
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16	REVISED PER	11/17/72	W.L.		
17	REVISED PER	11/17/72	W.L.		
18	REVISED PER	11/17/72	W.L.		
19	REVISED PER	11/17/72	W.L.		
20	REVISED PER	11/17/72	W.L.		

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330-3244	D	3244

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MNEMONICS	LOC.
AA	1C9
AB	9C11
BA	9A1
BB	9C11
BTDOR	8C11
BMT	9G6
BMR	9G6
BRO	8D11
BRR	8C11
BA0	8C11
BA1	8C11
BA4	8B11
BA5	8B11
B00-B05	8G11
CA	9B1
CB	9C11
CC	9B1
CF	9C11
CC	9C11
HS	8C1
HSYNC	8D1
HSYNC	8D1
INT	9A4
INTENS	8C1
INTENS	8D1
KBD	9G6
KBD GND	1C9
KBD OUT	9C1
KBD VCC	1C9
VID	8D1
VTD	8D1
VSI	8E1
VSYNC	8D1
VSYNC	8D1
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YC	2C1
WC	9E11
WB+WB	8B11

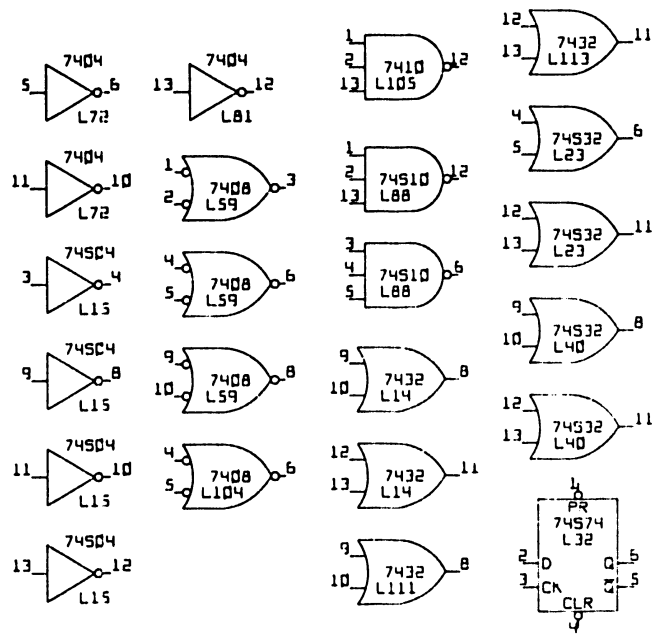


210 = 209 + 377 OR 378			
210	209	L9-12, 33-36, 61-64	L109
8263-A	8263	377-0345	377-0423

NOTES

1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.

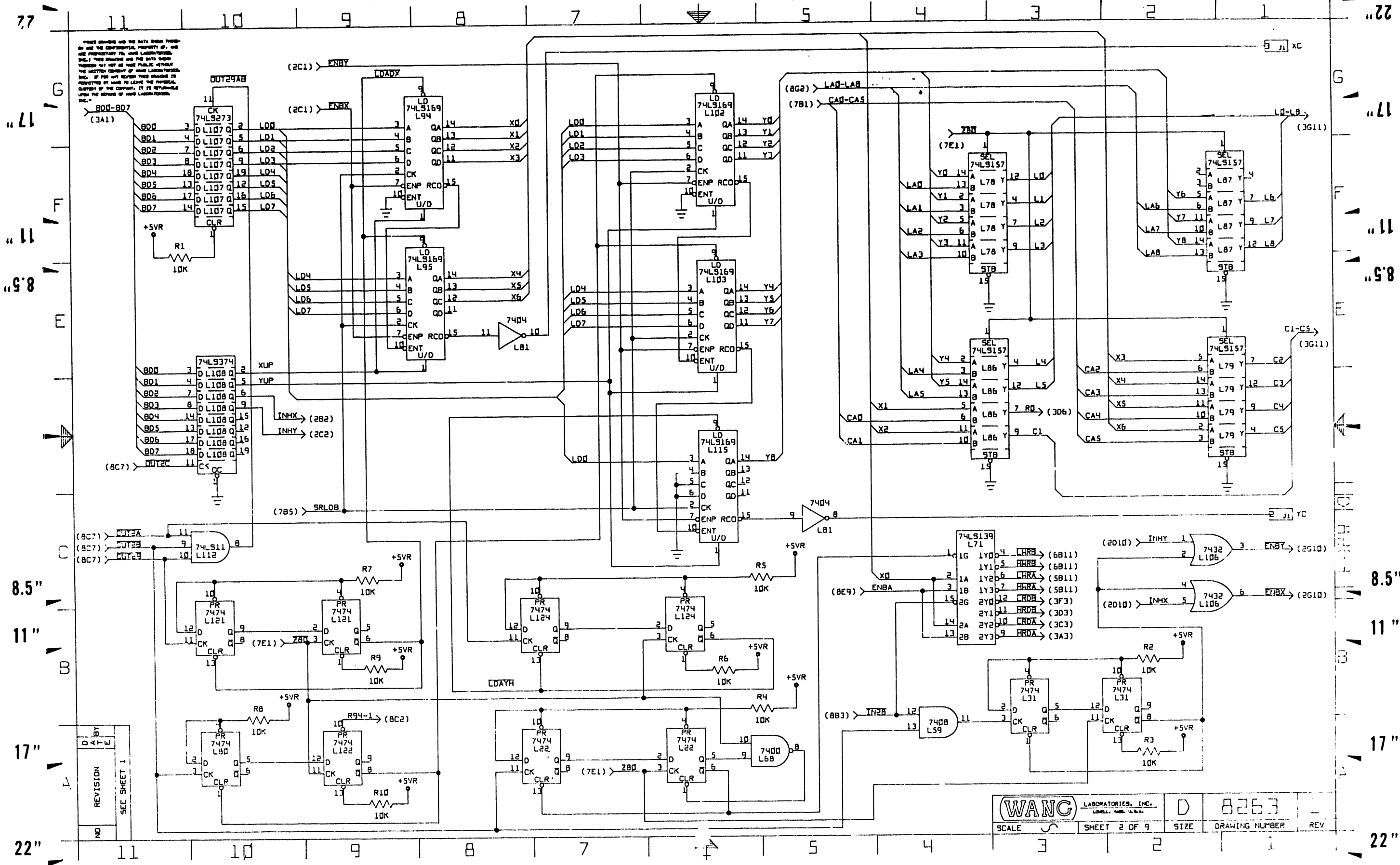
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NO	DATE	BY	PGD	PGD	SGC	KTH	KTH	KTH
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WANG LABORATORIES, INC. U.S.A.		SCHEMATIC DIAGRAM	
MODEL NUMBER H0140A		TITLE BIT MAP	
GRAPH TERM SEE CHART		OWN PGD	CHK SJ DIR
SCALE		8263	5
SHEET 1 OF 9		SIZE	DRAWING NUMBER REV

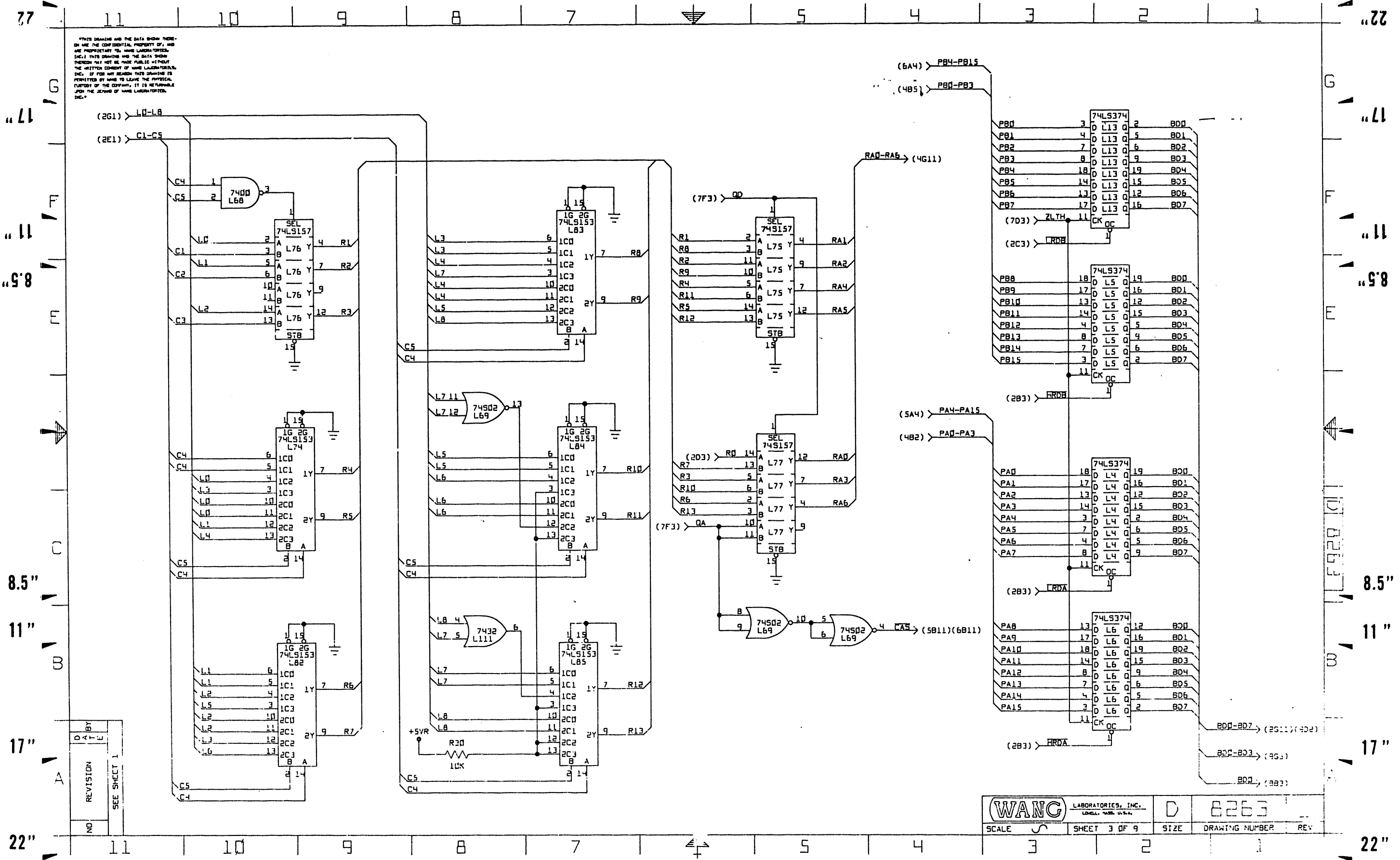


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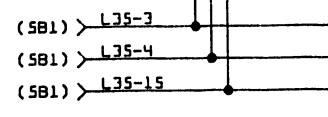
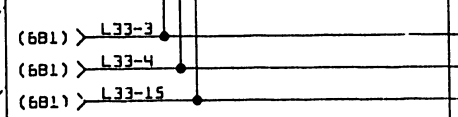
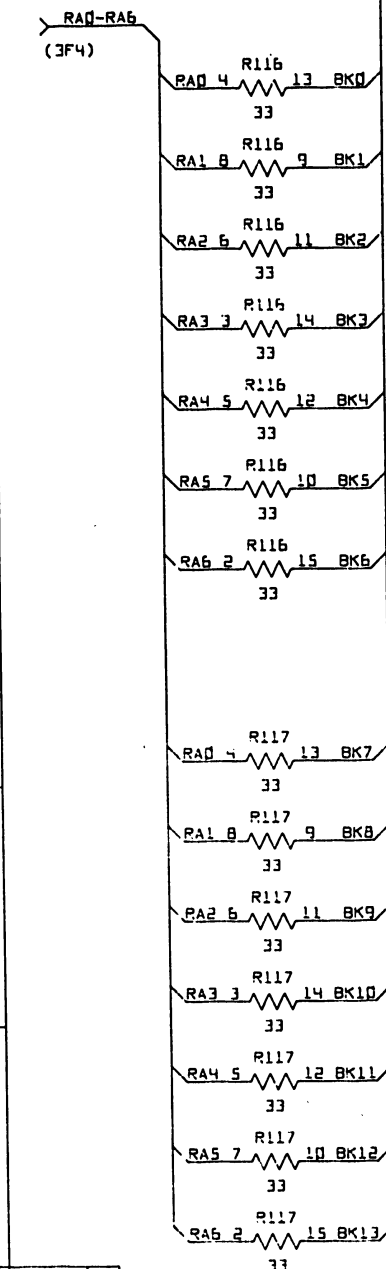
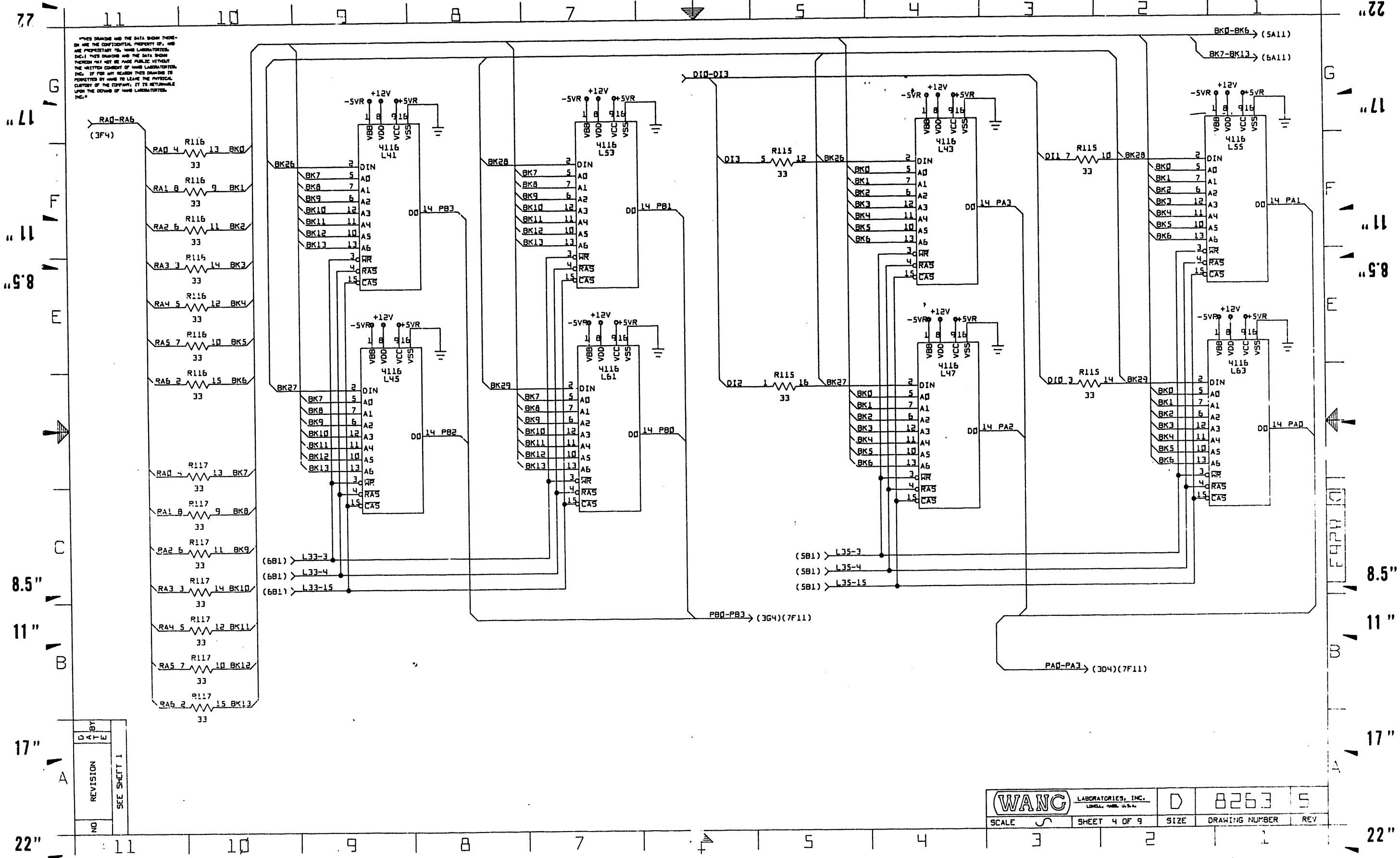


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SEE SHEET 1

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SCALE	SHEET 3 OF 9	SIZE	DRAWING NUMBER REV

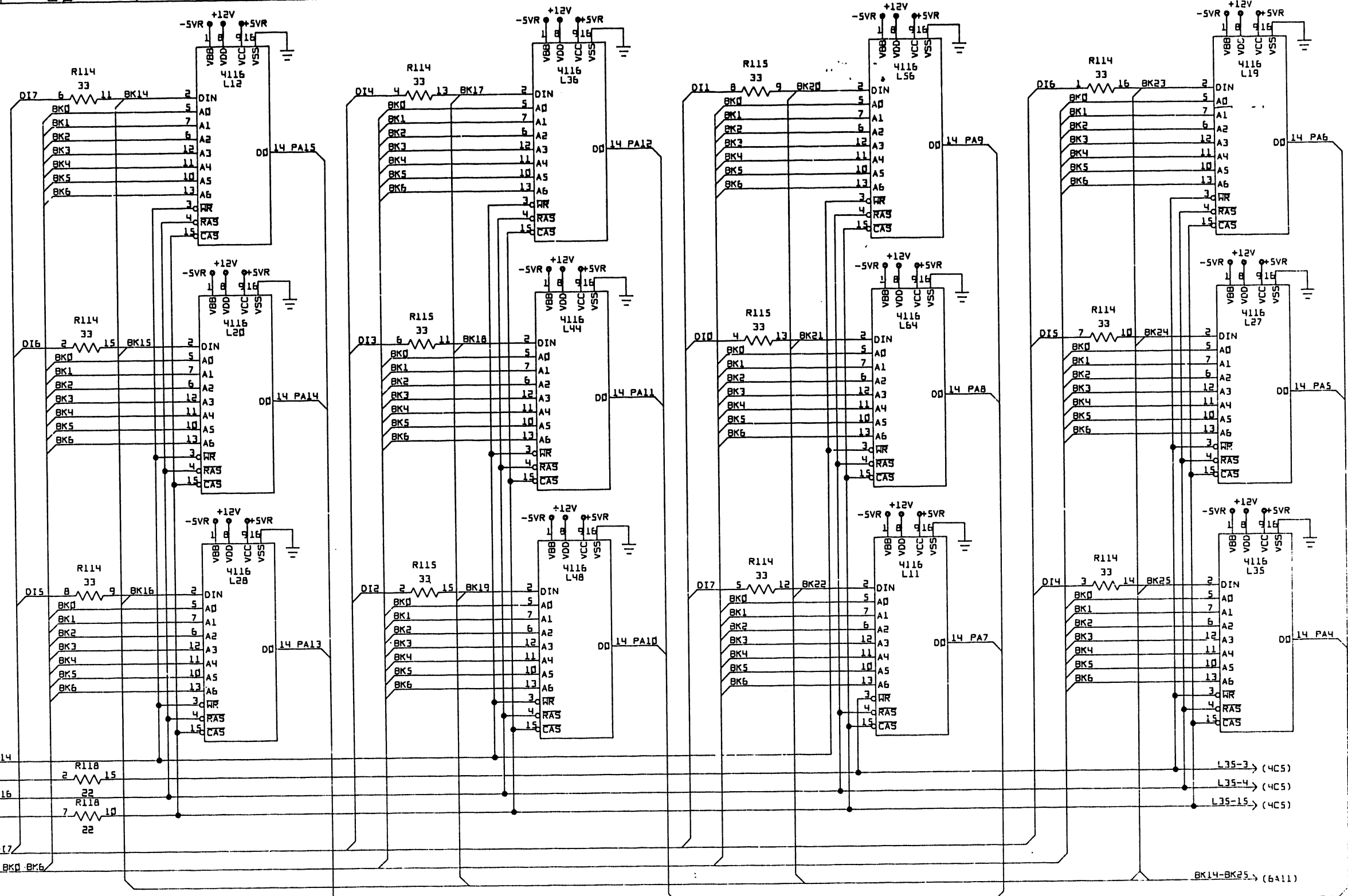
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WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		D	8263	S
SCALE	SHEET 4 OF 9	SIZE	DRAWING NUMBER	REV

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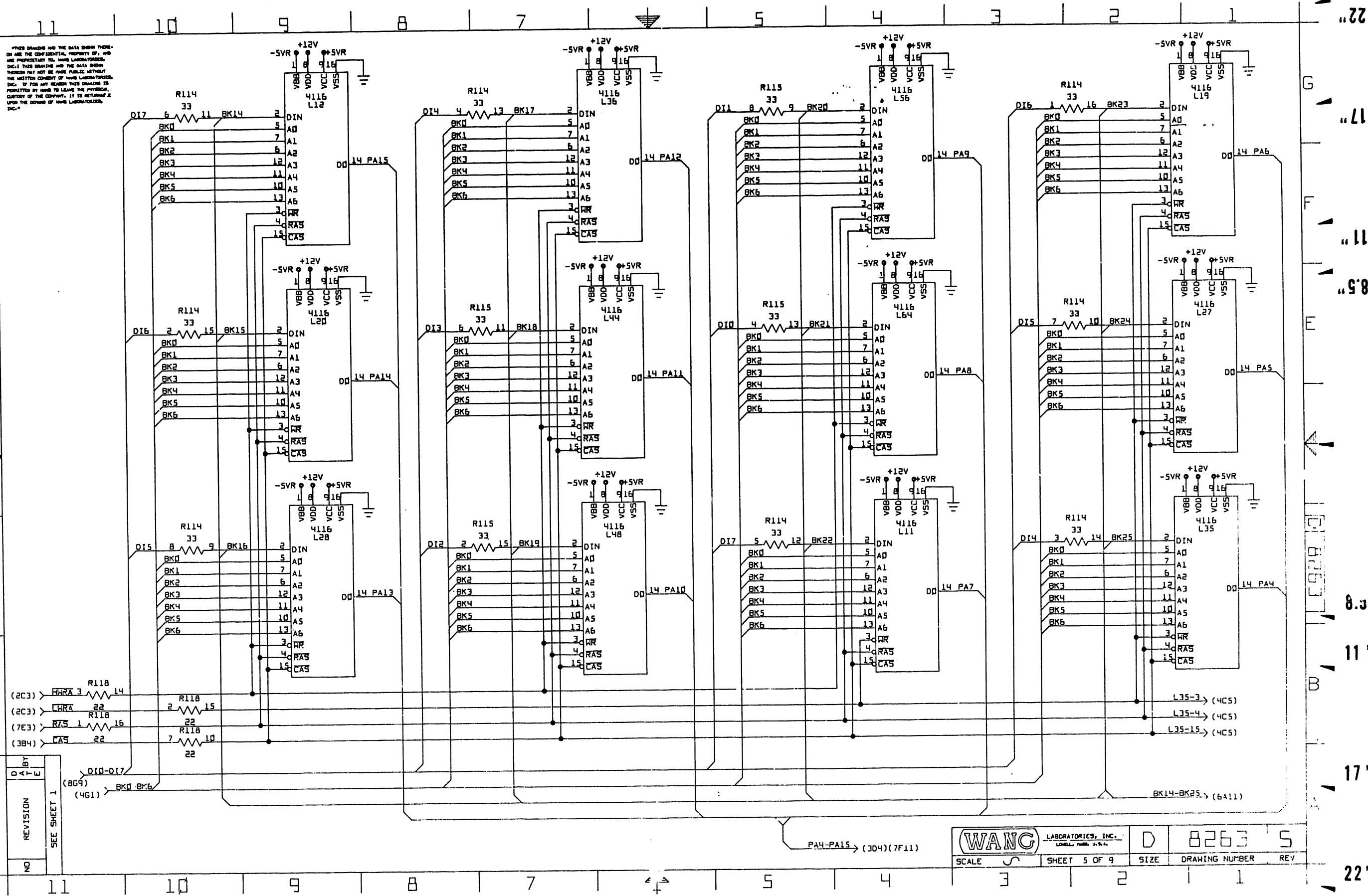
(2C3) > R118 14
 (2C3) > R118 22
 (7E3) > R118 16
 (3B4) > CAS 22

NO	BY	DATE
REVISION		
SEE SHEET 1		

D10-D17
 (8G4) BK0-BK6
 (4G1)

PA4-PA15 (304)(7F11)

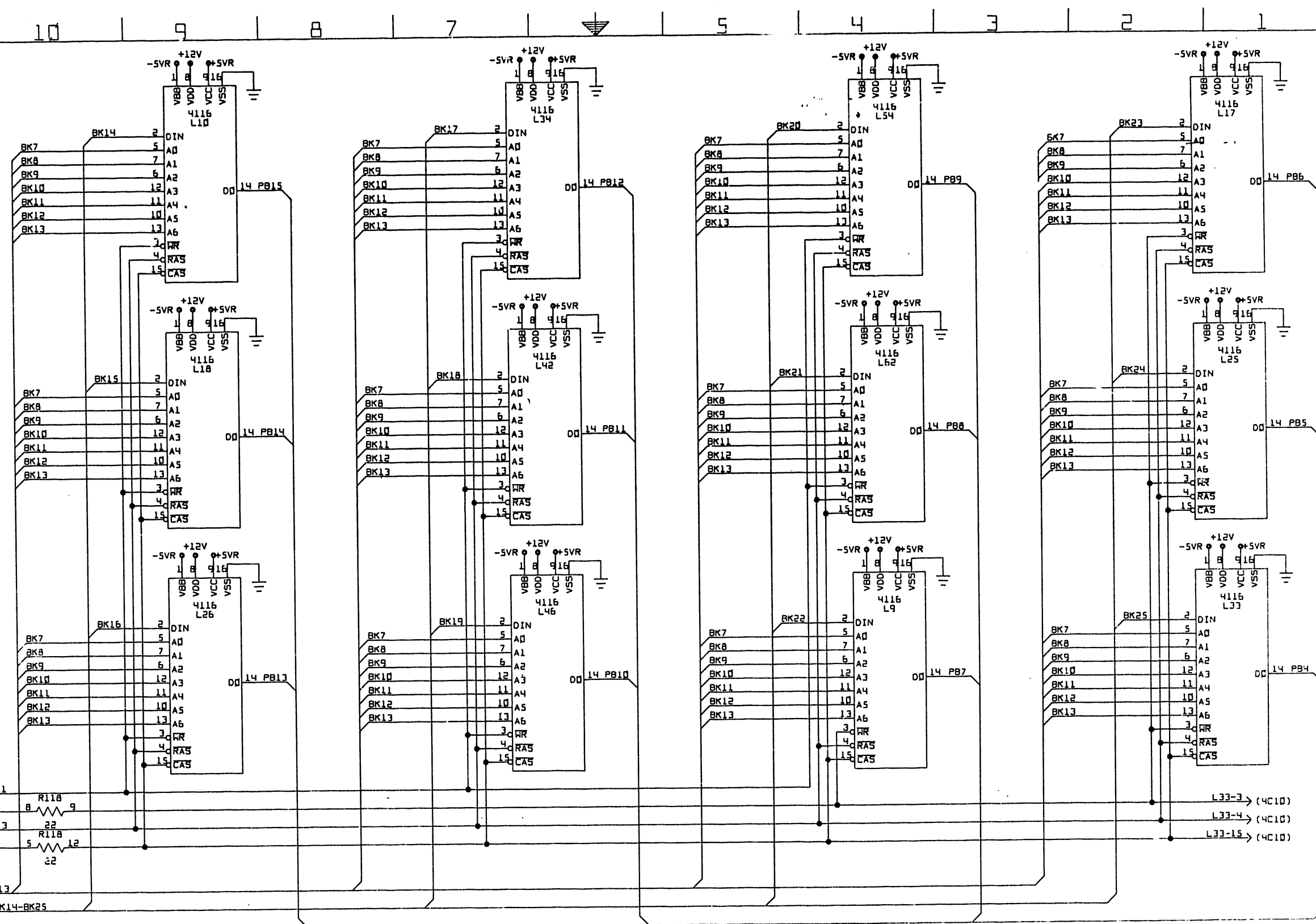
	LABORATORIES, INC.	D	8263	S
	SCALE			



22"
17"
11"
8.5"
8.5"
11"
17"
22"

22"
17"
11"
8.5"
8.3"
11"
17"
22"

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(2C3) → R118 6 11
 (2C3) → R118 22 8 9
 (7E3) → RAS 4 13 22 5
 (3B4) → CAS 22 5 12 22

NO	REVISION	DATE
	SEE SHEET 1	

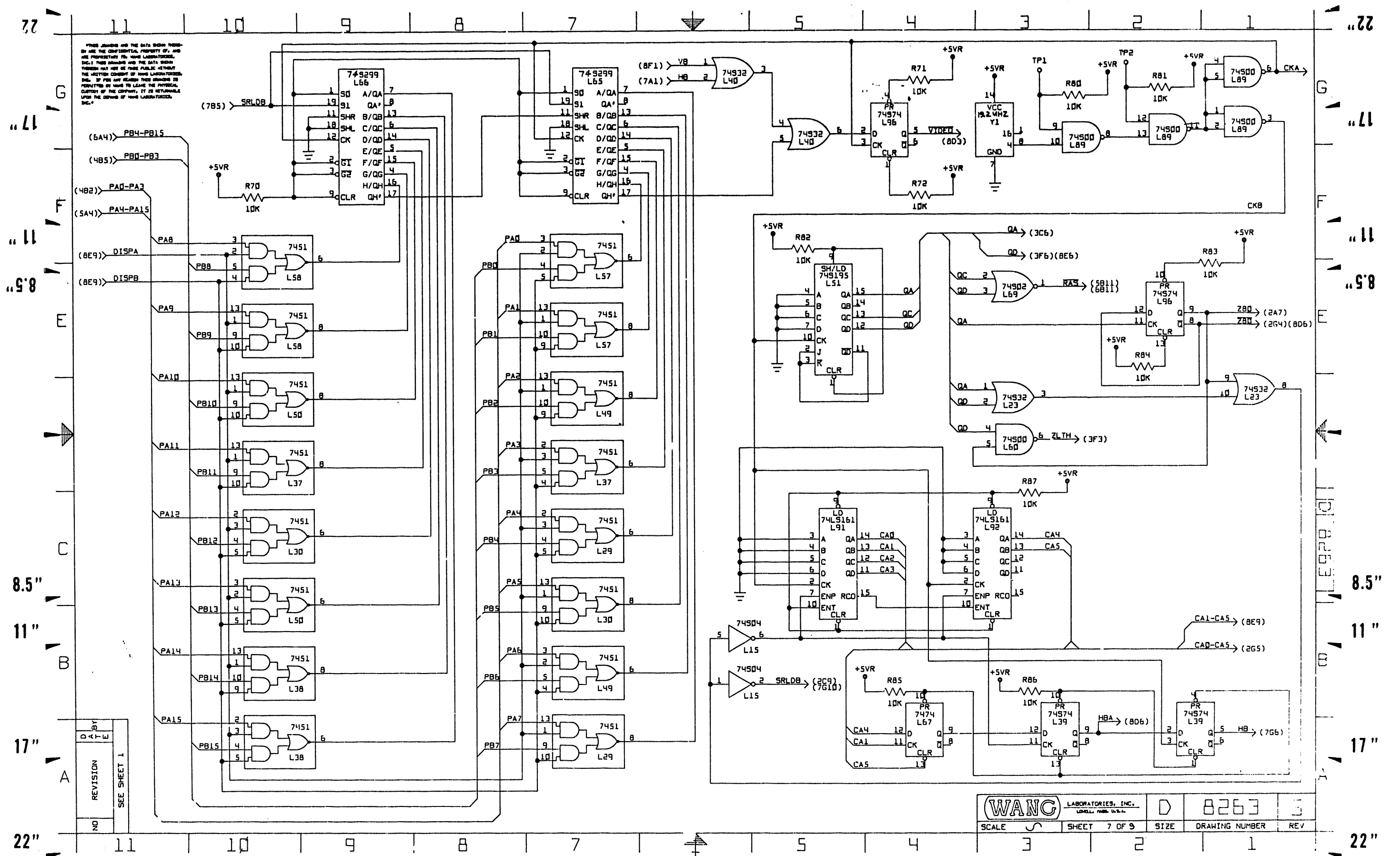
(4G1) BK7-BK13
 (5A1) BK14-BK25

PB4-PB15 (3G4)(7F11)

WANG LABORATORIES, INC.
 MODEL MADE U.S.A.

D 8263
 SCALE SHEET 6 OF 9 SIZE DRAWING NUMBER REV

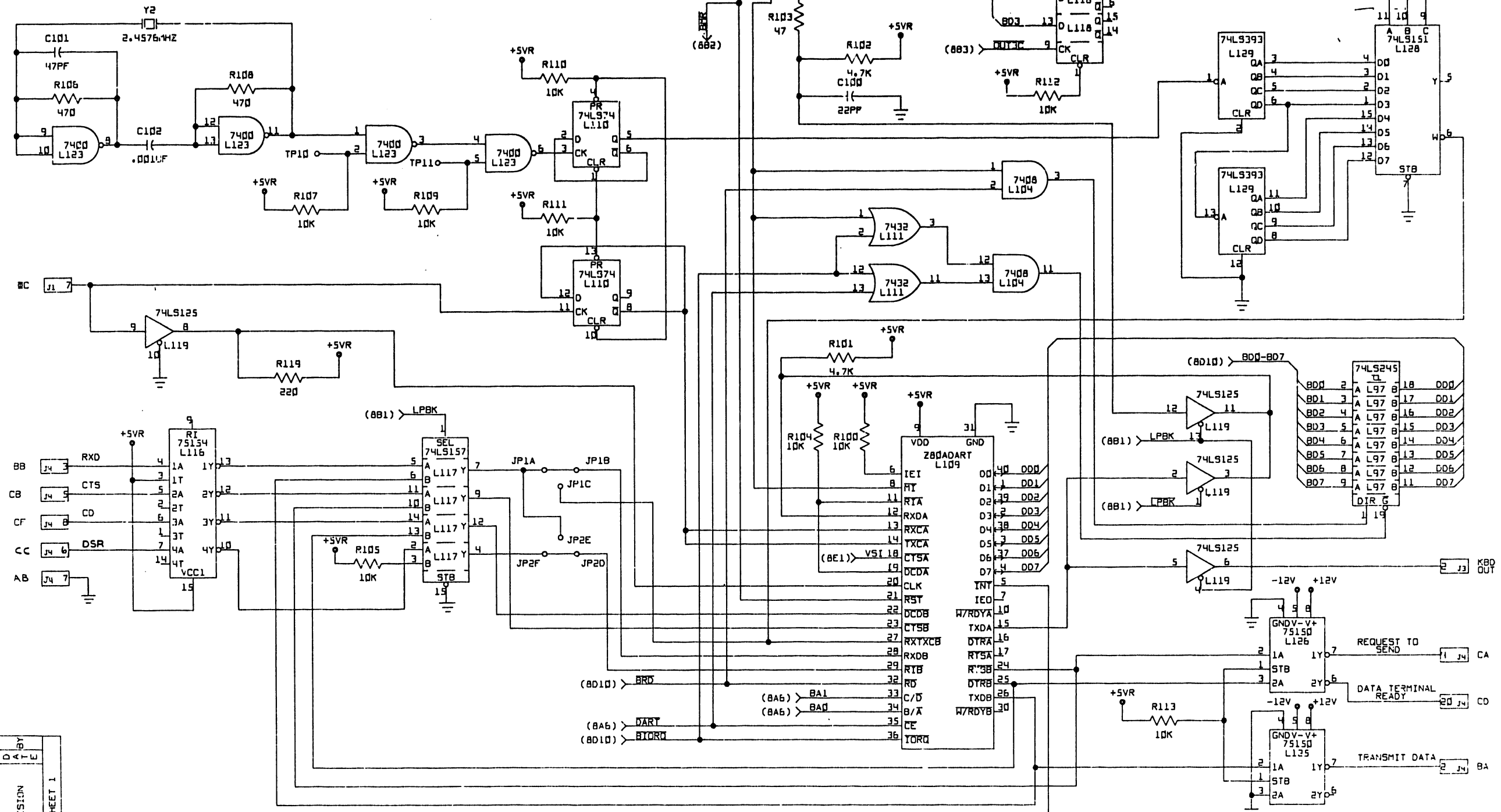
27 11 10 9 8 7 5 4 3 2 1 22
 17 11 8.5 8.5 11 17 22
 G F E D C B A
 11 10 9 8 7 5 4 3 2 1 22



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REVISION		
SEE SHEET 1		

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NO	REVISION	DATE	BY

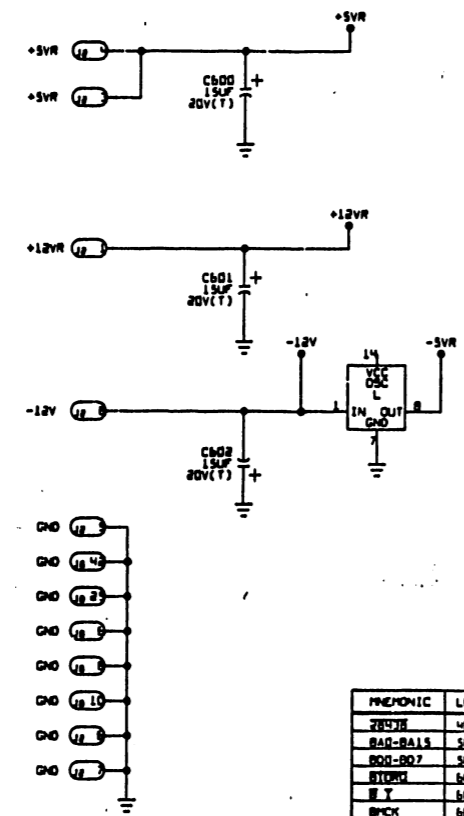
SEE SHEET 1

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.		D	8263	3
SCALE	SHEET 9 OF 9	SIZE	DRAWING NUMBER	REV

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NOTES

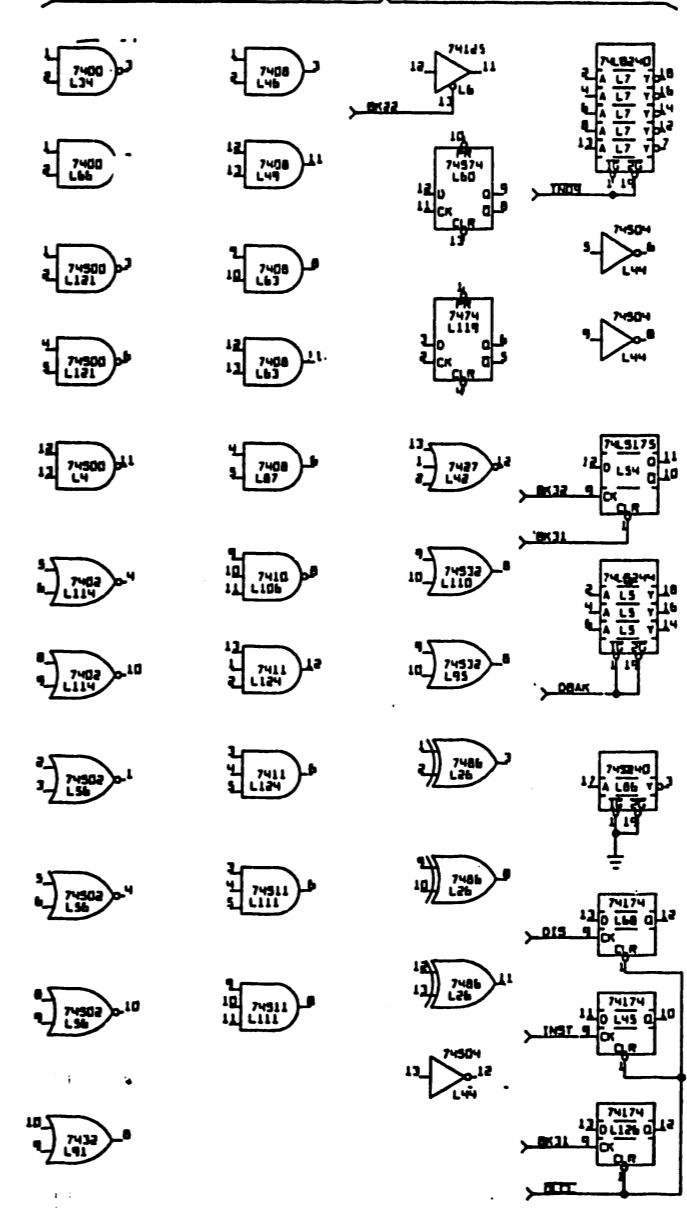
1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.



PHONIC	LOC.
7805	4C1
800-8A15	5F14
800-807	5F14
8100	6C1
81	6B1
820	6K10
81	6J11
81	6C1
81	6C1
81	6B2
81	6A12
81	6J11
81	4J14
81	4I8
81	6B12
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81	4I7
81	4F14
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81	6B3
81	6B13
81	6B13

210-202 + 378 RD NO 377			
210	202	L10	
8264	8264	378 RD-88-3-R1	

SPARES

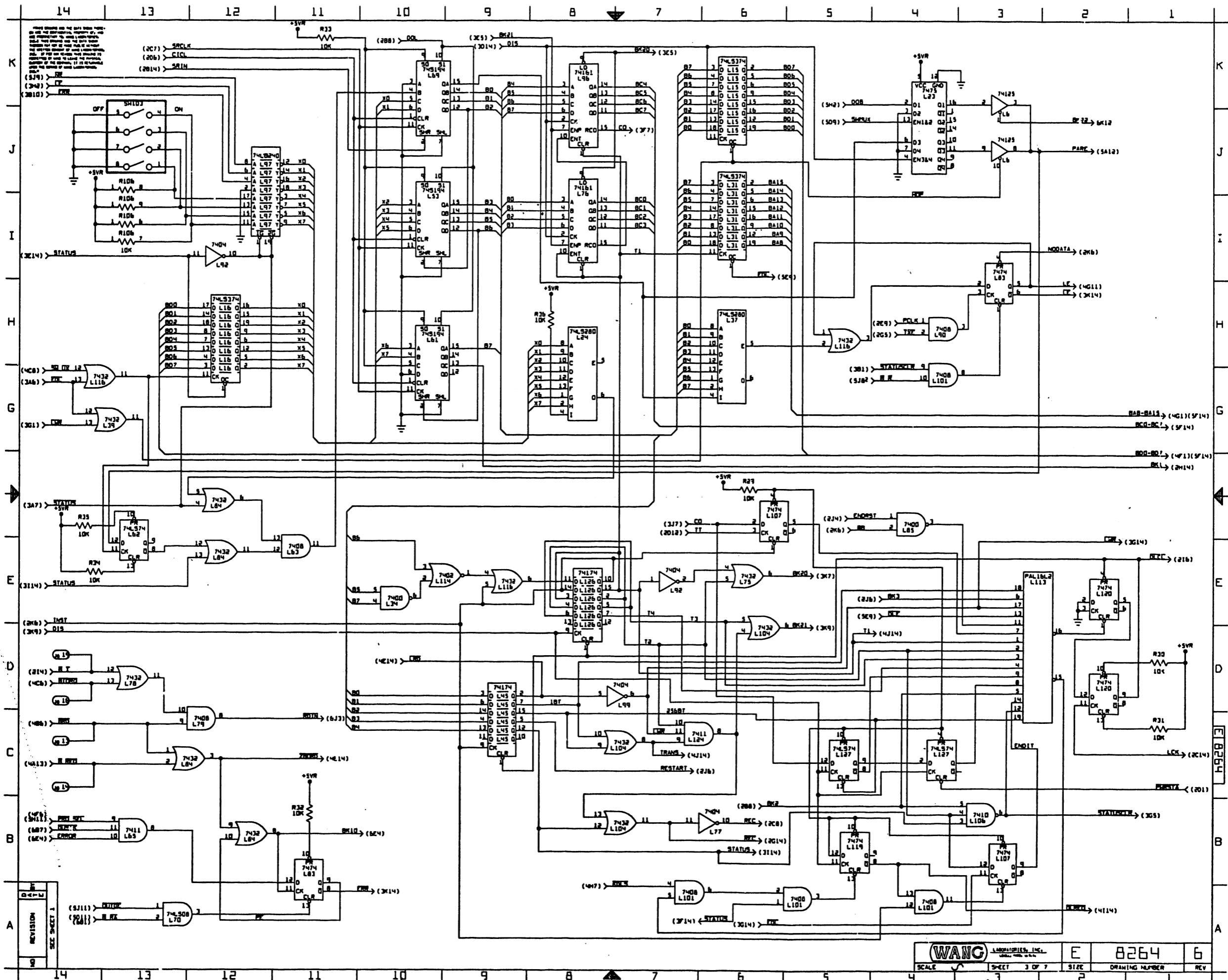


NO	REVISED PER	DATE	BY	NO	REVISED PER	DATE	BY	NO	REVISED PER	DATE	BY
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1	ORIGINATED PER	9/5/82	BN	2	REVISED PER	4/25/83	JSM	3	REVISED PER	5/16/83	JSM
2	ORIGINATED PER	9/5/82	BN	3	REVISED PER	4/25/83	JSM	4	REVISED PER	6/7/83	BN
3	ORIGINATED PER	9/5/82	BN	5	REVISED PER	6/7/83	BN	6	REVISED PER	9/15/83	KTH
4	ORIGINATED PER	9/5/82	BN	7	REVISED PER	2-16-84	JSM				

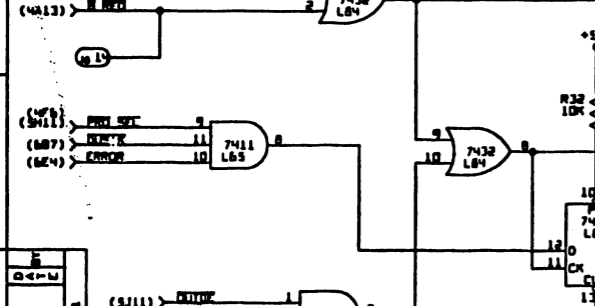
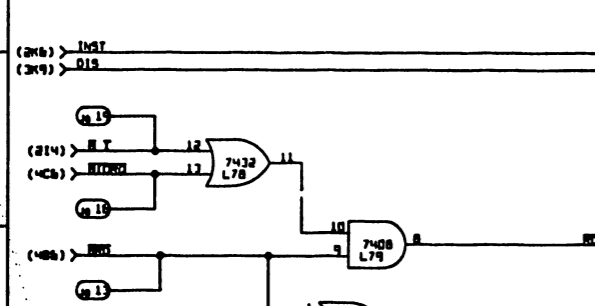
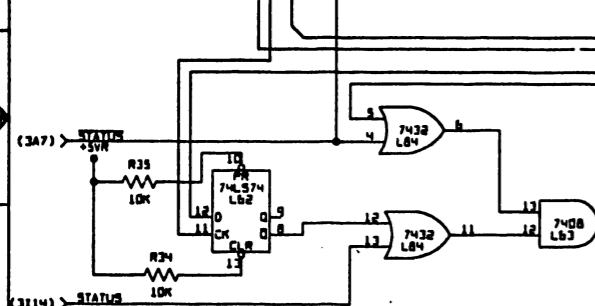
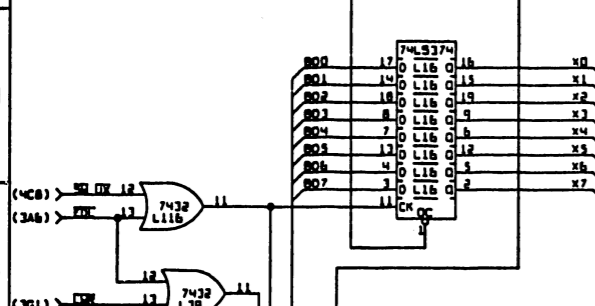
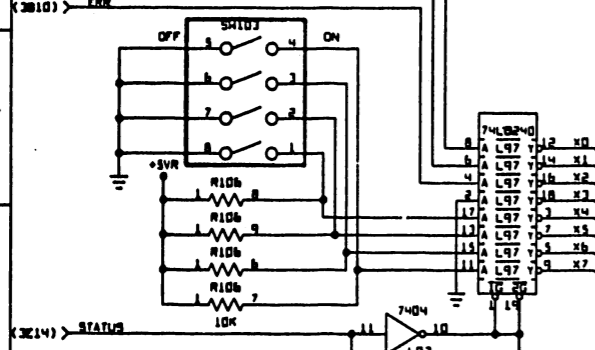
WANG LABORATORIES, INC.		SCHEMATIC DIAGRAM			
TITLE		CPU			
NO. 1	PI/DIA	WANG PART NUMBER	DNM	BN	CHK
GRAPH	TERM	SEE CHART	DJE	ENL	SJ
SCALE		SHEET 1 OF 7		SIZE	DRAWING NUMBER
				8264	6
				REV	

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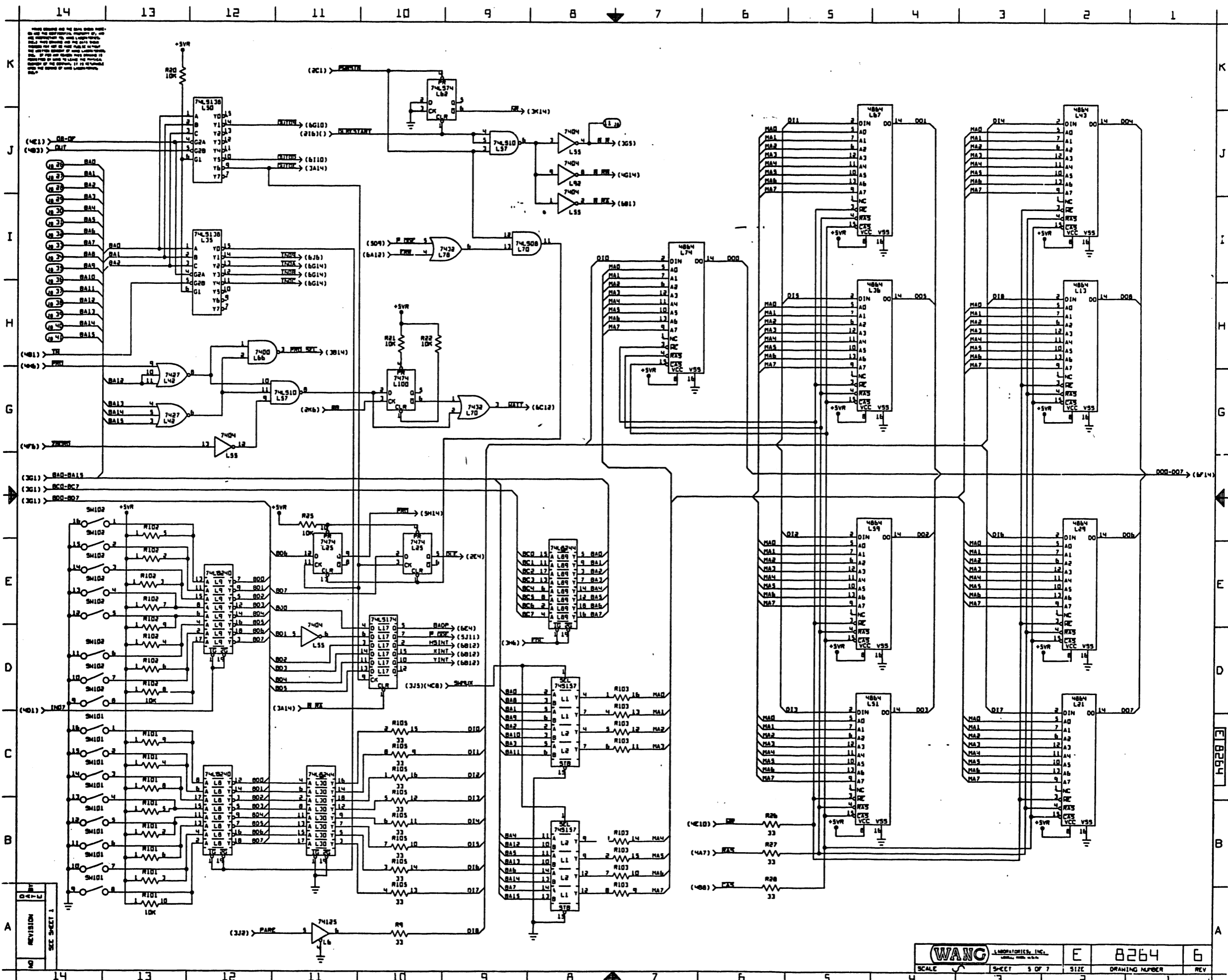
14 13 12 11 10 9 8 7 6 5 4 3 2 1



(317) SRCLK
 (207) C1C1
 (206) C1C2
 (2014) SRIN
 (318) SR
 (342) ST
 (2010) ST



NO	REVISION
1	REVISED
2	REVISED
3	REVISED
4	REVISED
5	REVISED
6	REVISED
7	REVISED
8	REVISED
9	REVISED
10	REVISED
11	REVISED
12	REVISED
13	REVISED
14	REVISED



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NO	REVISION	DATE

14 13 12 11 10 9 8 7 6 5 4 3 2 1

These drawings and the data herein represent the design of the equipment. They are not to be construed as a contract. The manufacturer shall be responsible for the proper interpretation of the drawings and the data herein. The manufacturer shall be responsible for the proper interpretation of the drawings and the data herein. The manufacturer shall be responsible for the proper interpretation of the drawings and the data herein.

ITEM NO.	IC LOCATION	TYPE	M.L. PART NO.	QTY
1	L1,L2	745157	376-0217	2
2	L4,L5,L6,L9,L121	74500	376-0228	4
3	L3,L12,L18,L19,L30,L31	74LS244	376-0288	6
4	L8,L33	74125	376-0324	2
5	L7,L9,L97	74LS240	376-0297	4
6	L10 IN SKT	272APROM	376-0043	1
7	L11 IN SKT	280ACPU	377-0368	1
8	L13,L21,L29,L36,L43,L31,L39,L37,L34	4884-2	397-0415	9
9	L14-L16,L20,L28,L31	74LS374	376-0286	6
10	L17	74LS174	376-0159	1
11	L22	74LS373	376-0310	1
12	L23	7475	376-0013	1
13	L24,L37,L41	74LS280	376-0242	3
14	L25,L26,L27,L100,L107,L112,L118,L119,L120,L48	7474	376-0006	10
15	L28	7486	376-0036	1
16	L27	74LS245	376-0285	1
17	L24,L66,L73,L85	7400	376-0002	4
18	L35,L50,L80	74LS138	376-0294	3
19	L39,L75,L78,L84,L91,L104,L116	7432	376-0093	7
20	L40,L60,L72,L88,L93	74574	376-0202	5
21	L42	7427	376-0125	1
22	L44	74504	376-0197	1
23	L45,L68,L126	74174	376-0098	3
24	L46,L49,L63,L71,L79,L90,L101	7408	376-0081	7
25	L106	7410	376-0003	1
26	L52,L53,L61,L69,L109	745194	376-0221	5
27	L54	74LS175	376-0160	1
28	L55,L77,L92,L99	7404	376-0010	4
29	L56,L105	74502	376-0199	2
30	L58	74LS139	376-0226	1
31	L65,L124	7411	376-0194	2
32	L76,L96,L103,L117,L122	74161	376-0094	5
33	L82	9602	376-0104	1
34	L86	745240	376-0334	1
35	L87	74508	376-0200	1
36	L95,L110	74532	376-0205	2
37	L98	74153	376-0048	1
38	L111	74511	376-0237	1
39	L113 IN SKT	16L2PAL	377-0037	1
40	L114	7402	376-0016	1
41	L125	74538	376-0298	1
42	L128	339	376-0240	1
43	L129	75113	376-0256	1
44	L130	75107	376-0146	1
44A	L47	74510	376-0238	1
44B	L57	74LS10	376-0209	1
44C	L62,L15,L23,L27	74LS74	376-0155	4
44D	L70	74LS08	376-0153	1

ITEM NO.	COMPONENT	TYPE	M.L. PART NO.	QTY
45	R1-R8,R13-R25,R29-R45,R48,R51,R52,R55-R64,R77,R78,R79	10K 1/4W 5%	330-4011	54
46	R9,R26-R28	33 1/4W 5%	330-1034	4
47	R46	390 1/4W 5%	330-2040	1
48	R47	91 1/4W 5%	330-1092	1
49	R49	270 1/4W 5%	330-2028	1
50	R50,R66	100 1/4W 5%	330-2011	2
51	R53	39K 1/4W 5%	330-4040	1
52	R54	22K 1/4W 5%	330-4023	1
53	R65	120K 1/4W 5%	330-5013	1
54	R67,R3	330 1/4W 5%	330-2034	2
55	R68,R69	12K 1/4W 5%	330-4013	2
56	R70	510 1/4W 5%	330-2052	1
57	R71	24K 1/4W 5%	330-4025	1
58				
59	R74	12 1/4W 5%	330-1013	1
60	R75	1K 1/4W 5%	330-3011	1
61	R76	22 1/4W 5%	330-1023	1
62	R101,R102,R104,R106	10K RES NETWORK	333-0809	4
63	R103,R105	33 RES NETWORK	333-0835	2
64				
65	C1,C2,C9-C16	.10F 50V	300-1833	10
66	C3,C17-61	.1F 50V	300-1966	46
67	C4,C600-R602	150F 20V (T)	300-4022	4
68	C5	.00150F 500V	300-1907	1
69	C6	100PF 500V	300-1100	1
70	C7	6.8UF 35V (T)	300-4038	1
71	C8	220UF 15V (T)	300-4045	1
72	C62	10PF	300-1969	1
73	Y1	16MHz CRYSTAL	321-015	1
74	Y2	17.1 OSC	321-1006	1
75	SH101,SH102	8-POS. SWITCH	325-1503	2
76	SH103	4-POS. SWITCH	325-1504	1
77	J2	8-POS CONN	350-0210	1
78	J3	BNC	350-3070	1
79	J4	TNC	350-3071	1
80	J6	50 PIN CONN	350-0228	1
81	L10	24-PIN SKT	376-9003	1
82	L11	40-PIN SKT	376-9011	1
83	D1,D2	IN4004	380-4000	1
84	D3	4.7V	380-2048	1
85	Q1	MP3 6551	375-1050	1
86		BRACKET, REAR	451-5233	1
87	FOR J3,J4	HEX NUT	652-6025	2
88	FOR J3,J4	WASHER	652-6047	2
89		RIVET	651-0406	2
90	Y1,Y2	16 PIN SPACER	376-9008	2

REVISION
SHEET 1 OF 7

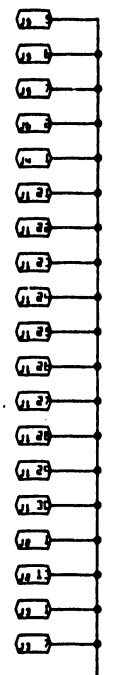
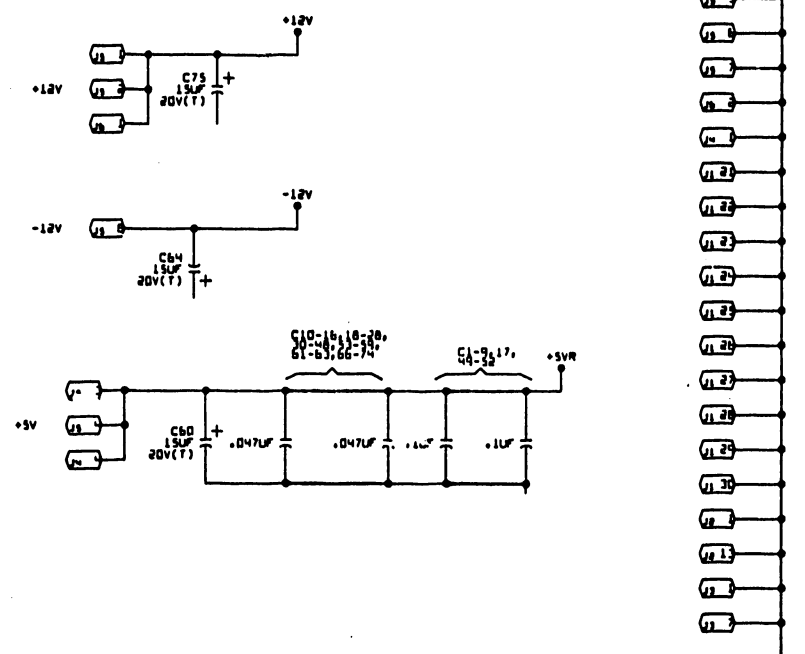
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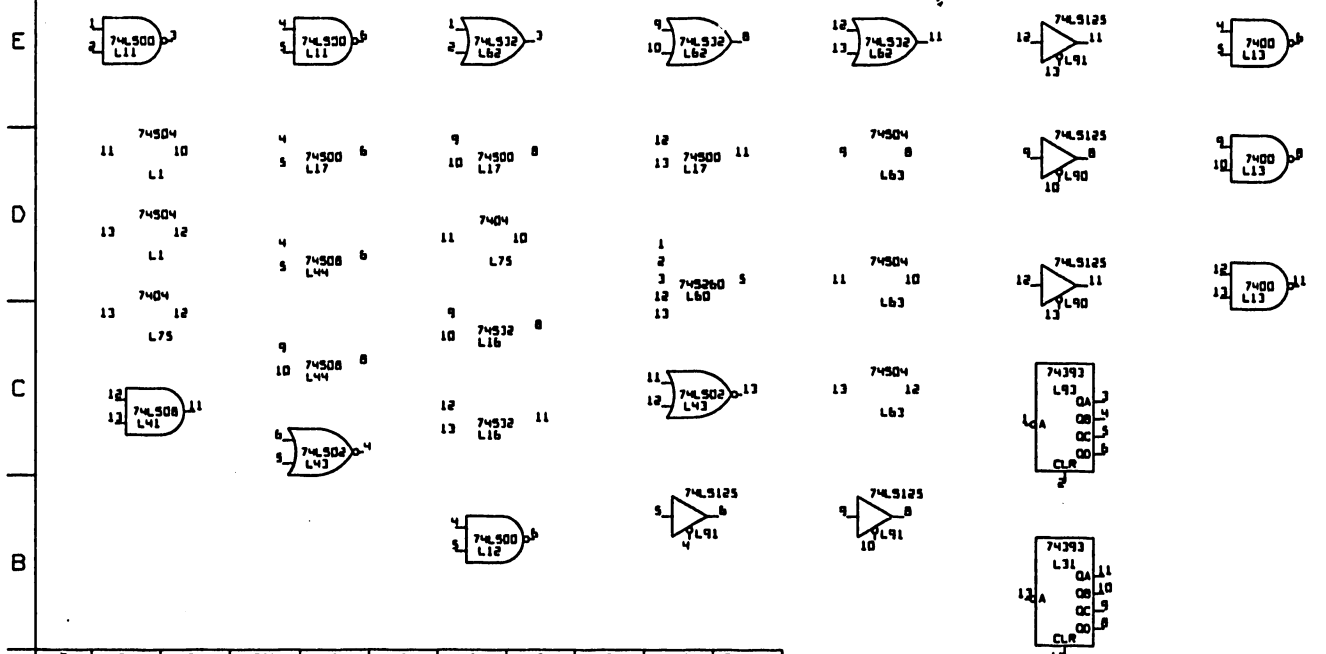
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NOTES

1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.



SPARES



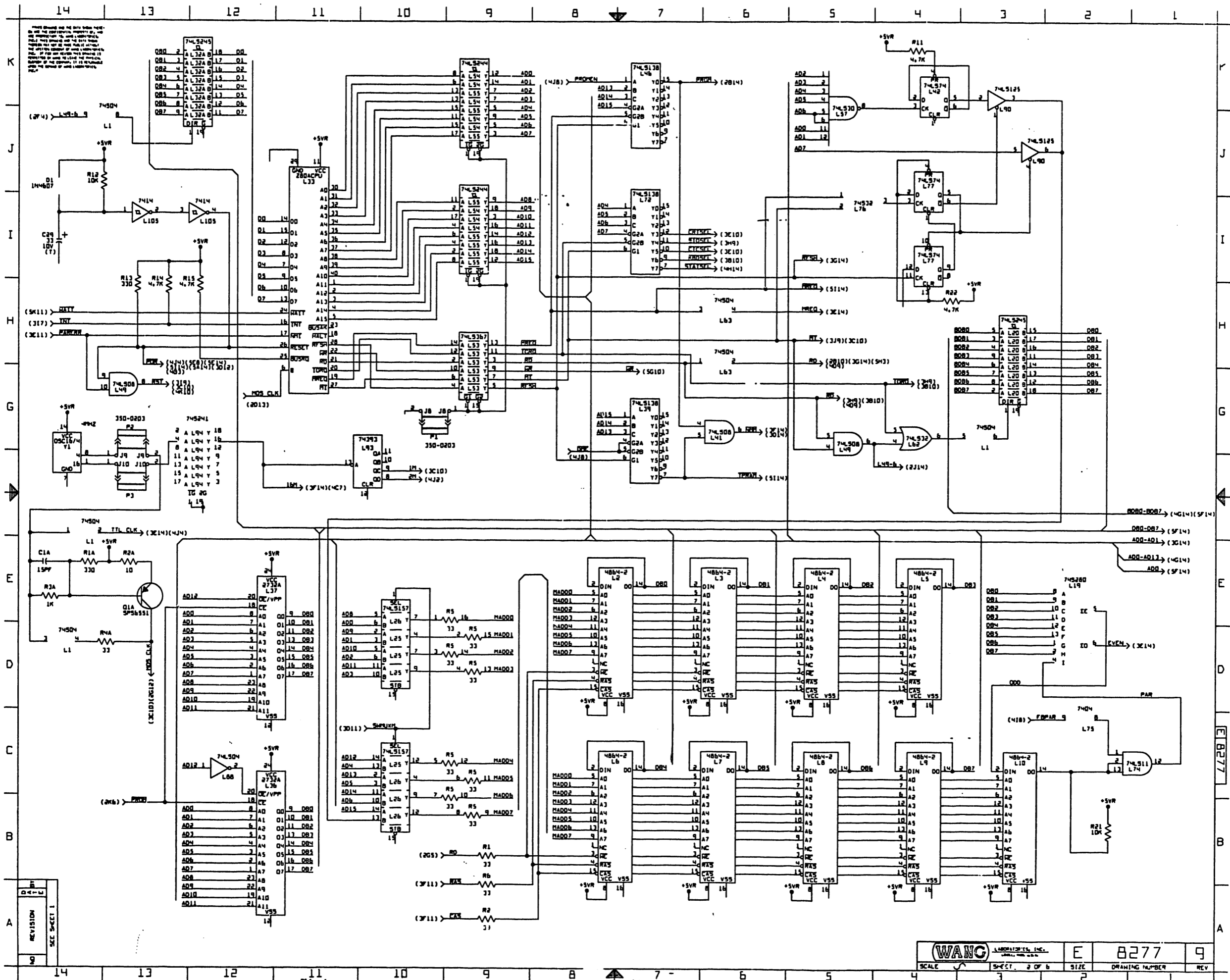
210-209 + 377 OR 378					
210	209	L33	L34, 35, 66, 67	L36	L37
8277-A	8277	397-0368	397-0430	378-8052	378-8047

E REV 3 N

REV	DATE	BY	CHKD	APP'D	DESCRIPTION
1	3/28/83	BN	PGD	KTH	INITIAL DESIGN
2	4/29/83	BN	KTH	KTH	REVISED PER ECO NO. 28152
3	7/22/83	PGD	KTH	KTH	REVISED PER ECO NO. 28153
4	9/6/83	KTH	KTH	KTH	REVISED PER ECO NO. 28154
5	10/5/83	KTH	KTH	KTH	REVISED PER ECO NO. 28155
6	3-03-84	KTH	KTH	KTH	REVISED PER ECO NO. 30353
7	3-03-84	KTH	KTH	KTH	REVISED PER ECO NO. 30355
8	3-03-84	KTH	KTH	KTH	REVISED PER ECO NO. 32159
9	3-15-84	BSR	KTH	BSR	REVISED PER ECO NO. 31871
10	06/01/84	R.B.P.	KTH	R.B.P.	INITIAL CHECK

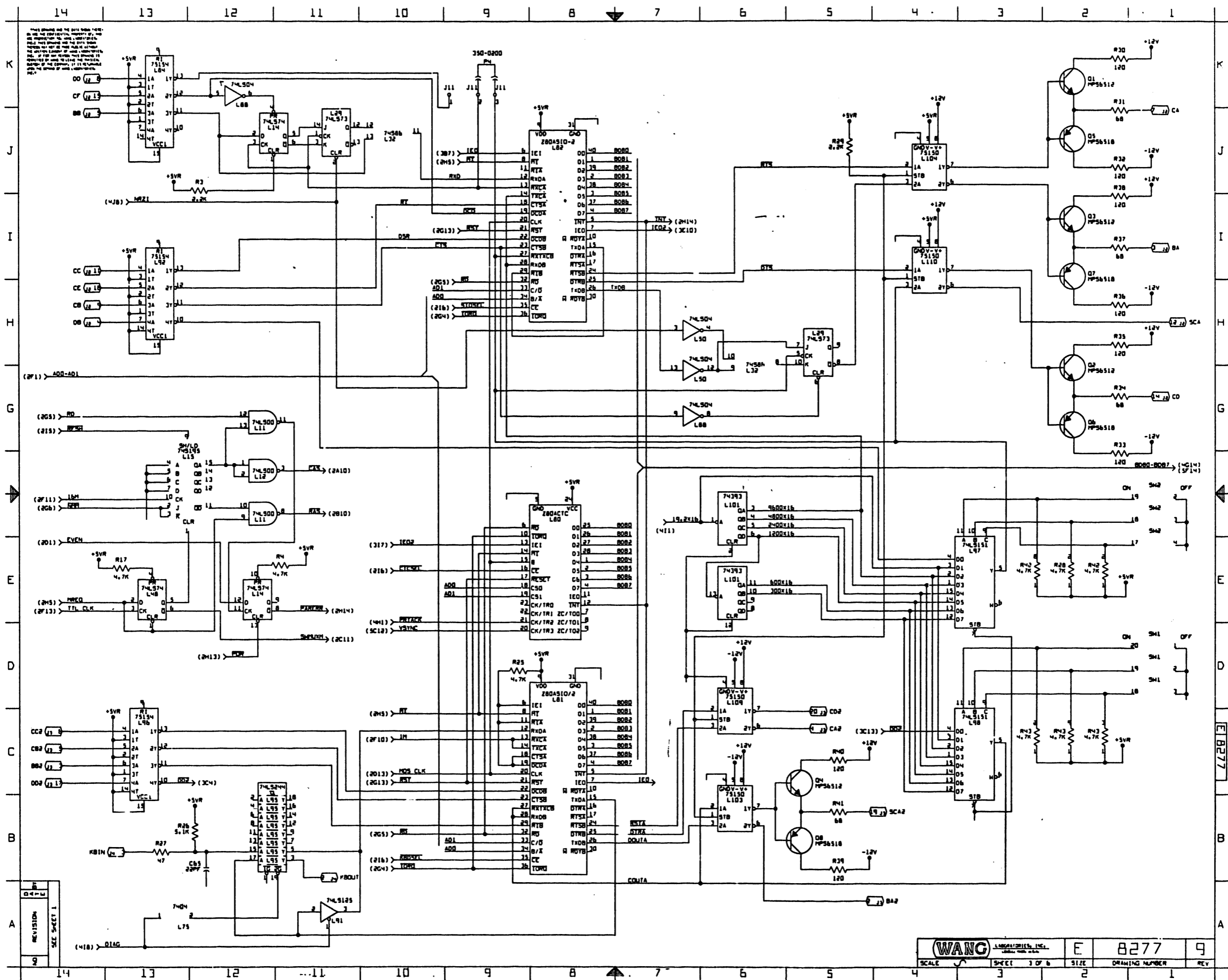
WANG LABORATORIES, INC.		SCHEMATIC DIAGRAM	
TITLE		REMOTE WORKSTATION	
DESIGN NUMBER	4200/V5-BA	WANG PART NUMBER	PO95A
DATE	3/28/83	SEE CHART	
SCALE	1/4" = 1"	SHEET	1 OF 6
SIZE	E	DRAWING NUMBER	8277
REV	9		

14 13 12 11 10 9 8 7 6 5 4 3 2 1



14 13 12 11 10 9 8 7 6 5 4 3 2 1
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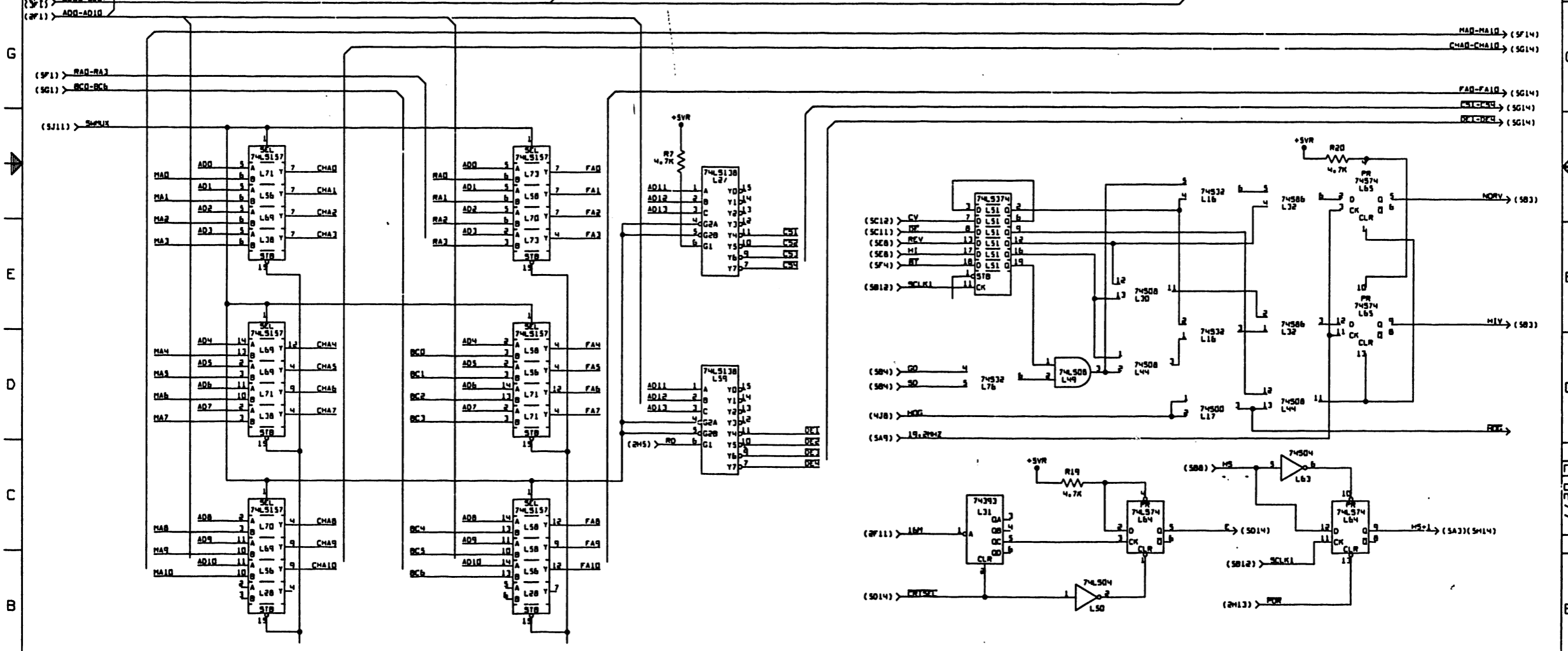
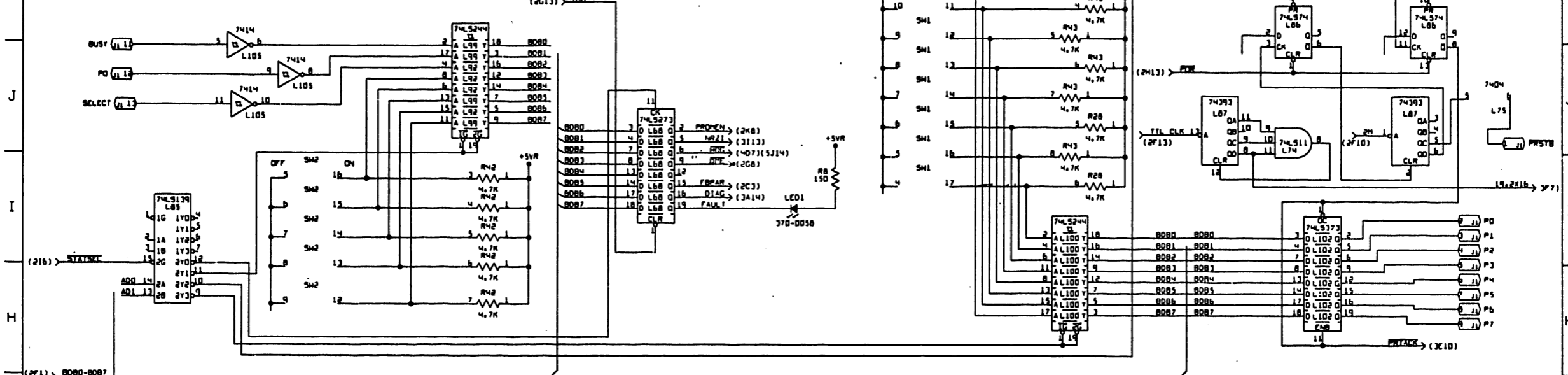
REV	DESCRIPTION
1	SEE SHEET 1



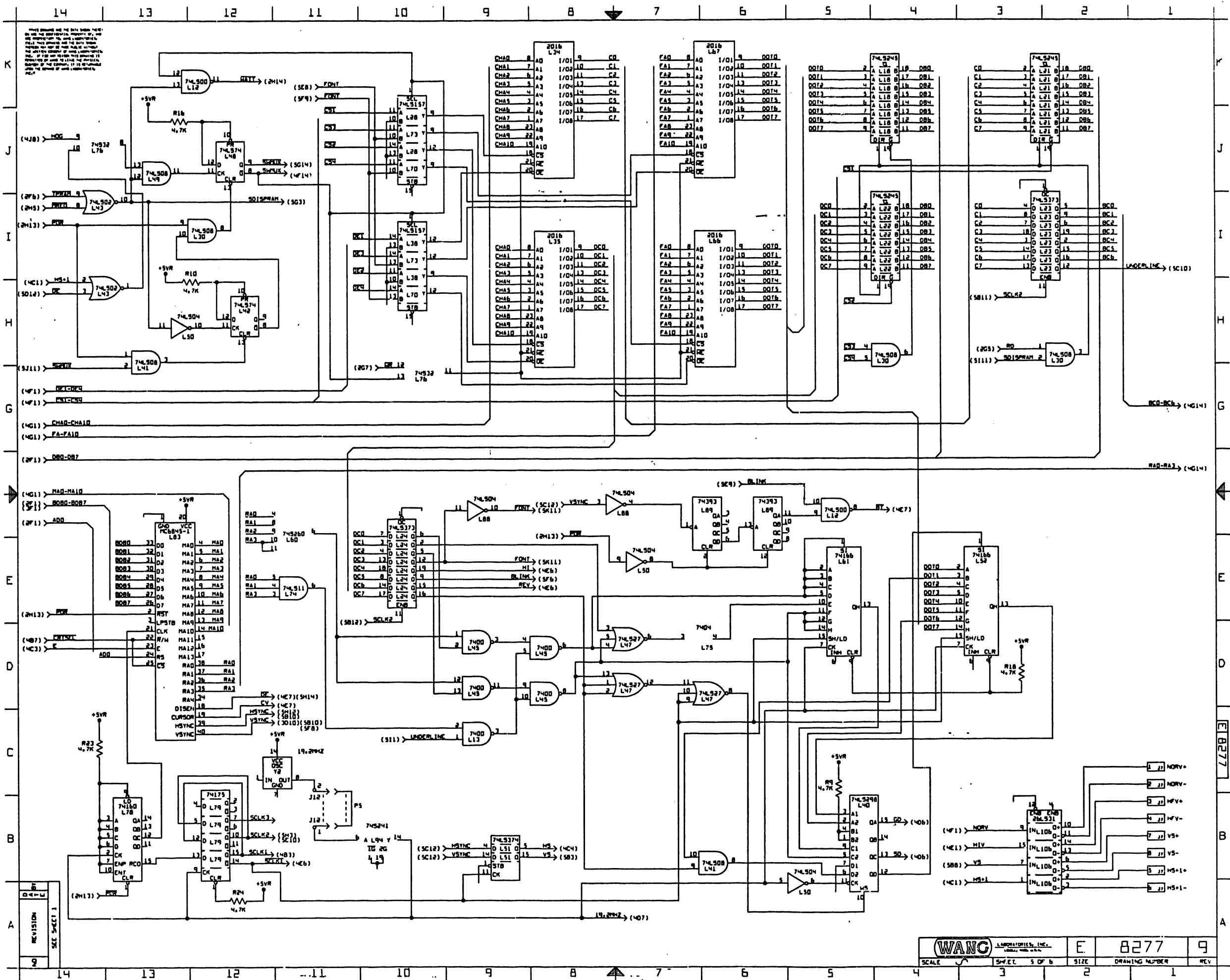
Notes shown on the data sheet refer to the manufacturer's literature and are not to be construed as a warranty or representation of any kind. The user is advised to consult the manufacturer's literature for the most current information regarding the operation of the device. The user is also advised to consult the manufacturer's literature for the most current information regarding the operation of the device.

REVISION	NO
SEE SHEET 1	

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NO.	REVISION
14	SEC. SPEC. 1



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REVISION
SEE SHEET 1

14 13 12 11 10 9 8 7 6 5 4 3 2 1

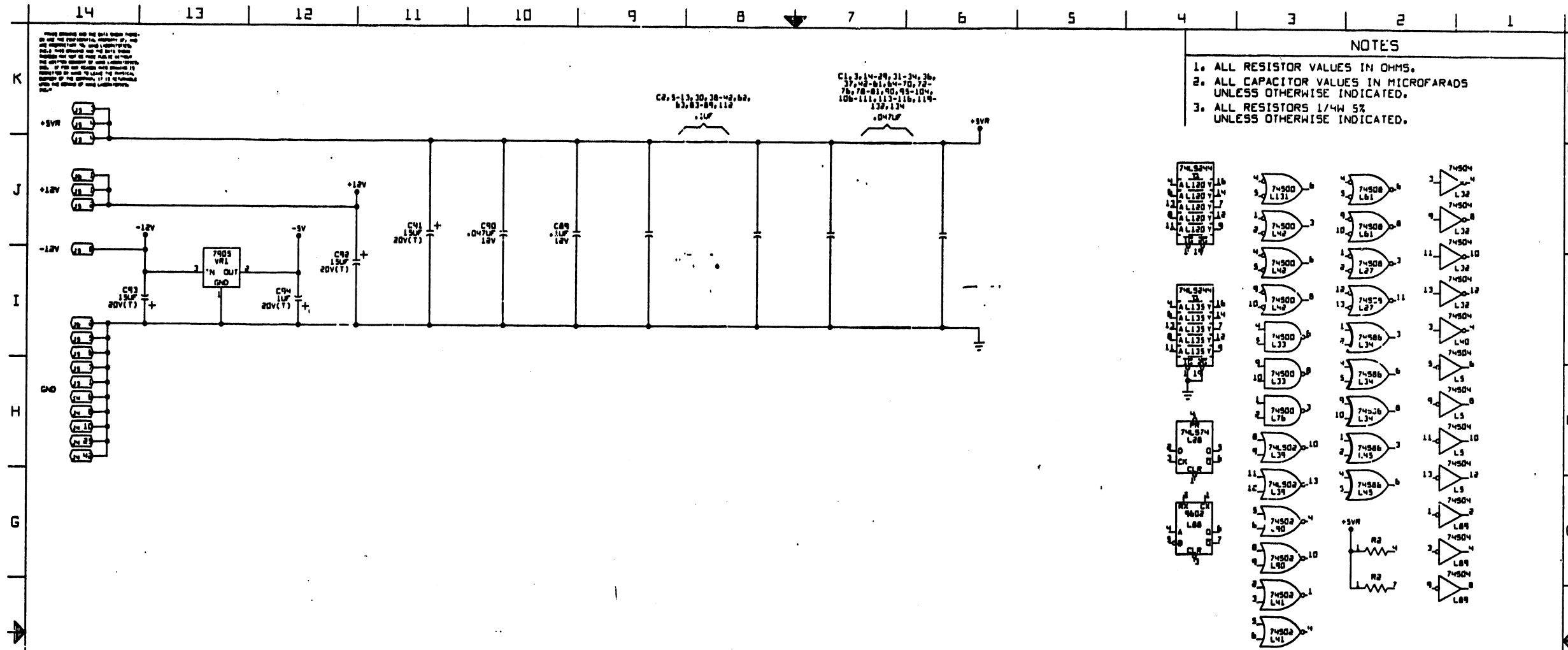
PLEASE CHECK FOR THE FOLLOWING: 1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED. 2. ALL DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED. 3. ALL DIMENSIONS ARE TO THE OUTSIDE UNLESS OTHERWISE SPECIFIED. 4. ALL DIMENSIONS ARE TO THE INSIDE UNLESS OTHERWISE SPECIFIED. 5. ALL DIMENSIONS ARE TO THE CENTER UNLESS OTHERWISE SPECIFIED. 6. ALL DIMENSIONS ARE TO THE OUTSIDE UNLESS OTHERWISE SPECIFIED. 7. ALL DIMENSIONS ARE TO THE INSIDE UNLESS OTHERWISE SPECIFIED. 8. ALL DIMENSIONS ARE TO THE CENTER UNLESS OTHERWISE SPECIFIED. 9. ALL DIMENSIONS ARE TO THE OUTSIDE UNLESS OTHERWISE SPECIFIED. 10. ALL DIMENSIONS ARE TO THE INSIDE UNLESS OTHERWISE SPECIFIED.

DESIGNATION	TYPE	HANG PART NO.
L1.83	74504	376-0197
L2.7, 2, 3, 4, 5, 6, 7, 8, 9, 10	4864-2	397-0417
L11.12	744500	376-0207
L107.108	95AHC	
L14, 48, 48, 64, 77, 86	744974	376-0155
L15	745195	376-0427
L62	744972	376-0211
L16, 76	745172	376-0203
L17	74500	376-0228
L18, 21, 22, 23, 24	744524	376-0285
L19	745280	376-0246
L23, 24, 102	744977	376-0310
L25-26, 28, 30, 36, 58, 64-71, 73	744917	376-0216
L27, 38, 46, 39, 77	744910	376-0294
L29	744973	376-0304
L30, 41, 49	744508	376-0137
L31, 32, 87, 89, 101	744977	376-0330
L32	74586	376-0271
L33	Z80ACPM	SEE CHART
L34, 35, 66, 67	2016	SEE CHART
L36	PH04	SEE CHART
L37	4220	SEE CHART
L40	744928	376-0232
L43	744502	376-0208
L44	74508	376-0200
L45, 13	74500	376-0002
L47	744927	376-0245
L50, 88	744504	376-0180
L51	744974	376-0286
L52, 61	74166	376-0109
L53	744937	376-0192
L54, 55, 56, 99, 100	744524	376-0288
L57	744970	376-0249
L60	745280	376-0206
L65	744974	376-0202
L68	744975	376-0302
L74	744911	376-0225
L75	7404	376-0010
L78	74160	376-0191
L79	74175	376-0119
L81, 82	Z80A510/2	397-0393
L83	6845-1	397-0473
L84, 92, 96	75154	376-0077
L85	744939	376-0226
L80	Z80ACTC	397-0371
L90, 91	744925	376-0486
L94	745241	376-0506
L97, 98	744931	376-0214
L103, 104, 109, 110	75150	376-0076
L105	7414	376-0139
L106	26, 371	376-0470
R28, 42, 43	4, 75 SIP	331-0812
R16, 17	330 0-4	330-2034
R27	47 0-4	330-1048
R31, 37, 34, 41	66 0-4	330-1065
R1, 2, 3, 4, 5	33 0-4	330-1074
R30, 32, 38, 26, 33, 35, 39, 40	120 0-4	330-2013
R3, 29	2, 2K	330-3023
R26	5, 1K	330-3052
R12, 21	10K	330-4011
R5	33 0-4 DIP	331-0835
R8	150 0-4	330-2016
R4, 7, 9-11, 14-20, 22-25	4, 7K	330-3048
R24	10	330-1011
R34	1K	330-3011

DESIGNATION	TYPE	HANG PART NO.
J1	26 PIN CONN	350-1060
J2	26 PIN CONN	350-0200
J3	25 PIN CONN	350-1047-M
J4	4 POS CONN	350-0540
J5	8 POS CONN	350-0210
J6	3 POS CONN	350-0539
J7	8 POS CONN	350-0542
J8, 9, 10, 12	2 POS CONN	350-0203
J11	3 POS CONN	654-0104
P1-P5	2 POS. SHUNT	350-4506
SH1, 2	10 POS. DIP	325-0069
LED1	LED, RED	370-0058
CR0, 64, 73	15W 25V (T)	300-4022
CR5	33W 10V (T)	300-4024
C1-9, 17, 49-52	10W 50V	300-1833
C10, 16, 18-20, 20-40, 51-54, 61-63, 66-74	0.047UF 50V	300-1966
C65	22PF	300-1022
C16	15PF	300-1015
D1	0100K 1N4007	380-1005
DS, 7, 8, 8	MS56518	375-1014
Q1, 2, 2, 4	MS56512	375-1012
Q14	MS56531	375-1050
Y2	15, 20W XIAL	321-1007
Y1	40W XIAL	321-1004
L33	40 PIN SMT	376-9011
L36, 37	24 PIN SMT	376-9003
Y1, Y2	TERNA 16 PIN	376-9008
(QTY) 2	STANCOFF	462-0548
(QTY) 6	SCR 22	651-0014
(QTY) 2	RIVET	651-0406
(QTY) 2	NUT	652-2004
(QTY) 2	WASHER	653-2002
(QTY) 1	DRKT PCB W/LABEL	451-5230

NO	REVISION	SEE SHEET 1
04	U	

14 13 12 11 10 9 8 7 6 5 4 3 2 1



- NOTES
1. ALL RESISTOR VALUES IN OHMS.
 2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
 3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.

210 • 209 • 377 OR 378						
210	209	L3	L72	L73	L116	L38
8287-A	8287	377-0368	377-0427	378-6099-R3	377-0508	378-8046
8287-1A	8287-1	377-0368	377-0427	378-6099-R3	377-0508	377-0418

* VARIATION CHART

BOARD NO.	LOCATION	M.L. PART NO.
8287 (4830)	L46, 49, 93-98	397-0476
	L50	377-3044
	L69	377-3043
8287-1 (4805)	L93, 96, 97	DO NOT LOAD
	L50	377-3065
	L69	377-3066

8287-1
E REV
1

8287
E REV
4

N

REV	DATE	BY	CHKD	APP'D	DESCRIPTION
1	3/23/83	JSM			ORIGINATED PER DMR NO. 21035 APPRI
2	6/27/83	JSM			REVISION PER CADM. SPEC. DMR NO. 21535 APPRI
3	9/19/83	KTH			REVISION PER ECD NO. 28780 APPRI
4	10/12/83	KTH			REVISION PER ECD NO. 291570 APPRI
5	10/12/83	KTH			REVISION PER ECD NO. 294210 APPRI
6	12/7/83	PGD			REVISION PER ECD NO. 30013 APPRI RLL

WANG LABORATORIES, INC.

SCHMATIC DIAGRAM

TITLE: SINGLE BD WS M/L

FORM NUMBER: M0095C 4230

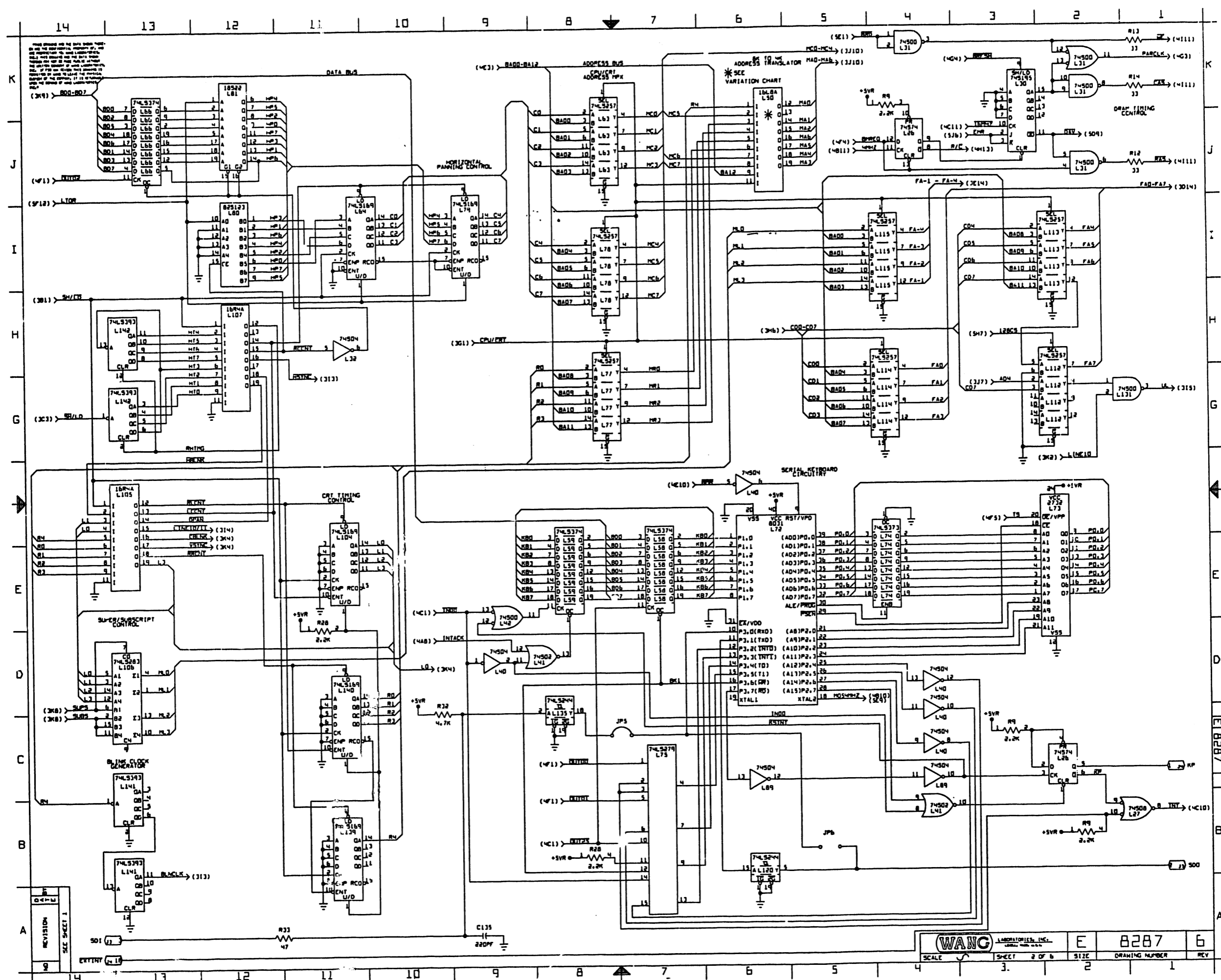
WANG PART NUMBER: SEE CHART

SCALE: SHEET 1 OF 6

SIZE: 8287 6

DRAWING NUMBER: 8287 6

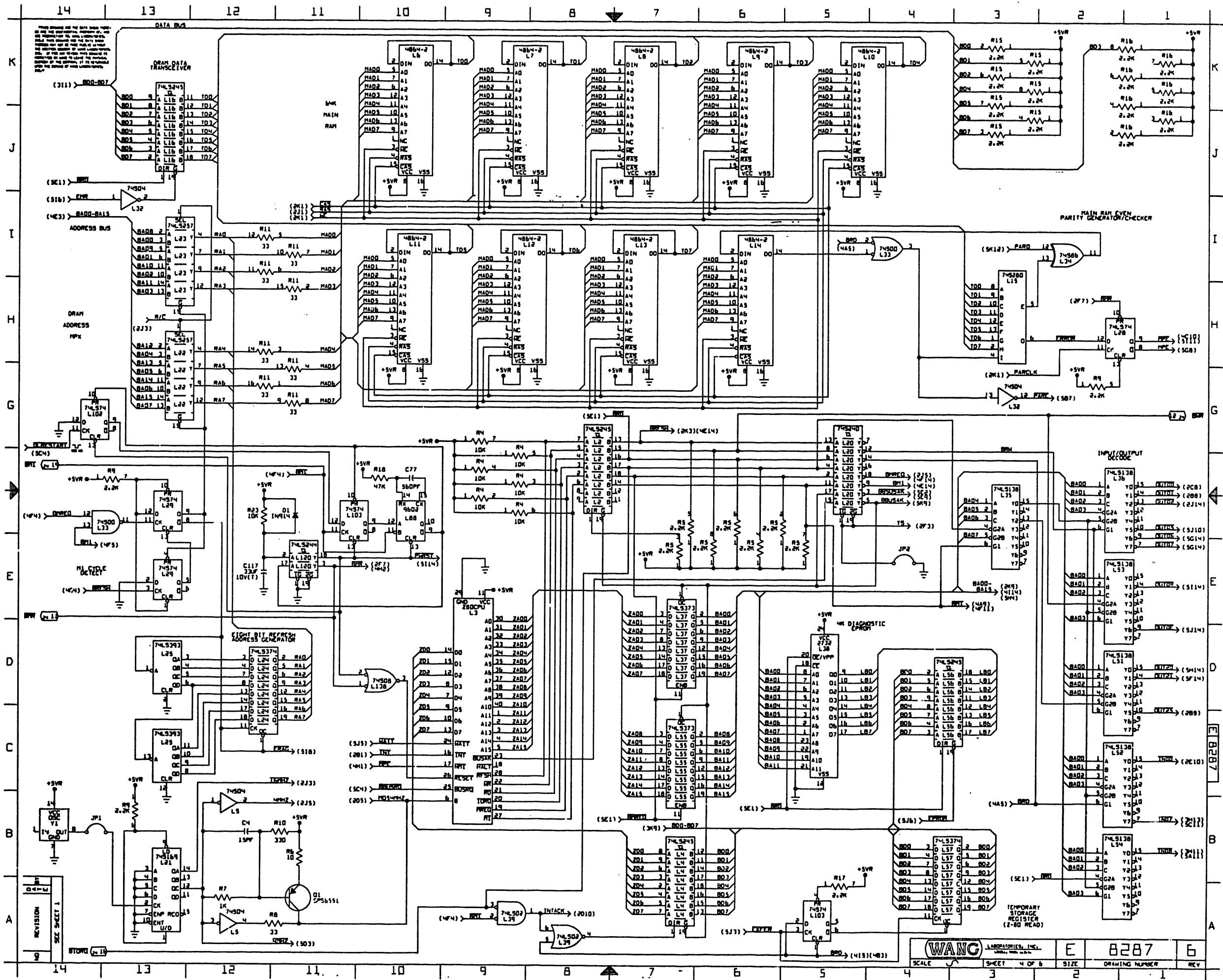
REV: 1



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REVISION	SEE SHEET 1
EXTINT	(4) 19

WANG LABORATORIES, INC.		E	8287	6
SCALE	SHEET 2 OF 6	SIZE	DRAWING NUMBER	REV



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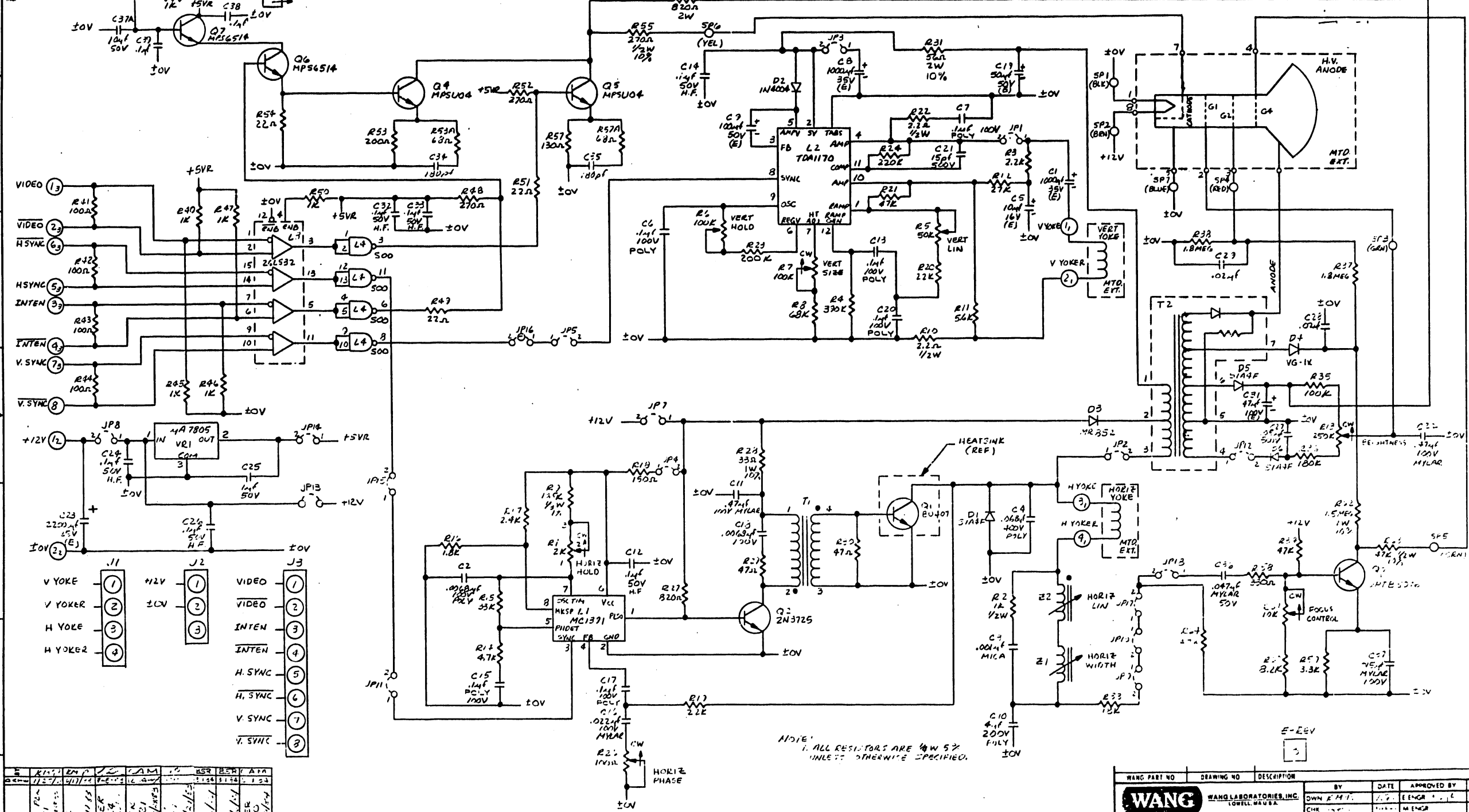
ITEM	I.C. LOCATION	TYPE	M.L. PART NO.	QTY
1	L1, L19	74LS175	376-0160	2
2	L2, L4, L16, L56, L62, L69, L84, L110, L111	74LS245	376-0285	9
3	L3	Z80ACPU	SEE CHART	1
4	L5, L32, L40, L81, L118	74504	376-0197	5
5	L6, L14	4804-2	377-0417	9
6	L13	745260	376-0246	1
7	L17, L18, L83, L117, L120, L135	74LS244	376-0288	6
8				
9	L20	745240	376-0334	1
10	L21	745169	376-0331	1
11	L22, L23, L60, L63, L77, L78, L112, L113	74LS257	376-0204	10
12	L24, L57-59, L66-68	74LS374	376-0286	7
13	L25, L141, L142	74LS393	376-0307	3
14	L26, L29, L86, L87, L103, L133	74574	376-0202	6
15	L27, L61, L138	74508	376-0200	3
16	L28, L70, L71, L102	74LS74	376-0155	4
17	L30, L91	745195	376-0427	2
18	L31, L33, L42, L76, L119, L131	74500	376-0228	6
19	L34, L45	74586	376-0271	2
20	L35, L36, L51-53, L99	74LS138	376-0294	7
21	L37, L55, L74	74LS373	376-0310	3
22	L38	2732A	SEE CHART	1
23	L39	74LS02	376-0208	1
24	L41, L90	74502	376-0199	2
25	L43, L81, L82, L92, L109, L134	SPARE5		
26	L44	74LS32	376-0211	1
27	L46-449, L93-98	8168-55	377-0476	10
28	L50	16LSA	377-3044	1
29	L64	16LSA	377-3043	1
30	L64, L79, L104, L139, L140	74LS169	376-0314	5
31	L72	8031	SEE CHART	1
32	L75	74LS279	376-0188	1
33	L80	825123	377-3048	1
34				
35	L85, L101	74532	376-0205	2
36	L88	9602	376-0104	1
37	L100	74LS125	376-0486	1
38				
39	L105	16R4A	377-3046	1
40	L106	74LS283	376-0332	1
41	L107	16R4A	377-3045	1
42	L108	74LS299	376-0303	1
43	L116	4L-2001	SEE CHART	1
44	L132	16R8A	377-3042	1
45	L136	75107	376-0146	1
46	L137	75113	376-0256	1
47	L143	745374	376-0305	1
48	L144	16R4A	377-3047	1
49	L145	26LS31	376-0470	1
50	L73	2732	SEE CHART	1

ITEM	LOCATION	TYPE	M.L. PART NO.	QTY
1	R1, R2, R4	10K	333-0809	3
2	R3	510 1/4W 5K	330-2032	1
3	R5, R9, R15, R17, R20	2.2K 51P	333-0806	6
4	R6, R25A	10 1/4W 5K	330-1011	2
5	R7, R26A	1K 1/4W 5K	330-3011	2
6	R8, R12, R14, R19A, R29C, R29D	33 1/4W 5K	330-1034	7
7	R10, R24A	330 1/4W 5K	330-2034	2
8	R11	33 DIP	333-0835	1
9	R17A	120 1/4W 5K	330-2013	1
10	R18	47K 1/4W 5K	330-4048	1
11	R19, R21	580 1/4W 5K	330-2069	3
12	R20A, R22, R27A	56 1/4W 5K	330-1057	3
13	R22, R23	10K 1/4W 5K	330-4011	2
14	R24	270 1/4W 5K	330-2028	1
15	R25	290 1/4W 5K	330-2040	1
16	R26	91 1/4W 5K	330-1092	1
17	R27	100 1/4W 5K	330-2011	1
18	R29, R31	2.2K 1/4W 5K	330-3023	3
19	R32	4.7K 1/4W 5K	330-3048	1
20	R33	47 1/4W 5K	330-1048	1
21				
22	C1, C3, C14-C29, C31-C34, C36, C37, C43-C51, C64-C70, C72-C76, C78-C81, C90, C95-C104, C108-C111, C113-C116, C118-C130, C134	.047UF 50V	300-1966	95
23	C2, C5-C13, C30, C38-C42, C62, C63, C83-C89, C112	.1UF 12V	300-1901	26
24	C4, 114A, 120A	15PF 500V	300-1015	3
25	C77	560PF 500V	300-1560	1
26	C91-C93	15UF 20V (T)	300-4022	3
27	C94	1UF 35V (T)	300-4000	1
28	C117	33UF 10V (T)	300-4024	1
29	C135	220PF 500V	300-5004	1
30				
31	D1	1W914A	380-1012	1
32	LED1	LED RED	370-0075	1
33				
34	J1	CONN BNC RTANG	350-3070	1
35	J2	CONN TNC RTANG	350-3071	1
36	J3	CONN RECEPT	350-0540	1
37	J4	CONN PC	350-0228	1
38	J5	CONN PC HOR	350-0210	1
39	J6	3 POS	350-0539	1
40	J7	8 POS	350-0542	1
41				
42	JP1, JP2, JP4-JP8	CONN HOR 2 POS PIN	350-0203	7
43	JP1, JP2, JP5, JP7, JP8	2 POS SHUNT	350-4506	5
44	Q1, Q2, Q3	SP56551	375-1050	3
45				
46	SH1, S42	SPST 8 POS	325-1503	2
47				
48	VR1	7R05	374-0002	1
49				
50	Y1	31.9488 MHz	321-1002	1
51	Y2	17.1 MHz	321-1006	1
52	Y3	19.2 MHz	321-1007	1
53				
54	L3, L72, L115	SKT 40 PIN	376-9011	3
55	Y1-Y3	SKT 14 PIN	376-9008	3
56				
57				
58				

REV	DATE	BY
1		
2		

SEE SHEET 1

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REV	DATE	BY	DESCRIPTION
1	11-23-64	WJG	ORIGINATED FOR DINA # 11-23-64
2	11-23-64	WJG	REVISED PER ECO # 11-23-64
3	11-23-64	WJG	REVISED PER ECO # 11-23-64
4	11-23-64	WJG	REVISED PER ECO # 11-23-64
5	11-23-64	WJG	REVISED PER ECO # 11-23-64
6	11-23-64	WJG	REVISED PER ECO # 11-23-64
7	11-23-64	WJG	REVISED PER ECO # 11-23-64
8	11-23-64	WJG	REVISED PER ECO # 11-23-64
9	11-23-64	WJG	REVISED PER ECO # 11-23-64
10	11-23-64	WJG	REVISED PER ECO # 11-23-64
11	11-23-64	WJG	REVISED PER ECO # 11-23-64

WANG PART NO	DRAWING NO	DESCRIPTION																
		MONITOR BOARD																
<table border="1"> <thead> <tr> <th>BY</th> <th>DATE</th> <th>APPROVED BY</th> <th>DATE</th> </tr> </thead> <tbody> <tr> <td>OWN E.M.T.</td> <td>11-23-64</td> <td>ENGR</td> <td>11-23-64</td> </tr> <tr> <td>CHK</td> <td></td> <td>M ENGR</td> <td></td> </tr> <tr> <td></td> <td></td> <td>MFG ENGR</td> <td></td> </tr> </tbody> </table>			BY	DATE	APPROVED BY	DATE	OWN E.M.T.	11-23-64	ENGR	11-23-64	CHK		M ENGR				MFG ENGR	
BY	DATE	APPROVED BY	DATE															
OWN E.M.T.	11-23-64	ENGR	11-23-64															
CHK		M ENGR																
		MFG ENGR																
<table border="1"> <thead> <tr> <th>MATERIAL</th> <th>MODEL NO</th> <th>TITLE</th> </tr> </thead> <tbody> <tr> <td></td> <td>11-23-64</td> <td>MONITOR BOARD</td> </tr> <tr> <td></td> <td></td> <td></td> </tr> </tbody> </table>			MATERIAL	MODEL NO	TITLE		11-23-64	MONITOR BOARD										
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	11-23-64	MONITOR BOARD																
<table border="1"> <thead> <tr> <th>FINISH</th> <th>TOL</th> <th>SCALE</th> </tr> </thead> <tbody> <tr> <td></td> <td>1/16" ± 0.0015"</td> <td>1/8" = 1"</td> </tr> </tbody> </table>			FINISH	TOL	SCALE		1/16" ± 0.0015"	1/8" = 1"										
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(FINAL BILL-OF-MATERIALS)

Table with columns: REF. DES., WANG PART NO., VALUE/TYPE, DESCRIPTION, DRAWING NO., QTY. Includes parts like CAP CERAMIC DISC, CAP CERAMIC MONO AXIAL LEADED, CAP POLYPROPYLENE FILM, etc.

BOARD NO. & TITLE: CB344 MONITOR BOARD SCHEMATIC REVISION (S): 07 SHEET OF PAGE 3

Table with columns: REF. DES., WANG PART NO., VALUE/TYPE, DESCRIPTION, DRAWING NO., QTY. Includes parts like RES VAR 100K OHM, IC REG 7805, TRANSFORMER, etc.

BOARD NO. & TITLE: CB344 MONITOR BOARD SCHEMATIC REVISION (S): 07 SHEET OF PAGE 2

Table with columns: REF. DES., WANG PART NO., VALUE/TYPE, DESCRIPTION, DRAWING NO., QTY. Includes parts like RES FIXED 1/4W 5%, RES FIXED METAL FILM, etc.

BOARD NO. & TITLE: CB344 MONITOR BOARD SCHEMATIC REVISION (S): 07 SHEET OF PAGE 4

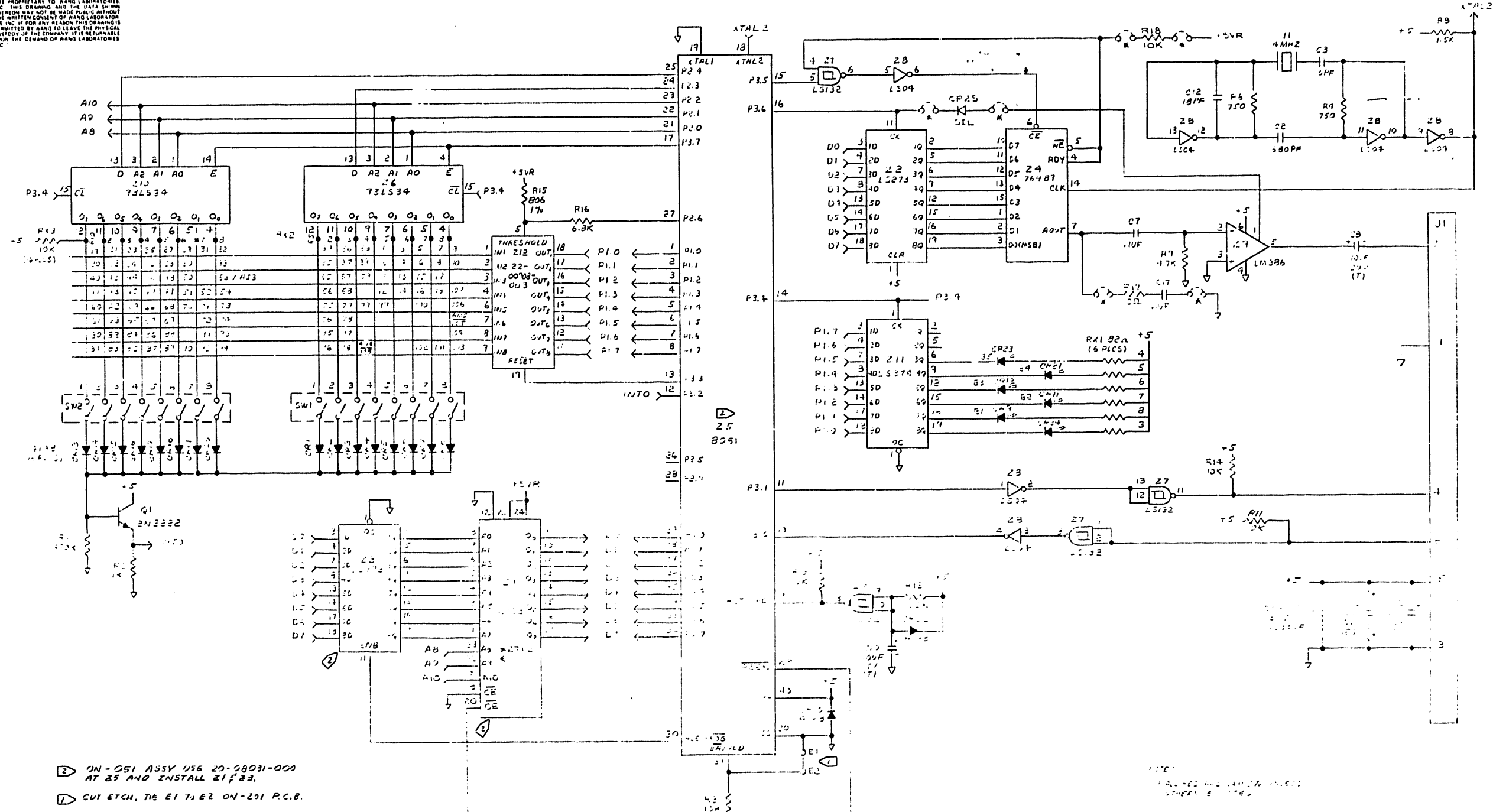
Table with columns: WANG PART NO., VALUE/TYPE, DESCRIPTION, DRAWING NO., QTY. Includes part 376-0228 IC QUAD 2-INPUT NAND GATE.

*** END-OF-REPORT ***

WANG LABORATORIES, INC. LOWELL, MA U.S.A. BY: DWN DATE: DATE APPROVED BY: E ENGR DATE: DATE. MATERIAL: MONITOR BOARD. FINISH: TOL EX AS NOTED. SCALE: SHT 2 OF 2. WANG PART NUMBER: 210-8344. SIZE: C. DRAWING NUMBER: 8344. REV: 7.

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DO NOT SCALE



- ② ON-051 ASSY USE 20-98031-000 AT 25 AND INSTALL 21F 23.
- ① CUT ETCH, TIE E1 TO E2 ON-291 P.C.B.

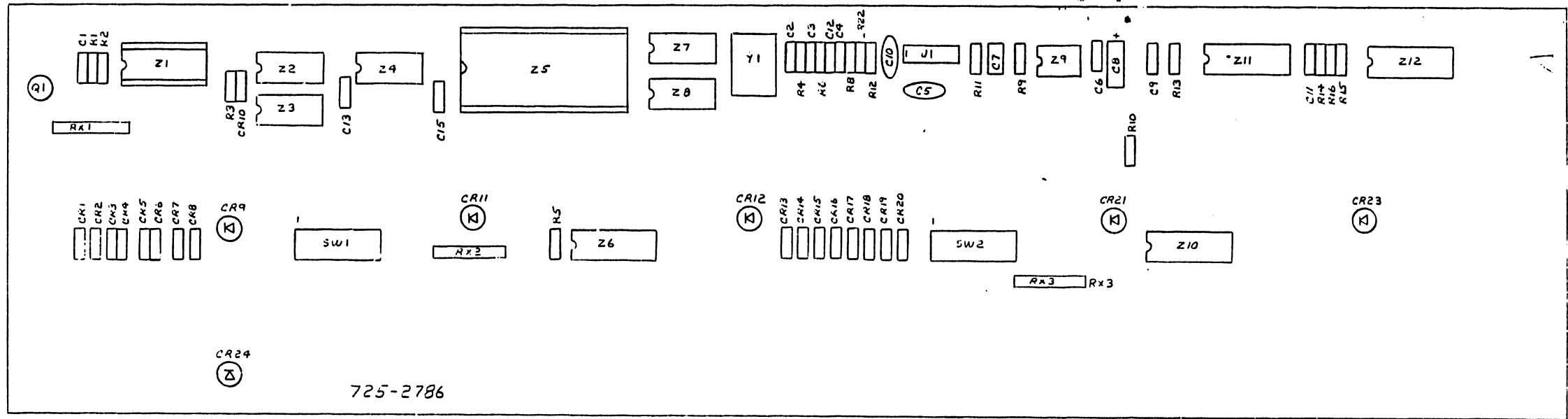
REV	NO	DATE	DESCRIPTION
0	1	11/21/74	OR. CHANGED PER DOW 11/21/74
1	1	11/21/74	REVISED PER APPROVED PER
2	1	11/21/74	REVISED PER APPROVED PER

WANG PART NO	DRAWING NO	DESCRIPTION	BY	DATE	APPROVED BY	DATE
WANG	WANG LABORATORIES, INC. LOWELL MA 01854		DWN	11/21/74	ENGR	
MATERIAL	MODEL NO	SEE IN ENG SPECIFICATIONS	CHK		M ENGR	
FINISH	TOL. EX. AS NOTED AR & DR FRAC. & 1/16" R&R & DR ANG. & 1/32" MIN	TITLE KEYBOARD			MFG ENGR	
SCALE	QTY 1 OF 2	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV	

77 11 10 9 8 7 5 4 3 2 1 22
 11 17 11 8.5 8.5 11 17 22
 G F E C B A
 22 17 11 8.5 8.5 11 17 22

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DO NOT SCALE



725-2786

COMPONENT	TYPE	W.L. PART NO.	COMPONENT	TYPE	W.L. PART NO.
Z1	2716	377-0398	C3	.05PF 500V	300-1410
Z2	74LS273	376-0302	C5,10	.1UF 35V(T)	300-4032
Z3	74LS373	376-0310	C7	.1UF 100V	300-1733
Z4	76487	376-0586	C8	.10UF 20V (T)	300-4063
Z5	8051	377-1000	C12	.180PF 50V	300-1769
Z6,10	73LS34	376-0173	C16	.001PF10V(T)	300-3112
Z7	74LS158	376-0173	CR1-8,10,13-20,22	11.4143	390-1014
Z8	74LS04	376-0140	CR7,11,12,21,23	LANP, RED	370-0031
Z9	LA1386	376-0585	CR7,11,12,21,23	SPACER RD	462-433
Z11	74LS374	376-0286	CR24	LED RED	370-0047
Z12	708	377-0447	CR25	SIL	380-1001
R1	470A 1/4W 5%	330-5048	C17	.1UF 12V	300-1701
R2	1K 1/4W 5%	330-1011	J1	6 PIN C/M/P	726-2457
R3,5,6,13,4,9	10K 1/4W 5%	330-7011	SW1,2	8 PGS DIP	325-1503
R4,6	150A 1/4W 5%	330-2076	Y1	4.00MHZ	331-0037
R8	1.5K 1/4W 5%	330-3216	Z1	24 PIN SKT	376-1003
R7	4.7K 1/4W 5%	330-3048	Z5	10 PIN SKT	376-7011
R12	100K 1/4W 5%	330-5011	Q1	2N2222	375-1005
R15	506A 1/4W 1%	333-0221			
R16	6.3K 1/4W 5%	330-3067			
RX1	B2A 51P	333-0850			
RX2,3	10K 51P	333-0827			
R17	.02 1/4W 5%	300-1011			
C1,4,6,7,11,13,15	.033UF 400V	300-2412			
C2	680PF	300-1452			

WANG PART NO.	DRAWING NO.	DESCRIPTION	BY	DATE	APPROVED BY	DATE
WANG	WANG LABORATORIES, INC. LOWELL, MASS.		DWNA	7-23	E ENGR	
			CHR		M ENGR	
					MFG ENGR	
MATERIAL	MODEL NO. 1067 FBC	TITLE	KEYBOARD PL. KIT			
FINISH	TOL. AS NOTED XX 2 DIA FRAG 2/164 XXX 2 DIA ANG 2/164 FROM W	725-2786	D	725-2786		
	SCALE 1/8" = 1"	WANG PART NUMBER	REV	DRAWING NUMBER	REV	

REV	DATE	DESCRIPTION
1		FILE SHIT 1

END