CUSTOMER ENGINEERING DIVISION

2200VS/8300

HARD/FLOPPY DISK DEVICE ADAPTER MANUAL

PRELIMINARY

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PREFACE
8300 BUS STRUCTURE

The 8300 System is a multiple processor system: The Central Processor (CP) is the master processor; the Input/Output Processors (IOPs) receive commands from the CP and control their attached peripheral devices. All processors (CP and IOPs) have the ability to access Main Memory by using the Main Memory bus (MMB). Processor requests for Main Memory operations are handled one at a time based on the high priority requesting processor at the start of each Main Memory cycle. A Main Memory operation consists of a transfer of one or two bytes between Main Memory and a processor.

A second bus, the Processor Communication Bus (PCB), allows the CP to send commands to any particular IOP. The PCB also provides an interrupt capability; after an IOP requests CP service, the CP can grant this pending interrupt request by using the PCB.

An IOP has one or more peripheral devices attached to it. The IOP performs control and data transfer operations involving these attached devices as directed by CP commands. CP commands are issued to a particular peripheral device; the command is performed by the IOP to which that device is attached. In general, an IOP has only one type of device attached to it. (This allows the IOP microprogram to be shared among the attached devices.)

The following conventions are used in this manual and schematics:

1. Each term is characterized by its logic active level-i.e.
   T01 = Time one active high (+3.8V)
   $\overline{\text{T01}}$ = Time one active low (0V to +.4V)

2. All logic device symbols reflect that devices stand-alone function not its function within a particular circuit.

3. Logic '1' = +3.8V = HIGH
   Logic '0' = 0V + .4V = LOW

4. The weight (binary) of bits within registers and busses is bit-0 being the most significant bit. The higher the bit number, the lower its value-i.e.

(MSB)	R0	R15	(LSB)
(MSB)	IC0	IC11	(LSB)

5a. All signals crossing an interface (DAI, DLI, PCBI) are active high +3.8V.

5b. All strobes crossing an interface are active low 0V +.4V.

NOTE:

These levels are recommended but not the rule. Any differences will be pointed out where they occur.

6a.  = Finger connections (bottom of board)

6b.  = Connector connections

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ICP DEVICE ADAPTER SUB-SYSTEM FOR HARD/FLOPPY DISK (7111 BOARD)

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IOP DEVICE ADAPTER SUB-SYSTEM OVERVIEW

DESCRIPTION:

The Device Adapter (DA) is that part of the Input/Output Processor (IOP) that adapts the peculiar requirements of a peripheral device to the requirements of the Microprocessor (MP) within the IOP.

GENERAL RELATIONSHIP:

The IOP exchanges information with the CP through main memory via a set of lines called the Main Memory Bus (MMB). The CP and the IOP engage in dialog via a set of lines called the Processor Communication Bus (PCB). The significance of these two sets of lines is qualified by two interfaces: the PCB interface (PCBI) and the MMB interface (MMBI). These two interfaces are integral components of the IOP as are the Device Level Interface (DLI) which qualifies signals between the devices and the IOP, and the Microprocessor (MP) which acts as the controller of these interfaces.

An IOP relieves the CP of the burden of communicating directly with I/O devices and permits data processing to proceed concurrently with I/O operations. An IOP provides the logical capabilities necessary to operate and control an I/O device. The IOP decodes the commands fetched from main memory and interprets them for the particular type of device.

Input/Output Devices

Input/Output devices provide external storage and a means of communication between data processing systems or between a system and its environment. Input/Output devices include such equipment as work-stations, magnetic tape units, disks, typewriter-keyboard devices, printers, and teleprocessing devices.

The WANG 8300 system is capable of connecting 8 input/output processors with each processor capable of connecting up to 16 I/O devices. (This configuration may be altered in future models.)

Each device has a one byte (8 bit) device address. All values from 00 to FF are legitimate device addresses. The priority of interrupt service is determined by the physical position of the IOP in the hardware configuration and not by the device address.

An 8-bit device address consists of an IOP portion and a device portion. The bit assignments are IOP dependent. The current IOP supports from four to sixteen devices; the high order four or six bits are therefore the IOP address and the low order two or four bits are the device address.*

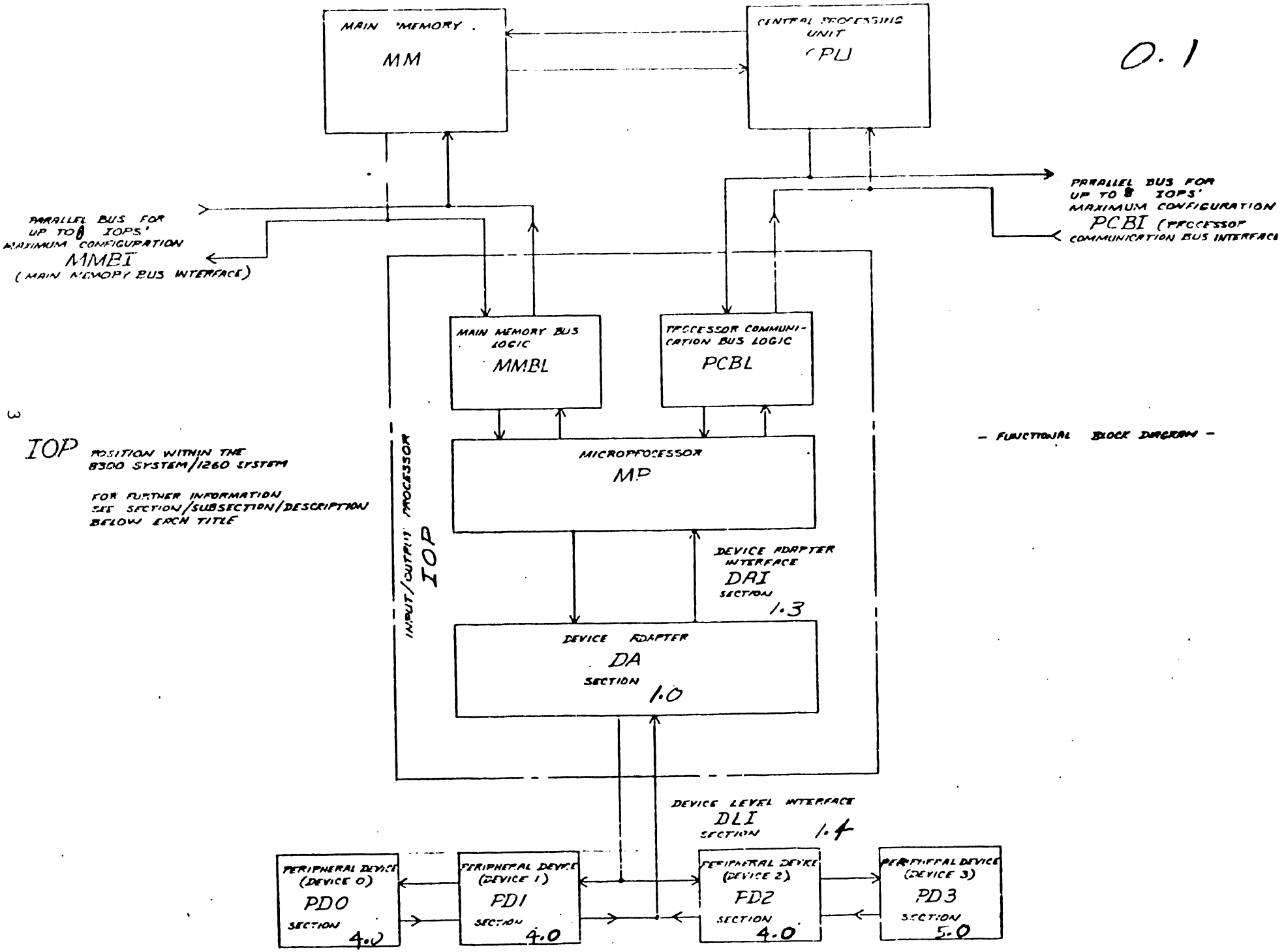
The following block diagram shows the functional relationship of major components within the IOP. The relationship of the IOP (shown inside of box) with Main Memory, CPU and the Peripheral Device(s), is via the MMBI, PCBI and DLI respectively.

The CPU converses with Main Memory via the MMBI as does each IOP. However, the block diagram shows a separate path to clarify the functional data path and control path of the 8300 system.

The device adapter (DA) contains hardware required to interface the peripheral device(s) to its controlling microprocessor. The DA resides in the same module as the MP but is part of the peripheral device's hardware. This module is referred to as the IOP and the peripheral device(s) as the IOP device(s).

For further description, operation and eventual hardware breakdown, refer to the section indicated below each title.

* IIII DDDD = 16 DEVICE IOP
IIIIII DD = 4 DEVICE IOP
I = IOP ADDRESS
D = DEVICE ADDRESS



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IOP POSITION WITHIN THE 8300 SYSTEM/1260 SYSTEM

FOR FURTHER INFORMATION SEE SECTION/SUBSECTION/DESCRIPTION BELOW EACH TITLE

– FUNCTIONAL BLOCK DIAGRAM –

- HARD/FLOPPY DISK DEVICE ADAPTER -
(210-7111 PC Board)

DESCRIPTION:

The Device Adapter converts the peculiar requirements of a particular peripheral device to the requirements of the Microprocessor portion of the 8300 IOP.

The Microprocessor commands the peripheral device, via the Device Adapter, and supplies various status associated with the peripheral and any other special information that might be required by the peripheral.

In the case of the Hard/Floppy Disk Device Adapter, the following tasks are performed by the Device Adapter:

A. DISK SELECTION - i.e., one of four possible disks is selected gaining access to the DLI port and made available for all data transfers and control information both to and from the microprocessor via the DLI and DAI.

1. This selection is a direct function of the MP's pointer register.

PT0	PT1		
0	0	=	SEL 0 (Hard Disk)
0	1	=	SEL 1 (Hard Disk)
1	0	=	SEL 2 (Hard Disk)
1	1	=	FLOPPY DISK SELECT

2. This select shifts the device adapter's internal operation of its clock to accomodate both the hard and floppy disk's different data rates.

B. INSTRUCTION DECODING - i.e., to determine what task is to be performed and the execution of that task satisfying the requirements of the disk and microprocessor/microprogram:

1 - Format
2 - Write
3 - Read
4 - Write/Verify
5 - Various Status Information
Transfers and Operations

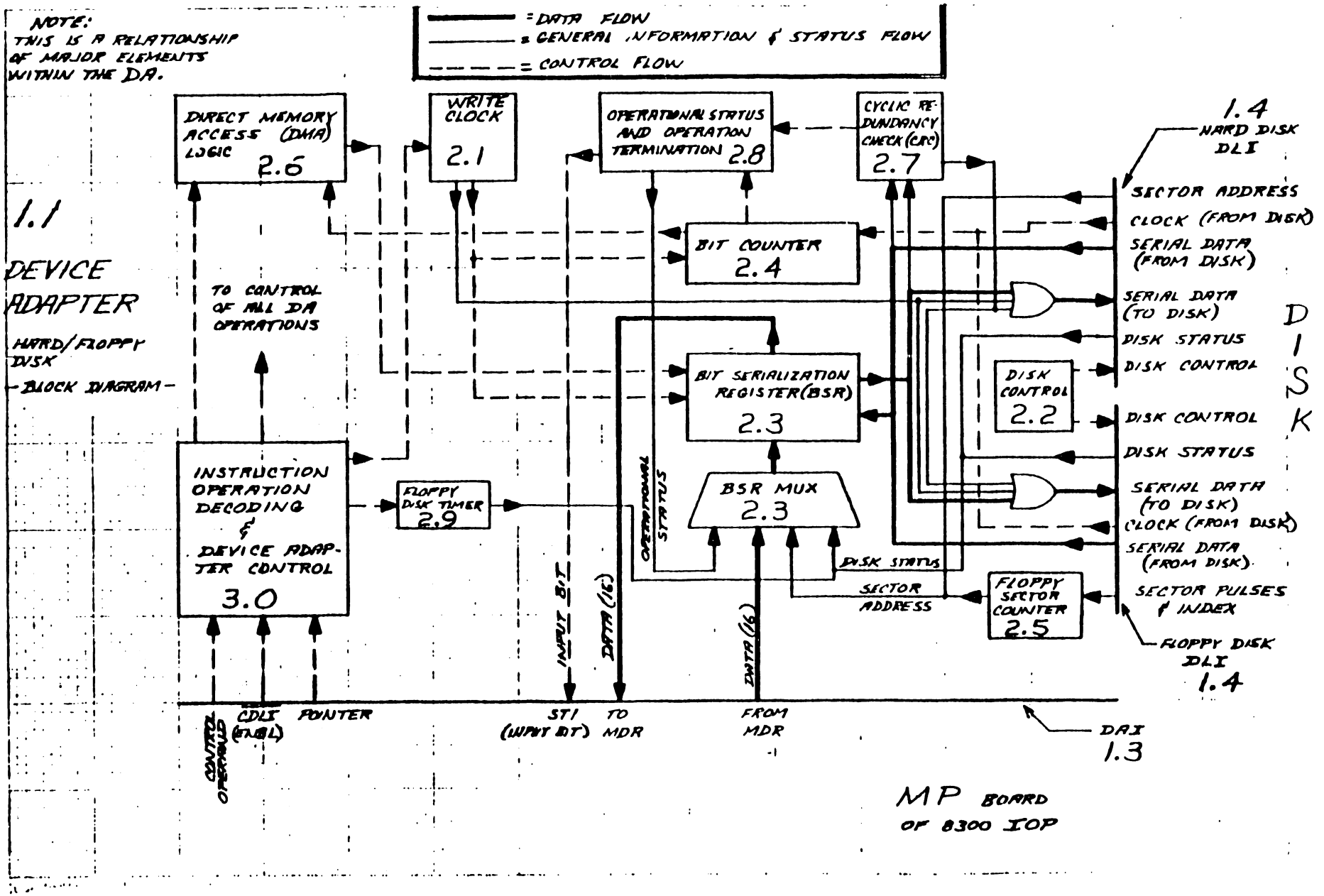
C. DIRECT MEMORY ACCESS (DMA) - i.e., the DA handles the actual main memory transfer by its hardware rather than the microprocessor by its Control Memory Bus Interface microinstruction ($\overline{\text{CMBI}}$). This results in a fast memory access required by the disk in order to read or write consecutive bytes.

1. There are 256 consecutive data bytes in each sector of the disk.

2. The microprocessor, after issuing the appropriate command to the device adapter, waits for the input bit to be set by the device adapter (signalling the end of the operation) before issuing any more commands to the device adapter.

The following block diagram shows the relationship between major elements within the Device Adapter.

For further description of each element, refer to the section indicated in each element block.


NOTE:
THIS IS A RELATIONSHIP OF MAJOR ELEMENTS WITHIN THE DA.
= DATA FLOW
= GENERAL INFORMATION & STATUS FLOW
= CONTROL FLOW
1.1
DEVICE ADAPTER
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POINTER
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TO MDR
FROM MDR
DAI
1.3
MP BOARD OF 8300 IOP

DEVICE ADAPTER
- DIABLO & SHUGART -

MNEMONIC LIST:

ACC & $\overline{\text{ACC}}$	=	Allow Cyclic Check
ACK & $\overline{\text{ACK}}$	=	'A' Clock
$\overline{\text{ADDR ACK}}$	=	Address Acknowledge
ADO	=	Allow DLI Instruction
APL	=	Allow Parallel Load
BCK & $\overline{\text{BCK}}$	=	'B' Clock
BSR	=	Bit Serialization Register
CCE	=	Cycle Check Error
$\overline{\text{CDLI}}$	=	Control Device Level Interface Microinstruction
CIS	=	Controller In Sync
CP	=	Central Processor
$\overline{\text{CSR}}$	=	Clear Serialization Register
DCE	=	Data Compare Error
DCP	=	Data Comparison
DDS	=	Disk Direction Stored
$\overline{\text{DLS}}$	=	Device Level Select
DOS	=	Data Order Stored
$\overline{\text{DSMH}}$	=	Device Strobe MDRH
$\overline{\text{DSML}}$	=	Device Strobe MDRL
DSO & $\overline{\text{DSO}}$	=	Disk Strobe Out
DO (MSB) $\leftrightarrow$ D15 (LSB)	=	Data to MP Board MDRH & MDRL Input Multiplexers
$\overline{\text{EOF}}$	=	End of Format
EOR	=	End of Read
$\overline{\text{EOW}}$	=	End of Write
FCS	=	Format Command Stored
$\overline{\text{FDP}}$	=	Floppy Disk Pointer
FIR & $\overline{\text{FIR}}$	=	File Inoperable Reset
$\overline{\text{FMC}}$	=	Format Command
$\overline{\text{FRN}}$	=	File Ready
$\overline{\text{HPS}}$	=	Head Position Select

$\overline{\text{HR16}}$ = Hardware Read 16

$\overline{\text{HTS}}$ = Hardware Transfer Stop

$\overline{\text{HW16}}$ = Hardware Write 16

$\overline{\text{INC2}}$ = Second Increment Pulse to MAR

$\overline{\text{INITE}}$ = Latched Initialize

$\overline{\text{INIT2}}$ = Initialize

IOP = Input/Output Processor

$\overline{\text{ISS}}$ = Inhibit Serialization (Reg.) Shift

IWC = Increment Write Clock

$\overline{\text{LAI}}$ = Logical Address Interlock

$\overline{\text{LIS}}$ = Load In Status

$\overline{\text{LSR}}$ = Load Serialization Register

$\overline{\text{LTZ}}$ = Load Track Zero

MDH0 (MSB) ↔ MDH7 (LSB) = Memory Address Register High

MDL0 (MSB) ↔ MDL7 (LSB) = Memory Address Register Low

MM = Main Memory

MP = Microprocessor

MXA = BSR Multiplexer Select 'A'

MXB = BSR Multiplexer Select 'B'

PT0 (MSB) ↔ PT1 (LSB) = Pointer Register Bits

RCS & $\overline{\text{RCS}}$ = Read Command Stored

$\overline{\text{RDC}}$ = Read Command

RDI & $\overline{\text{RDI}}$ = Read Data In

$\overline{\text{RFD}}$ = Resync For Data

RGA = Read Gate Allow

$\overline{\text{ROS}}$ = Reset Operational Status

$\overline{\text{RSA}}$ = Resync Allow

$\overline{\text{RST}}$ = Restore

$\overline{\text{RTS}}$ = Ready To Seek

$\overline{\text{RVC}}$ = Read & Verify Command

SCA = Strobe Cylinder Address

SCD = Sync Character Detected

SDD & $\overline{\text{SDD}}$ = Strobe Disk Direction (Step In/Out)

SDI = Serial Data In

SDO = Serial Data Out

SDP = Select Disk Platter

SDR = Shift During Read

$\overline{\text{SEL 0}}$ = Pointer to Drive #0

$\overline{\text{SEL 1}}$	=	Pointer to Drive #1
$\overline{\text{SEL 2}}$	=	Pointer to Drive #2
SHC & $\overline{\text{SHC}}$	=	Strobe Header Check
SHP & $\overline{\text{SHP}}$	=	Strobe Head Position (Up/Down)
$\overline{\text{SHW}}$	=	Set Write Request
SIE	=	Seek Incomplete
SINPT & $\overline{\text{SINPT}}$	=	Set Input Bit
SIS	=	Step Into Sixteen
$\overline{\text{SOP}}$	=	Surface Operation
SOS	=	Step Out of Sixteen
$\overline{\text{SPP}}$	=	Sector Pulse Present
$\overline{\text{SRR}}$	=	Set Read Request
$\overline{\text{SRT}}$	=	Start Read Termination
SSR	=	Shift Serialization Register
$\overline{\text{STG}}$	=	Shorten The Gap
$\overline{\text{STP}}$	=	Step-Floppy
$\overline{\text{S1}}$ (MSB) $\leftrightarrow$ $\overline{\text{S5}}$ (LSB)	=	Sector Address from Disk
$\overline{\text{TA0}}$ (MSB) $\leftrightarrow$ $\overline{\text{TA8}}$ (LSB)	=	Track Address Bits (Cylinder)
TIS	=	Time In Sync
T02, T04, T06	=	Subcycle Times (MP)
ULH	=	Upper-Lower Head
$\overline{\text{WCE}}$	=	Write Check/File Inoperative
$\overline{\text{WDC}}$	=	Write Data Command
WGT	=	Write Gate Time
WMR	=	Write Memory Request
$\overline{\text{WPT}}$	=	Write Protect
WTG & $\overline{\text{WTG}}$	=	Write The Gap

- DEVICE ADAPTER INTERFACE (DAI) -

The Device Adapter Interface is that set of interconnecting lines between the Microprocessor and the Device Adapter.

The following is a description of DAI terms and their pin assignments peculiar to the Hard/Floppy Disk Device Adapter sub-system. For a complete list of the DAI terms, see the 8300 MP Manual.

MDRH (MDH0 ↔ MDH7) & MDRL (MDL0 ↔ MDL7) LINES - MP TO DEVICE

These sixteen lines come from the microprocessor and are direct outputs from the MDR (Memory Data Register). Since the microprocessor is utilizing the MDR for its operations, the information across these lines can only be considered valid when the appropriate strobe and command is sent from the controller to the peripheral device. In addition, these lines may also be used to pass commands, (bits within the MDR) to the Device Adapter in conjunction with the microprocessor CDLI command.

DATA (D0-D15) LINES - DEVICE TO MP

These sixteen lines come from the Device Adapter and are utilized to pass data and status back to the microprocessor. These lines are used in conjunction with the SELECT MDR, STROBE MDRH and STROBE MDRL lines. These lines must have the same truth as the bits required in the MDR.

NOTE:

(D0-D7) = MDRH (D8-D15) = MDRL

CONTROL OPERAND OF CDLI INSTRUCTIONS (R5-R15)

These eleven lines come from the microprocessor and signal the Device Adapter as to the operation it is requested to perform. The usage of these bits varies from one machine to another and will be specific to the device type to be connected. These lines may be bit significant or binary coded.

If the instruction is transferred to the Device Adapter via the MDR register(s), the control operand of the CDLI instruction will remain undefined.

CDLI LINE ($\overline{CDLI}$)

This line, (active low) is valid from T02 (CLOCK TIME 2) throughout the execution of the microinstruction and is present when the microcode issues a command to the D.A. At this time, the D.A. electronics can interpret its instruction from either the eleven instruction lines or via the output lines from the MDR. The method used for implementation can be made by the hardware designer and the microprogrammer at the time of the design conception.

POINTER LINES (PT0 AND PT1)

These two lines come from the microprocessor and indicate to the device electronics the peripheral port which is of interest to the microprocessor.

T02-T04-T06

These lines come from the microprocessor and are the timing signals associated with microinstructions coming across the Device Adapter Interface.

SELECT MDR ($\overline{DLS}$)

This line is generated by hardware within the Device Adapter. When the D.A. electronics is required to put data or status into the MDR (under command of the microprocessor), this line must be brought low. At some time later, the appropriate MDR segment (either MDRH or MDRL) must be strobed.

STROBE MDRH (DSMH), MDRL (DSML)

These two lines are under control of the D.A. electronics. When data or status is loaded into the MDR, and at sometime after the MDR selection, the appropriate MDR strobe will be made.

INPUT RESPONSE (SINPT)

This line is generated within the Device Adapter. This line is used to set the INPUT bit in the microprocessor, thereby indicating a response from a device operation. The microcode within the microprocessor tests this bit periodically for a device response. The purpose of this bit is to allow for asynchronous operations within the peripheral device to become synchronous with the microprocessor. The minimum pulse width for this signal is 25 nanoseconds.

INITIALIZE (INIT2)

This line will be 0 volts during power-up time for 50 microseconds, then changes to +3.8 volts. An active low pulse of 50 microseconds will also be generated via the prime button.

HARDWARE WRITE SIXTEEN (HW16)

This line must be held at +3.8V when not in use. When this line is brought to 0 volts, the memory controller takes in the contents of the MDR.

HARDWARE READ SIXTEEN HR16)

This line must be held at +3.8V when not in use. When this line is brought to 0 volts, the memory controller loads the data from the main memory into the MDR.

HARDWARE STATUS BIT 1 (HSB1)

This line will be 0 volts normally and will go to +3.8V when a memory parity error occurs. This bit will become a status bit in the operational status byte.

HARDWARE STATUS BIT 2 (HSB2)

This line will be 0 volts normally and will go to +3.8V when an illegal address has been sensed by the memory controller. This bit will become a status bit in the operational status byte.

HARDWARE TRANSFER STOP ($\overline{HTS}$)

This line will be +3.8V normally and will go to 0 volts when either illegal address or parity error is detected. During a direct transfer, a 0 volt on this line will cause an immediate termination of the direct transfer operation.

RESET OPERATIONAL STATUS ($\overline{ROS}$)

This line is normally at +3.8V. A 0 volt level on this line causes hardware status bits 1 and 2 to be reset.

MAR INCREMENT ($\overline{INC2}$)

This line is normally +3.8V. When this line goes to 0V and then back to +3.8V, the memory address counter is incremented for the second time during the current MEMORY OPERATION.

SYSTEM INITIALIZE

This line is normally +3.8V. When this line goes to 0V, it indicates a master reset (power-on) from the system. This line will also go to 0V whenever the power supply voltages become out of tolerance.

DMI PIN ASSIGNMENT

DIRECT MEMORY ACCESS

SIGNAL NAME	PIN NO.
$\overline{HTS}$	3_4
HSB1	4_4
HSB2	5_4
$\overline{HW16}$	1_4
$\overline{HR16}$	2_4

MISCELLANEOUS SIGNALS

SIGNAL NAME	PIN NO.
SYSTEM INITIALIZE	13_1

MISCELLANEOUS SIGNALS

SIGNAL NAME	PIN NO.
MARH (MSB)	
MARM	
MARL (LSB)	
INC2	N_4

DAI PIN ASSIGNMENT

SIGNAL NAME		PIN NO.
MDH0	(MSB)	1_3
MDH1		15_2
MDH2		14_2
MDH3		13_2
MDH4		12_2
MDH5		11_2
MDH6		10_2
MDH7	(LSB)	9_2
MDL0	(MSB)	8_2
MDL1		7_2
MDL2		6_2
MDL3		5_2
MDL4		4_2
MDL5		3_2
MDL6		2_2
MDL7	(LSB)	1_2
R5	(MSB)	N_3
R6		M_3
R7		L_3
R8		K_3
R9		J_3
R10		H_3
R11		F_3
R12		E_3
R13		D_3
R14		C_3
R15	(LSB)	B_3
MOF		2_3
$\overline{TOS}$	(PULL UP TO +5V WHEN LOADED)	4_3
$\overline{CMI}$		10_3
PT0	(MSB)	8_3
PT1	(LSB)	9_3
TO2		P_3
TO4		S_3
TO6		15_3

CONTROL OPERAND

SIGNAL NAME		PIN NO.
D0	(MSB)	A_3
D1		S_2
D2		R_2
D3		P_2
D4		N_2
D5		M_2
D6		L_2
D7		K_2
D8		J_2
D9		H_2
D10		F_2
D11		E_2
D12		D_2
D13		C_2
D14		B_2
D15	(LSB)	A_2
$\overline{DLS}$		R_3
$\overline{DSMH}$		14_3
$\overline{DSML}$		13_3
$\overline{SINPT}$		12_3
$\overline{INIT2}$	(32 MA LOW)	11_3
+5VR		$B_1 - Z_1$ $R_4 - 14_4$
±0V		$7_3 - 6_3$ $C_1 - 3_1$ $P_4 - 13_4$
-5VR		15_4
+12VR		S_4

MDH

MDRL

- DEVICE LEVEL INTERFACE (DLI) -

The Device Level Interface consists of three connectors. Two connectors are used for connection to the first 10 megabyte hard disk. One or two more hard disk(s) can be attached in a daisy chain configuration - i.e., the second hard disk can be attached to the first, and the third hard disk can be attached to the second disk.

1. The last hard disk must be terminated. If only one hard disk is used, it must be terminated.

2. Connectors number one and two are used for the hard disk DLI:

= Connector No. 1 (J1)
= Connector No. 2 (J2)

The floppy disk has its own connector on the device adapter. Only one floppy disk can be attached - i.e., no daisy chain configuration of floppy disks is allowed.

1. The floppy disk DLI, for the most part, is in a parallel configuration with the DLI for the hard disk and uses the terminator block physically mounted on the hard disk. Those signals peculiar to the floppy disk only are terminated within the floppy disk.

, A single or multiple (up to 3 max.) hard disk configuration may appear without a floppy disk, OR A FLOPPY WITHOUT HARD DISKS, OR ANY COMBINATION FLOPPY AND HARD DISKS.

2. The connector with no subscript is used for the floppy disk DLI:

= Connector for the Floppy Disk

The following Device Level Interface description is broken into two parts. The first is the DLI for the Hard Disk(s) and the second is the DLI for the Floppy Disk:

- SIGNAL DESCRIPTION -

(HARD DISK)

- LINES TO THE DISK DRIVE -

UNIT SELECT LINES ($\overline{SEL0}$, $\overline{SEL1}$, $\overline{SEL2}$)

There are three unit select lines going out of the interface port. They are used to select one of the three possible drives in the daisy chain configuration. A value of '0' in one of these lines selects the corresponding unit. The selected drive has access to the interface port and all signals to and from the interface apply to this drive.

DISK SELECT (SDP)

This line selects the removable or the fixed cartridge. A '0' selects the removable cartridge; a '1' selects the fixed cartridge.

HEAD SELECT (ULH)

This line selects the upper or lower head of the selected cartridge. A '0' selects the upper surface head; a '1' selects the lower surface head.

TRACK ADDRESS ($\overline{TA0}$(MSB) ↔ $\overline{TA8}$(LSB))

These 9 lines active low (0V, .4V), are used to specify a cylinder address where the heads are to be moved. These lines are strobed with the strobe line and stored in an internal address register (disk drive).

DISK STROBE OUT ($\overline{DSO}$)

This line is used to enable the track address and the restore lines. This line is made '0' when the appropriate signal lines have settled and must be held until at least the leading edge of the address acknowledge signal is detected.

RESTORE ($\overline{RST}$)

This line is used to position the heads at cylinder 0. After completion of this command the heads are located over cylinder 0, and the seek incomplete condition is reset. This signal is active low (0V, .4V). This line must have settled before the application of $\overline{DSO}$.

WRITE GATE ($\overline{WRITE\ GATE}$)

This line turns on the write current in the selected head. The signal must be applied at least 2 μsec prior to writing the first flux transition, and held for the entire duration of the write operation. This signal is active low (0V, .4V).

**ERASE GATE ($\overline{ERASE\ GATE}$)*

This line turns on the erase current in the selected head. There is no built in delay of erase current. This signal is active low (0V, .4V).

WRITE DATA AND CLOCK ($\overline{WRITE\ DATA}$)

This line accepts multiplexed data and clock pulses for double frequency or phase encoding type recording. Pulses must have a minimum width of 100 nanoseconds. Leading edges must have a transition time of not more than 50 nanoseconds. Pulses are active low (0V, .4V).

READ GATE ($\overline{READ\ GATE}$)

This line enables the read clock and read data output lines. The read gate must be held active during the entire read operation. This signal is active low (0V, .4V).

*Erase Gate causes a "trim" erase of the data track. The hard disk does not have erasing of the entire track capability. The "trim" erase limits the width of a track by erasing all signals that are wider than the specified track width. (See Diablo Series 40 Maintenance Manual.)

— LINES FROM THE DISK DRIVE —

FILE READY ($\overline{FRN}$)

A '0' on this line indicates that all the following conditions are met (normal operation):

- Power On
- Dust Cover Loaded*
- Equipment Drawer Closed
- LOAD/RUN Switch In RUN Position
- Start Up Cycle Complete
- Write Check False
- File Select True

READY TO SEEK ($\overline{RTS}$)

A '0' on this line indicates that the drive is in the file ready condition and is not in the process of executing a seek operation. Following a seek command to a valid address (other than the present address), or a restore command, this line will go to '1' within 1 μsec after detecting the leading edge of the strobe signal. The return of the line to '0' indicates that the seek or restore operation has been completed. This line does not change when the present cylinder is addressed.

ADDRESS ACKNOWLEDGE ($\overline{ADDR\ ACK}$)

A '0' on this line indicates that a command to move the heads has been accepted and that execution of the command has started. An address acknowledge is issued 500 nanoseconds after the leading edge of the strobe is detected even if there is no change in the address. This signal is a 1 μsec pulse. The pulse will not be issued if a logical address interlock condition is detected.

*On the Diablo Series 40 Disk Drive, the removable disk platter need not be installed, just the dust cover, to obtain a file ready condition.

LOGICAL ADDRESS INTERLOCK (LAI)

A '0' on this line indicates that a track address greater than 407 has been received and that the command is not executable. The seek command is suppressed. This line is reset ('1') with the next valid address acknowledge or with the restore command.

SEEK INCOMPLETE ($\overline{SIE}$)

A '0' on this line indicates that a malfunction has caused an incomplete seek operation. This value will be maintained until a restore command has been received and executed by the disk drive.

SECTOR MARK ($\overline{SPP}$)

A '0' on this line indicates that a sector slot passes by the transducer. This line is pulsed for 40 μsec when this condition arises (24 times per revolution).

SECTOR ADDRESS ($\overline{S1}$(MSB) ↔ $\overline{S5}$(LSB))

These 5 lines define the sector address under the read/write heads. The selected address counter is advanced by the leading edge of the sector mark and is reset to zero by the leading edge of sector mark following the index mark. The value of the sector counter is not considered valid for the duration of the sector mark pulse. These lines are active low (0V, .4V).

READ CLOCK ($\overline{READ\ CLOCK}$)

This line provides clock pulses which have been separated from the data signals during reading. Pulse width is nominally 100 nanoseconds, with a minimum of 50 nanoseconds and a maximum of 150 nanoseconds. The negative going edge must be used for reference. This pulse is active low (0V, .4V).

READ DATA ($\overline{\text{READ DATA}}$)

This line is used for output data signals which have been separated from clock signals during reading. Pulse width is nominally 100 nanoseconds, with a minimum of 50 nanoseconds and a maximum of 150 nanoseconds. The negative going edge of this signal must be used for reference. This pulse is active low (0V, .4V).

WRITE CHECK ($\overline{\text{WCE}}$)

A '0' on this line indicates that one or more of the following conditions exist:

- Write current without a true write gate line
- Write and select on both heads
- Erase current without a true erase gate line
- Erase gate line true without erase current
- Significant voltage drop

All external commands are suppressed. This line is reset by either adjusting the voltage or by turning the LOAD/RUN switch to LOAD and back to RUN.

DLI (HARD DISK)

- PIN ASSIGNMENT -

SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.
$\overline{SEL\ 0}$	43_2	$\overline{FRN}$	43_1
$\overline{SEL\ 1}$	44_2	$\overline{RTS}$	38_1
$\overline{SEL\ 2}$	45_2	$\overline{ADDR\ ACK}$	47_2
SDP	31_2	$\overline{LAI}$	44_1
ULH	27_2	$\overline{SIE}$	37_1
$\overline{TA0}$ (MSB)	39_1	$\overline{SPP}$	29_1
$\overline{TA1}$	29_2	$\overline{S1}$ (MSB)	45_1
$\overline{TA2}$	48_1	$\overline{S2}$	33_1
$\overline{TA3}$	47_1	$\overline{S3}$	35_1
$\overline{TA4}$	49_1	$\overline{S4}$	36_1
$\overline{TA5}$	41_1	$\overline{S5}$ (LSB)	34_1
$\overline{TA6}$	40_1	$\overline{READ\ CLOCK}$	28_1
$\overline{TA7}$	46_1	$\overline{READ\ DATA}$	30_1
$\overline{TA8}$ (LSB)	42_1	$\overline{WCE}$	32_1
$\overline{DSO}$	36_2		
$\overline{RST}$	37_2		
$\overline{WRITE\ GATE}$	39_2		
$\overline{ERASE\ GATE}$	40_2		
$\overline{WRITE\ DATA}$	27_1		
$\overline{READ\ GATE}$	31_1		
+5V (FOR TERMINATOR)	48_2 & 49_2		

TO DISK DRIVE

FROM DISK DRIVE

NOTE:
PINS 1 TROUGH 25 OF BOTH CONNECTORS (J1 & J2) ARE CONNECTED TO ± 0V.

- SIGNAL DESCRIPTION -

(FLOPPY DISK)

- LINES TO THE DISK DRIVE -

FLOPPY DISK SELECT ($\overline{FDS}$)

This signal active low (0V, .4V) selects the floppy disk drive for access to the Device Level Interface port and all signals to and from the interface apply to this drive.

DIRECTION SELECT ($\overline{DDS}$)

This interface signal defines the direction of motion of the R/W head when the Step line is pulsed. A logical one level defines the direction as out and if a pulse is applied to the Step line the R/W head will move away from the center of the disk. Conversely, if this input is a logical zero level is applied the direction of motion is defined as in and if a pulse is applied to the Step line the R/W head will move towards the center of the disk.

STEP ($\overline{STP}$)

This interface line is a control signal which causes the R/W head to move with the direction of motion defined by the Direction Select line. The access motion is initiated on each logical zero to logical one transition of this signal.

HEAD LOAD (HPS)

This interface line performs two functions. One function is to remove the 24 volts from the stepper motor which will allow the motor to run cooler. This means that in order to step, the Head Load line must be a logical 0 level. It also is a control signal to an actuator that allows the disk to be moved into contact with the R/W head before a Read/Write operation. A logical one deactivates the head load actuator and causes a bail to lift the pressure pad from the disk, which removes

the load from the disk and R/W head. A logical zero level on this signal activates the head load actuator and allows the pressure pad to bring the disk into contact with the R/W head with the proper contact pressure.

FILE INOPERABLE RESET ($\overline{FIR}$)

This interface line provides a direct reset on the File Inoperable latch. The inactive level for this signal is a logical one. The File Inoperable condition is reset with a logical zero level applied to this line.

NOTE:

Under no circumstances should the drive be operated with this signal at a constant logical zero level since all data safety circuitry will be defeated.

WRITE GATE ($\overline{WRITE\ GATE}$)

Write Gate is an interface line which controls the writing of data on the disk. A logical one level on this interface line turns off the current source to the write drivers along with the current sinks for the write current. A logical zero level on this line enables the write current source and current sinks, and disables the stepping circuitry.

WRITE DATA ($\overline{WRITE\ DATA}$)

This interface line provides the data to be written on the disk and each transition from the logical one level to logical zero level causes the current through the R/W head to be reversed. Input impedance for Write Data = 100Ω.

— — LINES FROM THE DISK DRIVE —

INDEX ($\overline{INDEX}$)

This interface signal is provided by the disk drive once each revolution (166.67 ms) to indicate the beginning of the track. Normally,

this signal is a logical one level and makes the transition to the logical zero level for a period of .4 ms once each revolution.

TRACK 00 ($\overline{LTZ}$)

The Track 00 interface signal indicates when the R/W head is positioned at track zero (the outer most data track) and the access circuitry is driving current through phase one of the stepping motor (Head Load signal true). This signal is at a logical one level when the R/W head is not at track zero and is at a logical zero level when the R/W head is at track zero.

FILE INOPERABLE ($\overline{WCE}$)

File Inoperable is the output of the data safety circuitry and is at a logical zero level when a condition which jeopardizes data integrity has occurred.

File Inoperable = (Write Gate $\overline{\text{Write I Sense}}$)
+(Write Gate Write I Sense)
+(Write Gate $\overline{\text{Head Load}}$)
+(Write Gate $\overline{\text{Write Data}}$)
+(Write Gate $\overline{\text{Door Closed}}$)

SECTOR ($\overline{SECTOR}$)

This interface signal is provided by the disk drive 32 times each revolution. Normally, this signal is a logical one level and makes the transition to the logical zero level for a period of .4 ms 32 times each revolution (32 sectors).

WRITE PROTECT ($\overline{WPT}$)

This interface signal is provided by the disk drive to allow the user an indication when a write protected diskette is installed. The signal is a logical one level when the diskette is not protected and a logical zero when it is protected.

SEPARATED DATA ($\overline{\text{READ DATA}}$)

Separated Data is the interface line over which read data is sent to the using system. The frequency modulated signal written on the disk is demodulated by the drive electronics and the data pulses are sent to the using system over this interface line. Normally, this signal is a logical one level and each data bit recorded on the disk causes a transition to the logical zero level for 200 ns.

SEPARATED CLOCK ($\overline{\text{READ CLOCK}}$)

The Separated Clock interface line provides the using system the clock bits recorded on the disk in frequency modulation recording. The levels and timing are identical to the Separated Data line except that a separated clock pulse occurs each 4µs, instead of in multiples of 4µs.

READY ($\overline{\text{FRN}}$)

This interface signal is provided to indicate to the user that a diskette is installed properly, the door is closed, and that two index or sector pulses have been detected (diskette is turning). This signal is at a logical one level when not ready and is at a logical zero level when ready.

DLI (FLOPPY DISK)
- PIN ASSIGNMENT -

SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.
$\overline{FDS}$	23	$\overline{INDEX}$	15
DDS	5	$\overline{LTZ}$	25
$\overline{STP}$	3	$\overline{WCE}$	29
HPS	21	$\overline{SECTOR}$	19
$\overline{FIR}$	1	$\overline{WPT}$	17
$\overline{WRITE\ GATE}$	7	$\overline{READ\ DATA}$	13
$\overline{WRITE\ DATA}$	9	$\overline{READ\ CLOCK}$	11
		$\overline{FRN}$	27

TO DISK DRIVE

FROM DISK DRIVE

NOTE:

EVEN PINS 2 THROUGH 26 ARE CONNECTED TO ±0V.

- OPERATIONAL SPECIFICATION -

This section contains the operational specifications for the three 10 Megabyte Hard Disks and the 3.1 Megabit Floppy Disk controlled by the Device Adapter.

- HARD DISK - 100 MEGABIT (10 MEGABYTE -)

GENERAL DESCRIPTION:

* The Diablo Series 40 Disk Drive Model 44 is presently being used. It uses both a fixed disk and a removable top loading disk cartridge, for a capacity of 100 megabits of data at a recording density of 2200 Bits Per Inch (BPI) and an average access time of 38 milliseconds. Each disk has an upper and lower surface of 408 tracks each with a lateral track density of 200 Tracks Per Inch (TPI), giving the disk 408 cylinders of 4 tracks each. There are 24 sectors per track yielding a total of 39,168 sectors, with 256 (8-bit) bytes of usable data per sector.

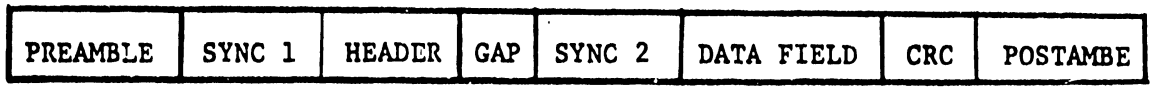
NOTE:

Hard Disk is the general terminology given to a disk system where the Read/Write head(s) do not make physical contact with the recording media. This recording media is of a close tolerance unflexable material.

*See Diablo Systems Incorporated, Series 40 Disk Drive Maintenance Manual. ('Diablo' is a trademark of Diablo Systems Incorporated.)

DISK FORMAT

Each track on the disk is divided into 24 sectors of equal length. Each full track rotation is approximately 25 milliseconds for the 2400 RPM drive. The following diagram illustrates the details of the track sector.



Preamble - This field is created during a format operation. It starts at the leading edge of the sector mark and consists of 20 bytes: the first nineteen bytes are 0 (all clock bits), the first 6 bits of the twentieth byte are 0, the last two bits are '11'. This field is used to switch the head to read the sync 1 character during write, read, and read/verify operations.

Sync 1 - This field is contained in the preamble. It consists of three bits (011). The interface detects a 011 and prepares to read the header.

Header - This section contains information identifying the sector as cylinder, head, disk, and actual sector address. It is created as a result of the format command. It is read and compared with MDR for write, read, and read/verify operations.

The following diagram describes the 16 bits of the header:

T1	T2	T3	T4	T5	T6	T7	T8	T0	D	H	S0	S1	S2	S3	S4
0			MDRH				7/0			MDRL					7

(MEMORY DATA REGISTER)

where T1 to T8 = Low 8 order bits of cylinder address
T0 = High order bit of cylinder address
D = Disk = 0 - Fixed disk
= 1 - Removable disk
H = Head = 0 - Bottom head
= 1 - Top head
S0 to S4 = Sector Address

For the seek command, bits 9 and 10 are used to select the platter (fixed/removable) and the surface (top/bottom) respectively.

Gap - The gap is composed of all clock bits but for the last two bits which are '11'. This field serves as a preamble to the data field. The gap is used for header comparison time and to allow for switching of the heads in the case of a write command.

Sync 2 - The sync 2 character is the last three bits of the gap (011). These bits are created during a write operation. For read and read/verify operations, these bits designate the start of the data field.

Data Field - This field contains 256 bytes of data.

CRC - (Cyclic Redundancy Check) - This check is a 2-byte character created from the sync 2 character and the 256 bytes of the data field.

Postamble - This section is composed of all clock bits.

DISK SECTOR FORMAT

FIELD	2400 RPM	APPROXIMATE BYTES
Preamble & Sync 1	64 µsec	20
Header	6.4 µsec	2
Gap And Sync 2	32 µsec	10
Data Field	819.2 µsec	256
CRC	6.4 µsec	2
Postamble	113.66 µsec	35.5
TOTAL	1041.66 µsec	325.5

The Preamble and Postamble are necessary to absorb system tolerances.

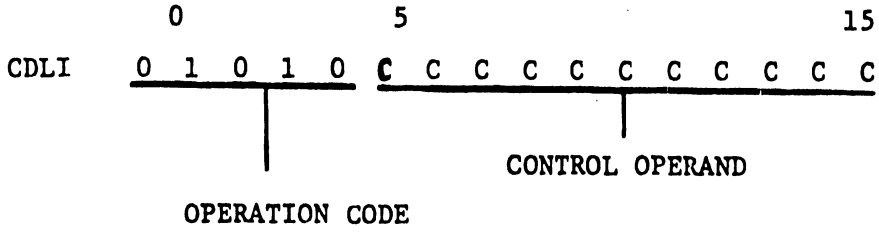
DISK SELECTION:

The hard disk gains access to the communication lines whenever the pointer register equals (00, 01, 10).

CDLI - CONTROL DEVICE LEVEL INTERFACE

Upon detection of this instruction, the MP sets the INPUT bit=0, alerts the DAI and allows the control operand. MDR (16 bits) and the pointer register (2 bits) are also allowed to the DAI. The *INPUT status bit is set to '1' by the DAI in response. The status register must not be used as a B-bus operand when waiting for the DAI response (INPUT bit).

FORMAT:



*The input bit signals the completion of an assigned task by the Device Adapter.

The table below lists the 9 commands as specified by the control operand.

BIT		OPERATION
8, 9	=	01 - Give Disk Status
	=	10 - Give Operation Status
	=	11 - Give Sector
10	=	1 - Seek
11	=	1 - Surface Operation
12, 13	=	00 - Format
	=	01 - Write
	=	10 - Read
	=	11 - Write/Verify
15	=	1 - Restore

GIVE DISK STATUS (CDLI 040)

Upon detection of this command the interface strobes 5 bits of status reflecting the state of the disk into BITS MDL3-MDL7. BITS MDL0-MDL2 are made 1. The status bits should be in MDRL by the start of the next instruction cycle.

MDRL Bit		Condition
MDL3	=	0 - Address interlock
MDL4	=	0 - File ready
MDL5	=	0 - Ready to seek/read/write
MDL6	=	0 - Seek incomplete
MDL7	=	0 - Write check

Address Interlock - This bit is set to 0 if the seek command cannot be executed due to a track address greater than the number of tracks available. This bit remains 0 until a restore command or a seek command to a valid address has been accepted.

File Ready - This bit is set to 0 if all of the following conditions are met:

(a) Power on.
(b) Dust cover loaded.
(c) Equipment drawer closed.
(d) LOAD/RUN switch in RUN position.
(e) Start-up cycle complete.
(f) Write check. (NOT ACTIVE (HIGH)).

Ready to Seek/Read/Write - This bit is set to 0 if the disk is not in the process of executing a restore command or a seek command to an address other than the one under the heads and if the File Ready bit is 0. The seek incomplete bit has no bearing on this bit.

Seek Incomplete - This bit is set to 0 if a malfunction keeps the seek operation from completing. This bit remains 0 until a restore command has been completed by the disk.

Write Check - This bit is set to 0 if a malfunction occurs which may not be corrected by the microprocessor.

GIVE OPERATION STATUS (CDLI 080)

Upon detection of this command, the interface strobes 8 bits of status reflecting the result of a read, write, write/verify, or format operations into BITS MDL0-MDL7. The status bits should be in MDRL by the start of the next instruction cycle.

MDRL Bit		Condition
MDL0	=	1 - File not ready
MDL1	=	1 - Parity Error
MDL2	=	1 - Illegal address
MDL3	=	1 - Data compare error
MDL4	=	1 - Header compare error
MDL5	=	1 - CRC error
MDL6	=	1 - Overrun
MDL7	=	1 - Mixed error

File Not Ready - This bit is set to 1 if the disk presents a file not ready condition (write check, etc.).

Parity Error - This bit is set to 1 whenever the interface is in a direct memory access operation and the memory controller reports a parity error.

Illegal Address - This bit is set to 1 whenever the interface is in a direct memory access operation and the memory controller reports an illegal address.

Data Compare Error - This bit is set to 1 if during a read/verify operation the data does not compare equal.

Header Compare Error - This bit is set to 1 whenever the interface finds that the header bytes in MDR are not the same as the header bytes in the sector.

CRC Error - This bit is set to 1 whenever the interface finds that the computed CRC is not the same as the CRC written on the disk.

Overrun - This bit is set to 1 if the interface is ready for a memory operation and the last memory operation has not completed.

Mixed Error - This bit is set to 1 if any of the following conditions occur during an operation:

(a) The interface cannot detect the sync 2 character.
(b) There is still data to be read or written on the disk and a sector mark has been detected.
(c) No sector mark detected after a sector's time.

Operation status must be requested after every surface operation. The microprogram should time the duration of the surface operation since a condition may arise which keeps the input bit from being set.

GIVE SECTOR (CDLI 0C0)

* The complemented value of the sector address lines is strobed into BITS MDL3-MDL7. If the sector is not valid (a sector mark pulse is present), BIT MDL2 is made 0. BITS MDL0 and MDL1 are forced to 1.

SEEK (CDLI 020)

The low order 8 bits of track address are in BITS MDH0-MDH7, the high order track address bit is in BIT MDL0. The interface gates the 9 track address bits to the disk address lines and issues a strobe. If the address is invalid, the address interlock bit will reflect this condition. If the address interlock bit is zero and the disk accepts the command, the address interlock bit is set to 1.

If the command is accepted and the track address is valid, the heads are placed at the selected track.

If the disk is deselected, the platter select and surface select revert to the default values (fixed platter, bottom surface). Because of this, it is necessary to issue a seek command to select the platter and surface prior to a surface operation. After platter and surface selection, a six microsecond delay must be introduced prior to requesting the selected sector counter. Also a 25 microsecond delay must be introduced from the time of seek to the time of a surface operation.

For the above four commands, the interface does not set the input bit to 1.

FORMAT (CDLI 010)

Upon receipt of this command, the interface awaits the leading edge of the sector mark pulse. Once it has sensed it, the format operation

*The sector address is active low (0V, .4V). MDL3 is the most significant bit of the sector address.

starts. The interface creates the preamble, writes the sync 1 character and writes the header (from MDR-16 bits). The input bit is set to 1 immediately after the header is written.

WRITE (CDLI 014)

Upon receipt of this command, the interface awaits the leading edge of the sector mark pulse. Once it has sensed it, the write operation starts. The interface detects the sync 1 character and prepares to read the header. The read header is compared with the header in MDR (16-bits); if the headers do not match, a status bit is set in the operation status and no data transfer takes place. The input bit is set to 1, and the operation is terminated.

If the headers match, the interface writes the gap and the sync 2 character designating the start of the data field. The MAR contains the memory address from which the data is to be transferred. The interface reads two bytes at the time from memory, increments the memory address by 2, writes the two bytes on the disk and computes the CRC. A total of 256 data bytes are transferred from memory, the two CRC bytes are written, the interface sets the input bit to 1, and creates the postamble.

READ (CDLI 018)

Upon receipt of this command, the interface awaits the leading edge of the sector mark pulse. Once it has sensed it, the read operation starts. The interface detects the sync 1 character and prepares to read the header. The read header is compared with the header in MDR (16-bits); if the headers do not match, a status bit is set in the operation status and no data transfer takes place. The input bit is set to 1, and the operation is terminated.

If the headers match, the interface detects the gap and the sync 2 character and prepares to read the data. The MAR contains the memory address at which the data is to be transferred. The interface reads two

bytes at the time from the disk, computes the CRC, writes the two bytes into memory and increments the memory address by 2. A total of 256 data bytes are transferred to memory. The computed CRC is compared with the CRC read from the disk; if they do not match, the appropriate bit in the operation status reflect the condition. The interface sets the input bit to 1 indicating operation completion.

The CRC is written and checked by the device adapter. The MP never participates in this activity, however, the MP is notified if a CRC error has occurred.

WRITE /VERIFY (CDLI 016)

Upon receipt of this command, the interface awaits the leading edge of the sector mark pulse. Once it has sensed it, the operation starts. The interface detects the sync 1 character and prepares to read the header. The read header is compared with the header in MDR (16-bits); if the headers do not match, a status bit is set in the operation status and no data comparison takes place. The input bit is set to 1, and the operation is terminated.

If the headers match, the interface detects the gap and the sync 2 character and prepares to read the data from the disk. The MAR contains the memory address from which the data is to be read. The interface reads 2 bytes from the disk and two bytes from memory at a time, compares them and if they do not match, the data compare error bit in the status register is set to 1. The CRC character is computed. This is done for all of the 256 bytes in the disk. The computed CRC is compared with the CRC read from the disk; if it does not match, the appropriate bit in the operation status reflects the condition. The interface sets the input bit to 1 indicating operation completion.

If there is a sector mark pulse at the time one of the above four commands is issued, the interface sets the input bit to 1 before the next instruction cycle and terminates the operation.

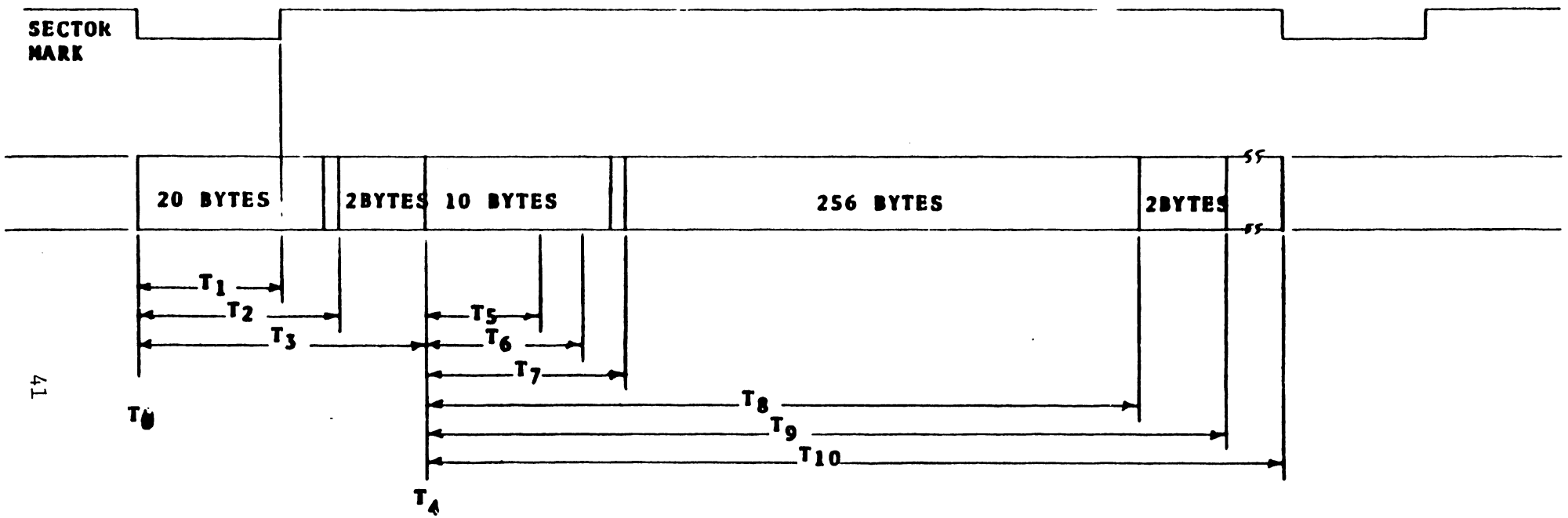
RESTORE (CDLI 001)

This command causes the heads to be positioned over track 0; once there, the seek incomplete indication is reset.

The input bit is not set to 1 by the interface as a response to this command.

8300 HARD DISK TIMING

10 MEGA BYTE 2400 RPM



T0 = LEADING EDGE OF SECTOR MARK, SWITCH HEADS DURING A FORMAT SEQUENCE
T1 = STARTING POINT DURING A READ/WRITE/READ VERIFY, LOOKING FOR SYNC CHARACTER 011(40uS±20uS)
T2 = WRITE SYNC CHARACTER FOR HEADER (20 BYTES) (64uS)
T3 = LAST BIT OF THE TWO BYTE HEADER (22 BYTES) (70.4uS) (CTR=176 FORMAT) (CTR=16 READ/WRITE/READ VERIFY)
T4 = REFERENCE POINT FOR READ/WRITE/READ VERIFY SEQUENCE, COUNTER NOW LOADED TO 96
T5 = SWITCH HEADS DURING A WRITE SEQUENCE (6 BYTES) (19.2uS) (CTR=144)
T6 = STARTING POINT DURING A READ-OR A-READ VERIFY, LOOKING FOR SYNC CHARACTER 011(8 BYTES) (25.6uS) (CTR=160)
T7 = FINISH WRITING DATA SYNC CHARACTER DURING A WRITE SEQUENCE (10 BYTES) (32uS) (CTR=176)
T8 = END OF WRITE FOR SYNC TWO AND DATA FIELD (266 BYTES) (851.2uS) (CTR=2224)
T9 = END OF CRC (268 BYTES((857.6uS) (CTR=2240)
T10 = END OF POSTAMBLE (303 BYTES) (969.6uS) (POSTAMBLE=112uS)

- FLOPPY (315 KILOBYTE) -

GENERAL DESCRIPTION:

The Shugart Floppy *Model 901 consists of one diskette, one read/write head which makes contact with the diskette's surface during step and surface operations, one PCB which provides some elementary functions, and other controlling and controlled mechanisms. Most of the electronics necessary to control the floppy are also used to control the hard disks. There are a few components which are dedicated to the control of the floppy. One is the sector counter which is set to 0 by the leading edge of the index mark and incremented by 1 every time two sector marks have been sensed. Another is the timer which is a 12.6 ms (±10%) one shot that is controlled by a CDLI instruction and monitored through one bit obtained in MDRL after execution of the Give Disk Status CDLI instruction. The timer is used to fulfill three functions: to time the duration of step, to time the head settling time once at the desired track, and to measure the 50 ms interval that must be introduced between head load and valid data. Those components used to control the hard disk are modified (clock frequency changed, counters preset, etc.) to control the floppy.

NOTE:

Floppy Disk is the general terminology given to a disk system where the Read/Write head(s) makes physical contact with a flexible recording media.

*See Shugart Associates Diskette Storage Drive Manual SA900/901 (Wang Laboratories Service Bulletin No. 46.2 starting on page 10).

DRIVE CHARACTERISTICS

Rotational Speed: 360 RPM
Rotational Period: 166.72 ms
Average Access Time: 424 ms
Average Latency: 83 ms
Data Transfer Rate: 31250 bytes/sec.
Bit Cell Time: 4 µsec
Track to Track Access Time: 11 ms
Head Settling Time Once at Desired Track: 11 ms
One Sector's Time: 5.21 ms
Number of Sectors Per Track: 32
Number of Tracks: 77
Sector Mark Duration: 400 µsec $\pm$ 200 µsec
Index Mark Duration: 400 µsec $\pm$ 200 µsec
Direction Select Pulse Duration: 1 µsec min.
Time Between Head Load and Valid Data: 50 ms
Time Between Head Load and Step: 30 ms

DISK FORMAT

Each track on the disk is divided into 32 sectors of equal length. The present specifications require a sector to be 256 data bytes long. In order to allow for this, two sectors must be used, so in effect, each track is divided into 16 sectors each lasting 10.42 ms. The following diagram illustrates the sector organization.

PREAMBLE	SYNC 1	HEADER	GAP	SYNC 2	DATA FIELD	CRC	POSTAMPLE

Preamble - This field is created during a format operation. It starts at the leading edge of the sector mark and consists of 20 bytes: the first nineteen bytes are 0 (all clock bits), the first 6 bits of the twentieth byte are 0, the last two bits are '11'. This field is used to switch the head to read the sync 1 character during write, read, and read/verify operations.

Sync 1 - This field is contained in the last byte of the preamble. It consists of three bits (011). The interface detects a 011 and prepares to read the header.

Header - This section contains information identifying the sector as cylinder, head, disk, and actual sector address. It is created as a result of the format command. It is read and compared with MDR (16-bit) for write, read, and read/verify operations.

The following diagram describes the 16 bits of the header:

Header

First Byte								Second Byte							
0			MDRH				7	0			MDRL				7
0	64	32	16	8	4	2	1	0	0	0	0	8	4	2	1
Track Address								Sector Address							

Valid Binary Values:

0000 0000 through
0100 1100 = 77 Tracks

Valid Binary Values:

0000 0000 through
0000 1111 = 16 Sectors

Gap - The gap is composed of all clock bits but for the last two bits which are '11'. This field serves as a preamble to the data field. The gap is used for header comparison time and to allow for switching of the heads in the case of a write command.

Sync 2 - The sync 2 character is the last 3 bits of the gap (011). These bits are created during a write operation. For read and read/verify operations, these bits designate the start of the data field.

Data Field - This field contains 256 bytes of data.

CRC - (Cyclic Redundancy Check) - This check is a 2-byte character created from the sync 2 character and the 256 bytes of the data field.

Postamble - This section is composed of all clock bits.

The preamble and postamble are necessary to absorb system tolerances.

DISKETTE SECTOR FORMAT

FIELD	LENGTH	APPROXIMATE BYTES
Preamble & Sync 1	640 µsec	20
Header	64 µsec	2
Gap & Sync 2	640 µsec	20
Data Field	8192 µsec	256
CRC	64 µsec	2
Postamble	820 µsec	25
TOTAL	10420 µsec	325

DISK SELECTION:

The floppy disk gains access to the communication lines whenever the pointer register is 11. It is undesirable tc have the select/deselect function become the head load/unload function. The disk select sole function is to qualify the communication lines for floppy operations.

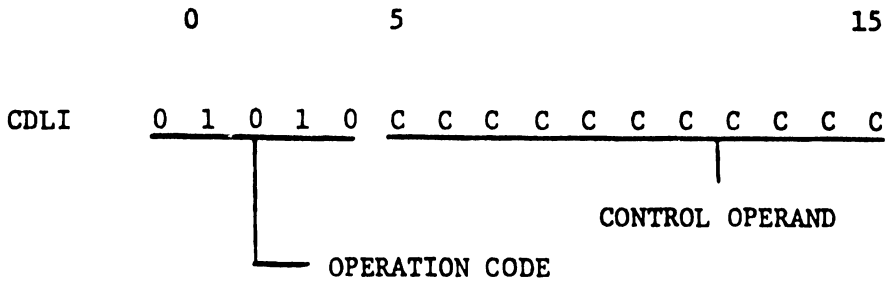
CDLI - CONTROL DEVICE LEVEL INTERFACE

Upon detection of this instruction, the MP sets the INPUT bit=0, alerts the DAI and allows the control operand. MDR (16 bits) and the pointer register (2 bits) are *also* allowed to the DAI. The *INPUT

*The input bit signals the completion of an assigned task by the Device Adapter.

status bit is set to '1' by the DAI in response. The status register must not be used as a B-bus operand when waiting for the DAI response (INPUT bit).

FORMAT:



The table below lists the 12 commands as specified by the control operand.

BIT		OPERATION
5, 6, 7	=	001 - Step
	=	111 - Head Control
	=	011 - Direction Select
	=	100 - Start Timer
	=	101 - File Inoperable Reset
8, 9	=	01 - Give Disk Status
	=	10 - Give Operation Status
	=	11 - Give Sector
11	=	1 - Surface Operation
12, 13	=	00 - Format
	=	01 - Write
	=	10 - Read
	=	11 - Write/Verify

GIVE DISK STATUS (CDLI 040)

Upon detection of this command, the interface strobes 5 bits of status reflecting the state of the disk into MDRL. The status should be in MDRL by the start of the next instruction cycle.

MDRL Bit		Condition
MDL0	=	0 - Track 0
MDL1	=	0 - Write Protect
MDL2	-	Undefined
MDL3	-	Undefined
MDL4	=	0 - File Ready
MDL5	=	0 - Timer Not Active
MDL6	-	Undefined
MDL7	=	0 - File Inoperable

Track 0 - This bit is 0 whenever the head is positioned at the outermost data track (away from disk registration hub).

Write Protect - This bit is 0 whenever the diskette is write protected. It is a microprogram responsibility to reject any write commands to a diskette that is write protected.

File Ready - This bit is 0 when all of the following conditions are met:

(a) Power on.
(b) Diskette properly loaded.
(c) Door closed.
(d) Diskette is turning (two sector marks sensed).

The ready indication is provided when two sector marks (or an index mark and a sector mark) are sensed, not necessarily when the drive is up to speed For this reason the program introduces a two second delay at initialize time.

Timer Not Active - This bit goes to 1 as soon as the Start Timer command is issued; it goes to 0 once 12.6 ms (± 10%) have elapsed from the time the Start Timer command was received.

File Inoperable - This bit is set to 0 whenever the head is improperly energized. When this bit is 0, no surface operations should take place since the data integrity circuitry is not at its optimum. A File Inoperable Reset command must be issued to reset this indicator.

GIVE OPERATION STATUS (CDLI 080)

This command produces the result described in the hard disk specification and must be used as specified there.

GIVE SECTOR (CDLI 0C0)

* This command works as specified in the hard disk specification. Bit MDL3 always receives a 1.

Surface Commands - Format (CDLI 010), Write (CDLI 014), Read (CDLI 018), WRITE /Verify (CDLI 01C). These commands work as specified in the hard disk specification.

STEP (CDLI 100)

This command causes the interface to pulse the step line which in turn causes the floppy to move the head one track in the direction previously selected. For this command to work properly, the head must have been loaded for at least 30 ms. The interface does not require program attention during the time (11 ms) that it takes the step to complete, that is, the floppy may be deselected.

*The floppy has only 4 sector address lines (MDL4 becomes the most significant bit).

HEAD CONTROL (CDLI 700)

Through this command, the head may be loaded and unloaded. Once the head is loaded, the microprogram must introduce a 50 ms delay before valid data is expected, that is, before a Surface operation is started. Also, the microprogram must delay at least 30 ms from the time the head is loaded to the time of the first step. This delay is part of the 50 ms delay.

Bit MDL4 of MDRL is used to specify load or unload.

MDL4 = 0 - Head Unload.
MDL4 = 1 - Head Load.

The other bits in MDRL may be set to any value while issuing this command.

DIRECTION SELECT (CDLI 300)

This command is used to select the direction in which the head is to move during the Step command. The direction selected is stored in the interface so it is not necessary to select it every time a step is to be done. The direction is selected through bit MDL4 of MDRL.

MDL4 = 0 - Direction Out (towards track 0).
MDL4 = 1 - Direction In (towards track 76).

The other bits in MDRL may be set to any value. The following sequence is acceptable:

Load MDRL with Direction Bi
Direction Select
Step
Start Timer

The direction may be selected any time after initialize.

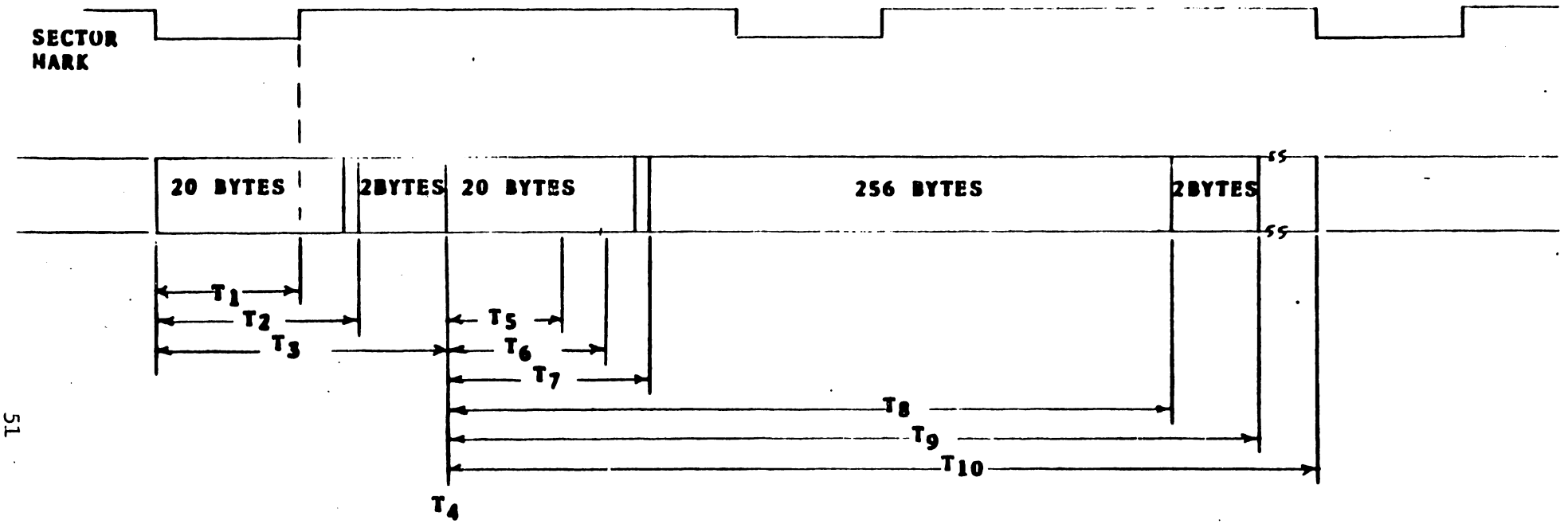
START TIMER (CDLI 400)

Upon receipt of this command, the interface will fire the 12.6 ms (± 10%) one shot and set the Timer Not Active bit to 1. Once the 12.6 ms have elapsed, the Timer Not Active bit is set to 0. This is the only command that may be issued independent of the selected device, that is, the pointer register may contain any value and the command will be acknowledged. However, to monitor the timer (through the Give Disk Status CDLI instruction) the pointer register must contain a '11'. The timer may be started and monitored even if there is no disk connected in the interface port.

FILE INOPERABLE RESET (CDLI 500)

This command will cause the File Inoperable bit to be reset without clearing the condition which caused it to be set. This command is necessary because if the condition clears, the File Inoperable bit will not be automatically set to 1.

8300 FLOPPY DISK TIMING



T0 = LEADING EDGE OF THE SECTOR MARK, SWITCH HEADS DURING A FORMAT SEQUENCE
T1 = STARTING POINT DURING A READ/WRITE/READ VERIFY, LOOKING FOR SYNC CHARACTER 011 (400uS±200uS)
T2 = WRITE SYNC CHARACTER FOR HEADER (20 BYTES) (640uS)
T3 = LAST BIT OF THE TWO BYTE HEADER (22 BYTES) (704uS) (CTR=176 FORMAT) (CTR=16 READY/WRITE/READ VERIFY)
T4 = REFERENCE POINT FOR READ/WRITE/READ VERIFY SEQUENCES
T5 = SWITCH HEADS DURING A WRITE SEQUENCE (16 BYTES) (512uS) (CTR-144)
T6 = STARTING POINT DURING A READ-OR A- READ VERIFY, LOOKING FOR SYNC CHARACTER 011 (18 BYTES) (576uS) (CTR=160)
T7 = FINISH WRITING DATA SYNC CHARACTER DURING A WRITE SEQUENCE (20 BYTES) (640uS) (CTR=176)
T8 = END OF WRITE FOR SYNC TWO AND DATA FIELD (276 BYTES) (8832uS) (CTR=2224)
T9 = END OF CRC (278 BYTES) (8896uS) (CTR=2240 WRITE) (2224 READ)
T10= END OF POSTAMBLE (303 BYTES) (9696uS) (POSTAMBLE=800uS)

*ALL TIMES SHOWN ARE NOMINAL

- HARDWARE OPERATION -

The hardware operation is broken down into major elements of operation - i.e., each element described has, for the most part, an independent circuit operation and provides a distinct operational function.

These major element descriptions are limited to the immediate circuit operation. The relationship of these elements to each other are described in the Instruction Operation Section - 3.0.

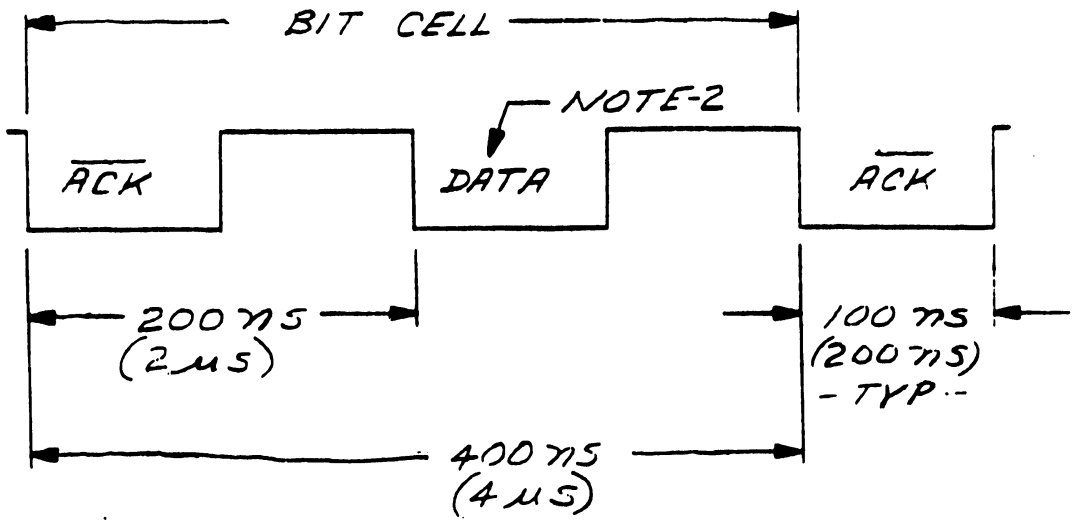
The following elements are described:

- WRITE CLOCK -

The Write Clock circuit is used to provide all the necessary timing relationships required to write data on the disk drive media - i.e., to generate 'bit-cells' which will contain the data bit, and, to place the data bit within that 'bit-cell'. Two clock components are generated to satisfy this 'bit-cell' arrangement. They are 'A-clocks' (ACK & $\overline{\text{ACK}}$), and 'B-clocks' (BCK & $\overline{\text{BCK}}$). The 'A-clocks' are used to form the 'bit-cell' and the 'B-clocks' are used to place the data bit in the center of the 'bit-cell'.

Both the hard disk and the floppy disk have this 'bit-cell' arrangement, however, the rotational speed and density of the hard and floppy disks are different. Therefore, the 'bit-cells' and the actual 'A-clocks' and 'B-clocks' are of different duration for each. The write clock network automatically supplies the correct timing for the selected disk drive.

The following schematics, description, and timing diagrams depict the Write Clock operation:



NOTES:

1. XXX = HARD DISK.
   (XXX) = FLOPPY DISK.
2. DATA:
   HIGH = LOGIC '0'
   LOW = LOGIC '1'
   THE DATA IS WRITTEN AT 'BCK' TIME.

DISK 'BIT-CELL'

CIRCUIT OPERATION

The Write Clock network can be broken into two areas. The generation of the Increment Write Clock (IWC), used to step the write counter and to provide the actual pulse width of the 'A-clocks' (ACK & $\overline{\text{ACK}}$) and the 'B-clocks' (BCK & $\overline{\text{BCK}}$), and the generation of the 'bit-cell' duration and 'data-bit' placement within the 'bit-cell'.

INCREMENT WRITE CLOCK (IWC)

A 10 MHz crystal oscillator is the base for all write clock circuitry. The buffered oscillator output (L10-6) is felt at the input of IWC multiplexer (L33-2), and is passed through when the clock speed flop (L22-5) is selected to the hard disk timing (fast, L22-5 = '1'). The speed select flop is set via term $\overline{\text{FDS}}$ at a logic '1' level (floppy disk not selected) and clocked via L10-12 (Write $\overline{\text{CTR=15}}$) on the low to high transition. The write counter is a free running counter clocked by the term IWC (Increment Write Clock). It should be noted that IWC is always active at one of its two speeds.

The output of the IWC multiplexer reflects the inversion of the buffered oscillator (L10-6). This signal has a 100 ns period with a 50% duty cycle. The buffered oscillator output is also felt on the clock input of flop L22-9. The '$\overline{\text{Q}}$' output of flop L22-9 (L22-8) is tied to the 'D' input of that flop forming a divide by two counter. When the speed select flop is set to floppy disk timing (L22-5=logic '0') the buffered oscillator output felt on L33-2 is blocked and the divide by two counter felt on L33-5 is gated through the IWC multiplexer via L22-6 felt on L33-4. The output of the IWC multiplexer (L33-6) reflects the inversion of the divide by two flop (L22-9). This signal has a 200 ns period with a 50% duty cycle.

When changing IWC speed there is no chance for a spike to occur on the IWC term - i.e., both L33-2 and L33-5 are at the logic '0' level (disabling the IWC multiplexer) when the clock speed select flop is clocked.

Please refer to the following timing diagram for further explanation.

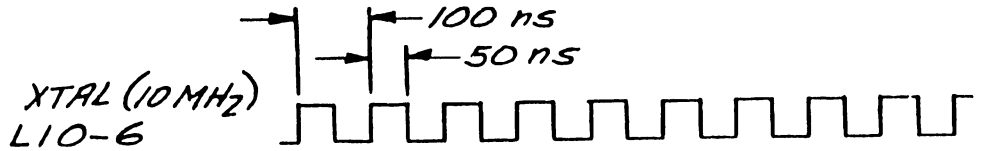
'BIT-CELL' GENERATION

The base for 'bit-cell' generation is the free running write counter (L21). This counter is a programmable synchronous four bit binary counter (74LS161). It increments on the low to high transition of the clock. This counter has a synchronous load - i.e., the programmable inputs A, B, C and D are loaded into the counter on the low to high transition of the clock if the load enable is active (Pin 9 = '0').

By varying the programmable inputs and loading the counter each time it steps out of binary 15, a method of controlling the period of the 'Counter=15' signal (Pin 15) becomes possible - i.e., a value of binary 14 is loaded into the counter (L21) when the counter steps out of binary 15 via programmable inputs A='0', B='1', C='1', D='1' ('D' input to counter is from clock speed select flop L22-5='1' - hard disk) and load enable active (L21-9). You will notice the load enable signal is the inverse of Counter=15 term (L21-15). This causes a signal pulse of 100 ns with a period of 200 ns present at L21-15 (Counter=15).

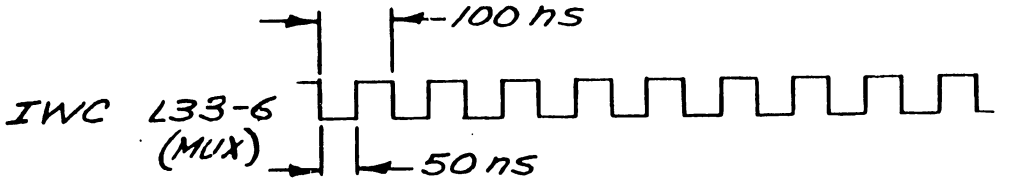
By loading a binary value of 6 into the counter via programmable inputs A=0, B=1, C=1 and D=0 ('D' input to counter is from clock speed select flop L22-5=0 - floppy disk), the counter must increment nine times to reach binary 15 and once again to load for the next cycle. This results in ten IWC periods of 200 ns each giving a period of 2 µs and a pulse width of 200 ns for the Counter=15 signal present on (L21-15).

The clock speed select flop (L22-5) not only changes the load count into the write counter, but changes the frequency of IWC as explained above. This accounts for the 200 ns pulse width of the Counter=15 signal and accounts for some of the greatly increased period of the Counter=15 signal.



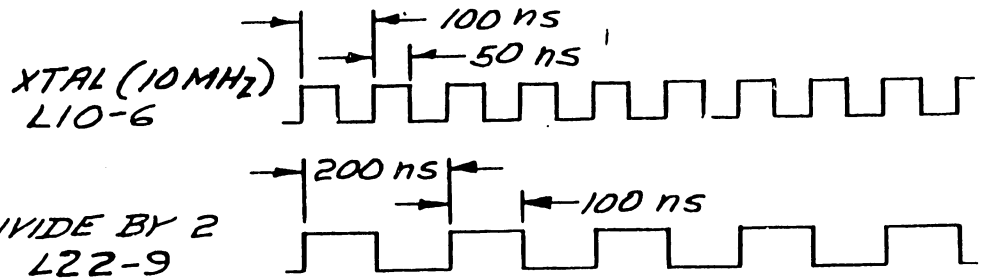
CLOCK SPEED SELECT L22-5 — (HIGH - FAST)

HARD DISK SPEED — MADE FROM FLOPPY DISK NOT SELECTED [$\overline{FDS}$ = HIGH]



INCREMENT WRITE CLOCK (HARD DISK) MADE FROM XTAL AND CLOCK SPEED SELECT [L10-6 • L22-5]

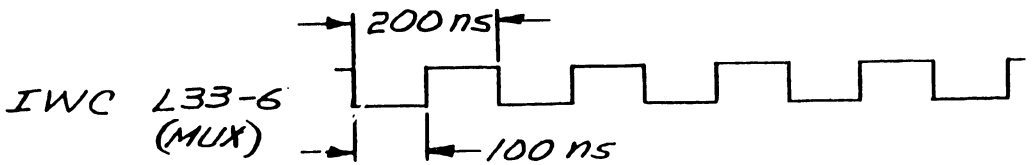
IWC GENERATION FOR HARD DISK



MADE FROM XTAL AND DIVIDE BY 2 $\bar{Q}$ OUTPUT [L10-6 • L22-8]

CLOCK SPEED SELECT L22-5 — (LOW - SLOW)

FLOPPY DISK SPEED — MADE FROM FLOPPY DISK SELECT [$\overline{FDS}$ = LOW]



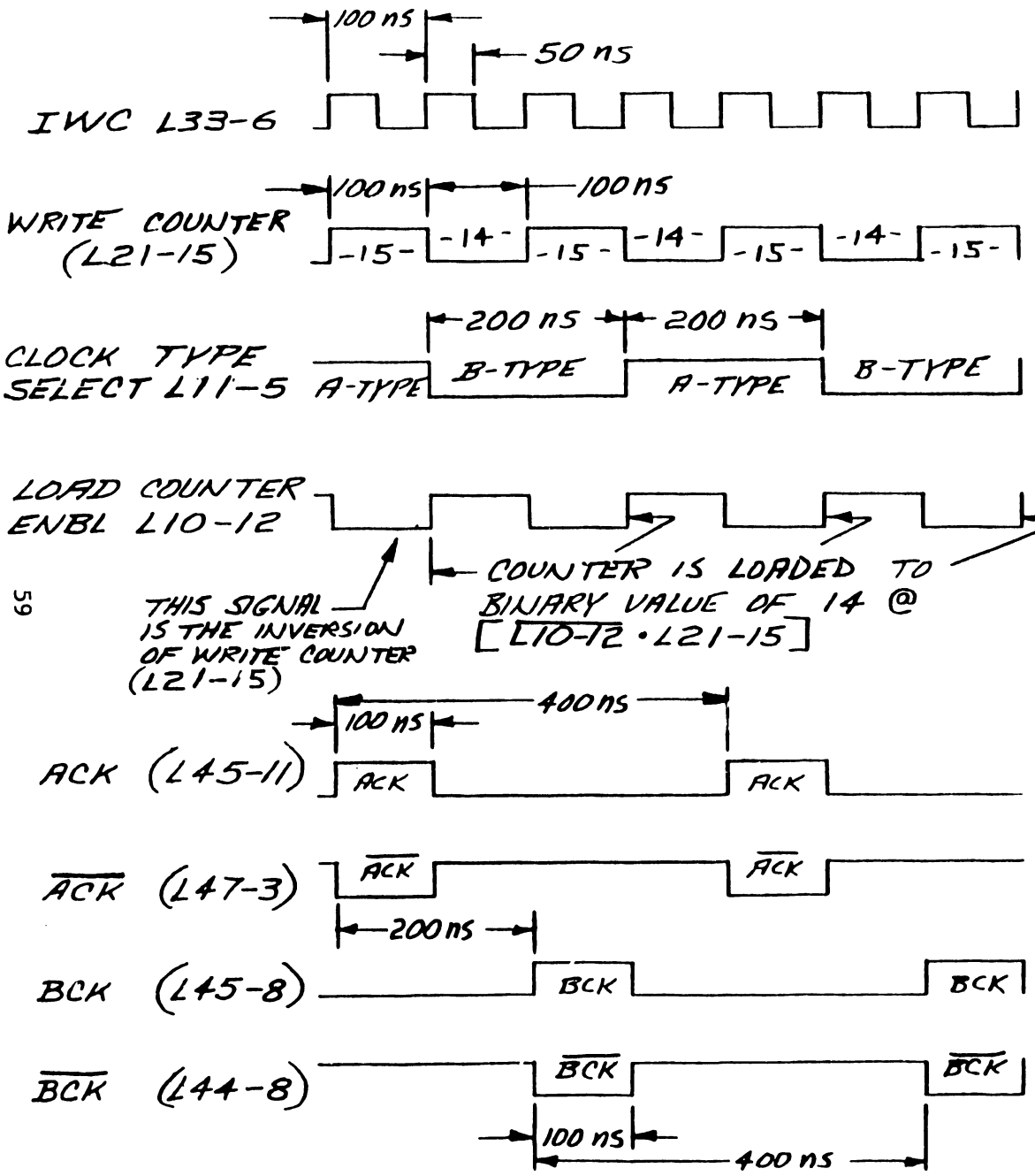
INCREMENT WRITE CLOCK (FLOPPY DISK) MADE FROM DIVIDE BY 2 AND CLOCK SPEED SELECT [L22-9 • L22-6]

IWC GENERATION FOR FLOPPY DISK

It is the Counter=15 signal and the clock type select flop (L11-5) that generates the 'A-clocks' and 'B-clocks' via L45-11 (ACK), L47-3 ($\overline{ACK}$), L45-8 (BCK) and L44-8 ($\overline{BCK}$). The clock type select flop (L11-5) is switched when the write counter steps out of binary 15. (This is the same time the write counter is loaded). This arrangement gives alternate clock pulses ('A-clocks' then 'B-clocks') with a pulse width equal to the Counter=15 signal (L21-15) pulse width and a period equal to the period of the Counter=15 signal.

When the clock speed select flop (L22-5) is switched, there will be one write counter (L21) period with the improper IWC frequency. However, the clock speed select flop can only be changed at the beginning of a 'CDLI' command, at which time no operation is in progress. (The protocol between the MP and Hard/Floppy Disk Device Adapter prohibits issuing of new commands until the present command is complete.)

Please refer to the following timing diagrams for further explanation.



INCREMENT WRITE CLOCK IS CLOCK TO WRITE COUNTER (L21)

THIS COUNTER (74LS161) IS PROGRAMMED TO DIVIDE BY TWO VIA LOADING INPUTS & LOAD CIRCUIT

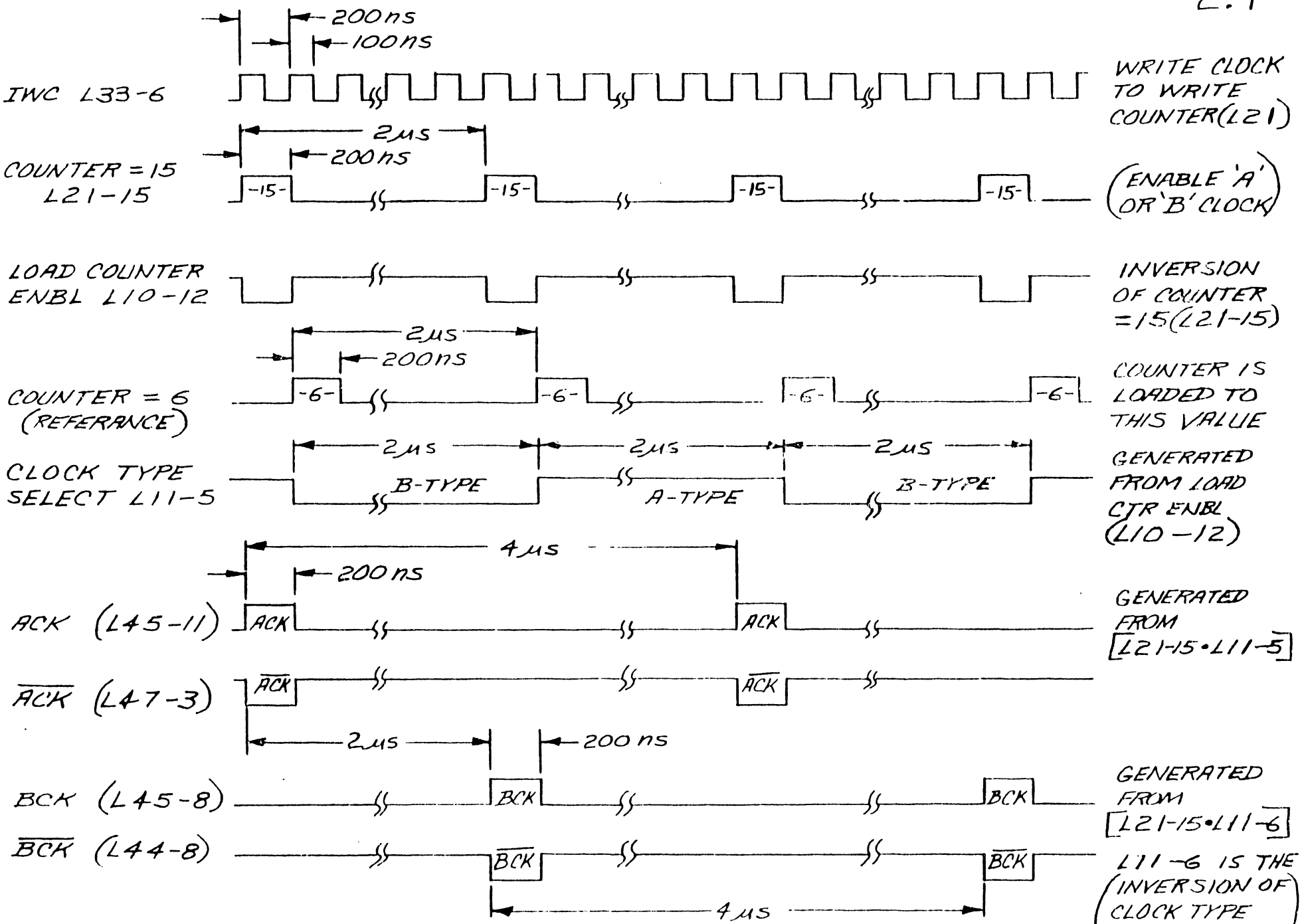
CLOCK TYPE IS SWITCHED EACH LOW-TO-HIGH TRANSITION OF LOAD COUNTER ENBL (L10-12)

COUNTER IS LOADED VIA ICW LOW-TO-HIGH TRANSITION AND LOAD COUNTER ENBL LOW. A LOAD VALUE OF BINARY 14 IS SELECTED VIA LOAD INPUT A=0, B=1, C=1, AND D=1 (L22-5).

ACK & $\overline{ACK}$ ARE GENERATED FROM WRITE COUNTER = 15 AND CLOCK TYPE SELECT [L21-15 • L11-5]

BCK & $\overline{BCK}$ ARE GENERATED FROM WRITE COUNTER = 15 AND CLOCK TYPE SELECT [L21-15 • L11-6]

ACK & BCK' GENERATION FOR HARD DISK



ACK & BCK GENERATION FOR FLOPPY DISK

60

- DISK CONTROL -

Disk Control is handled as part of the instruction operation - i.e., the conditions required by the disk for status, read, write, error recovery, are met by that instruction's execution. These disk control requirements will be described in the Instruction Operation Section - 3.0. However, there are two conditions that have to be met before any operation can begin:

1. The Device Adapter board has to be selected.

2. A particular disk drive has to be selected (one of four).

Following is a schematic and description.

DISK SELECT

The Device Adapter can have three hard disks and one floppy disk attached to it. However, only one of these devices can be used at any given time. The qualifying term for the selected drive (allowing only that drive access to the Device Adapter via the Device Level Interface) are the select terms $\overline{\text{SEL0}}$, $\overline{\text{SEL1}}$, $\overline{\text{SEL2}}$ (hard disk select drive #0, 1 or 2) and the term $\overline{\text{FDS}}$ (Floppy Disk Select). These terms are mutually exclusive of each other and are statically decoded from the microprocessors Pointer Register (PT0 & PT1) via decoder L9.

1. Select terms $\overline{\text{SEL0}}$, $\overline{\text{SEL1}}$, $\overline{\text{SEL2}}$ are for the hard disks and therefore, the Clock Speed Select Flop in the Write Clock Section - 2.1 is selected for fast. Term $\overline{\text{FDS}}$ (Floppy Disk Select) forces a Slow Speed Select.

2. There will always be a disk drive selected due to the static output of decoder L9 (it is always enabled).

DEVICE ADAPTER SELECT

The Device Adapter is selected to receive a new command at T02 of a CDLI microinstruction from the MP board. The DA Select Flop (L74-9) is set via [$\overline{\text{CDLI}}$ T02] L85-6. The DA Select Flop is cleared at T06 trailing edge (T07) via a logic '0' on the 'D' input of DA Select Flop (L74-12) and clocked via L84-6 at T07.

It should be noted that this select is up for only 750 ns (T02 through T06 at 150 ns/subcycle time) and that the commands take considerably more time to execute. However, the command is latched elsewhere and the protocol of the MP/DA prohibits any further command until either the input bit is set by the device adapter or a predetermined time-out has expired within the M.P. The method of completion is predetermined by the hardware/software design philosophy. The output of the DA Select Flop is referred to as 'Allow DA Operation' (ADO & $\overline{\text{ADO}}$).

- BIT SERIALIZATION REGISTER (BSR) -

The Bit Serialization Register is the primary register within the Device Adapter. All data being written onto the disk, read from the disk, data to the MP Memory Data Registers, data from the MP Memory Data Registers, and status information pass through the BSR.

The following is a schematic and description of the BSR network.

CIRCUIT OPERATION

The Bit Serialization Register consists of four 4-bit parallel load, parallel out, serial in and serial out shift register devices (74LS195) at locations L79, L80, L81 and L82.

The BSR has four dual 4-channel multiplexer devices (74LS153) at locations L68, L69, L70 and L71.

The BSR multiplexer provides four paths for loading the low order 8-bits of the BSR (D8-MSB, D15-LSB). The channel assignments are as follows:

Channel C0 = Sector Counter (2.5/3.3)
Channel C1 = Operational Status (2.8/3.2)
Channel C2 = Disk Status (3.1)
Channel C3 = Memory Data Register Low (From DAI - 1.3)

The BSR multiplexer is steered via L85-11 (MXA) and L85-8 (MXB). The BSR multiplexer channel select is enabled via the Device Adapter Select Flop term ADO (L74-9) present at L85-9&12, and the Control Operand terms R8 and R9 (ROM terms) perform the actual steering as follows:

R8	R9	CHANNEL
0	0	C3
0	1	C2
1	0	C1
1	1	C0

The parallel outputs from the BSR (D0-MSB through D15-LSB) pass to the MP Memory Data Register via the DAI.

D0 (MSB) ↔ D7 (LSB) = MDRH
D8 (MSB) ↔ D15 (LSB) = MDRL

The serial output D0 (L82-12) passes to the disk drive as serial data. The serial data input 'SDI' (L79-2&3) receives serial data from the disk drive.

The term '$\overline{\text{LSR}}$' (Load Shift Register) parallel loads the BSR (L79-9, L80-9, L81-9, L82-9).

The term 'SSR' (Shift Shift-Register) shifts data out or into the BSR (L79-10, L80-10, L81-10, L82-10).

1. The term 'SSR' is the clock term to the 74LS195 Shift Register Device. Serial data is shifted from 'QA' toward 'QD' outputs on the low to high transition of the clock term 'SSR' (L79-10, L80-10, L81-10, L82-10) when the load input is high (term '$\overline{\text{LSR}}$').

2. The Shift Register is loaded when the load input (term $\overline{\text{LSR}}$) is at a logic '0' and at the clocks (term 'SSR') low to high transition.

The term '$\overline{\text{CSR}}$' (Clear Shift Register) clears the shift register (L79-1, L80-1, L81-1, L82-1).

- BIT COUNTER -

The Bit Counter is used to control the actual 'bit placement' onto the disk drive media and to retrieve the disk 'serial data' from the disk drive media.

All data written onto the disk media is placed in the 'data field' of the disk's sector format - i.e., the data is placed between 'sync 2' and 'CRC'.

At this time, review the disk format in the Operational Specification section (1.5).

The Bit Counter provides the relative position (by binary value) of each segment of the sector format. The 'bit counter' binary value is monitored providing the beginning (binary value), the length (binary value), and the end (binary value) of each format segment - i.e., Preamble, Sync 1, Header, Gap, Sync 2, Data Field, CRC, and Postamble.

The Bit Counter also provides the End of Operation signal ($\overline{\text{SINPT}}$) by a predetermined binary value.

The operation termination (binary value) is dependent on the particular operation being performed - i.e., Format, Write, Read, and Write Verify.

Obviously the 'Bit Counter' is the primary controlling element for all surface operations. The actual controlling binary values will be described in the Instruction Operation section of this manual (3.0).

The following is a general description of the bit counter with the common controlling gates.

Please refer to the following schematic segment for this description.

CIRCUIT OPERATION

The 'Bit Counter' consists of three 74LS161 synchronous, binary, programmable counters (L76, L77, and L78). The Bit Counter has two modes of operation: writing onto the disk media and reading from the disk media. A common 'Sync Character Detected' Flop allows incrementing from the disk via 'READ CLOCKS'.

Writing - The Bit Counter is incremented by BCK felt at Bit Counter 'Clock' Multiplexer L39-13. This multiplexer is enabled for Write mode via term RGA (Read Gate Allow) not active (low) at L55-11 enabling the multiplexer (L39-1/high). Multiplexer half L39-9 is disabled by term SCD (Sync Character Detected) not active (low) via Sync Character Detected Flop L56-5 in the reset condition (L56-5/low).

The general protocol for writing data onto the disk media requires that the header first be read and verified. Therefore, all surface operations, less the disk format command, must first read the header from the disk media - i.e., all commands, less format, start as a read from disk; gated to the bit counter via 'READ CLOCKS' from the disk felt at L39-9. It should be noted that even in the case of a write operation, the 'Bit Counter' multiplexer (L39-8) is steered to read the disk via Sync Character Detected Flop (L56-5) felt as a high on L39-12. L39-12 is low at this time, term TIS (Timer In Sync) is not active (L34-9/low).

Reading - The primary increment for the 'Bit Counter' is from the disk's 'READ CLOCKS' felt at the 'Bit Counter' multiplexer L39-9 via L45-3.

The term RCA (Read Gate Allow) is active (high), L55-11, disabling BCK incrementing of the 'Bit Counter' at 'Bit Counter' binary value of 160 (L55-9&10). This value (160) is the start of the data field and will be described in the Instruction Operation section (3.0).

SYNC CHARACTER DETECTED

The 'Sync Character Detected' Flop (L56-5) is used for all surface operations less format. The purpose of this flop is to mark the beginning of valid data (either header or data field). A sync character of (00000011/ binary) is written on the disk media prior to the header during a format command. The same sync character is written prior to the data field during a write command. This 'Sync Character' must be detected before the appropriate surface operation can begin.

HEADER (SYNC 1)

The 'Sync Character' allows the 'Bit Counter' to be incremented by the disk's 'READ CLOCKS' and thereby read the header for the Read, Write, and Write Verify commands. After the header is read in, the 'Sync Character Detected' Flop is reset inhibiting any further counter increments. The reset signal to the 'Sync Character Detected' flop (L56-5) is derived by the last bit of the header (16 bit header) via ISS (Inhibit Serialization Shift) flop L67-8. This flop is set at the seventeenth count of the 'Bit Counter' [L76-15 (CTR=15) · CTR CLOCK].

1. No further 'Bit Counter' increments are allowed from the disk until another 'Sync Character' is detected (Sync 2) for Read and Write Verify commands.

2. Only 'Sync 1' is detected for a Write command. 'Sync 2' is written prior to the data field during a Write command.

DATA FIELD (SYNC 2)

The 'Sync Character' allows the 'Bit Counter' to be incremented by the disk's 'READ CLOCKS' and thereby read the data field for Read and Write Verify commands.

The reset is removed from the 'SCD' Flop (L56-5) via the Resync Allow Circuit L14-9, L14-5 clocking Read Command Stored Flop L12-9/low (L27-2/low), resetting the 'ISS' Flop (L67-8).

The 'Sync Character Detected' Flop (L56-5) is now enabled to detect the 'Sync 2' character. When the character is detected, the 'SCD' Flop (L56-5) will latch-up and allow the disk's read clocks to the Bit Counter.

The 'SCD' Flop (L56-5) will not be reset until the end of the read command via $\overline{\text{SINPT}}$ - i.e., 'ISS' Flop (L67-8) is held in reset via term DOS (Data Order Stored/low).

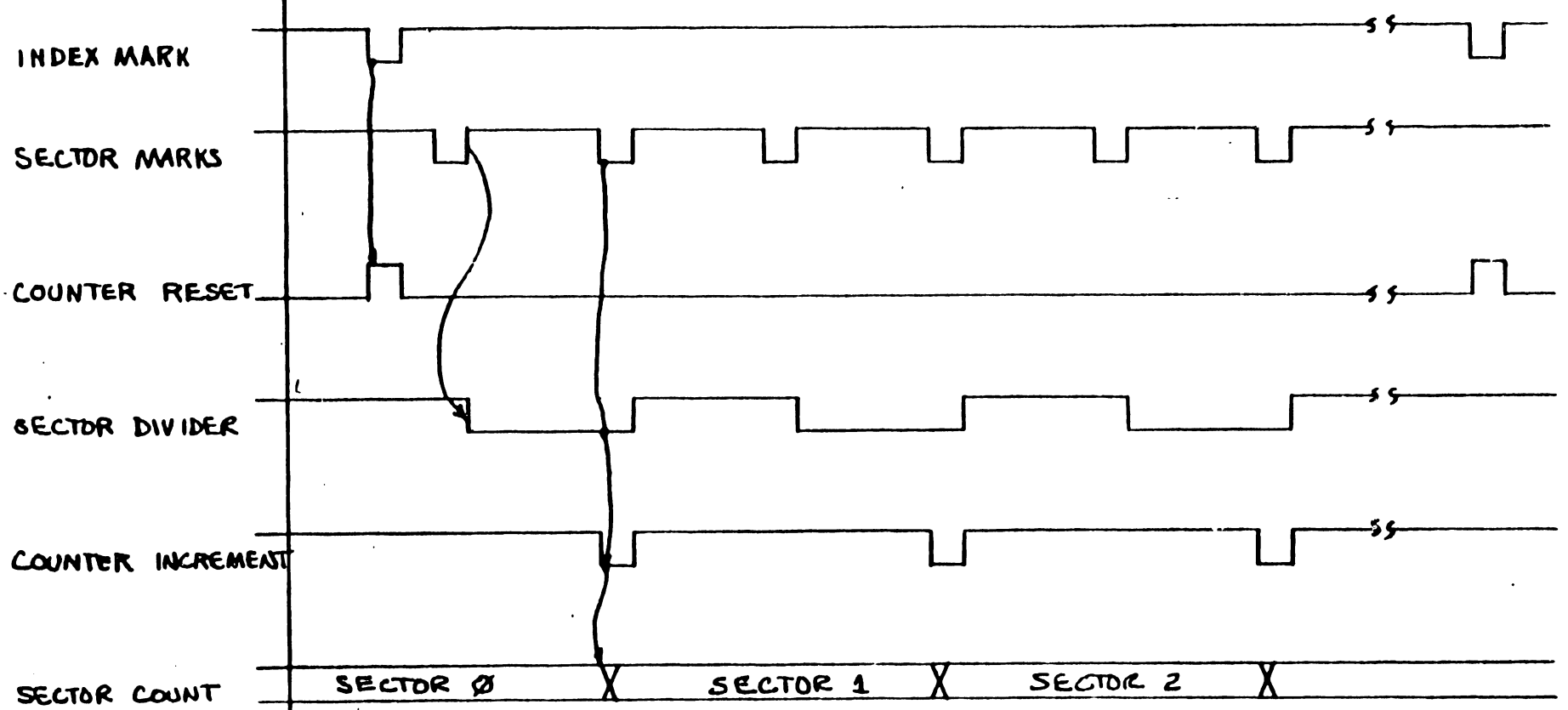
For further information see the Instruction Operation section of this manual (3.0).

- SECTOR COUNTER -

The floppy disk drive does not provide the interface with a sector count like the Diablo. Therefore, it becomes necessary to develop a count from the incoming index and sector pulses.

The floppy disk normally uses a 32 sector, 128 byte/sector format. To make the interface compatible with both the floppy and the hard disk, it is necessary to increase the number of bytes/sector to 256, this is accomplished by ignoring every other sector mark. Thus, to the interface, the floppy disk has 16 sectors with a capacity of 256 bytes/sector. The timing diagram below illustrates sector counter operation.

FLOPPY DISK SECTOR COUNTER



NOTE: IF COUNTER OR SECTOR DIVIDER SHOULD BE COME NONSYNCHRONIZED, BOTH WILL BE RESET WITH THE NEXT INDEX MARK.

CIRCUIT OPERATION

The sector counter is designed so it is reset every revolution by index mark. That means that within one revolution after power is stable, during a power up, the sector counter will by synchronized, and should it become non-synchronized, the next index mark will reset the counter causing resynchronization.

Operational description begins with the occurance of an index mark which:

1. Resets the sector counter (L-8).
2. Presets the sector divider (L-74).

The next sector mark that occurs will be ignored in view of the fact that L72 pin 2 is high disabling that gate. The trailing edge of sector pulse clocks L74 reset, this preconditions the circuit to accept the next sector mark and allow the counter to be incremented. The trailing edge of the second sector mark clocks the sector divider (L74) set again, preconditioning the circuit to ignore the next sector pulse. This sequence of counting every other sector mark continues until an index mark occurs resetting the counter to zero, at which time the cycle begins again. If the floppy disk is selected ($\overline{FDS}$=low) the sector count is gated through L2 along with Sector Pulse Present ($\overline{SPP}$, L1-8) and presented to the BSR multiplexer. If the hard disk is selected the sector count and sector pulse are provided by the drive.

- DIRECT MEMORY ACCESS (DMA) -

Direct Memory Access is a method of transferring data to and from Main Memory (MM) without the MP's intervention - i.e., the memory transfer is not controlled by the MP (microcode) in any way.

The device adapter board controls all the memory transfers by its hardware, to increase the data transfer rate by requesting 'MM' at the appropriate time. The disk DA makes memory requests every time the 'BSR' is full/empty - i.e., once for every 16 counts (bits). A memory request is made every 6.4 μs for the hard disk and every 64 μs for the floppy disk.

The 'MP starts the memory operation by issuing a surface operation command to the 'DA'. The 'MP' then waits looking for the 'Input Bit' from the device adapter signalling that the required operation and appropriate memory transfers have been performed. At this time, the 'MP' is again in control of the 'MMBI'.

Following is a schematic and description of the 'DMA' portion of the 'DA'.

CIRCUIT OPERATION

The 'DMA' portion of the 'DA' consists primarily of two flops; 'Hardware Read 16' ($\overline{HR16}$) and 'Hardware Write 16' ($\overline{HW16}$) at locations L63-8 and L63-13 respectively.

HARDWARE READ 16 ($\overline{HR16}$)

The disk 'DA', upon receipt of a Disk Write command, sets the $\overline{HR16}$ flop (L63-8) on 16 bit 'BSR' boundaries.

The 'DA' writes 16 bits onto the disk media (half word) per 'MM' transfer. Data must be ready prior to the actual write operation, therefore, the 'MM' is read (requested) each time the 'BSR' starts shifting data to the disk.

The controlling gate for read requests is L41-6. This gate clocks the $\overline{HR16}$ flop (L63-8) at 'ACK' time (L41-5), Write Memory Read Request Allow (WMR) felt at L41-3, and stepped into sixteen time L41-4 (L67-5). The $\overline{HR16}$ flop will remain active (low) until it is reset via L75-10 ($\overline{INC2}$).

$\overline{INC2}$ is the second ripple pulse to the MP's 'MAR'. At this time '$\overline{INC2}$', the memory transfer has been completed and set up for the next transfer has begun.

The first memory request during a write operation is made via L47-8 (L56-9). It is necessary to provide the first request via L56-9 and 'WGT' (Write Gate Time) due to the inactivity of 'WMR' flop (L23-5) prior to the first write onto the disk.

The disk 'DA', upon receipt of a disk 'Write Verify' command, sets the '$\overline{HR16}$' flop (L63-8) on 16 bit boundaries as does the 'Write Command'. However, the '$\overline{HR16}$' flop is clocked via L28-11 (allow verify memory requests and 'SOS' (stepped out of 16).

HARDWARE WRITE 16 ($\overline{HW16}$)

The disk 'DA' upon receipt of a disk 'Read' command, set the '$\overline{HW16}$' flop (L63-13) on 16 bit 'BSR' boundaries.

The 'BSR' reads 16 bits from the disk media (half word) per 'MM' transfer. The serial data is read from the disk bit-by-bit and shifted into the 'BSR' via the disk's '$\overline{READ\ CLOCKS}$'. The 'BSR', upon receiving 16 bits, makes a 'MM' request ($\overline{HW16}$) via L20-9 (allow memory requests/ read), 'SIS' (stepped into 16/L67-5) and 'SDR' (Shift Data Read/L43-3) forcing L31-6 low. L31-6 is felt at '$\overline{HW16}$' flop L63-1 clocking the flop active (L63-13/low).

The '$\overline{HW16}$' flop is reset via '$\overline{INC2}$' in the same manner as the '$\overline{HR16}$' flop was reset.

1. Both memory requests cause a 'MM' transfer to/from the MP's 'MDR' register (see MP Manual Section 3/2/0).

2. For further description and timing relationship, see the Instruction Operation section of this manual (3.0).

- CYCLIC REDUNDANCY CHECK (CRC) -

The purpose of the 'CRC' is to verify the data read from disk is correct.

During a 'Disk Write' operation, a two byte (16 bit) 'CRC' check character is computed and written onto the disk media directly after the 256 byte data field.

During a 'Disk Read' operation, the data being read from the disk media is passed through the 'CRC' circuit, and a 'CRC' check character is computed. The 'CRC' check character, after the data field, is also read from the disk and passed to the 'CRC' circuit where it will cancel the check character computed by the 'Disk Read' operation.

The 'CRC' circuit will report an error for the Disk Read if the 'CRC' check character (from disk) did not cancel the computed check character during the 'Disk Read' operation. The error condition will set the 'CRC Error' flop in the Operational Status Error Flag section (2.8).

CIRCUIT OPERATION

The 'CRC' circuit utilizes a 'CRC' integrated circuit (Device Type 9401). For the device operation, please refer to its data sheet - 'Fairchild Macrologic *9401 CRC Generator/Checker'.

WRITE OPERATION

During a Disk Write, the data (from the 'BSR') is felt at the input of the 'CRC' device (L32) via term 'DO' (Data Out) L44-1 gated with term 'WGA' (Write Gate Allow/L44-2), and passed to 'CRC' L32-11 through 'OR' L44-6. This data is then clocked into L32 via L36-12 through 'OR' L24-12.

Term 'ACC' (Allow Cyclic Check) is used to control the 'CRC' device and clock steering to the device.

$\overline{\text{ACC}}$ (High) = Load 'CRC' Device
$\overline{\text{ACC}}$ (Low) = Shift Out 'CRC' Check Character

Term '$\overline{\text{ACC}}$' will go low at the end of the data field to allow the 'CRC' check character to be shifted to the disk via clock input L46-8 through 'OR' L24-12. '$\overline{\text{ACC}}$' is felt at L32-10 controlling the 'CRC' device.

Term '$\overline{\text{SHC}}$' (Strobe Header Check) clears the 'CRC' device (L32) just prior to the data field.

READ OPERATION

During a Disk Read, the data (from the disk) is felt at the input of the 'CRC' device (L32) via term 'RDI' (Read Data In) L44-12 gated with term 'RGA' (Read Gate Allow/L44-13), and passed to 'CRC' L32-11 through 'OR' L44-6. This data is then clocked into L32 via term 'SDR' (Shift Data Read) at L24-2.

*A trademark of 'Fairchild Camera and Instrument Corporation'.

The entire 256 byte sector is passed to the 'CRC' device (L32) and a check character is computed. The check character trailing the data field is also shifted in cancelling the computed 'CRC' check character computed during the read. L32-13 will go high signalling an error, if it has occurred.

- OPERATIONAL STATUS ERROR FLAGS & OPERATION TERMINATION -

ERROR STATUS FLAGS

There are five Operational Error Status Flags:

1. Header Error
2. CRC Error
3. Write Verify Error
4. Sector Overrun Error
5. Memory Overrun Error

There are, in addition, two 'MM' error conditions reported by the 'DMA' memory operation:

6. 'MM' Parity Error (MMP)
7. 'MM' Illegal Memory Address Error (IMA)

In the event of any error condition being sensed, an immediate termination of the surface operation is executed via the input bit ($\overline{\text{SINPT}}$). This is done to prevent destruction of data in the 'MM' or on the disk media (CRC Error excepted).

OPERATION TERMINATION

There are three normal operation terminations:

1. $\overline{\text{EOR}}$ = End of Read & Write Verify
2. $\overline{\text{EOW}}$ = End of Write
3. $\overline{\text{EOF}}$ = End of Format

Each of these signals will set the input bit ($\overline{\text{SINPT}}$).

ERROR STATUS FLAGS

1. Header Error:

The 'Header Error Flop', L51-5 samples the header read from disk (BSR) and the header in the MP's 'MDR' register via comparator [L57, L58, L59 and L60]. The comparison (High = Good) is felt at L51-2 'DCP' and clocked by term 'SHC' (Strobe Header Check/L65-7) felt at L51-3. L51-5 will go low signalling a Header Error and will terminate the surface operation via L40-1.

2. CRC Error:

The 'CRC Error Flop', L50-9, samples the error pin on the 'CRC' device L32-13 (High = Error). The 'CRC Error Flop' is clocked via term 'SRT' (Set Read Termination/L20-6) felt at L50-11. L50-9 will go high signalling a 'CRC' Error, however this error conditions does not terminate the surface operation (no input bit) due to the non-destructive nature of the error.

3. Write Verify Error:

The 'Write Verify Error Flop', L50-5, samples the data read from disk (BSR) and the data in the MP's 'MDR' register via comparator [L57, L58, L59 and L60]. The comparison (High = Good) is felt at L50-2 'DCP' and clocked by [SDR (Shift Data Read) . SIS (Stepped Into 16)] felt at L50-3. L50-5 will go low signalling a 'Write Verify' error and will terminate the surface operation via L40-2.

4. Sector Overrun Error:

The 'Sector Overrun' flop L49-9, samples 'RGA' (Read Gate Allow) and 'WGA' (Write Gate Allow) felt at L49-12. If either signal is active (high) when a sector is entered, a Sector Overrun condition exists - i.e., the surface operation should have been completed prior to entering a new sector.

Term 'SPP' (Sector Pulse Present) clocks the 'Sector Overrun' flop via L49-11. L49-8 will go low signalling a Sector Overrun Error and will terminate the surface operation via L40-3.

5. Memory Overrun Error:

The 'Memory Overrun' flop, L51-9, samples both memory request signals, '$\overline{\text{HW16}}$' and '$\overline{\text{HR16}}$' for activity (Low = Active) at the moment a new request is requested - i.e., the previous request, if it was not serviced by 'MM', will indicate that 'MM' was unable to respond in time and that the data in the MP's 'MDR' register is invalid. The 'Memory Overrun' flop is clocked via term '$\overline{\text{SHW}}$' (Set Write Request) or term '$\overline{\text{SRR}}$' (Set Read Request) felt at L51-11. L51-8 goes low signalling a Memory Overrun Error and will terminate the surface operation via L40-12.

6&7. 'MM' Parity Error (MMP) & 'MM' Illegal Memory Address Error:

These two errors are a function of the 'MM' and are reported to the 'MP' board where they are stored. The 'MP' transfers these error conditions to the 'DA' via terms 'HSB1' (Hardware Status Bit One/$\overline{\text{MMP}}$) and 'HSB2' (Hardware Status Bit Two/$\overline{\text{IMA}}$). HSB1 and HSB2 are active high.

These terms are felt at the 'BSR' Input Multiplexer' L71-5 (HSB1) and L70-11 (HSB2) for transfer to the MP's 'MDR' register. Term '$\overline{\text{HTS}}$' (Hardware Transfer Stop) signals to the 'DA' that 'HSB1' or 'HSB2' is active and terminates the surface operation via L40-11. $\overline{\text{HTS}}$ is from the 'MP' Memory Bus Interface Logic.

All of these error flags are reset via a 'Give Operational Status' command decoded by L64-6 or $\overline{\text{INIT2}}$. 'Give Operational Status' command is issued after every surface operation command.

Operation Termination:

The normal operation termination is decoded off the 'BSR' and felt on L40 via terms: $\overline{\text{EOF}}$ (End of Format) = L40-6, EOR (End of Read/Write Verify) = L39-4&5, and $\overline{\text{EOW}}$ (End of Write) = L40-5.

Miscellaneous Termination:

If a surface operation is requested, and a sector pulse is present, the surface operation will be terminated via L39-2 (SPP) and L39-3 ($\overline{\text{SOP}}$). Initialize will also terminate any surface operation.

- FLOPPY DISK TIMER -

The purpose of the 'Floppy Disk Timer' (L53-7) is to provide a time delay after certain floppy disk commands are issued - i.e., the floppy disk requires settling time after certain commands are issued due to the floppy disk not reporting an inoperable condition. These commands are:

- Seek
- Head Load/Unload

Although these commands require a settling time, a separate command is used to start the timer - i.e., the 'Start Timer' command. The timer is retriggerable and has a time of 12.65 ms.

CIRCUIT DESCRIPTION

The timer is a one-shot (9602) at location L53-7. It is triggered via L41-12 and allowed to the MDR via term 'FDS' (Floppy Disk Select) at L5-10 and then through the 'BSR' multiplexer channel - C0 at L69-6.

- TERMINATOR VOLTAGE & PROTECT -

TERMINATOR VOLTAGE

The terminator (mounted on the Diablo 10-Meg Disk) must be supplied with +5V in the event the Diablo power is off.

+5V is supplied to the terminator through diode A15F felt at pins 48_2 and 49_2 of the DLI.

PROTECT

In the event of a power failure or any voltage failure, the disk media must be protected from false data writes, etc. The power supply monitors all of its voltages (system supply) and issues a System Initialize if they become out of tolerance.

This System Initialize is felt at pin 13, on the 'DAI' and removes the bias on both Write Gate and Erase Gate transistors on the 'DA'.

-INSTRUCTION OPERATION -

- HARD DISK -

The Diablo* Systems Incorporated Series 40 Disk Drive Model 44 (10 Megabyte) is presently being used.

Please refer to Diablo Systems Incorporated Series 40 Disk Drive Maintenance Manual (Model 44) for service requirements and procedures.

*'Diablo' is a trademark of Diablo Systems Incorporated.

-FLOPPY DISK -

The Shugart Associates Model 901 Diskette Storage Drive is presently being used.

Please refer to Shugart Associates Diskette Storage Drive Manual SA900/901. SA900/901 Maintenance Manual may be found in Wang Laboratories Service Bulletin No. 46.2.

LEAVE IN	REMOVE
A	B
R	DS

JUMPER L13 TO 3A AND 5&6

FAIRCHILD MACROLOGIC* • 9401
CRC GENERATOR/CHECKER

Description The 9401 Cyclic Redundancy Check (CRC) Generator/Checker provides an advanced tool for the implementation of the most widely used error detection scheme in serial digital data handling systems. A 3-bit control input selects one of eight generator polynomials. The list of polynominals includes CRC-16 and CRC-CCITT as well as their reciprocals (reverse polynomials). Automatic right justification is incorporated for polynomials of degree less than 16. Individual clear and preset inputs are provided for floppy disc and other applications. The ERROR output indicates whether or not a transmission error has occured. Another control input inhibits feedback during check word transmission. The 9401 is a member of Fairchild's Macrologic family and is fully compatible with all TTL families.

Typical Applications

- Floppy and other disc storage systems.
- Digital cassette & cartridge systems.
- Data communication systems.

Features

- Guaranteed 12 MHz data rate.
- 8 selectable polynomials.
- Error indicator.
- Separate Preset & Clear controls.
- Automatic right justification.
- Fully compatible with all TTL logic families.
- 14-pin package.

*A Trademark of Fairchild Camera and Instrument Corporation

LEAD NAMES		Loading (note a) HIGH (U.L.)	LOW (U.L.)
S_0, S_1, S_2	Polynomial Select Inputs	0.5	.23
D	Data Input	0.5	.23
$\overline{CP}$	Clock (operates on HIGH to LOW transition) Input	0.5	.23
$\overline{CWE}$	Check Word Enable (active LOW) input	0.5	.23
$\overline{P}$	Preset (active LOW) input	0.5	.23
MR	Master Reset (active HIGH) input	0.5	.23
Q	Data Output	10	5 (note b)
ER	Error (active HIGH) output	10	5 (note b)

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) temperature Ranges.

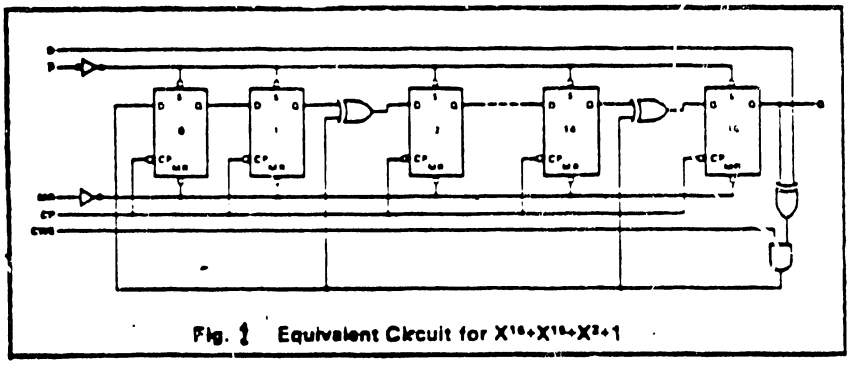
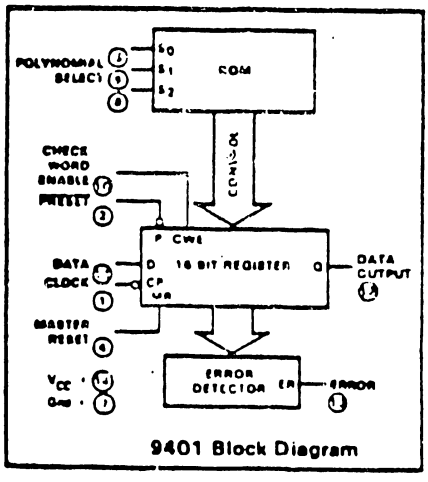
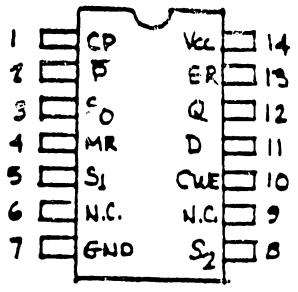


Fig. 1 Equivalent Circuit for $X^{16}+X^{15}+X^{2}+1$



9401 Block Diagram



CONNECTION DIAGRAM (TOP VIEW)

LEADS 6, 9 NOT CONNECTED

Functional Description - The 9401 Cyclic Redundancy Check (CRC) Generator/Checker is a 16-Bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 9401 implements the polynomials listed in Table I by applying the appropriate logic levels to the select pins S_0, S_1 & S_2.

The 9401 consists of a 16-bit register, a Read-Only-Memory (ROM) and associated control circuitry as shown in the Block Diagram. The polynomial control code presented at inputs S_0, S_1, and S_2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data (D) input, using the HIGH to LOW transition of the Clock ($\overline{CP}$) input. This data is gated with the most significant output (Q) of the register, and controls the Exclusive OR gates (Figure 1). The Check Word Enable ($\overline{CWE}$) must be held HIGH while the data is being entered. After the last data bit is entered, the $\overline{CWE}$ is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating (Figure 2).

To check an incoming message for errors, both the data and check bits are entered through the D input with the $\overline{CWE}$ input held High. The 9401 is not in the data path, but only monitors the message. The Error output becomes valid after the last check bit has been entered into the 9401 by a HIGH to LOW transition of $\overline{CP}$. If no detectable errors have occured during the data transmission, the resultant internal register bits are all LOW and the Error output (ER) is LOW. If a detectable error has occured, ER is HIGH. ER remains valid until the next HIGH to LOW transition of $\overline{CP}$ or until the device has been Preset or Reset.

A HIGH level on the Master Reset (MR) input asynchronously clears the register. A LOW level on the Preset ($\overline{P}$) input asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

TABLE I

SELECT CODE S_2	S_1	S_0	POLYNOMIAL	REMARKS
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

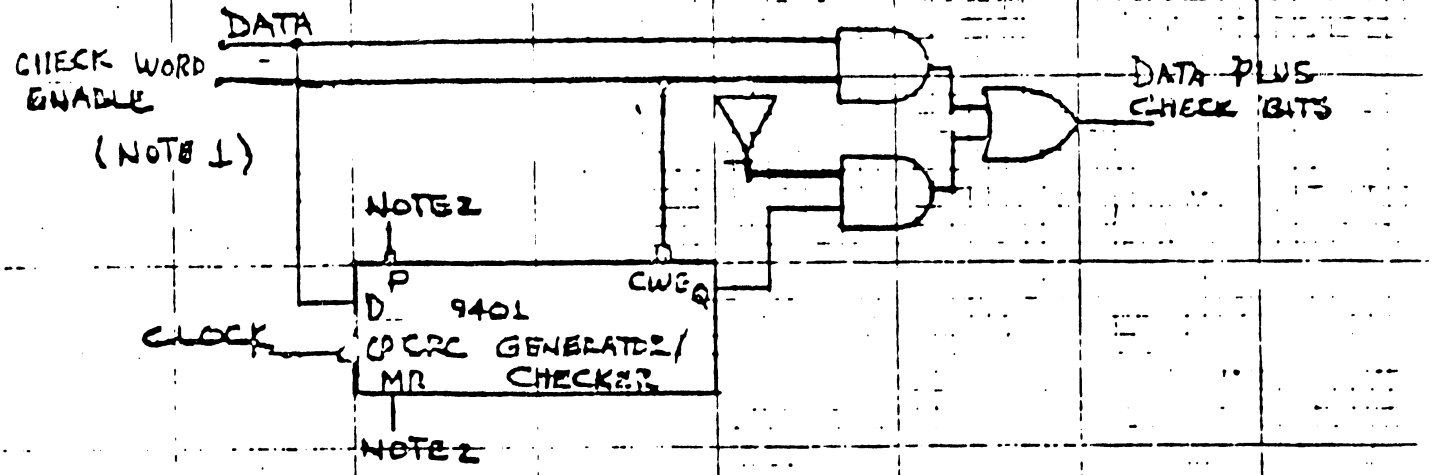
RECOMMENDED OPERATING CONDITIONS

PARAMETER	9401 XM			9401 XC			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	V
Operating Free Air Temperature Range	−55	25	125	0	25	75	°C

X = package type; D for Ceramic Dip, P for Plastic Dip.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA
		XC	2.7	3.4			
V_{OL}	Output LOW Voltage	XM&XC		0.35	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
		XC		0.45	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
	Input HIGH Current			1.0	20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−10		−42	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			70		mA	V_{CC} = MAX, INPUTS OPEN



NOTES

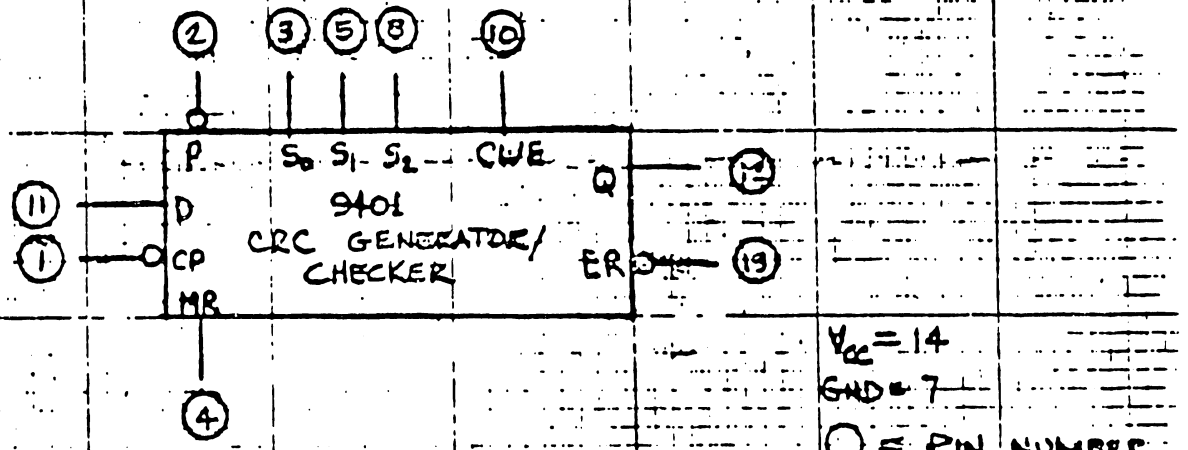
1. CHECK WORD ENABLE IS HIGH WHILE DATA IS BEING CLOCKED, LOW DURING TRANSMISSION OF CHECK BITS

2. 9401 MUST BE RESET OR PRESET BEFORE EACH COMPUTATION

FIGURE 2

CRC CHECK BITS ARE GENERATED AND APPENDED TO DATA BITS

LOGIC SYMBOL



Switching Characteristics (T_A = 25°C, V_{CC} = 5.0V)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP (note 2)	LIMITS MAX	UNITS	CONDITIONS	
f_{max}	Maximum Clock Frequency	12	20		MHz	Fig.3, 4,5	C_L = 15 pF
t_{PHL} t_{PLH}	Propagation delay, Clock,MR to Data Output		30	55	ns		
t_{PHL} t_{PLH}	Propagation delay, Preset to Data Output		40	60			
t_{PHL} t_{PLH}	Propagation delay,Clock,MR or Preset to Error Output		40	60	ns		

Switching Set-up Requirements (T_A = 25°C, V_{CC} = 5.0V)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS	
t_wCP (L)	Clock pulse width (LOW)	35			ns	Fig.2	C_L = 15 pF
t_sD	Set-up time, Data to Clock		35	55	ns	Fig. 6	
t_sCWE	Set-up time, CWE to Clock		35	55	ns		
t_h	Hold time, Data and CWE to Clock		0		ns		
t_wP (L)	Preset pulse width (LOW)	35	25		ns	Fig.4	
t_wMR (H)	Master Reset pulse width (HIGH)	35	25		ns	Fig.6	
t_{rec}	Recovery time, MR and Preset to Clock		25	35	ns	Fig.4,5	

Notes:

1. For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC}=5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

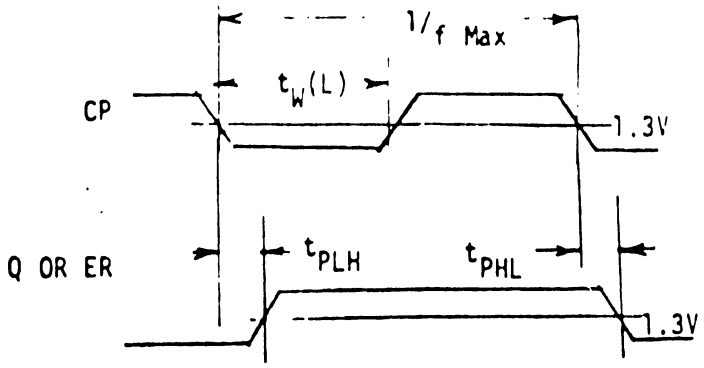


Fig. 3

PROPAGATION DELAYS, CLOCK TO Q AND CLOCK TO ER

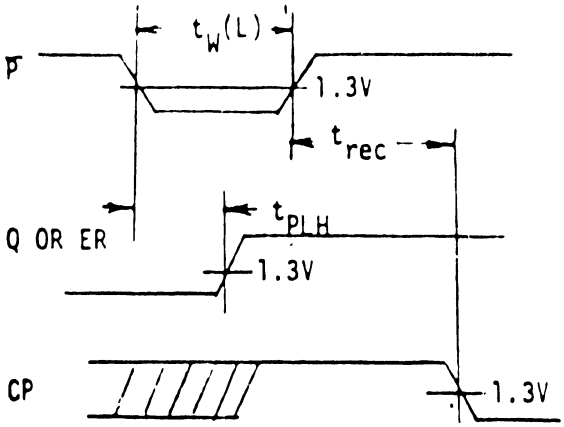


Fig. 4

PROPAGATION DELAYS, $\overline{P}$ TO Q AND ER, PLUS RECOVERY TIME $\overline{P}$ TO CP

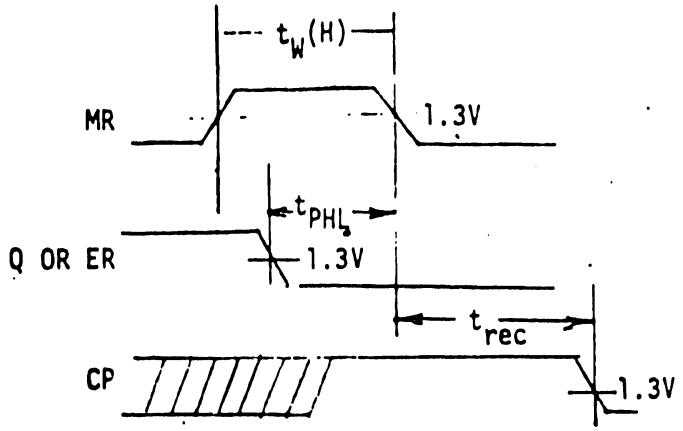


Fig. 5

PROPAGATION DELAYS, MR TO Q AND ER PLUS RECOVERY TIME, MR TO CP

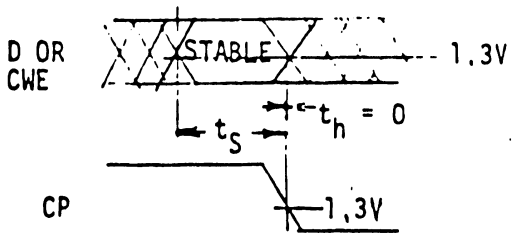
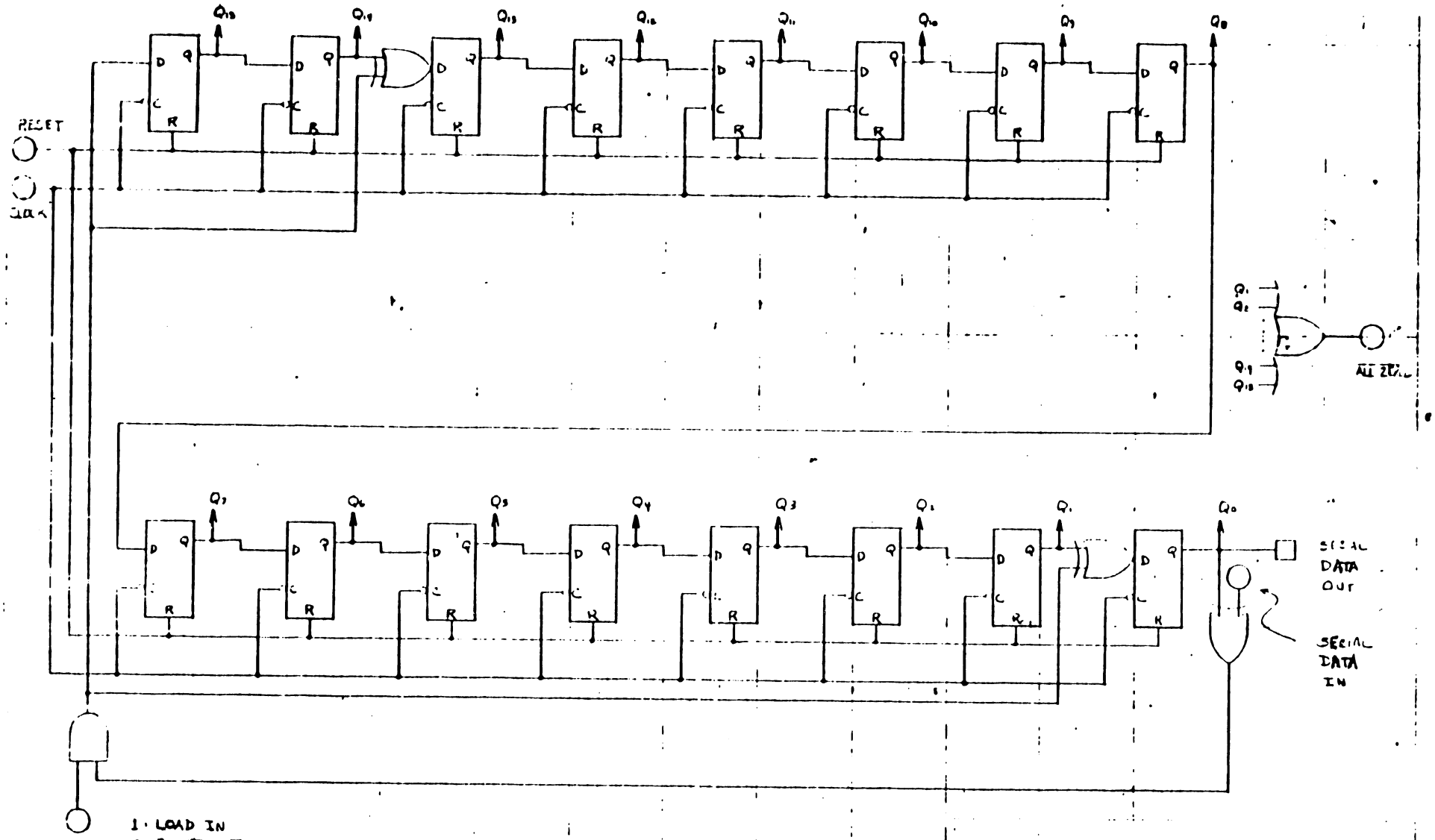


Fig. 6

SET-UP AND HOLD TIMES, DATA TO CLOCK AND CWE TO CLOCK


RESET
CLOCK
SERIAL DATA OUT
SERIAL DATA IN
1 : LOAD IN
0 : SHIFT OUT
$X^{16} + X^{15} + X^2 + 1$

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