WESTERN DIGITAL

WD83C593
LAN ADAPTER BUS INTERFACE CONTROLLER FOR IBM PS/2 WITH MICRO CHANNEL*

ENGINEERING SPECIFICATION

Revision X1

January, 1989

ADVANCE INFORMATION

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1. FEATURES (83C593 Microchannel Interface Controller)

-84 pin ASIC, 2 micron tech. CMOS

-Single power supply +5v

- Interfaces to IBM microchannel as a non-DMA slave

- Interfaces to 8390 NIC, BIOS ROM, Buffer RAM ===on 8003x/A board
  OR
  Interfaces to another master (V50 processor),BIOS ROM==on 8023x/A board

- When used on 8003x/A board, the buffer RAM is used as shared memory

- When used on 8023x/A board, the on board 14x16 FIFO will be used for data transfer. The[2] PS/2 will communicate with the FIFO using I/O String, and the V50 will use one of its DMA channels.

- Four programmable Option Select registers, to conform to IBM Micro Channel Specs

- 10 EEPROM registers (Lan Adress, POS ID)

- External MODE SELECT pin (8003x/A vs 8023x/A application)

- Testable/programmable before and/or after assembly

- Four VCC and Four GROUND pins are provided

- Four program selectable IRQ pins are provided

- Programmable RAM size (16KB,64KB)

- Programmable BIOS ROM size (16KB,32KB,64KB)

*** 8003x/A is a non intelligent Ethernet(x=E) or Starlan(x=S) card
*** 8023x/A is an intelligent Ethernet(x=E) or Starlan(x=S) card

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[2] PS/2 is a trademark of IBM Corporation

2. PIN DESCRIPTIONS

In the case of multiplexed signals of the form AAA/BBBB, the current description is of the UNDERLINED portion

PIN	NAME	DESCRIPTION
	PS/2 BUS SIGNALS	
15-20 23-38	LA00-LA21 (I)	PS/2 ADRESS LINES These are the 20 bits of the PS/2 adress lines
2-10 77-83	BD00-BD15 (I/O)	BUFFERED PS/2 DATA BUS D0-D15 out of the PS/2 are buffered external
71	-ADL (I)	ADRESS DECODE LATCH This input is used to indicate that the microchannel addresses are to be latched. The trailing edge is used.
40	-CDDS16 (O)	CARD DATA SIZE 16 This output is used to indicate to the PS/ that the current data transfer is 16 bits wide It is derived from a valid adress decode.
72	MADE24 (I)	MEMORY ADRESS ENABLE 24 This input when active indicates that an unextended adress space less than or equal to 16M is being presented on the adress bus.
75	M/-IO (I)	MEMORY /-INPUT OUTPUT This input distinguishes a memory cycle from an I/O cycle
11	-REFRESH/VPPOUT	REFRESH CYCLE

74,73 -S0,-S1 (I)

STATUS BITS 0 AND 1

These inputs indicate the start of a channel cycle and also define the type of channel cycle.

M/-IO	-S0	-S1	FUNCTION
0	0	0	Reserved A
0	0	1	IO Write
0	1	0	IO Read
0	1	1	Reserved B
1	0	0	Reserved C
1	0	1	Memory Write
1	1	0	Memory Read
1	1	1	Reserved D

50 -CMD (I)

COMMAND

This input is used to define when the data is valid on the data bus. The trailing edge of this signal indicates the end of the bus cycle

41 -CDSFDBK (O)

CARD SELECTED FEEDBACK

This output is asserted as an acknowledgement when an I/O or Memory device on the LAN card is selected.

39 CDCHRDY (O)

CHANNEL READY

This output, normally active, is pulled inactive to allow additional time to complete a channel operation. The maximum time that this line can be held inactive is 3.5 microseconds.

45-48 -IRQ0-3 (O)

INTERRUPT REQUEST

These outputs are used to signal the host microprocessor that attention is needed by the LAN card.

68 -CDSETUP (I)

CARD SETUP

This input is generated by the host logic to individually select channel connectors during system configuration and error recovery procedures. This input together with LA0-LA2 is used to access the configuration registers. -CDSFDBK output is not asserted during configuration.

67 CHRESET (I)

CHANNEL RESET

This signal is generated by the host at power up power failure, or under software control.

LAN CONTROLLER SIGNALS (8003x/A)

70	INT/AINT (I)	LAN INTERRUPT This input indicates that the NIC needs host's attention. (End of operation, error etc.)
56	BREQ/ABACK (I)	LAN BUS REQUEST This input is generated by the NIC to indicate that a DMA transfer is needed. It is automatically generated when the NIC FIFO need servicing.
55	BACK/ABREQ (O)	LAN BUS ACKNOWLEDGE This output is generated as an acknowledgement of the LAN BUS REQUEST.
61	-RST/AA00 (O)	LAN RESET Places the LAN in reset mode immediately.No packets are received or transmitted by the LAN until STA bit in the lan is set.
60	-IOR/AA01 (O)	LAN I/O READ This output together with -LANCS, is used to read the internal LAN registers.
59	-IOW/AA02 (O)	LAN I/O WRITE This output together with -LANCS, is used to write into the internal LAN registers.
62	-LANCS/-ACS (O)	LAN CHIP SELECT This output places the LAN chip in slave mode for access to internal registers.
58	-ACK/AA03 (I)	LAN SLAVE I/O ACKNOWLEDGE This input is asserted by the LAN chip when it grants access to its internal registers. It is used to insert wait states until LAN is synchronized for a register read or write operation.
76	BSCK (I)	CLOCK This input is the 40 MHz clock

EEPROM RELATED SIGNALS

11	REFRESH/VPPOUT (O)	EEPROM SERIAL OUTPUT This is an EEPROM serial test OUTput
52	DDIR/EE-SOUT (O)	EEPROM SERIAL OUTPUT This is an EEPROM serial test output
12	EE-TEST (I)	EEPROM TEST When 18 volts(dc) is applied to this pin, the chip is placed in an EEPROM test mode.
14	LA22/EE-CLK (I)	EEPROM CLOCK This input provides a clock for EEPROM testin
13	LA23/EE-STR (I)	EEPROM STROBE This input serves as an EEPROM test strobe

ALTERNATE MODE SIGNALS

69	MODE (I)	ALTERNATE MODE SELECT This input is used to multiplex between two modes. If left open (internally pulled high), it means that the 83C593 is being used on an 8003x/A board, interfacing the 8390 NIC and th buffer memory directly. If shorted to ground, it means that the 83C593 is being used on an 8023E board, interfacing the V50 microprocessor.
55	BACK/ABREQ (O)	ALTERNATE DMA REQUEST This output is to inform the DMA channel of the V50 processor that the host requests data transfer.
56	BREQ/ABACK (I)	ALTERNATE DMA ACKNOWLEDGE This input indicates that the V50 DMA channel has granted the bus for data transfer.
61	-RST/AA00 (I)	ALTERNATE ADRESS 00 Alternate adress lines AA00-AA04 are used by the V50 processor to access 83C593 internal registers.
60	-IOR/AA01 (I)	ALTERNATE ADRESS 01
59	-IOW/AA02 (I)	ALTERNATE ADRESS 02
58	-ACK/AA03 (I)	ALTERNATE ADRESS 03
66	-AIOW (I)	ALTERNATE I/O WRITE This input is used as an I/O write from the V50 processor.
63	-AIOR (I)	ALTERNATE I/O READ This input is used as an I/O read strobe from the V50 processor.

62	-LANCS/-ACS	(I)	ALTERNATE I/O CHIP SELECT This input is used as an I/O chip select from the V50 processor
53	-RAMOE/-AREADY	(O)	ALTERNATE READY This output is used as an I/O ready signal to the V50 processor. It is asserted when additional wait states are necessary
70	INT/AINT	(O)	ALTERNATE INTERRUPT This output is generated to attract the alternate processor's (V50) attention to a request made by the Host processor.
57	-ATC	(I)	ALTERNATE TERMINAL COUNT This input indicates that the alternate DMA Controller (V50) is finished transferring a packet. This is used to negate the ABREQ output.

RAM SIGNALS

53 -RAMOE/-AREADY (O) RAM OUTPUT ENABLE
This output is used to gate the buffer RAM onto the data bus BD00-BD15.

51 -RAMWE (O) RAM WRITE ENABLE
This output is used to write host data into the buffer RAM.

ROM SIGNAL

54 -BOE (O) BIOS ROM OUTPUT ENABLE
This output is the chip select for the bios ROM. It gates the data onto BD0-BD7

BUFFER CONTROL SIGNALS

52 -DDIR/EE-SOUT (O) DATA DIRECTION
This output is generated to control the direction of the external bidirectional buffers between the host data bus and DB00-DB15 (local data bus)

49 -DEN (O) DATA BUFFER ENABLE
This output is generated to enable or disable the external the bidirectional data buffers.

42 -MREQ (O) MEMORY REQUEST
This output is provided for use in a possible memory mapped scheme. Unlatched memory decode

POWER

21,43,64,84	VCC	+5V DC.
1,22,65,44	GND	GROUND

3.0 THEORY OF OPERATION

3.1 MODES OF OPERATION

This section will briefly discuss the operation of the two major modes that the 83C593 can assume. The selection between the modes is done using a separate pin called MODE. Leaving this pin open (internally pulled high) places the chip in a mode where it can be used on a non-intelligent slave board (8003x/A Mode). Shorting the MODE pin to ground will place the chip in a mode where it can be used on an intelligent slave board (8023x/A Mode)

3.1.1 8003x/A MODE:

In this mode the 83C593 interfaces the IBM Micro Channel as a non-DMA slave on one side and the 8390 NIC, BIOS ROM, and the BUFFER RAM on the other. The 83C593 satisfies all the necessary interfacing requirements of The IBM Micro Channel, does all the decoding for local I/O and memory spaces and generates all the necessary chip select control and handshake signals.

In the use of SHARED MEMORY the 83C593 will basically behave as an arbiter between The Host and the 8390 NIC for the BD00-BD15 data bus. During 8390 Local DMA bursts in and out of the Buffer RAM, it will isolate the BD data bus from the Micro Channel via external buffering and arm itself to deny any intervention by The Host during that time. It will negate the CDCHRDY in case of a valid decode. At other times the external buffers will be enabled so that The Host can do Memory or I/O cycles to anywhere on the card. The Host will use 16 bit wide MOVE STRING operation to transfer data to and from the Buffer RAM. During this time the 83C593 will generate the RAM control signals (Hi-Z during Local DMA).

3.1.2 8023x/A MODE

In this mode the 83C593 will interface the Micro Channel on one side and a processor (V50) on another. For data transfers, The Host will use the I/O STRING operation to communicate with the on board 14x16 FIFO while the V50 processor will use one of its DMA channels. The two sides will be time sharing the same data bus (BD00-BD15). On the Host side the handshake signal will be CDCHRDY and on the V50 side the handshake will be done through ABREQ, ABACK, AREADY.

If the V50 wants to read/write into the onboard 83C593 registers it will use the alternate adress and control signals (AA00-AA03, -AIOR, -AIOW, -ACS, -AREADY)

Example :
The V50 wants to send a packet to the PS/2.

PS/2 Action	V50 Action
(V50 interrupt has been enabled, all other interrupts are masked)	
	1-Prepare the DMA controller and write the code word to reg. 0x07
	2-Set VINT bit to generate an interrupt to the PS/2.
3-Read the VINT bit to verify the V50 interrupt. Reset VINT bit to clear the interrupt.	
4-Read reg. 0x07 and jump (in this case jump to "RECEIVE"	
RECEIVE 5-Set TOPS bit (data direction)	
6-Set ABREQ bit (DMA request)	
	7-Start the DMA to send the packet
8-Read and test NEMP bit NEMP=1 go to 8 NEMP=0 continue	
9-Set EIE bit (enable NEMP interrupt)	
10-Start or continue IO STRING read operation until NEMP interrupt comes.	
11-Mask NEMP Interrupt (by resetting the EIE bit). Is the packet received in full? YES = Go to 13 NO = Continue	
12-Read and Test the NEMP bit NEMP = 1 Go to 12 NEMP = 0 Go to 9	
13-Disable all interrupts except V50, and exit. (Reset EIL, EIE, EIF bits)	

3.2 POS REGISTERS AND DECODING

This section will briefly discuss what POS (Programmable Option Select) is and how the Space decodings will be achieved through POS registers.

3.2.1 POS REGISTERS

The microchannel architecture dictates the adapter card designers to use two READ ONLY ID BYTES and upto six READ/WRITE POS REGISTERs for the purposes of:

a-eliminating the use of switches and jumpers
b-permitting installation of multiple identical cards
c-positively identifying any card by slot
d-resolving resource assignment conflicts

The designer is also required to provide an Adapter Description File (.ADF) reporting the contents of the ID BYTES, how many POS REGISTERS used on the card and their purpose and contents, togetherwith possible alternate contents. The only bits architected by the Microchanel are

POS[2] bit 0.....Card enable (adress 102h)
POS[5] bit 7.....CH CK active indicator (105h)
POS[5] bit 6.....CH CK status available indicator (105h)

The rest of the POS REGISTERS are of freeform and can be used by the designer for Space Decodings, Arbitration Levels etc. After a Reset each adapter card must turn the Card Enable bit off, which in turn disables all the outputs from that card including interrupt request lines.

The central Configuration Software interrogates all slots independently for ID BYTES, uses the .ADF files provided to resolve conflicts and set up all the POS registers. It is ONLY during this time that the POS registers can be accessed, and only by The Configuration Software.

-CD SETUP (N) line together with the least significant three adress lines are used to decode for POS register and ID access.

3.2.2 DECODING (8003x/A Mode)

In this mode the MODE input will be left open, and the 83C593 POS ID Bytes will assume ;

PID1 msB =6Fh
PID0 lsB =C0h (for ethernet) or =C1h (for Starlan)

Three POS Registers will be used; POS[2], POS[3], POS[4] to decode for the card I/O Space, Shared Ram Space, and BIOS ROM Space respectively.

Conditions for I/O Space Decoding;
M/-IO.....LOW
LA12-LA15...ALL ZEROES

POS[2]

7	6	5	4	3	2	1	0
LA11	LA10	LA09	LA08	LA07	LA06	LA05	CDEN

If a 29h is written in POS[2], the 83C593 I/O space will be placed in the range 0280h-029F (this is one of128 possible 32 byte ranges) For each of the primary and alternate choices, one or more interrup levels will be defined in the .ADF file.

Conditions for Shared Ram Space Decoding:
M/-IO.....HIGH
LA20-LA23...ALL ZEROES

POS[3]

7	6	5	4	3	2	1	0
LA19	LA18	LA17	LA16	LA15	LA14	PME	CLAIM

If a C2h is written in POS[3], the Shared Ram Space will be placed in 0C0000h-0C3FFFh. This is one of 64 possible 16KB ranges. It is intended to place the Shared Ram in the general range of 0C0000h-0DFFFFh.

Conditions for BIOS ROM Space Decoding:
M/-IO.....HIGH
LA20-LA23...ALL ZEROES

POS[4]

7	6	5	4	3	2	1	0
LA19	LA18	LA17	LA16	LA15	LA14	BE1	BE0

If a D0h is written in POS[4], the BIOS ROM Space will be place in 0D0000h-0D3FFFh. This is one of 64 possible 16KB ranges. It is intended to place the BIOS ROM in the general range of 0C0000h-0DFFFFh.

3.2.3 DECODING (8023x/A Mode)

In this mode the MODE input will be grounded, and the 83C593 POS ID Bytes will assume ;

PID1 msB =XYh
PID0 lsB =PQh (for ethernet) or =PKh (for Starlan)

Two POS Registers will be used; POS[2], POS[4] to decode for the card I/O Space, and BIOS ROM Space respectively.

Conditions for I/O Space Decoding;
M/-IO.....LOW
LA12-LA15...ALL ZEROES

POS[2]

7	6	5	4	3	2	1	0
LA11	LA10	LA09	LA08	LA07	LA06	LA05	CDEN

If 29h is written in POS[2], the 83C593 I/O space will be placed in the range 0280h-029F (this is one of128 possible 32 byte ranges) For each of the primary and alternate choices, one or more interrup levels will be defined in the .ADF file.

Conditions for BIOS ROM Space Decoding:
M/-IO.....HIGH
LA20-LA23...ALL ZEROES

POS[4]

7	6	5	4	3	2	1	0
LA19	LA18	LA17	LA16	LA15	LA14	BE1	BE0

If a C0h is written in POS[4], the BIOS ROM Space will be placed in 0C0000h-0C3FFFh. This is one of 64 possible 16KB ranges. It is intended to place the BIOS ROM in the general range of 0C0000h-0DFFFFh.

3.2.4 OTHER POS FUNCTIONS

POS[5]

7	6	5	4	3	2	1	0
N/A	N/A	X	X	MSE	CDIV	IEN1	IEN0

Other than space decodings, some bits of the POS registers will be used for various functions:

CDEN- Card Enable (POS2 bit 0)
This bit wakes up low, and until it is set by the configuration routine it keeps the card in a sleep mode.

CLAIM- Claim bit (POS3 bit 0)
This bit is reserved (R/W) for use by the Driver software

PME- Memory Enabled (POS3 bit 1)
This bit wakes up low, and until it is set by the configuration routine it keeps the RAM Buffer disabled.

MSE- Memory Size Enable (POS5 Bit 3)
When set to 1 memory size increases from 8KX16 to 32KX16

CDIV- Clock Divider (POS5 bit 2)
This bit, when reset, divides the BSCK clock by 2 for internal use. The bit is cleared with hard reset.

BE0,BE1 -Bios Size/Enable bits (POS4 bit 0, bit 1)
The combination of these two bits are used to size the BIOS ROM and disable it when necessary, as follows:

BE1	BE0	FUNCTION
0	0	BIOS is 16KB
0	1	BIOS is 32KB
1	0	BIOS is DISABLED
1	1	BIOS is 64KB

IEN0-IEN1 Interrupt Enable bits (POS5 Bit 0, bit 1)
The combination of these bits enable/disable the interrupts to the host ,and decide on the level as follows:

IEN0	IEN1	FUNCTION
0	0	Interrupt level is IRQ0
1	0	Interrupt level is IRQ1
0	1	Interrupt level is IRQ2
1	1	Interrupt level is IRQ3

4.0 INTERNAL REGISTERS

4.1 I/O MAP

0x00	R/W	MEMORY ENABLE ,RESET REG.	(MER)
0x01	W	EEPROM CONTROL REGISTER	(EEC)
0x02	W	Reserved (PID0)	
0x03	W	Reserved (PID1)	
0x04	R/W	INTERRUPT CONTROL & STATUS	(ICS)
0x05	R/W	COMMUNICATION CONTROL REG	(CCR)
0x06	R/W	FIFO ENTRY-EXIT (16 BIT WIDE)	(FEX)
0x07	R/W	GENERAL PURPOSE REGISTER	(GPR)
0x08-0x0F	R	LAN ADRESS REGISTERS	(LAR)
0x10-0x1F	R/W	8390 NIC REGISTERS	(LAN)

4.1.1 MEMORY ENABLE, RESET REG. (MER)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit0
REST	MENB	n/a	n/a	n/a	n/a	n/a	n/a

Only bits 7 and 6 of this register are used. All bits are cleared with a HARD RESET.

Bit 7 (REST): Setting this bit and clearing it after 1us will reset the 8390 NIC and the rest of the registers except (LAR), (PID0), (PID1) and (FEX).

Bit 6 (MENB): Setting this bit enables the host PS/2 to share th on-board buffer RAM (8003). If cleared the RAM is disabled.

4.1.2 EEPROM CONTROL REGISTER (EEC) 0X01 W

This register is used only by Manufacturing to fix the values in the EEPROM register. After LARs, PID0 and PID1 are written an A5 is written into this register, and then the register is cleared (or some value other than A5H is written). At least 15 milliseconds must be allowed for the values to be stored in the non-volatile (EEPROM) registers.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	0	1	0	0	1	0	1

4.1.3 Reserved (PID0) 0x02 W
Reserved (PID1) 0x03 W

These two write only registers are used only by Manufacturing to set the Micro Channel POS ID numbers.

4.1.4 INTERRUPT CONTROL & STATUS (ICS) 0x04 R/W

This register is used in the alternate (8023) mode for exchanging interrupts between the PS/2 and the V50 (on board processor). Only SIX bits of this register are used and they are cleared at power up or soft reset.

bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7
--	--	EMPTY	FULL	AINT	NFLL	NEMP	VINT

bit2 (EMPTY): This bit is low when the internal FIFO is completely empty. When TOPS (of register 0x05) is low, it temporarily negates the ABREQ output to allow the FIFO be filled again.

bit3 (FULL): This bit is low when the internal FIFO is completely full. When the TOPS (of register 0x05) is high, it temporarily negates the ABREQ output to allow the FIFO to be emptied.

bit4 (AINT): PS/2 sets this bit to generate an interrupt to V50. The V50 reads this bit to verify the source of the interrupt it received (and clear it). This interrupt is intended to be used in conjunction with the general purpose register 0x07. PS/2 places a action code in reg. 0x07 for the V50 before setting the AINT bit

bit5 (NFLL): This bit is high when the internal FIFO is nearly full. It generates an interrupt to the PS/2 so that the IO Strin operation can be stopped before the FIFO overflows. Care should b taken not to write more than three more words after this interrup is asserted. This interrupt is enabled using the EIF bit (of reg 0x05) when the data flow is to be FROM the PS/2 (TOPS of reg 0x0 is low).

bit6 (NEMP): This bit is high when the internal FIFO is nearly empty. It generates an interrupt for the PS/2 so that the FIFO ca be filled before it gets totally empty. Care should be taken not to read more than three more words after this interrupt is asserted. The end of a packet can be detected by either monitorin the word count or allowing a maximum timeout period after the interrupt is detected (and then read three more words). This interrupt is enabled using the EIE bit when the data flow is to be TOWARDS the PS/2 (TOPS of reg 0x05 is high).

bit7 (VINT): V50 sets this bit to generate an interrupt to the PS/2. The PS/2 reads this bit to verify the source of the interrupt it received (and clear it). This interrupt is intended to be used in conjunction with the general purpose register 0x07 The V50 will place an action code for PS/2 in reg. 0x07 before setting the VINT bit.

4.1.5 INT. MASK & COMM.CONTROL REG. (IMCCR) 0X05 R/W

This register is used in both 8003 and 8023 modes. All bits of this register are cleared with a hard or soft reset. Bit 7 will also be cleared when the terminal count is reached by the V50 DM controller.

bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7
---	---	EIL	EIE	EIF	EIV	TOPS	ABREQ

bit 2 (EIL): This bit is used in the 8003 mode to enable or disable the interrupt from 8390 to the PS/2. The PS/2 has to set this bit to 1 to enable the interrupt.

bit 3 (EIE): This bit is used in the 8023 mode. The PS/2 sets this bit to enable the FIFO EMPTY interrupt before it starts reading the internal FIFO (and clears the EIL, EIF and EIV bits)

bit 4 (EIF): This bit is used in the 8023 mode. The PS/2 sets this bit to enable the FIFO FULL interrupt before it starts filling the internal FIFO (and clears the EIL, EIE and EIV bits)

bit 5 (EIV): This bit is used in the 8023 mode. The PS/2 sets this bit whenever it wants to be able to receive interrupts from the V50 processor(and clears the EIL, EIE, and EIF bits).

bit 6 (TOPS): This bit is used in the 8023 mode. It determines the direction of the data flow through the internal FIFO. If the bit is set the data flows towards PS/2, if it is cleared the dat flows towards V50.

bit 7 (ABREQ): This bit when set to 1 sends a DMA request to the V50 DMA controller. It stays set until there is a hard or soft reset, there is a terminal count signal from V50, or cleared by the PS/2. The PS/2 sets this bit as the last action before the data transfer actually starts in either direction. The bit is normally cleared by the terminal count (ATC) signal from the V5 DMA controller at the end of a packet transfer.

4.1.6 FIFO ENTRY-EXIT REGISTER (FEX) (0X06) R/W

This is a 16 bit wide I/O port used only in the alternate (8023) mode to fill or empty the contents of the internal FIFO. This register can not be used in the non-intelligent (8003) mode.

4.1.7 GENERAL PURPOSE REGISTER (GPR) (0X07) R/W

This is an 8 bit general purpose register. It is accessible in both modes. Together with the interrupts, this register can be utilized for exchanging messages between the host and the alternate processor (V50).

4.1.8 LAN ADDRESS REGISTERS (LAR) (0X08-0X0F) R

These are 8 read only registers backed by the internal EEPROM.

4.1.9 8390 REGISTERS (LAN) (0X10-0X1F)

These 16 registers are physically located in the National 8390 LAN Controller chip. Only the decode and the control circuitry for these registers are internal to the WD83C593.
For the functional definitions of these registers, refer to the National Semiconductors Specs.

5. ELECTRICAL CHARACTERISTICS & TIMING

5.1.1 DC PARAMETER CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I_{dd}	VDD Supply current		8	10	mA	
Vdd	Voltage Supply	4.5	5	5.5	V	
V_{ih}	Input High Voltage	2.0			V	
V_{il}	Input Low Voltage			0.8	V	
V_{oh}	Output High Voltage	2.4			V	note (1)
V_{ol}	Output Low Voltage			0.4	V	note (2)
I_{lh}	Input Source Current			1.0	uA	V_{in}=Vdd
I_{ll}	Input Sink Current			-1.0	uA	V_{in}=0
I_{ozh}	Tristate High Current	-10		10	uA	V_{in} =Vdd
I_{ozl}	Tristate Low Current	-10		10	uA	V_{in} =0
I_{pu}	Pull-up Current	-100		1000	uA	V_{in} =0
Vpp	HVS Vpp	15.5		19.0	V	note (3)

Note (1) I_{oh}= -24 mA on following pins:
IRQ0, IRQ1, IRQ2, IRQ3.
$I_{o}h$= -8mA on following pins:
All other outputs and I/O pins.

Note (2) I_{ol}= 24mA on following pins:
IRQ0, IRQ1, IRQ2, IRQ3.
I_{ol}= 8mA on the following pins:
All other outputs and I/O pins.

Note (3) A special test pattern is used to force REFRESH/VPP pin into th Vpp state.

5.1.2 NON-OPERATIONAL SPECIFICATIONS

Parameter	min	typ	max	unit
Storage temperature	-65		150	deg. C
Voltage on any pin with respect to VSS	-0.6		Vcc + 0.3 (except Vpp)	volts
Voltage on Vcc with respect to Vss			7.0	volts

5.2.2 OPERATIONAL SPECIFICATIONS

Parameter	min	typ	max	unit
Ambient temperature	0	25	70	Deg. C
Humidity	20		95	Percent
Vcc supply voltage with respect to Vss	4.50	5.0	5.50	Volts
Icc supply current (full loading)			100	milliamps
Power dissipation			500	milliwatts

5.2 TIMING DIAGRAMS

5.2.1 NON-INTELLIGENT (8003) TIMING

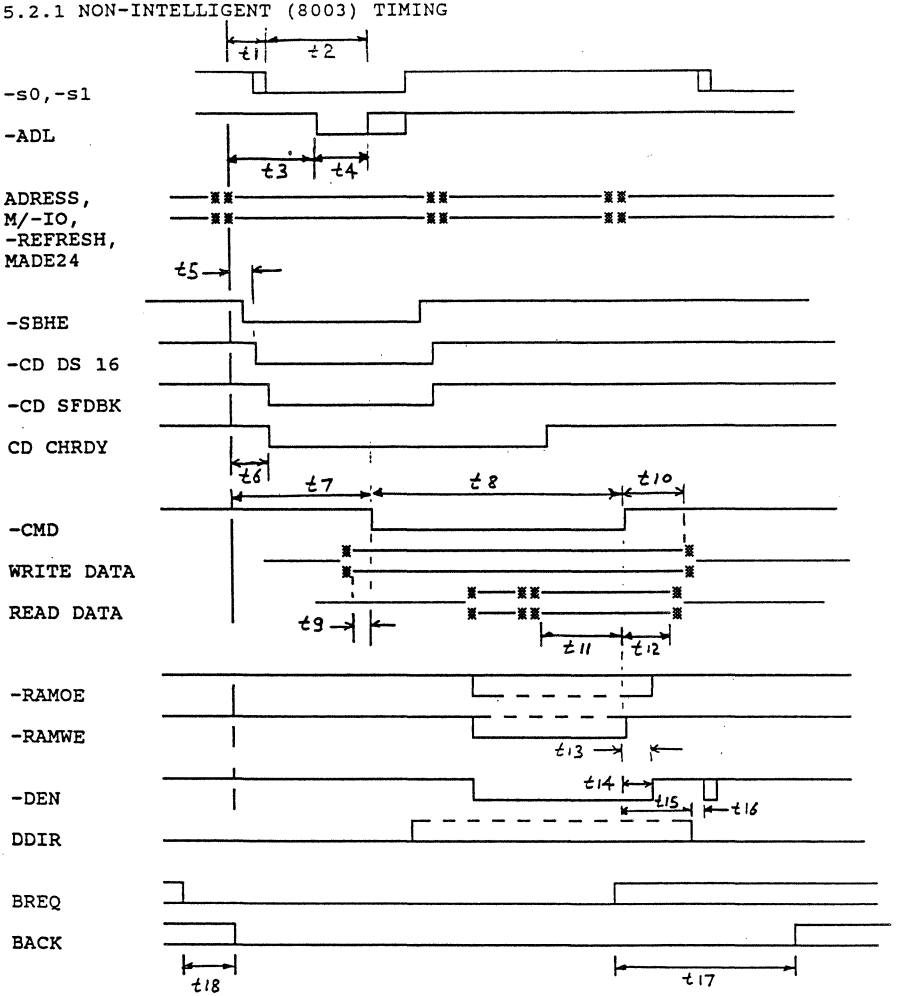


FIGURE 5.2.1.1
Host - Memory Read Write Timing

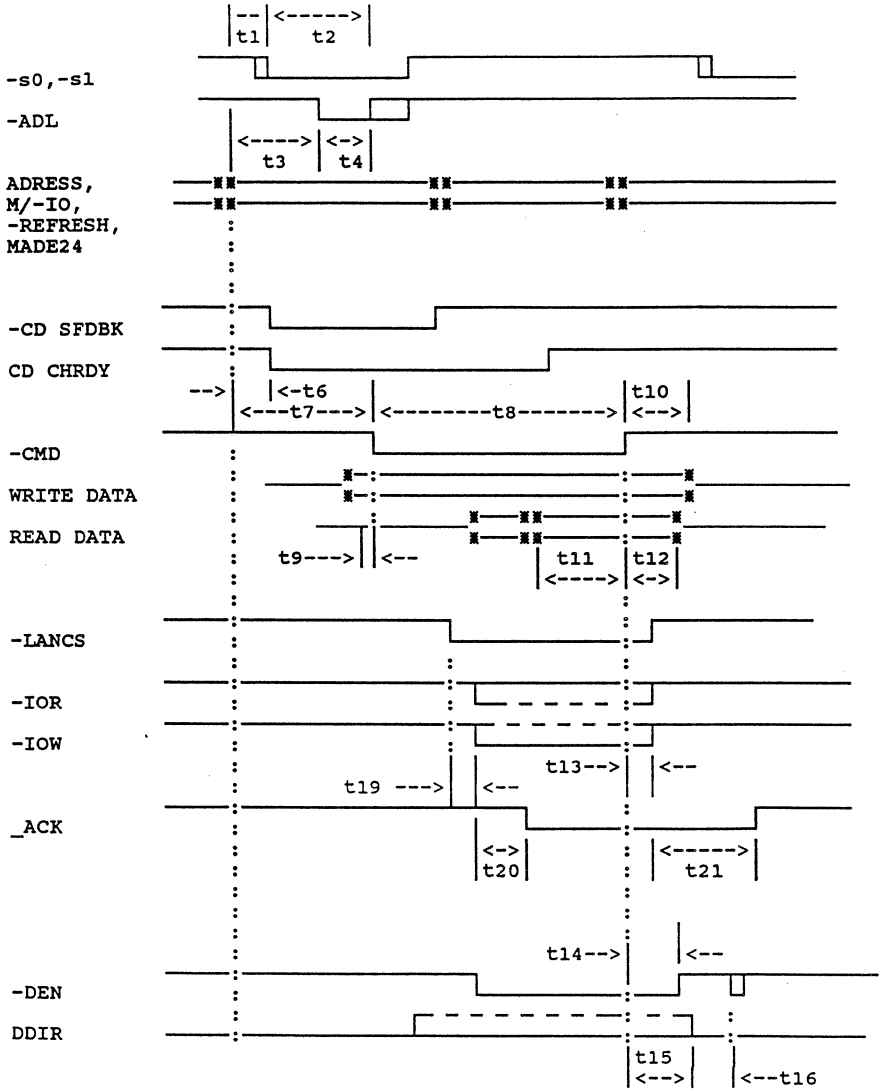

t1
t2
-s0,-s1
-ADL
t3
t4
ADRESS,
M/-IO,
-REFRESH,
MADE24
-CD SFDBK
CD CHRDY
t6
t7
t8
t10
-CMD
WRITE DATA
READ DATA
t9
t11
t12
-LANCS
-IOR
-IOW
t13
t19
_ACK
t20
t21
t14
-DEN
DDIR
t15
t16

FIGURE 5.2.1.2

Host - I/O (8390) Read Write Timing

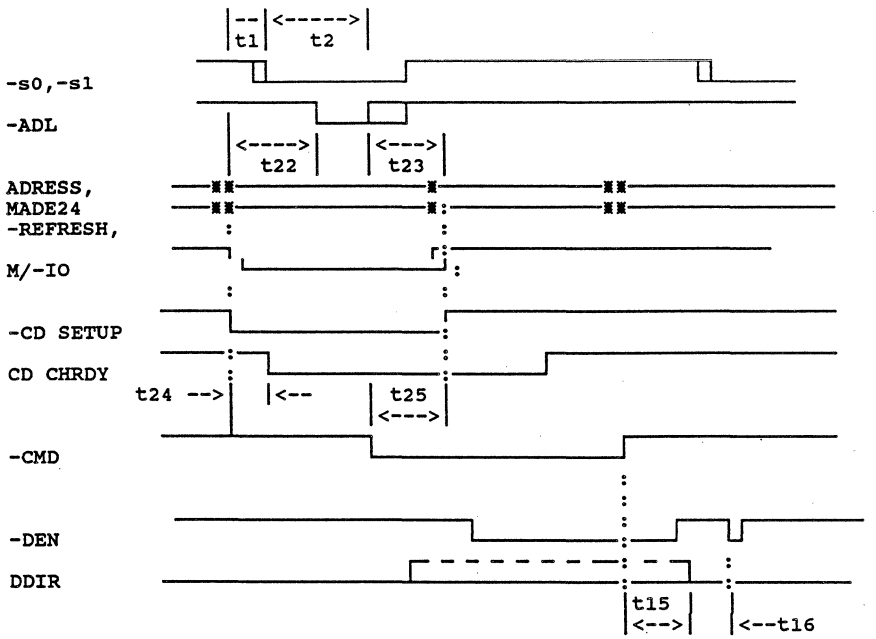
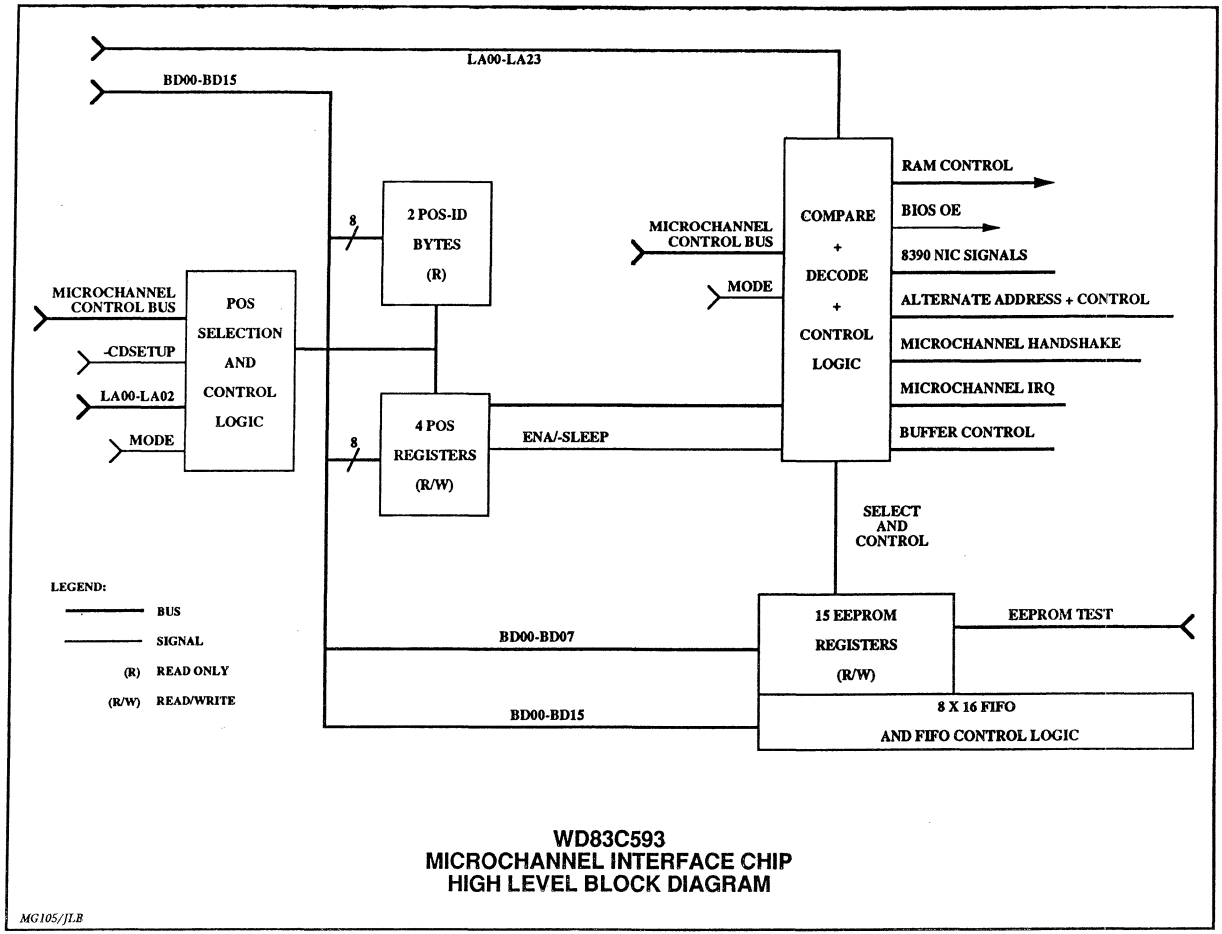


FIGURE 5.2.1.3
Setup Timing

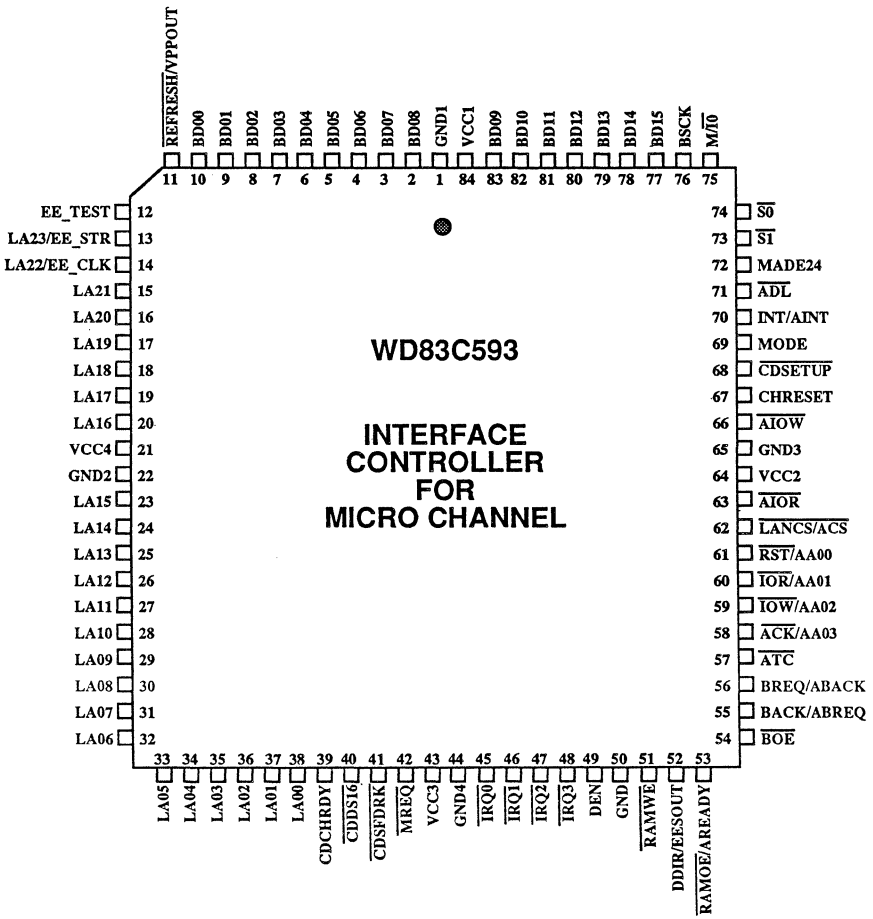
SYMBOL	PARAMETER	MIN.	MAX	UNITS
t1	Status active low from ADRESS, M/-IO,-Refresh valid	10		ns
t2	-CMD active low from status active low	55		ns
t3	-ADL active low from ADRESS, M/-IO,-REFRESH valid	45		ns
t4	-ADL active low to -CMD active low	40		ns
t5	-CDDS16 active low from ADRESS, M/-IO,-REFRESH valid		55	ns
t6	-CDSFDBK and CDCHRDY low from ADRESS valid		60	ns
t7	-CMD active low from ADRESS valid	85		ns
t8	-CMD pulse width	90		ns
t9	Write data setup to -CMD active low	0		ns
t10	Write data hold time from -CMD high (at the MC Bus)	30		ns
t11	Read data setup time to -CMD high (at the MC Bus)	60		ns
t12	Read data hold time from -CMD high (at the MC Bus)	5		ns
t13	-CMD high to -RAMOE or -RAMWE high	0		ns
t14 WRITE CYC.	-CMD high to -DEN high (During WRITE)	15		ns



WD83C593
MICROCHANNEL INTERFACE CHIP
HIGH LEVEL BLOCK DIAGRAM

MG105/JLB

WESTERN DIGITAL



SYMBOL	PARAMETER	MIN.	MAX	UNITS
t14 READ CYC.	-CMD high to DEN high (During READ)	0	25	ns
t15	-CMD high to DDIR low	0		ns
t16	DDIR low to "glitch" (Read cycles only)	0		ns
t17	BREQ active high to BACK active high	1 clk cyc time		
t18	BREQ low to BACK low	1 clk cyc time	3 clk cyc time+25ns	
t19	-LANCS active low to -IOR or -IOW active low	0		ns
t20	-ACK active low from -IOR or -IOW active low	0		ns
t21	-ACK high from -IOR or -IOW high	0		ns
t22	-CDSETUP active low to -ADL active low	15		ns
t23	-CDSETUP hold from -ADL high	25		ns
t24	-CDCHRDY inactive low from -CDSETUP active low		100	ns
t25	-CDSETUP hold from -CMD active low	30		ns