W E S T E R N D I G I T A L

C O R P O R A T I O N

O.E.M. MANUAL

WD7000-ASC HOST BUS ADAPTER

DOC.# 79-000124

TABLE OF CONTENTS

SECTION 4 INTERFACE CONNECTIONS PAGE

SECTION 6 COMMANDS PAGE

SECTION 7 TIMING PAGE

LIST OF TABLES

LIST OF ILLUSTRATIONS

SECTION 1

INTRODUCTION

1.0 DOCUMENT SCOPE

This document describes the design and performance of the WD7000-ASC Host Bus Adapter. The user is encouraged to become familiar with the following related documents:

WD33C93	SCSI Bus Interface Controller Data Sheet
WD37C65	Floppy Disk Subsystem Controller Data Sheet
SCSI	ANSI Standard Specification X3T9.2
IBM AT	IBM AT Technical Reference Manual
Z80	Zilog Technical And Programming Manuals

1.1 DESCRIPTION

The WD7000-ASC is an interface channel between the IBM AT bus and the SCSI bus. All the necessary drivers and receivers are included. Direct cable connections to the SCSI bus are made possible through a 50 pin connector. The IBM AT interface is made through two card edges as defined by the IBM AT Technical Manual. Address space, DMA channels, and interrupt requests can be selected to suit the user's application by optional jumper configurations.

To facilitate data transfer between the IBM AT and SCSI buses, the WD7000-ASC contains an onboard CPU (Z80) and a 16 byte FIFO on the IBM AT bus to maintain a 2.5 Mbyte/sec synchronous SCSI data transfer rate with the WD33C93, or a 4.0 Mbyte/sec synchronous SCSI data transfer rate with the WD33C93A. First Party DMA Logic (FPDMA) is employed to handle most of the command, data and status information via an outgoing mail box system, so that several logical units can be connected simultaneously. All other handshaking required to transfer data is done by the local CPU (LCPU).

The SCSI interface consists of the WD33C93 SCSI Bus Interface Controller (SBIC) that handles all of the arbitration, selection, disconnection, and reselection, leaving the LCPU to manage data transfers more efficiently. The SBIC is usually configured to operate as the initiator but can operate as a target as well in a multi-initiator system. Selection as a target generates an unsolicited interrupt to the Host IBM AT computer, if so enabled by the Host. Further communication is controlled totally by the Host IBM AT system, with the LCPU managing all of the required handshaking between the SBIC and the Host CPU.

An onboard floppy disk subsystem controller and a BIOS ROM are provided for the convenience of the Host. The WD37C65 Floppy Disk Subsystem Controller supports two floppy and is controlled entirely by the Host CPU. The BIOS ROM enables the Host to boot off a SCSI drive if desired.

The WD7000-ASC supports the common command set including all of the extended SCSI commands. SCSI commands are queued by the WD7000-ASC and can be linked by any initiator in the system. The SCSI bus parity option is fully supported as well. The onboard diagnostic capability allows field replacements easily and quickly.

The WD7000-ASC is based on a proprietary chip set specifically designed to add an SCSI port to the IBM AT bus.

1.2 FEATURES

- o INTELLIGENT Z80 CPU CHANNEL CONTROL
- o WD37C65 FLOPPY DISK CONTROLLER (OPTIONAL)
- o BIOS ROM (OPTIONAL)
- o WD33C93 SBIC FOR SCSI INTERFACE
- o FIRST PARTY DMA DATA TRANSFERS
- o ANY BLOCK SIZE TRANSFERS UP TO 16 MBYTES
- o EVEN OR ODD DMA START ADDRESS
- o 16 BYTE FIFO ON AT BUS
- o USER SELECTABLE DEVICE ADDRESS, DMA AND INTERRUPT CHANNELS
- o 4.0 MB/SEC SCSI SYNCHRONOUS DATA TRANSFER RATE*
- o 2.0 MB/SEC SCSI ASYNCHRONOUS DATA TRANSFER RATE
- o MULTIPLE LOGICAL THREAD CONNECTIONS UP TO 16 UNITS
- o OPERATES AS INITIATOR OR TARGET
- o BUS ARBITRATION INCLUDING DISCONNECT AND RECONNECT
- o STANDARD AND EXTENDED SCSI COMMANDS
- o SUPPORTS FULL SCSI COMMAND SET
- o SCSI BUS PARITY OPTION
- o QUEUED SCSI COMMANDS
- o PROGRAMMABLE DMA BUS ON/OFF TIMES
- o LINKED SCSI COMMANDS
- o ONBOARD CONTROLLER DIAGNOSTICS
- o IBM AT FORM FACTOR
- o SINGLE +5V POWER SUPPLY

* 4.0 MB/SEC WITH WD33C93A
  2.0 MB/SEC WITH WD33C93

1.3 OPERATION

This section provides an operational overview of the WD7000-ASC Host Bus Adapter. Figure 1-1 illustrates the WD7000-ASC Host Bus Adapter block diagram with the major functional blocks. The major functional blocks are:

- o Local Microprocessor (LCPU)
- o Program Memory (ROM)
- o Scratchpad RAM (SRAM)
- o First Party DMA Logic (FPDMA)
- o Host Interface Logic (HIL)
- o SCSI Bus Interface Controller (SBIC)
- o Floppy Disk Subsystem Controller (FDC)
- o BIOS ROM (BIOS)
- o Control Support Logic (CS)

1.3.1 LOCAL MICROPROCESSOR (LCPU)

The Local Microprocessor (LCPU) is a Zilog Z80, the heart of the control logic for the WD7000-ASC. By interpreting commands sent from the Host, the LCPU configures the other logic blocks to perform the desired operation. This includes setting the data transfer direction, DMA starting address, time on and time off the IBM AT bus counters, as well as control of the SBIC.

Host access to the WD7000-ASC via the command port causes the LCPU to read the command byte immediately. The command is decoded and either executed if it is an ASC local command or put in the SBIC queue if it is meant for a SCSI device. In all cases, the Host is informed within 70uS whether the command has been accepted or not by the WD7000-ASC.

The actual execution time for a particular command, that has been put in a queue, is governed by: the programmed DMA bus on/off times, the number of mail boxes available, the length of the data transfers, and any exception handling involved.

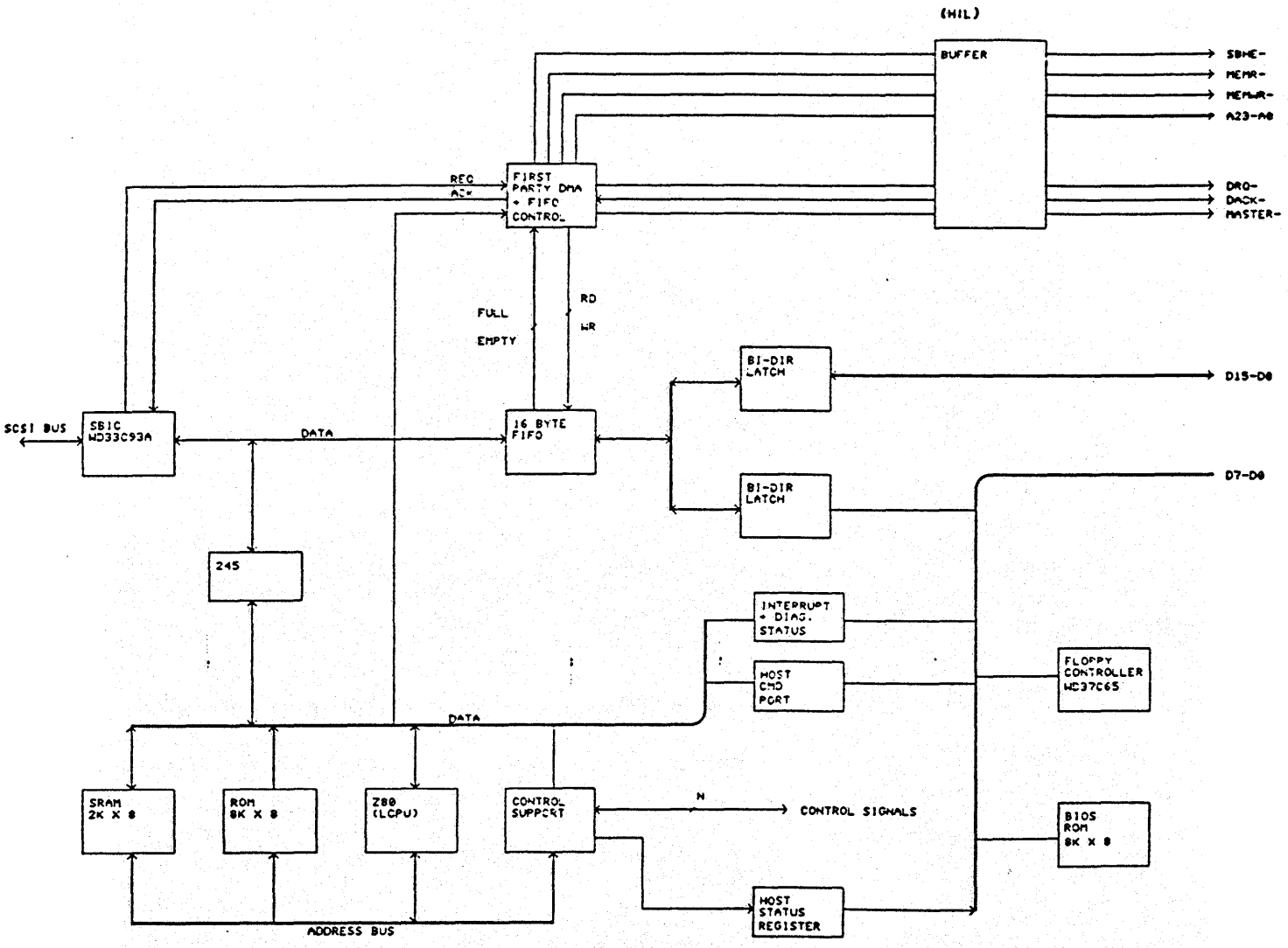


FIGURE 1-1. WD7000-ASC HOST BUS ADAPTER BLOCK DIAGRAM

1.3.1.1 LCPU CLOCK

The LCPU uses a 4 MHz clock obtained by dividing the 8 MHz clock used for the SBIC device. This gives the LCPU a basic clock period of 250nS referred to as the T cycle. The machine cycles vary from 4 to 23 T states. A complete description of the instruction set and execution times can be found in the references listed in the front of this Section.

1.3.2 PROGRAM MEMORY

The Program Memory (ROM) is an 8K X 8 PROM that contains the control firmware for the LCPU with a provision for up to 32K with small changes in the hardware design for any future enhancements. The other 32K of the address space, differentiated by A15, is reserved for data memory.

1.3.3 SCRATCHPAD RAM

The Scratchpad RAM (SRAM) is 2K X 8 and is used by the LCPU to store variables and queued commands issued by the Host. Since SCSI command data is directly passed between the Host and the SBIC, no provision has been made to buffer any data, eliminating any latencies required to store and then transfer the data.

The present RAM size is sufficient to handle 16 logical threads which implies that up to 16 commands for different SCSI LUNs can be active at any given instant of time. In addition, the SCAN MAIL BOX command can be used to issue more than 16 commands without requiring any further Host intervention than simply issuing the command. However, more logical threads can be supported by increasing the size of the Scratchpad RAM depending upon future applications at the cost of minor hardware modifications.

1.3.4 FIRST PARTY DMA LOGIC

First Party DMA Logic (FPDMA) provides high speed data transfers by allowing the WD7000-ASC to be master of the IBM AT bus. The hardware consists of a 16 byte FIFO that can transfer a word across the AT bus every 375nS, DMA control logic to transfer data in word mode or byte mode, on even or odd addresses, and a 24-bit counter to address up to 16M of Host memory. The bus on/off times are fully programmable by the Host. The DMA state machine control is implemented using PALS as described in the referencess listed in the front of this Section.

The LCPU sets data transfer direction, starting DMA address, time on and time off the AT bus and then issues a START. For WD7000-ASC to AT transfers, the FPDMA will wait for data to be filled in the FIFO, then arbitrate for the AT bus by asserting DRQ. Upon receiving $\overline{\text{DACK}}$ the FPDMA will assert $\overline{\text{MASTER}}$ and then start writing to the AT's memory. The FPDMA will continue as master until time on the bus is exhausted or FIFO is empty. It will stay off the bus until the time off the bus is exhausted then re-arbitrate if data is still in the FIFO. AT to WD7000-ASC transfers are similiar except reads are done from the AT's memory and data is stored in the FIFO. The WD7000-ASC will continue to re-arbitrate for the bus until all data has been transferred across the FIFO.

The FPDMA also provides the necessary signals to transfer data between the SBIC and FIFO and between the LCPU and FIFO.

1.3.5 HOST INTERFACE LOGIC

The Host Interface Logic (HIL) contains the requisite logic to buffer all data and control between the IBM AT bus and the WD7000-ASC. The Host interface consists of 16 data lines, a 24-bit address bus and control lines. For a description of the signals and pinouts refer to Section 4. HIL also contains a: Command Register, WD7000-ASC Interrupt Strobe, Static Reset, and an SCSI Bus Reset.

1.3.6 SCSI BUS INTERFACE CONTROLLER

The SCSI Bus Interface Controller (SBIC) is a single chip SCSI controller that can operate either as a target or an initiator. When the SBIC status register indicates reselection, it is configured as the initiator. If the selection status is set, then it is configured as a target. The SBIC, under the control of the LCPU, generates all of the necessary signals and timing to command the SCSI bus and transfer information across it.

1.3.7 FLOPPY DISK SUBSYSTEM CONTROLLER

The Floppy Disk Subsystem Controller (FDC) is a single chip floppy disk controller. With minimal hardware it interfaces directly to the IBM AT bus and enables the Host to control up to two drives.

1.3.8 BIOS ROM

The BIOS ROM (BIOS), consisting of an 8K X 8 ROM, enables the Host to boot directly from a hard disk drive on the SCSI bus and to determine the number of logical units connected to the bus at power on. The other main function is to convert the Host DOS interrupt 13 protocol to the mail box protocol, including the SCSI CDB construction.

The address space of the BIOS is configurable in the range COXXX-DEXXX (Hex), with the LSB 13 bits being used to address the 8K ROM.

1.3.9 CONTROL SUPPORT LOGIC

The Control Support Logic (CS) consists mainly of decoders in the I/O address space of the LCPU, the reset circuitry, miscellaneous combination logic and memory elements needed to control the various functional blocks. Due to the nature of the CS, Control Support Logic tends to be logically distributed as required instead of being mostly centralized as other blocks. Nevertheless, CS can functionally be thought of as a block that is used by the LCPU to implement all of the real time control functions required to direct the signal flow within the WD7000-ASC channel.

1.3.9.1 RESET LOGIC

The reset pulse for the WD7000-ASC can come from three sources: power-up reset, Host, or the SCSI port.

The reset from the SCSI port is used to reset the SBIC device but not the LCPU. This was done to maintain all of the Host command queue so that these commands can be re-started without having the Host re-issue the commands again.

A similiar set/reset D-FF is provided to reset all of the devices on the SCSI interface. Host access to these two reset registers is explained in Section 5 along with the other Host addressable WD7000-ASC ports.

SECTION 2

SPECIFICATIONS

2.0 GENERAL

This section contains the overall specifications for the WD7000-ASC Host Bus Adapter.

2.1 PHYSICAL

Form Factor:	IBM PC AT
Length:	13.1 inches (33.27 centimeters)
Height:	0.50 inches (1.27 centimeters)
Width:	4.75 inches (10.67 centimeters)

2.2 POWER

Voltage:	+5VDC ± 5%
Current:	2.0 amps max, 1.7 amps typical

2.3 PERFORMANCE

Host Transfer Rate:	5.3 MByte/sec Burst
SCSI Transfer Rate:	4.0 Mbyte/sec Synchronous 2.0 Mbyte/sec Asynchronous
LCPU Clock:	4 MHZ
SBIC Clock:	8 MHZ
Selection Time Out:	250mS
Logical Threads:	16
AT Bus On/Off Time:	Programmable
MTBF:	10,000 POH
MTTR:	30 minutes

2.4 HOST INTERFACE

16-Bit, Bi-directional AT Bus
62 Pin Card Edge Connector
38 Pin Card Edge Connector

2.5 SCSI INTERFACE

9-Bit, Bi-directional SCSI Bus
50 Pin SCSI connector
20 ft.max (6 meters) Drive Cable length

2.6 ENVIRONMENTAL:

Ambient Temperature:	$0^{o}C$ ($32^{o}F$) to $55^{o}C$ ($131^{o}F$)
Relative Humidity:	10% to 95% non-condensing
Air Flow:	100 lin ft/min. at 0.5" from component surface
Altitude:	10,000 ft. max (operating)
Altitude:	15,000 ft. max (storage)

SECTION 3

INSTALLATION

3.0 GENERAL

This section briefly covers the installation of the WD7000-ASC into an IBM AT computer. Reference should be made to the IBM AT Technical Reference Manual during installation.

3.1 HARDWARE INSTALLATION

Observe the following basic steps while installing the WD7000-ASC Host Bus Adapter:

1. Ensure that all electrical power to the computer is OFF.
2. Install the WD7000-ASC Host Bus Adapter into the computer chassis.
3. Refer to Figure 3-1, then connect the 50 pin SCSI interface connector to J4 and the 34 pin disk drive connector to J2. Connect Host furnished power source to J1.
4. Power up the computer.

3.2 SOFTWARE INSTALLATION

Refer to the IBM Disk Operating System Manual for complete formatting instructions.

3.3 JUMPER CONFIGURATIONS

The various jumper configurations are shown in figure and tables. Installing the jumper in the positions shown will force that option to a logic low level. Removing the jumper from the position shown will force that option to a logic high level.

There are eight jumper locations on the WD7000-ASC Host Bus Adapter: W1, W2, W3, W4, W5, W6, W7, W8. The user may select to change the WD7000-ASC I/O Address Space, the BIOS ROM Address Space, the DMA Channel, the Interrupt Request Channel, Terminator Power, Floppy Controller Deselection, Select one of two speeds for the Floppy Disk Drive, or select the time factor to Write Precompensation for the Floppy Controller.

Table 3-1 presents the WD7000-ASC jumper configurations.

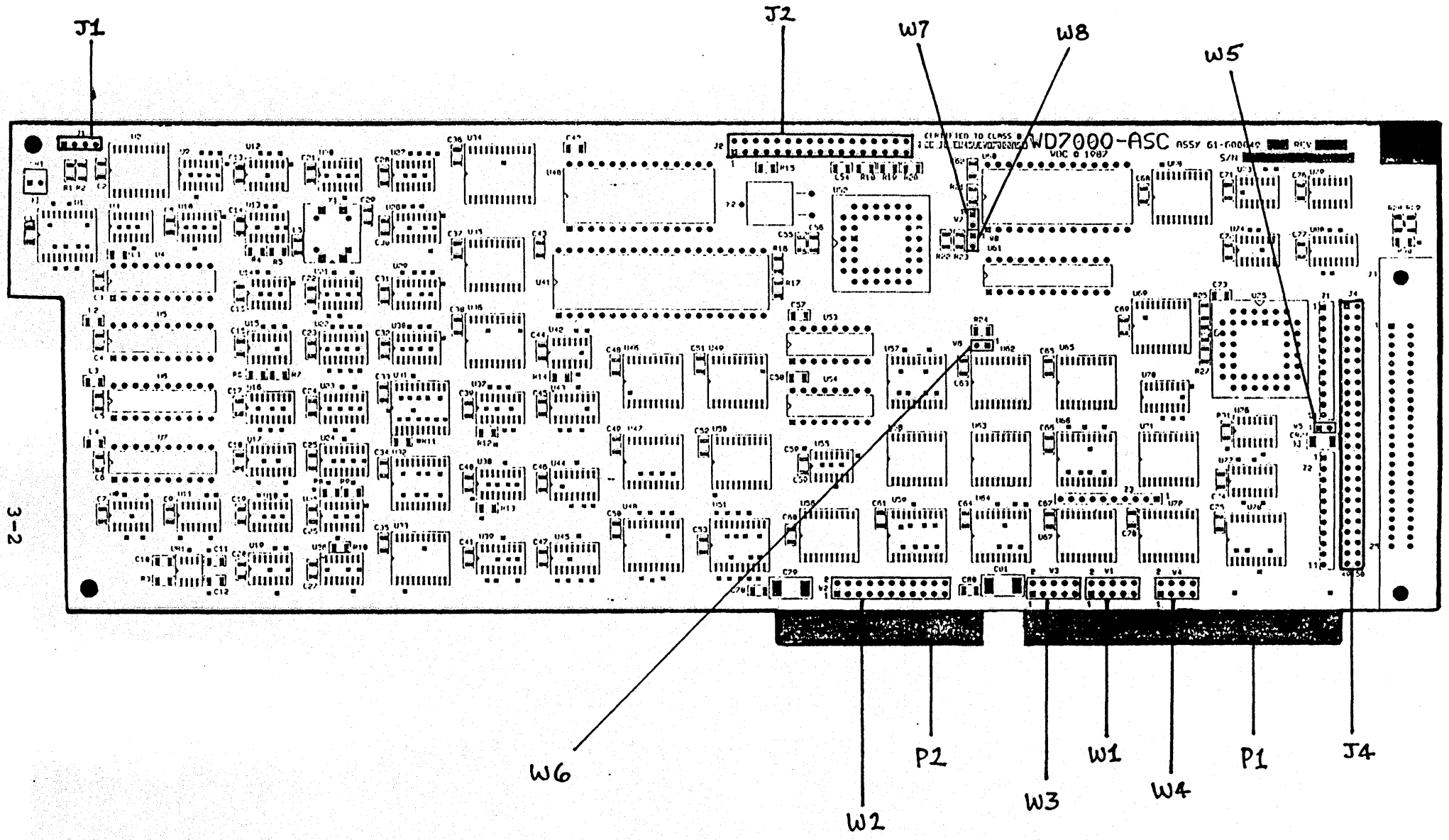
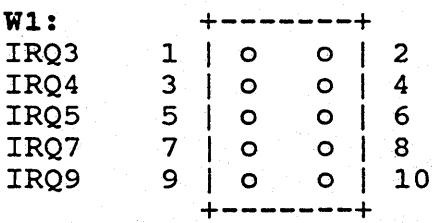


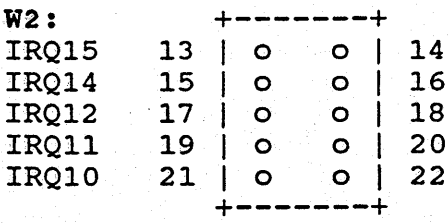
FIGURE 3-1. WD7000-ASC BOARD CONNECTORS AND JUMPER LOCATIONS

TABLE 3-1. WD7000-ASC JUMPER CONFIGURATIONS

W1:

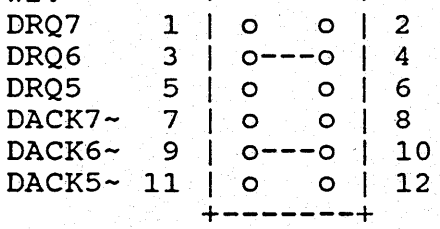


W2:



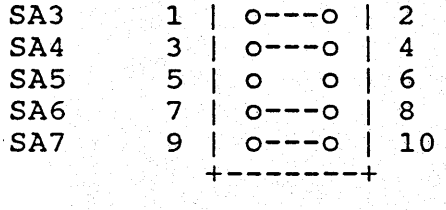
DRQ/DACK JUMPERS (W2):

W2:



I/O ADDRESS SPACE (W3):

W3:

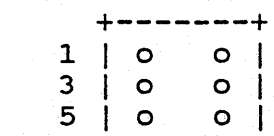


SA7	SA6	SA5	SA4	SA3	I/O ADDRESS
1	1	1	1	1	3F8H
1	1	1	1	0	3F0H
1	1	1	0	1	3E8H
1	1	1	0	0	3E0H
1	1	0	1	1	3D8H
1	1	0	1	0	3D0H
1	1	0	0	1	3C8H
1	1	0	0	0	3C0H
1	0	1	1	1	3B8H
1	0	1	1	0	3B0H
1	0	1	0	1	3A8H
1	0	1	0	1	3A0H
1	0	0	1	1	398H
1	0	0	1	0	390H
1	0	0	0	1	388H
1	0	0	0	0	380H
0	1	1	1	1	378H
0	1	1	1	0	370H
0	1	1	0	1	368H
0	1	1	0	0	360H
0	1	0	1	1	358H
0	1	0	1	0	350H
0	1	0	0	1	348H
0	1	0	0	0	340H
0	0	1	1	1	338H
0	0	1	1	0	330H
0	0	1	0	1	328H
0	0	1	0	0	320H
0	0	0	1	1	318H
0	0	0	1	0	310H
0	0	0	0	1	308H
0	0	0	0	0	300H

NOTE: A "1" INDICATES **NO JUMPER**

TABLE 3-1. WD7000-ASC JUMPER CONFIGURATIONS (CONTINUED)

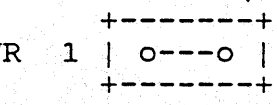
W4:



SA16	SA15	SA14	SA13	BIOS ADDRESS
1	1	1	1	DE00H
1	1	1	0	DC00H
1	1	0	1	DA00H
1	1	0	0	D800H
1	0	1	1	D600H
1	0	1	0	D400H
1	0	0	1	D200H
1	0	0	0	D000H
0	1	1	1	CE00H
0	1	1	0	CC00H
0	1	0	1	CA00H
0	1	0	0	C800H
0	0	1	1	C600H
0	0	1	0	C400H
0	0	0	1	C200H
0	0	0	0	C000H

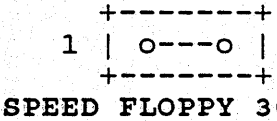
NOTE: A "1" INDICATES NO JUMPER

TERMINATOR POWER (W5):



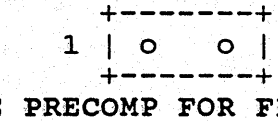
FLOPPY CONTROLLER DESELECTION (W6):

W6:



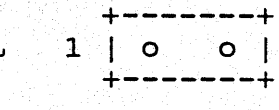
DUAL SPEED FLOPPY 300/360 RPM (W7):

W7:



WRITE PRECOMP FOR FLOPPY CONTROLLER 125NS WITHOUT JUMPER 187NS WITH JUMPER (W8):

W8:



SECTION 4

INTERFACE CONNECTORS

4.0 GENERAL

The WD7000-ASC has five onboard connectors; two Host interface connectors, a 50 pin SCSI interface connector, a 34 pin connector for the floppy disk drive interface, and a four pin connector for the Host furnished drive select led.

The Host interface connectors provide interface signals that are compatible with the IBM PCAT on the mother board. For a complete description of the interface, reference should be made to the IBM AT Technical Manuals.

The SCSI interface is completely explained in the ANSI Standard X3T9.2 Specifications.

4.1 HOST INTERFACE CONNECTORS (P1, P2)

The Host interface is made through the 62 pin board edge connector (P1), and a 36 pin board edge connector (P2), where the computer I/O bus and power is available to the WD7000-ASC (refer to Figure 3-1). Connector pins A1 through A31, and C1 through C18, are located on the component side of the WD7000-ASC. Pins B1 through B31, and D1 through D18 are on the conductor side. The WD7000-ASC does not load the computer I/O bus with more than two LSTTL DC loads per line. The P1 edge connector pin outs are listed in Table 4-1. The P2 edge connector pin outs are listed in Table 4-2.

TABLE 4-1. P1 CONNECTOR PIN OUTS

I/O PIN	I/O	SIGNAL NAME	I/O PIN	I/O	SIGNAL NAME
A1	N/C	IOCHCK	B1	GND	GND
A2	I/O	D7	B2	I	HMR
A3	I/O	D6	B3	+5	+5VDC
A4	I/O	D5	B4	O	IRQ9
A5	I/O	D4	B5	-5	-5VDC
A6	I/O	D3	B6	O	DRQ2
A7	I/O	D2	B7	-12	-12VDC
A8	I/O	D1	B8	O	OWS
A9	I/O	D0	B9	+12	+12VDC
A10	N/C	IOCHRDY	B10	GND	GND
A11	I	AEN	B11	N/C	SMEMW
A12	I/O	A19	B12	N/C	SMSMR
A13	I/O	A18	B13	I/O	IOW
A14	I/O	A17	B14	I/O	IOR
A15	I/O	A16	B15	I	DACK3
A16	I/O	A15	B16	O	DRQ3
A17	I/O	A14	B17	I	DACK1
A18	I/O	A13	B18	O	DRQ1
A19	I/O	A12	B19	I/O	REFRESH
A20	I/O	A11	B20	I	CLK
A21	I/O	A10	B21	O	IRQ7
A22	I/O	A9	B22	O	IRQ6
A23	I/O	A8	B23	O	IRQ5
A24	I/O	A7	B24	O	IRQ4
A25	I/O	A6	B25	O	IRQ3
A26	I/O	A5	B26	I	DACK2
A27	I/O	A4	B27	N/C	T/C
A28	I/O	A3	B28	N/C	BALE
A29	I/O	A2	B29	+5	+5VDC
A30	I/O	A1	B30	N/C	OSC
A31	I/O	A0	B31	GND	GND

TABLE 4-2. P2 CONNECTOR PIN OUTS

I/O PIN	I/O	SIGNAL NAME	I/O PIN	I/O	SIGNAL NAME
C1	I/O	SBHE	D1	O	MEMCS16
C2	I/O	LA23	D2	O	IOCS16
C3	I/O	LA22	D3	O	IRQ10
C4	I/O	LA21	D4	O	IRQ11
C5	I/O	LA20	D5	O	IRQ12
C6	I/O	LA19	D6	O	IRQ15
C7	I/O	LA18	D7	O	IRQ14
C8	I/O	LA17	D8	I	DACK0
C9	I/O	MEMR	D9	O	DRQ0
C10	I/O	MEMW	D10	I	DACK5
C11	I/O	D8	D11	O	DRQ5
C12	I/O	D9	D12	I	DACK6
C13	I/O	D10	D13	O	DRQ6
C14	I/O	D11	D14	I	DACK7
C15	I/O	D12	D15	O	DRQ7
C16	I/O	D13	D16	+5	+5VDC
C17	I/O	D14	D17	O	MASTER
C18	I/O	D15	D18	GND	GND

4.1.1 DATA BUS (D7 - D0)

Positive true 8-bit, tri-state, bi-directional, data bus for data, commands, and status communication between the WD7000-ASC and the Host. D7 - D0 form the least significant byte of a 16-bit data transfer.

4.1.2 ADDRESS ENABLE (AEN)

Address Enable is used to degate the Host CPU and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the WD7000-ASC DMA controller has control of the Host address bus, memory control, and data busses. When AEN is active, I/O port addresses are no longer generated for I/O port access. The BIOS ROM can still be addressed via A19 - A0.

If AEN is inactive (or low), and a valid port address (XX0-XX3) is present on the address bus, then the WD7000-ASC is in programmed I/O mode.

4.1.3 ADDRESS BUS (A19 - A0)

Positive true 20-bit address. The least significant 10 bits are decoded to obtain the address, ports XX0 through XX3, for processor I/O instruction execution. They are inhibitted during DMA by AEN. The full 20 address bits are decoded to address the on-board ROM, regardless of the state of AEN.

4.1.4 BUFFERED ADDRESS LATCH ENABLE (BALE)

A19 - A0 are latched on the falling edge of BALE to indicate a valid address by the Host. During DMA cycles the Host forces $\overline{\text{BALE}}$ high. BALE is not used by the WD7000-ASC controller.

4.1.5 MEMORY READ ($\overline{\text{MEMR}}$)

The Memory Read signal, active on all memory read cycles, instructs the memory devices to drive data onto the data bus. $\overline{\text{MEMR}}$ may be driven by any microprocessor or DMA controller in the system. When the WD7000-ASC drives the $\overline{\text{MEMR}}$ signal, the address lines are valid at least one system clock period before driving $\overline{\text{MEMR}}$ active.

4.1.6 MEMORY WRITE ($\overline{\text{MEMW}}$)

The Memory Write signal, active on all memory write cycles, instructs the memory devices to store data from the data bus. $\overline{\text{MEMW}}$ may be driven by any microprocessor or DMA controller in the system. When the WD7000-ASC drives the $\overline{\text{MEMW}}$ signal, the address lines are valid at least one system clock period before driving $\overline{\text{MEMW}}$ active.

4.1.7 I/O READ ($\overline{\text{IOR}}$)

The I/O Read signal, active when the Host (microprocessor or DMA controller) or the WD7000-ASC (microprocessor or DMA controller) resident on the I/O channel, instructs an I/O device to drive data onto the data bus.

4.1.8 I/O WRITE ($\overline{\text{IOW}}$)

The I/O Write signal, active when the Host (microprocessor or DMA controller) or the WD7000-ASC (microprocessor or DMA controller) resident on the I/O channel, instructs an I/O device to read data from the data bus.

4.1.9 SYSTEM MEMORY ACCESS ($\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$)

These system memory read and write strobes are used by the Host to address any memory that is mapped within the low 1Mb of the memory space. These strobes are not used by the WD7000-ASC controller.

4.1.10 RESET (RESET DRV)

When asserted, RESET DRV places the WD7000-ASC in its initial power-up condition.

4.1.11 I/O CHANNEL READY ($\overline{\text{IOCHRDY}}$)

This input signal to the IBM AT bus is pulled low by a memory or an I/O device to lengthen I/O or memory cycles by an internal number of clock cycles (167nS). This signal is not used by the WD7000-ASC controller.

4.1.12 I/O CHANNEL CHECK ($\overline{\text{IOCHCHK}}$)

This signal to the Host IBM AT bus provides the system with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error. This output line to the Host is not used by the WD7000-ASC controller.

4.1.13 ZERO WAIT STATE (OWS)

The Zero Wait State signal tells the Host processor that it can complete the present bus cycle without inserting any additional wait cycles. The address space of any onboard memory accessible to the Host, along with the read and write strobes, can be used to generate this signal. This signal is not presently used by the WD7000-ASC controller.

4.1.14 REFRESH DYNAMIC MEMORY ($\overline{\text{REFRESH}}$)

The $\overline{\text{REFRESH}}$ strobe, generated about every 15uS by the Host, is used by the WD7000-ASC to surrender the IBM AT bus so that the Host can refresh the system's dynamic memory.

4.1.15 SYSTEM CLOCK (CLK)

The 6 or 8 MHz synchronous system clock signal used in the IBM AT is not used by the WD7000-ASC controller.

4.1.16 OSCILLATOR CLOCK (OSC)

The Oscillator Clock signal (70nS - 14.31818 MHz) used in the IBM AT is not used by the WD7000-ASC.

4.1.17 TERMINAL COUNT (TC)

The Terminal Count signal is provided by the Host when the terminal count for any DMA channel is reached. This signal is not used by the WD7000-ASC.

4.1.18 +5VDC (B3, B29, D16)

+5 Volts D.C. power supply.

4.1.19 -12VDC (B7)

-12 Volts D.C. power supply.

4.1.20 +12VDC (B9)

+12 Volts D.C. power supply.

4.1.21 GROUND (B1, B10, B31, D18)

Ground return for all signals.

4.1.22 BUS MASTER ($\overline{\text{MASTER}}$)

This signal is used with a DRQ line to gain control of the Host system bus. The WD7000-ASC DMA controller issues a DRQ to a DMA channel in the cascade mode and receives a $\overline{\text{DACK}}$. Upon receiving the $\overline{\text{DACK}}$, the WD7000-ASC controller asserts $\overline{\text{MASTER}}$, which allows it to control the system address, data, and control lines for no more than 15uS so that the Host can refresh the system memory at regular intervals.

The WD7000-ASC DMA controller waits at least one system clock period before driving the address and data lines, and two clock periods before issuing any memory read or write strobes.

4.1.23 DMA DATA REQUEST (DRQ5 to DRQ7)

DMA request 5-7 are asynchronous channel requests used by peripheral devices to gain DMA service or control of the Host bus. DRQ5-DRQ7 will perform 16-bit DMA transfers and are available as jumperable options on the WD7000-ASC controller (reference Section 3).

4.1.24 DATA ACKNOWLEDGE ($\overline{DACK5}$ to $\overline{DACK7}$)

DMA Acknowledge, asserted by the Host in response to a DMA request from the WD7000-ASC. These are active low signals and are jumper selectable on the WD7000-ASC controller (reference Section 3).

4.1.25 INTERRUPT REQUEST (IRQX)

Interrupt Request 3-7, 9-12, and 14-15 are used to signal the Host that an I/O device needs attention. A jumper configurable interrupt request is asserted by the WD7000-ASC to interrupt the Host upon completion of an operation.

4.1.26 MEMORY CHIP SELECT 16-BIT ($\overline{MEMCS16}$)

This signals the Host system that the present data transfer ia a 1 wait state, 16-bit, memory cycle, derived from the decode of LA17-LA23.

4.1.27 I/O CHIP SELECT 16-BIT ($\overline{IOCS16}$)

This signal is similiar to the $\overline{MEMCS16}$ signal. It indicates to the Host system that the present data transfer is a 1 wait state, 16-bit, I/O cycle. It is derived from an address decode.

4.1.28 SYSTEM BUS HIGH ENABLE (SBHE)

The SBHE signal indicates that a data transfer on the upper byte (SD15-SD8) of the data bus. The present bus master uses this signal to condition the data bus buffers driving SD15-SD8 lines.

4.1.29 DATA BUS (SD0-SD15)

Data Bus lines SD15-SD0 form the AT's 16-bit data bus.

4.1.30 UNLATCHED ADDRESS BUS (LA23-LA17)

These unlatched signals can be used to address memory and I/O devices within the system, extending the address space to 16Mb.

4.2 SCSI INTERFACE CONNECTOR

The SCSI Interface Connector is a 50 pin, vertical header, consisting of two rows of 25 male pins (2.54mm) apart. The single ended cable length shall not exceed 6.0 meters as specified by the ANSI Specifications.

The pin outs are listed in Table 4-3. All odd numbered pins except pin 25 are connected to ground.

The WD7000-ASC is configured as an initiator or a target with signal descriptions defined in the WD33C93-SBIC data sheets.

TABLE 4-3. SCSI INTERFACE CONNECTOR PIN OUTS

I/O PIN	I/O	SIGNAL NAME
2	I/O	$\overline{DB0}$
4	I/O	$\overline{DB1}$
6	I/O	$\overline{DB2}$
8	I/O	$\overline{DB3}$
10	I/O	$\overline{DB4}$
12	I/O	$\overline{DB5}$
14	I/O	$\overline{DB6}$
16	I/O	$\overline{DB7}$
18	I/O	$\overline{DBP}$
20	GND	GND
22	GND	GND
24	GND	GND
26	N/C	TERMPWR

I/O PIN	I/O	SIGNAL NAME
28	GND	GND
30	GND	GND
32	0	$\overline{ATN}$
34	GND	GND
36	I/O	$\overline{BSY}$
38	0	$\overline{ACK}$
40	I/O	$\overline{RST}$
42	I	$\overline{MSG}$
44	I/O	$\overline{SEL}$
46	I	$\overline{C}$ /D
48	I	$\overline{REQ}$
50	I	$\overline{I}$ /O

4.3 FLOPPY DISK DRIVE INTERFACE CONNECTOR

The floppy port is controlled entirely by the Host. The WD7000-ASC hosts the floppy interface hardware but does not control it in any way. The descriptions of the floppy interface signals are given in the WD37C65 data sheets or may be found in the OEM manual of the floppy disk drive manufacturer.

The pin outs for the 34 pin Floppy Disk Drive Interface Connector are listed in Table 4-4.

TABLE 4-4. FLOPPY DISK DRIVE CONNECTOR PIN OUTS

SIGNAL GROUND	SIGNAL PIN #	DIR I/O	SIGNAL MNEMONIC	SIGNAL DESCRIPTION
1	2	O	$\overline{RWC}$	Reduce Write Current
3	4	N/C	-	No Connection
5	6	N/C	-	No Connection
7	8	I	$\overline{IDX}$	Index Pulse
9	10	O	$\overline{MOA}$	Motor Enable A
11	12	O	$\overline{DSB}$	Drive Select B
13	14	O	$\overline{DSA}$	Drive Select A
15	16	O	$\overline{MOB}$	Motor Enable B
17	18	O	$\overline{DIRC}$	Direction In
19	20	O	$\overline{STEP}$	Step Pulse
21	22	O	$\overline{WD}$	Write Data
23	24	O	$\overline{WG}$	Write Gate
25	26	I	$\overline{TKOO}$	Track 00
27	28	I	$\overline{WP}$	Write Protect
29	30	I	$\overline{RD}$	Read Data
31	32	O	$\overline{HS}$	Head Select0 or 1
33	34	I	$\overline{DCHNG}$	Diskette Change

SECTION 5

HOST INTERFACE PROTOCOL

5.0 GENERAL

The interface between the Host AT system and the WD7000-ASC controller occurs at three levels: Host WD7000-ASC control, SCSI DMA access, and Interrupt generation. The hardware aspects of the interface do not enter the I/O drivers with the exception of the maximum bus on/off times. Bus on/off time, in this context, is defined as the amount of time the WD7000-ASC is on the AT bus during DMA transfers and the amount of time that elapses after a packet of data has been transferred before the next packet of data can be transferred. The Host bus on/off times are both programmable parameters of the Host adapter, and can be specified via a WD7000-ASC command discussed in Section 6. On the SCSI side, disconnection can occur as required by the target provided all of the required SCSI protocol has been properly followed. Before specifying the actual handshake between the AT-WD7000-ASC-SCSI in either direction, a general signal flow will be described to understand the interaction between all of the major logic components in the system. Refer to Section 7 for timing parameters.

5.1 GENERAL SIGNAL FLOW

All communication between the Host and the WD7000-ASC takes place via the HIL, using command control byte and a mail box system. The Host issues commands to the WD7000-ASC by first selecting the WD7000-ASC through it's address bus and writing a command byte to the command port. The command strobe clears the COMMAND PORT READY status bit alerting the Host and the onboard LCPU that command execution is now in progress. The Host must provide additional parameter bytes, if required, by writing to the command port when the COMMAND PORT READY status bit is set within 70us. This 8-bit programmed I/O data transfer handshake is repeated until the required number of bytes to complete the command have been transferred. The START I/O command byte contains a mail box number. This out going mail box contains the command block pointer of the SCSI/WD7000-ASC command to be executed. The four bytes contained in this mail box are accessed using the onboard DMA controller (First Party DMA).

The 32 bytes of the command block that are accessed from the system memory are stored in the SRAM before being decoded for execution. The command is then executed by the LCPU or is re-issued to the SBIC for a SCSI access. The SBIC device handles all of the SCSI protocol including arbitration, selection or re-selection, etc.

For any write operation to a SCSI LUN additional bytes of data are accessed from the Host system memory using First Party DMA transfers controlled by the bus hold time programmable parameters. This sector of data is written directly to the SBIC using the SBIC's DRQ-/DACK- handshake until all of the bytes have been transferred. For all other commands that do not require data, this phase of the operation is skipped. At the end of the data transfer phase the SBIC obtains the command status and generates an SINTRQ to the LCPU. This status is then read by the Host upon command completion via the ICMB or the CDB, signalled by an interrupt to the Host.

On a read operation from the selected LUN, arbitration and selection takes place as before except that the flow of data is reversed. The transfer of data can be throttled by the DMA controller by not asserting the DACK- input to the SBIC device.

For the same logical unit, commands can be linked via the Host CDB. The next Host CDB will be accessed and executed when the prior command has been completed. This new Host CDB can in turn point to another command to be executed. In this fashion several commands may be chained together. Interrupts to the Host can be programmed to be generated at the end of every command or on completion of the entire chain of commands.

When the WD7000-ASC is selected as the target, whether anticipated or not, an interrupt is generated to the LCPU which in turn sets an appropiate incoming mail box and interrupts the Host, if so enabled. The command, data and status bytes are then transferred in three or more packets. Each information packet is only initiated after the WD7000-ASC receives an appropiate command from the Host to accept that packet from the SCSI Initiator. Each SCSI command is executed by the AT in several small steps. At the completion of a single phase command an interrupt is generated to the Host. This process is repeated, under Host control, until all of the necessary information packets have been transferred to the Host to execute that command as desired by the SCSI initiator.

Since the WD7000-ASC is a single threaded channel resource, commands can only be queued from either side, SCSI port or the Host AT port, when no data transfers are taking place across the channel. To limit LCPU overhead and SRAM space, no more than 16 commands can be queued at any given time. The queued commands are then executed in the order received by the LCPU as described above.

5.1.1 POWER-UP SEQUENCE

On RESET, the WD7000-ASC executes a Power-Up Sequence to setup internal parameters and initialize the onboard circuitry properly. The LCPU resets and initializes the SBIC device, followed by initialization of any required tables and default values. Further details can be obtained from the WD7000-ASC source listing. The minimum required warm RESET pulse width is 1.0uS for an operation of the SBIC at 10.0 MHZ. The LCPU (4 MHZ clock input) requires a reset pulsewidth of 3 clock cycles. For a cold start, the minimum RESET required is 1mS.

Onboard WD7000-ASC diagnostics will be executed for about 2 seconds. If an error is detected, the approprate error code is set in the interrupt status register that can be read by the Host after the LCPU has set the command port READY line. In order to detect any power-up diagnostic failures, the Host should first read this interrupt status register before requesting the WD7000-ASC to execute a command even though an IRQ is not set. Additionally, the LCPU does not turn off a LED to visually signal a diagnostic error condition. Details of the diagnostics are discussed in Section 6.

The LCPU is interrupt driven by the COMMAND PORT READY line from the Host controller for command execution. Having read the diagnostic status, the Host must then issue an INITIALIZATION command and pass 9 additional bytes using programmed I/O. The LCPU will then direct the DMA control logic to read off the command block as defined in the following paragraphs and prepare the WD7000-ASC for command execution.

5.2 HOST HARDWARE INTERFACE

The Host utilizes four I/O ports for WD7000-ASC control as defined in Table 5-1. Using only four ports keeps the requirements on Host I/O space to a minimum, so that only two of the lower address are decoded to access the R/W ports. Address lines A9-A3 are jumper configurable so that the WD7000-ASC can reside in any address space from 300-3FF. Additionally, the DMA and IRQ channels are user selectable. Refer to Section 3 for all of the jumper options available.

TABLE 5-1. WD7000-ASC I/O PORT DEFINITION

ADDRESS	READ PORT	TYPE	WRITE PORT	TYPE
0	WD7000-ASC Status	D7 - D4	Command Register	Byte
1	Host Interrupt Status	Byte	WD7000-ASC Acknowledge	Strobe
2	Reserved		Host Control Reg	
3	Reserved			

5.2.1 STATUS PORT = WD7000-ASC STATUS (TABLE 5-1)

The Host must read the status on power-up or before issuing any command through the command port. On RESET, this byte is cleared or set of all zeros. The format of the status byte is shown in Table 5-2.

TABLE 5-2. WD7000-ASC STATUS BYTE FORMAT

BIT	DESCRIPTION	MEANING
7	Interrupt Image Flag	0 = Interrupt Inactive 1 = Interrupt Active
6	Command Port Ready	0 = Port Busy 1 = Port Ready
5	Command Port Byte Rejected	0 = Byte Accepted 1 = Illegal Command Parameter
4	WD7000-ASC Initialized Flag	0 = Initialization Required 1 = WD7000-ASC Initialized
3	Reserved	Set To 1
2	Reserved	Set To 1
1	Reserved	Set To 1
0	Reserved	Set To 1

5.2.1.1 INTERRUPT IMAGE FLAG (D7)

This reflects the image of the hardwired interrupt to the Host. This enables the Host to poll the interrupt line when the WD7000-ASC interrupt is disbaled on the system board for some reason.

5.2.1.2 COMMAND PORT READY (D6)

This bit is useful to transfer command bytes in the programmed I/O mode. The Host can send the command byte when bit (6) of the status port is a 1. Writing a byte to the command port will reset this bit. The WD7000-ASC sets the bit when it is ready for the next byte. Using this handshake technique, the prearranged number of command bytes can be transferred.

5.2.1.3 COMMAND BYTE REJECTION (D5)

After the LCPU sets the READY line within about 70uS, the Host should also examine bit 5 of the status byte to check if the byte written was accepted. This is required since there is no other means other than the ICMB to warn the Host about an illegal command or parameter. The ICMB technique involves DMA transfer after the fact, making it difficult for the Host to take a corrective action.

This bit also informs the Host that an SCSI command has been entered in the SBIC queue or that a local WD7000-ASC command has completed execution. If the SBIC queue is full, then the Host command byte will always be rejected until space is available in the queue.

On power-up or during the INITIALIZATION command, this bit is set if any other command other than the INITIALIZATION command is issued. For the 9 subsequent bytes, it indicates a parameter out of range and the Host is required to send that byte again before transmitting the other command parameter.

5.2.1.4 WD7000-ASC INITIALIZED FLAG (D4)

When this bit is reset, the Host must issue an INITIALIZATION command to establish the mail box parameters so that commands can be executed properly using First Party DMA.

This bit is reset by the Host master reset (HMR or RESET DRV) at the interface or the WD7000-ASC reset port. After the INITIALIZATION command has been executed, this flag is set by the LCPU.

5.2.2 INTERRUPT STATUS BYTE

The Host read only registers also include an interrupt information byte that contains the mail box number pertaining to the current interrupt. Normally the interrupt information byte is valid only when the interrupt status bit is set implying that the Host CPU must read this register before acknowledging the interrupt. However, the diagnostic error code is also latched into this register since this event and a Host interrupt request are mutually exclusive events. The diagnostic error code is valid after power-up, reset, or a diagnostic command, after the LCPU has set the READY signal to the Host. The byte is formatted as shown in Table 5-3.

TABLE 5-3. INTERRUPT STATUS BYTE/DIAGNOSTIC ERROR CODE

BITS 7,6,5,4,3,2,1,0	DEFINITION
01	No Dianostic Error Occured
02	RAM Failure
03	FIFO Read/Write Failed
04	SBIC Register Read/Write Failed
05	Initialization D-FF Failed
06	Host IRQ D-FF Failed
07	ROM Checksum Error
10NNNNNN	Outgoing mailbox number 'N' is available. Used only when 'INTERRUPT ON FREE OGMB' command has been issued.
11NNNNNN	Incoming mailbox 'N' needs service.

5.2.3 COMMAND PORT

The Host issues WD7000-ASC control commands via the first write port to get its attention. All control commands are 1 byte instructions except the INITIALIZATION command which must be sent to the WD7000-ASC after power-up or WD7000-ASC reset. The other two byte exception is the SCSI soft reset. The format of this command is shown in Table 6-2.

The command port allows the Host to queue commands at any rate desired as opposed to just scanning the mail boxes once when the START MULTIPLE I/O command is issued. No more than 16 Host commands can be queued at any given time. When the queue is full, the command port byte will be rejected by the LCPU.

Table 6-1 list all commands that the Host can issue using the command port.

5.2.4 INTERRUPT ACKNOWLEDGE

This input strobe clears the hardware Interrupt Request to the Host. In the case of queued commands, the WD7000-ASC will not set the Interrupt unless the interrupts have been enabled by the Host and the previously set interrupt has been acknowledged by the Host.

The IRQ signal status to the queued but only after the command status has been written to the Host via the incoming mail box (as described in Section 6. The interrupt acknowledge signal clears the previous IRQ signal and frees up an ICMB so that it can be re-used. If the number of these mail boxes allocated is small, then the Host should service the interrupts as quickly as possible (about 100-200uS), else the execution time for the next command in the queue will be proportionately larger.

5.2.5 HOST CONTROL REGISTER

The Host can write to a control register to selectively enable or disable the functions indicated in Table 5-4. On power-up Reset or RESET DRV, all registers except the WD7000-ASC RESET register are cleared to all zeros.

TABLE 5-4. HOST CONTROL BYTE FORMAT

BIT	DESCRIPTION	MEANING
7	Reserved	Not Used
6	Reserved	Not Used
5	Reserved	Not Used
4	Reserved	Not Used
3	Interrupt Enable	0 = Interrupt Off 1 = Interrupt On
2	DMA Request Enable	0 = DRQ Disabled 1 = DRQ Enabled
1	SCSI Port Reset	0 = SCSI Reset Off 1 = SCSI Reset On
0	WD7000-ASC Reset (RESET DRV Sets This D-FF)	0 = WD7000-ASC Reset Off 1 = WD7000-ASC Reset On

5.2.5.1 WD7000-ASC RESET (DO)

This 1-bit register allows the Host to reset only the WD7000-ASC controller instead of the entire system using the RESET DRV input line at the Host interface. The Host writes twice to this port so that the reset pulsewidth can be tailored and onboard logic minimized without excessive use of the bus bandwidth on the AT backplane.

5.2.5.2 SCSI RESET (D1)

Similiar to the WD7000-ASC Reset except that the SCSI port is reset instead of the WD7000-ASC or the entire AT system. For software resets, refer to Section 6.

5.2.5.3 DMA REQUEST ENABLE (D2)

The Host can program the DRQ signal from being enabled/disabled on the Host bus by simply writing a 'I/O' to this D-FF. This is done so multiple devices can share the same DMA channel. The Host must write a '1' to this register before a IRQ signal is generated to the Host upon command completion or poll status of the IRQ signal via the Host status register.

5.2.5.4 INTERRUPT REQUEST ENABLE (D3)

The Host can program the IRQ signal from being enabled/disabled on the Host bus by simply writing a 'I/O' to this D-FF. This is done so multiple devices can share the same IRQ channel. The Host must write a '1' to this register before First Party DMA transfers by the WD7000-ASC can begin or poll the status of the IRQ signal via the Host status register.

5.3 MAIL BOXES

In order to fetch and execute a command block setup by the Host in it's system memory, the Host must provide the I/O channel with the starting address of the block. Likewise, when the WD7000-ASC completes a command, it must indicate to the Host the address of the CDB it has just completed. These handshakes are accomplished via outgoing and incoming mail box systems. The terms 'outgoing' and 'incoming' are with respect to the Host system. At system start-up, the Host issues the initialization command which sets the number of outgoing/incoming mail boxes and the starting address of mail box block. The relative mail box number is given in the command port control opcodes. The format of a typical mail box is shown in Table 5-5.

TABLE 5-5. MAIL BOX FORMAT

MAIL TYPE	CONTENTS
Outgoing #N	Mail Status (0 = empty, else full)
	Command Block Pointer (MSB)
	Command Block Pointer
	Command Block Pointer (LSB)
Incoming #M	Action Status
	Command Block Pointer (MSB)
	Command Block Pointer
	Command Block Pointer (LSB)

OGMB Address = Starting address of mail box + mail box number N x 4
ICMB Address = Starting address of mail box + mail box number M x 4
+ 4 (total number of OGMBs)

Where 0 <=N <=P-1 and 0 <=M <=Q-1

N,M = mail box offset numbers from 0 to 63 (maximum)
P,Q = number of OGMBs/ICMBs respectively (maximum 64)

Note: These mail boxes do not occur in pairs. In fact, the number of OGMBs is independent of the number of ICMBs. All OGMBs are presumed to be assigned consecutive memory locations, followed by all of the ICMB assignments.

5.3.1 OUTGOING MAIL

An outgoing mail box is marked full or empty by the mail box status byte. A value of zero means that the WD7000-ASC has picked up mail that may have been in the box, and the Host may issue a new command via that particular box. A non-zero value indicates a full box which the WD7000-ASC has not had time to service.

After the Host has set up the OGMB command pointer, it sets the status byte to full (non-zero). The Host then notifies the WD7000-ASC to either check all the boxes, starting with a particular mail box number, or just a single mail box via the direct WD7000-ASC START commands. The WD7000-ASC reads the necessary amount of mail boxes and marks them empty. Generally, the commands are executed on a first come basis. If disconnect is supported within the SCSI system, several commands could be in progress and the order of completion may not be the same as the start.

? show do we correct a reject command w/ actual command if it was in a queue? or does this only mean queue full at this time?

Since the WD7000-ASC has a limited number of SRAM and I/O sub-channels, it cannot concurrently process an infinite number of commands. Once the WD7000-ASC has occupied all of it's sub-channels it will respond to START commands with rejected status. It will not empty a mail box until it has completed a pending I/O command. The Host will know that the WD7000-ASC limit has been reached by the fact that all the OGMBs are full or that the command is rejected. At this time the Host has two options: it may continue to poll for an empty mail box or it may issue an INTERRUPT ON FREE OGMB command. AS soon as the
WD7000-ASC has freed an OGMB an interrupt is generated and the proper status is reported to the Host.

5.3.2 INCOMING MAIL

The ICMB is used to notify the Host which command has completed execution or which other SCSI initiator has requested service. The WD7000-ASC code, indicating completion or Host attention, is the first byte in an ICMB. The next three bytes point to the command block in memory that the WD7000-ASC just finished executing. These bytes are the link back from the WD7000-ASC to the operating system I/O driver that generated the command block. In the case of another SCSI initiator, or for interrupts with no associated CDB, these three bytes are defined as indicated in the ICMB return status byte values in Table 5-6, otherwise, they are meaningless.

5.3.2.1 ICMB RETURN STATUS

The ICMB Return Status bytes are broken down to two classes. The first class (00-7F) is known as solicted interrupt status. These are codes accompanying interrupts which were in response to a Host command to the WD7000-ASC. The second class, unsolicited interrupts, accompany an interrupt as a result of a WD7000-ASC detected condition. These interrupts do not have a corressponding Host request (CDB) for an interrupt. Besides Host service attention service, these codes are typically used for reporting an error condition that can be treated as solicited interrupts if an error logger exists in the Host system to record their occurance. The Host can disable or enable unsolicited interrupts via SCB commands described in Section 6. The codes which can be returned in the return status bytes are defined in Table 5-6.

TABLE 5-6. ICMB RETURN STATUS BYTE VALUES

CODE	DEFINITION/EFFECT
00	Reserved
01	Command Complete; No Errors
02	Command Complete, Error Logged In SCB/ICB Status Area
03	Reserved
04	Command Failed To Complete; Time-Out Error
05	Command Terminated; Bus Reset By External Device
06	Unexecutable Command Received As Target
07->7F	Reserved
80	Unexpected Reselection; Byte 1 = Target ID; Byte 2 = LUN
81	Unexpected Selection; Byte 1 = Initiator ID; Byte 2 = LUN
82	Abort Command Message; Byte 1 = Initiator ID; Byte 2 = LUN
85	Reserved
83	SCSI Bus Software Reset
84	SCSI Bus Hardware Reset
86->FF	Reserved

5.4 COMMAND BLOCKS (CB)

In order to perform a WD7000-ASC interface channel operation, the Host must first build a command block in memory. Two types of command blocks are defined. The first type, a SCSI Command Block (SCB), is intended to be processed by an SCSI device utilizing the Host adapter as the DMA channel into Host memory. The SCB is always used when the WD7000-ASC is operating as the initiator. The Interface Command Block (ICB) contains a functional command to be executed by the WD7000-ASC which may sometimes involve the SCSI bus, especially when selected as a target by another SCSI initiator, else it is intended for local execution. The SCSI Command Block is presented in Table 5-7.

TABLE 5-7. SCSI COMMAND BLOCK

BYTE	BIT POSITION/DESCRIPTION							
	7	6	5	4	3	2	1	0
00	S/I	Command Opcode						
01	Target ID				0		LUN	
02	SCSI Command Block (Byte #1)							
thru	SCSI Command Block (Bytes 2 - 11)							
13	SCSI Command Block (Byte #12)							
14	SCSI Return Status Block (Byte #1)							
15	Vendor Unique Error Status							
16	Maximum Data Transfer Length (MSB)							
17	Maximum Data Transfer Length							
18	Maximum Data Transfer Length (LSB)							
19	SCSI Data Block Pointer (MSB)							
20	SCSI Data Block Pointer							
21	SCSI Data Block Pointer (LSB)							
22	Next Command Link Pointer (MSB)							
23	Next Command Length Pointer							
24	Next Command Link Pointer (LSB)							
25	Write	Reserved For Future Expansion						
thru	Reserved For Future Expansion							
31	Reserved For Future Expansion							

The MSB of the first byte (00) indicates whether the CB is intended for an SCSI port execution or meant for execution by the WD7000-ASC. A value of 00 specifies a SCSI command where the WD7000-ASC acts as the SCSI initiator. Values of 01-7F (Hex) are reserved for future expansion. Values of 80-FF are used as WD7000-ASC command codes.

Byte 1 contains sufficient information for the LCPU to direct the SBIC to start arbitration and the selection process.

Bytes 2 through 13 are written to the SBIC device. The other bytes are used to access additional parameters required to complete the command. The command completion status, as generated by the selected SCSI LUN, is logged into byte 14.

Byte 15 is used to write the vendor unique error code.

Bytes 16 - 18 if the target transfers more or less than the number of bytes specified in this field, the WD7000-ASC will complete the command but will return a vendor unique error code informing the Host that this occurred. No provision has been made at this time to return count of the actual number of bytes transferred across the SCSI bus. This diagnostic capability will be added to the firmware at a future date.

Bytes 22 - 24 provide the next SCB address which will be used by the WD7000-ASC with chained commands, i.e. next command to be executed after the current command has been completed, depending upon the LINK bit in the SCSI CDB.

Byte 25, bit 7 is really a direction bit and not a write protection bit as implied. Accordingly, bit 7 should be interpreted to mean the following:

Bit 7 = 0 : implies a read operation from Host memory.
Bit 7 = 1 : implies a write operation to the Host memory.

If this direction bit is set incorrectly for the present operation, the WD7000-ASC will return an error code without invitiating any SCSI data transfer. The SCSI read operation should have this bit set. A SCSI write to the disk should have this bit reset.

Figures 5-1 and 5-2 illustrates the start of command execution and completion using the mail box system.

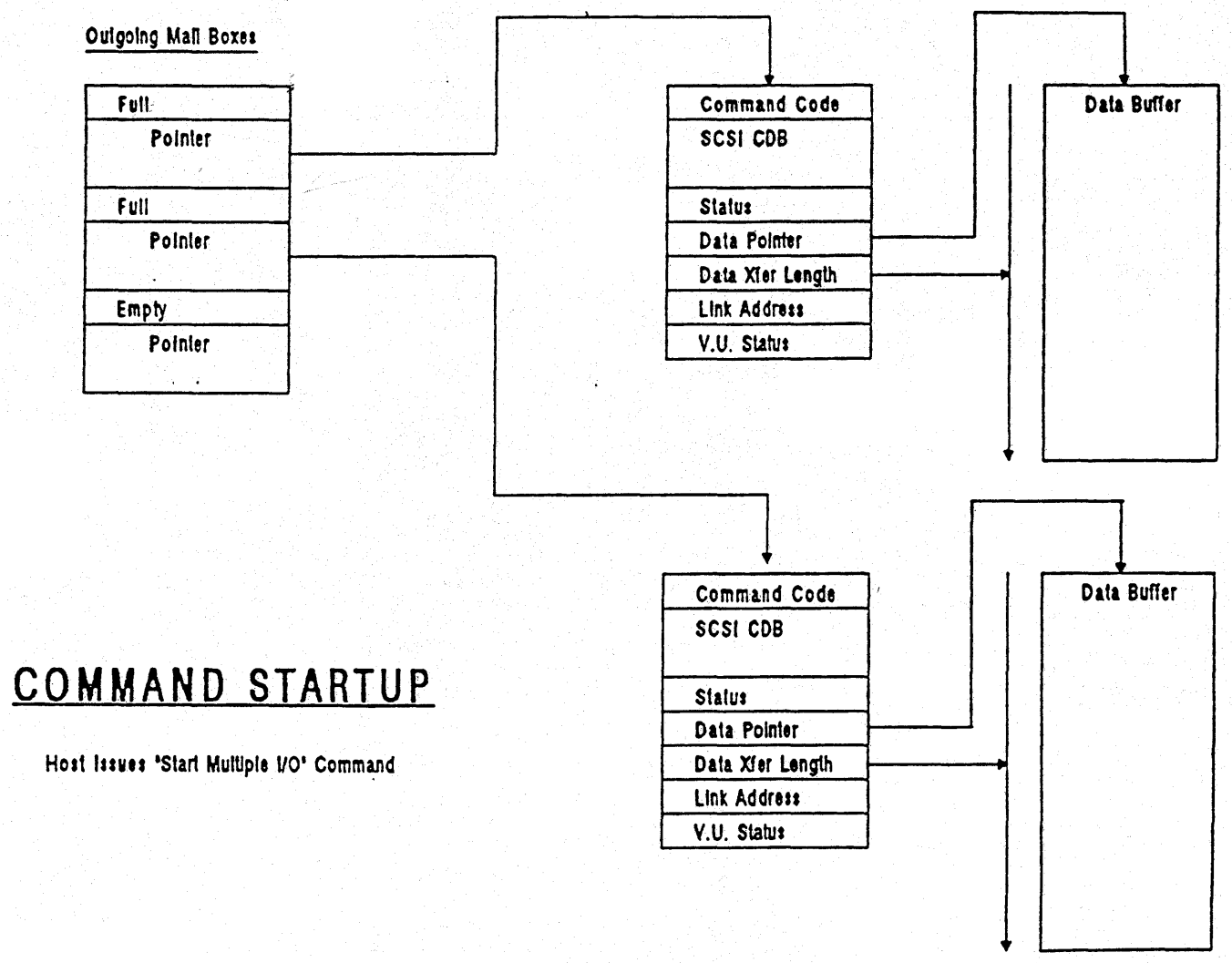


FIGURE 5-1. EXECUTION OF SCB/ICB

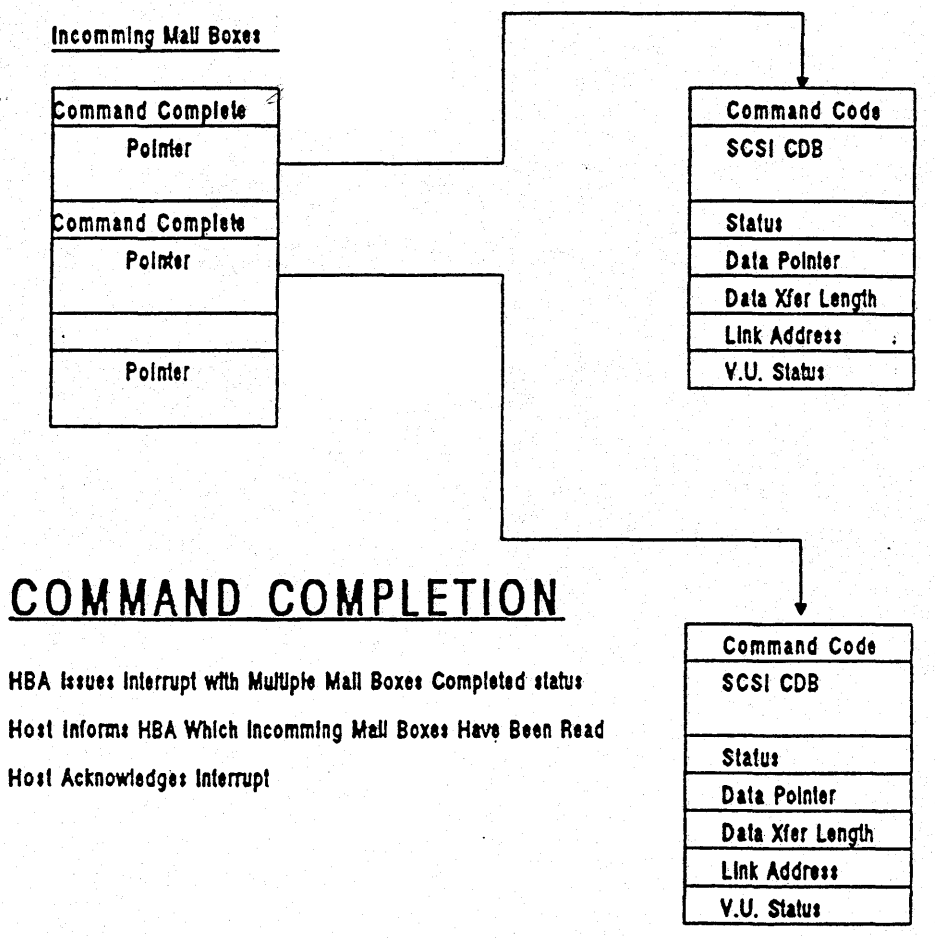


FIGURE 5-2. COMPLETION OF SCB/ICB

5.4.1 INTERFACE COMMAND BLOCK (ICB)

The ICB is comprised of the command byte, six parameters bytes, and a status byte as shown in Table 5-8. The six parameter commands are defined by the WD7000-ASC commands described in Section 6.

TABLE 5-8. ICB COMMAND EXECUTION BLOCK

	BIT POSITION/DESCRIPTION							
BYTE	7	6	5	4	3	2	1	0
00	S/I	Command Opcode						
01	ICB Parameter Byte # 1							
02	ICB Parameter Byte # 2							
03	ICB Parameter Byte # 3							
04	ICB Parameter Byte # 4							
05	ICB Parameter Byte # 5							
06	ICB Parameter Byte # 6							
07	ICB Parameter Byte # 7							
08	ICB Parameter Byte # 8							
09	ICB Parameter Byte # 9							
10	ICB Parameter Byte # 10							
11	ICB Parameter Byte # 11							
12	ICB Parameter Byte # 12							
13	ICB Parameter Byte # 13							
14	ICB Parameter Byte # 14							
15	WD7000-ASC Vendor Unique Error Status							

5.5 COMMAND QUEUING

To keep the LCPU overhead and the RAM requirements to a minimum, 16 logical threads will be supported. No more than than 16 Host and/or 16 SCSI commands can be pending execution on the WD7000-ASC. Commands will be processed on a FIFO basis. No more than 1 command per LUN can be queued, i.e., any given LUN can only have 1 command pending or in execution but never both. To manage command execution properly, 3 queues are used. The Host and the SBIC queues both support 16 commands each. The Host interrupt queue can handle up to 32 command completions, subject to the number if ICMBs specified by the Host. These 3 queues are serviced in a 'round robin' fashion.

To begin, the Host issues a command by writing a byte into the command port using programmed I/O. If the command specifies a mail box access then it is queued, else it is executed immediately. In either case, the READY signal is set in about 70uS, and the Host should read the status register to check if the command byte has been accepted.

After the command has been entered in the Host queue, the specified mail box is accessed to begin command execution. If the command is an SCSI command, then it is entered in a separate queue, or else it a local WD7000-ASC command that is to be executed. As long as the command to be executed does not require any additional data for completion, it is executed without further delay. However, if data trasnfer is required, the Host memory is accessed again provided no previous data transfer is in progress. If the bus is being used by the DMA channel, then command execution is suspended until freed by the DMA channel. If the data bus is being used by the LCPU to complete command execution, then DMA transfers cannot start until the LCPU has finished accessing the Host memory.

When the command has completed execution, the Host is notified via the ICMB. Once again the same data transfer in progress restrictions apply to write the ICMB data to the Host. After successful ICMB completion, the command is removed from the Host queue, and the interrupt status byte specifying the ICMB used is entered in another queue designed solely to interrupt the Host.

If the previous interrupt has been acknowledged by the Host, then the Host will be notified of the next command completion entered in this queue. The interrupt acknowledge is also used to free a previously used ICMB so that it can be re-used. If the number of ICMBs specified by the Host is small, then the interrupt request should be serviced by the Host within 200uS in order to avoid delaying the execution of the next command entered in the Host queue.

New commands are issued to the desired target providing the previous target has disconnected from the SBIC device. If no other exception handling is required, then command completion is reported to the Host in a manner similiar to that described. The completed command is then removed from the SBIC queue.

5.6 SCSI PROTOCOL

The SCSI Protocol followed is defined by ANSI SCSI Specification X3T9.2. The WD33C93-SBIC data sheet specifies the protocol requirements used for the WD7000-ASC design for all communication with the SCSI port.

5.6.1 WD7000-ASC SUPPORT MESSAGES

The SCSI message system allows communication between an intiator and the target for the purpose of physical path management.

Most SCSI messages, shown in Table 5-9, are handled by the LCPU totally transparent to the Host CPU. In addition, hooks for some messages like ABORT command and SCSI RESET messages have been provided via the ICB, since these are useful at the Host level as well. These are indicated by the letter H (for Host) followed by the opcode of the WD7000-ASC command which describes the action that takes place. If a message is not supported, it is marked NS (not supported). Among the extended messages only the synchronous data transfer request message is supported.

TABLE 5-9. WD7000-ASC SUPPORTED MESSAGES

SCSI MSGE	DESCRIPTION	MODE Of OPERATION INITIATOR	TARGET
00	Command Complete		H:85, 87, 88
01	Extended Message		
02	Save Data Pointer		NS
03	Restore Pointer		NS
04	Disconnect		
05	Initiator Detected Error		
06	Abort	H:81	
07	Message Reject		
08	No Operation		
09	Message Parity Error		
0A	Linked Command Complete		NS
0B	Linked Command Complete With Flag		NS
0C	Bus Device Reset	H:81	
80-FF	Identify		

5.7 EXCEPTION HANDLING

To be furnished.

SECTION 6

COMMANDS

6.0 GENERAL

The commands supported by the WD7000-ASC fall into two broad catergories; SCSI commands, and commands executed by the WD7000-ASC. The SCSI commands are merely passed through the WD7000-ASC with the LCPU handling all of the required handshakes to accomplish such a transfer. The commands executed by the WD7000-ASC include setup and execution of commands by the Host as the initiator or as the target. In the Initiator mode, the SCSI Command Block (SCB) contains all of the necessary information to execute the entire command. In the Target mode, the Host sets up the WD7000-ASC, using the Interface Command Block (ICB) format to execute the command in several small steps. In either mode, the command port is always available to the Host to control the WD7000-ASC. The ICB format can also be used to control the WD7000-ASC if desired. The distinction is that command port commands are usually 1 byte action commands using programmed I/O, whereas for SCB or ICB, First Party DMA access is required to complete the command.

The diagnostic error code is not valid until the READY status has been set. After READY has been set following diagnostics, no other command except INITIALIZATION (Opcode 01) will be accepted until all 10 bytes have been received successfully. If a byte is rejected in this process, the Host must re-issue that byte.

6.1 COMMAND PORT CONTROL OPCODES

The control commands in Table 6-1 are issued by the Host by writing to the command port. Only the INITIALIZATION command is multi-byte, the other commands require only a single byte.

TABLE 6-1. WD7000-ASC COMMAND PORT OPCODES

OPCODE	DEFINITION
00	No Operation
01	Initialization (10 byte sequence)
02	Disable Unsolicited Interrupts
03	Enable Unsolicited Interrupts
04	Interrupt on Free OGMB
05	SCSI Soft Reset
06	SCSI Hard Reset Acknowledge
07-7F	Reserved
10NNNNNN	Start Command in OGMB #N
11NNNNNN	Start Multiple I/O (Scan mail boxes) N = Scan Signature 6 bits maximum.

6.1.1 NO OPERATION (00)

This command does nothing other than toggle bit 6 of read status port 0. Useful for diagnostic reasons to make sure that the LCPU is at least functioning partially.

6.1.2 INITIALIZATION (01)

The INITIALIZATION command which is sent to the WD7000-ASC after power-on or WD7000-ASC reset. The Host can send the command byte when byte 6 of the WD7000-ASC status port is 1. Writing a byte to the command port will reset this bit. The WD7000-ASC sets the bit when it is ready for the next byte. Using this programmed I/O technique, the remaining 9 bytes of the INITIALIZATION command can be sent to the WD7000-ASC. These 9 bytes establish the number of outgoing and incoming mail boxes and the starting address of the entire mail box block, and the bus on/off times. All other programmable parameters can be selected by the Host via an ICB.

The OGMBs are followed by the ICMBs so that the relative mail box number, specified by the control port command byte, can be added to the 3 byte base address specified in Table 6-2 to compute the absolute mail box address. The mail box or any of the data blocks do not wrap around memory from the highest 24 bit memory address to the lowest memory address of zero.

In Table 6-2, a value of zero in bytes 8 and 9 will be taken to imply that at least 1 OGMB and 1 ICMB are allocated by the Host. The maximum value that the Host can specify in these 2 bytes is 64 instead of 63.

bus time on/off

If byte 2 is set to zero and a DMA transfer is required, at least one word will be transferred by the First Party DMA controller before giving up the Host bus. A value of zero in byte 3 implies that the DMA controller will relinguish the bus for only 125nS before re-arbitrating for it again. The maximum on time used should be less than 15uS less all overhead time required to allow the Host to service memory refresh cycles, including DMA bus arbitration time. The WD7000-ASC DMA controller transfers a word every 375nS once it has control of the bus. For optimum performance, the Host should use a bus on time of 3.0uS (or greater) to transfer eight words, the length of the FIFO. Bus arbitration overhead is about 2 to 3uS.

TABLE 6-2. INITIALIZATION COMMAND FORMAT

BYTE NUM.	BIT POS. 7654 3210	DEFINITION
00	0000 0001	Command Opcode
01	0000 0SSS	3 Bit SCSI WD7000-ASC ID Field and Options
02	TTTT TTTT	Bus On Time (125ns per count value)
03	TTTT TTTT	Bus Off Time (125ns per count value)
04	0000 0000	Reserved
05	AAAA AAAA	Starting Address of Mail Block (MSB)
06	AAAA AAAA	Starting Address of Mail Block
07	AAAA AAAA	Starting Address of Mail Block (LSB)
08	ONNN NNNN	Number of OGMB (maxium 64) (0,1 = 1)
09	ONNN NNNN	Number of ICMB (maxium 64) (0,1 = 1)

24 bits

6.1.3 DISABLE UNSOLICITED INTERRUPTS (02)

This command allows the Host to turn off interrupts generated by another initiator on the SCSI bus. In this mode, the WD7000-ASC will not respond as a target.

6.1.4 ENABLE UNSOLICITED INTERRUPTS (03)

This command allows the Host to turn on interrupts generated by another initiator on the SCSI bus, depending upon the bit mask set by the Host.

The interrupt due to a SCB/ICB command execution are always set. The Host may program the IRQ enable on/off and poll the selected interrupt channel instead.

6.1.5 INTERRUPT ON FREE OGMB (04)

This command is issued by the Host when all of the OGMBs have been used and it does not wish to scan for an available OGMB. The WD7000-ASC will generate an interrupt to the Host as soon as one is available. The relative OGMB number can be read by the Host from the interrupt status byte (WD7000-ASC read port 01).

6.1.6 START COMMAND (80 - BF)

These opcodes are used to start the execution of a single I/O command pointed by a specific OGMB. The lower 6 bits of the opcode are used to specify the OGMB number.

6.1.7 START MULTIPLE I/O (CO - FF)

This command is provided so that the Host can initiate multiple commands at the same time. The WD7000-ASC LCPU will scan all the OGMBs and execute the commands pointed to, if the mail box full status has been set by the Host. This non-zero byte can be used by the Host to identify the 6-bit signature passed with the SCAN command, so that only mail boxes bearing the correct signature will be executed. The order of execution is on a FIFO basis, starting with the base address of the OGMB, up to the maximum number of OGMBs specified with the INITIALIZATION command. At the completion of each command a separate interrupt will be generated. This simplifies the ICMB information reported back to the Host since holes can exist in the OGMBs.

The SCAN MAIL BOX command may be somewhat inefficient because the mail box memory is scanned in blocks of 16 bytes per command execution poll sequence starting from the base address. Depending upon which OGMB contains the command to be executed, the overhead incurred in command execution could be significant. Compared to executing a command contained in a specific OGMB, the computation time of the OGMB address and all associated handling, eventhough small, adds to the execution time of a given command.

6.2 WD7000-ASC COMMANDS (ICB)

WD7000-ASC commands include all of the Host adapter functions which are outside the scope of the SCSI INITIATOR specification. These functions include operation as a target in a Host/Host communication activity, DMA bus release timing, SCSI device reset control, etc.

For all of the commands supported, the WD7000-ASC will signal completion of the command by loading an ICMB and interrupting. The interrupt status byte contains the relative mail box number. The Host acknowledges the interrupt by sending an interrupt acknowledge to complete the handshake. The ICB commands supported are summarized in Table 6-3.

TABLE 6-3. ICB COMMAND OPCODES

OPCODE	DEFINITION
80	Open Receive Buffer (as a target)
81	Receive Command From Another Initiator
82	Receive Data From Another Initiator
83	Receive Data With Status From Another Initiator
84	Send Data To Another Initiator
85	Send Data With Status To Another Initiator
86	Send Command Status To Another Initiator
87	Reserved
88	Read Initialization Bytes
89	Read WD7000-ASC SCSI ID
8A	Set Unsolicated Interrupt Mask
8B	Read Unsolicited Interrupt Mask
8C	Read Firmware Revision Level
8D	Execute On-board Diagnostics
8E	Set Execution Parameters
8F	Read Execution Parameters

6.2.1 OPEN RECEIVE BUFFER (80)

To operate as a target, the WD7000-ASC must be given a place to put an incoming network message. The Host must define a buffer starting address and buffer length for an anticipated message. This operation is performed by the OPEN RECEIVE BUFFER command.

After the Host has determined that another SCSI initiator wants to send a message, it issues this command to the WD7000-ASC. This enables the WD7000-ASC to act as a target and accept an SCSI SEND command to any of the Host LUNs specified in the LUN acceptance vector.

The LUN acceptance vector defines the target LUNs (i.e., LUNs associated with the AT bus) which will accept WD7000-ASC write data from an initiator. Each bit position corresponds to a LUN. To enable responses on LUNs 7 and 0, the acceptance vector would be set to 81H. The Open Receiver Buffer ICB Format is presented in Table 6-4.

TABLE 6-4. OPEN RECEIVER BUFFER ICB FORMAT

	BIT POSITION / DESCRIPTION							
BYTE	7	6	5	4	3	2	1	0
00	1	0	0	0	0	0	0	0
01	LUN Acceptance Vector							
02	Receive Buffer Length in Bytes (MSB)							
03	Receive Buffer Length in Bytes							
04	Receive Buffer Starting Address (LSB)							
05	Receive Buffer Starting Address (MSB)							
06	Receive Buffer Starting Address							
07	Receive Buffer Starting Address (LSB)							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

6.2.2 RECEIVE COMMAND (81)

The RECEIVE command specifies a command buffer to the WD7000-ASC so that it can request and receive command information from another initiator. This information is stored in the system memory designated by the Host.

A RECEIVE command may be issued in response to, or in anticipation of, the WD7000-ASC being selected by another initiator. If this command is issued before selection, it allows the WD7000-ASC to receive the command information immediately after being selected since a designated system memory area has already been assigned. If issued after selection, the WD7000-ASC is forced to disconnect and reselect the initiator to receive the command information since a receive memory block was not pre-assigned by the Host. In either case, the WD7000-ASC will send the disconnect message and disconnect from the SCSI bus after receiving the specified number of command bytes. The number of the command bytes are specified by the 3 MSBs of byte 0 in the SCSI command block. The lower 5 bits specify the SCSI command opcode. The WD7000-ASC will signal completion of the command by loading an ICMB and interrupting. The Receive Command ICB Format is presented in Table 6-5.

TABLE 6-5. RECEIVE COMMAND ICB FORMAT

BYTE	BIT POSITION / DESCRIPTION							
	7	6	5	4	3	2	1	0
00	1	0	0	0	0	0	0	1
01	SCSI Device ID			0	0	LUN		
02	Command Buffer Length (MSB)							
03	Command Buffer Length							
04	Command Buffer Length (LSB)							
05	Command Buffer Starting Address (MSB)							
06	Command Buffer Starting Address							
07	Command Buffer Starting Address (LSB)							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

6.2.3 RECEIVE DATA (82)

RECEIVE DATA commands the WD7000-ASC to reconnect to an initiator, request and receive data, and disconnect from the bus. Specifically, the WD7000-ASC arbitrates for the bus, reselects the initiator, sends the Identify message, request and receives the specified number of data bytes, and stores them into the designated data buffer in the Host memory. It then sends the Save Data Pointer massage followed by the Disconnect message and then disconnects from the SCSI bus. Table 6-6 presents the Receive Data ICB Format.

TABLE 6-6. RECEIVE DATA ICB FORMAT

BYTE	BIT POSITION / DESCRIPTION							
	7	6	5	4	3	2	1	0
00	1	0	0	0	0	0	1	0
01	SCSI Device ID			0	0	LUN		
02	Data Buffer Length (MSB)							
03	Data Buffer Length							
04	Data Buffer Length (LSB)							
05	Data Buffer Starting Address (MSB)							
06	Data Buffer Starting Address							
07	Data Buffer Starting Address (LSB)							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

6.2.4 RECEIVE DATA WITH STATUS (83)

RECEIVE DATA WITH STATUS commands the WD7000-ASC to reconnect to an initiator, request and receive data, send status and then disconnect from the bus to terminate the I/O operation. Specifically, the WD7000-ASC arbitrates for the bus, reselects the initiator, sends the Identify message, request and receives the specified number of data bytes, and stores them into the designated data buffer in the Host memory. If a recoverable error occurs, the WD7000-ASC sends the Save Data Pointer message followed by a single completion message and disconnects from the SCSI bus.

If a non-recoverable error occurs, the WD7000-ASC does not send the Save Data Pointer message and the completion status byte. Instead, it disconnects from the bus without sending a Disconnect or Command Complete message. In either case, the WD7000-ASC will load an ICMB and interrupt the Host after disconnecting from the SCSI bus. Table 6-7 represents the Receive Data With Status ICB Format.

TABLE 6-7. RECEIVE DATA WITH STATUS ICB FORMAT

	BIT POSITION / DESCRIPTION							
BYTE	7	6	5	4	3	2	1	0
00	1	0	0	0	0	0	1	1
01	SCSI Device ID			0	0	LUN		
02	Data Buffer Length (MSB)							
03	Data Buffer Length							
04	Data Buffer Length (LSB)							
05	Data Buffer Starting Address (MSB)							
06	Data Buffer Starting Address							
07	Data Buffer Starting Address (LSB)							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

6.2.5 SEND DATA (84)

SEND DATA commands the WD7000-ASC to reconnect to an initiator, request and send data, and disconnect from the bus. The WD7000-ASC arbitrates for the bus, reselects the initiator, sends the Identify message, request and sends the specified number of data bytes from the designated data buffer in the Host memory. It then sends the Save Data Pointer message followed by the Disconnect message and then disconnects from the SCSI bus. Table 6-8 presents the Send Data ICB Format.

TABLE 6-8. SEND DATA ICB FORMAT

	BIT POSITION / DESCRIPTION							
BYTE	7	6	5	4	3	2	1	0
00	1	0	0	0	0	1	0	0
01	SCSI Device ID			0	0	LUN		
02	Data Buffer Length (MSB)							
03	Data Buffer Length							
04	Data Buffer Length (LSB)							
05	Data Buffer Starting Address (MSB)							
06	Data Buffer Starting Address							
07	Data Buffer Starting Address (LSB)							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

6.2.6 SEND DATA WITH STATUS (85)

SEND DATA WITH STATUS commands the WD7000-ASC to reconnect to an initiator, request and send data, send status and then disconnect from the bus to terminate the I/O operation.

The WD7000-ASC arbitrates for the bus, reselects the initiator, sends the Identify message, requests and sends the specified number of data bytes from the designated buffer in the Host memory. If a recoverable error occurs, the WD7000-ASC sends the Save Data Pointer message followed by a single completion status byte with data equal to OOH. It then sends the Command Completion message and disconnects from the SCSI bus.

If a recoverable error occurs, the WD7000-ASC does not send the Save Data Pointer message and the completion status byte. Instead, it disconnects from the bus without sending a Disconnect or Command Complete message. In either case, the WD7000-ASC will load an ICMB and interrupt the Host after disconnecting from the SCSI bus. Table 6-9 presents the Send Data With Status ICB Format.

TABLE 6-9. SEND DATA WITH STATUS ICB FORMAT

BYTE	BIT POSITION / DESCRIPTION							
	7	6	5	4	3	2	1	0
00	1	0	0	0	0	1	0	1
01	SCSI Target ID			0	0	LUN		
02	Data Buffer Length (MSB)							
03	Data Buffer Length							
04	Data Buffer Length (LSB)							
05	Data Buffer Starting Address (MSB)							
06	Data Buffer Starting Address							
07	Data Buffer Starting Address (LSB)							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

6.2.7 SEND STATUS (86)

SEND STATUS commands the WD7000-ASC to reconnect to an initiator, request and send status, and disconnect from the bus.

The WD7000-ASC arbitrates for the bus, reselects the initiator, sends the Identify message, requests and sends the specified completion status byte(s) from the ICB in the Host memory. It then sends the Command Complete message and disconnects from the SCSI bus. Table 6-10 presents the Send Status ICB Format.

TABLE 6-10. SEND STATUS ICB FORMAT

BYTE	BIT POSITION / DESCRIPTION							
	7	6	5	4	3	2	1	0
00	1	0	0	0	0	1	1	0
01	SCSI Device ID			0	0	LUN		
02	Completion Status Byte 1							
03	Reserved							
04	Reserved							
05	Reserved							
06	Reserved							
07	Reserved							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

6.2.8 READ INITIALIZATION BYTES (88)

This command reads the initialization bytes written by the Host into the system memory area designated by the Host. Bytes 2 through 8 are written depending upon the length of the chosen data field. A value of zero will result in no bytes being written by the WD7000-ASC, and a value greater than 8 will be reported as an error. The format and order of the bytes is the same as the INITIALIZATION command. Table 6-11 presents the Read Initialization Bytes ICB Format.

TABLE 6-11. READ INITIALIZATION BYTES ICB FORMAT

	BIT POSITION / DESCRIPTION							
BYTE	7	6	5	4	3	2	1	0
00	1	0	0	0	1	1	0	1
01	Reserved							
02	Data Buffer Length (MSB)							
03	Data Buffer Length (set to zero)							
04	Data Buffer Length (LSB) (maximum 8)							
05	Data Buffer Starting Address (MSB)							
06	Data Buffer Starting Address							
07	Data Buffer Starting Address (LSB)							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

6.2.9 READ WD7000-ASC DEVICE ADDRESS (89)

This commands the WD7000-ASC to write it's own SCSI ID into Byte 01, and Bits 7-5 of the ICB command block. Table 6-12 presents the Read WD7000-ASC Device Address ICB Format.

TABLE 6-12. READ WD7000-ASC DEVICE ADDRESS ICB FORMAT

	BIT POSITION / DESCRIPTION							
BYTE	7	6	5	4	3	2	1	0
00	1	0	0	0	1	0	0	1
01	SCSI WD7000-ASC ID			0	0	0	0	0
02	Reserved							
03	Reserved							
04	Reserved							
05	Reserved							
06	Reserved							
07	Reserved							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

6.2.10 SET UNSOLICITED INTERRUPT MASK (8A)

This command allows the Host to choose the error conditions which will generate an unsolicited interrupt. If any bit of byte 1 is set, then the error condition corresponding to that bit will not generate an interrupt.

On power-up byte 1 is presumed to be zero so that any error condition listed will cause an unsolicited interrupt until the interrupt has been set by the Host. Table 6-13 presents the Set Unsolicited Interrupt Mask ICB Format.

TABLE 6-13. SET UNSOLICITED INTERRUPT MASK ICB FORMAT

	BIT POSITION / DESCRIPTION							
BYTE	7	6	5	4	3	2	1	0
00	1	0	0	0	1	0	1	0
01	Unsolicited Interrupt Mask (see legend)							
02	Reserved							
03	Reserved							
04	Reserved							
05	Reserved							
06	Reserved							
07	Reserved							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

Legend: Interrupt Mask: 1 = Masked 0 = Unmasked

Bit	Unsolicited Interrupt	Bit	Unsolicited Interrupt
0	Unexpected Reselection	4	Bus Reset
1	ID Error (any SCSI device)	5	WD7000-ASC Error
2	Abort (received)	6	Unexpected Selection
3	Bus Device Reset (received)	7	Reserved

6.2.11 READ UNSOLICITED INTERRUPT MASK (8B)

This command allows the Host to read the mask established by the previous SET UNSOLICITED INTERRUPT MASK command or the byte presumed after the power-up condition. Byte 1 is written by the WD7000-ASC into the Host ICB memory area. Table 6-14 presents the Read Unsolicited Interrupt Mask ICB Format.

TABLE 6-14. READ UNSOLICITED INTERRUPT MASK ICB FORMAT

BYTE	BIT POSITION / DESCRIPTION 7	6	5	4	3	2	1	0
00	1	0	0	0	1	0	1	1
01	Unsolicited Interrupt Mask (see legend)							
02	Reserved							
03	Reserved							
04	Reserved							
05	Reserved							
06	Reserved							
07	Reserved							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

Legend: Interrupt Mask: 1 = Masked 0 = Unmasked

Bit	Unsolicited Interrupt	Bit	Unsolicited Interrupt
0	Unexpected Reselection	4	Bus Reset
1	ID Error (any SCSI device)	5	WD7000-ASC Error
2	Abort (received)	6	Unexpected Selection
3	Bus Device Reset (received)	7	Reserved

6.2.12 READ FIRMWARE REVISION LEVEL (8C)

This command allows the Host to read the WD7000-ASC firmware revision level. Byte 1 provides the primary revision level and byte 2 represents the secondary revision level. Table 6-15 presents the Read Firmware Revision ICB Format.

TABLE 6-15. READ FIRMWARE REVISION LEVEL ICB FORMAT

	BIT POSITION / DESCRIPTION							
BYTE	7	6	5	4	3	2	1	0
00	1	0	0	0	1	1	0	0
01	Primary Revision Level (*)							
02	Secondary Revision Level (*)							
03	Reserved							
04	Reserved							
05	Reserved							
06	Reserved							
07	Reserved							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

6.2.13 EXECUTE DIAGNOSTICS (8D)

This command allows the Host to execute WD7000-ASC diagnostics whenever desired. The power-up WD7000-ASC diagnostics does not exercise the First Party DMA controller and the FIFO since the system memory will be destroyed. This command allows the Host to designate a specific memory area for such a purpose.

The LCPU normally executes diagnostics for the PROM, SRAM, SBIC task file registers, command and status ports, in that order. The First Party DMA logic is not tested unless specifically requested by the Host in the diagnostic type code (byte 1) as shown in Table 6-16. The contents of the specified memory area will be destroyed by the LCPU. Several data patterns are written and read back to ensure data integrity. Table 6-16 presents the Execute Diagnostics ICB Format.

TABLE 6-16. EXECUTE DIAGNOSTICS ICB FORMAT

	BIT POSITION / DESCRIPTION							
BYTE	7	6	5	4	3	2	1	0
00	1	0	0	0	1	1	0	1
01	Diagnostic Type Code							
02	Data Buffer Length (MSB)							
03	Data Buffer Length							
04	Data Buffer Length (LSB)							
05	Data Buffer Starting Address (MSB)							
06	Data Buffer Starting Address							
07	Data Buffer Starting Address (LSB)							
08	Reserved							
09	Reserved							
thru	Reserved							
14	Reserved							
15	Vendor Unique Error Code							

Legend: Diagnostic Type Code
0 = Execute Normal Power-Up Diagnostics Only
1 = Execute Walking 1's Pattern Diagnostics
2 = Execute DMA System Memory Diagnostics
3 = Execute Both Options 1 + 2 Above

6.2.14 SET EXECUTION PARAMETERS (8E)

T.B.D.

6.2.15 READ EXECUTION PARAMETERS (8F)

T.B.D.

6.3 VENDOR UNIQUE ERROR CODES

T.B.D.

SECTION 7

TIMING

7.0 GENERAL

This section covers the timing characteristics of the WD7000-ASC.

7.1 ELECTRICAL SPECIFICATIONS

7.1.1 D.C. CHARACTERISTICS

The Host interface requirements are shown below in Table 7-1. Input drive requirements are one standard 'LS' load. Detailed specifications can be found in the references listed in Section 1.

VCC = 5V $\pm$ 5% GND = 0V TA = 0 to 55^{o}C

TABLE 7-1. D.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
VIH	Input high voltage	2.0		V	
VIL	Input low voltage		0.8	V	
VOL1	SCSI Output Low Voltage		0.5	V	IOL = 48.0 mA
VOL2	Host Output Low Voltage		0.5	V	IOL = XX.0 mA
VOH1	SCSI Output High Voltage	2.4		V	IOH = -400 uA
VOH2	Host Output High Voltage			V	IOH = XXX uA

7.1.2 A.C. CHARACTERISTICS

The A.C. Characteristics for the SCSI and the Host interface timings are completely defined in the references in Section 1. Portions pertinent to the WD7000-ASC design are covered in this section.

The Host executes I/O reads from the WD7000-ASC ports or the BIOS, and then writes to the ports to execute a command or generates a control strobe. The FPDMA is used for data transfers between the WD7000-ASC and the Host system RAM memory.

Data transfers across the SCSI bus use the $\overline{REQ}$ /$\overline{ACK}$ handshake as defined in the SBIC data sheets.

7.1.2.1 HOST PROGRAMMED I/O OR BIOS ROM READ

For addressing the four ports decoded as XX0-XX3 (Hex), the LSB 10 bits of the 20-bit address bus are used. AEN should be low or de-asserted. The full 20-bit address bus is used to read the ROM regardless of AEN. The ROM address may optionally be gated with $\overline{MEMR}$, if so desired. The data bus, D7-D0, is qualified by the read strobes, $\overline{IOR}$ or $\overline{MEMR}$, but not both. Figure 7-1 illustrates the Host Programmed I/O or BIOS ROM Read Timing Diagram. Table 7-2 list the Host Programmed I/O or BIOS ROM Read Parameters.

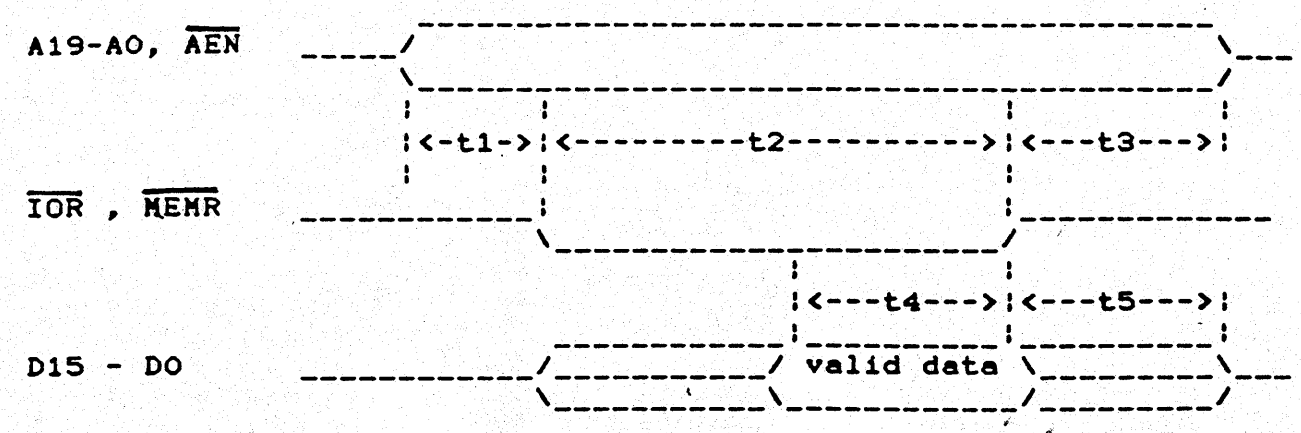


FIGURE 7-1. HOST PROGRAMMED I/O OR BIOS ROM READ TIMING DIAGRAM

TABLE 7-2. HOST PROGRAMMED I/O OR BIOS ROM READ PARAMETERS

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	NOTES
t1	Read Address Setup Time	x		nS	
t2	Read Active Time (ROM)	x		nS	
	(I/O)	xxx			
t3	Address Hold Time	x		nS	
t4	Data Valid Time	x		nS	
t5	Data Hold Time	0	x	nS	

7.1.2.2 HOST PROGRAMMED I/O WRITE

The Host Programmed I/O Write is similar to the Host Programmed I/O Read, except that the ROM cannot be obviously written to. Figure 7-2 illustrates the Host Programmed I/O Write Timing Diagram. Table 7-3 list the Host Programmed I/O Write Parameters.

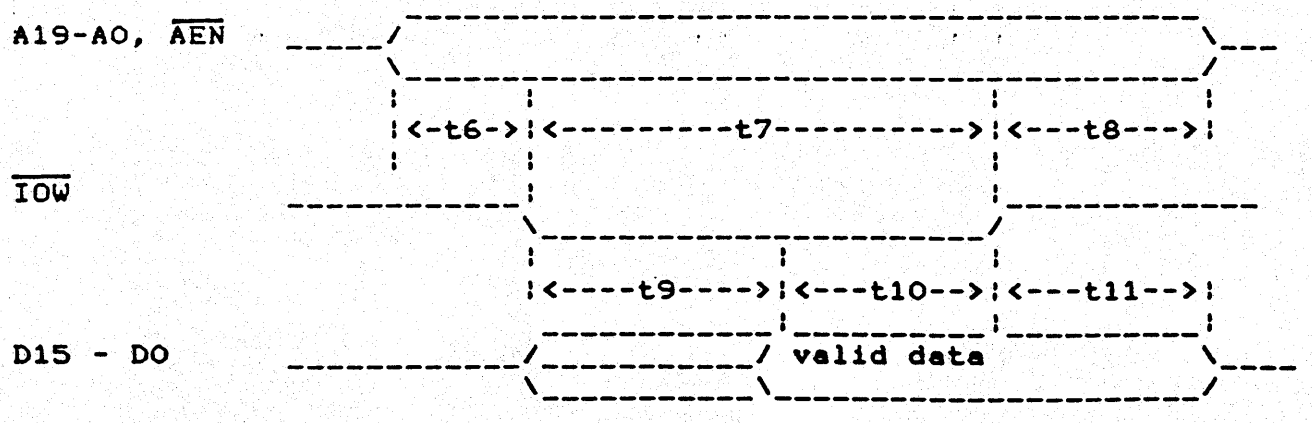


FIGURE 7-2. HOST PROGRAMMED I/O WRITE TIMING DIAGRAM

TABLE 7-3. HOST PROGRAMMED I/O WRITE PARAMETERS

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	NOTES
t6	Write Address Setup Time	x		nS	
t7	Write Active Time (I/O)	x		nS	
t8	Address Hold Time	x		nS	
t9	Data Setup Time	x		nS	
t10	Data Valid Time	x		nS	
t11	Data Hold Time	x		nS	

7.1.2.3 HOST DMA READ CYCLE

The WD7000-ASC memory cycle is indicated by the absence of any valid address lines. These are disabled by AEN being asserted high. Instead of the address lines, the DMA is gated with $\overline{\text{DACKX}}$. It is de-asserted when $\overline{\text{DACKX}}$ is asserted. These two lines complete the handshake between the DMA processor and the Host until all bytes of data have been transferred to the SCSI device buffer. Figure 7-3 illustrates the Host DMA Read Cycle Timing Diagram. Table 7-4 list the Host DMA Read Cycle Timing Parameters.

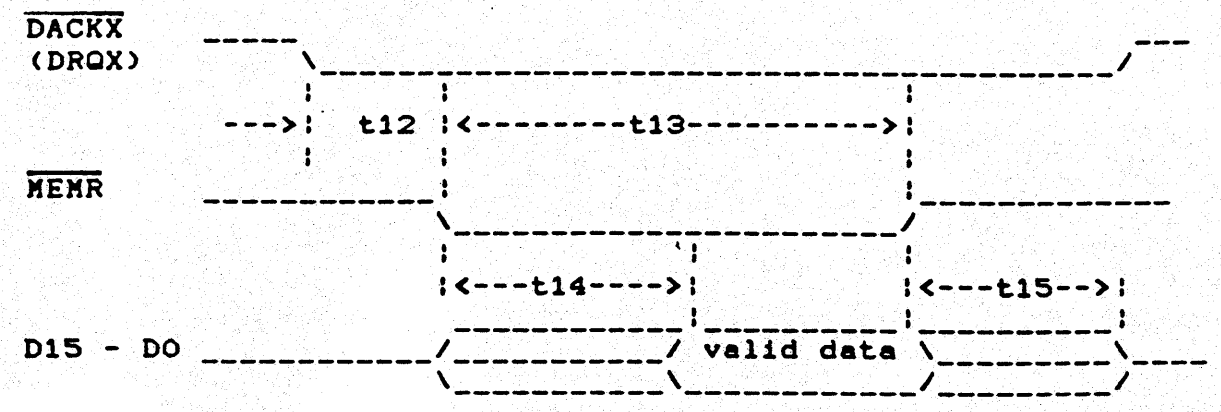


FIGURE 7-3. HOST DMA READ CYCLE TIMING DIAGRAM

TABLE 7-4. HOST DMA READ CYCLE TIMING PARAMETERS

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	NOTES
t12	$\overline{\text{DACKX}}$ Setup Time	x	x	nS	
t13	Read Active Time	x	x	nS	
t14	Data Valid Setup Time		x	nS	
t15	Data Hold Time	0	x	nS	

7.1.2.4 HOST DMA I/O WRITE CYCLE

The Host DMA I/O Write Cycle is similiar to the Host DMA Read Cycle, except that the SBIC buffer data is transferred to the Host system memory. Figure 7-4 illustrates the Host DMA I/O Write Cycle Timing Diagram. Table 7-5 list the Host DMA I/O Write Cycle Timing Parameters.

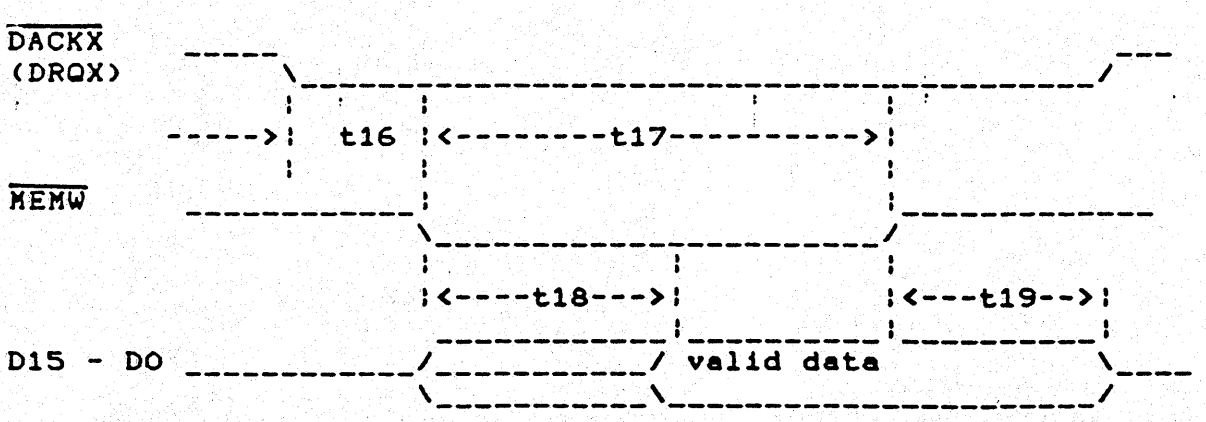


FIGURE 7-4. HOST DMA I/O WRITE CYCLE TIMING DIAGRAM

TABLE 7-5. HOST DMA I/O WRITE CYCLE TIMING PARAMETERS

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	NOTES
t16	$\overline{\text{DACKX}}$ Setup Time	x	x	nS	
t17	Read Active Time	x		nS	
t18	Data Valid Setup Time		x	nS	
t19	Data Hold Time	x		nS	