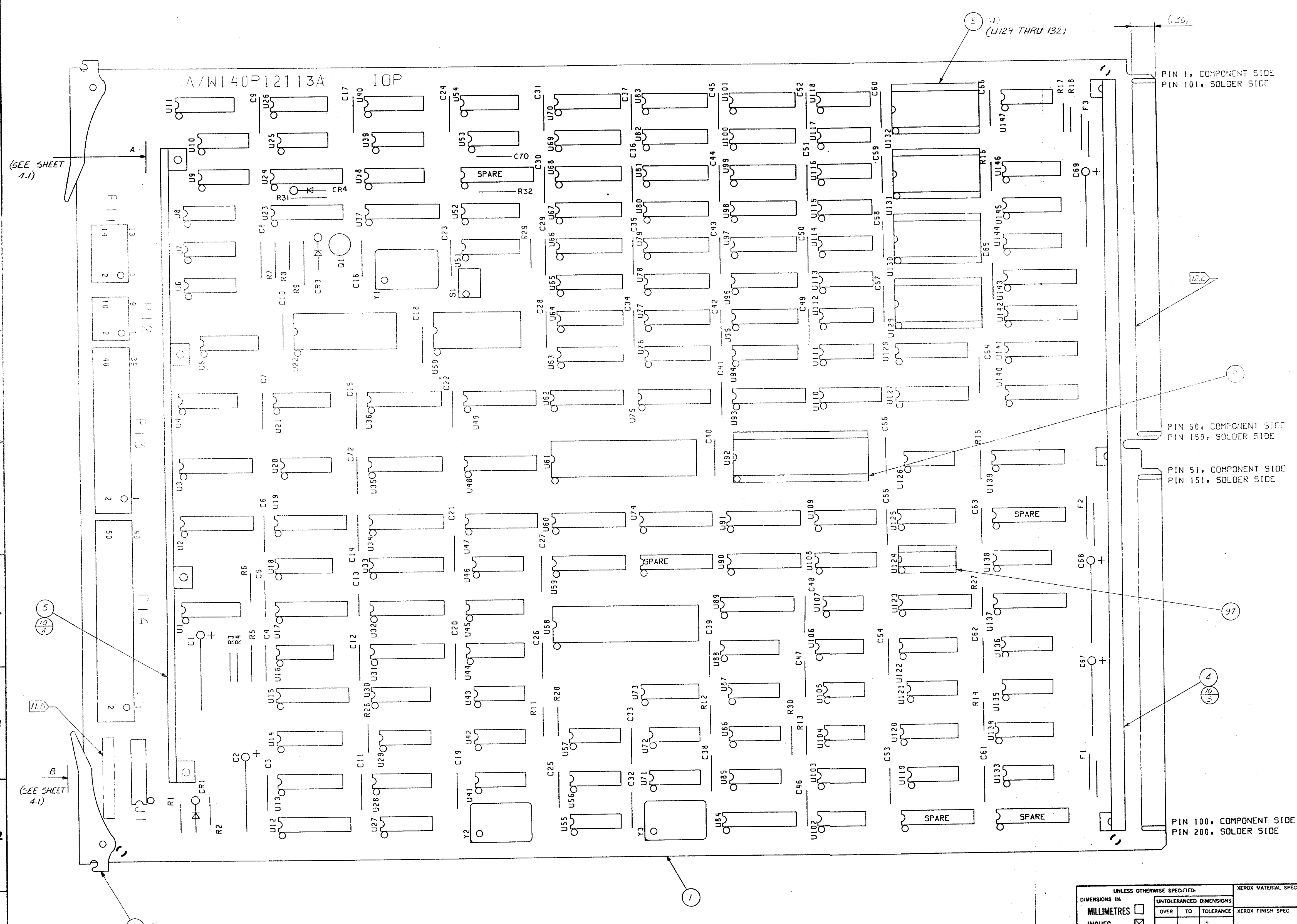
11.0 MARK PER 88P215, CLASS 1. LOCATE APPROXIMATELY WHERE SHOWN.

12.0 CONTACT FINGERS SHALL BE KEPT FREE OF SOLDER ON BOTH SIDES BETWEEN THE LINE OF DEMARCATION AND THE BOARD EDGE.



ITEM	PART NUMBER	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS IN: MILLIMETRES ☐ INCHES ☒
REFER TO 88P200 FOR DWG INTERPRETATION
THIRD ANGLE PROJECTION
MAXIMUM SURFACE TEXTURE √

UNTOLERANCED DIMENSIONS		
OVER	TO	TOLERANCE
		±
		±
		±
		±
		±
ANGLES		±

XEROX MATERIAL SPEC

XEROX FINISH SPEC

RELATED SPECIFICATIONS

APPROVAL SIGNATURES		DATE
DRAWN	[signature]	1 MAR 82
CHECKED	E. Santiago (CODE 3)	11 MAR 82
ENGRG	O. [signature]	30 MAR 82

REFERENCE CODES

XEROX

TITLE: PWB ASSEMBLY, IOP

DWG SIZE: A0 — DRAWING NUMBER: 140S2650X — SHEET 4.0 OF — REVISION: B — SEE SHEET 1 REV RECORD FOR LATEST DRAWING REV

SHEET 1.0
DWG NO. 140S2650X

XEROX

ASSEMBLY REVISION RECORD

REV FOR 140S2650— (SEE BELOW)

9	8	7	6	5	4	3	2	1	0	TYPE
									A	ISS
									B	D/C
								A		ISS

REVISION RECORD

DWG STATUS REV	DWG STATUS TYPE	CHG NO. CHG BY/DATE	CHK BY/DATE	CHK CODE	REV CHG NO.	MF CHK
A	ISS	[illegible]			559788	MF
B	D/C	E.S. Ramirez 9 FEB 84	E.S. Ramirez 9 FEB 84	3	559805	MF
C	D/C	MS 04JAN85	E Sanchez 5 JAN 85	3	559877	MF
D	D/C	D Llanes 11 NOV 85	E Sanchez 20 NOV 85	3	588998	MF

SHEET NO.	SIZE	SHEET REVISION						SHEET NO.	SIZE	SHEET REVISION						
2.0	A4	A		C	D											
2.1	A4	A			D											
3.0	A4	A	B		D											
3.1	A4	A			D											
3.2	A4	A			D											
3.3	A4	A	B		D											
4.0	A0	A	B													
4.1	A1	A														

XEROX MATERIAL SPEC	XEROX FINISH SPEC	RELATED SPECS
		88P200, 83P215, 88P220, 156P11828, 082P80232

PREPARED BY/DATE	CHECKED BY/DATE	APPROVED BY/DATE	REFERENCE CODES
D. DELGADILLO 25 FEB 82 11	E Sanchez 3 25 OCT 82	[illegible] 8 NOV 82	

TITLE	DWG SIZE	DWG NO.	SHEET	SEE REV RECORD ABOVE
PWB ASSEMBLY, IOP	A4	140S2650X	1.0 OF 9	

1.0 ASSEMBLY MUST MEET ALL THE REQUIREMENTS OF 88P220.

2.0 COMPONENT HEIGHT SHALL NOT EXCEED .50 INCH.

3.0 UNLESS OTHERWISE SPECIFIED:
CAPACITANCE VALUES ARE IN MICROFARADS.
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 0.25 W.
RESISTANCE TOLERANCES ARE ± 5 PERCENT.

4.0 THE PADS FOR THE POSITIVE TERMINALS OF CAPACITORS AND THE CATHODES OF DIODES ARE CIRCLED.

5.0 ON THE PWB, A " + " SYMBOL IS MARKED ADJACENT TO THE POSITIVE TERMINAL OF POLARIZED CAPACITORS. THE ARROWHEAD OF THE SYMBOL " ⊢ " BETWEEN PADS, POINTS TO THE CATHODE TERMINAL PAD FOR DIODES.

6.0 SEMICONDUCTORS ARE TO BE SCREENED ACCORDING TO THE REQUIREMENTS OF 156P11828. IN THE EVENT OF CONFLICT, THE COMPONENT SPECIFICATION TAKES PRECEDENCE.

7.0 THE GENERIC PART NAMES LISTED IN THE DESCRIPTION FIELD ARE FOR REFERENCE ONLY. ALL ITEMS MUST BE PURCHASED TO THE REQUIREMENTS OF THE XEROX COMPONENT SPECIFICATION.

8.0 HAYWIRES ARE ACCEPTABLE WITHIN THE LIMITS AND REQUIREMENTS OF 082P80232.

9.0 MAXIMUM PROTRUSION SOLDER SIDE IS .10 INCH.

10.0 ELECTROSTATIC SENSITIVE DEVICE, PROVIDE ADEQUATE PROTECTION FROM ELECTROSTATIC DISCHARGE PER 88P220, SECTION 17.0 (SEE SHEETS 3.1, 3.2 AND 3.3).

TITLE	DWG. SIZE	DWG. NO.	SHEET REV
PWB ASSEMBLY, IOP	A4	140S2650X	D
		SHEET 2.0 OF	

11.0 SEE SHEET 4.0.

12.0 SEE SHEET 4.0.

13.0 SEE SHEET 4.1.

14.0 TESTING TO BE PERFORMED PER THE APPROPRIATE TEST SPECIFICATION (SEE SHEET 3.2).

15.0 ALTERNATE PART (SEE SHEET 3.3).

XEROX

REFERENCE DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QUANTITY REQUIRED PER ASSEMBLY									
				0 REV	1 REV	2 REV	3 REV	4 REV	5 REV	6 REV	7 REV	8 REV	9 REV
				B	A								
	1	140P12114	PWB DETAIL, IOP	1	1								
	2	156P11952	SCHEMATIC, IOP	REF	REF								
	3	003P87082	EXTRACTOR	2	2								
	4	030P87014	STIFFENER, (FRONT)	1	1								
	5	030P83244	STIFFENER, (BACK)	1	1								
	6	091P87222	LABEL, IOP	1	1								
	7	091P87219	LABEL, PWB ASSY	1	1								
	8	713W20725	SOCKET, 24-PIN	4	4								
	9	713W20625	SOCKET, 40-PIN	1	1								
	10	320W13201	RIVET	7	7								
C1,2	11	702W08901	CAP., 10, 25 V	2	2								
C3 THRU 12, 14 THRU 66. 72	12	702W05218	CAP., 0.1, 50 V	64	64								
C13	13	702W02418	CAP., 0.001, 100 V	1	1								
C67,69	14	702W28005	CAP., 22, 35 V	2	2								
C68	15	702W17105	CAP., 68, 15 V	1	1								
CR1,3	16	707W00642	DIODE 1N4003	2	2								
F1,3	17	708W11302	FUSE, 7 AMP	2	2								
F2	18	708W11502	FUSE, 15 AMP	1	1								
J1	19	713W21830	CONN, 18 PIN	1	1								
P11	20	713W15120	CONN, 14 PIN	1	1								
P12	21	713W12220	CONN, 10 PIN	1	1								
P13	22	713W12720	CONN, 40 PIN	1	1								
P14	23	713W10820	CONN, 50 PIN	1	1								
Q1	24	707W01916	TRANSISTOR 2N2905A	1	1								
R1,26,28	25	703W34688	RES, 10 k	3	3								
R2	26	703W35088	RES, 15 k	1	1								
R3,4	27	703W31488	RES, 470	2	2								
R5	28	703W35888	RES, 33 k	1	1								
R6	29	703W29888	RES, 100	1	1								
R7,17,18	30	703W30688	RES, 220	3	3								
R8,11 THRU 16,27,29,30	31	703W32288	RES, 1 k	10	10								
R9	32	703W26687	RES, 4.7, 0.5 W	1	1								

TITLE	DWG. SIZE	DWG. NO.	SHEET REV
PWB ASSEMBLY, IOP	A4	140S2650X	D
		SHEET 3.0 OF	

XEROX

REFERENCE DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QUANTITY REQUIRED PER ASSEMBLY									
				0 REV	1 REV	2 REV	3 REV	4 REV	5 REV	6 REV	7 REV	8 REV	9 REV
S1	33	710W00002	DIPSWITCH, 2-POLE	1	1								
U1	34	703W01291	R-DIP, 150 x 8	1	1								
U2,17,37,140	35	733W01633	IC, OCT BFR 74S240	4	4								
U3,36,49,90, 128,142	36	733W01698	IC, D-FF 74LS374	6	6								
U4	37	703W30891	R-DIP, 160/260 x 14	1	1								
U5	38	733W00100	IC, DRVR 75114	1	1								
U6,55,87,133	39	733W01705	IC, OR 74LS32	4	4								
U7	40	733W01911	IC, DRVR 75188	1	1								
U8	41	733W00098	IC, RCVR 75189	1	1								
U9,57,107,135	42	733W01704	IC, AND 74LS08	4	4								
U10,25,39,53	43	733W01663	IC, CNTR 74LS393	4	4								
U11,26,40,54	44	733W01674	IC, REG 74LS165	4	4								
U12,47,89,141	45	733W01624	IC, D F-F 74LS273	4	4								
U13	46	537P02280	IC, PROM 93453	1	1								
U14	47	537P02279	IC, PROM 93453	1	1								
U15,137,143	48	733W01640	IC, D F-F 74S374	3	3								
U16	49	733W01916	IC, DATA SEL 74LS153	1	1								
U18	50	733W00378	IC, RCVR 75115	1	1								
U19,24,60,74, 139	51	733W01626	IC, OCT BFR 74LS244	5	5								
U20,41,43,56, 85,86,121,136	52	733W01675	IC, D F-F 74LS74	8	8								
U21	53	537P02283	IC, PROM 93427	1	1								
10.0 U22	54	733W01946	IC, USART I8251A	1	1								
U23,35,48,84, 108,123,127	55	733W01625	IC, OCT BFR 74LS240	7	7								
U27,147	56	733W01643	IC, NOR 74S02	2	2								
U28	57	733W01770	IC, CNTR 74LS163A	1	1								
U29	58	733W01771	IC, D F-F 74S74	1	1								
U30	59	733W01775	IC, MULTIV 74123	1	1								
U31,32,33,34	60	733W01909	IC, CNTR 74LS569	4	4								
U38,120	61	733W01745	IC, MUX 74LS157	2	2								
U42	62	733W00339	IC, HEX INV 7414	1	1								

TITLE	DWG. SIZE	DWG. NO.	SHEET REV
PWB ASSEMBLY, ICP	A4	140S2650X	D
		SHEET 3.1 OF	

XEROX

REFERENCE DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QUANTITY REQUIRED PER ASSEMBLY									
				0 REV	1 REV	2 REV	3 REV	4 REV	5 REV	6 REV	7 REV	8 REV	9 REV
U44,45,51,134, 144,145,146	63	733W01706	IC, DCDR 74LS138	7	7								
U46,104,105	64	733W01672	IC, HEX INV 74LS04	3	3								
10.0 U50	65	733W02225	IC, TIMER I8253-5	1	1								
U52	66	703W14991	R-DIP, 5.1 k x 15	1	1								
10.0 U58	67	733W02214	IC, FDC FD1797A	1	1								
U59,62,91,109	68	733W01740	IC, XCVR 74LS245	4	4								
10.0 U61	69	733W02232	IC, DMA CONT 18257-5	1	1								
10.0 U63 THRU 70, 76 THRU 83, 94 THRU 101, 111 THRU 118	70	733W01502	IC, RAM I2114	32	32								
U71,72,119	71	733W01671	IC, NAND 74LS00	3	3								
U73	72	703W15691	R-DIP, 10 k x 15	1	1								
U75,93,110	73	733W01708	IC, D-LATCH 74LS373	3	3								
U88,122	74	733W01642	IC, D F-F 74LS175	2	2								
10.0 U92	75	733W02221	IC, MICROPRO I8085A	1	1								
U102,103	76	733W01766	IC, MUX 74LS353	2	2								
U106	77	537P02281	IC, PROM 93427	1	1								
U124	78	537P02284	IC, PROM 93427	1	1								
U125	79	733W01662	IC, DCDR 74LS155	1	1								
U126	80	733W00318	IC, NAND 74S00	1	1								
10.0 U129	81	537P03029	IC, PROM I2716	1	NA								
10.0 U130	82	537P03030	IC, PROM I2716	1	NA								
10.0 U131	83	537P03700	IC, PROM I2716	1	NA								
10.0 U132	84	537P03032	IC, PROM I2716	1	1								
U138	85	537P02282	IC, PROM 93427	1	1								
Y1	86	733W01800	IC, 1.8432 MHz K1114A	1	1								
Y2	87	733W01802	IC, 16 MHz K1114A	1	1								
Y3	88	733W01801	IC, 6 MHz K1114A	1	1								
14.0	89	156P11270	TEST SPEC, IOP	REF	REF								
	90	156P12302	REWORK INSTRUCTIONS	REF	REF								
	91	117P10059	WIRE, 26 AWG	AR	AR								
C70	92	702W05918	CAP., 0.033, 100 V	1	1								

PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS

TITLE	DWG. SIZE	DWG. NO.	SHEET REV
PWB ASSEMBLY, IOP	A4	140S2650X	D
		SHEET 3.2 OF	

XEROX

REFERENCE DESIGNATION	ITEM	PART NUMBER	DESCRIPTION	QUANTITY REQUIRED PER ASSEMBLY									
				0 REV	1 REV	2 REV	3 REV	4 REV	5 REV	6 REV	7 REV	8 REV	9 REV
15.0 CR4	93	707W00273	DIODE 1N4148	1	1								
15.0 CR4	94	707W00347	DIODE 1N270	1	1								
R31	95	703W33988	RES, 5.1 k	1	1								
R32	96	703W31088	RES, 330	1	1								
	97	713W20525	SOCKET, 16 PIN	1	1								
10.0 U129	98	537E02180	IC, PROM I2716	NA	1								
10.0 U130	99	537E02190	IC, PROM I2716	NA	1								
10.0 U131	100	537E02200	IC, PROM I2716	NA	1								
	101	073K16160	PROM KIT, 80 MB	NA	REF								

PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS

TITLE	DWG. SIZE	DWG. NO.	SHEET REV
PWB ASSEMBLY, IOP	A4	140S2650X	D
		SHEET 3.3 OF	

57308-1 D7

PLEASE FILL IN COMPLETELY ABOVE DOUBLE LINES

XEROX ☐ CR ☒ CRLV | PROGRAM(S): 8010 | PAGE: 1 OF 3 | CR/CRLV #: 026753

PART NUMBER	REV	PART NAME	NEXT ASSY	S/S NO
1405-26500 1405-27878		PWBA-IOP		

ORIGINATOR-LOCATION-PHONE-DATE	RESPONSIBLE DESIGN ENGINEER	DEPT APPROVAL
LEN BRADY ES 39538 1/13/87	ROY OGUS	

END ITEM(S)	FIELD DISPOSITION ☐ REPAIR BY REPLACEMENT ☐ NONE ☐ USE TILL DEPLETION ☐ MANDATORY RETROFIT	REQUESTED CUT-IN: IMMEDIATE	REPLACEMENT RATE

☐ BASE NO CHANGE ☐ SUPERCESSION CHANGE ☐ REVISION CHANGE | EME AFFECTED ☐ YES ☒ NO | SAFETY AFFECTED ☐ YES ☒ NO | MFG. CUT-IN: IMMEDIATE

PROBLEM STATEMENT (INCLUDE CONSEQUENCES OF FAILURE TO TAKE ACTION)

EXISTING 16K E-PROMS ARE NO LONGER (733W01506)

BEING MANUFACTURED BY TEXAS INSTEUMENTS.

REQUEST ALLOW ESM TO USE 32K E-PROMS (733W01597) IN LIEU OF SPECIFIED DEVICES.
PATTERN NOS. = 537P03029, 3030, 3032, & 3700.
(SEE ATTACHED MEMO)

Logged 1/14/87

DATE TO S/S TEAM | PRIORITY | CLASS | TOOLING COST

DISPOSITION
☐ REJECT ——
☐ ACCEPT ——
☒ ACCEPT CRLV —
☐ PENDING ——

DATE
CR PKG NO
DATE 1/14/87
DESIGN DUE DATE

LIST AND ATTACH SUPPORTING DOCUMENTS

DELTA UMC

COB APPROVAL
ENG R Hanson for R Ogus 1/14/87
MFG Jon Brady 1/15/87
SERVICE MS Jones 1-14-87
PROGRAM

CUSTOMER CONCURRENCE REQUIRED

EXPLANATION OF DISPOSITION

Laurel Message

From: DRODGERS.ES Date: Thu, 8 Jan 87 20:00 PST

Subject: 32K Masters

To: R. Dances M2-03<ESMail>

XEROX

Bob,
Relative to the note below, I have a set of master EPROM's that you may have if you want them for the four patterns.

DR.

Date: Fri, 19 Dec 86 13:19 PST
From: DRODGERS.ES
Subject: Substitute for 16K EPROM on 8010
To: Len Brady ESCG-237<ESMail>
cc: S. McMullen M4-06/ A. Ray A2-18<ESMail>, AKanadjian, DRodgers

This is a response to your request to find a solution to the lack of suppliers on the 733W01506 2KX8 EPROM that is used on the IOP board of 8010. We recommend that you replace this part with the 4KX8 EPROM 733w01597. We have reviewed the board design and the device specifications and found that there is no difference in the device pins for the two devices as used on the IOP except as follows:

Pin#/ -1506 /-1597 / IOP board function
18/PDPGM/ CEbar / BankSelectbar
20/ CEbar /OEbarVPP/MemReadbar
21/ VPP / A11 / VCCtie

Pin 18 PDPGM or CEbar act in an identical way to select or powerdown the part.
Pin 20 CEbar and OEbarVPP act the same to turn on/off the outputs of the part.
Pin 21 The VCCtie for the -1597 merely causes only one half of the 32K part to be accessed if it is used on the IOP board.

We programmed two sets of four EPROMS using the -1597 32K device by putting the same 16K pattern in each half (A11=0 and A11=1) of the device. One set used TI parts and one used Fujitsu parts; the two qualified sources for the 32K. The devices were used to stuff two IOP's which were then tested on the GRboard tester and 8010 systems in M1 and M2; no failures occurred.

There should be no problem using the 32K device on the board as long as it is programmed correctly. Change Requests should be written against the four 537 pattern drawings to change the part no. from 733w01506 to 733w01597 and the test spec. no. from 156P16305 to 156P12575 and to change the data pattern as follows:

The first two pages of the data pattern should remain as is and two more pages should be added that are identical to the first except the four hex

addresses under the address column start at 0800 and count up to 0FE0 as they would for the last 16K bits of a 32K device.

The pattern #'s are: 537P03029, 537P03030, 537P03032, 537P03700

Len, sorry for the delay in getting this to you, we had many high priority tasks recently.

DR.

---

cc: [redacted]
DRodgers

XEROX

REVISION RECORD

DWG STATUS		CHG. NO.		REV		
REV	TYPE	CHG BY/DATE	CHK BY/DATE	CHK CODE	CHG NO.	MF CHK
A	ISS	J. Adams 9 MAR 83			559788	MF
B	D/C	E.J. Cariaga 26 JUL 83	E.J. Cariaga 26 JUL 83	3	559794	MF

SHEET NO.	SIZE	SHEET REVISION						SHEET NO.	SIZE	SHEET REVISION					
0.2	A4							10	A4	A	B				
0.3	A4	A	B					11	A4	A	B				
0.4	A4	A	B					12	A4	A	B				
0.5	A4	A	B					13	A4	A	B				
0.6	A4	A	B					14	A4	A	B				
0.7	A4	A	B					15	A4	A	B				
01	A4	A	B					16	A4	A	B				
02	A4	A	B					17	A4	A	B				
03	A4	A	B					18	A4	A	B				
04	A4	A	B					19	A4	A	B				
05	A4	A	B					20	A4	A	B				
06	A4	A	B					21	A4	A	B				
07	A4	A	B					22	A4	A	B				
08	A4	A	B					23	A4	A	B				
09	A4	A	B					24	A4	A	B				

XEROX MATERIAL SPEC	XEROX FINISH SPEC	RELATED SPECS

PREPARED BY/DATE	CHECKED BY/DATE	APPROVED BY/DATE	REFERENCE CODES
D. Flores 27 FEB 82	E. Santiago 3 5 MAR 82	D. Rice 30 MAR 82	

TITLE	DWG SIZE	DWG NO.	SEE REV RECORD ABOVE
SCHEMATIC, IOP	A4	156P11952	
		SHEET 0.1 OF 66	

XEROX

SHEET NO.	SIZE	SHEET REVISION						SHEET NO.	SIZE	SHEET REVISION					
25	A4	A	B					58	A4	A	B				
26	A4	A	B					59	A4	A	B				
27	A4	A	B												
28	A4	A	B												
29	A4	A	B												
30	A4	A	B												
31	A4	A	B												
32	A4	A	B												
33	A4	A	B												
34	A4	A	B												
35	A4	A	B												
36	A4	A	B												
37	A4	A	B												
38	A4	A	B												
39	A4	A	B												
40	A4	A	B												
41	A4	A	B												
42	A4	A	B												
43	A4	A	B												
44	A4	A	B												
45	A4	A	B												
46	A4	A	B												
47	A4	A	B												
48	A4	A	B												
49	A4	A	B												
50	A4	A	B												
51	A4	A	B												
52	A4	A	B												
53	A4	A	B												
54	A4	A	B												
55	A4	A	B												
56	A4	A	B												
57	A4	A	B												

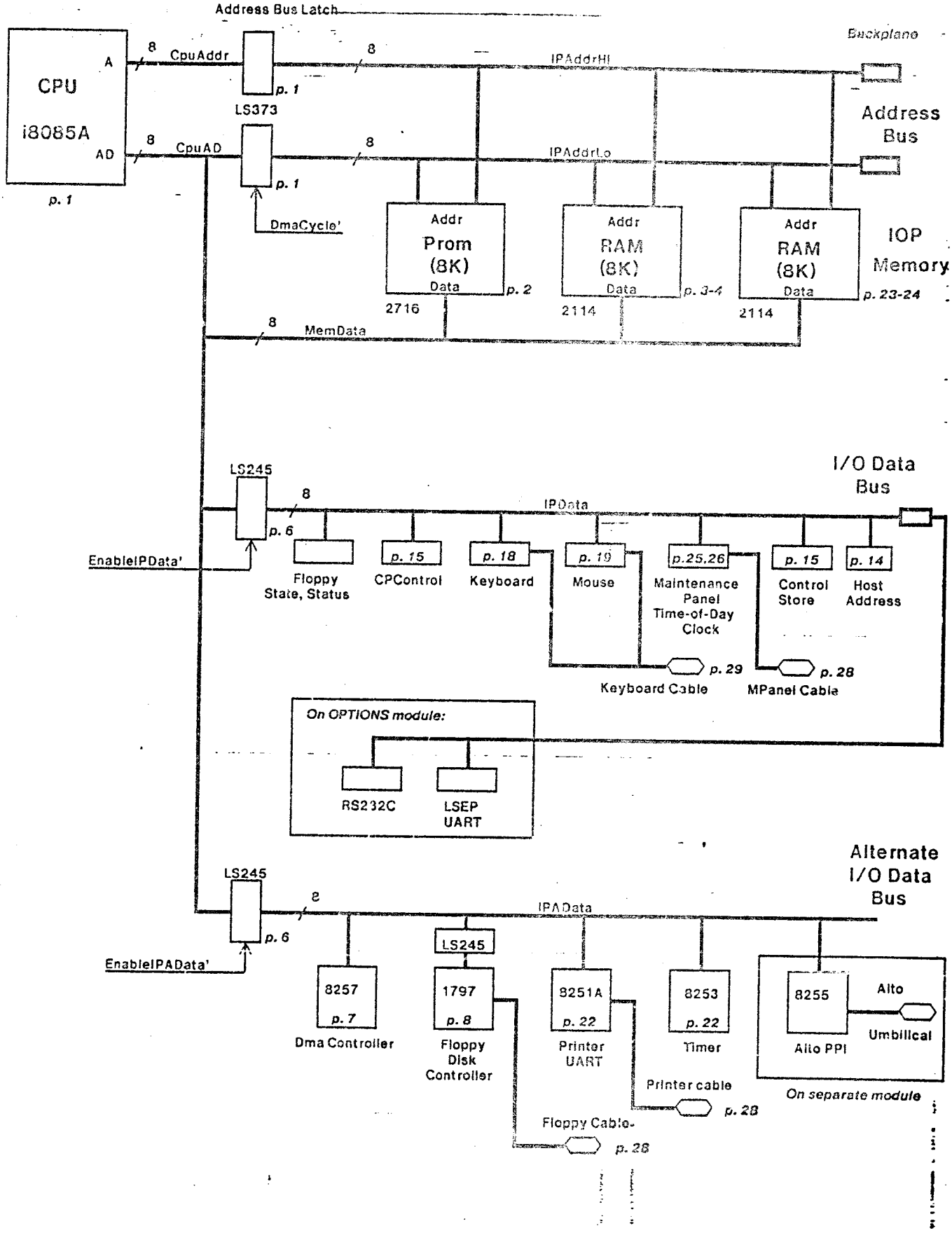
PROPRIETARY NOTE ON SHEET 1 APPLIES TO ALL SHEETS

TITLE	DWG. SIZE	DWG. NO.	SHEET REV.
SCHEMATIC, IOP	A4	156P11952	(Record Above)
		SHEET 0.2 OF	

SHEET	
0.4	BLOCK DIAGRAM: I/O PROCESSOR DATA PATHS
0.5	BLOCK DIAGRAM: I/O PROCESSOR CONTROL ORGANIZATION
0.6	BLOCK DIAGRAM: FLOPPY CONTROLLER
0.7	BLOCK DIAGRAM: CP - IOP PORT
1	CPU
2	PROM, MEMORY CONTROL
3	4K RAM MEMORY BANKS 0 - 3
4	4K RAM MEMORY BANKS 4 - 7
5	I/O CONTROL, MEMORY CONTROL
6	I/O DATA BUS CONTROL
7	DMA CONTROLLER
8	FLOPPY DISK CONTROLLER
9	FLOPPY DISK CONTROLLER WRITE COMPARE
10	FLOPPY DISK CONTROLLER MISCELLANEOUS
11	FLOPPY DISK RECEIVERS/DRIVERS
12	FLOPPY DISK CONTROLLER DATA SEPARATOR
13	DMA TEST REGISTER
14	INTERRUPT REQUEST REGISTER
15	CP CONTROL, CONTROL STORE
16	CP - IOP PORT - 1
17	CP - IOP PORT - 2
18	KEYBOARD INTERFACE
19	MOUSE INTERFACE
20	TIME-OF-DAY/MAINTENANCE PANEL INTERFACE
21	MISCELLANEOUS CPU CONTROL
22	PRINTER INTERFACE
23	4K RAM MEMORY BANKS 8 - 11
24	4K RAM MEMORY BANKS 12 - 15
25	TIME-OF-DAY CLOCK - 1
26	TIME-OF-DAY CLOCK - 2
27	DISCRETES, I/O CONNECTORS - 1
28	I/O CONNECTORS - 2
29	FUSES, POWER SUPPLY, CONNECTORS
30	BOOT AND RESET CIRCUITRY
31	FILTER CAPACITORS
32	SPARE COMPONENTS
33	TEST POINT LISTING, CONNECTOR LISTING, SIGNAL LISTING

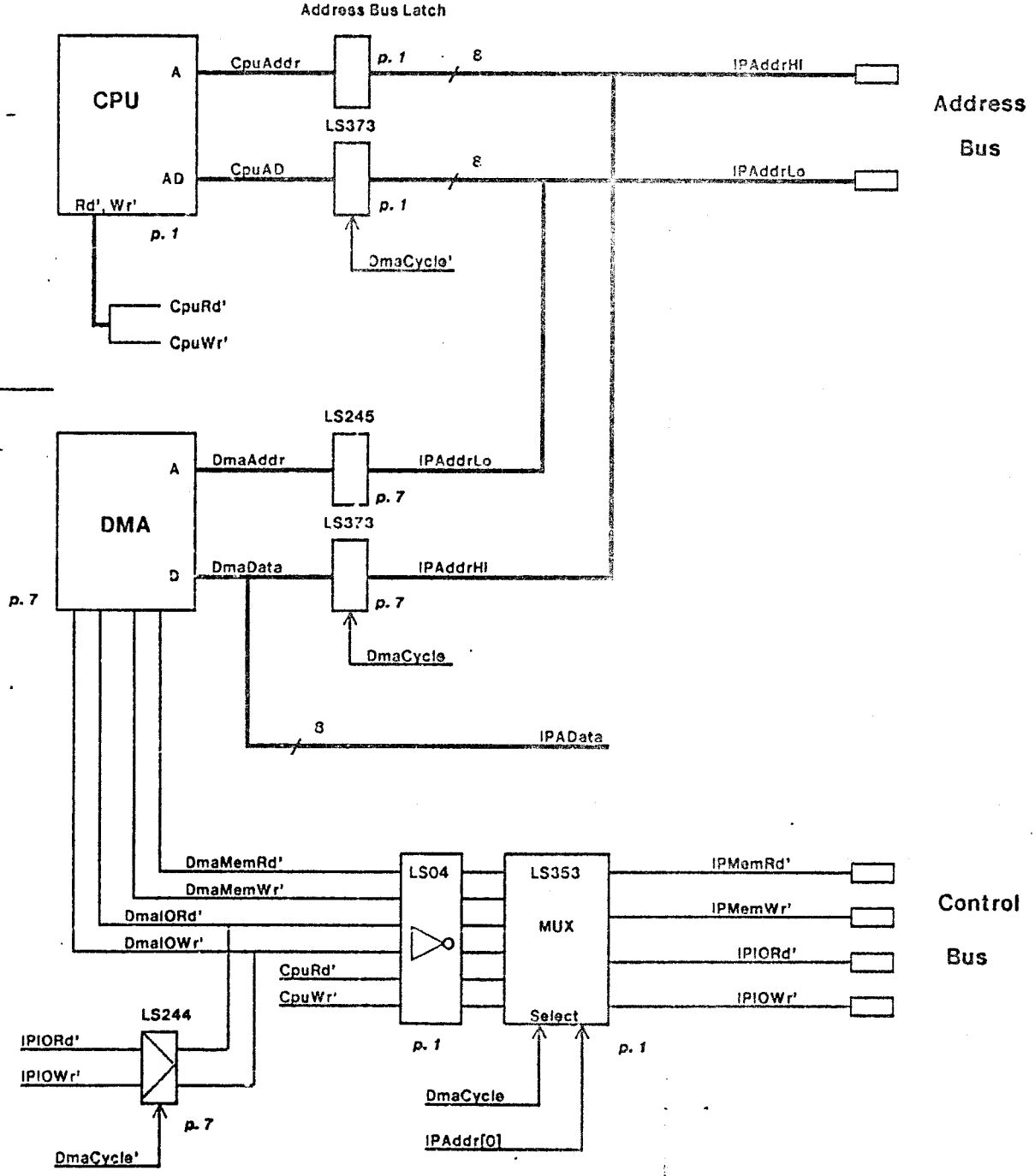
Note: The issued schematic drawing is made from [Rain]<SDMod>IOP3.dmASIL-C

TABLE OF CONTENTS



BLOCK DIAGRAM: I/O PROCESSOR DATA PATHS

ROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP Reference	A4	SHEET 0.4 OF	B

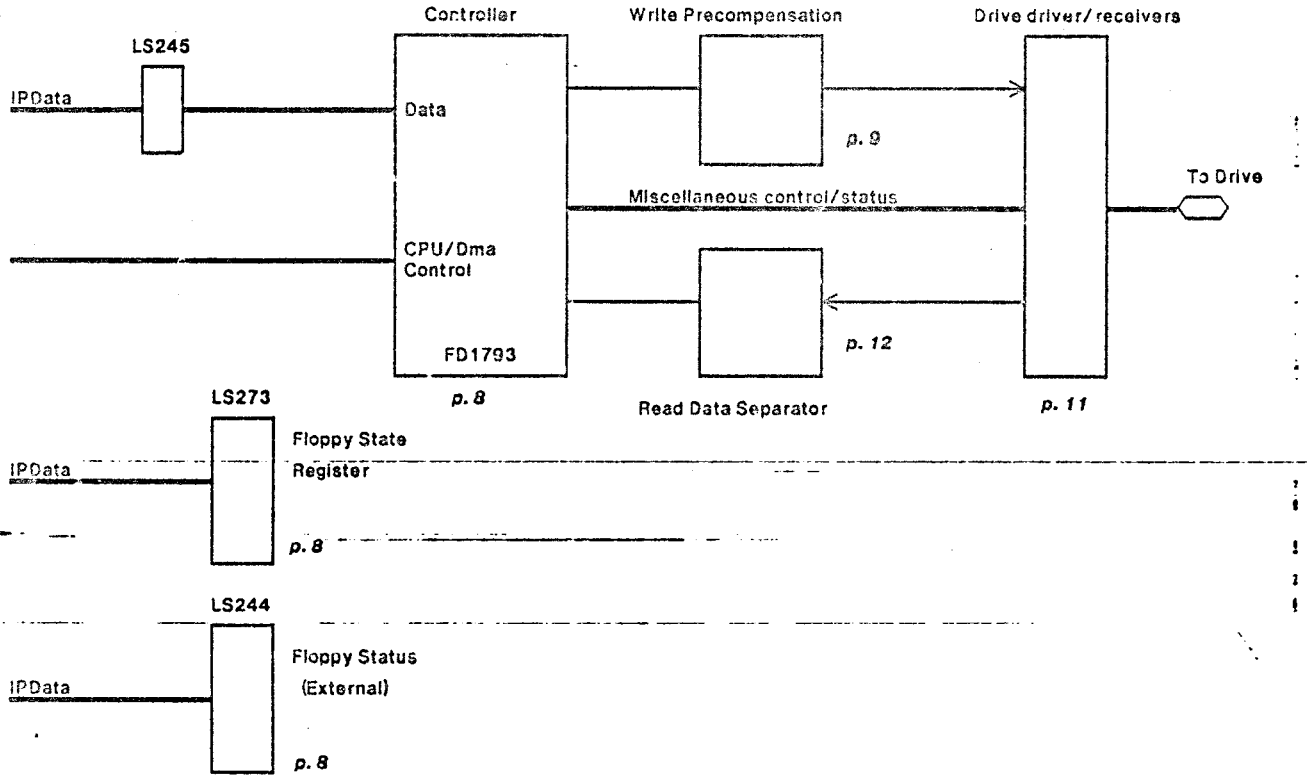


BLOCK DIAGRAM: I/O PROCESSOR CONTROL ORGANIZATION

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP *Reference*	A4	SHEET 0.5 OF	B

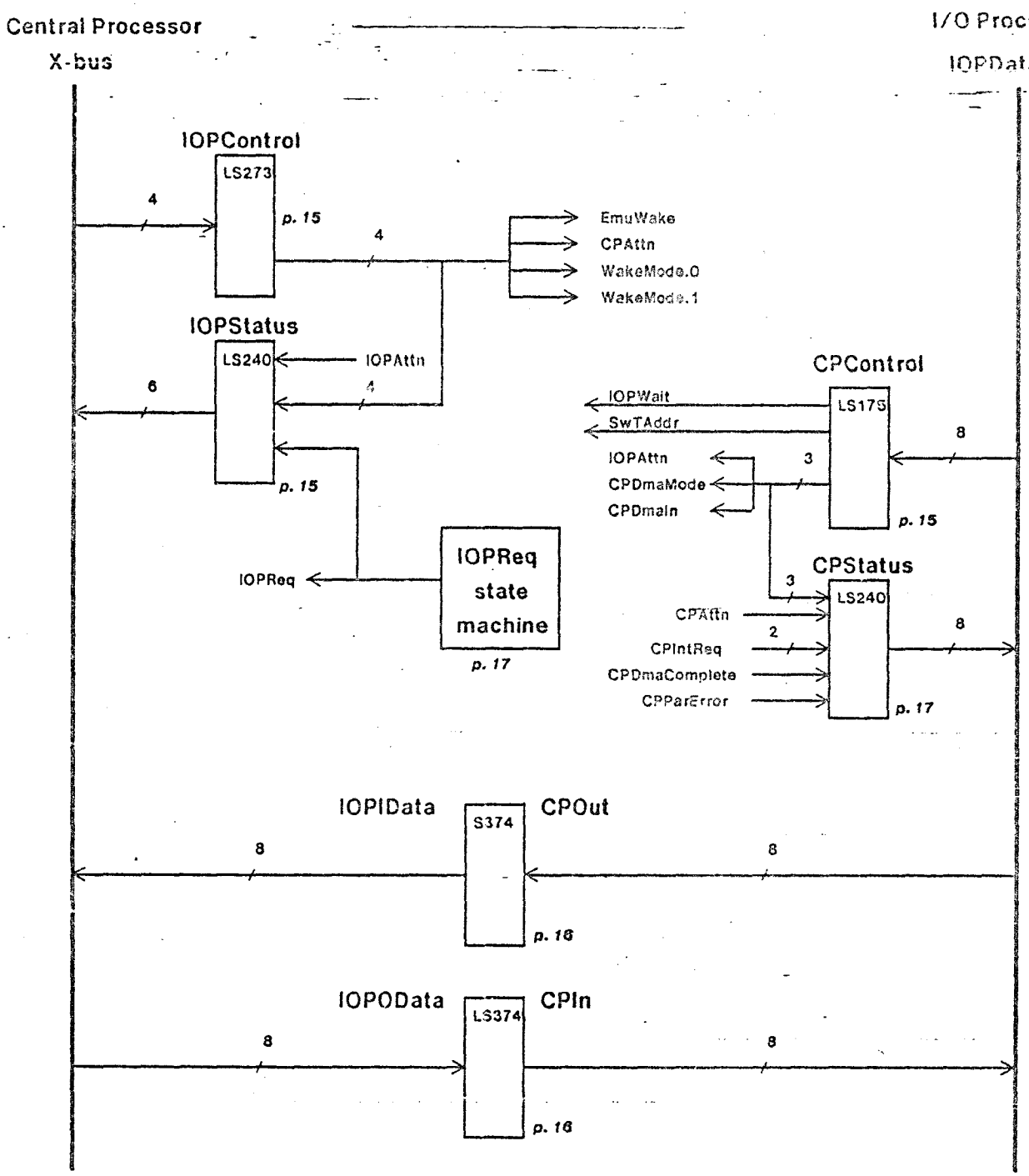
I/O Processor Floppy Disk Controller

Block Diagram



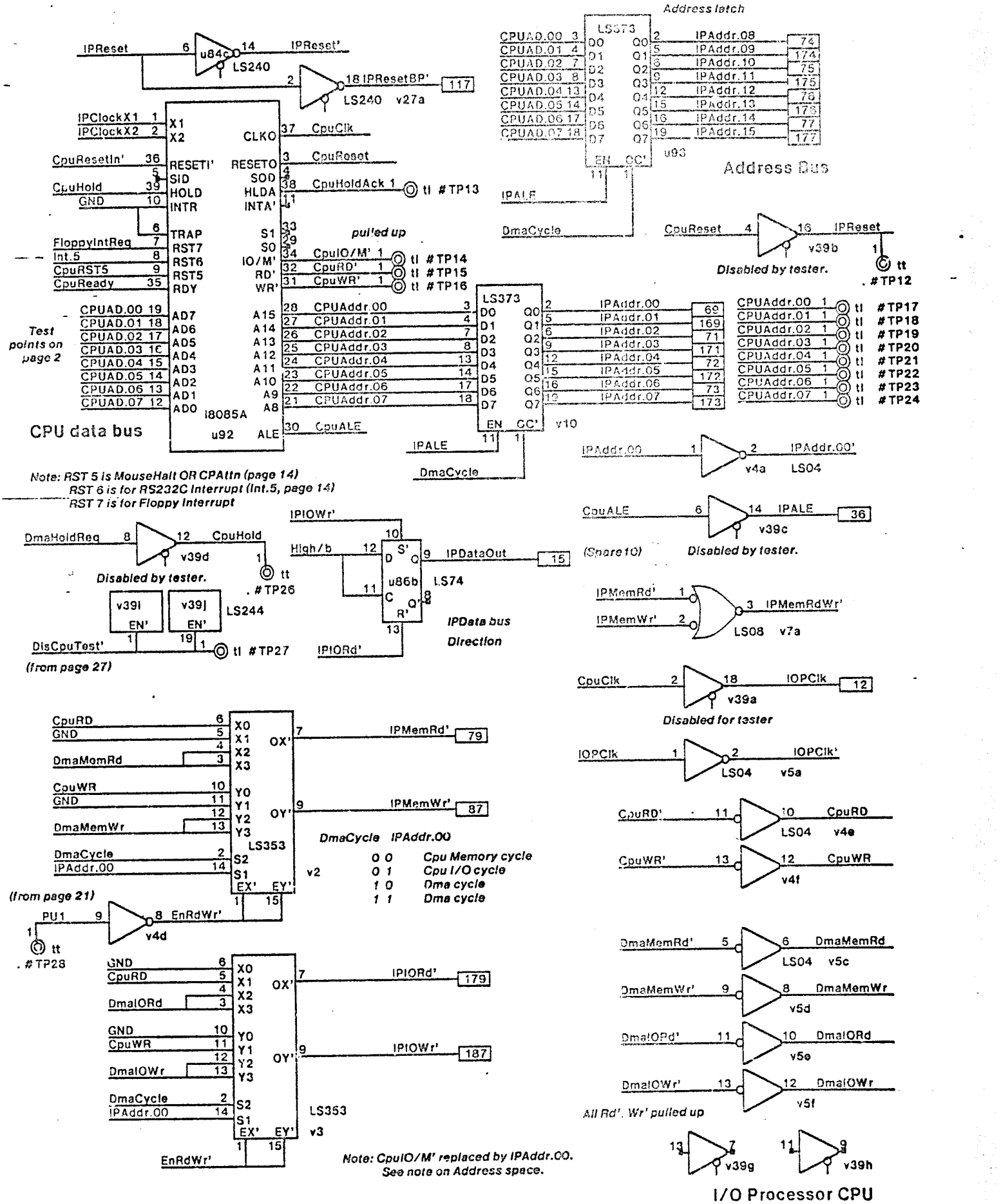
BLOCK DIAGRAM: FLOPPY CONTROLLER

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP *Reference*	A4	SHEET 0.6 OF	B



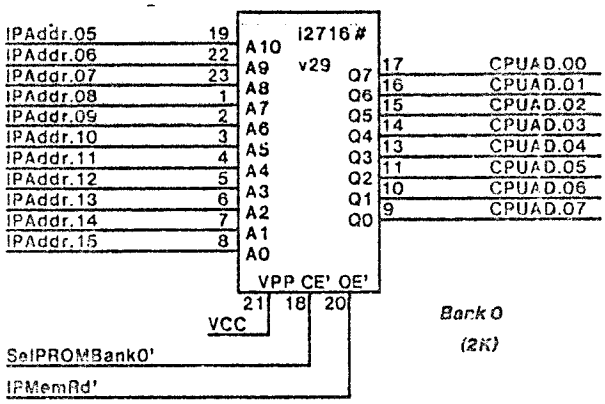
BLOCK DIAGRAM: CP - IOP PORT

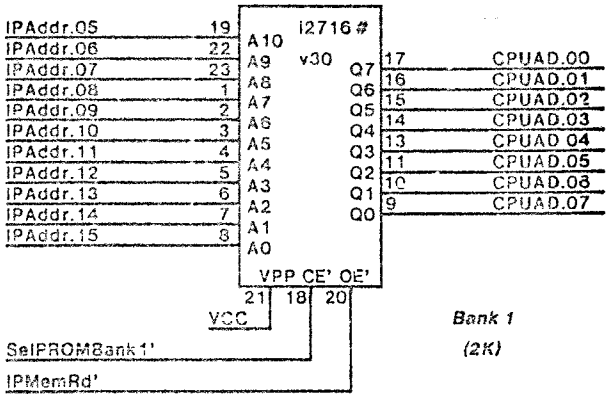
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP *Reference*		SHEET 0.7 OF	

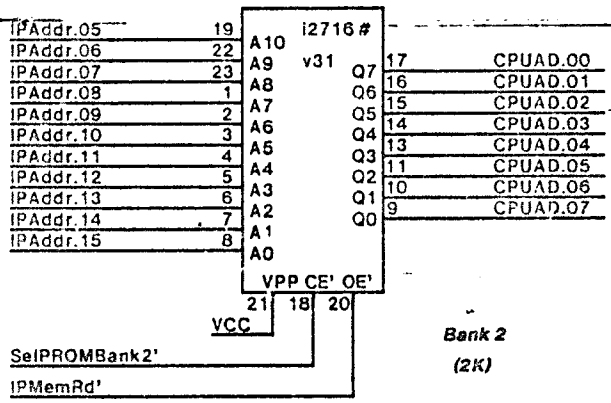


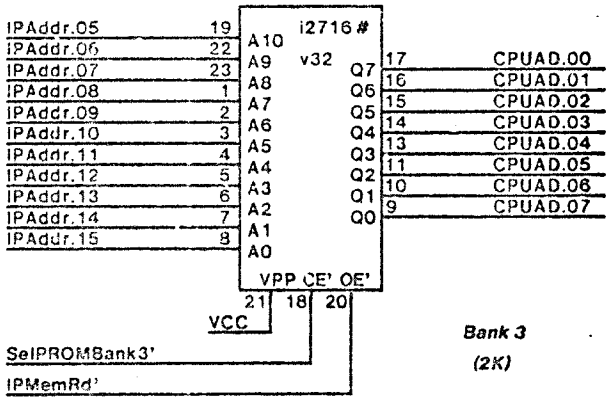
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 01 OF	B

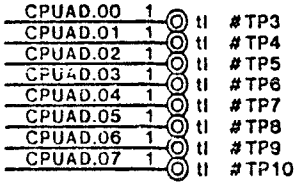
Prom







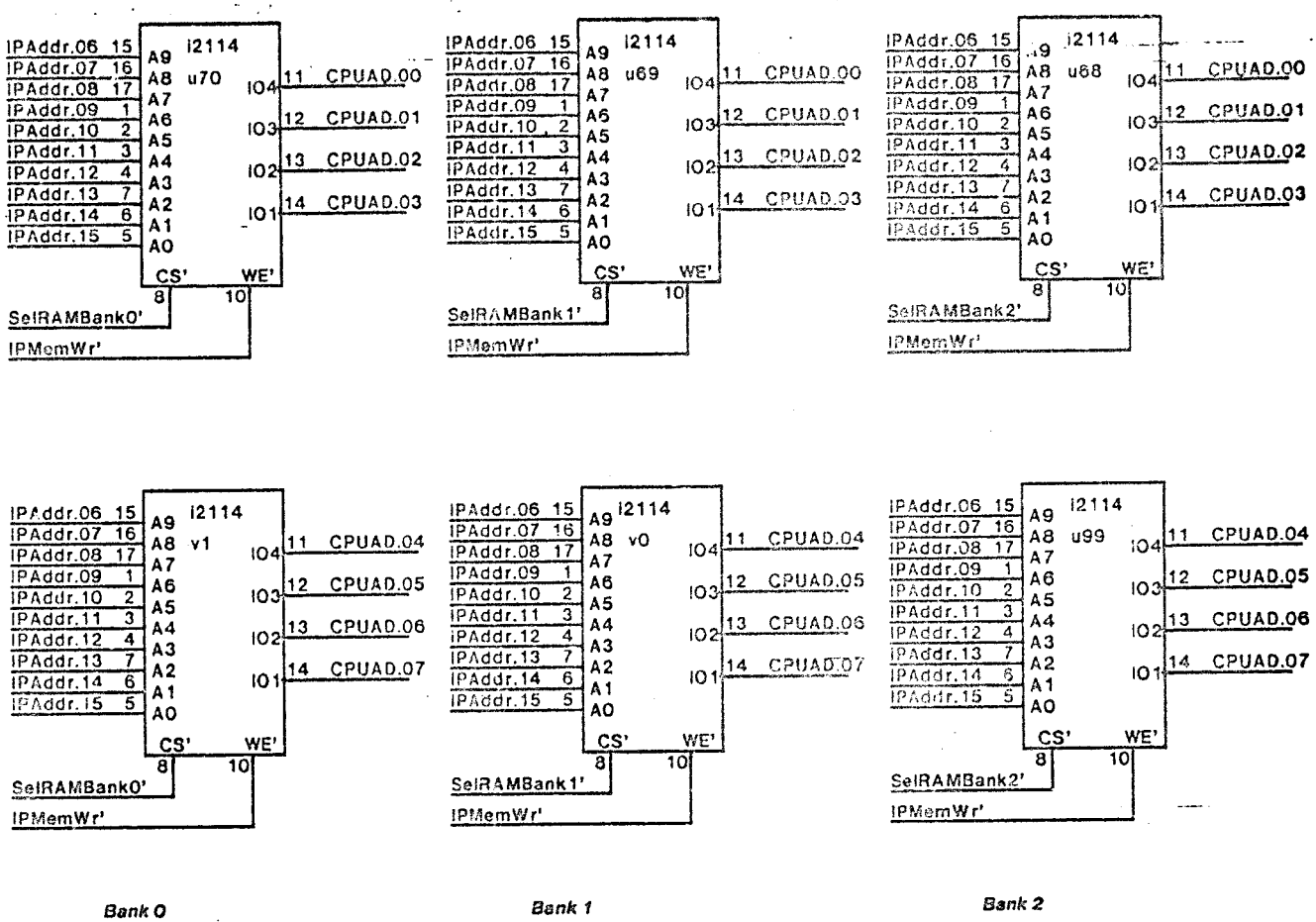




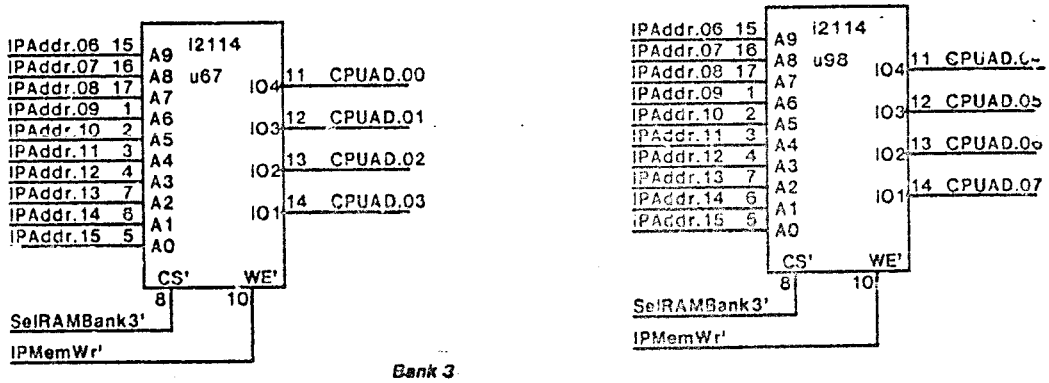
I/O Processor PROM

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 02 OF	B

RAM - Banks 0 - 3



Bank 0 *Bank 1* *Bank 2*

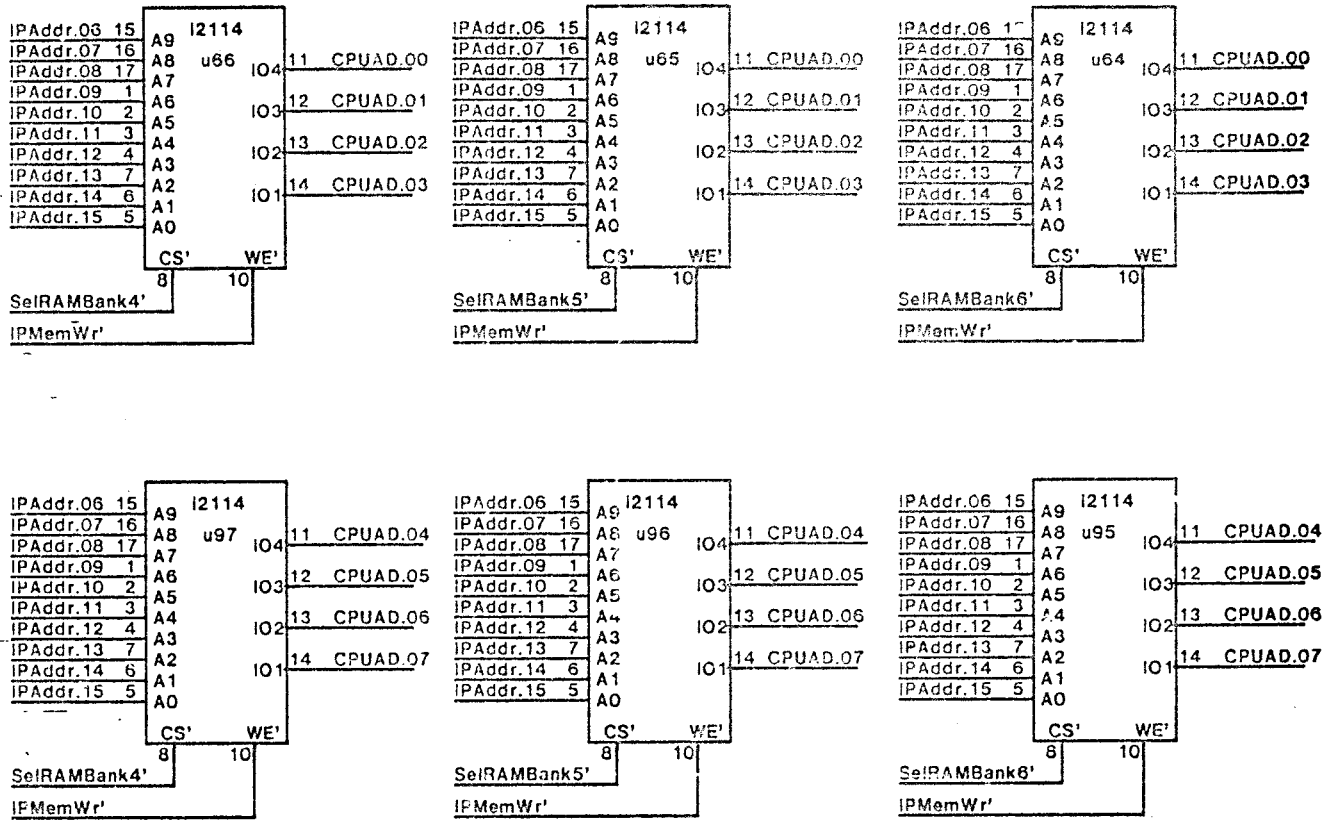


Bank 3

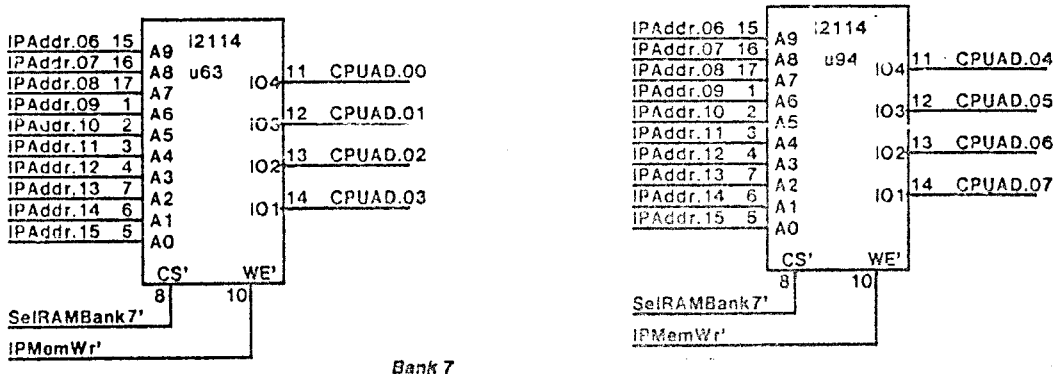
I/O Processor 4K RAM Memory-Banks 0 - 3

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 03 OF	B

RAM - Banks 4 - 7



Bank 4 *Bank 5* *Bank 6*



Bank 7

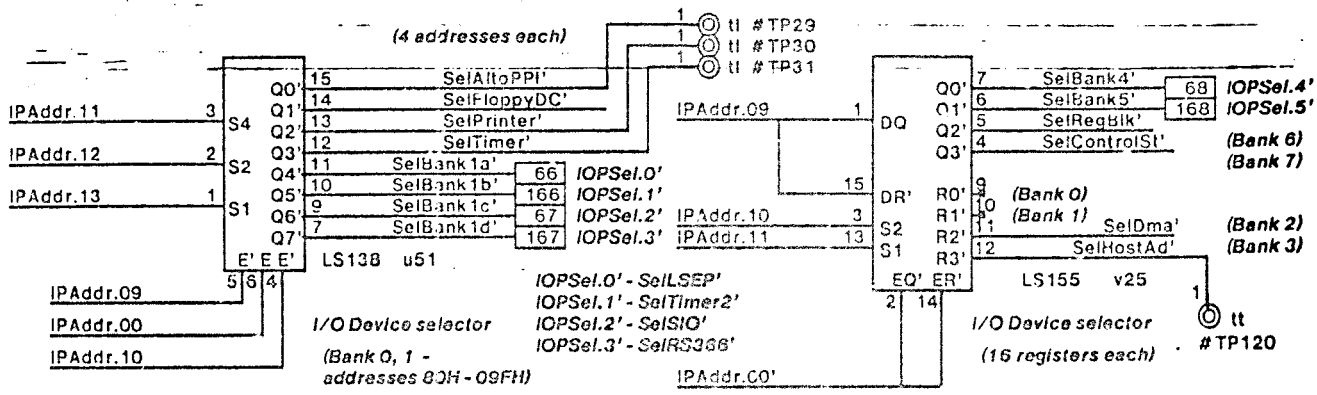
Note: RAM Banks 8 - 15 on pages 23 and 24.

I/O Processor 4K RAM Memory-Banks 4-7

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 04 OF	

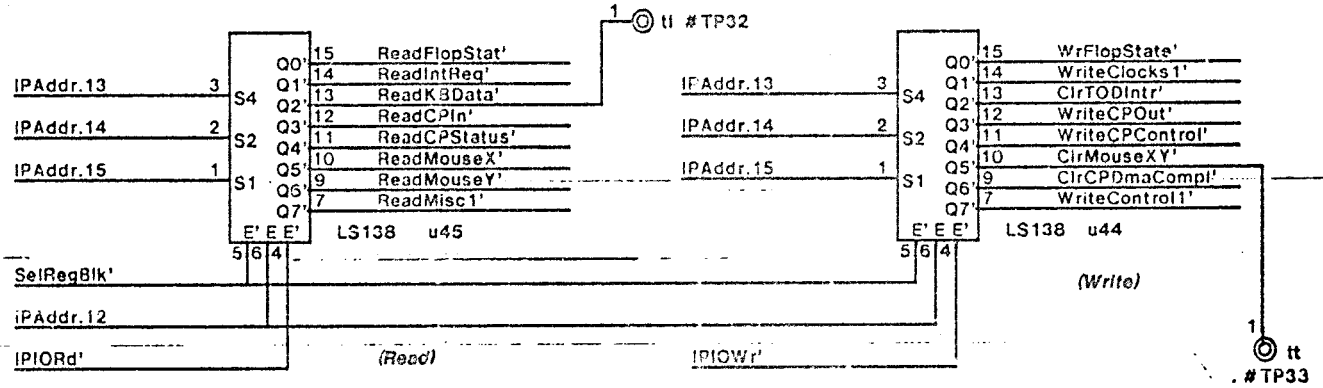
I/O Control

(Depends on Addr[0] = Addr[8], etc. for I/O. IPAddr[0] = 1 for I/O addresses.)



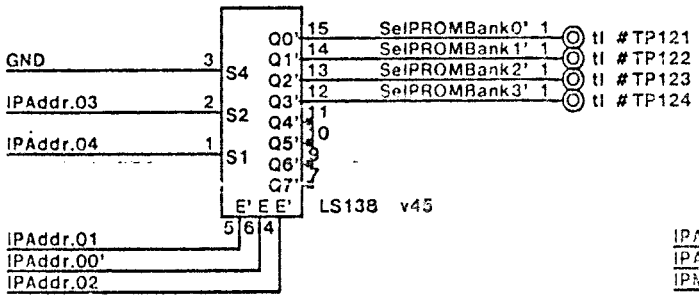
Note: Bank 4 reserved for Options card.

Note: Bank 5 is used by IPData bus test register.

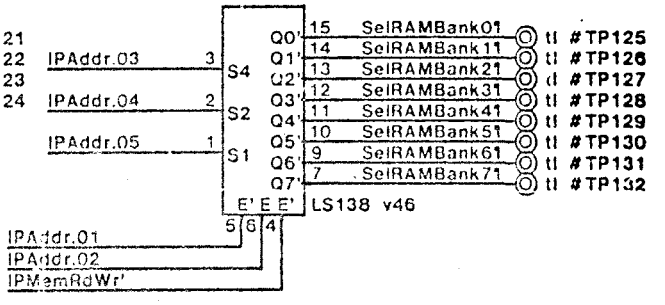


Single Register Block
(Bank 6, registers 8-15, addresses 0E3H - 0EFH)

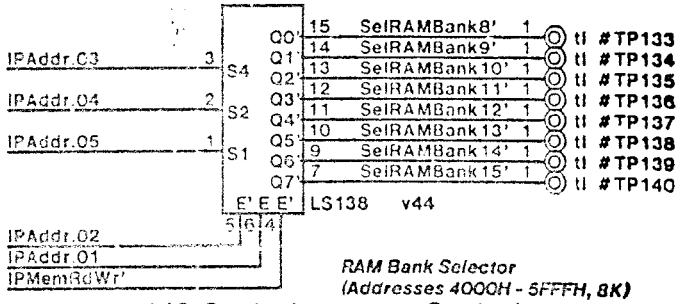
Memory Control



PROM Bank Selector
(Addresses Bank 0: 0 - 7FFH,
Bank 1: 800H - 0FFFH,
Bank 2: 1000H - 17FFH,
Bank 3: 1800H - 1FFFH)



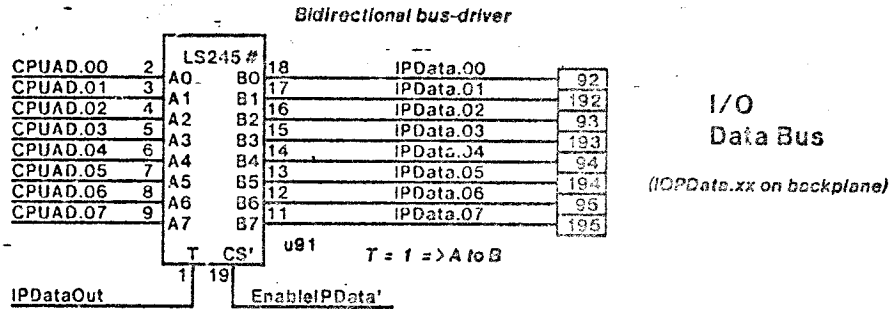
RAM Bank Selector
(Addresses 2000H - 3FFFH, 8K)

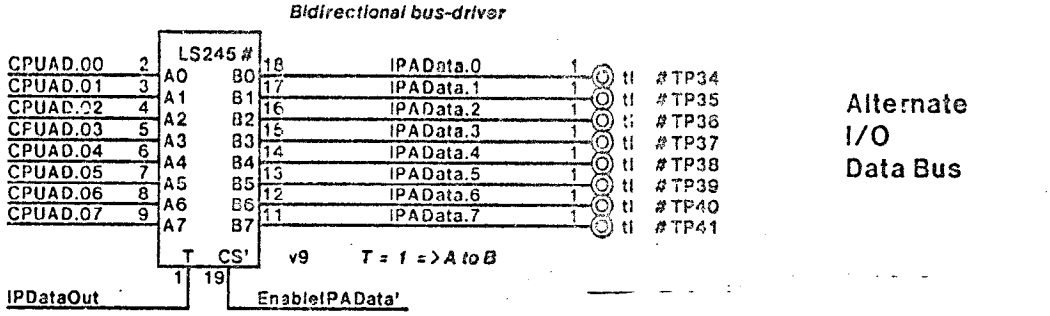


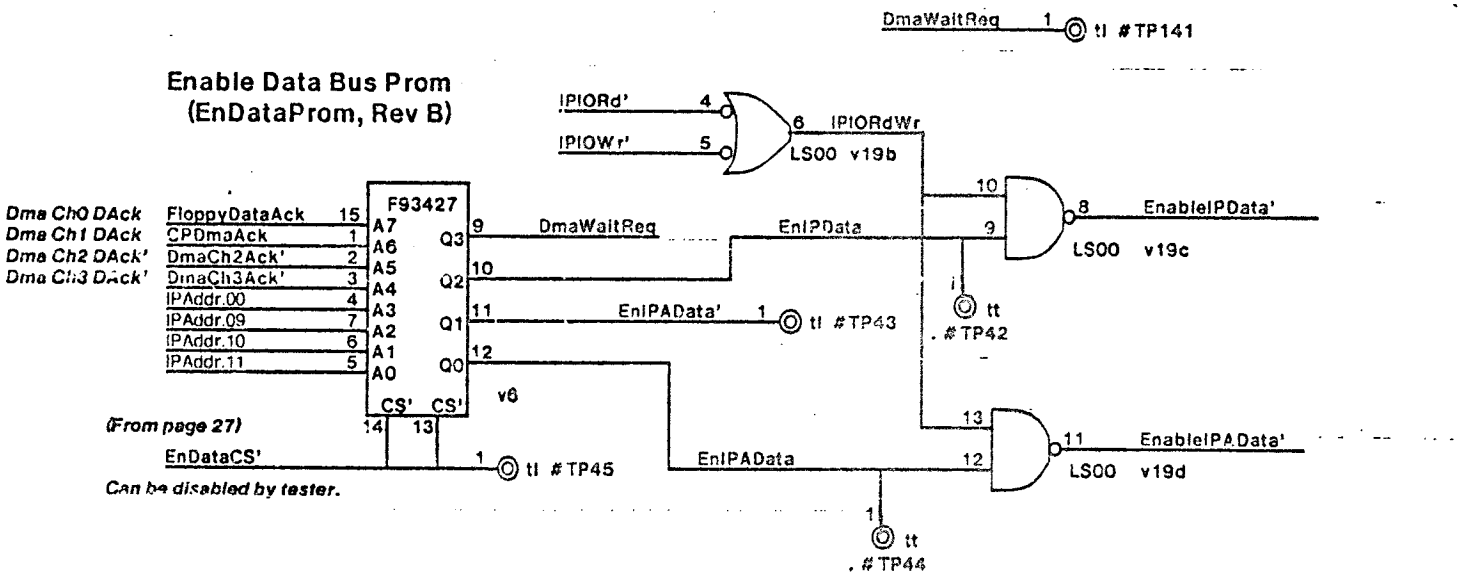
RAM Bank Selector
(Addresses 4000H - 5FFFH, 8K)

I/O Processor I/O Control, memory Control

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 05 OF	



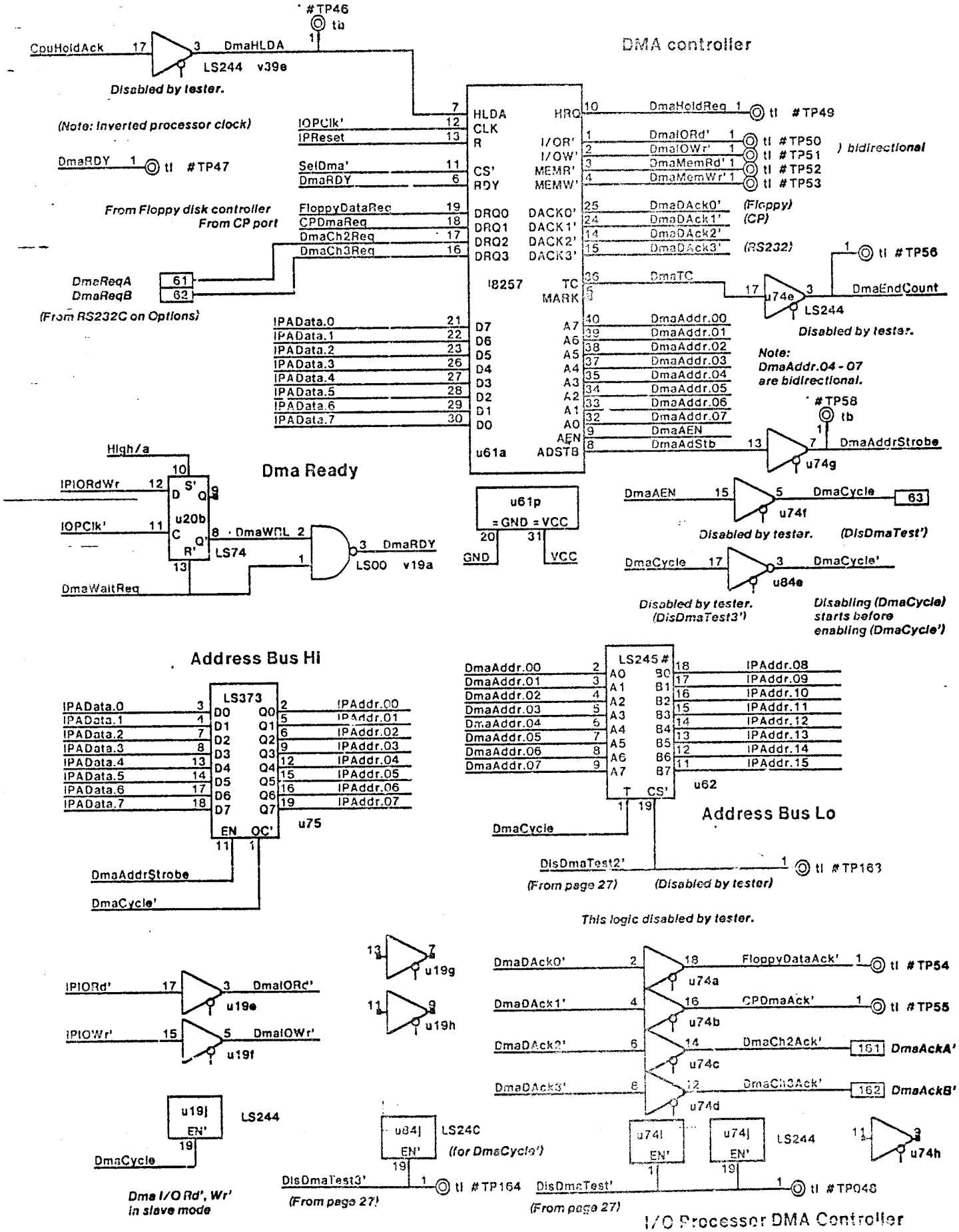




Note: Do not use DMA memory addresses in the I/O Address space.

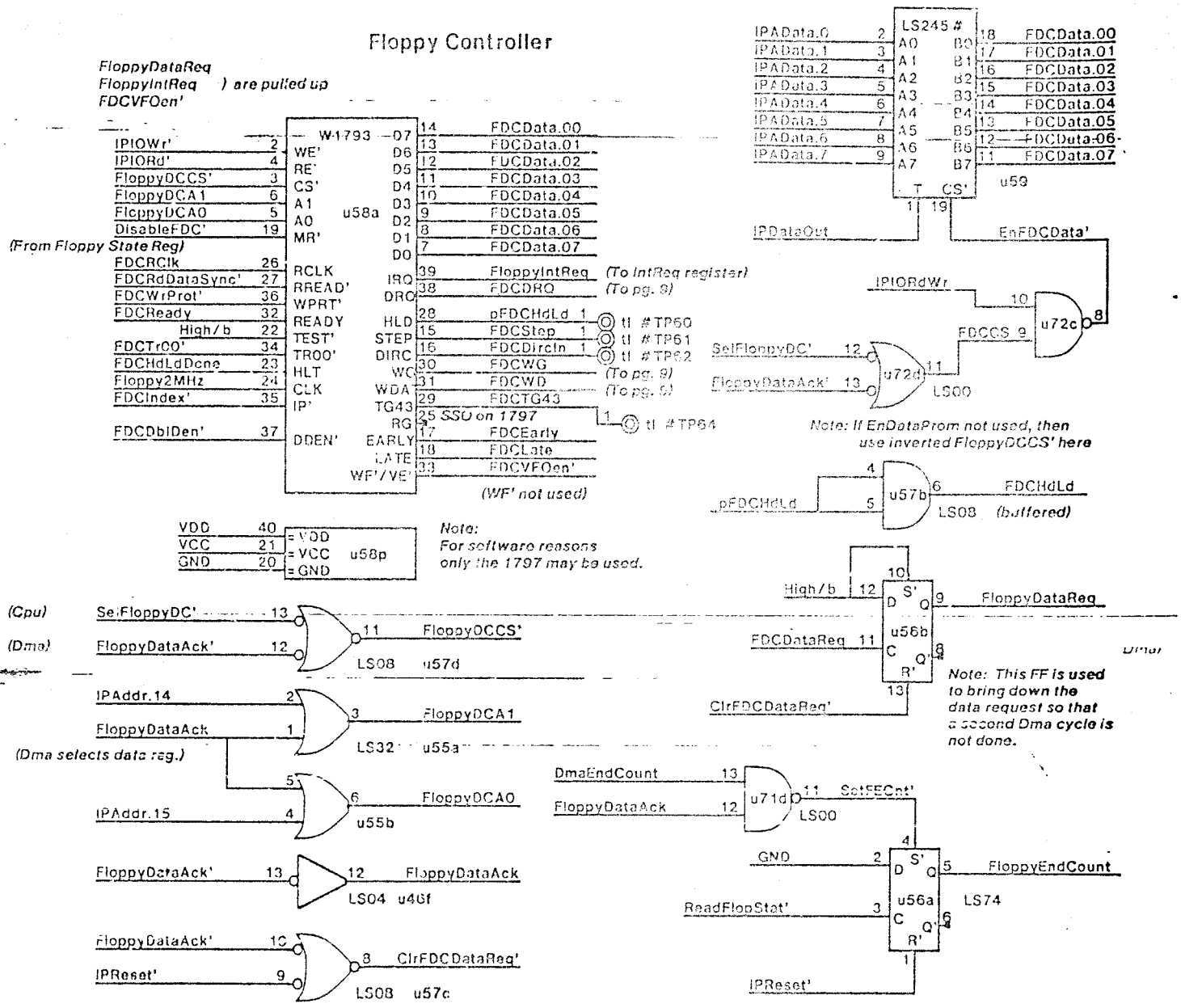
I/O Processor I/O Data Bus Control

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 06 OF	B

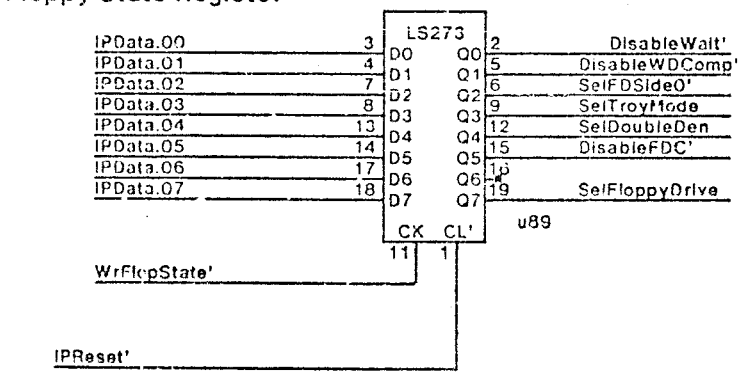


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 07 OF	3

Floppy Controller



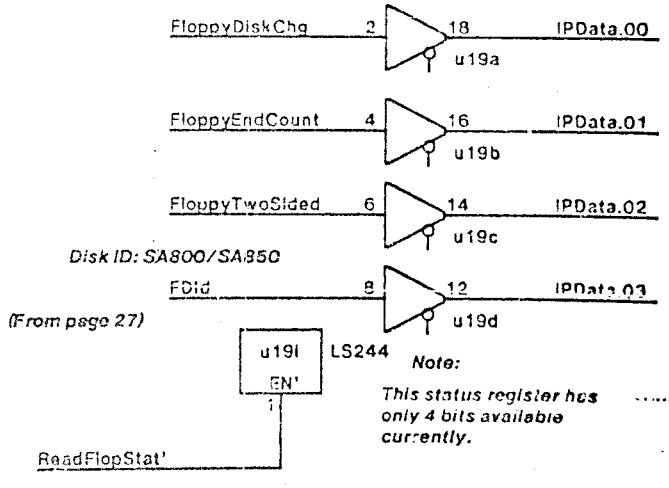
Floppy State Register



State register format:

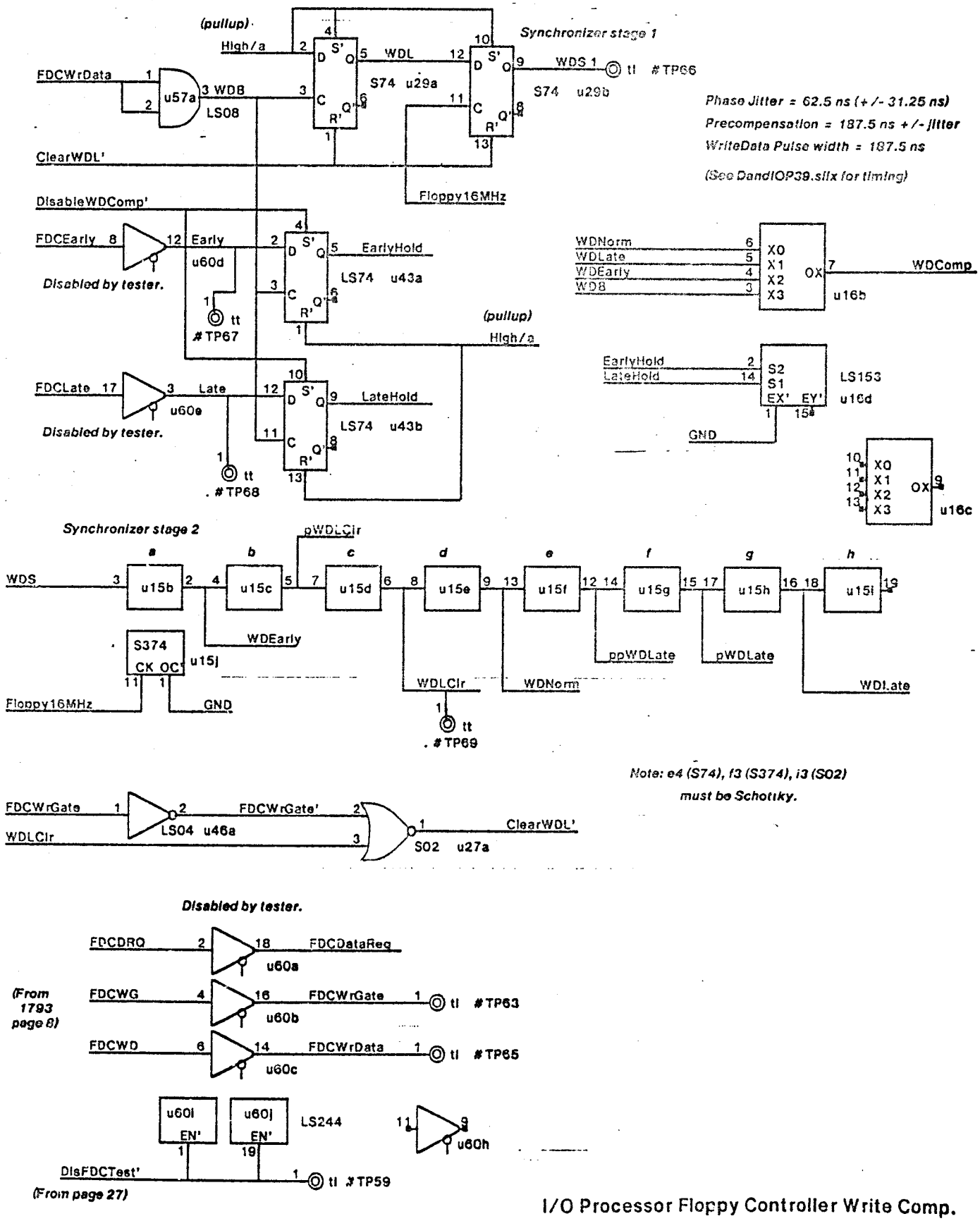
- *Bit 0 - Enable Cpu Waits*
- *Bit 1 - Enable Write PreComp*
- *Bit 2 - Select Side 1*
- *Bit 3 - Select Troy mode*
- *Bit 4 - Select Double Density*
- *Bit 5 - Enable Floppy Controller*
- *Bit 6 - (unused)*
- *Bit 7 - Enable Floppy Drive*

Floppy Status



I/O Processor Floppy Controller

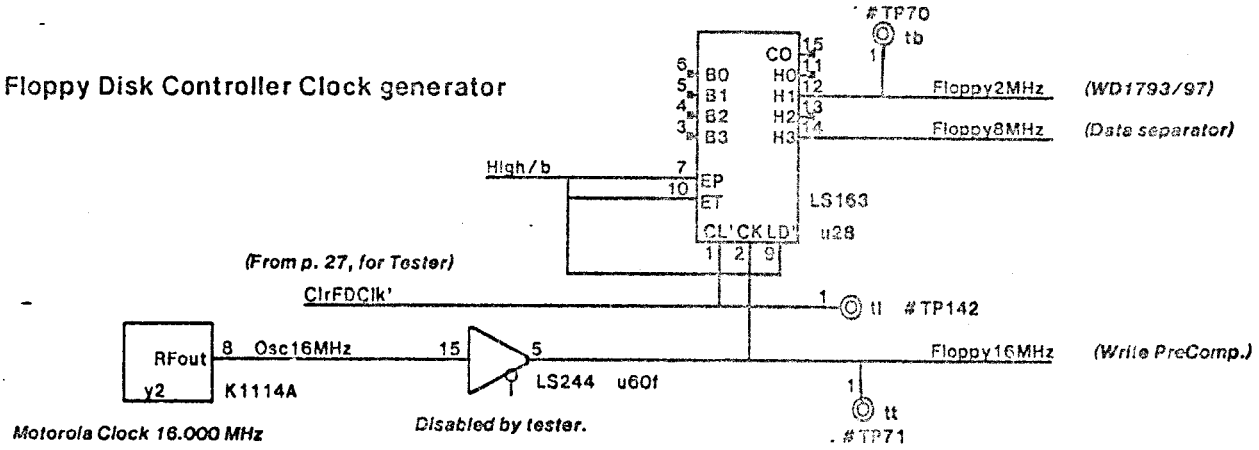
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 08 OF	B



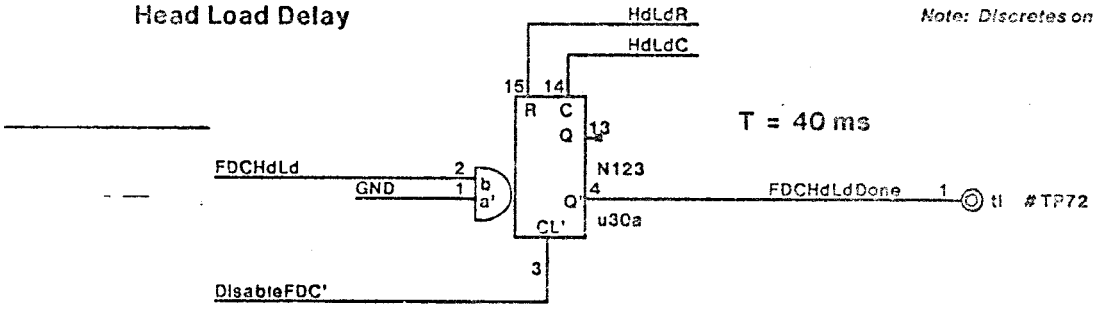
I/O Processor Floppy Controller Write Comp.

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 09 OF	

Floppy Disk Controller Clock generator



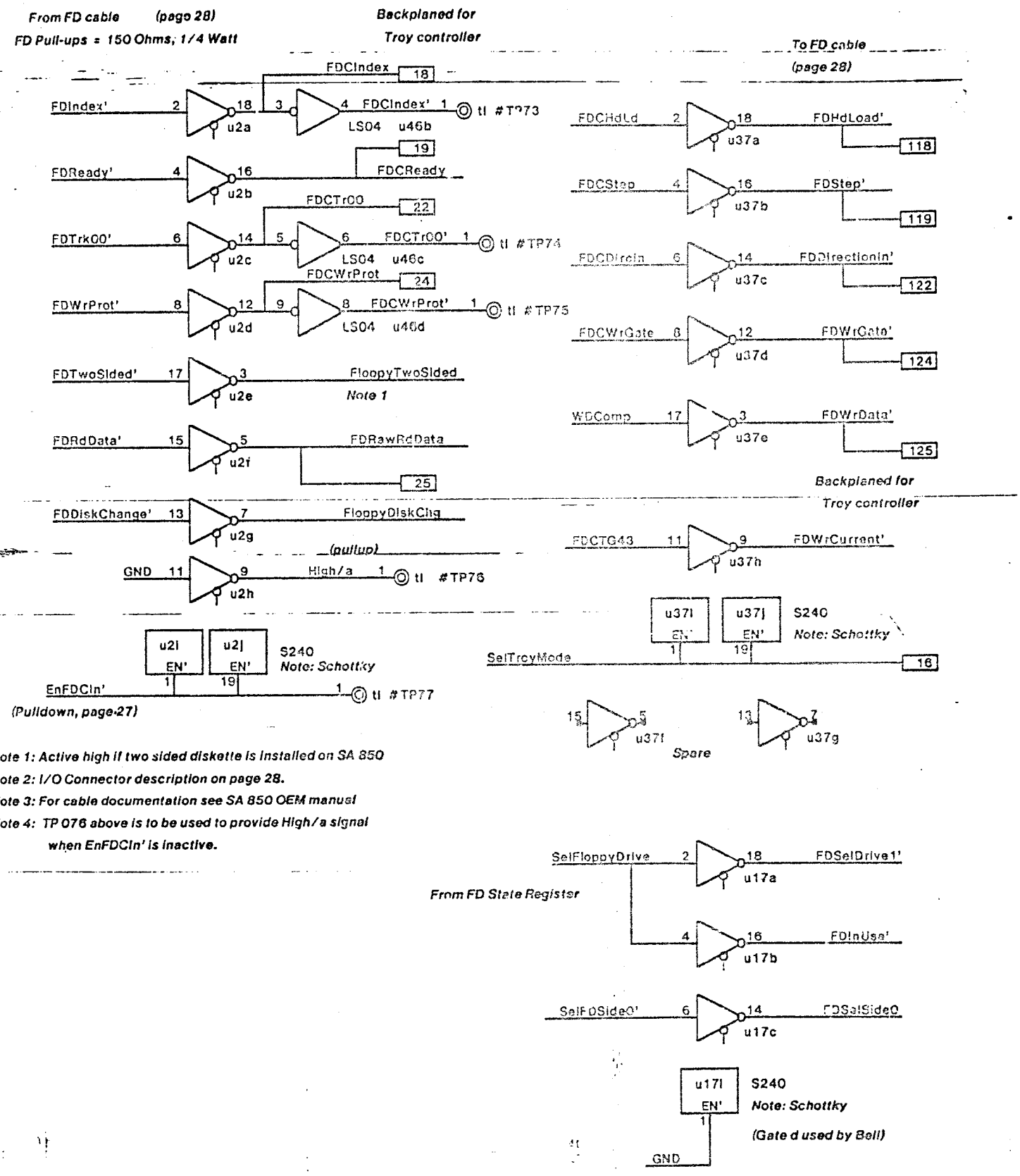
Head Load Delay



Note: Discretes on page 27

I/O Processor Floppy Controller Miscellaneous

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 10 OF	B



Note 1: Active high if two sided diskette is installed on SA 850

Note 2: I/O Connector description on page 28.

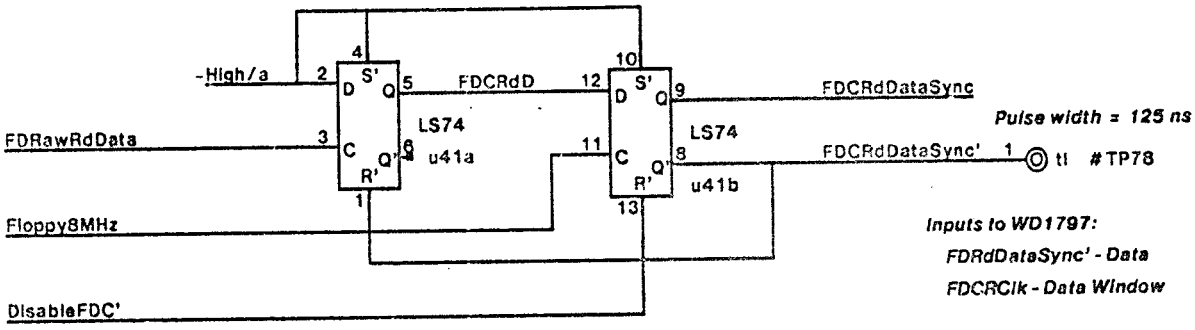
Note 3: For cable documentation see SA 850 OEM manual

Note 4: TP 076 above is to be used to provide High/a signal when EnFDCIn' is inactive.

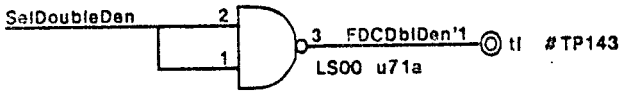
I/O Processor Floppy Disk Receivers/Drivers

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 11 OF	B

Raw Read Data synchronizer and pulse shaper

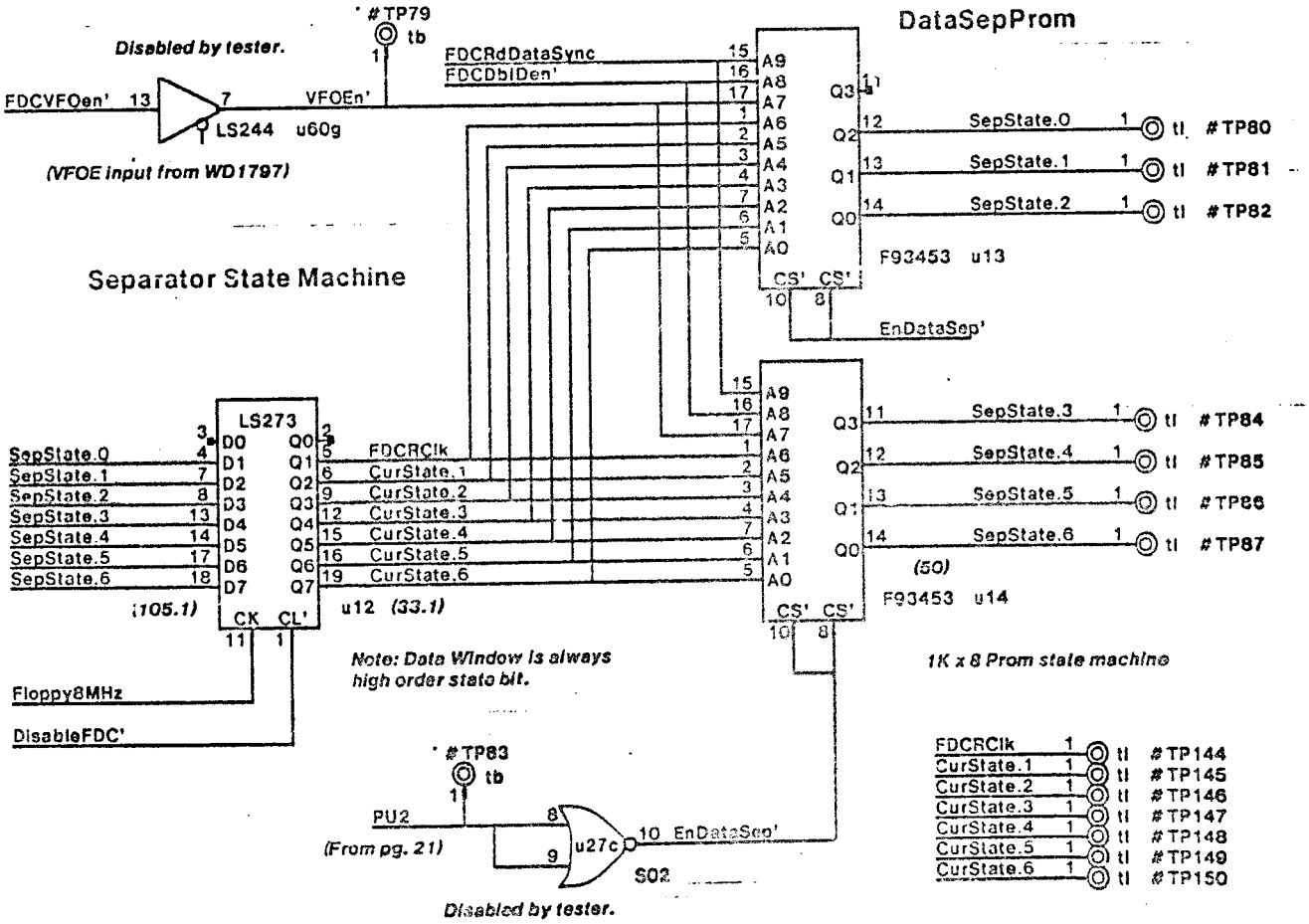


Double density selection



Separator State Machine

DataSepProm



I/O Processor Floppy Data Separator

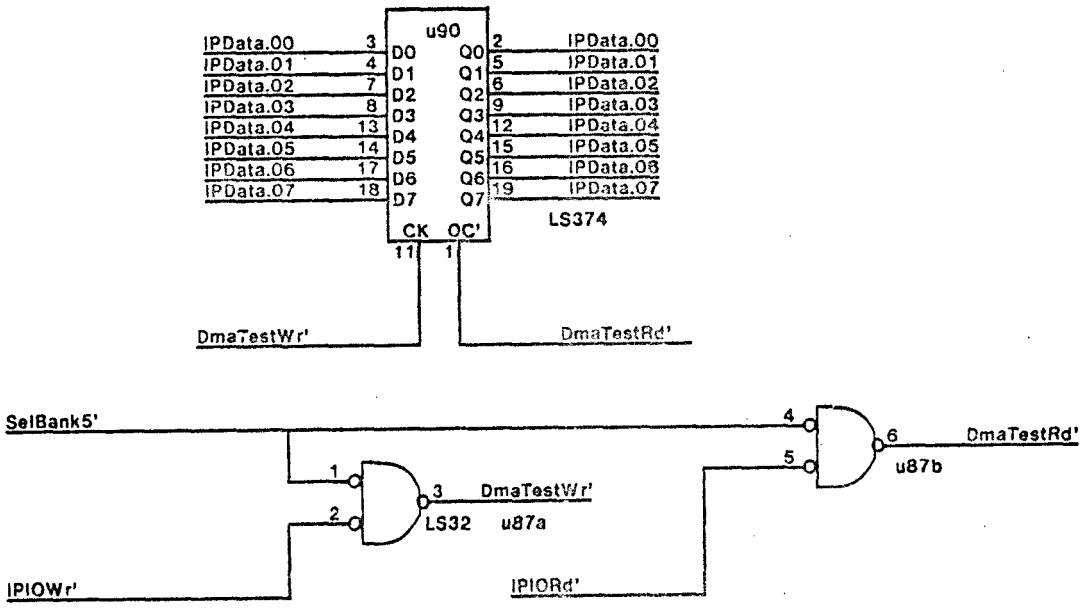
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 12 OF	B

IPData bus Test

This register can be used to test the integrity of the IPData bus, which is the external data bus.

The register can be written and then read back to determine the soundness of the bus.

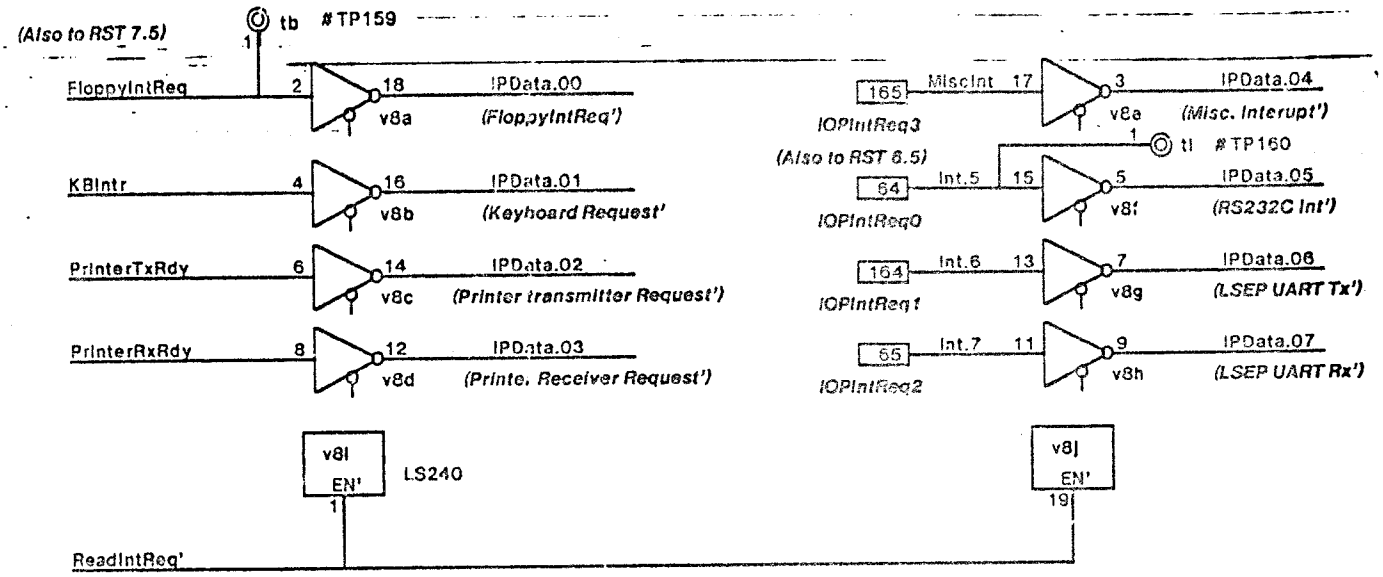
This register uses SelBank5' to enabled it.



I/O Processor IPData bus Test

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 13 OF	B

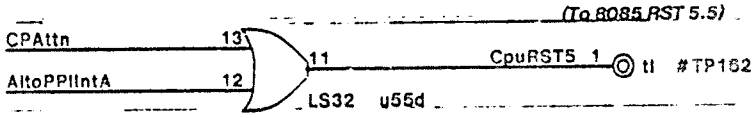
Interrupt Request Register



This register contains the interrupt requests of various devices.

To read true value of the requests, XOR with XOR vector = 1111 1111 (0FFH)

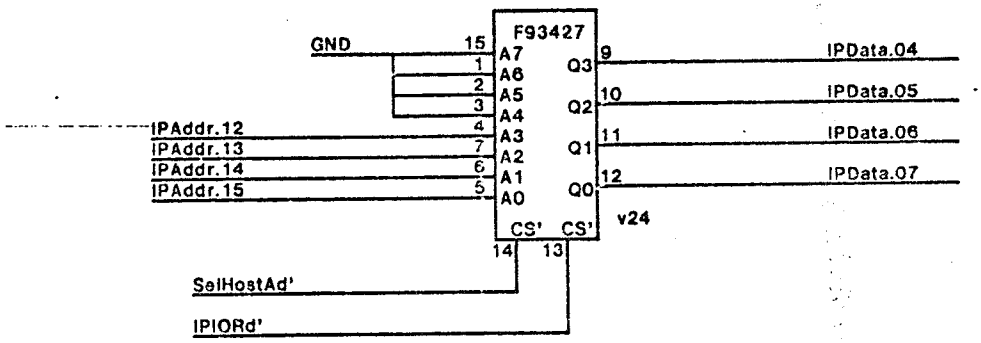
IOPIntReq0 - RS232C - Options
IOPIntReq1 - LSEP UART Tx - Options
IOPIntReq2 - LSEP UART Rx - Options
IOPIntReq3 - Miscellaneous interrupt (from Timer)



RST 5.5 interrupt is for MouseHalt or CPAttn

Host Address Prom

(HostAddrProm)



Host address is 48 bits long, stored in addresses 0 - 11 of the Prom.

Address 12, 13 contains an 8-bit checksum, 14, 15 contains the complement of the checksum.

Host address Prom has the 16 I/O Bank 3 addresses.

I/O address	*Host address bits*
0B0H	*0:3*
/	/
0BBH	*44:47*
0BCH, 0BDH	*checksum*
0BEH, 0BFH	*checksum'*

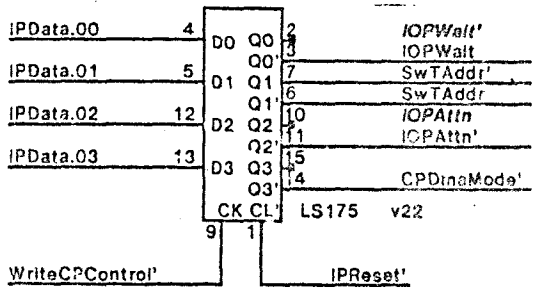
I/O Processor Interrupt Req. reg, Host address

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 14 OF	

Central processor control
CP port control

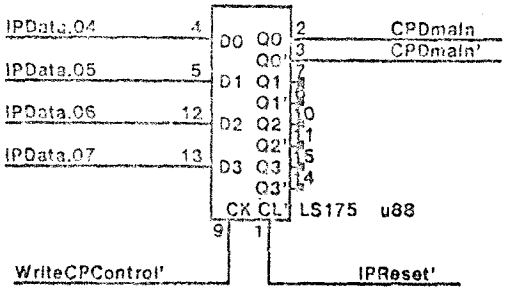
Data:

- Bit 0 - Enable CP (remove Wait)
- Bit 1 - Switch TPC address from NIAX
- Bit 2 - Set CP Attention
- Bit 3 - Set Dma Mode for CP port
- Bit 4 - Set Dma Mode for CPport as input/output'

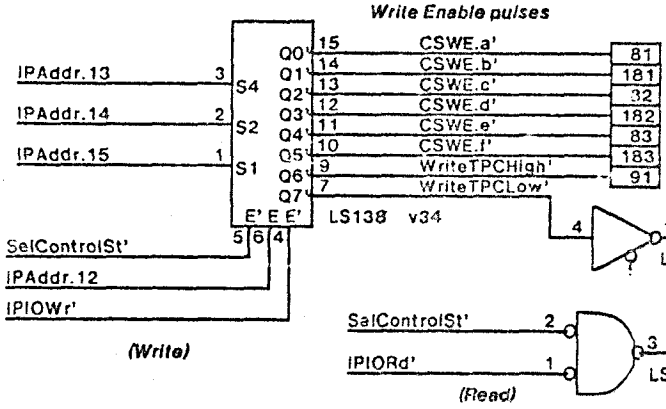


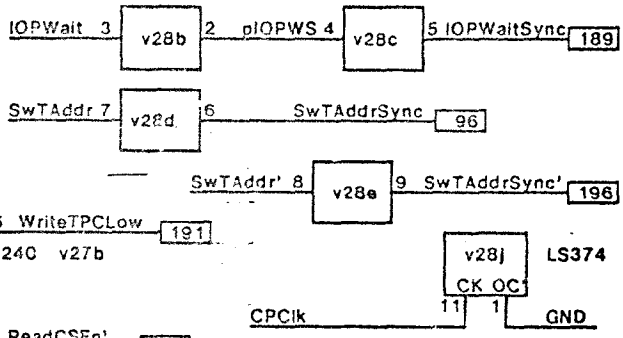
(IOPWait and SwTAddr should be true after booting)

Normal state of register is 1100 0xxx



Control Store handling





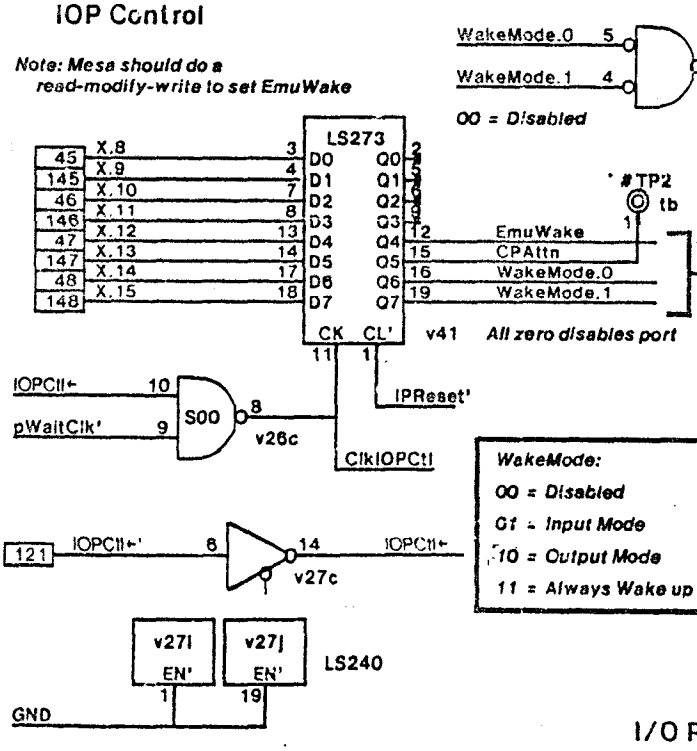
Note: All 16 addresses will respond for Read, use 8-15.

(Bank 7, registers 8-15, addresses 0F8 - 0FFH)

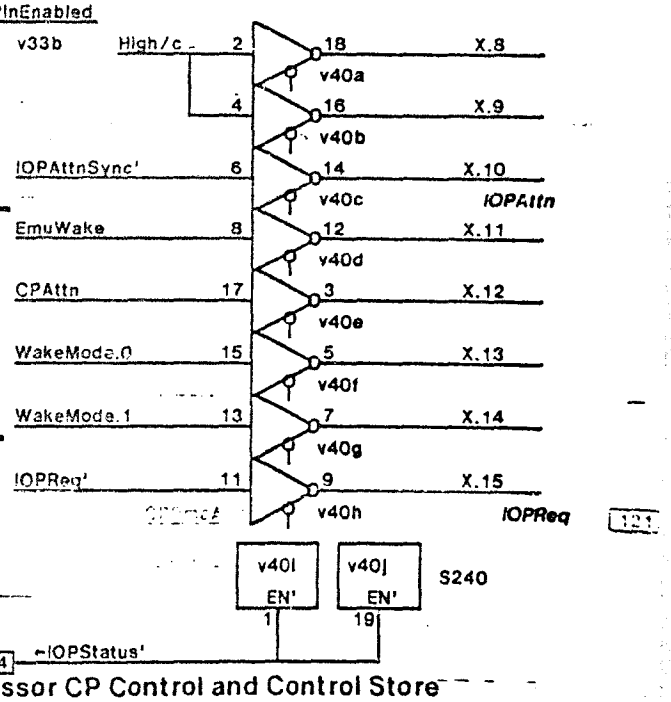
Central Processor registers

IOP Control

Note: Mesa should do a read-modify-write to set EmuWake



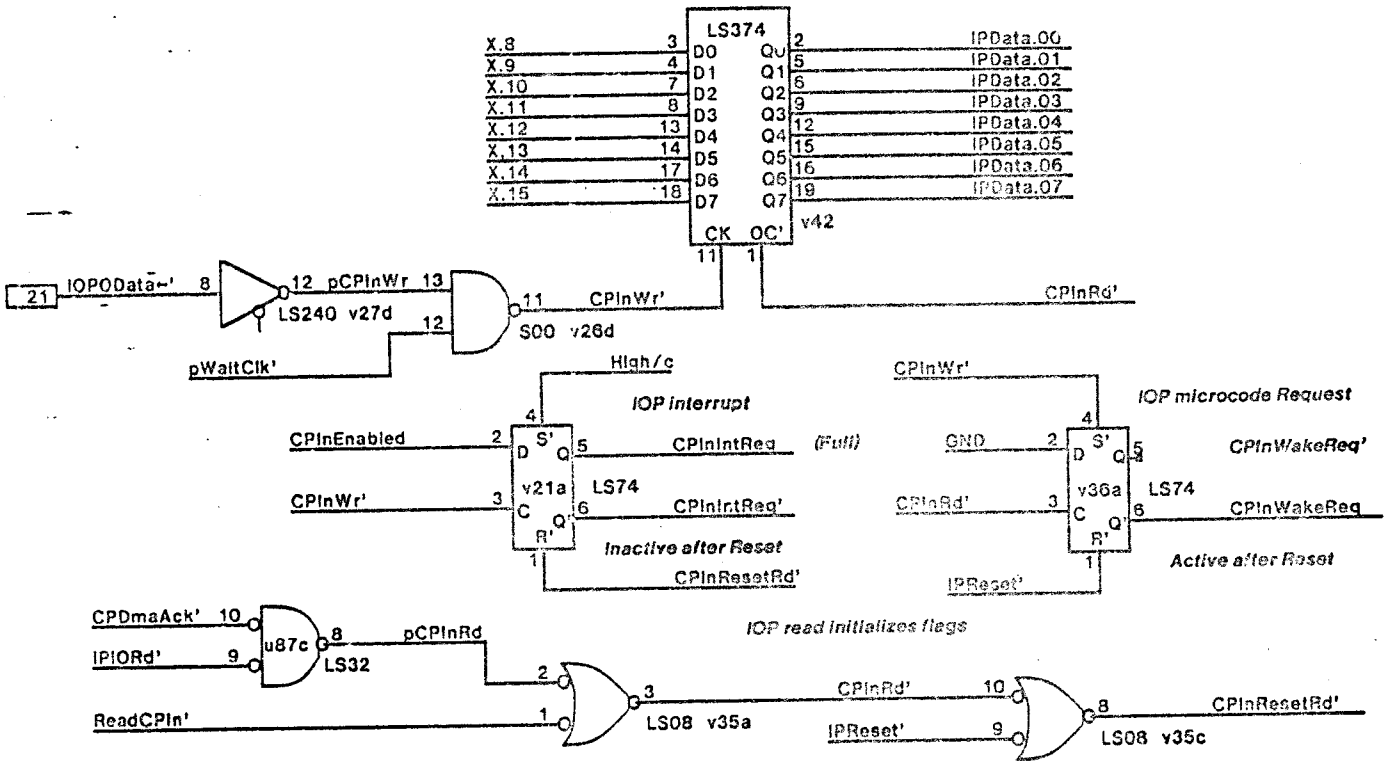
IOP Status



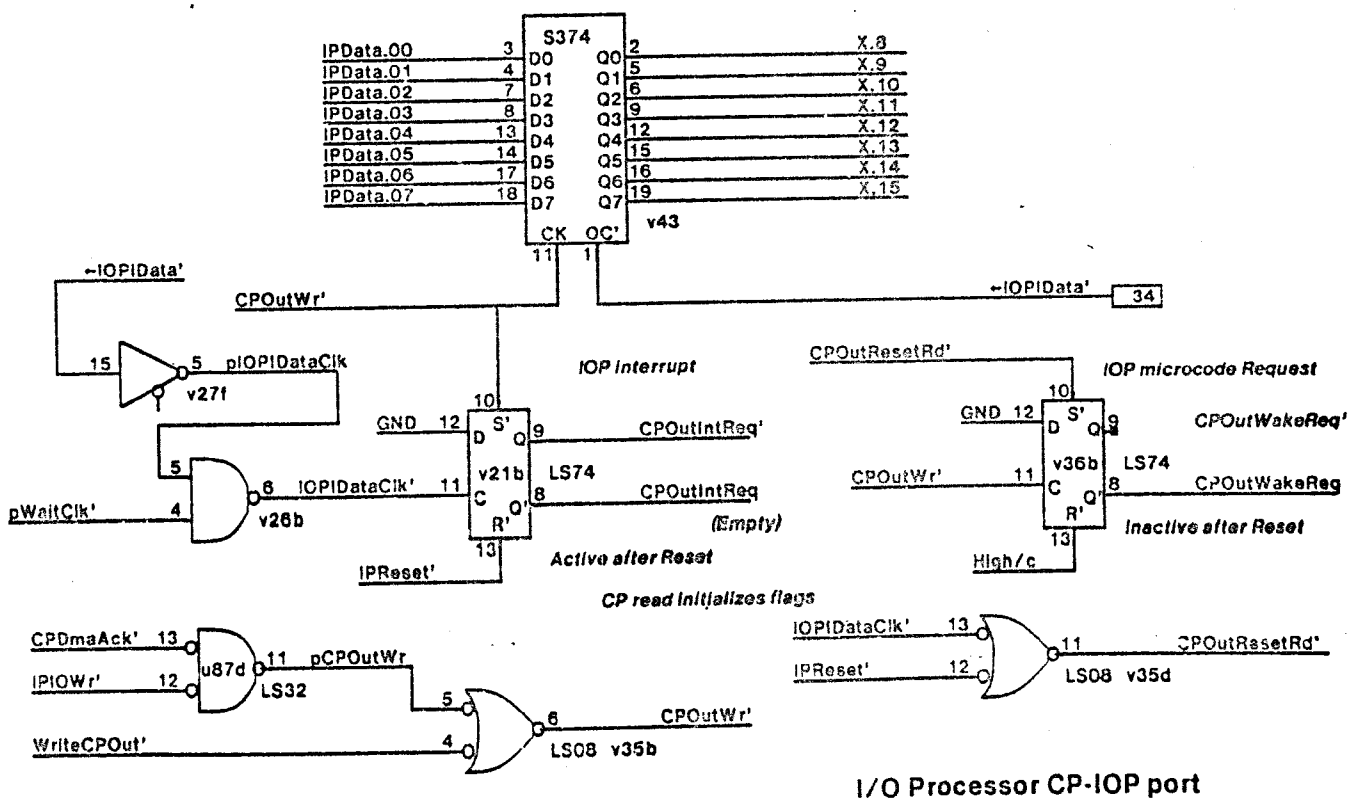
I/O Processor CP Control and Control Store

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 15 OF	

CPIn (From CP)



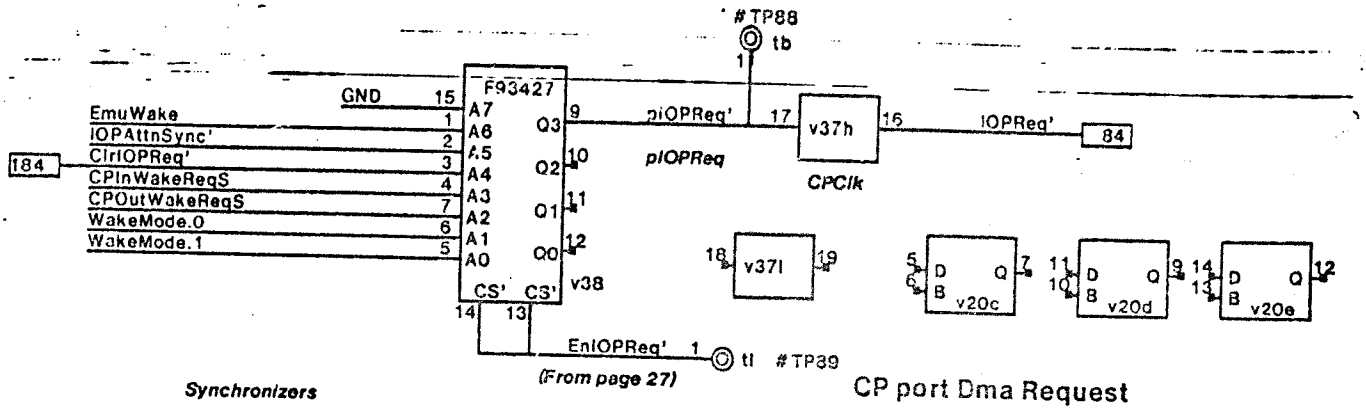
CPOut (To CP)



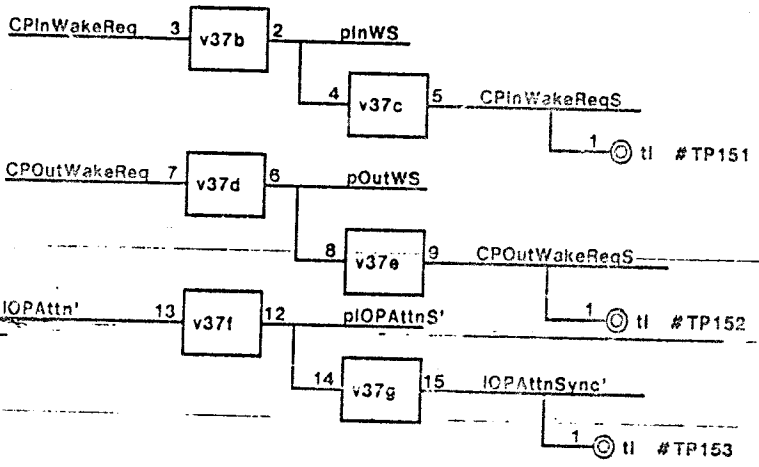
I/O Processor CP-IOP port

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 16 OF	B

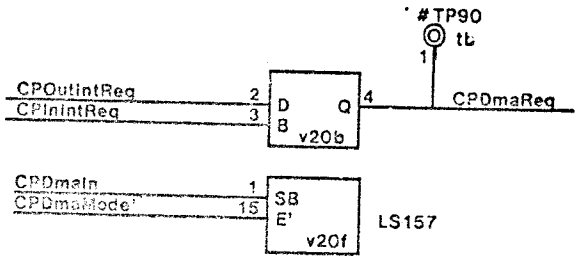
IOPReq



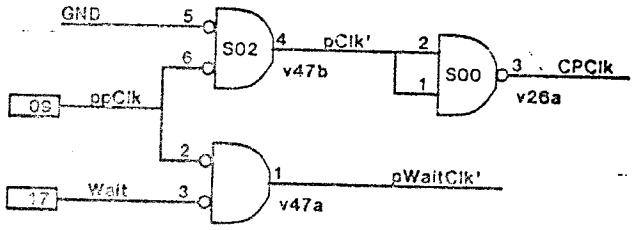
Synchronizers



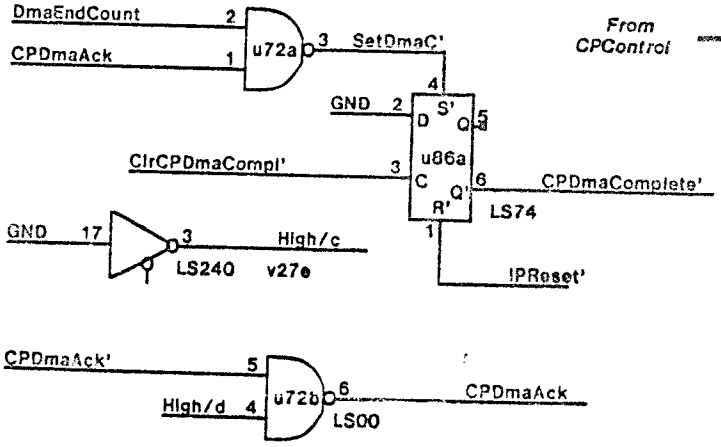
CP port Dma Request



CP Clock

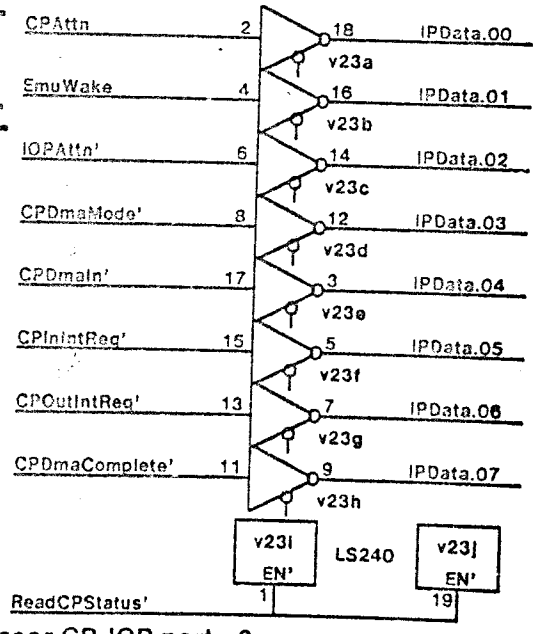


CP port Dma Complete



CP port status

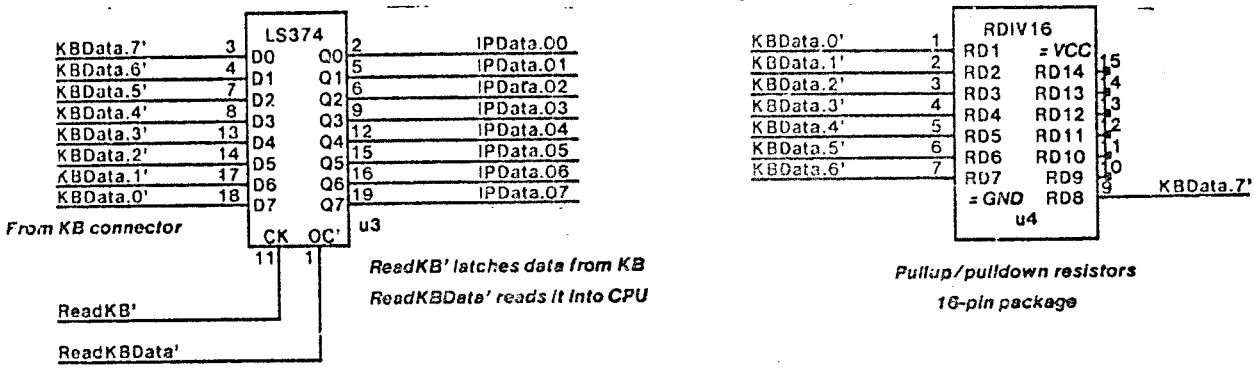
Also to I8085 RST 5 (with MouseHalt)

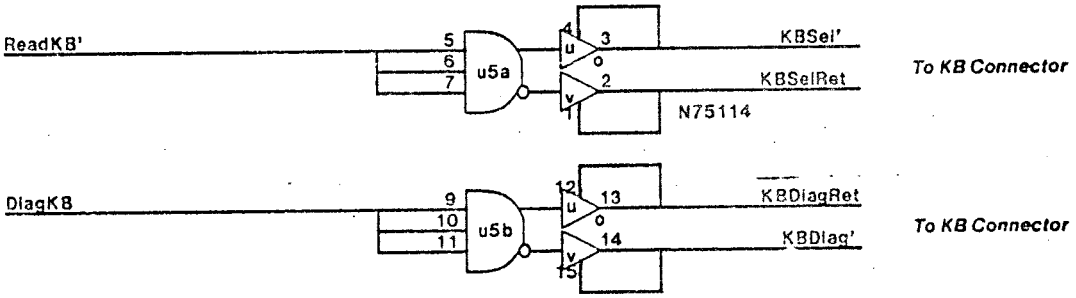


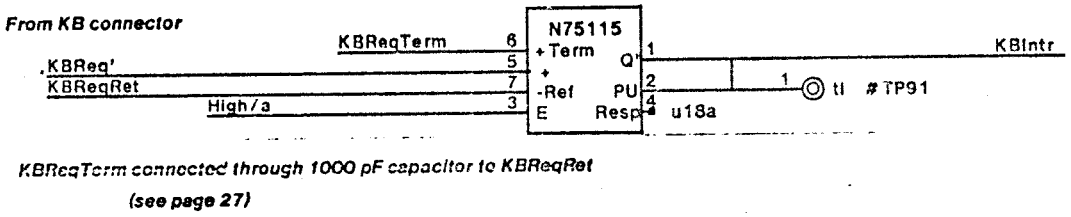
I/O Processor CP-IOP port - 2

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 17 OF	

Keyboard Data





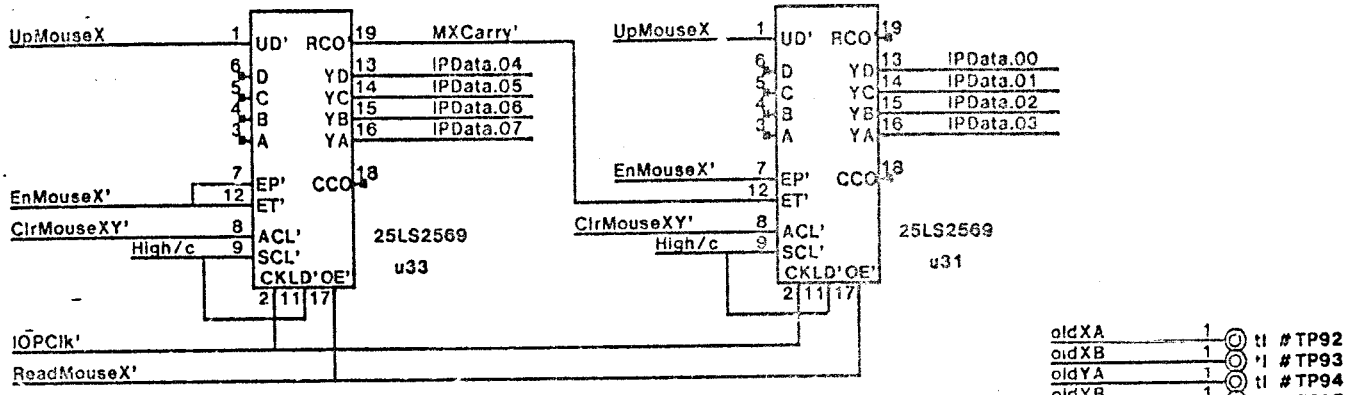


Bell circuit on page 27.

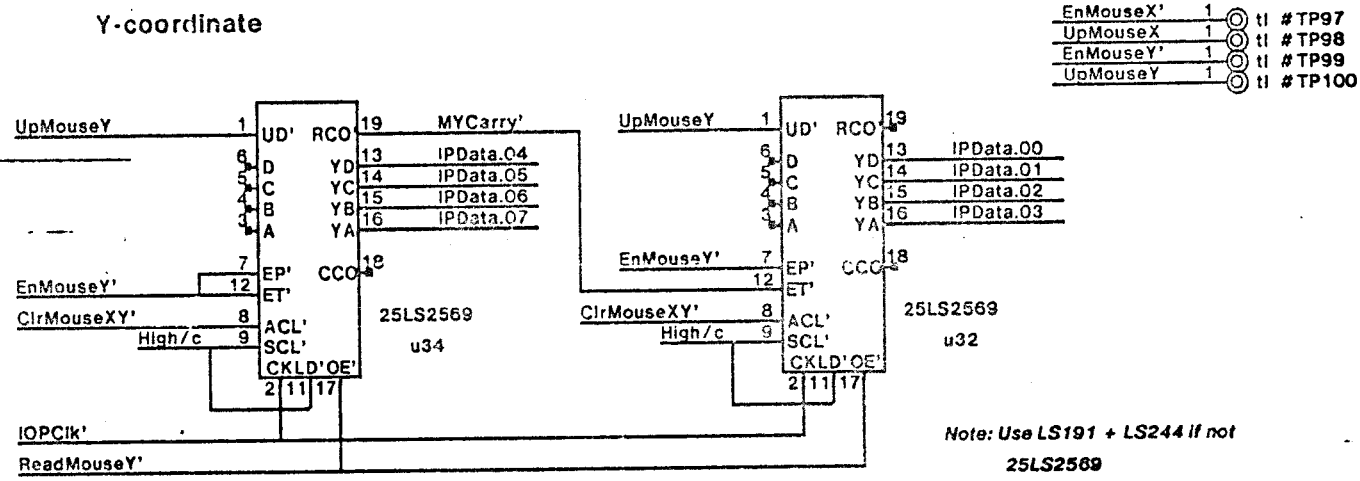
I/O Processor Keyboard Interface

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 18 OF	B

X-coordinate



Y-coordinate

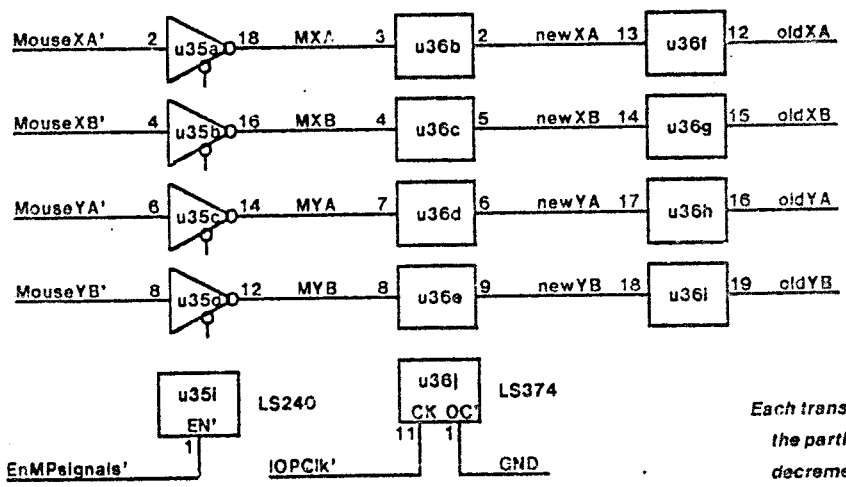


Note: Use LS191 + LS244 if not 25LS2569

From KB connector

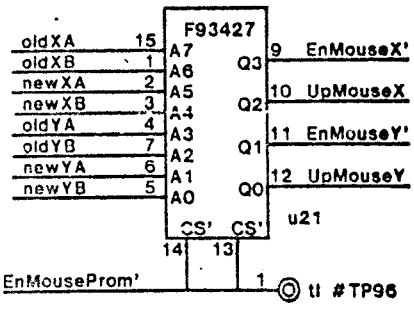
New sample

Old sample



(Note: u35 is powered by MVcc. This signal tristates outputs during power down.)

MouseProm

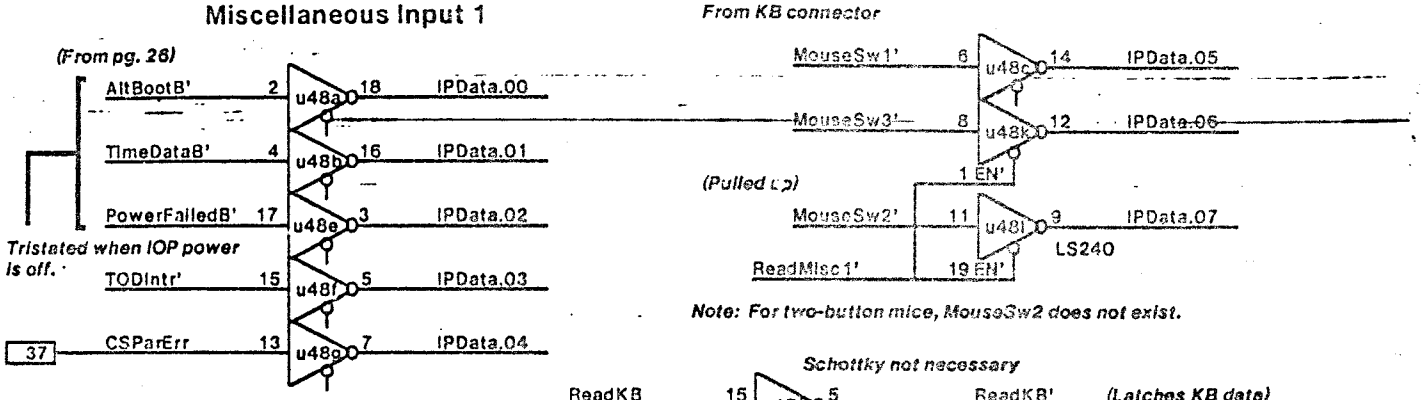


Each transition of XA or XB (YA or YB) causes the particular counter to be incremented or decremented. The samples are made with the inverted processor clock to ensure that the counters are stable when a read or clear of the counters is done.

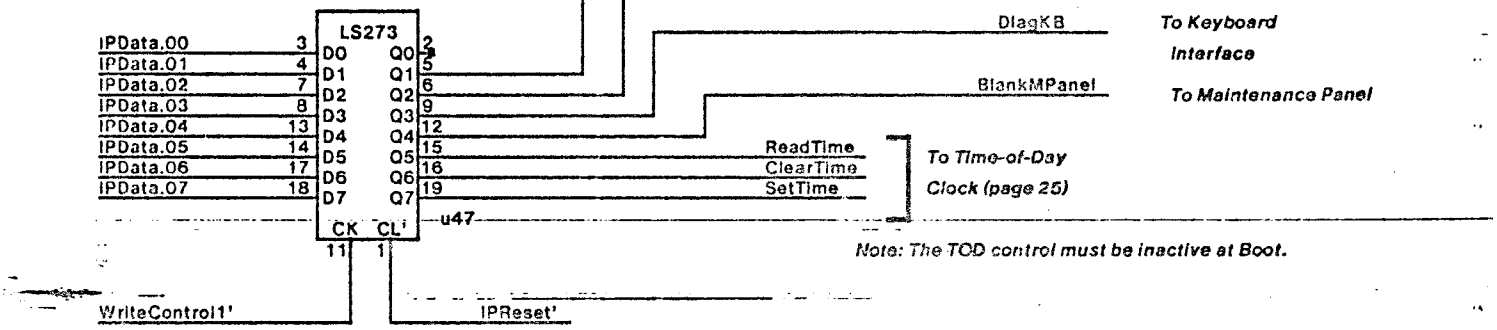
I/O Processor Mouse interface

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 19 OF	

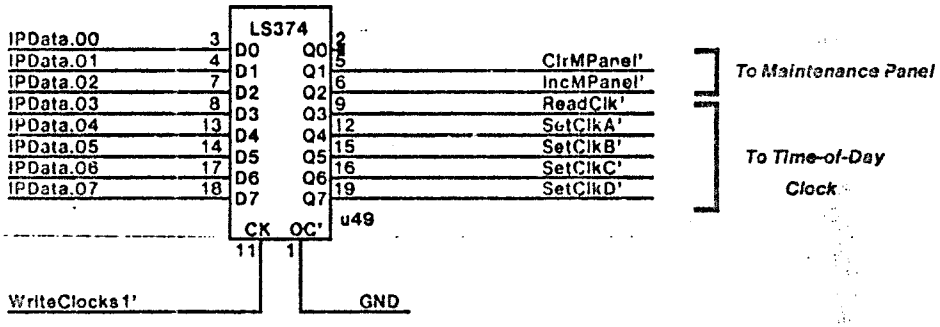
Miscellaneous Input 1



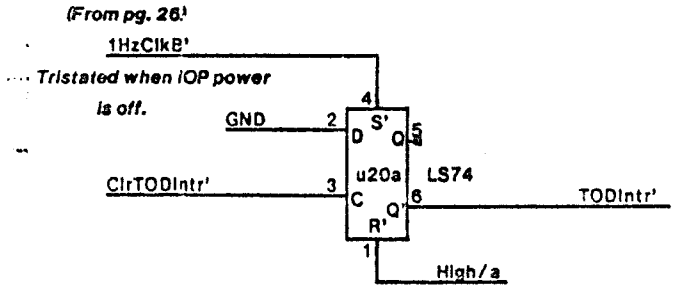
Miscellaneous control 1



Miscellaneous Clocks 1



Time-of-Day 1 second interrupt



Procedure to read time:

- *Wait for TODIntr to be set*
- *When set, clear and wait for it to be set again*
- *read time*

(maximum delay = 2 seconds)

Alternative:

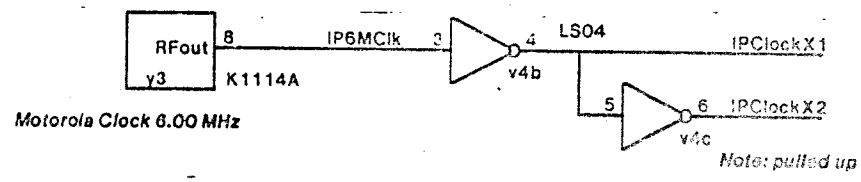
- *clear TODIntr (if being set will not be cleared)*
- *wait until set*
- *read time*

(maximum delay = 1 second)

I/O Processor TOD/MP interface, misc. reg.

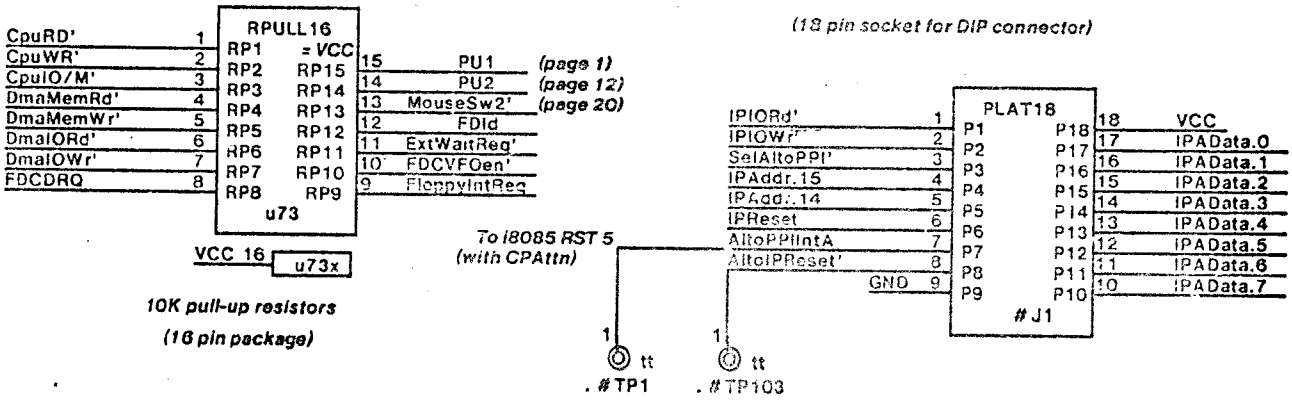
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 20 OF	B

IOP CPU Clock generator



Dip Cable to Alto-IOP interface

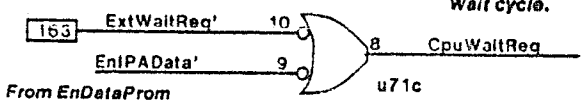
(18 pin socket for DIP connector)



External Waits can be requested from the Options card. The RS232 will require a Wait cycle.

(Pulled up)

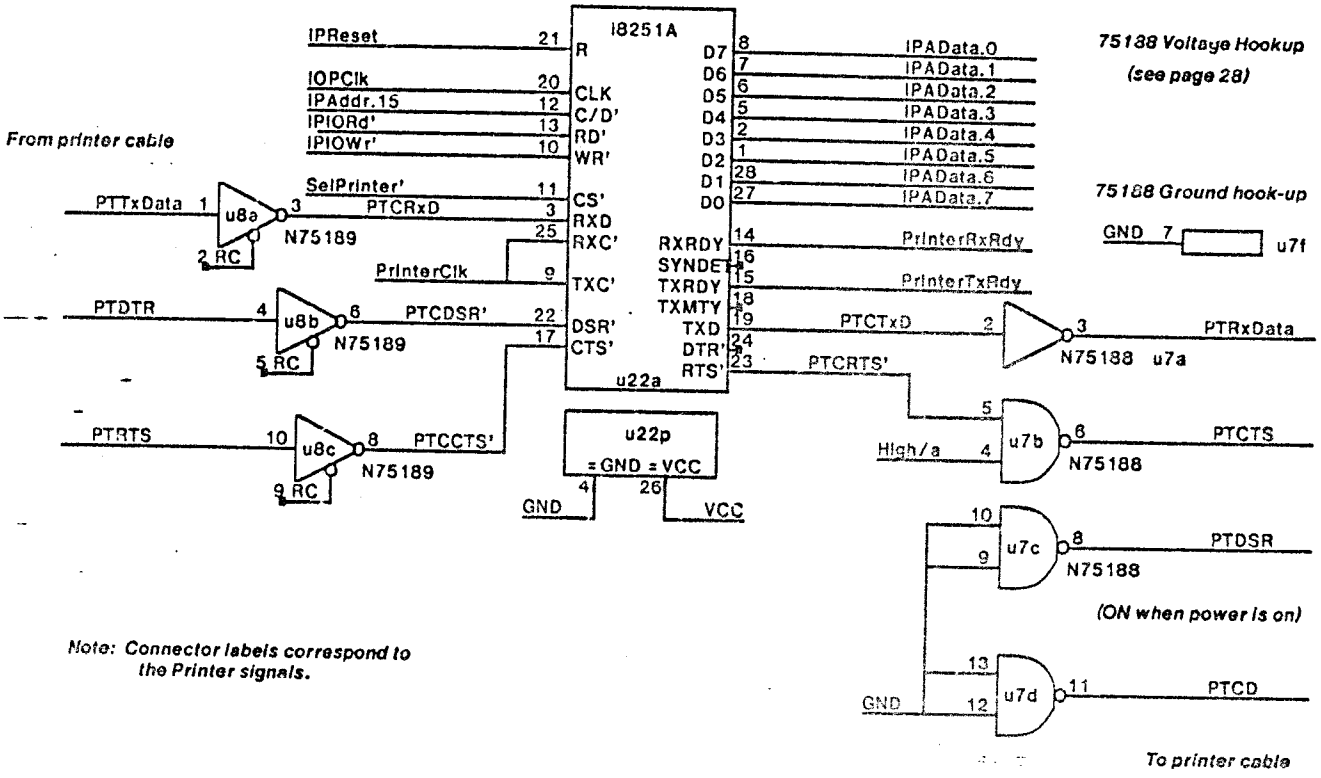
Currently, all devices on IPAData cause a Wait cycle.



I/O Processor Miscellaneous CPU control

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 21 OF	B

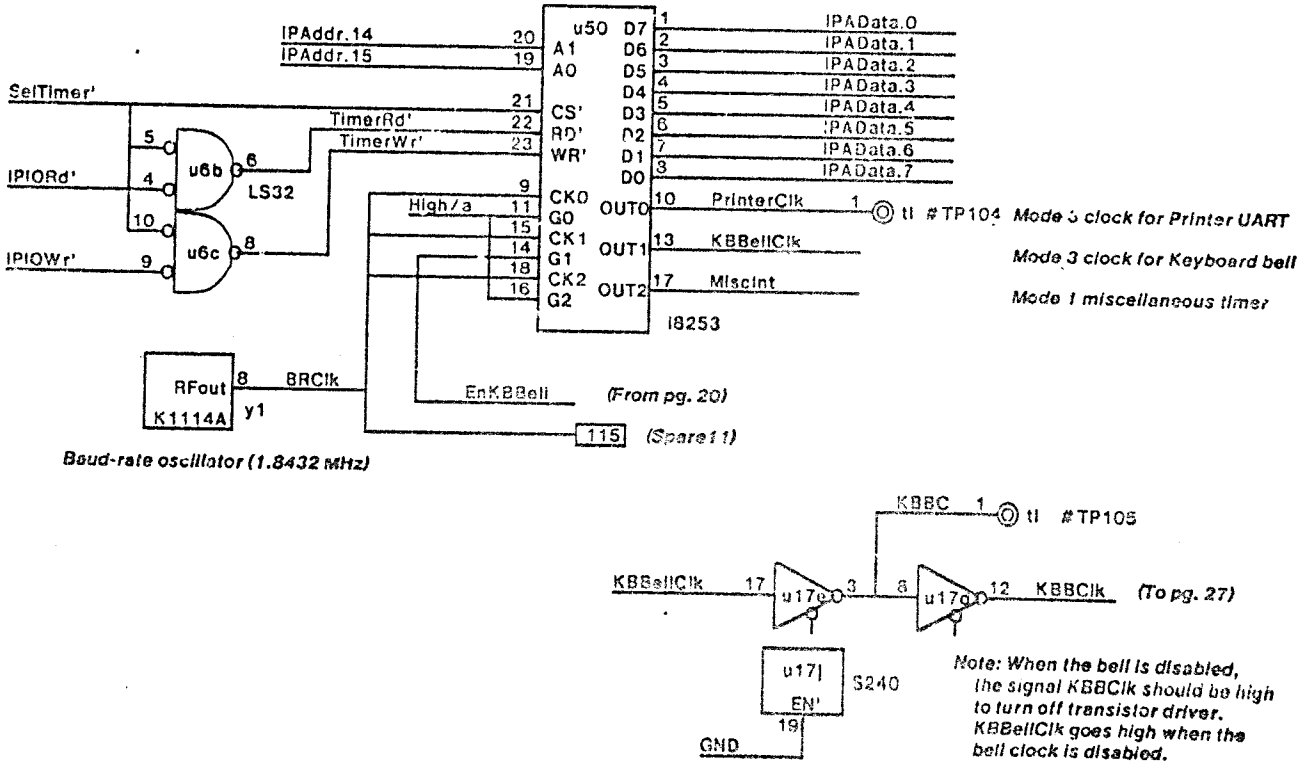
Printer UART



Note: Connector labels correspond to the Printer signals.

Note: Due to a design shortcoming the RD' and WR' lines of the 8253-5 must be externally qualified.

Baud-rate generator

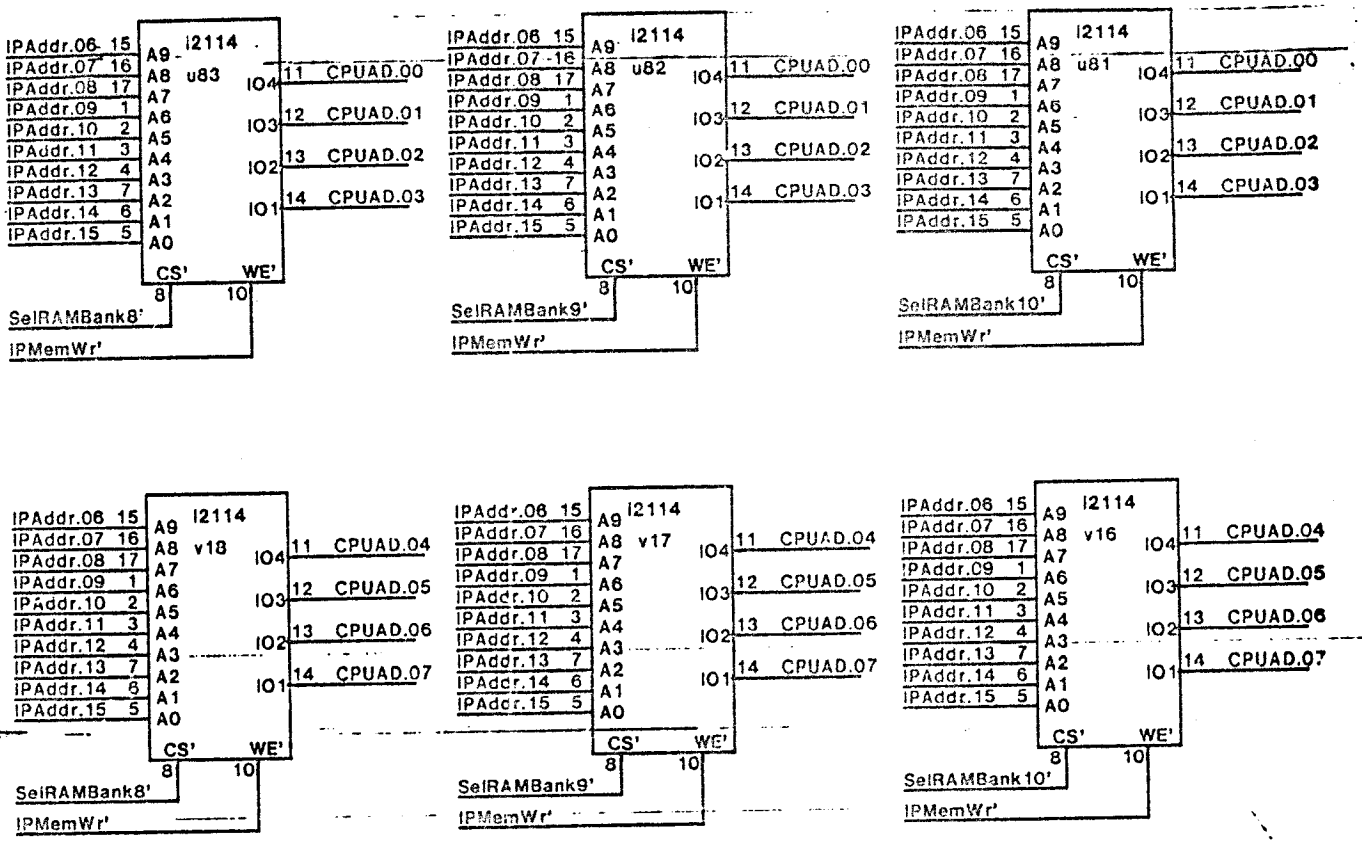


Note: When the bell is disabled, the signal KBBClk should be high to turn off transistor driver. KBBellClk goes high when the bell clock is disabled.

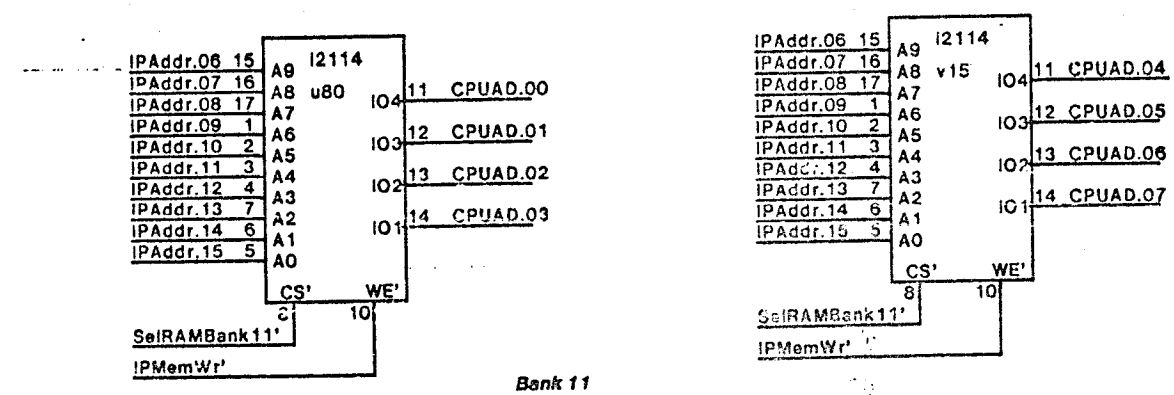
I/O Processor Diablo Priner Interface

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 22 OF	

RAM - Banks 8 - 11



Bank 8 *Bank 9* *Bank 10*

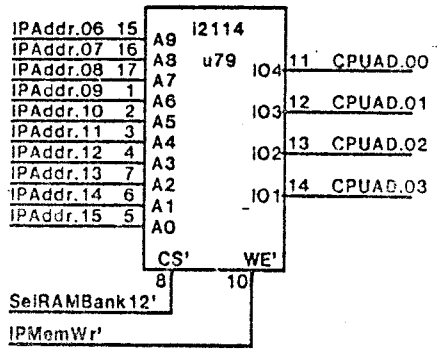


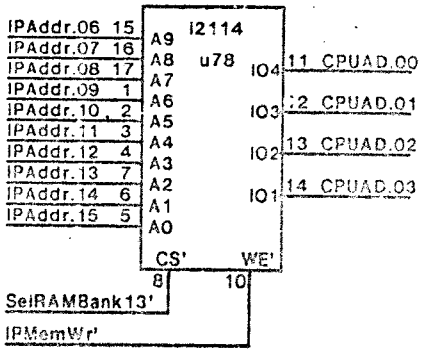
Bank 11

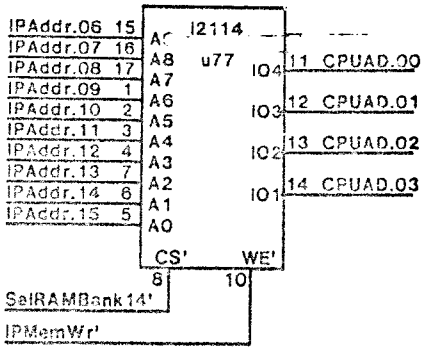
I/O Processor 4K RAM Memory-Banks 8-11

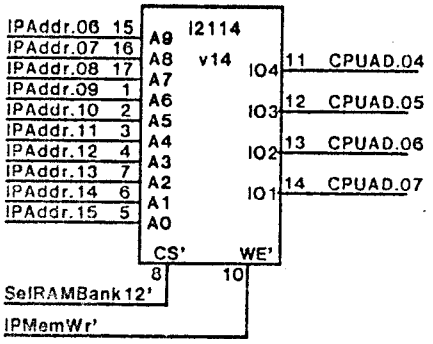
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 23 OF	

RAM - Banks 12 - 15

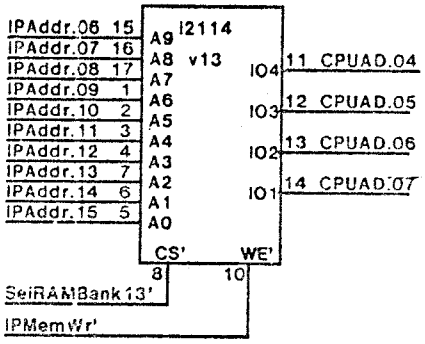




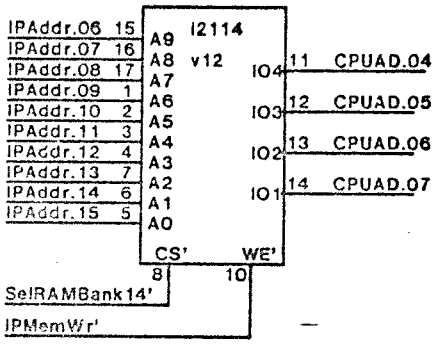




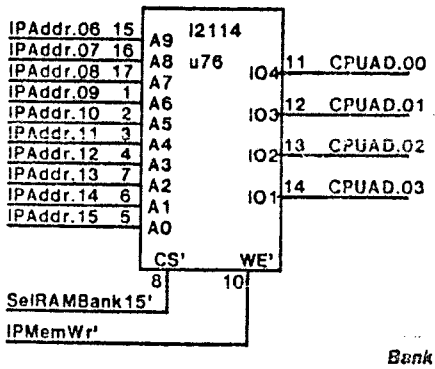
Bank 12



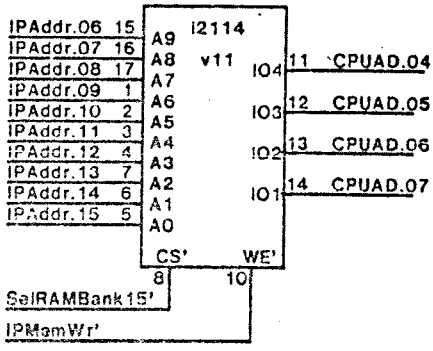
Bank 13



Bank 14



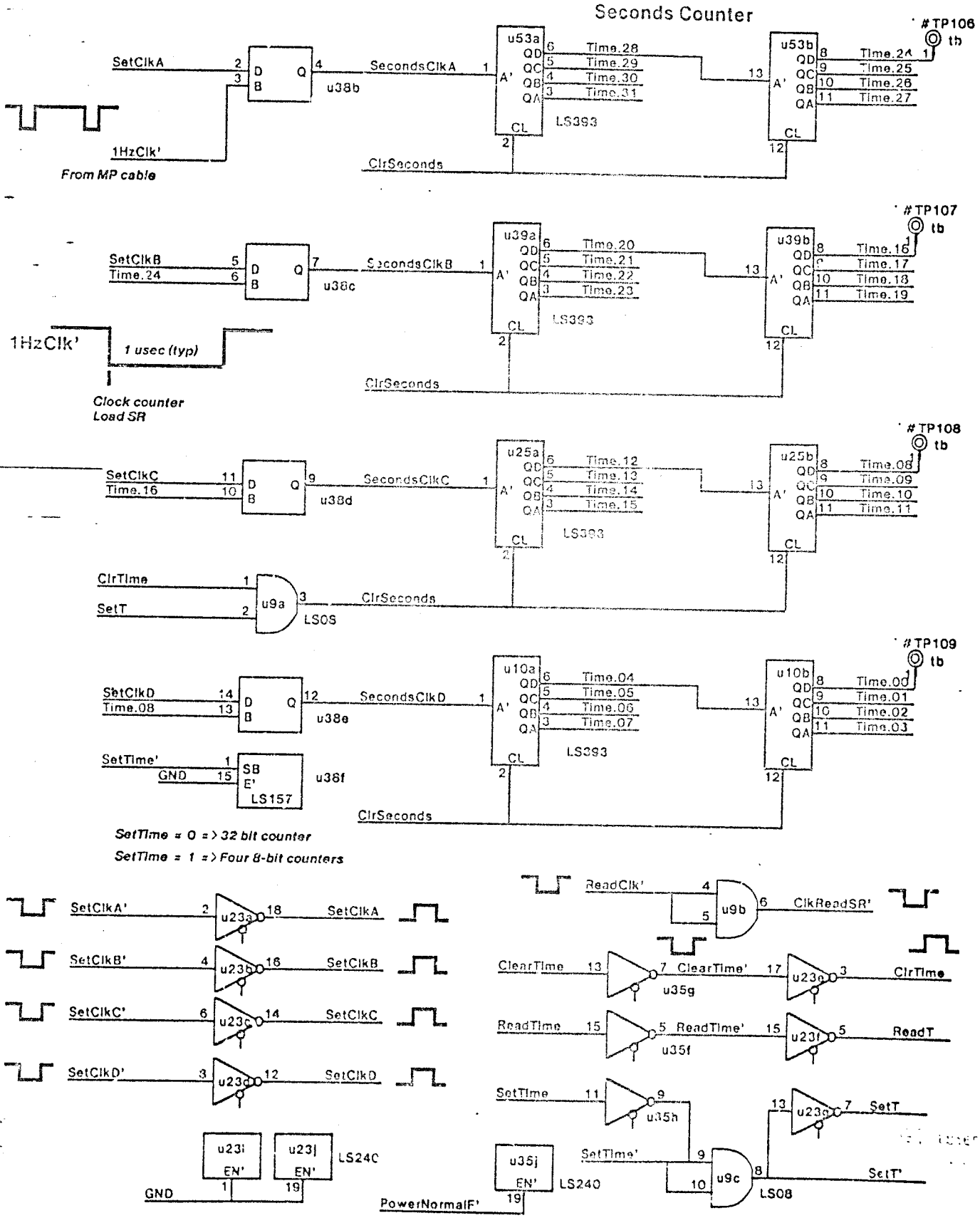
Bank 15



I/O Processor 4K RAM Memory-Banks 12-15

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 24 OF	B

Note: All the logic on this page is powered from the Maintenance panel +5V supply, MVcc (see page 26)



The 8 inputs SetClkA', SetClkB', SetClkC', SetClkD', ReadClk', ClearTime', ReadTime', SetTime' are pulled up for power-down condition.

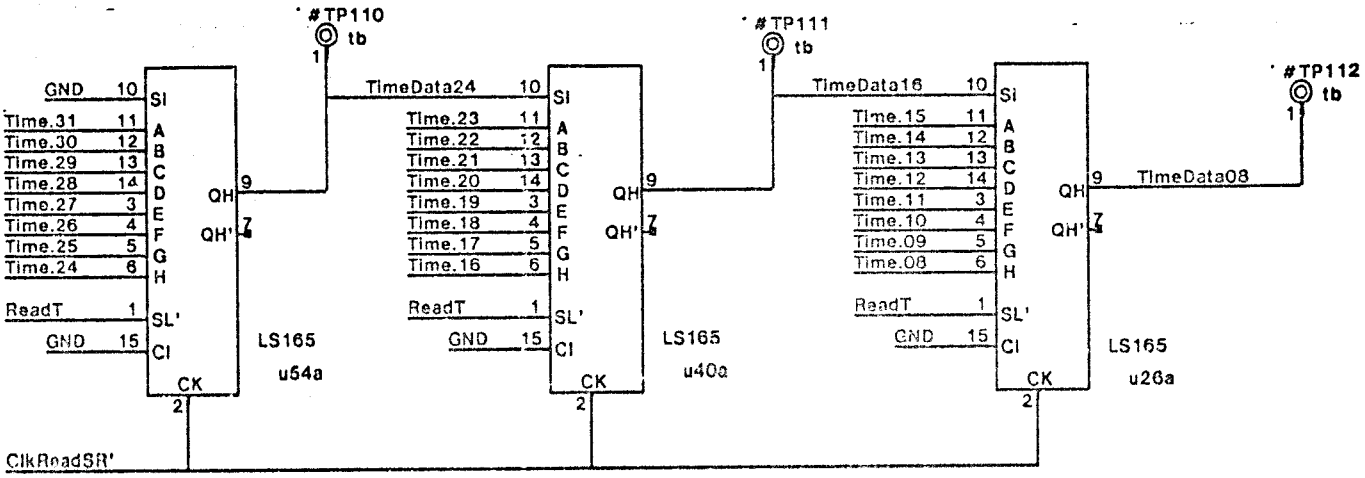
I/O Processor Time-of-Day Clock - 1

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 25 OF	

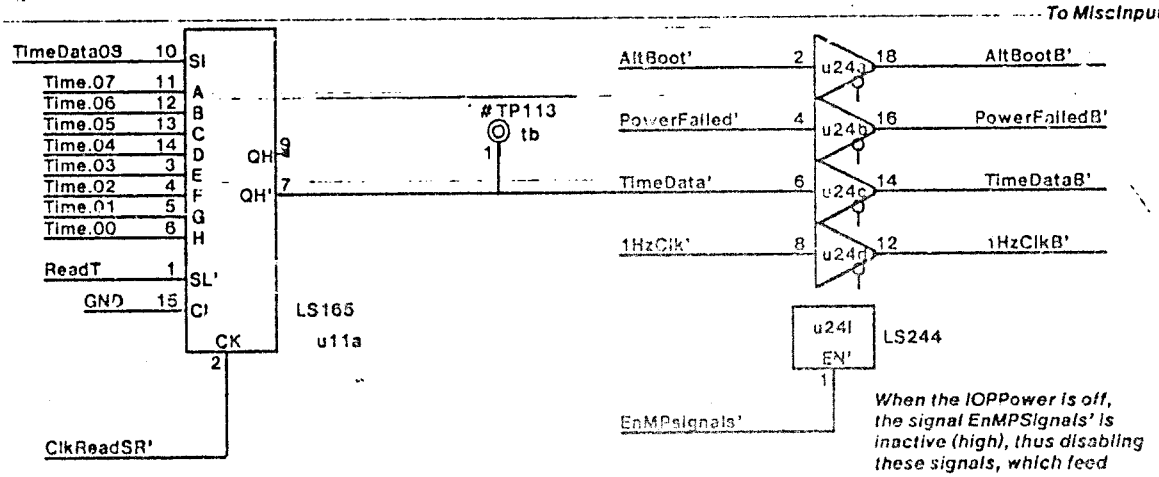
Note: All the logic on this page is powered from the Maintenance panel +5V supply, MVcc

Time Read Shift Register

ReadTime = 0 =>
Shift register parallel loads Seconds Counter
ReadTime = 1 =>
Shift register in serial shift mode, ClkReadSR' clock

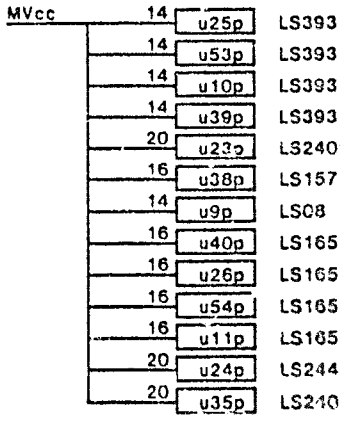


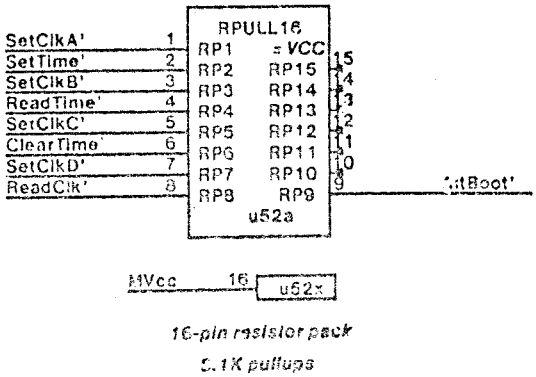
To MiscInput1



When the IOPPower is off, the signal EnMPSignals' is inactive (high), thus disabling these signals, which feed unpowered logic.

Power for Time-of-day clock from Maintenance Panel

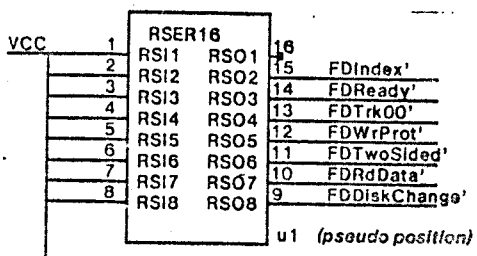


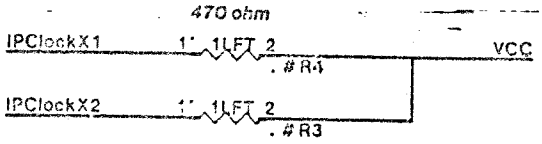


I/O Processor Time-of-Day Clock - 2

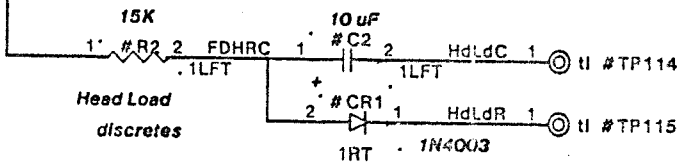
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 26 OF	B

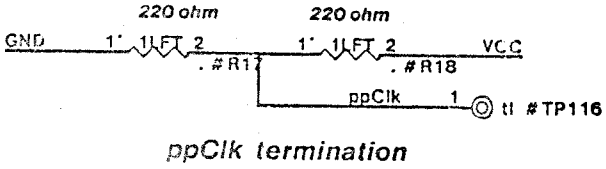
Pullups, 150 ohm, 1/4 watt
Allen-Bradley 3168151





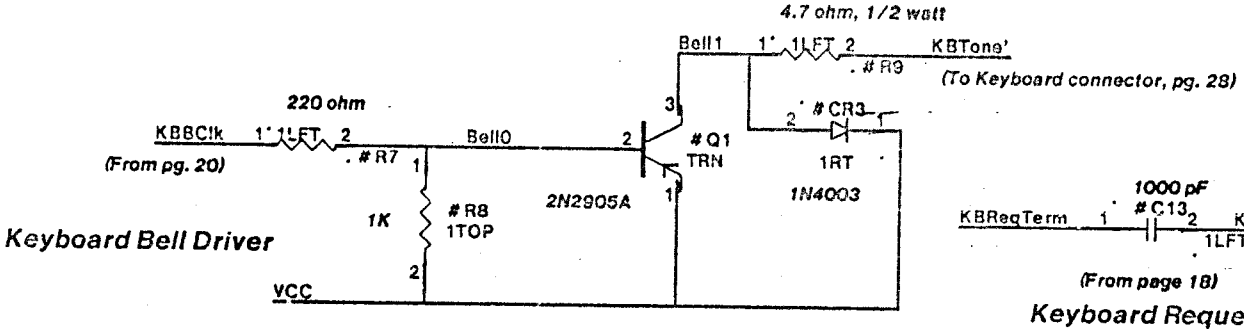
CPU clock driver pull-ups



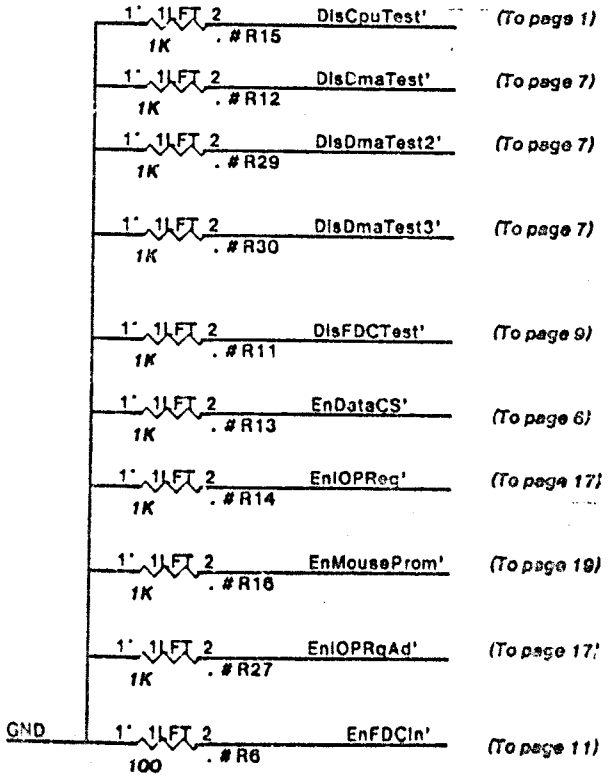


ppClk termination

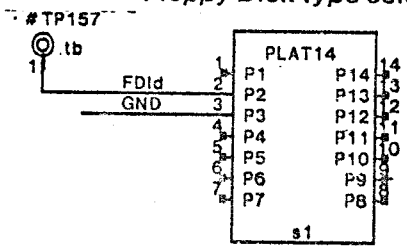
Miscellaneous Floppy Controller discrete components



Discretes for Testability



Floppy Disk type selector Dip switch

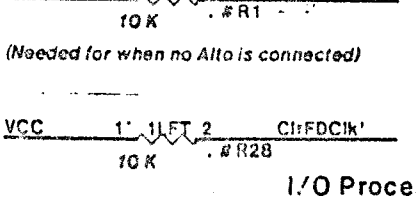


(2-switch DIPSwitch)

This is the switch to select the type of Floppy Disk drive in the system. Only 1 switch is needed, and should be the rightmost switch of a DIPSwitch package. The smallest package should be used.
The package should be inserted in the spare position between u50 and u51, or below u74, whichever is easier, right adjusted. Shown here as position x51.

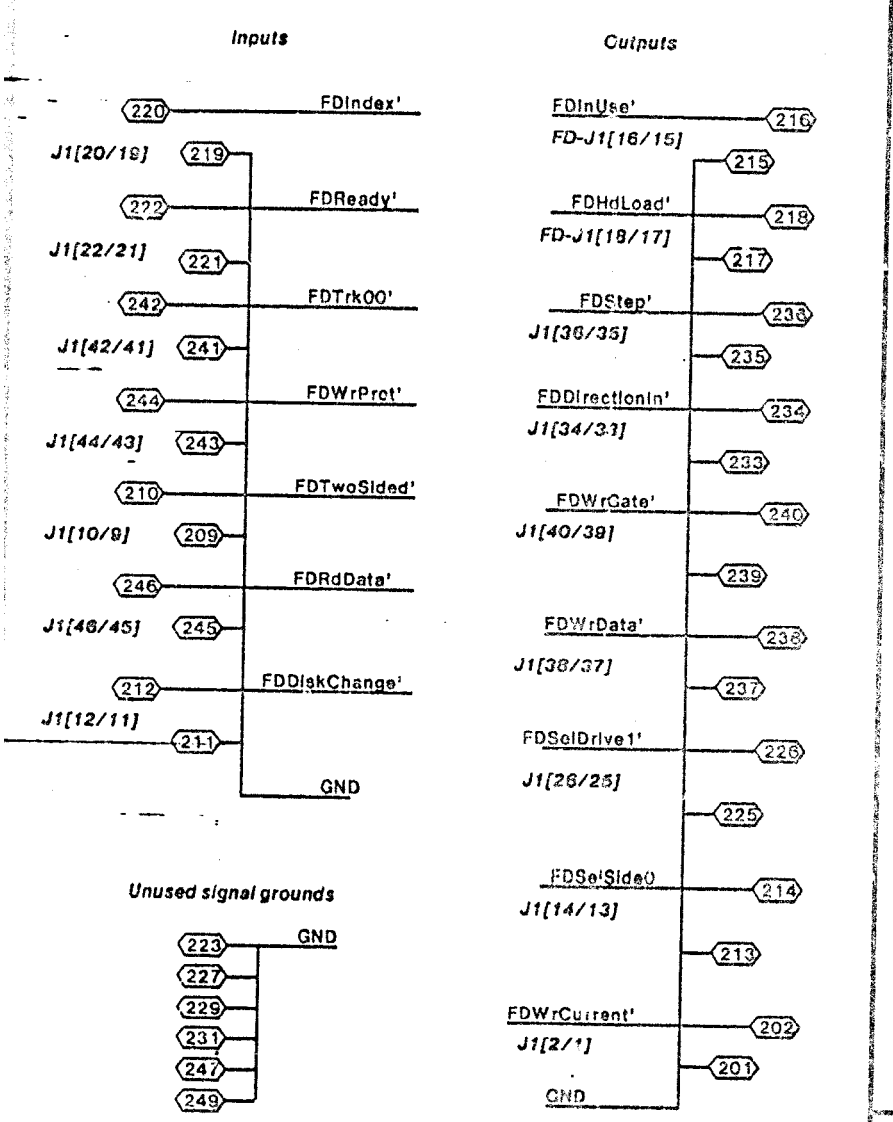
Examples: 4-switch DIP package: Grayhill 76RSB04 or 76SB04.
Xerox P/N 710W00004
2-switch DIP package: Grayhill 76RSB02 or 76SB02.

Pullups



I/O Processor PC discretes

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 15GP11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 27 OF	



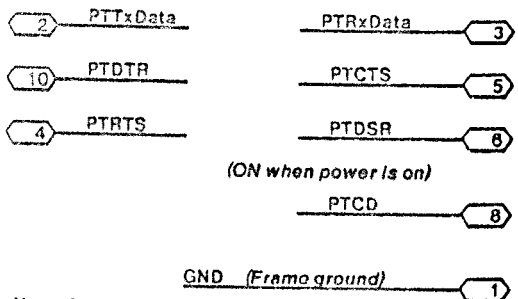
Floppy Disk Cable Connector

50-pin male connector

Xerox 713W14320

(Subtract 200 from above pin numbers to get physical pin number)

(Printer)



Note: Connector labels correspond to the Printer signals.

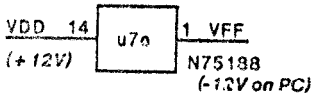
RS-232-C DCE port Cable Connector

10-pin male connector

Xerox 713W12220

(Above pin numbers are same as physical pin numbers)

75188 Voltage hookup

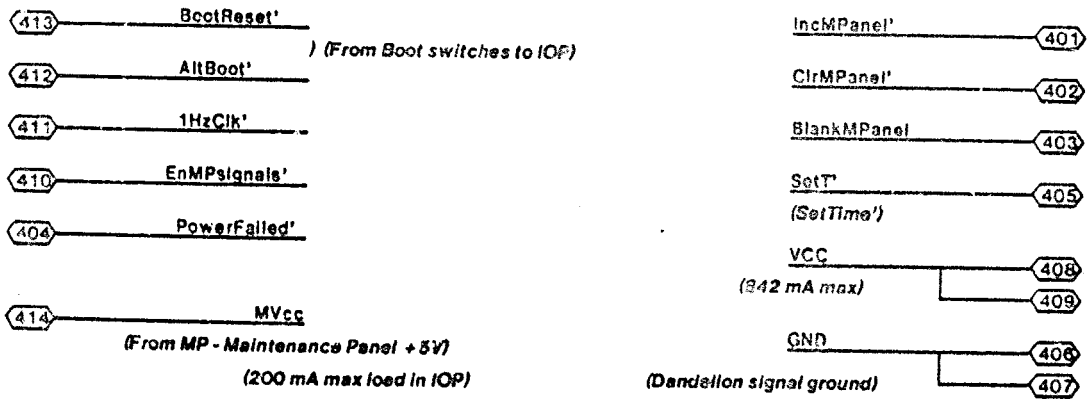


Maintenance Panel Cable Connector

14-pin male connector

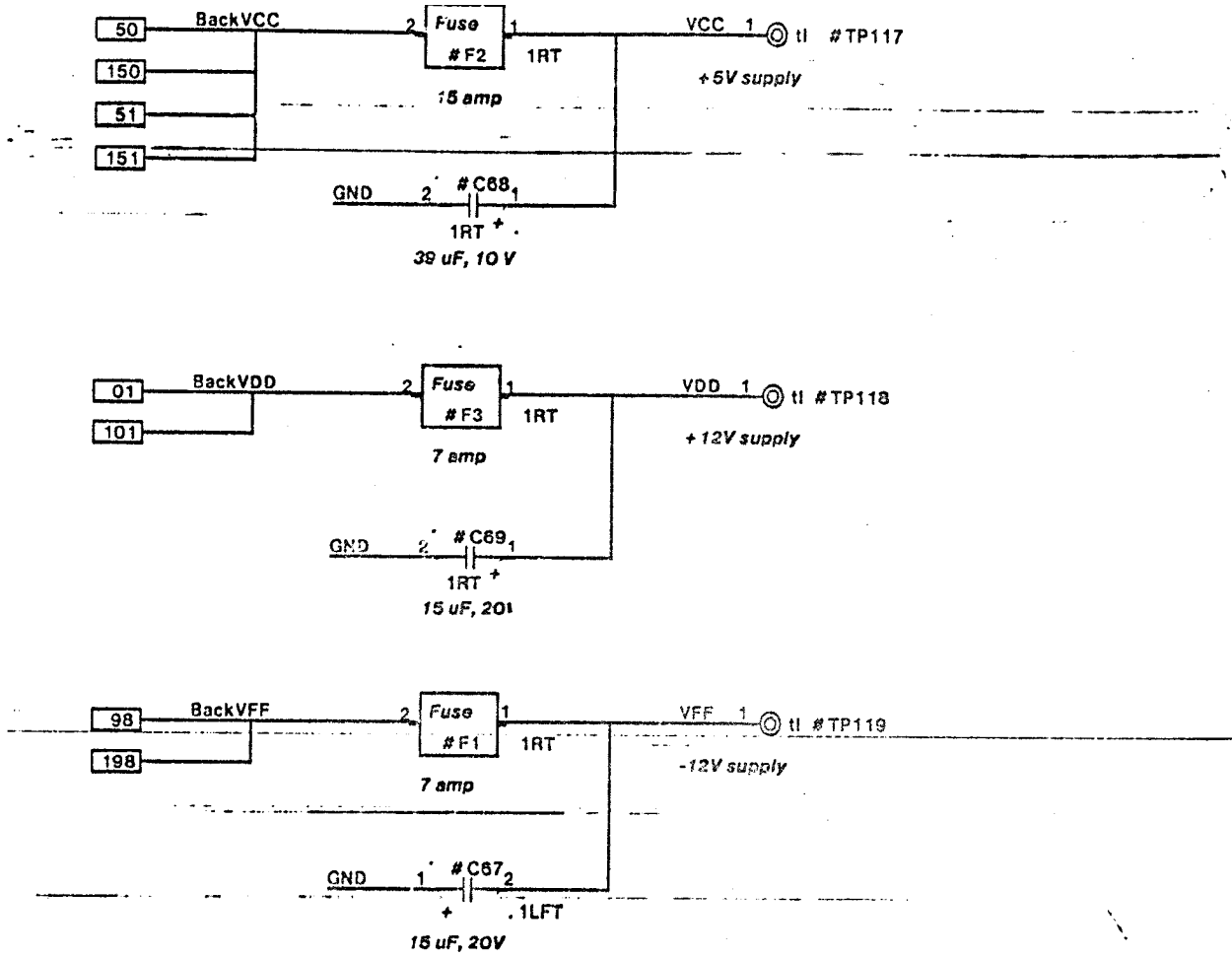
Xerox 713W13320

(Subtract 400 from pin numbers to get physical pin number)

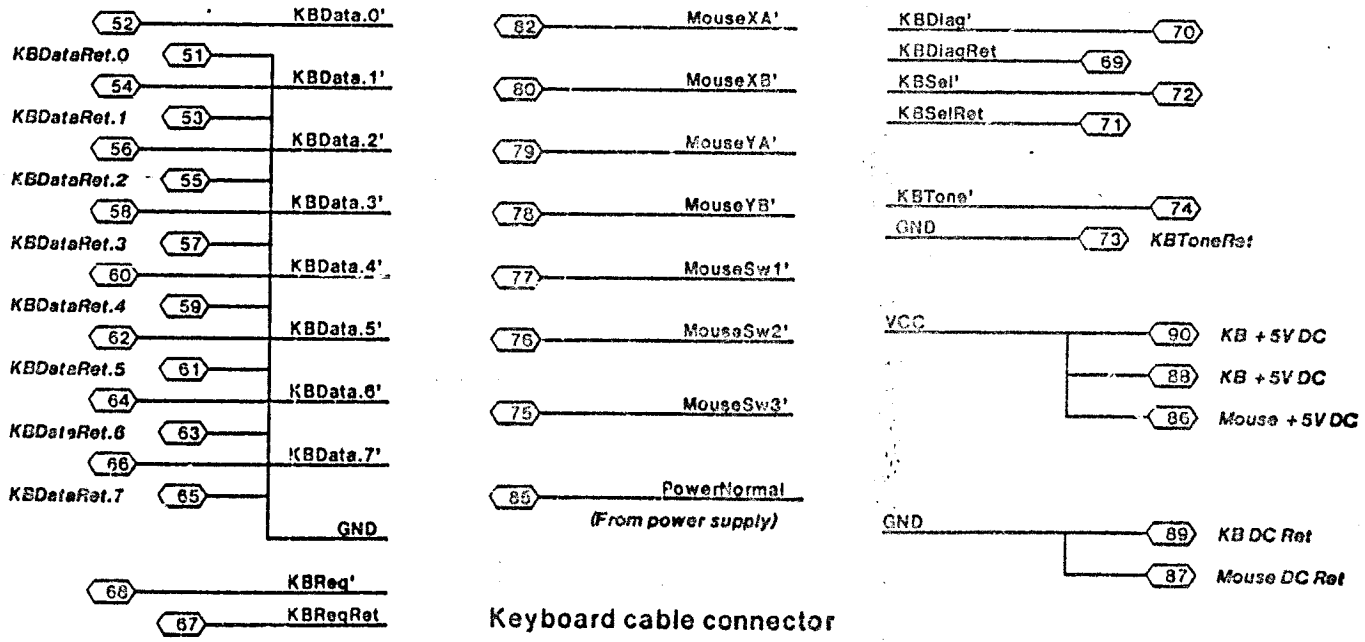


I/O Processor I/O Connectors - 2

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 28 OF	



CABLES



Keyboard cable connector

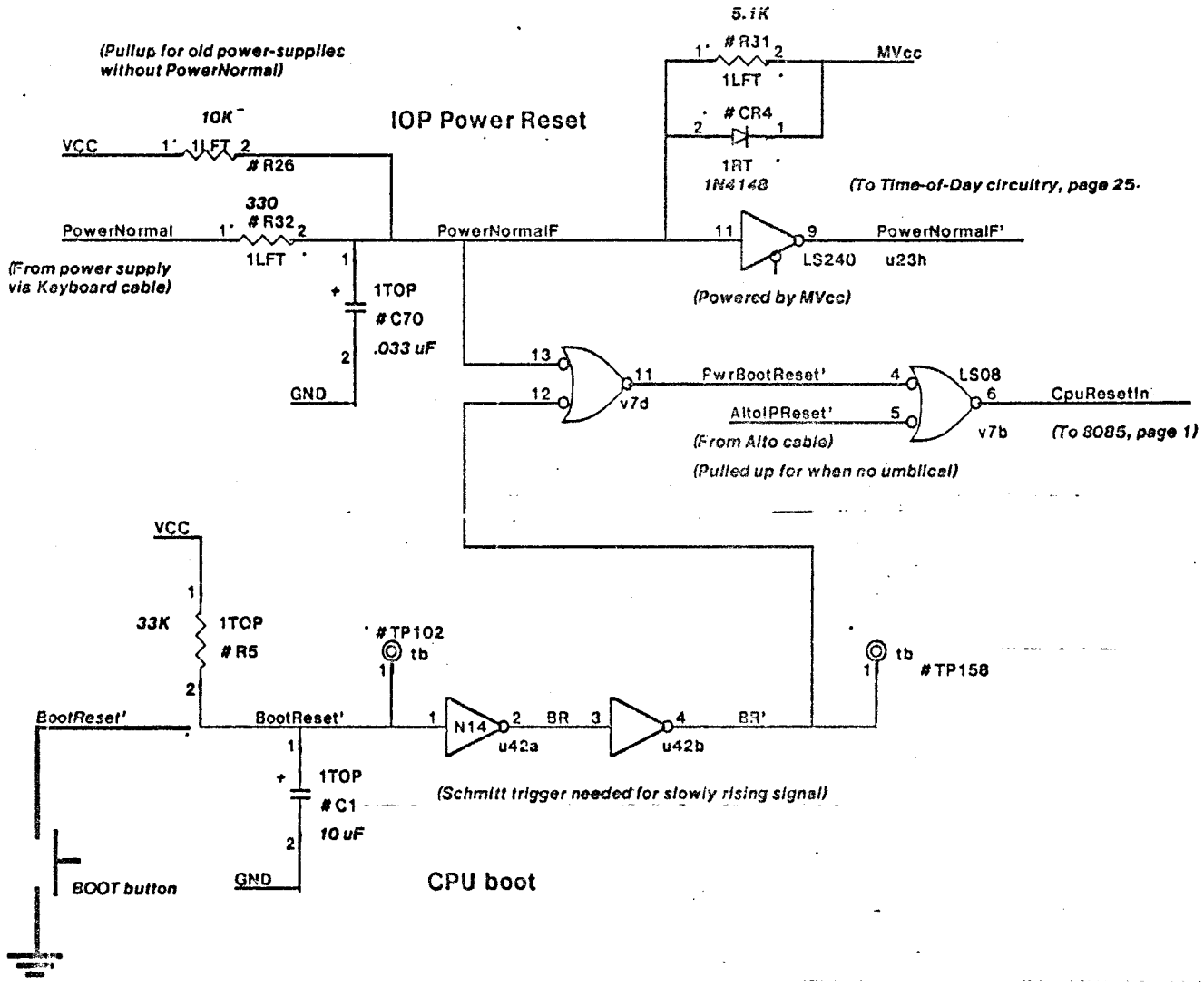
40-pin male connector

Xerox 713W12720

(Subtract 50 from above pin numbers to get physical pin number)

Power Supply and Fuses Keyboard cable connector

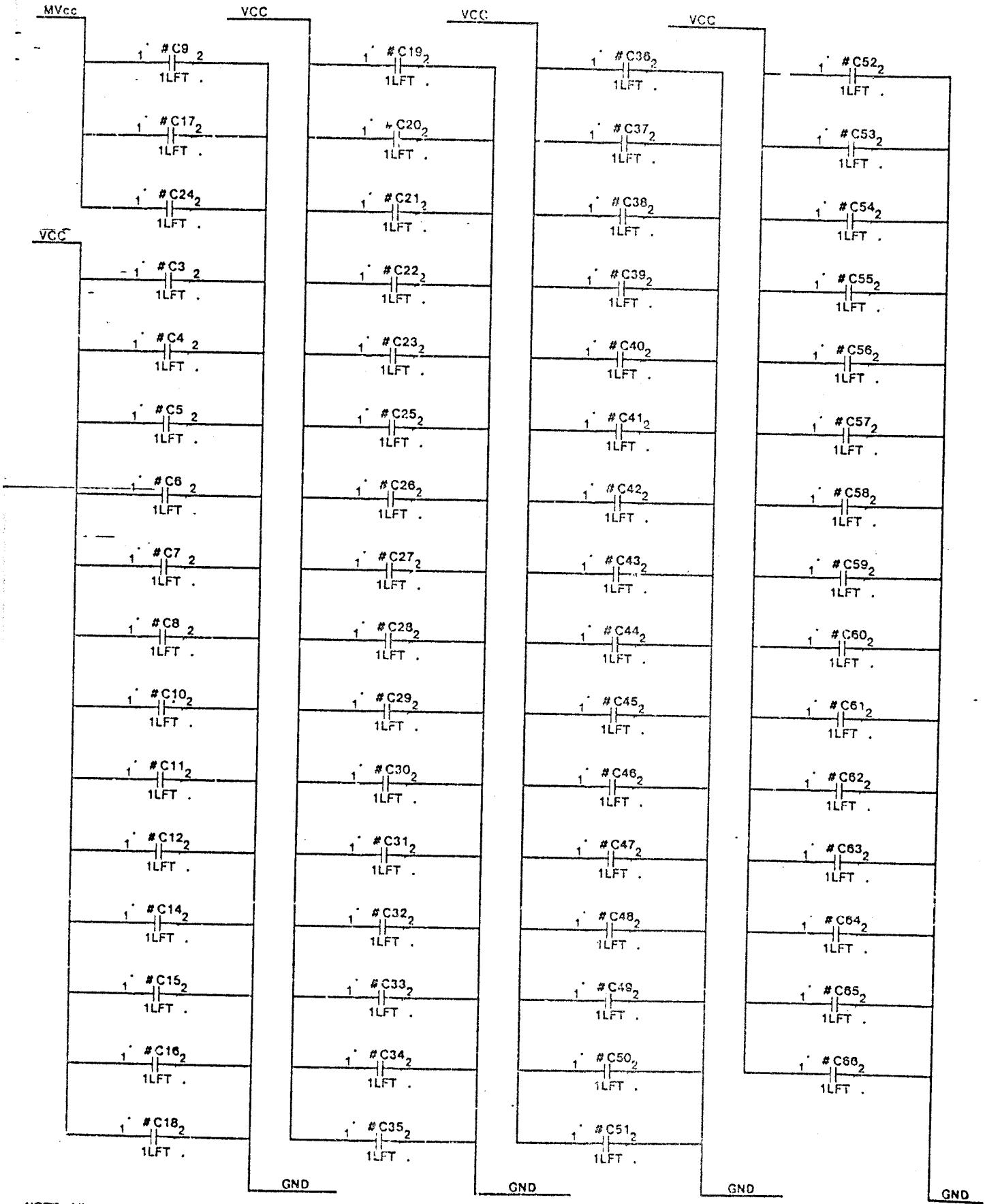
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 29 OF	B



The PowerNormal signal is produced in new power supplies. This signal monitors the +5 V power. When +5 V initially rises after power-up, PowerNormal is low for 50 msec after the +5 V power has stabilized. On power down, PowerNormal is rapidly made low to cause an IOPReset before the power disappears.

I/O Processor: IOP Boot and Reset circuitry

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 30 OF	B

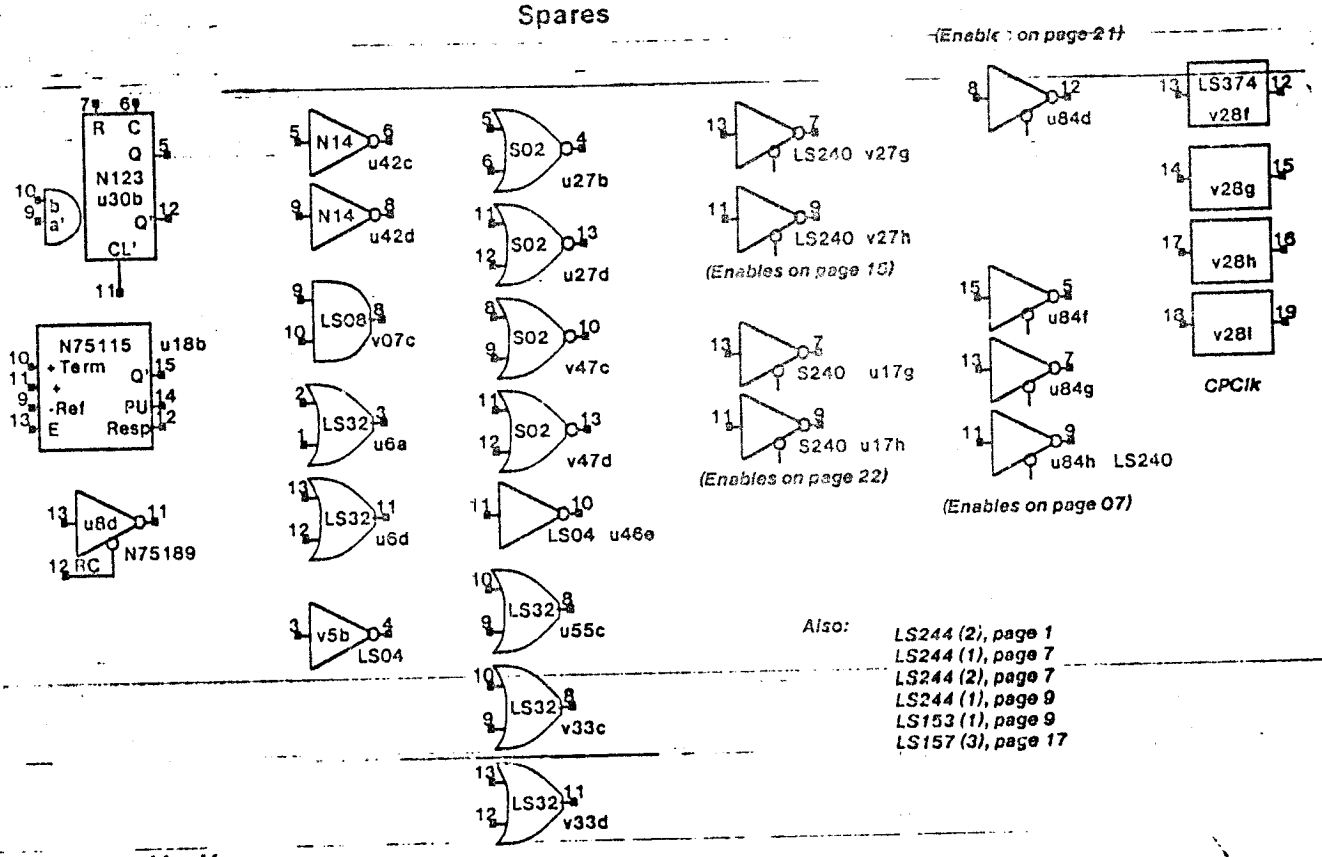


NOTE: All capacitors on this page are ceramic capacitors, 50V, 0.10 uf, part number 702WC5218

DISCRETE CAPACITORS

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. 8
	TITLE SCHEMATIC, IOP		SHEET 31 OF	

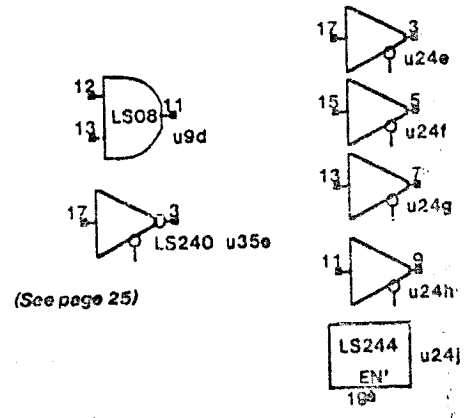
Spares



Also:

LS244 (2), page 1
LS244 (1), page 7
LS244 (2), page 7
LS244 (1), page 9
LS153 (1), page 9
LS157 (3), page 17

Powered by Vcc



Powered by MVcc

I/O Processor Spares

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11952	SHEET REV. B
	TITLE SCHEMATIC, IOP		SHEET 32 OF	

Comments:

1) *Designator notation notes: u1-99 = U1-99, v0-99 = U100-199, w0-99 = U200-299*
2) *The last item on lines below, preceeded by a semicolon (;), is the schematic page number on which the test point, connector or signal information originates.*
3) *Line with no page number was a continuation of the previous line.*

```
#TP048    .1i  DisDmaTest'       ;07
#TP1      .1i  AltoPPIIntA       ;21
#TP10     .1i  CPUAD.07          ;02
#TP100    .1i  UpMouseY          ;19
#TP101    .1i  EnKBBell          ;20
#TP102    .1i  BootReset'        ;30
#TP103    .1i  AltoIPReset'      ;21
#TP104    .1i  PrinterClk        ;22
#TP105    .1i  KBBC              ;22
#TP106    .1i  Time.24           ;25
#TP107    .1i  Time.16           ;25
#TP108    .1i  Time.08           ;25
#TP109    .1i  Time.00           ;25
#TP110    .1i  TimeData24        ;26
#TP111    .1i  TimeData16        ;26
#TP112    .1i  TimeData08        ;26
#TP113    .1i  TimeData'         ;26
#TP114    .1i  HdLdC             ;27
#TP115    .1i  HdLdR             ;27
#TP116    .1i  ppClk             ;27
#TP117    .1i  VCC               ;29
#TP118    .1i  VDD               ;29
#TP119    .1i  VFF               ;29
#TP12     .1i  IPReset           ;01
#TP120    .1i  SelHostAd'        ;05
#TP121    .1i  SelPROMBank0'     ;05
#TP122    .1i  SelPROMBank1'     ;05
#TP123    .1i  SelPROMBank2'     ;05
#TP124    .1i  SelPROMBank3'     ;05
#TP125    .1i  SelRAMBank0'      ;05
#TP126    .1i  SelRAMBank1'      ;05
#TP127    .1i  SelRAMBank2'      ;05
#TP128    .1i  SelRAMBank3'      ;05
#TP129    .1i  SelRAMBank4'      ;05
#TP13     .1i  CpuHoldAck        ;01
#TP130    .1i  SelRAMBank5'      ;05
#TP131    .1i  SelRAMBank6'      ;05
#TP132    .1i  SelRAMBank7'      ;05
#TP133    .1i  SelRAMBank8'      ;05
#TP134    .1i  SelRAMBank9'      ;05
#TP135    .1i  SelRAMBank10'     ;05
#TP136    .1i  SelRAMBank11'     ;05
#TP137    .1i  SelRAMBank12'     ;05
#TP138    .1i  SelRAMBank13'     ;05
#TP139    .1i  SelRAMBank14'     ;05
#TP14     .1i  CpuIO/M'          ;01
#TP140    .1i  SelRAMBank15'     ;05
#TP141    .1i  DmaWaitReq        ;06
#TP142    .1i  ClrFDClk'         ;10
#TP143    .1i  FDCDblDen'        ;12
#TP144    .1i  FDCRClk           ;12
#TP145    .1i  CurState.1        ;12
#TP146    .1i  CurState.2        ;12
#TP147    .1i  CurState.3        ;12
#TP148    .1i  CurState.4        ;12
#TP149    .1i  CurState.5        ;12
#TP15     .1i  CpuRD'            ;01
#TP150    .1i  CurState.6        ;12
#TP151    .1i  CPInWakeReqS      ;17
#TP152    .1i  CPOutWakeReqS     ;17
#TP153    .1i  IOPAttnSync'      ;17
#TP154    .1i  EnIOPRqAd'        ;17
#TP155    .1i  IPReady           ;21
#TP156    .1i  CpuReady          ;21
#TP157    .1i  FDId              ;27
#TP158    .1i  BR'               ;30
#TP159    .1i  FloppyIntReq      ;14
#TP16     .1i  CpuWR'            ;01
#TP160    .1i  Int.5             ;14
#TP162    .1i  CpuRST5           ;14
#TP163    .1i  DisDmaTest2'      ;07
#TP164    .1i  DisDmaTest3'      ;07
#TP17     .1i  CPUAddr.00        ;01
#TP18     .1i  CPUAddr.01        ;01
#TP19     .1i  CPUAddr.02        ;01
#TP2      .1i  CPAttn            ;15
#TP20     .1i  CPUAddr.03        ;01
#TP21     .1i  CPUAddr.04        ;01
#TP22     .1i  CPUAddr.05        ;01
#TP23     .1i  CPUAddr.06        ;01
#TP24     .1i  CPUAddr.07        ;01
#TP26     .1i  CpuHold           ;01
#TP27     .1i  DisCpuTest'       ;01
#TP28     .1i  PU1               ;01
#TP29     .1i  SelAltoPPI'       ;05
#TP3      .1i  CPUAD.00          ;02
#TP30     .1i  SelPrinter'       ;05
#TP31     .1i  SelTimer'         ;05
#TP32     .1i  ReadKBData'       ;05
#TP33     .1i  ClrMouseXY'       ;05
#TP34     .1i  IPAData.0         ;06
#TP35     .1i  IPAData.1         ;06
#TP36     .1i  IPAData.2         ;06
#TP37     .1i  IPAData.3         ;06
#TP38     .1i  IPAData.4         ;06
#TP39     .1i  IPAData.5         ;06
#TP4      .1i  CPUAD.01          ;02
#TP40     .1i  IPAData.6         ;06
#TP41     .1i  IPAData.7         ;06
#TP42     .1i  EnIPData          ;06
#TP43     .1i  EnIPAData         ;06
#TP44     .1i  EnIPAData         ;06
```

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11952	SHEET REV.
	TITLE SCHEMATIC, IOP	A4	SHEET 33 OF	B