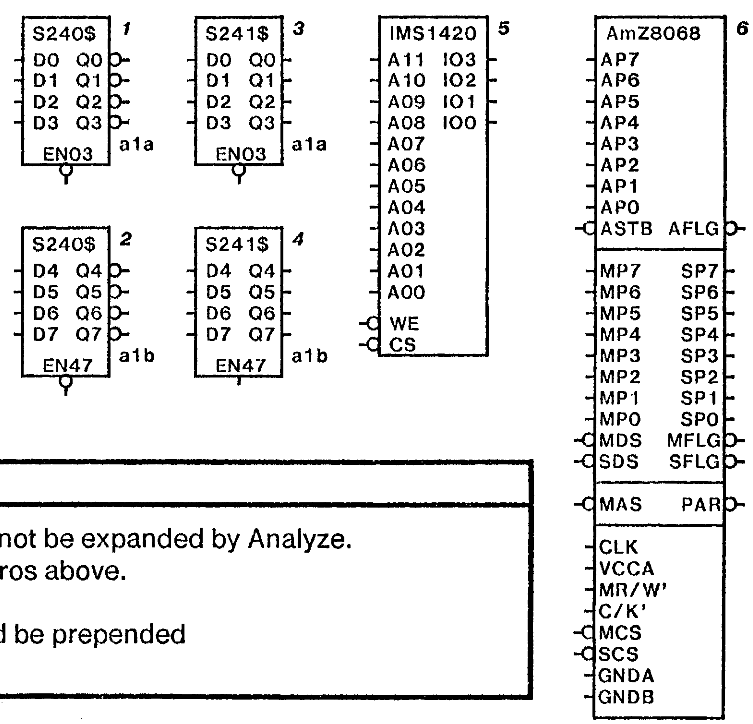
Prom Name	Rev	Part No.	Location	Page	Comments	
SwitchProm	R	F93427	i14	14	New Rev for 16K Control Store CP	256 x 4
KernPC16Prom	B	F93427	h14	15	Standard	256 x 4
CSIntProm	D	F93453	e20	22	Standard	1K x 4
StackVirtProm	I	F93427	h24	15	Standard	256 x 4
ScheduleProm	D	F93453	h18	14	Standard	1K x 4
ErrorProm	E	F93453	g14	15	Standard	1K x 4
IBProm-PC.0	G	F93453	i17	05	Standard	1K x 4
IBProm-PC.4	G	F93453	h17	05	Standard	1K x 4
DesMpProm.0	B	F93427	a16	33	Added to control DES logic	256 x 4
DesMpProm.4	B	F93427	b16	33	Added to control DES logic	256 x 4
DesSpProm	A	F93427	b15	33	Added to control DES logic	256 x 4

Prom files are stored on [Indigo]<Dandelion>CPE>Proms>*
Bringover /a [Indigo]<Dandelion>CPE>DfFiles>Proms.df *to fetch all files, sources, tools, etc.*

Labels:

Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A
Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A
Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A
Switch i14 Rev-R	KernPC16 h14 Rev-B	CSInt e20 Rev-D	StackVirt h24 Rev-I	Schedule h18 Rev-D	Error g14 Rev-E	IB-PC.0 i17 Rev-G	IB-PC.4 h17 Rev-G	DesMp.0 a16 Rev-B	DesMp.4 b16 Rev-B	DesSp b15 Rev-A

Font 4 Macros

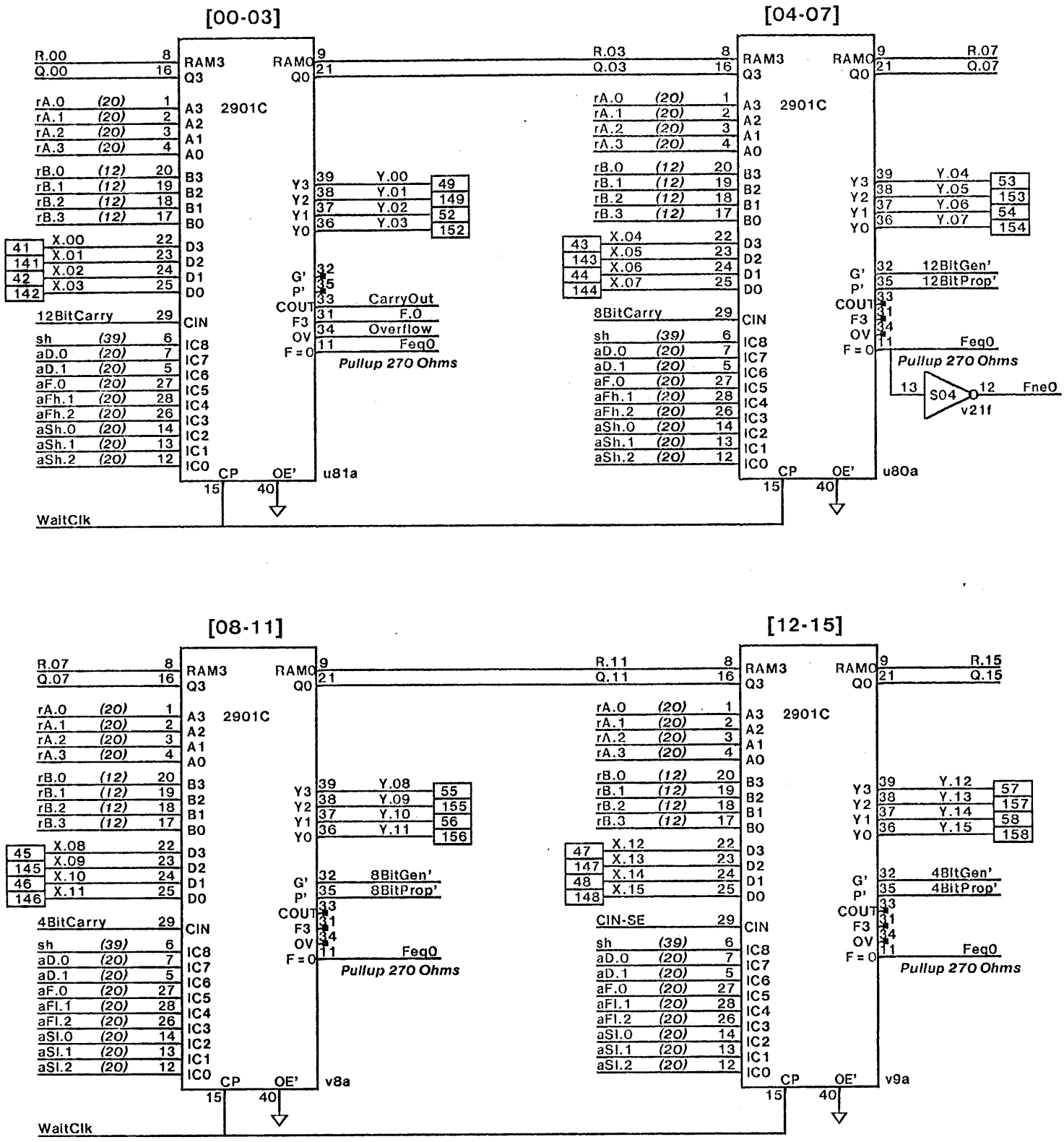


Important Notes:

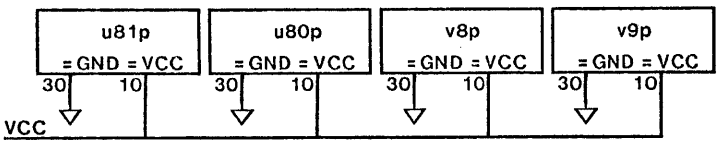
Only macros 0-9 are valid component names and will not be expanded by Analyze.
Some of these drawings contain instances of the macros above.
Those that do have a warning on them, see below left.
There is a corresponding CPEDict.analyze that should be prepended to the dictionary chain.

Warning: This drawing contains font 4 macros!

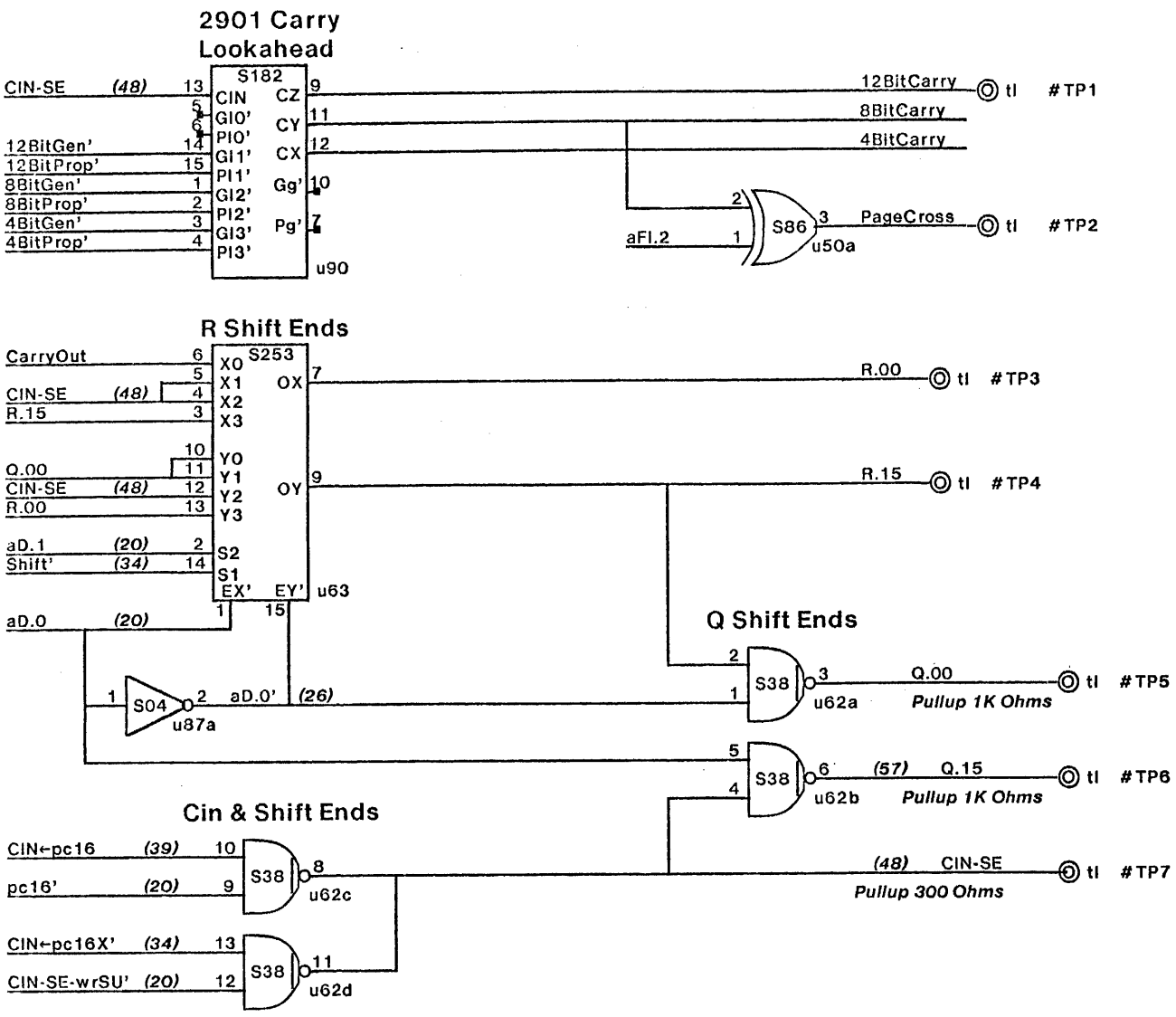
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS TITLE SCHEMATIC, CPE-FP *Reference*	DWG SIZE A4	DWG NO. 156P12560 SHEET 02 OF	SHEET REV. A



2901C Timing			As of 10/05/82		
Setup	sh,,aD	10			
Setup	aF	30			
Setup	aS	30			
rA	to G,P	37	rA	to Y	40
D	to G,P	30	D	to Y	30
			Cn	to Y	22
rA	to Cout	40	aS	to Y	35
D	to Cout	30	aF	to Y	35
Cin	to Cout	20	aD	to Y	25



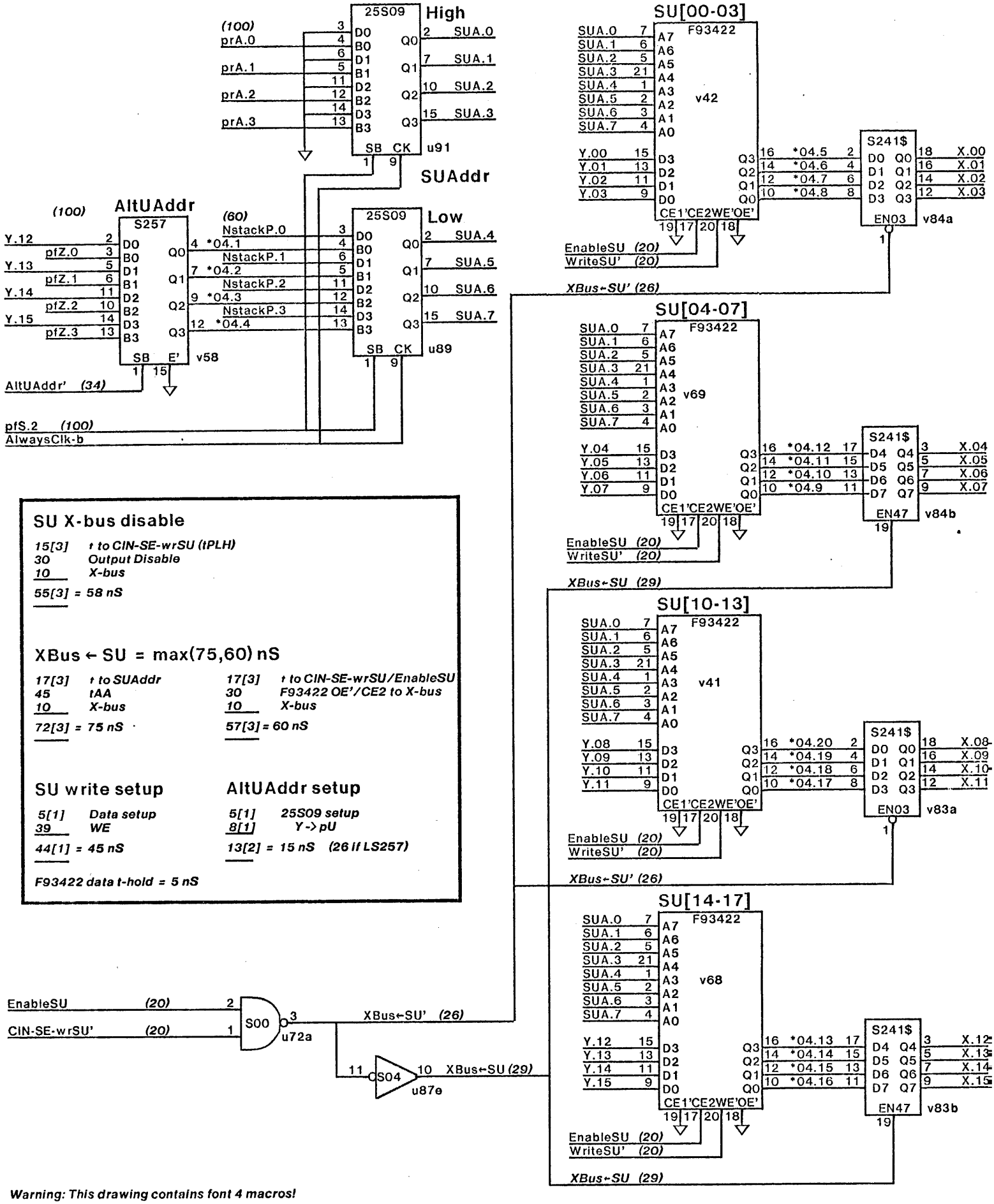
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC, CPE-FP	A4	SHEET 03 OF	A



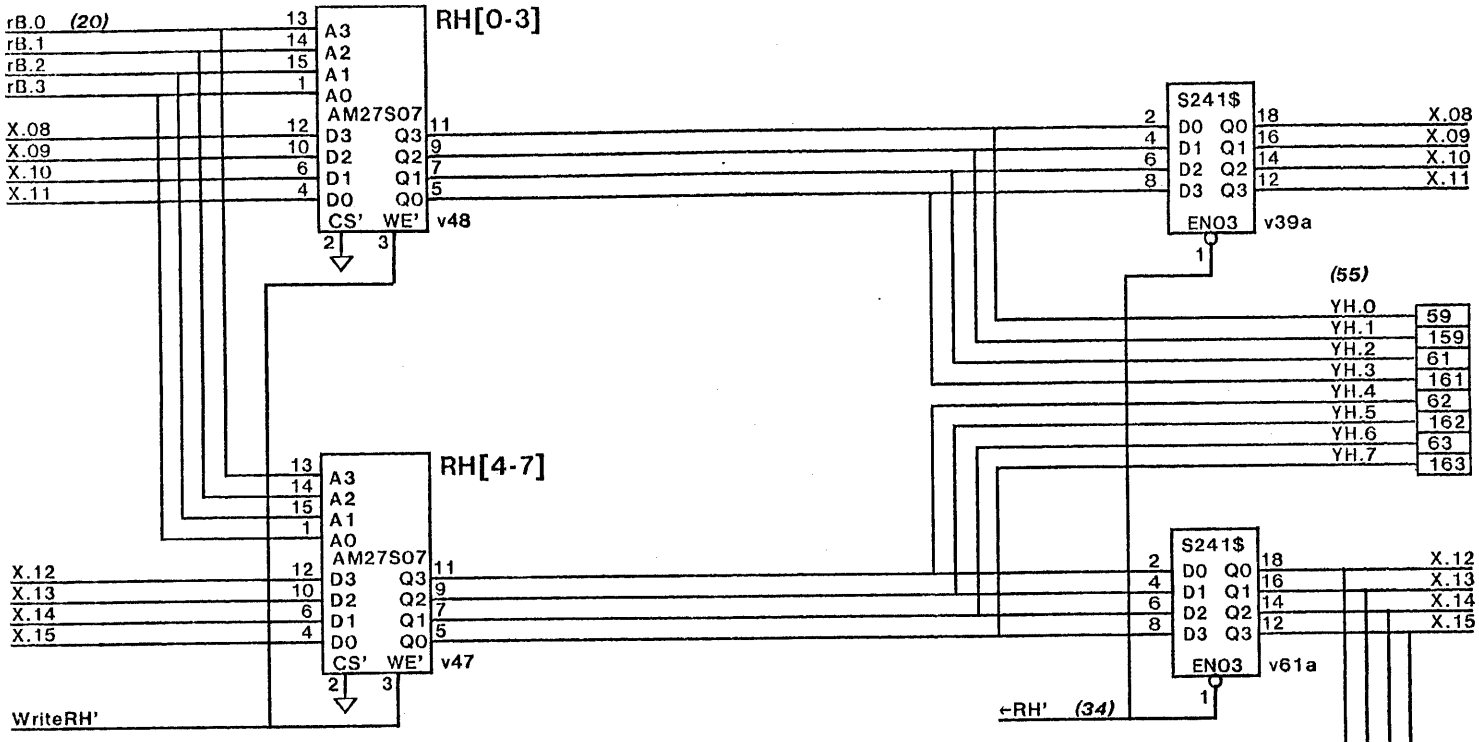
aD.1	Shift'	Shift configuration
0	0	Cout → R ~ Q ← ~Cin
0	1	Cin → R ~ Q ← ~Cin
1	0	Cin → R ← Cin
1	1	R

aD.0 = 0 implies right shift

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 04 OF	

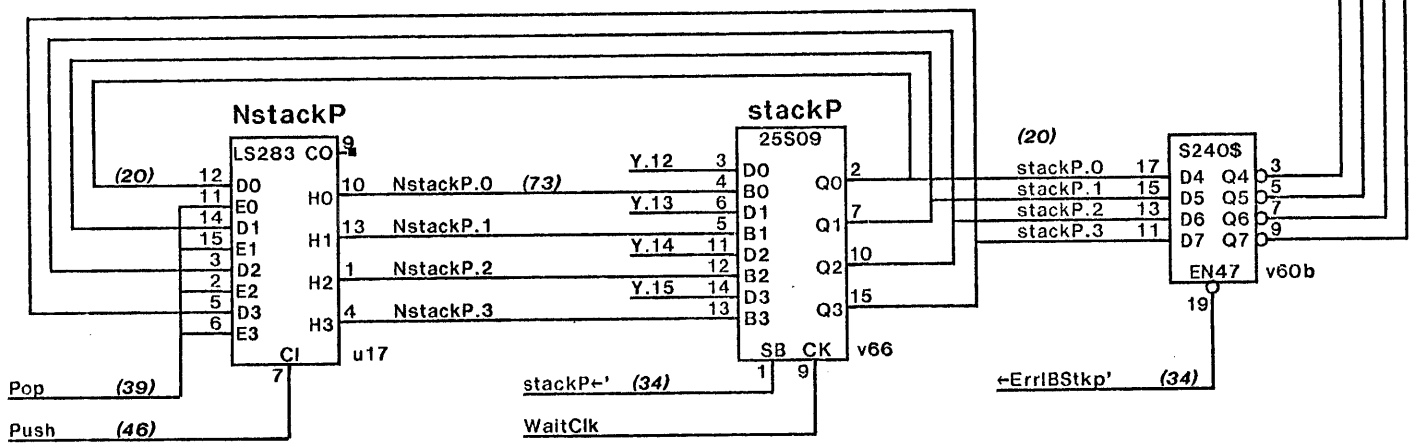


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC, CPE-FP	A4	SHEET 05 OF	A



XBus ← RH = max(74,59) nS

17[3]	*t to rB'*	*34*	*t to ←RH'*
35	*S189 tAA (wr recovery = 35 nS)*	*15*	*S241 EN' to X-bus*
9	*YH to X*	*10*	*X-bus*
10	*X-bus*	*59 nS*	
71[3] = 74 nS			



Push Timing

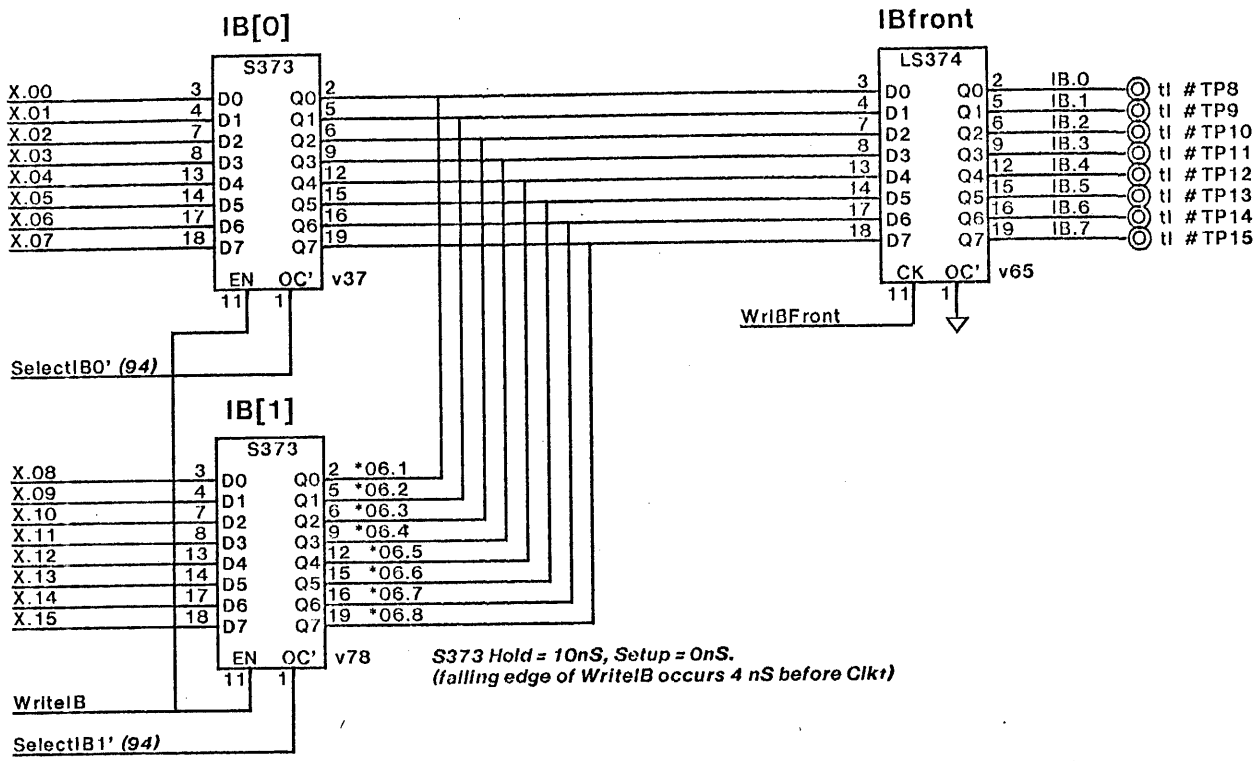
46	*t to Push*
24[3]	*Push to NstackP*
5[1]	*25S09 setup*
75[4] = 79 nS	

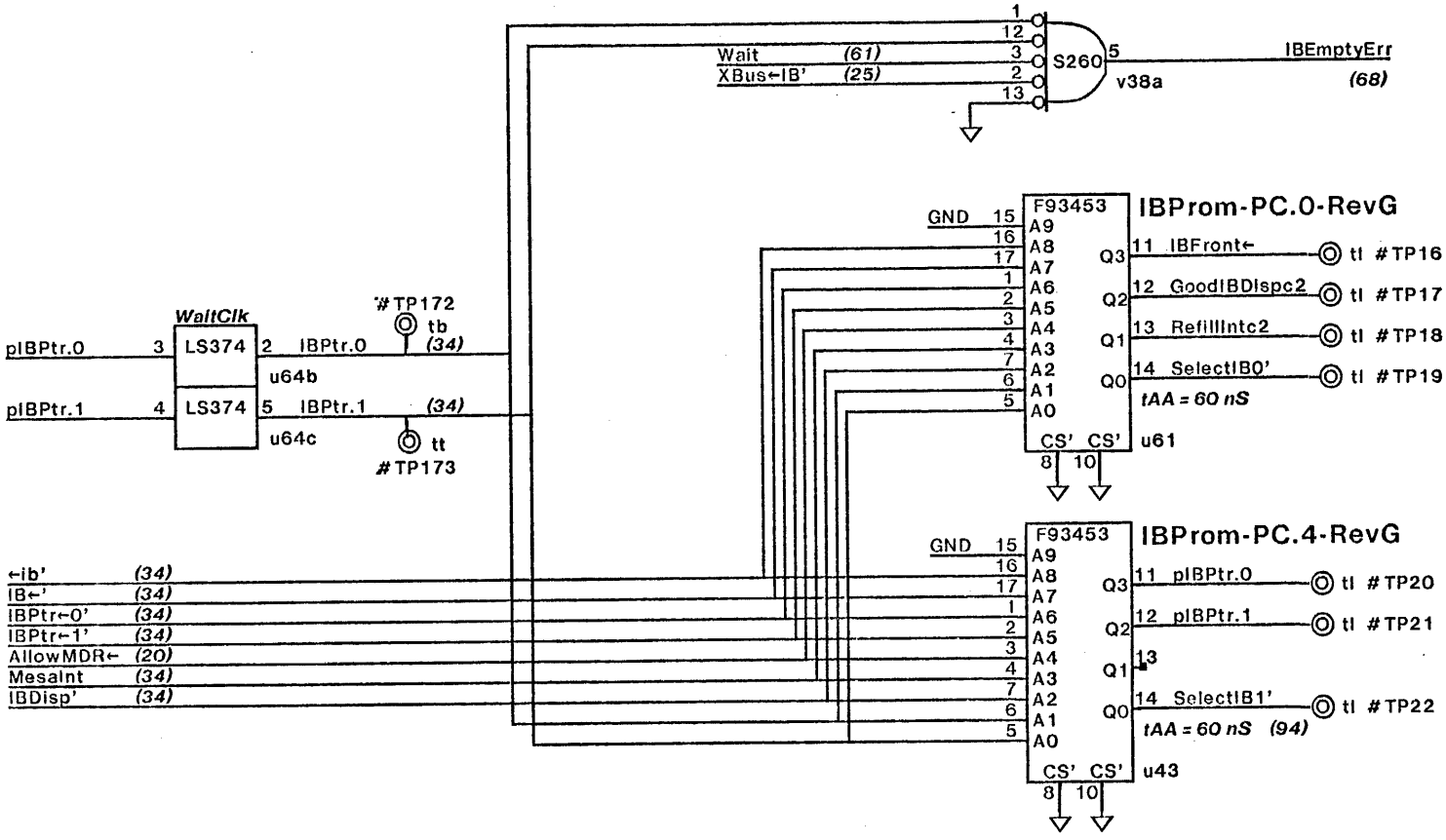
XBus ← stackP = max(59, 38) nS

17[3]	*t to stackP*	*34*	*t to ←ErrIntstackP'*
7	*S240 data to X-bus*	*15*	*S240 EN' to X-bus*
10	*X-bus*	*10*	*X-bus*
34[3] = 38 nS		*59 nS*	

Warning: This drawing contains font 4 macros!

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 06 OF	





Timing for HM7649 IBProm (Old Proms -- not 2nd sourced)

IBFront ← Xbus = (x + 37, x + 36) nS

x	Xbus to IB
43	WriteIB rises 43 nS before end of cycle
-6	Difference between S373 "EN to Q" and "Data to Q" = 18[2] - 13[1] = 6 nS. Data can arrive 6 nS after WriteIB goes high.
x+37 nS	

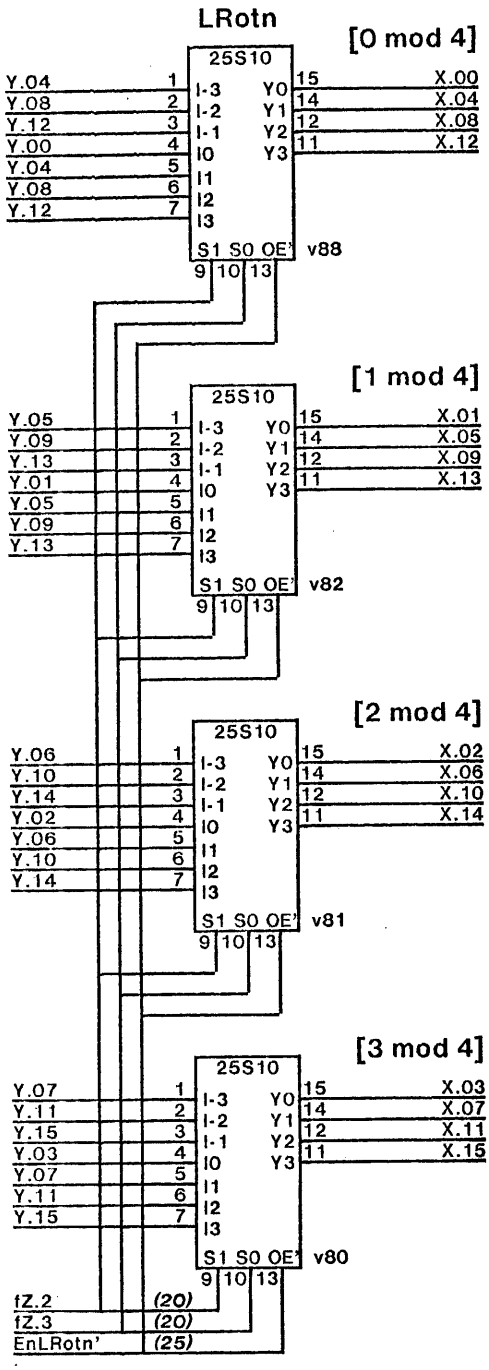
x	Xbus to IB
13[1]	S373 Data to NB
20[2]	LS374 setup
x+36 nS	

IBfront←IB[1]

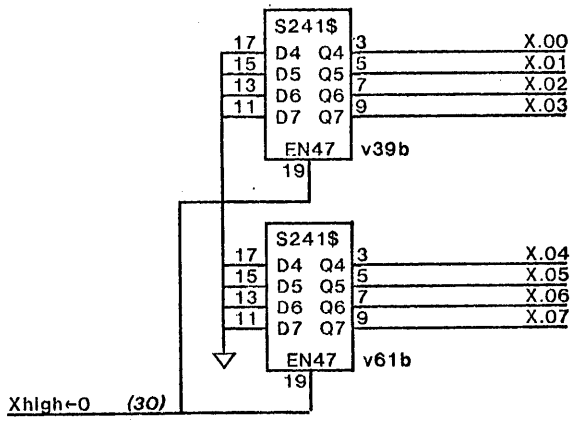
94	WriteIB rises
18[2]	S373 EN to NB
20[2]	LS374 setup
132[4] = 136 nS	

34	t to IBPtr←1'
60	tAA
18[2]	SelectIB1' to NB
20[2]	LS374 setup
132[4] = 136 nS	

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 07 OF	



fZ.2	fZ.3	Rotate
0	0	Left 0
0	1	Left 12
1	0	Left 8
1	1	Left 4



Zero disable X-bus

30	t to Xhigh←0
15	S241 EN to X-bus
10	X-bus
55 nS	

Xbus[0-7] ← 0

30	t to Xhigh←0
15	S241 OE
10	X-bus
55 nS	

Xbus ← Y LRotn = max(y + 22, 56, 50) nS

y	t to Y bus
12	25S10 data in to out
10	X-bus
y + 22 nS	

25	t to EnLRotn'
21	25S10 OE
10	X-bus
56 nS	

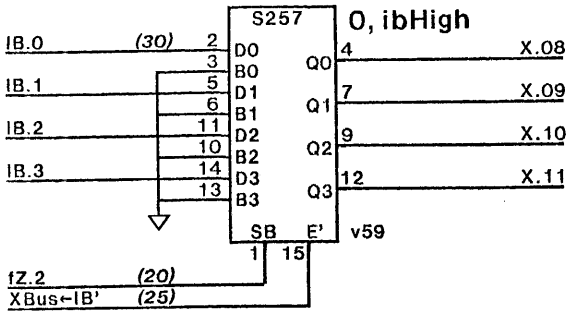
20	t to fZ.2
20	25S10 Select to X-bus
10	X-bus
50 nS	

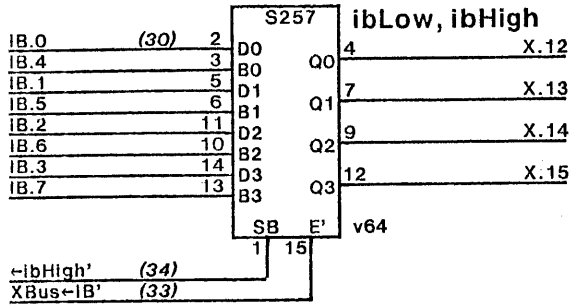
LRotn disable X-bus

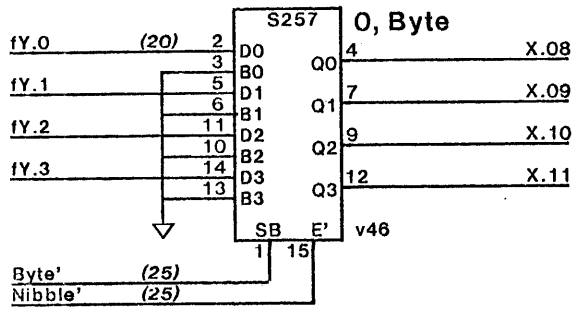
25	t to EnLRotn'
15	25S10 OE' to X-bus
10	X-bus
50 nS	

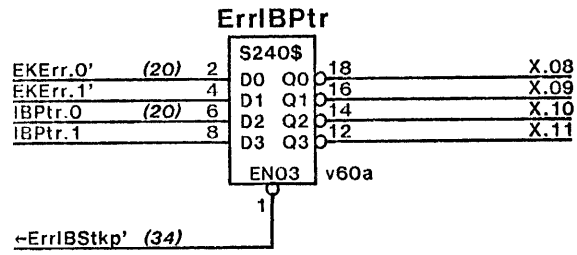
Warning: This drawing contains font 4 macros!

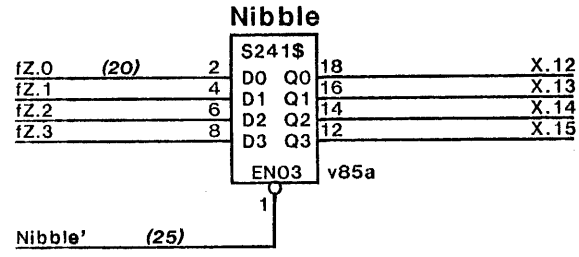
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 08 OF	











IB disable X-bus

25	t to XBus←IB'
14	S257 E' to X-bus
10	X-bus
49 nS	

Byte disable X-bus

25	t to Nibble'
14	S257 E' to X-bus
10	X-bus
49 nS	

Nibble disable X-bus

25	t to Nibble'
15	S241 EN' to X-bus
10	X-bus
50 nS	

Xbus←IB = max(56,56,59) nS

34[4]	t to IB
8	S257 data to Xbus
10	X-bus
52[4] = 56 nS	

25	t to Xbus←IB'
21	S257 E' to Xbus
10	X-bus
56 nS	

34	t to←ibHigh'
15	S257 SB to Xbus
10	X-bus
59 nS	

Xbus ← Nibble = max(39, 50) nS

20	t to fZ
9	S241 data to X-bus
10	X-bus
39 nS	

25	t to Nibble'
15	S241 EN' to X-bus
10	X-bus
50 nS	

Xbus ← Byte = max(38, 56,50) nS

20	t to fY
8	S257 data to X-bus
10	X-bus
38 nS	

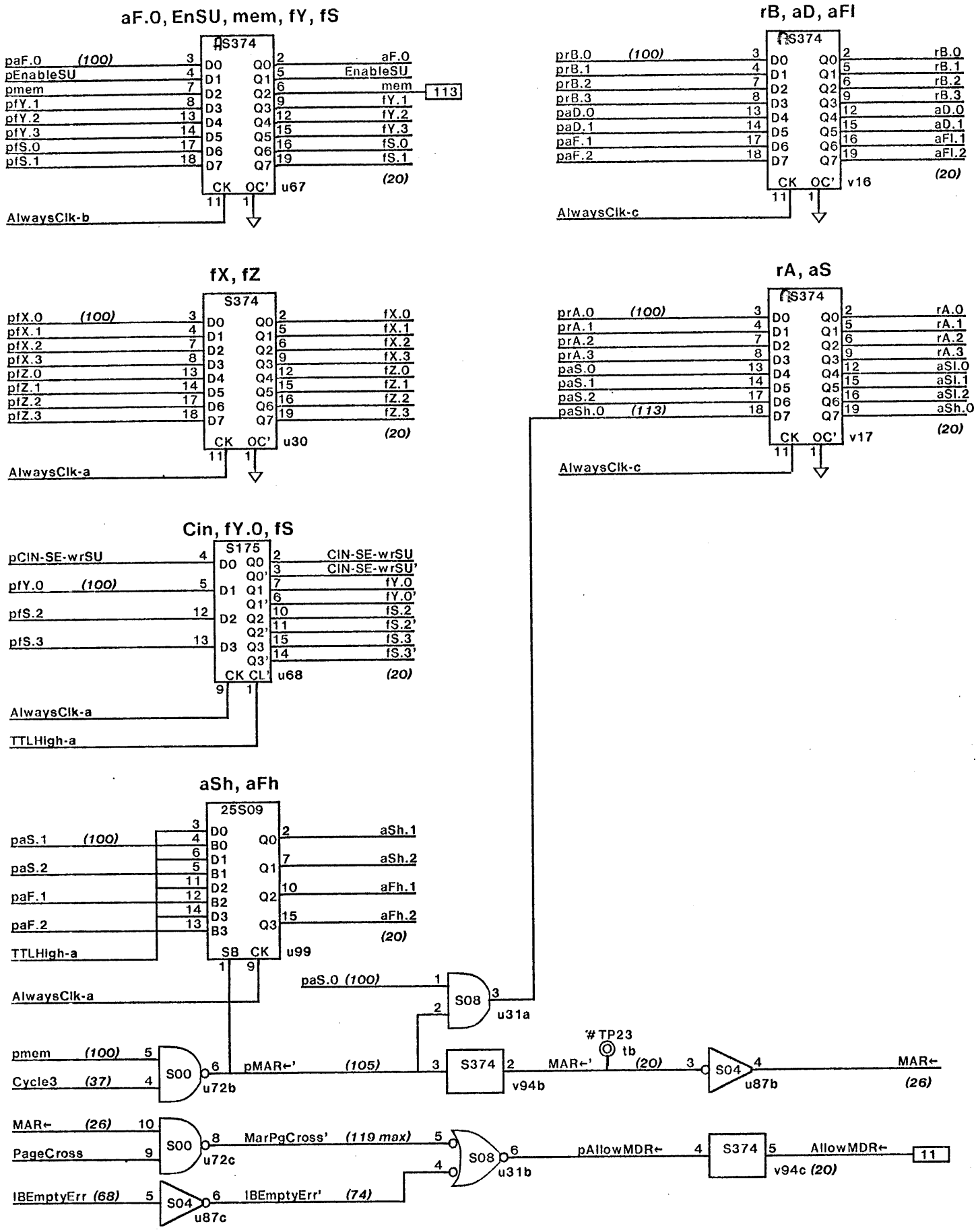
25	t to Nibble'
21	S257 E' to X-bus
10	X-bus
56 nS	

25	t to Byte'
15	S257 SB to Xbus
10	X-bus
50 nS	

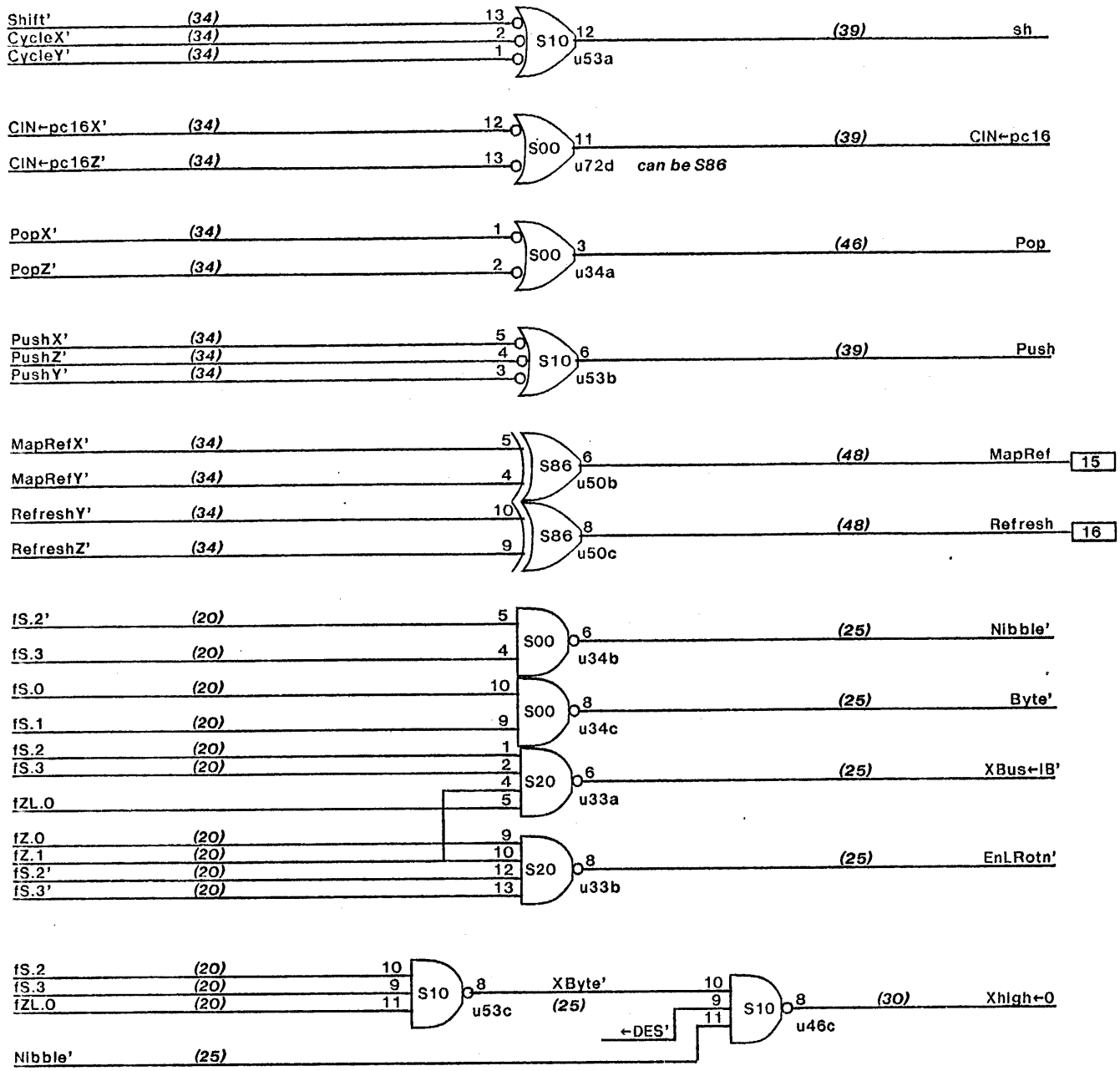
See stackP timings for ErrIBPtr

Warning: This drawing contains font 4 macros!

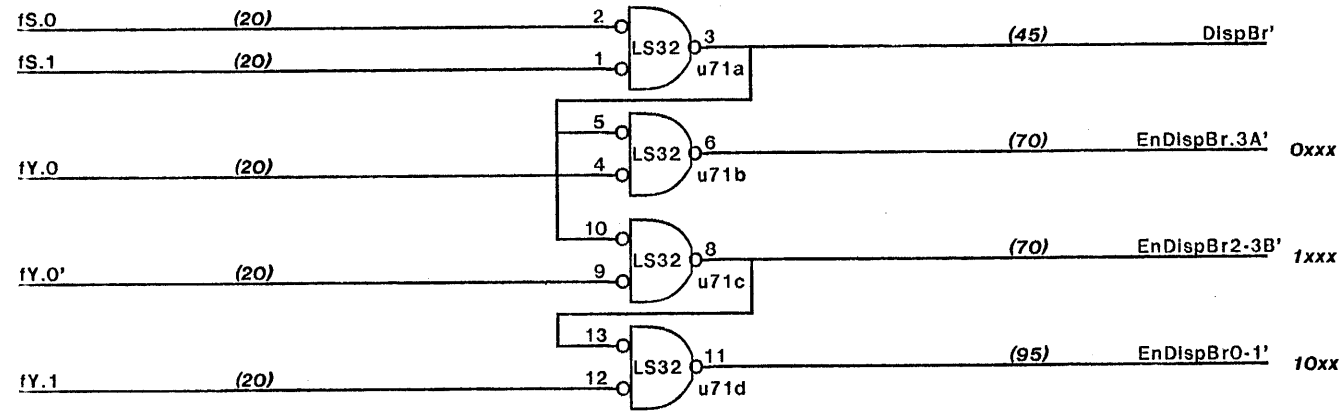
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 09 OF	



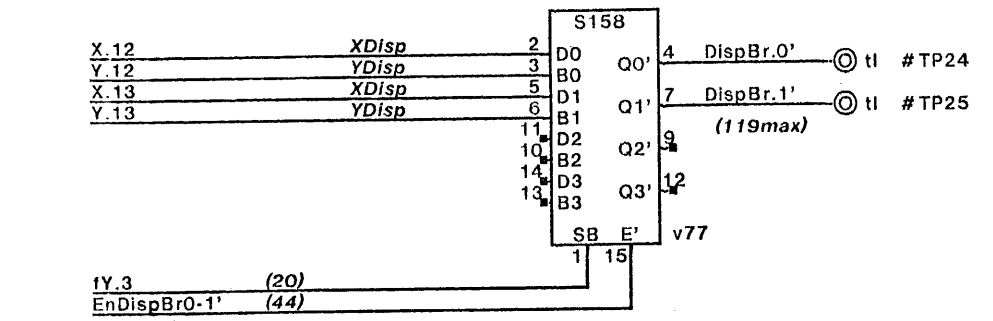
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC, CPE-FP	A4	SHEET 10 OF	A

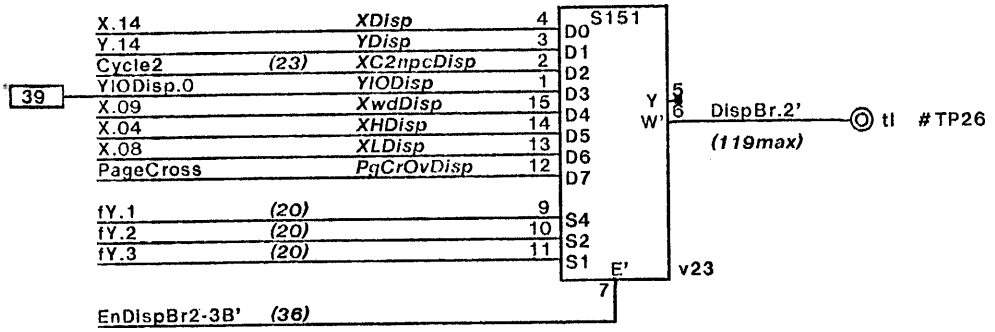


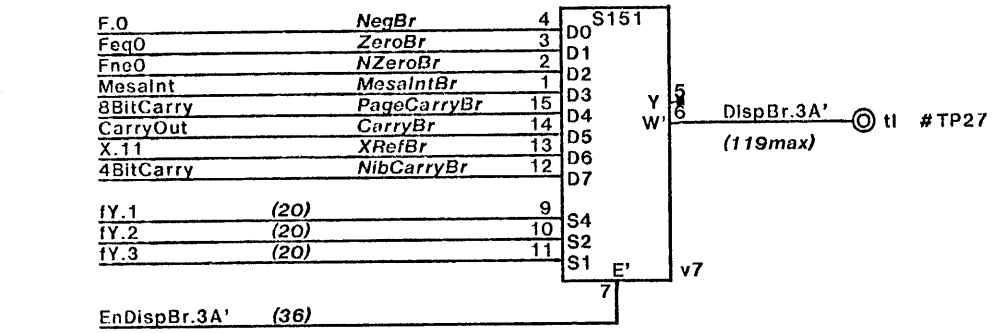
EnDispBr

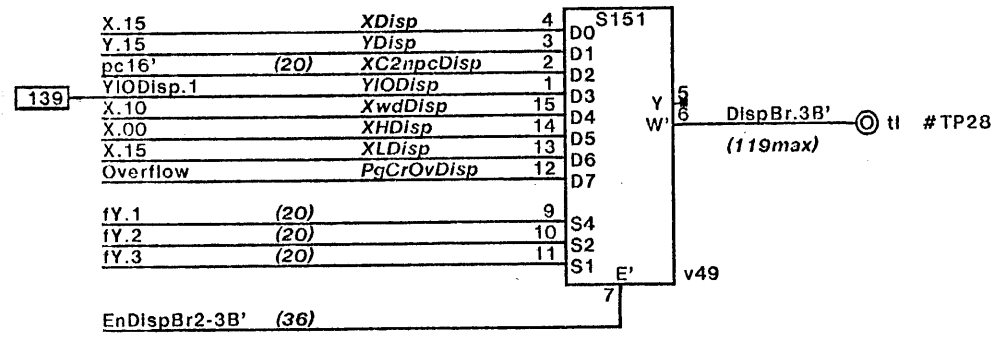


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 12 OF	









DispBr[0-1] = max(c + 32,69,133)

20	t to fY
24[3]	S151 select to DispBr
18	DispBr' setup

64[3] = 69

95	t to EnDispBr0-1'
18[2]	S151 E' to DispBr
18	DispBr' setup

131[2] = 133 nS

c	condition source
12[2]	S151 data to DispBr
18	DispBr' setup

c + 30[2] = c + 32

DispBr Setup

5	S00 in to pTC
6[1]	S64 in to pNIA
5[1]	25S09/S374 setup

18 nS

DispBr[2-3] = max(c + 26,55,103)

20	t to fY
15[2]	S151 select to DispBr
18	DispBr' setup

51[4] = 55 nS

70	t to EnDispBr.3A'
13[2]	S151 E' to DispBr
18	DispBr' setup

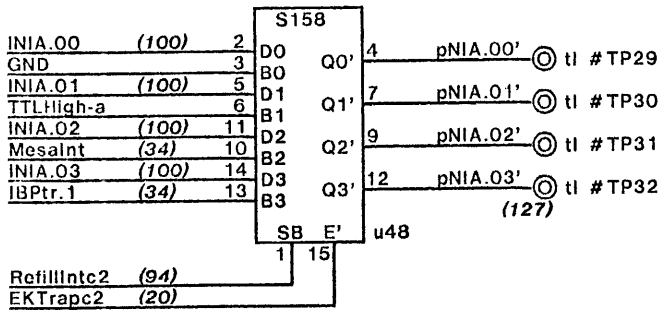
101[2] = 103 nS

c	condition source
7[1]	S151 data to DispBr
18	DispBr' setup

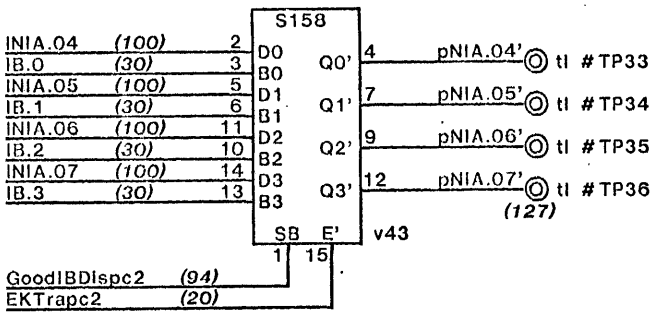
c + 23[3] = c + 26 nS

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC CPE-FP		SHEET 13 OF	

pNIA[0-3]



pNIA[4-7]

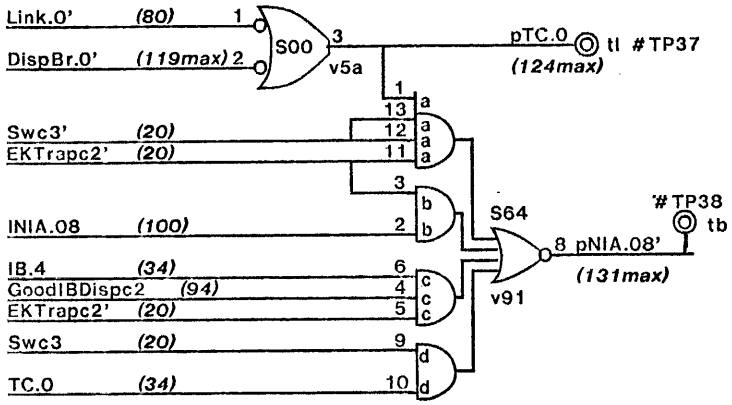


pNIA[0-7] = max(127, 120, 46) nS

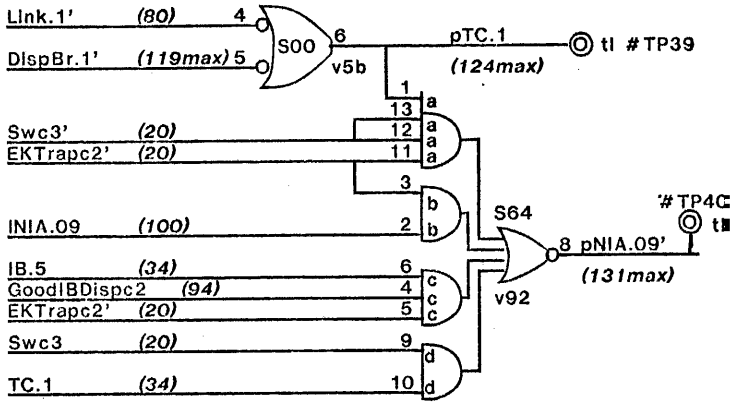
94	t to RefillIntc2	100	t to INIA	20	t to EKErrc2
24[3]	LS158 SB to pNIA'	12[2]	LS158 data to pNIA'	18[2]	LS158 E' to pNIA'
5[1]	25S09/S374 setup	5[1]	25S09/S374 setup	5[1]	25S09/S374 setup
123[4] = 127 nS		117[3] = 120 nS		43[3] = 46nS	

(See page 11 for pNIA[8-11] timing)

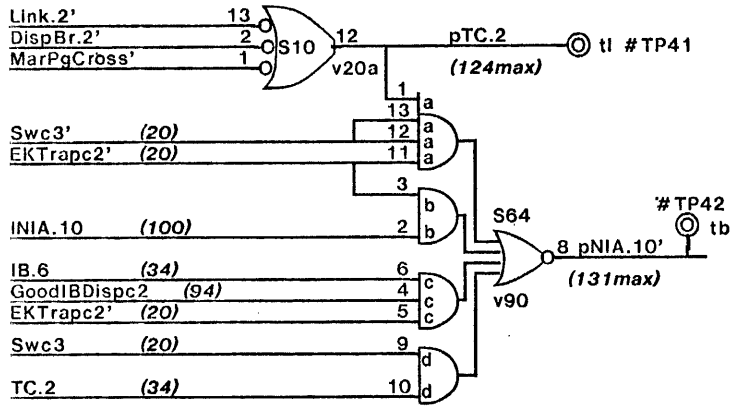
pNIA.8



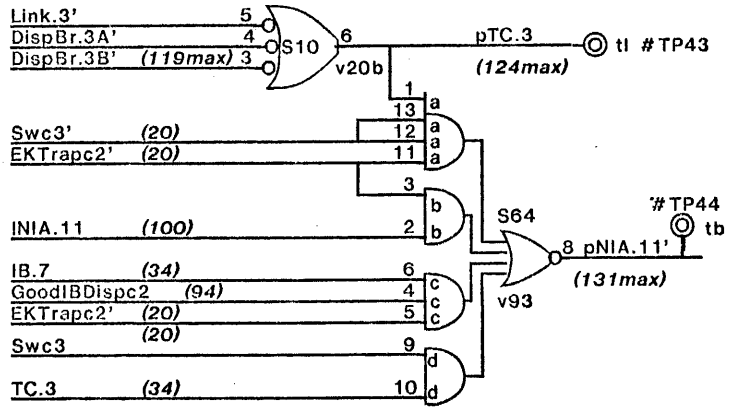
pNIA.9



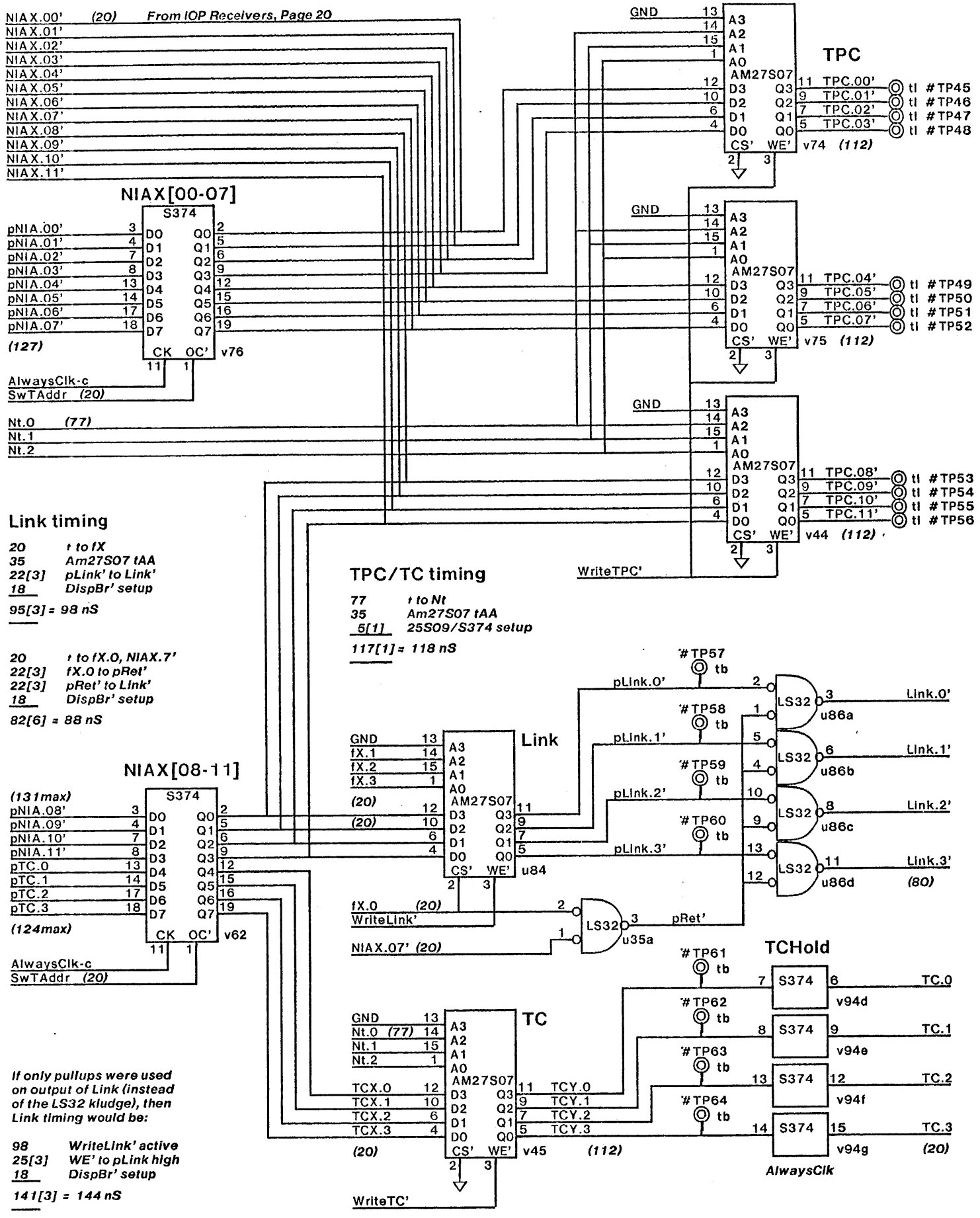
pNIA.10



pNIA.11

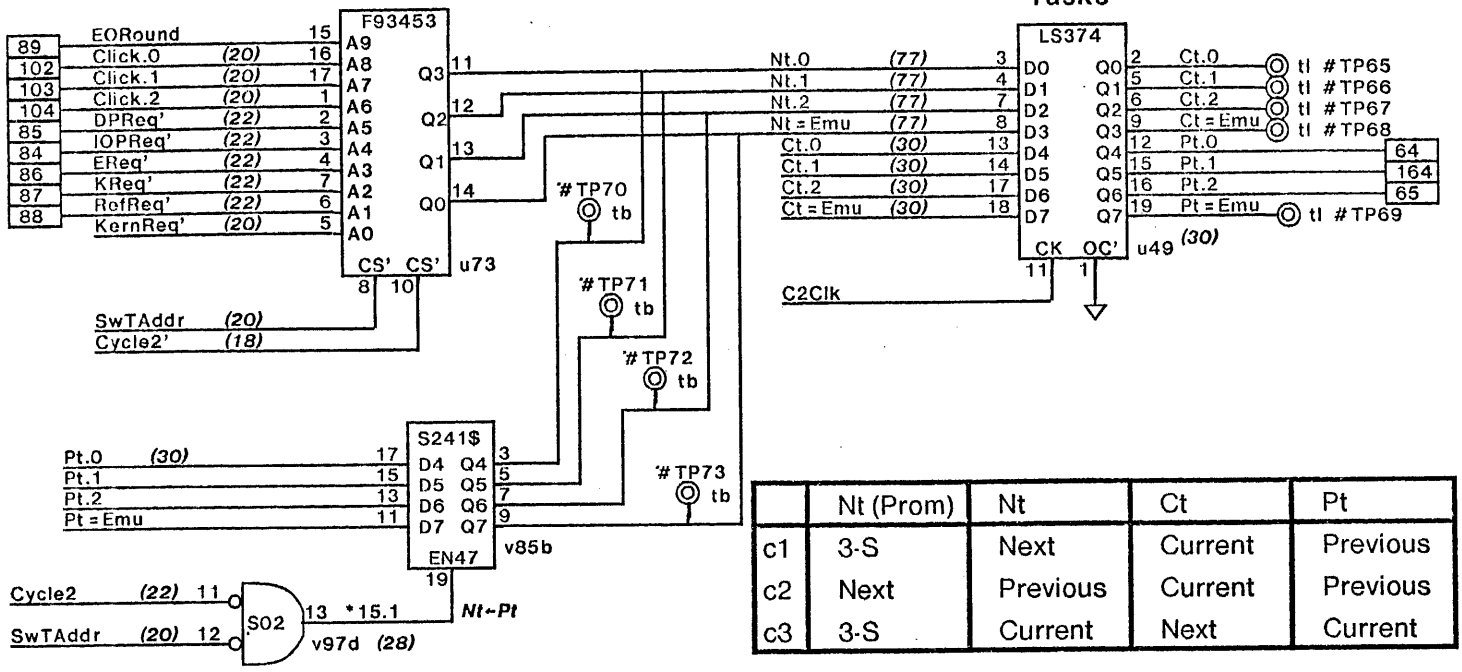


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC, CPE-FP	A4	SHEET 14 OF	A



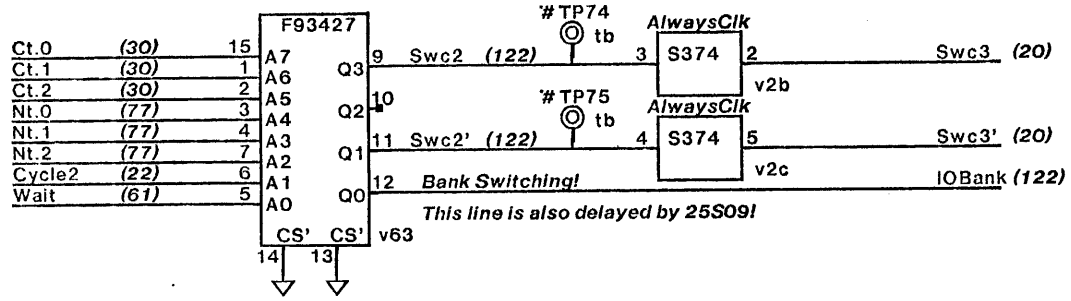
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC CPE-ER		SHEET 15 OF	

ScheduleProm-RevD



	Nt (Prom)	Nt	Ct	Pt
c1	3-S	Next	Current	Previous
c2	Next	Previous	Current	Previous
c3	3-S	Current	Next	Current

SwitchProm-RevR



Note: This is a non-standard PROM. IOBank has been added!

Task Numbers

0	Emulator
1	Display/LSEP
2	Ethernet
3	Refresh
4	Disk
5	IOP
6	Control Store R/W
7	Kernel

Swc2 timing = max(133,101,101)

22	t to Kreq'	20	t to SwTAddr	28	t to Nt←Pt
55	F93453 addr to Nt	25	F93453 CS' to Nt	15[2]	S241 EN to Nt
45	F93427 addr to Swc2	45	F93427 addr to Swc2	45	F93427 addr to Swc2
10[1]	25S09 SB setup	10[1]	25S09 SB setup	10[1]	25S09 SB setup
132[1] = 133 nS		100[1] = 101 nS		98[3] = 101 nS	

Click Assignment

0	Ethernet
1	Disk
2	IOP
3	Ethernet/Disk
4	Display/LSEP/Rfrsh

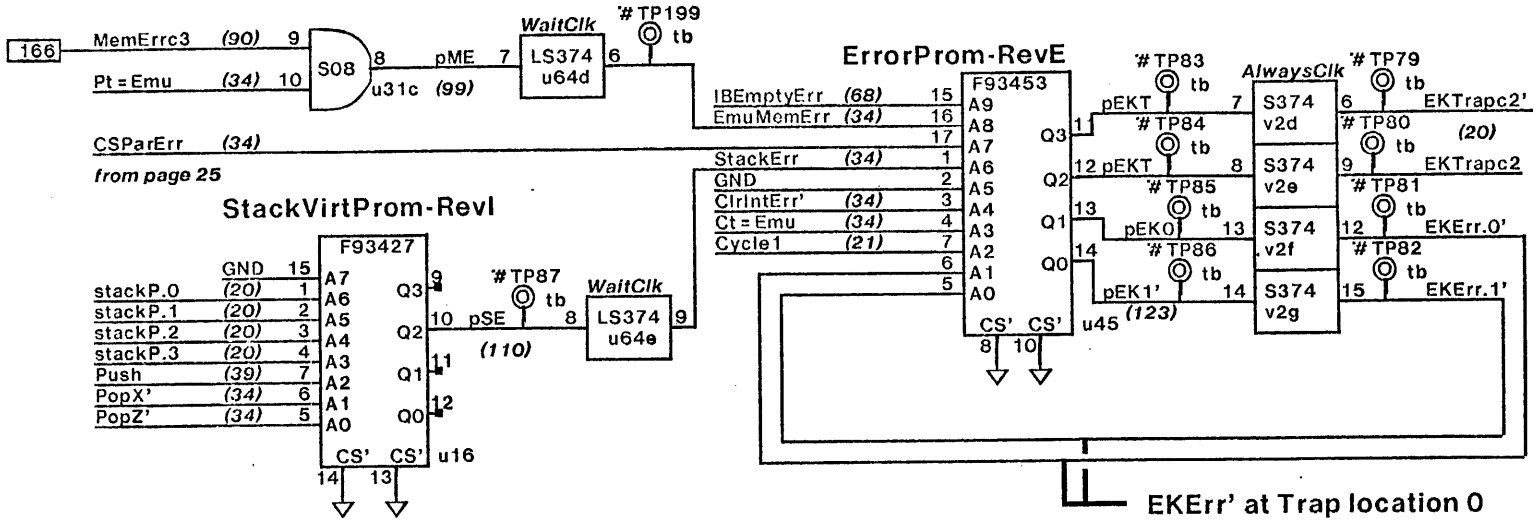
Notes:

When Disk = SA4000, Click 3 is Ethernet only.
When Disk = Trident, Click 3 is Ethernet on even rounds, Trident on Odd rounds (ie, 10-click round)

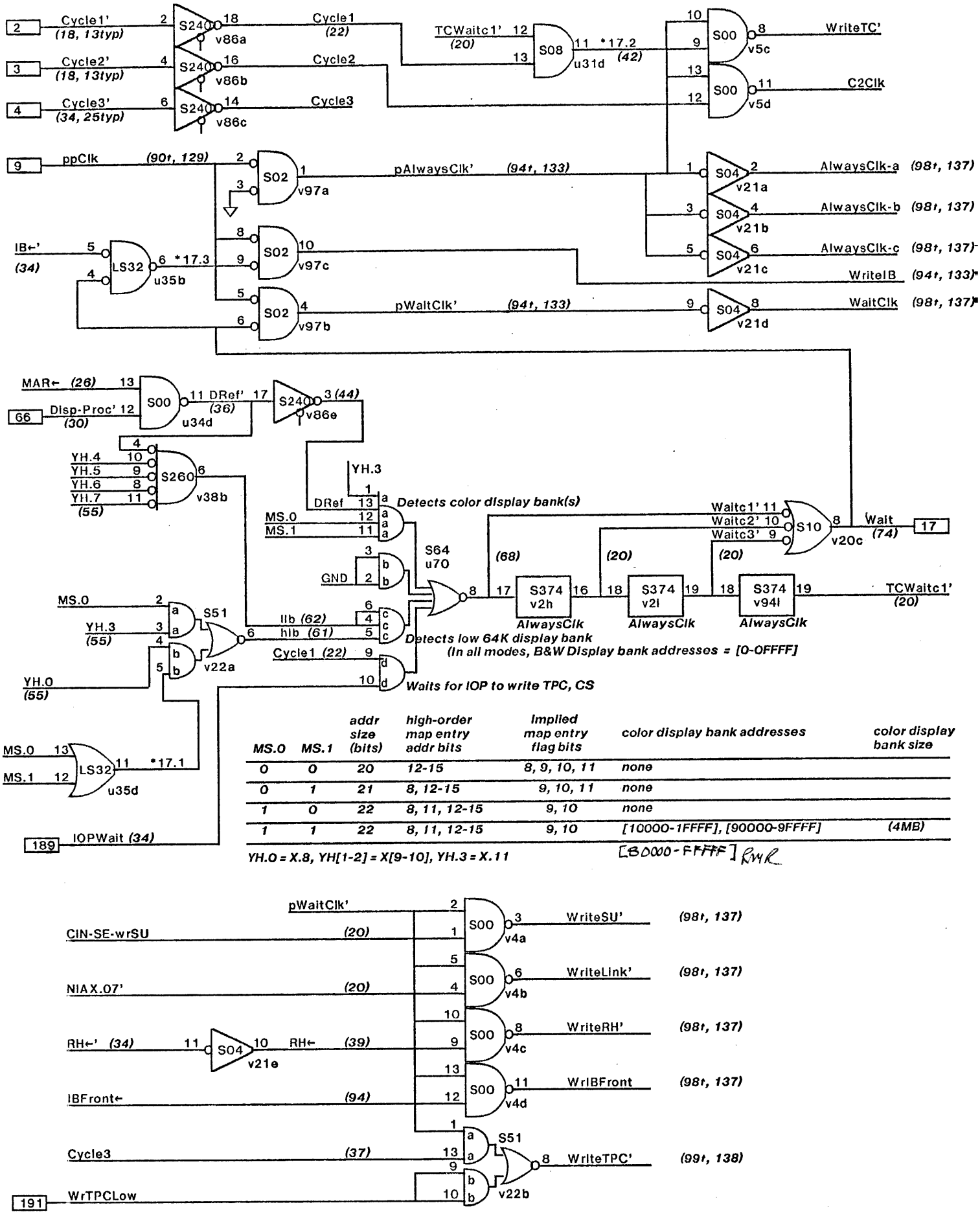
The Display & LSEP-refresh tasks never both use Click 4

Warning: This drawing contains font 4 macros!

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC CPE.EP		SHEET 16 OF	



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-EP		SHEET 17 OF	

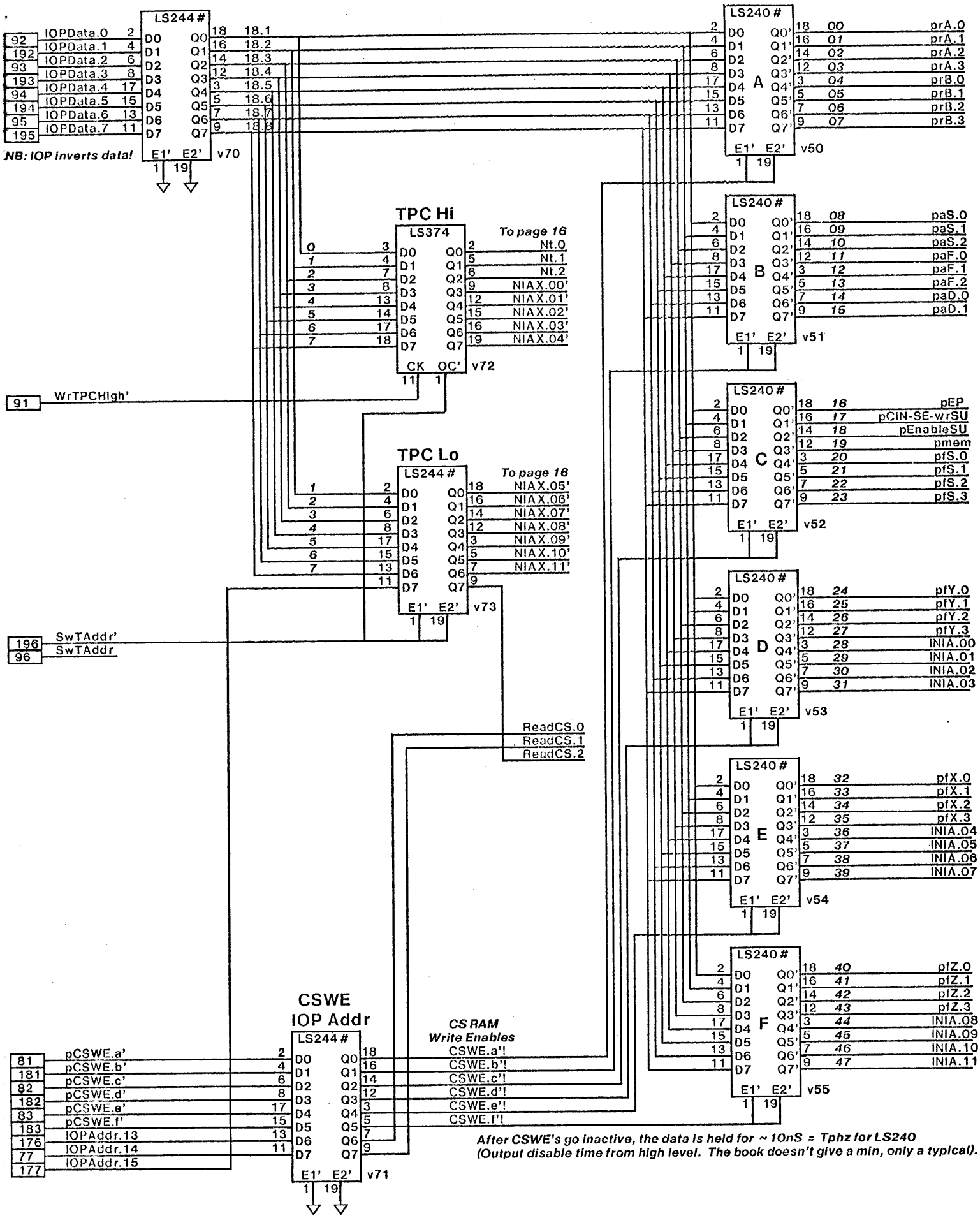


MS.0	MS.1	addr size (bits)	high-order map entry addr bits	Implied map entry flag bits	color display bank addresses	color display bank size
0	0	20	12-15	8, 9, 10, 11	none	
0	1	21	8, 12-15	9, 10, 11	none	
1	0	22	8, 11, 12-15	9, 10	none	
1	1	22	8, 11, 12-15	9, 10	[10000-1FFFF], [90000-9FFFF]	(4MB)

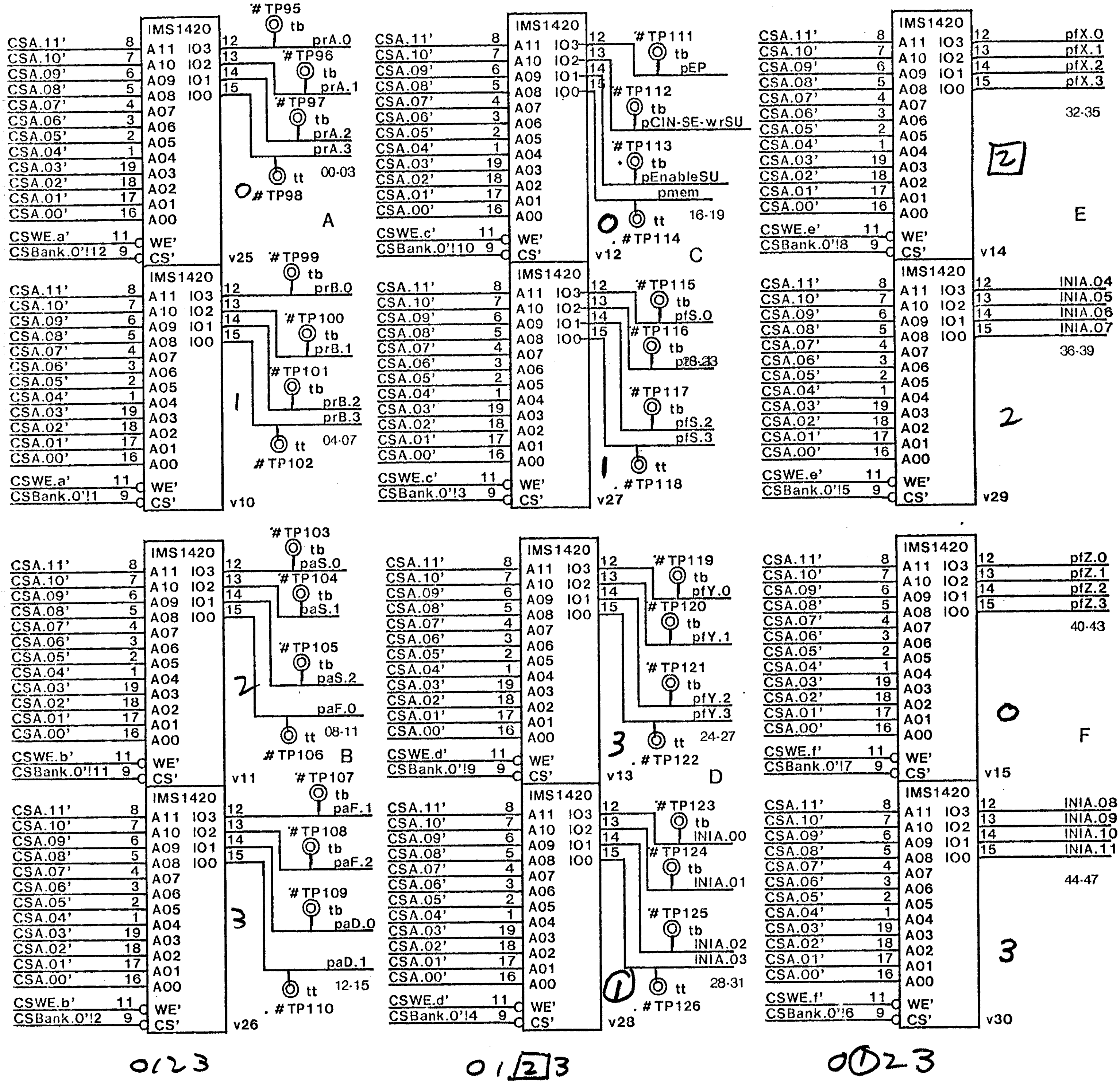
YH.0 = X.8, YH[1-2] = X[9-10], YH.3 = X.11

[80000-FFFFF] RMR

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC CPE-ER		SHEET 18 OF	



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC CPE ER		SHEET 19 OF	

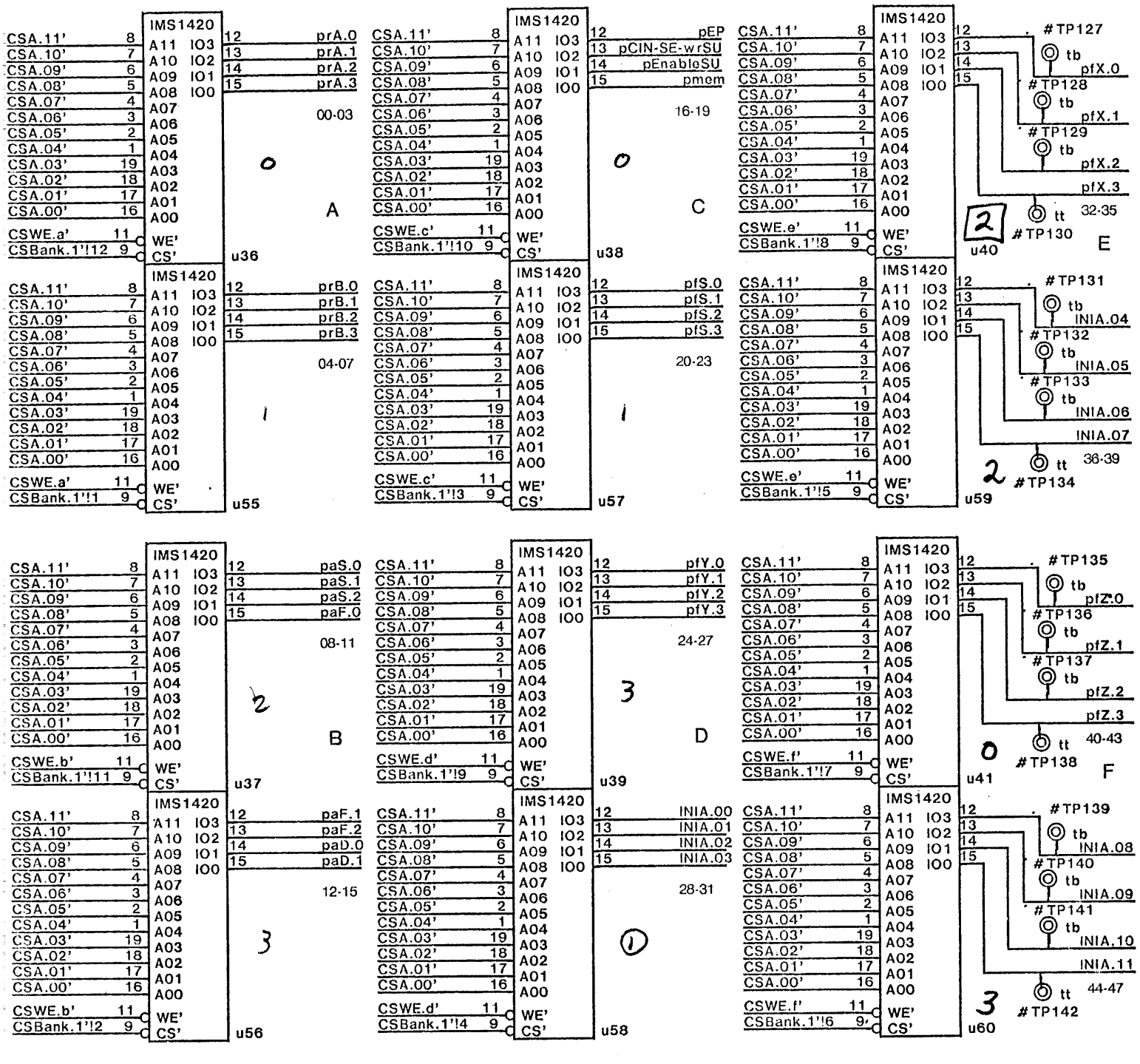


READ		**WRITE - Data Hold**	
Clock to CSA' valid	*17*	*tPLH for LS240*	*12*
Transmission Delay	*13*	*tPZ for LS244*	*10*
tAA for IMS 1420-55	*50*		*22*
CS Data valid at	*80*		

This suggests that IMS 1420-70 would also work without any trouble.

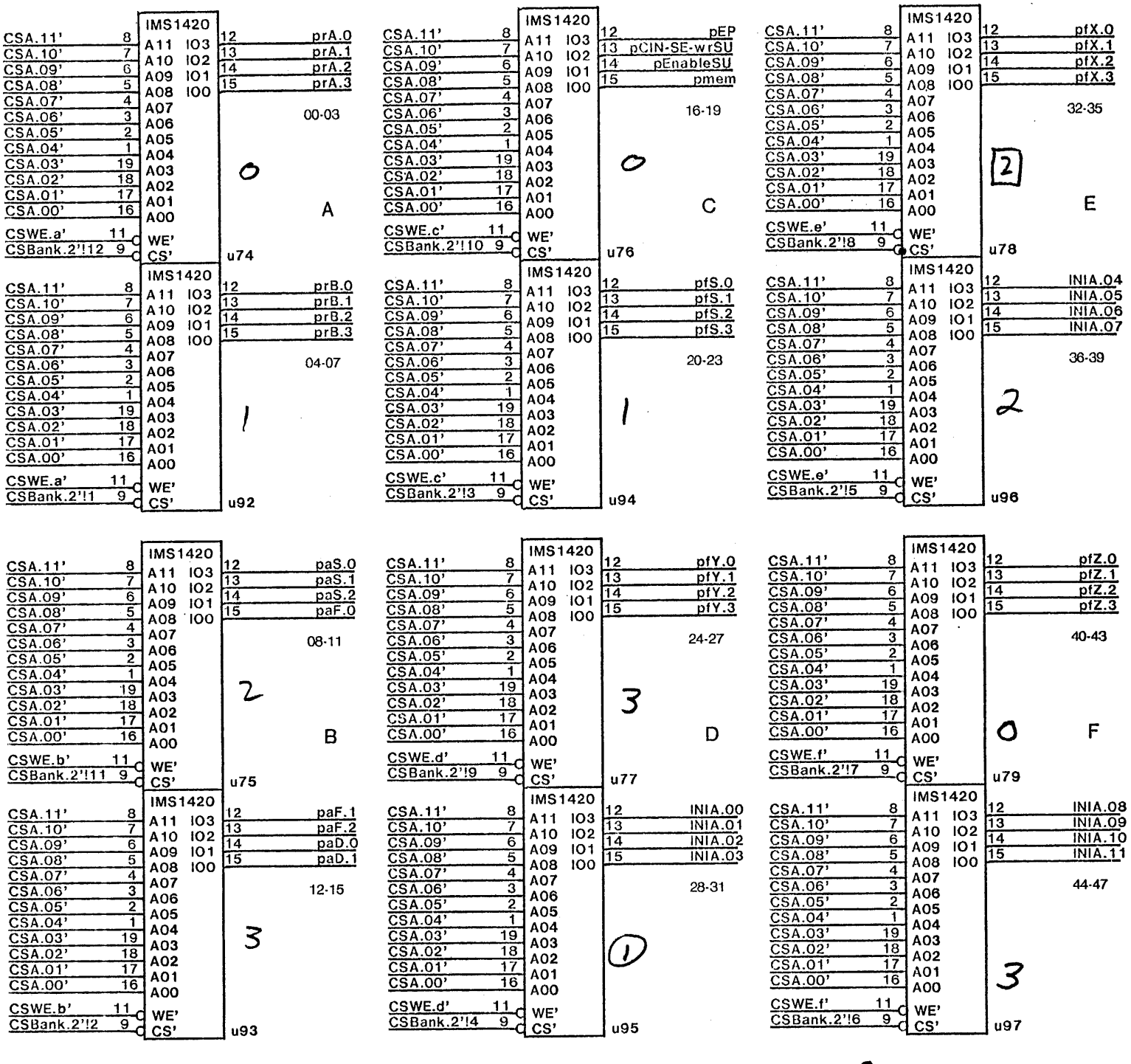
Warning: This drawing contains font 4 macros!

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS / TITLE	DWG SIZE A4	DWG NO. 156P12560 / SHEET 20 OF	SHEET REV. A



Warning: This drawing contains font 4 macros!

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC CPE-FP		SHEET 21 OF	



0123 0123 0123

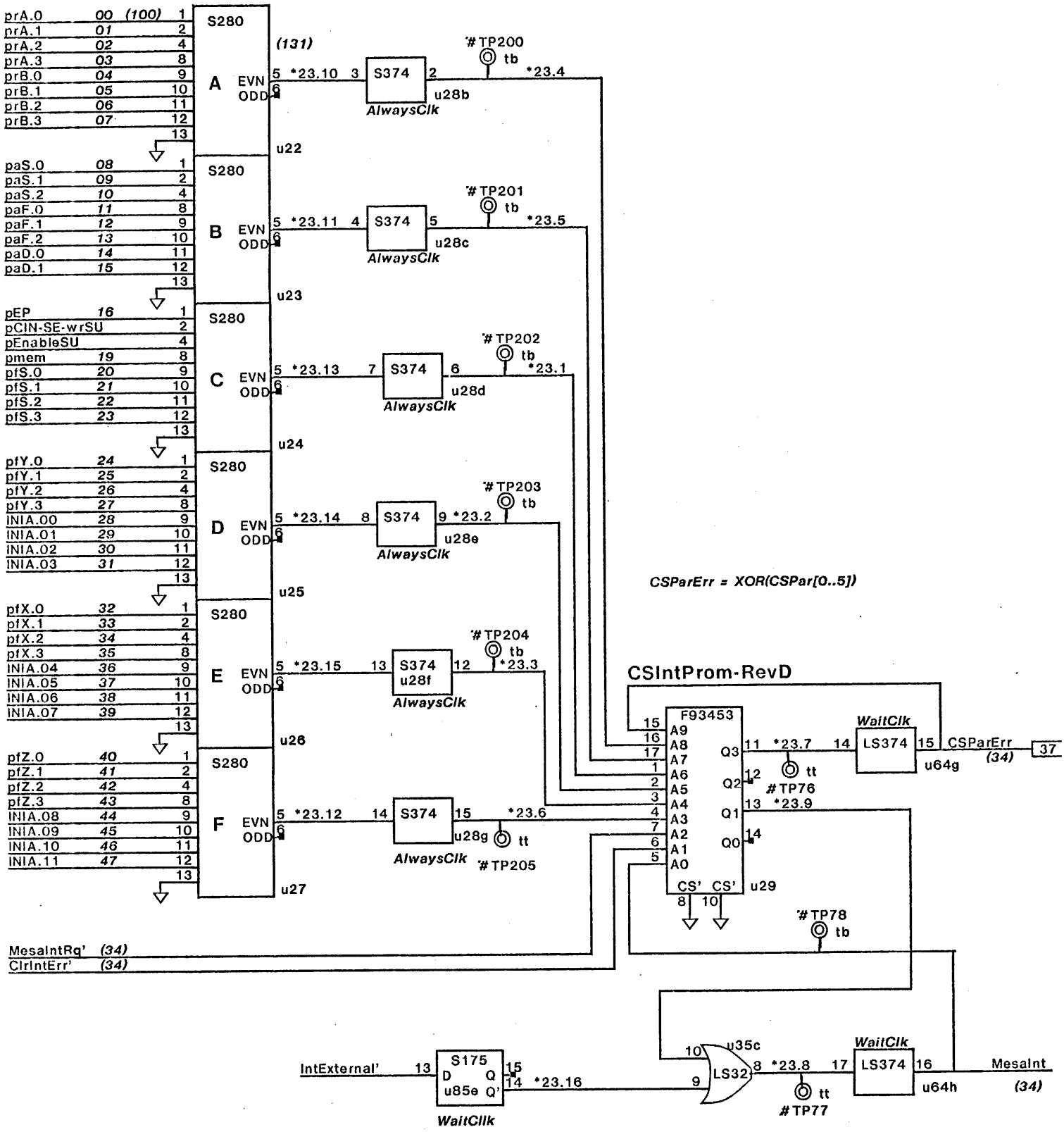
Warning: This drawing contains font 4 macros!

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC CRE-ER		SHEET 22 OF	

The control Store has been removed to make room for the floating point module.

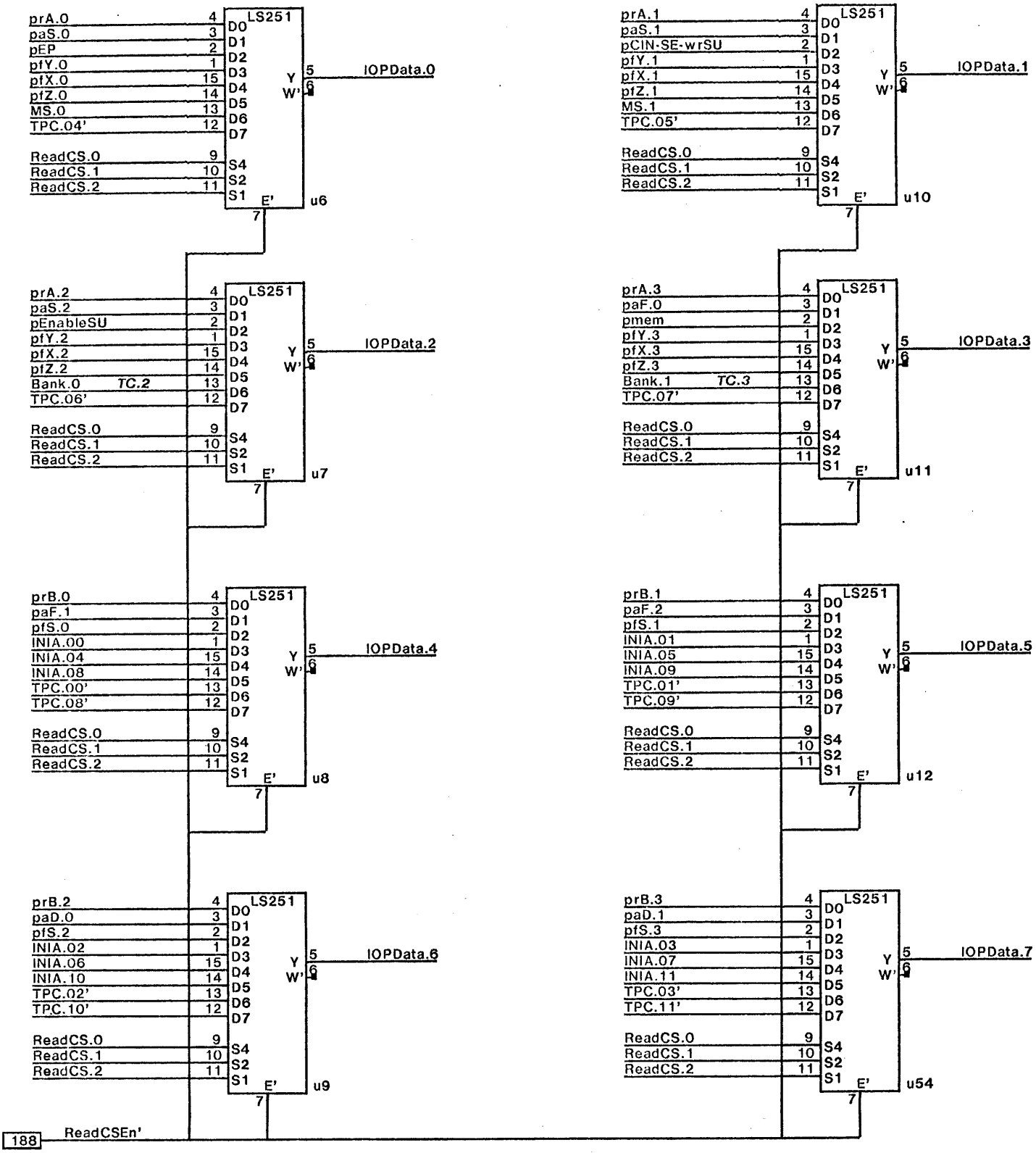
Warning: This drawing contains font 4 macros!

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC, CPE-FP	A4	SHEET 23 OF	A



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 24 OF	

NB: TC[0-3] have been replaced by Bank[0-3].

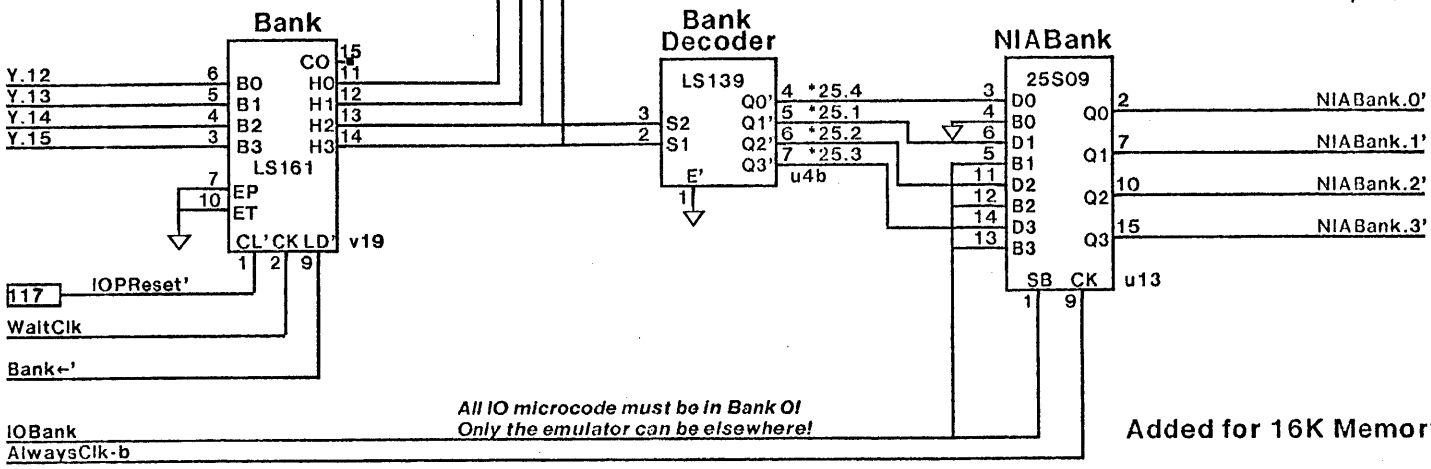


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC, CPE-FP	A4	SHEET 25 OF	A

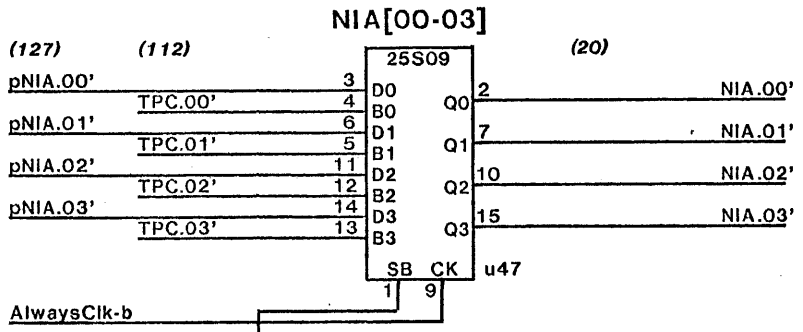
see p. 19

MS.0
MS.1
Bank.0
Bank.1

to p. 26



This section is standard



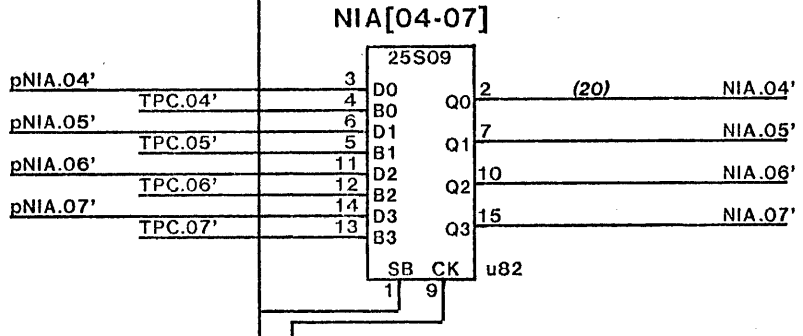
NOTE on Control Store Addresses

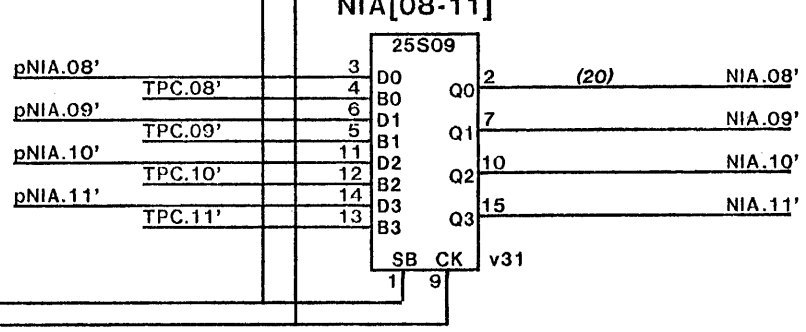
The next instruction address for the control store comes from one of two basic places:

1. *TPC registers if switching tasks*
2. *From the INIA field of the previous microinstruction*

In the case of (1), task 6's TPC registers are used by the IOP to provide the address when the IOP wants to read or write data into the control store.

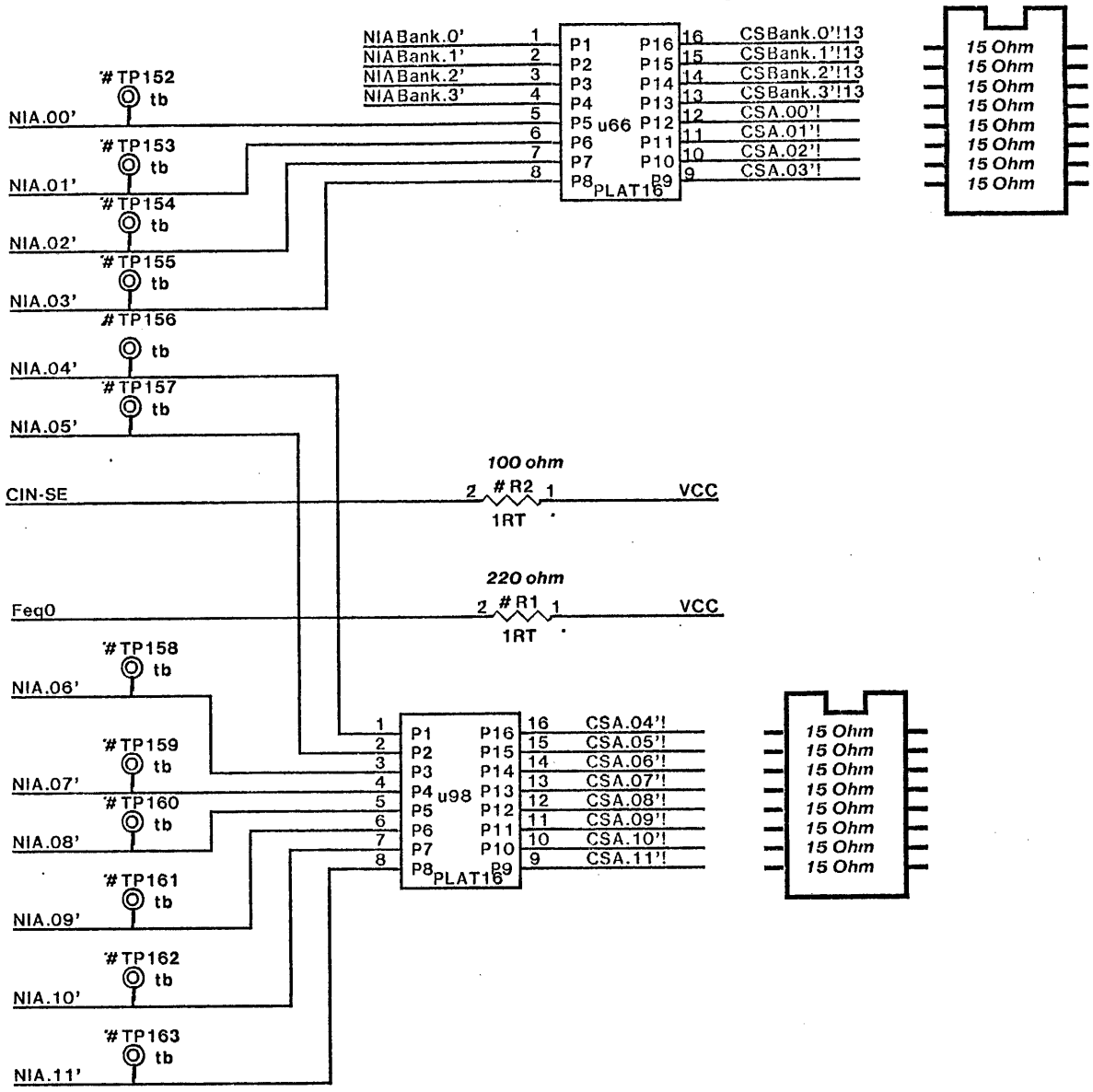
In the case of (2), the INIA field is suitably modified by the trap and conditional branch logic on page 16



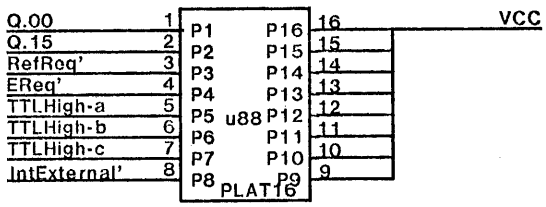


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC, CPE-FP	A4	SHEET 26 OF	A

CS NIA Line Matching



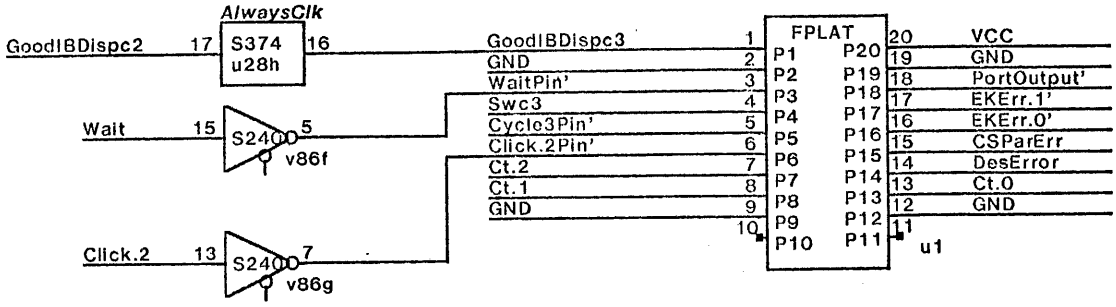
1 KOhm Pullups

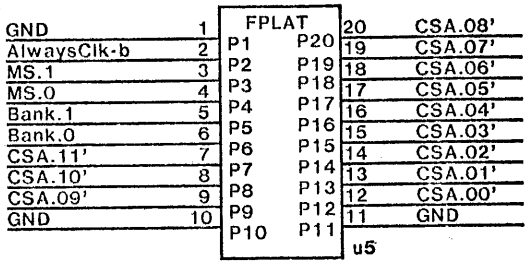


Beckman Resnet DIP

898-1-1K

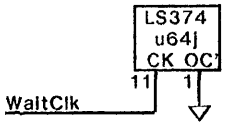
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 27 OF	


AlwaysClk
GoodIBDispc2
17
S374
u28h
16
Wait
15
S240
5
v86f
Click.2
13
S240
7
v86g
GoodIBDispc3
GND
WaitPin'
Swc3
Cycle3Pin'
Click.2Pin'
Ct.2
Ct.1
GND
1
2
3
4
5
6
7
8
9
10
FPLAT
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P20
P19
P18
P17
P16
P15
P14
P13
P12
P11
20
19
18
17
16
15
14
13
12
11
VCC
GND
PortOutput'
EKErr.1'
EKErr.0'
CSParErr
DesError
Ct.0
GND
u1


GND
AlwaysClk-b
MS.1
MS.0
Bank.1
Bank.0
CSA.11'
CSA.10'
CSA.09'
GND
1
2
3
4
5
6
7
8
9
10
FPLAT
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P20
P19
P18
P17
P16
P15
P14
P13
P12
P11
20
19
18
17
16
15
14
13
12
11
CSA.08'
CSA.07'
CSA.06'
CSA.05'
CSA.04'
CSA.03'
CSA.02'
CSA.01'
CSA.00'
GND
u5

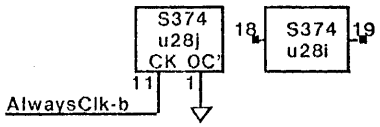
LS374 u89

b IBPtr.0
c IBPtr.1
d EmuMemErr
e StackErr
f pc16'
g CSParErr
h MesaInt
i SFLG'



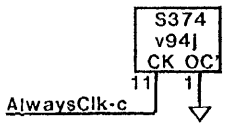
S374 v03

b CSPar.0
c CSPar.1
d CSPar.2
e CSPar.3
f CSPar.4
g CSPar.5
h GoodIBDispc3
i



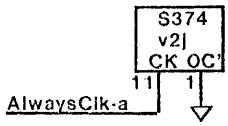
S374 v15

b MAR←'
c AllowMDR←
d TC.0
e TC.1
f TC.2
g TC.3
h KernReq'
i TCWaitc1'



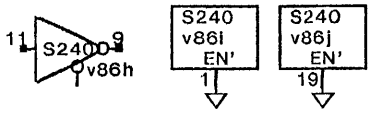
S374 u69

b Swc3
c Swc3'
d EKTrapc2'
e EKTrapc2
f EKErr.0'
g EKErr.1'
h Waitc2'
i Waitc3'



S240 w05

a Cycle1
b Cycle2
c Cycle3
d Cycle3'
e DRef
f WaitPin'
g Click.2Pin'
h



S04 v43

a aD.0'
b MAR←
c IBEmptyErr'
d Des←YBus
e XBus←SU
f Port←

S04 v39

a AlwaysClk-a
b AlwaysClk-b
c AlwaysClk-c
d WaitClk
e RH←
f Fne0

S10 x01

a FPCLK
b ←FP'
c Xhigh←0

S175 u35

b MAS'
c MDS'
d SDS'
e IntExternal
f *anon*

S00 v42

a XBus←SU'
b pMAR←'
c MarPgCross'
d CIN←pc16

S00 v85

a Pop
b Nibble'
c Byte'
d DRef'

S00 u36

a *anon*
b WPort
c *anon*
d DesClkDisable

S00 v93

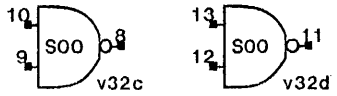
a WriteSU'
b WriteLink'
c WriteRH'
d WrIBFront

S00 u33

a pTC.0
b pTC.1
c WriteTC'
d C2Clk

S00 u54

a pByte'
b SelFP'
c
d



S02 v08

a pAlwaysCLK'
b pWaitCLK'
c WriteIB
d Nt←Pt

S08 v32

a paSh.0
b pAllowMDR←
c pME
d *anon*

S51 u90

a hlb
b WrTPC

S10 v79

a sh
b Push
c XByte'

S10 v23

a pTC.2
b pTC.3
c Wait

S20

a XBus←IB'
b EnLRotn'

LS32 v98

a DispBr'
b EnDispBr.3A'
c EnDispBr2-3B'
d EnDispBr0-1'

LS32 v20

a Link.0'
b Link.1'
c Link.2'
d Link.3'

LS32 u18

a pRet'
b *anon*
c MesaInt
d M01

S38 v58

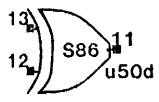
a Q.00
b Q.15
c CarryIn
d CarryIn

S51 u90

a Waitc1'
b WriteTPC'

S86 v81

a PageCross
b MapRef
c Refresh
d



S260 w04

a IBEmptyErr
b *anon*

LS139 v49

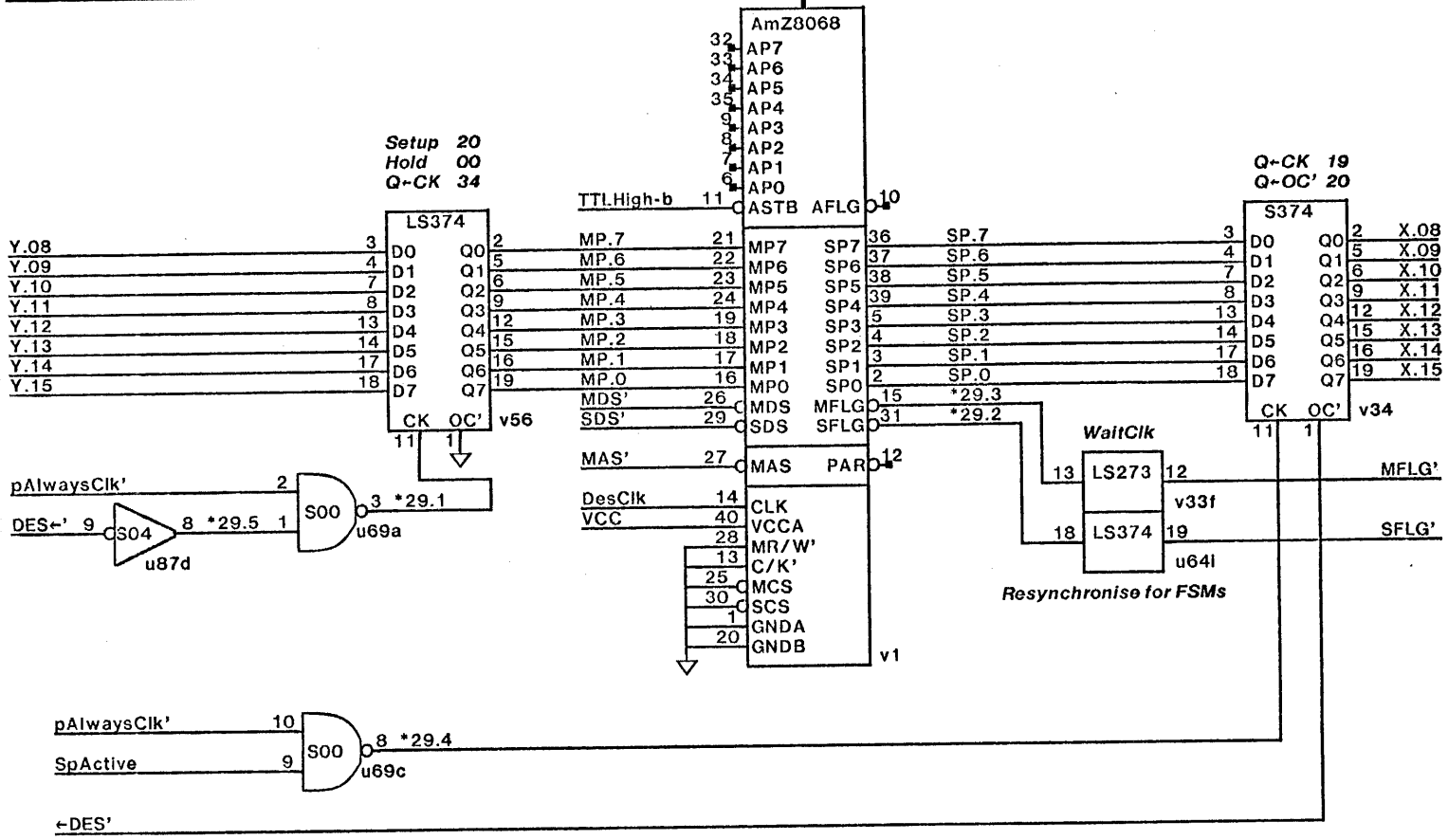
a 8-bit port
b bank decode

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 29 OF	

DES Hardware Configuration Information

The chip is hard-wired in multiplexed control mode.
The Master port is wired for writes only.
The Auxiliary port is not used at all.
Data always flows from the Master port to the Slave port.
Des clock is high for c2 and c3, low for c1
The microcode is synchronous, so MFLG' is ignored.
Key parity errors, PAR', are ignored!

Zero out the high X bus when reading DES
←DES' triggers Xhigh←0 page12(CPE11.sil)



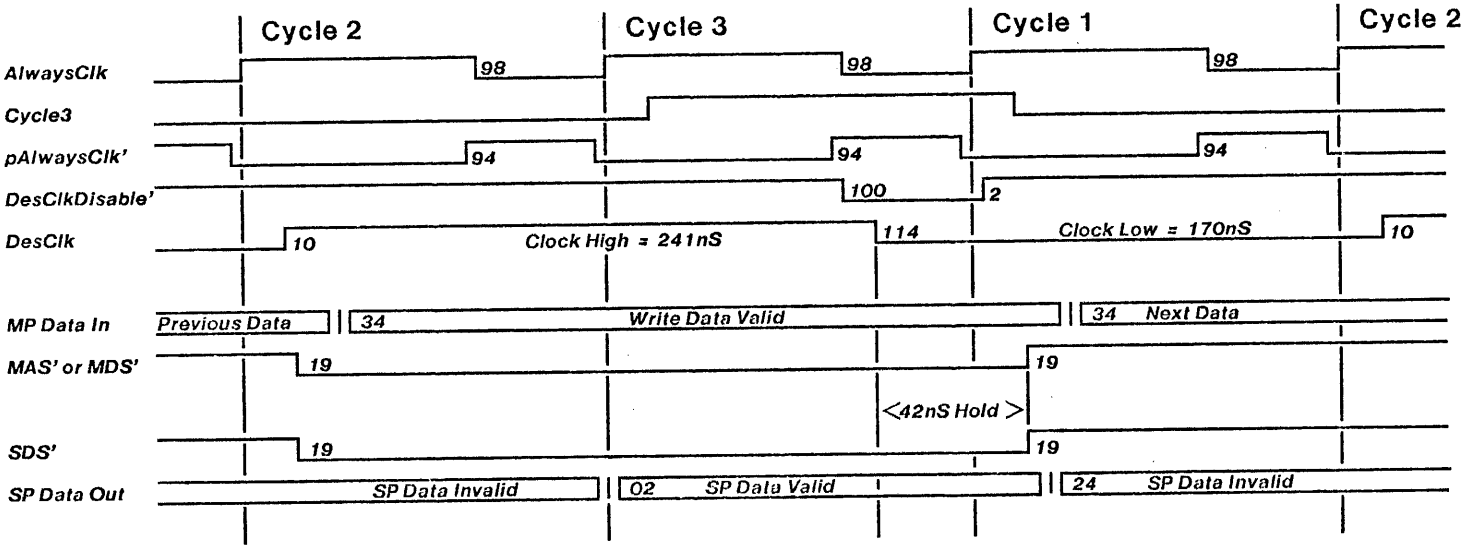
Warning: This drawing contains font 4 macros!

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC CPE ER		SHEET 30 OF	

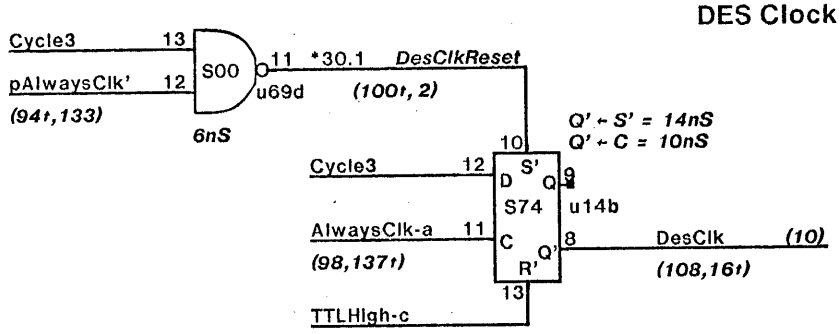
		AMD #	min.	max.	actual used	Notes
Clock & Reset						
Clock width HIGH		1	115		241	
Clock width LOW		2	115		170	
Clock Cycle		3	250		411	
Clock High to MAS'&MDS' High	Reset Hold	6	0	50	19	
MP and SP Strobe Times						
MAS' falling to MAS' rising (address)	MAS width Low	32	80		274	
MDS' falling to MDS' rising (data)	MDS width Low	44a	125	1000	274	Can't exceed 1000, so have to watch out for WaitClk
MDS' rising to MDS' falling	MDS Recovery	46	125		137	
SDS' falling to SDS' rising (data read)	SDS width Low	44a	125	1000	274	Can't exceed 1000, so have to watch out for WaitClk
SDS' rising to SDS' falling	SDS Recovery	46	125		137	
Clk falling to MDS' rising	MDS Hold	45	20	70	42	This is the difficult bit! See circuitry below.
Clk falling to SDS' rising	SDS Hold	46	20	70	42	This is the difficult bit! See circuitry below.
MAS Write into Master Port						
Data Valid to MAS' rising	Address Setup	36	55		268	
Data Hold after MAS' rising	Address Hold	37	60		243	
MDS Write into Master Port						
Data Valid to MDS' rising	Data Setup	47b	125		268	
Data Hold after MDS' rising	Data Hold	48	80		243	
SDS Read from Slave Port						
SDS falling to Data Valid	SP Access	49b		120		
SDS rising to Data Invalid	SP Data Hold	50	5			
SDS falling to SFLG rising	SP Flag	51		125		for last byte read

DES Clock Generator Timing

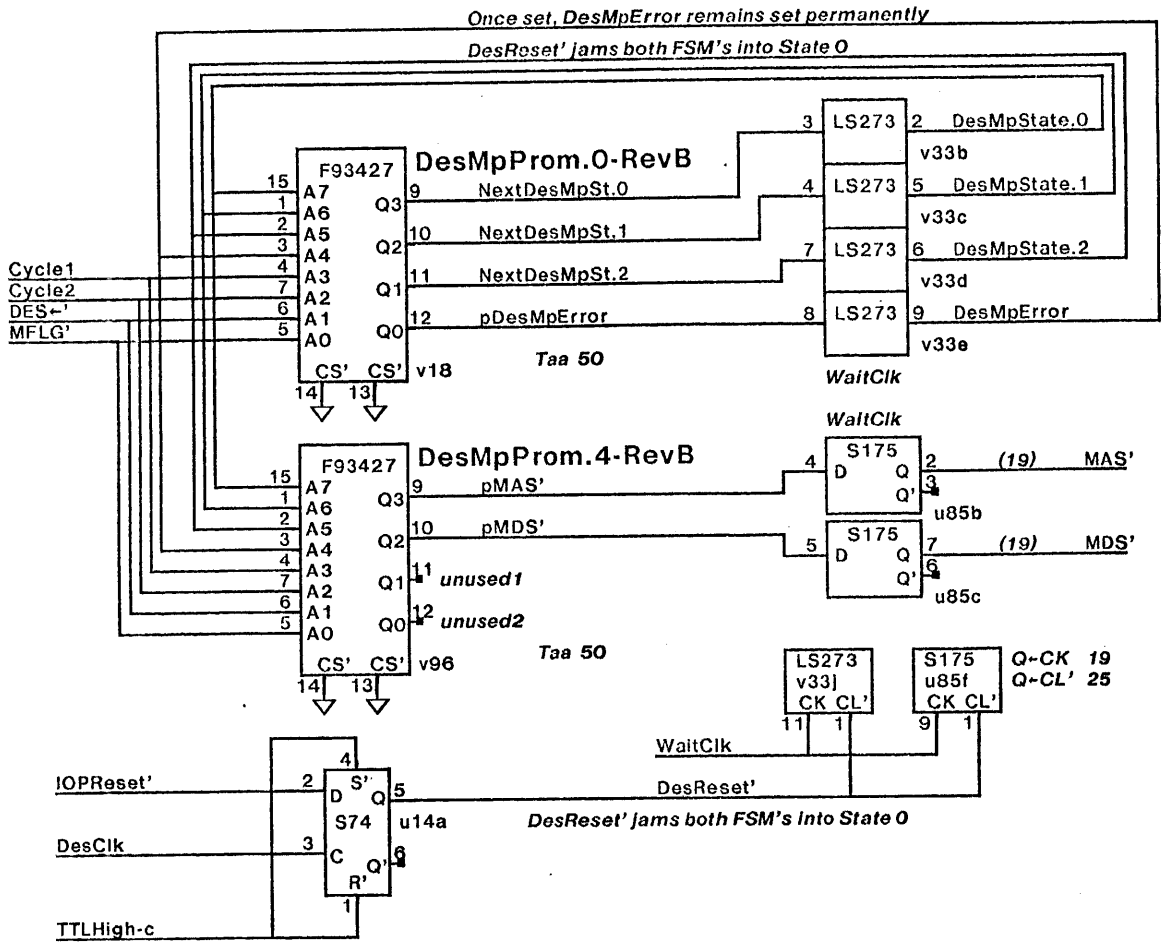
Note: Because of the requirement to hold MDS' and SDS' for 20 to 70 nanoseconds after DesClk falling, we bring DesClk down early in Cycle 3. MAS', MDS' and SDS' follow at the end of Cycle 3.



DES Clock Generator

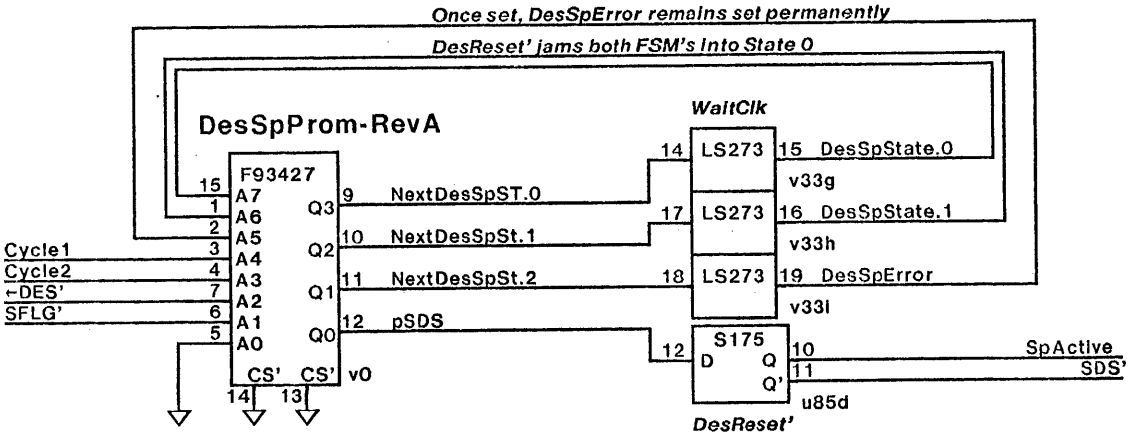


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 31 OF	

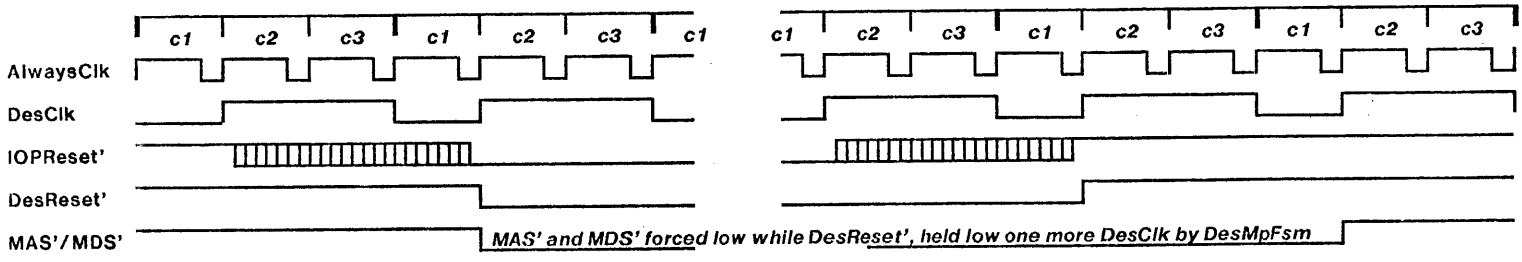


Des Master Port FSM

Des Slave Port FSM



Reset Des Chip and FSM's with IOPReset'

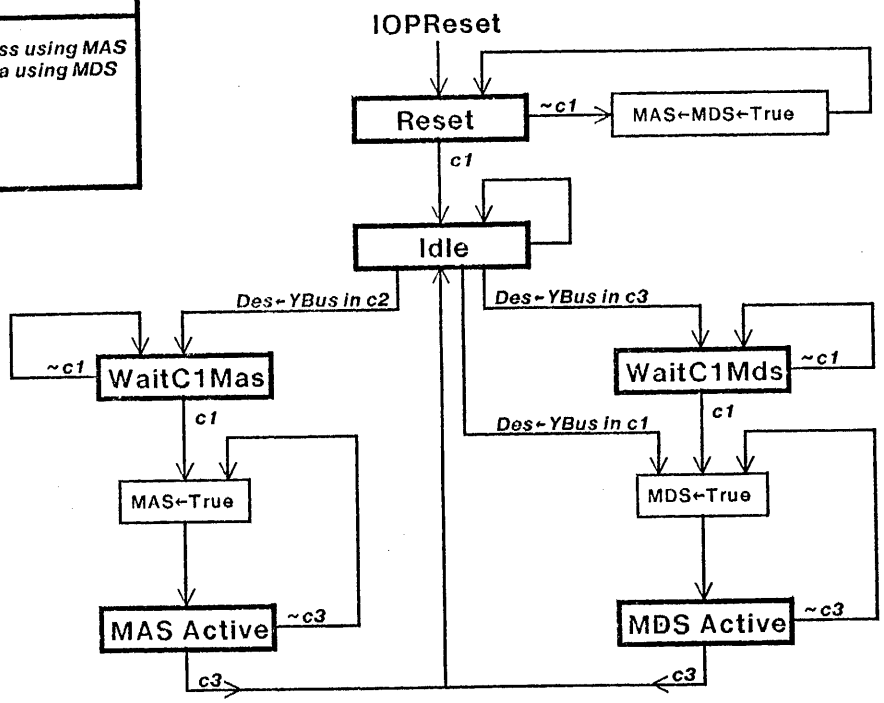


XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC, CPE-FP	A4	SHEET 32 OF	A

Note on semantics of Master Port Writes

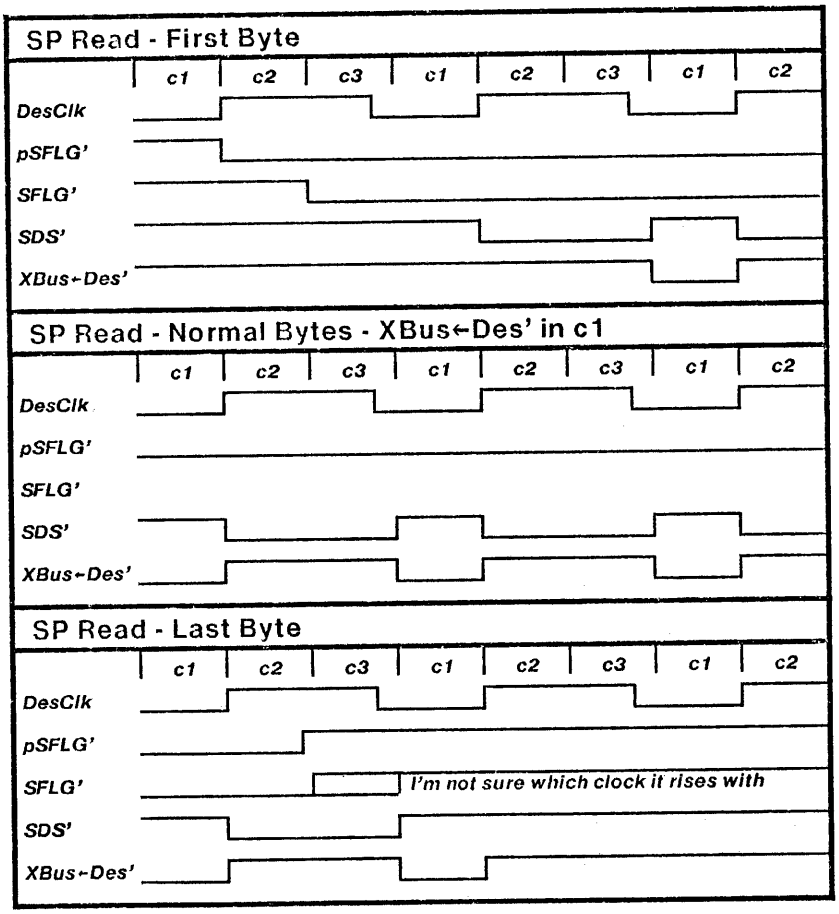
If you write to the Des chip in c2, it means write an address using MAS
If you write to the Des chip in c1 or c3, it means write data using MDS
You may have to wait for c1 in some of these cases.

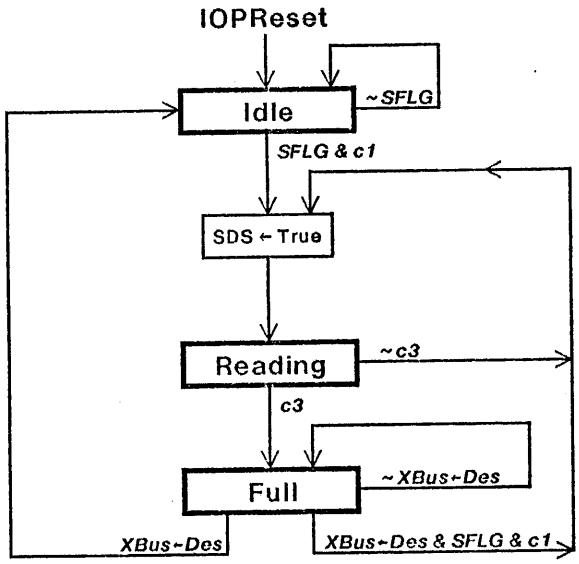
The signals are shown logical-true.
The implementation below inverts signals as required.



Master Port Finite-State Machine - Error handling of DesMpError signal is not shown

Slave Port Finite-State Machine - Error handling of DesSpError signal is not shown

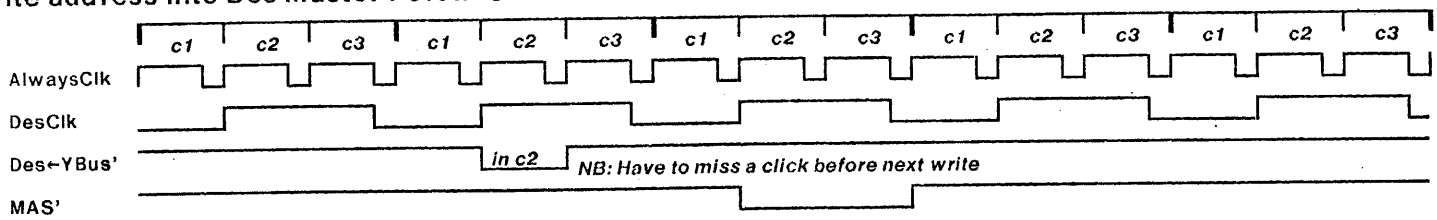




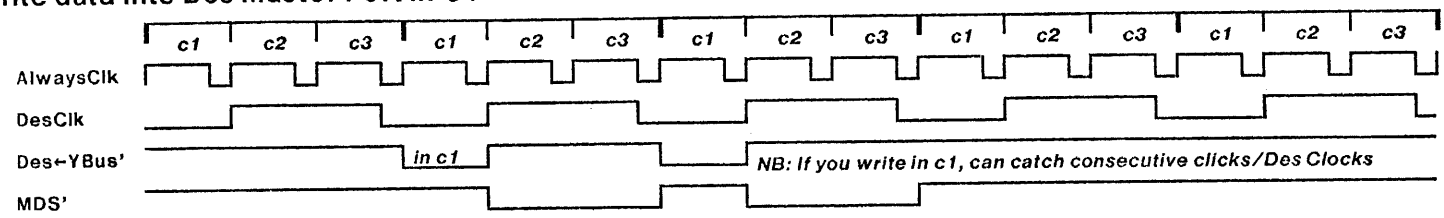
The signals are shown logical-true.
The implementation below inverts signals as required.

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC CPE-ER		SHEET 33 OF	

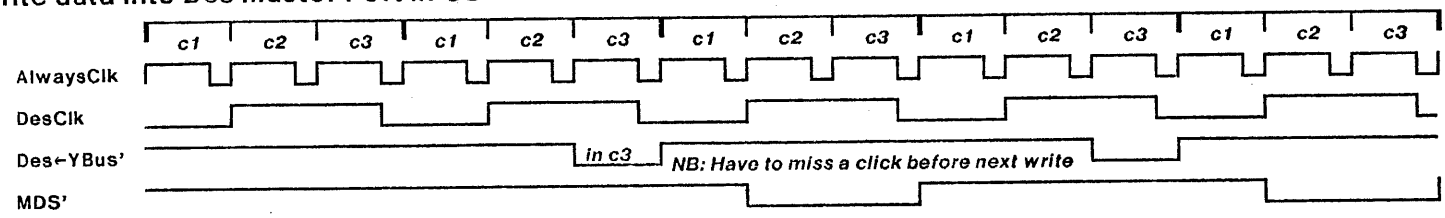
Write address into Des Master Port in C2



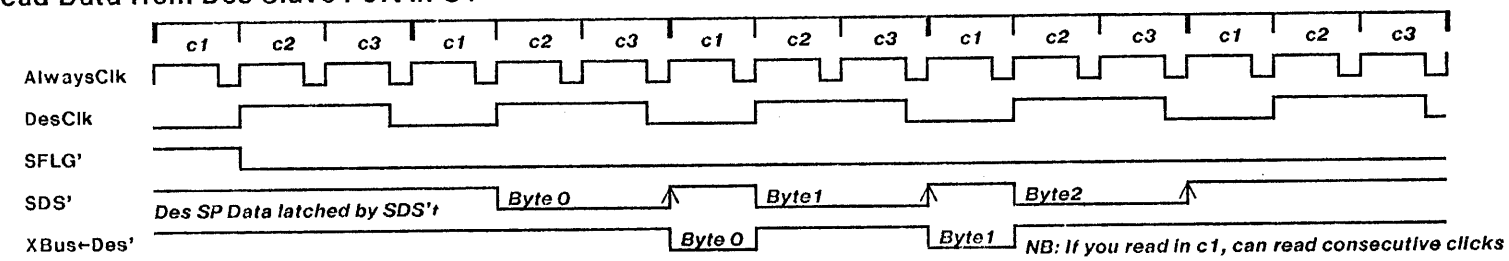
Write data into Des Master Port in C1



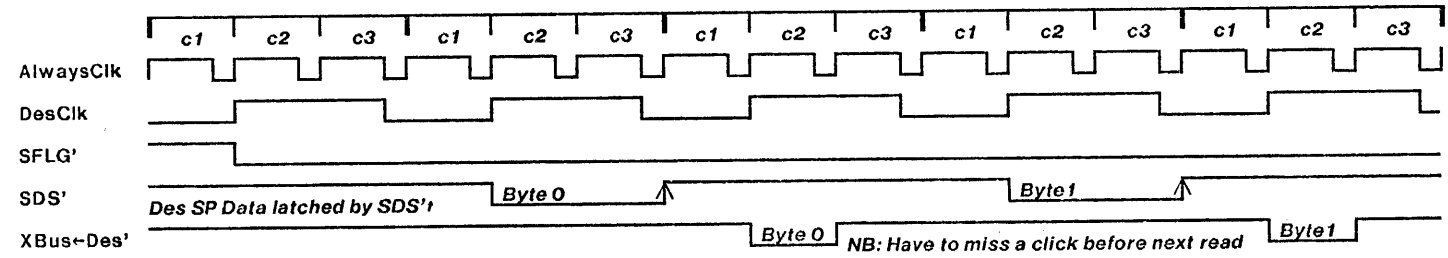
Write data into Des Master Port in C3



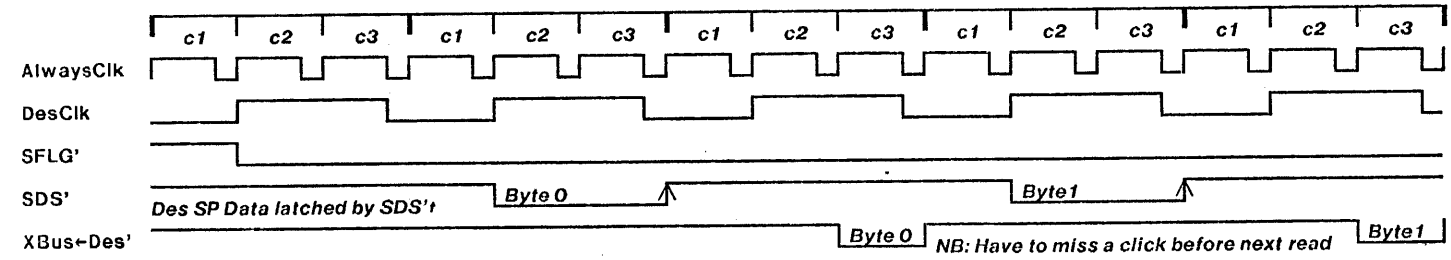
Read Data from Des Slave Port in C1



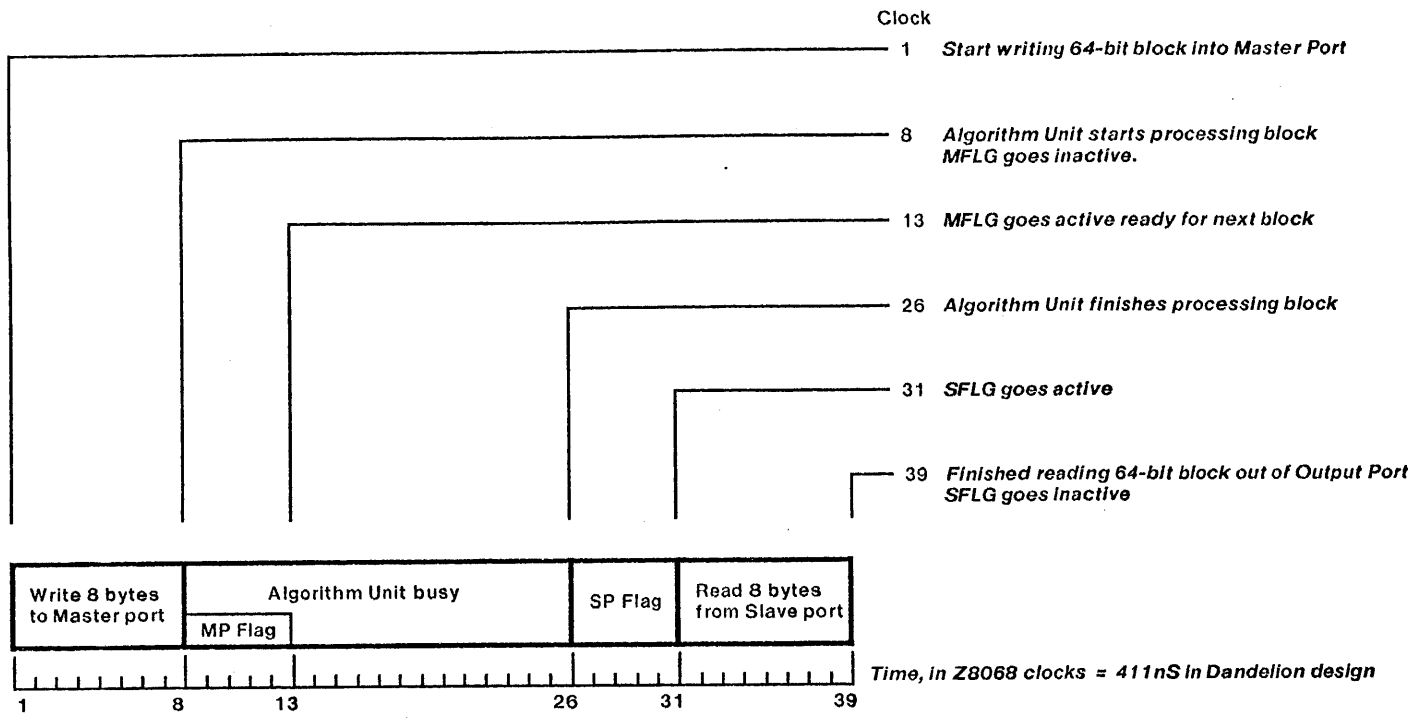
Read Data from Des Slave Port in C2



Read Data from Des Slave Port in C3



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC, CPE-FP *Reference*	A4	SHEET 34 OF	A



WARNING! This data is not guaranteed to be correct!

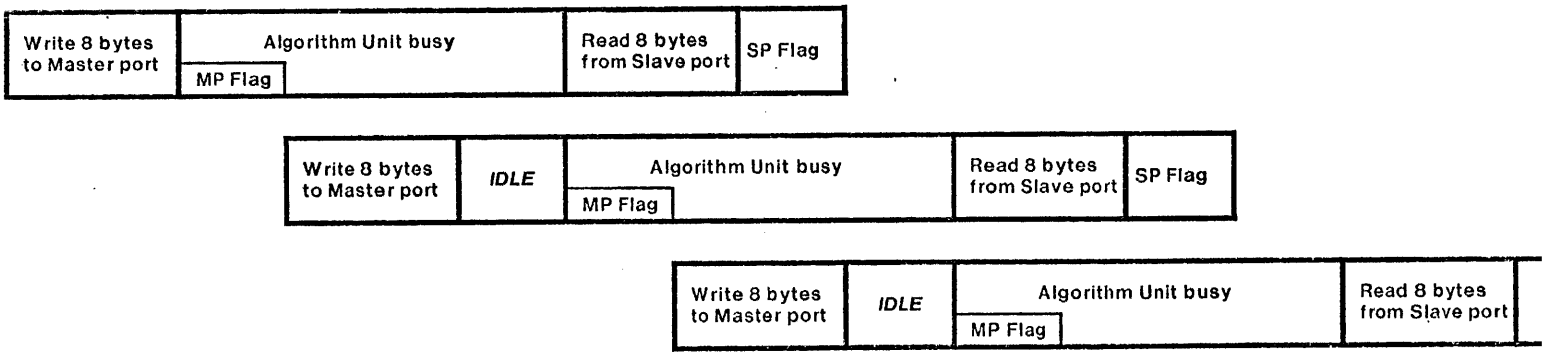
NOTES:

The longest operation in encrypting a block is the time it takes to get the data through the algorithm unit, 18 clocks. Therefore, this is the bottleneck in the pipelining scheme, and the software must aim to keep the Algorithm unit fully busy.

Apart from the first and last blocks, the time taken to encrypt the middle blocks is 18 clocks.

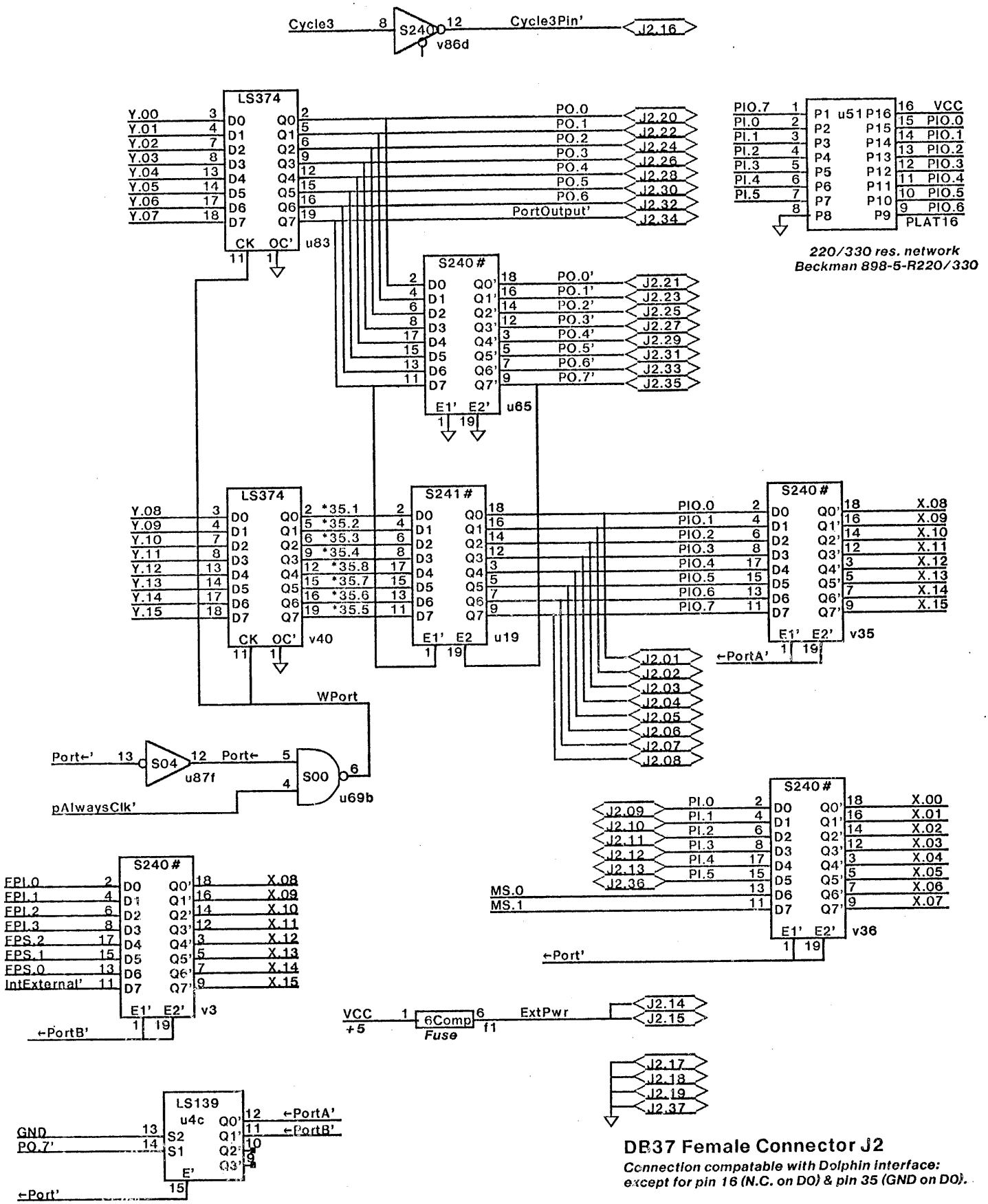
One possible pipelining scheme

WARNING! This data is not guaranteed to be correct!



WARNING! This data is not guaranteed to be correct!

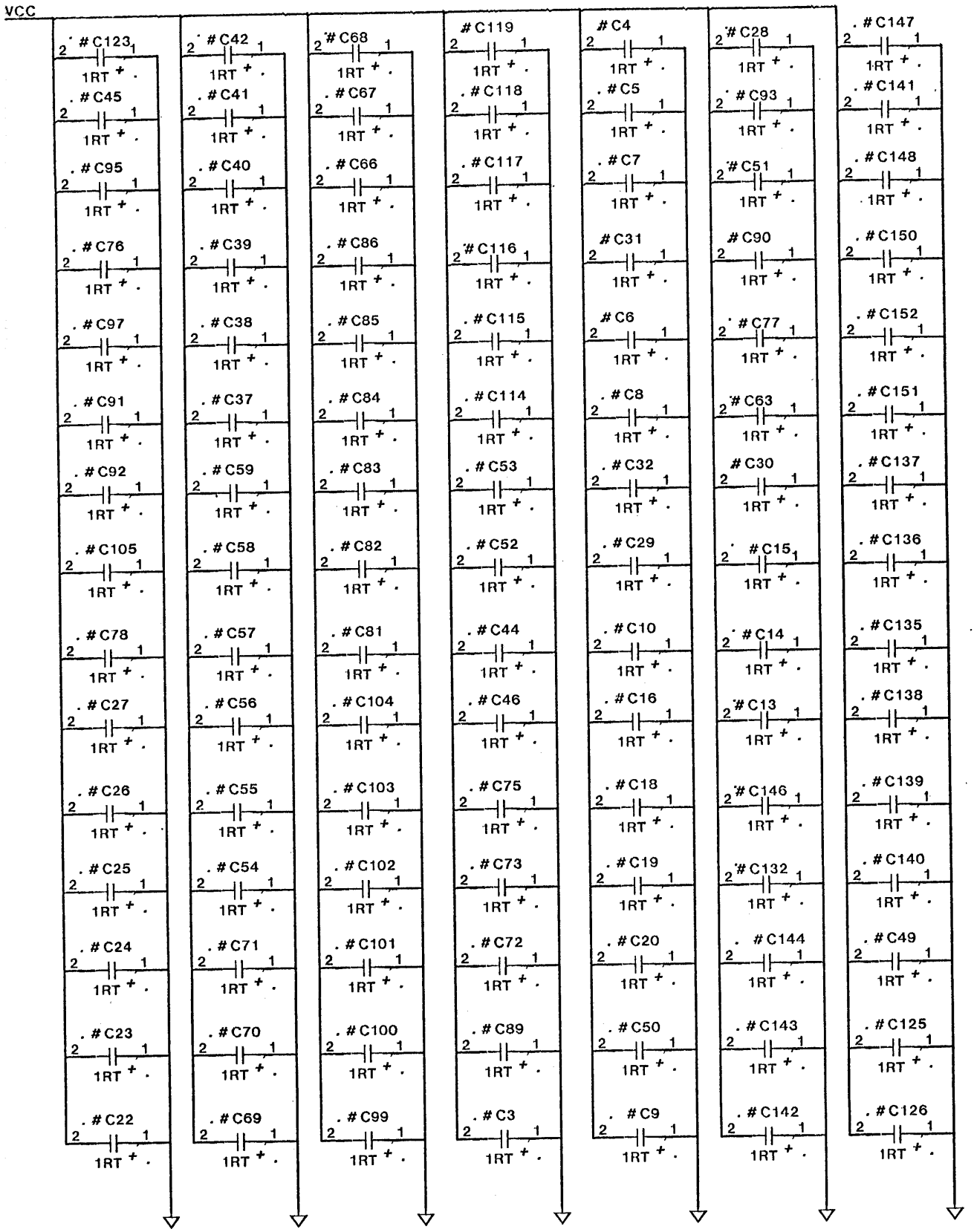
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC, CPE-FP *Reference*	A4	SHEET 35 OF	A



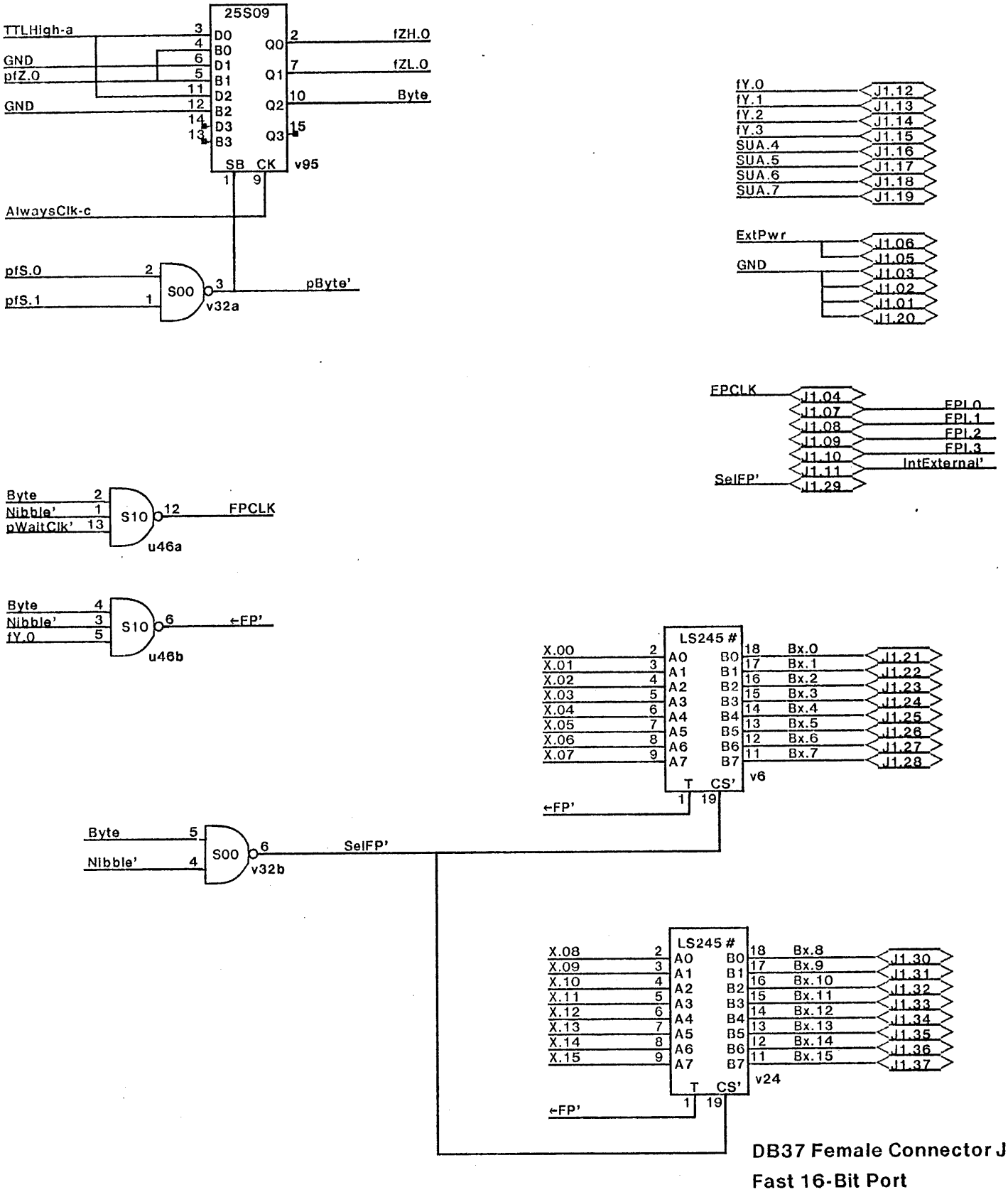
DB37 Female Connector J2

Connection compatable with Dolphin interface: except for pin 16 (N.C. on DO) & pin 35 (GND on DO).

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 36 OF	



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 37 OF	



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P12560	SHEET REV.
	TITLE SCHEMATIC CPE-FP	A4	SHEET 38 OF	A

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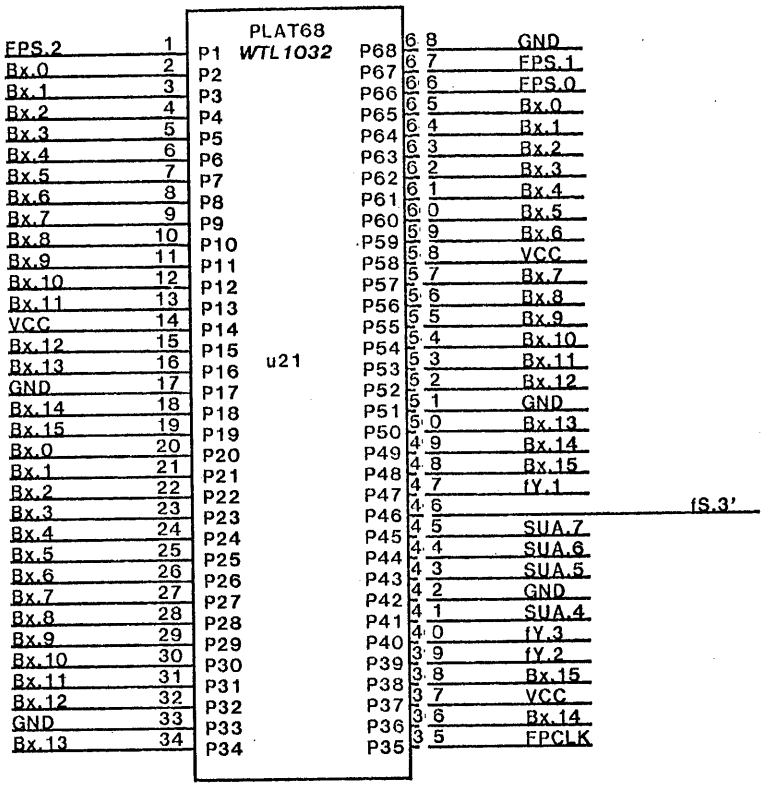
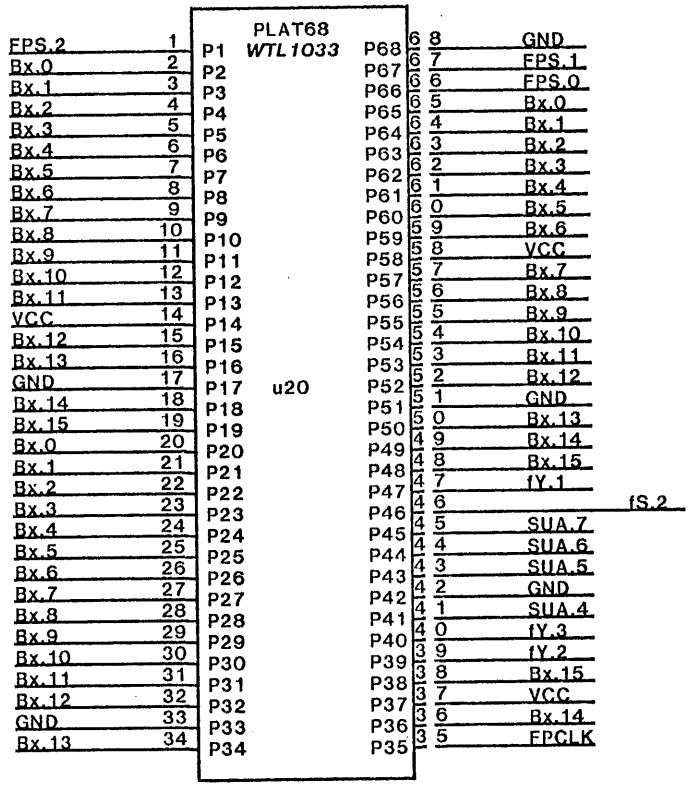
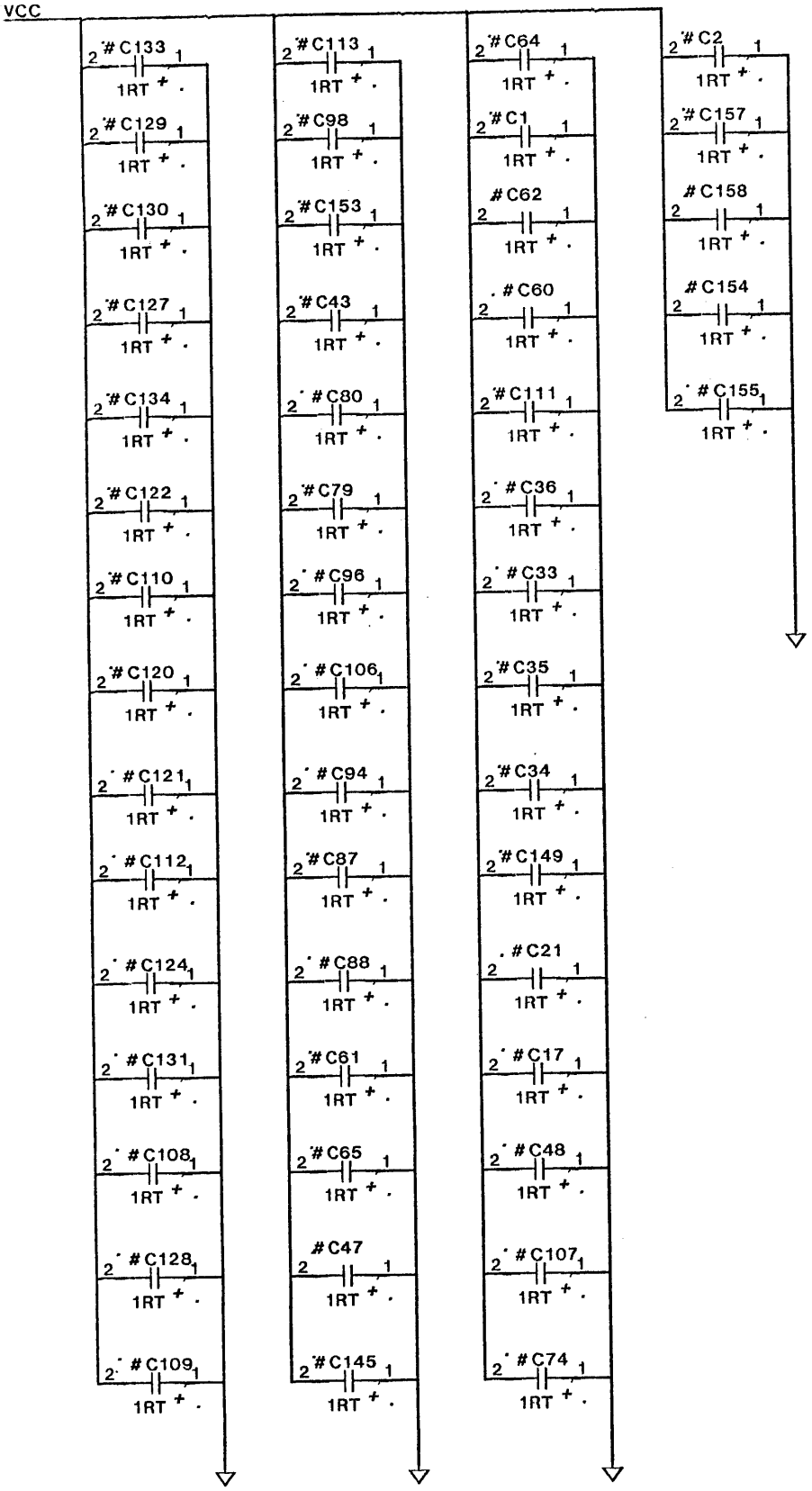
Old contents merged with next page

Floating Point Timing Diagram to be done

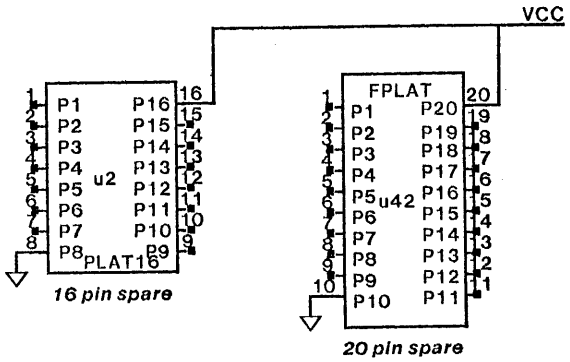


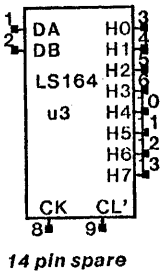


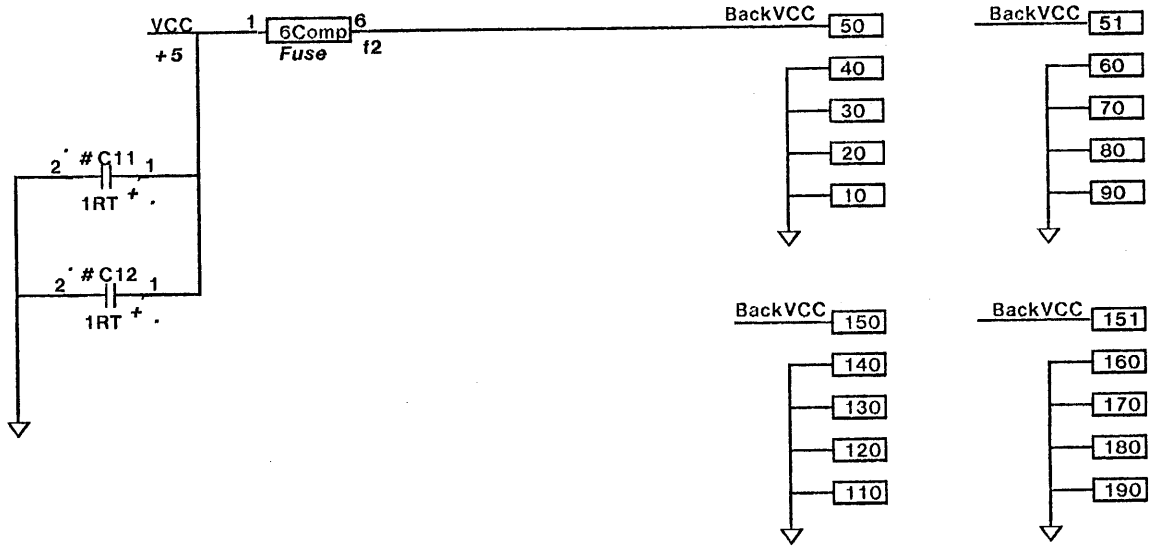
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 40 OF	



XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC CPE-FP		SHEET 41 OF	







XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P12560	SHEET REV. A
	TITLE SCHEMATIC, CPE-FP		SHEET 42 OF	

Comments:

1) *Designator notation notes: u1-99 = U1-99, v0-99 = U100-199, w0-99 = U200-299*
2) *The last item on lines below, preceeded by a semicolon (;), is the schematic page number on which the test point, connector or signal information originates.*
3) *Line with no page number was a continuation of the previous line.*

```
#TP1      .1i  12BitCarry      ;04
#TP10     .1i  IB.2            ;07
#TP100    .1i  prB.1           ;20
#TP101    .1i  prB.2           ;20
#TP102    .1i  prB.3           ;20
#TP103    .1i  paS.0           ;20
#TP104    .1i  paS.1           ;20
#TP105    .1i  paS.2           ;20
#TP106    .1i  paF.0           ;20
#TP107    .1i  paF.1           ;20
#TP108    .1i  paF.2           ;20
#TP109    .1i  paD.0           ;20
#TP11     .1i  IB.3            ;07
#TP110    .1i  paD.1           ;20
#TP111    .1i  pEP             ;20
#TP112    .1i  pCIN-SE-wrSU    ;20
#TP113    .1i  pEnableSU       ;20
#TP114    .1i  pmem            ;20
#TP115    .1i  pfS.0           ;20
#TP116    .1i  pfS.1           ;20
#TP117    .1i  pfS.2           ;20
#TP118    .1i  pfS.3           ;20
#TP119    .1i  pfY.0           ;20
#TP12     .1i  IB.4            ;07
#TP120    .1i  pfY.1           ;20
#TP121    .1i  pfY.2           ;20
#TP122    .1i  pfY.3           ;20
#TP123    .1i  INIA.00         ;20
#TP124    .1i  INIA.01         ;20
#TP125    .1i  INIA.02         ;20
#TP126    .1i  INIA.03         ;20
#TP127    .1i  pfX.0           ;21
#TP128    .1i  pfX.1           ;21
#TP129    .1i  pfX.2           ;21
#TP13     .1i  IB.5            ;07
#TP130    .1i  pfX.3           ;21
#TP131    .1i  INIA.04         ;21
#TP132    .1i  INIA.05         ;21
#TP133    .1i  INIA.06         ;21
#TP134    .1i  INIA.07         ;21
#TP135    .1i  pfZ.0           ;21
#TP136    .1i  pfZ.1           ;21
#TP137    .1i  pfZ.2           ;21
#TP138    .1i  pfZ.3           ;21
#TP139    .1i  INIA.08         ;21
#TP14     .1i  IB.6            ;07
#TP140    .1i  INIA.09         ;21
#TP141    .1i  INIA.10         ;21
#TP142    .1i  INIA.11         ;21
#TP15     .1i  IB.7            ;07
#TP152    .1i  NIA.00'         ;27
#TP153    .1i  NIA.01'         ;27
#TP154    .1i  NIA.02'         ;27
#TP155    .1i  NIA.03'         ;27
#TP156    .1i  NIA.04'         ;27
#TP157    .1i  NIA.05'         ;27
#TP158    .1i  NIA.06'         ;27
#TP159    .1i  NIA.07'         ;27
#TP16     .1i  IBFront←        ;07
#TP160    .1i  NIA.08'         ;27
#TP161    .1i  NIA.09'         ;27
#TP162    .1i  NIA.10'         ;27
#TP163    .1i  NIA.11'         ;27
#TP17     .1i  GoodIBDispc2    ;07
#TP172    .1i  IBPtr.0         ;07
#TP173    .1i  IBPtr.1         ;07
#TP174    .1i  ExitKernel'     ;11
#TP175    .1i  EnterKernel'    ;11
#TP176    .1i  ClrIntErr'      ;11
#TP177    .1i  IBDisp'         ;11
#TP178    .1i  MesaIntRq'      ;11
#TP179    .1i  IBPtr←1'        ;11
#TP18     .1i  RefillIntc2     ;07
#TP180    .1i  IBPtr←0'        ;11
#TP181    .1i  PopZ'           ;11
#TP182    .1i  ←ib'            ;11
#TP19     .1i  SelectIB0'      ;07
#TP192    .1i  pPC16'          ;17
#TP199    .1i  EmuMemErr       ;17
#TP2      .1i  PageCross       ;04
#TP20     .1i  pIBPtr.0        ;07
#TP200    .1i  *23.4           ;24
#TP201    .1i  *23.5           ;24
#TP202    .1i  *23.1           ;24
#TP203    .1i  *23.2           ;24
#TP204    .1i  *23.3           ;24
#TP205    .1i  *23.6           ;24
#TP21     .1i  pIBPtr.1        ;07
#TP22     .1i  SelectIB1'      ;07
#TP23     .1i  MAR←'           ;10
#TP24     .1i  DispBr.0'       ;13
#TP25     .1i  DispBr.1'       ;13
#TP26     .1i  DispBr.2'       ;13
#TP27     .1i  DispBr.3A'      ;13
#TP28     .1i  DispBr.3B'      ;13
#TP29     .1i  pNIA.00'        ;14
#TP3      .1i  R.00            ;04
#TP30     .1i  pNIA.01'        ;14
#TP31     .1i  pNIA.02'        ;14
#TP32     .1i  pNIA.03'        ;14
#TP33     .1i  pNIA.04'        ;14
#TP34     .1i  pNIA.05'        ;14
```

#TP35	.1i	pNIA.06'	;14
#TP36	.1i	pNIA.07'	;14
#TP37	.1i	pTC.0	;14
#TP38	.1i	pNIA.08'	;14
#TP39	.1i	pTC.1	;14
#TP4	.1i	R.15	;04
#TP40	.1i	pNIA.09'	;14
#TP41	.1i	pTC.2	;14
#TP42	.1i	pNIA.10'	;14
#TP43	.1i	pTC.3	;14
#TP44	.1i	pNIA.11'	;14
#TP45	.1i	TPC.00'	;15
#TP46	.1i	TPC.01'	;15
#TP47	.1i	TPC.02'	;15
#TP48	.1i	TPC.03'	;15
#TP49	.1i	TPC.04'	;15
#TP5	.1i	Q.00	;04
#TP50	.1i	TPC.05'	;15
#TP51	.1i	TPC.06'	;15
#TP52	.1i	TPC.07'	;15
#TP53	.1i	TPC.08'	;15
#TP54	.1i	TPC.09'	;15
#TP55	.1i	TPC.10'	;15
#TP56	.1i	TPC.11'	;15
#TP57	.1i	pLink.0'	;15
#TP58	.1i	pLink.1'	;15
#TP59	.1i	pLink.2'	;15
#TP6	.1i	Q.15	;04
#TP60	.1i	pLink.3'	;15
#TP61	.1i	TCY.0	;15
#TP62	.1i	TCY.1	;15
#TP63	.1i	TCY.2	;15
#TP64	.1i	TCY.3	;15
#TP65	.1i	Ct.0	;16
#TP66	.1i	Ct.1	;16
#TP67	.1i	Ct.2	;16
#TP68	.1i	Ct=Emu	;16
#TP69	.1i	Pt=Emu	;16
#TP7	.1i	CIN-SE	;04
#TP70	.1i	Nt.0	;16
#TP71	.1i	Nt.1	;16
#TP72	.1i	Nt.2	;16
#TP73	.1i	Nt=Emu	;16
#TP74	.1i	Swc2	;16
#TP75	.1i	Swc2'	;16
#TP76	.1i	*23.7	;24
#TP77	.1i	*23.8	;24
#TP78	.1i	MesaInt	;24
#TP79	.1i	EKTrapc2'	;17
#TP8	.1i	IB.0	;07
#TP80	.1i	EKTrapc2	;17
#TP81	.1i	EKErr.0'	;17
#TP82	.1i	EKErr.1'	;17
#TP83	.1i	pEKT	;17
#TP84	.1i	pEKT	;17
#TP85	.1i	pEK0'	;17
#TP86	.1i	pEK1'	;17
#TP87	.1i	pSE	;17
#TP9	.1i	IB.1	;07
#TP91	.1i	pKR'	;17
#TP93	.1i	KernReq'	;17
#TP94	.1i	pc16'	;17
#TP95	.1i	prA.0	;20
#TP96	.1i	prA.1	;20
#TP97	.1i	prA.2	;20
#TP98	.1i	prA.3	;20
#TP99	.1i	prB.0	;20

E002	Cycle1'	;18
E003	Cycle2'	;18
E004	Cycle3'	;18
E009	ppClk	;18
E010	GND	;42
E011	AllowMDR←	;10
E015	MapRef	;12
E016	Refresh	;12
E017	Wait	;18
E020	GND	;42
E021	IOPOData←'	;11
E022	KOData←'	;11
E023	EOData←'	;11
E024	DCtlFifo←'	;11
E025	DBorder←'	;11
E026	←TStatus'	;11
E027	KCmd←'	;11
E028	POData←'	;11
E030	GND	;42
E031	←EIData'	;11
E032	←KIData'	;11
E033	←KTest'	;11
E034	←IOPIData'	;11
E035	EStrobe'	;11
E037	CSParErr	;24
E039	YIODisp.0	;13
E040	GND	;42
E041	X.00	;03
E042	X.02	;03
E043	X.04	;03
E044	X.06	;03
E045	X.08	;03
E046	X.10	;03
E047	X.12	;03
E048	X.14	;03
E049	Y.00	;03
E050	BackVCC	;42
E051	BackVCC	;42
E052	Y.02	;03
E053	Y.04	;03
E054	Y.06	;03
E055	Y.08	;03
E056	Y.10	;03
E057	Y.12	;03
E058	Y.14	;03
E059	YH.0	;06
E060	GND	;42
E061	YH.2	;06
E062	YH.4	;06
E063	YH.6	;06

E064	Pt.0	;16
E065	Pt.2	;16
E066	Disp-Proc'	;18
E070	GND	;42
E077	IOPAddr.14	;19
E080	GND	;42
E081	pCSWE.a'	;19
E082	pCSWE.c'	;19
E083	pCSWE.e'	;19
E084	IOPReq'	;16
E085	DPReq'	;16
E086	EReq'	;16
E087	KReq'	;16
E088	RefReq'	;16
E089	EORound	;16
E090	GND	;42
E091	WrTPCHigh'	;19
E092	IOPData.0	;19
E093	IOPData.2	;19
E094	IOPData.4	;19
E095	IOPData.6	;19
E096	SwTAddr	;19
E102	Click.0	;16
E103	Click.1	;16
E104	Click.2	;16
E110	GND	;42
E113	mem	;10
E114	←MStatus'	;11
E115	MCtl←'	;11
E117	IOPReset'	;26
E120	GND	;42
E121	IOPCtl←'	;11
E122	KCtl←'	;11
E123	EICtl←'	;11
E124	DCtl←'	;11
E126	EOCtl←'	;11
E127	←TIData'	;11
E128	PCtl←'	;11
E130	GND	;42
E131	←EIStatus'	;11
E132	←KStatus'	;11
E133	KStrobe'	;11
E134	←IOPStatus'	;11
E139	YIODisp.1	;13
E140	GND	;42
E141	X.01	;03
E142	X.03	;03
E143	X.05	;03
E144	X.07	;03
E145	X.09	;03
E146	X.11	;03
E147	X.13	;03
E148	X.15	;03
E149	Y.01	;03
E150	BackVCC	;42
E151	BackVCC	;42
E152	Y.03	;03
E153	Y.05	;03
E154	Y.07	;03
E155	Y.09	;03
E156	Y.11	;03
E157	Y.13	;03
E158	Y.15	;03
E159	YH.1	;06
E160	GND	;42
E161	YH.3	;06
E162	YH.5	;06
E163	YH.7	;06
E164	Pt.1	;16
E166	MemErrc3	;17
E170	GND	;42
E176	IOPAddr.13	;19
E177	IOPAddr.15	;19
E180	GND	;42
E181	pCSWE.b'	;19
E182	pCSWE.d'	;19
E183	pCSWE.f'	;19
E185	ClrDPReq'	;11
E186	ClrRefReg'	;11
E187	ClrKFlags'	;11
E188	ReadCSEn'	;25
E189	IOPWait	;18
E190	GND	;42
E191	WrTPCLow	;18
E192	IOPData.1	;19
E193	IOPData.3	;19
E194	IOPData.5	;19
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J1	.03	GND	;38
J1	.04	FPCLK	;38
J1	.05	ExtPwr	;38
J1	.06	ExtPwr	;38
J1	.07	FPI.0	;38
J1	.08	FPI.1	;38
J1	.09	FPI.2	;38
J1	.10	FPI.3	;38
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J1	.13	fY.1	;38
J1	.14	fY.2	;38
J1	.15	fY.3	;38
J1	.16	SUA.4	;38
J1	.17	SUA.5	;38
J1	.18	SUA.6	;38
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J1	.20	GND	;38
J1	.21	Bx.0	;38
J1	.22	Bx.1	;38
J1	.23	Bx.2	;38
J1	.24	Bx.3	;38
J1	.25	Bx.4	;38
J1	.26	Bx.5	;38
J1	.27	Bx.6	;38
J1	.28	Bx.7	;38

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J1          .30   Bx.8                ;38
J1          .31   Bx.9                ;38
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J1          .33   Bx.11               ;38
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*04.10: v69.12o, v84.13i  ;05

*04.11: v69.14o, v84.15i  ;05

*04.12: v69.16o, v84.17i  ;05

*04.13: v68.16o, v83.17i  ;05

*04.14: v68.14o, v83.15i  ;05

*04.15: v68.12o, v83.13i  ;05

*04.16: v68.10o, v83.11i  ;05

*04.17: v41.10o, v83.8i   ;05

*04.18: v41.12o, v83.6i   ;05

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*04.1:  v58.4o, u89.4i ;05

*04.20: v41.16o, v83.2i   ;05

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*04.3:  v58.9o, u89.12i   ;05

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*04.5:  v42.16o, v84.2i   ;05

*04.6:  v42.14o, v84.4i   ;05

*04.7:  v42.12o, v84.6i   ;05

*04.8:  v42.10o, v84.8i   ;05

*04.9:  v69.10o, v84.11i  ;05

*06.1:  v78.2o, v65.3i, v37.2o  ;07

*06.2:  v78.5o, v65.4i, v37.5o  ;07

*06.3:  v78.6o, v65.7i, v37.6o  ;07

*06.4:  v78.9o, v65.8i, v37.9o  ;07

*06.5:  v78.12o, v65.13i, v37.12o  ;07

*06.6:  v78.15o, v65.14i, v37.15o  ;07

*06.7:  v78.16o, v65.17i, v37.16o  ;07

*06.8:  v78.19o, v65.18i, v37.19o  ;07

*15.1:  v97.13o, v85.19i  ;16

*17.1:  u35.11o, v22.5i   ;18

*17.2:  u31.11o, v05.9i   ;18

*17.3:  u35.6o, v97.9i ;18

*23.10: u22.5o, u28.3i ;24

*23.11: u23.5o, u28.4i ;24

*23.12: u27.5o, u28.14i   ;24
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*23.14: u25.5o, u28.8i ;24

*23.15: u26.5o, u28.13i   ;24

*23.16: u85.14o, u35.9i   ;24

*23.1:  #TP202.1i, u28.6o, u29.1i  ;24

*23.2:  #TP203.1i, u28.9o, u29.2i  ;24

*23.3:  #TP204.1i, u28.12o, u29.3i ;24

*23.4:  #TP200.1i, u28.2o, u29.16i ;24

*23.5:  #TP201.1i, u28.5o, u29.17i ;24

*23.6:  #TP205.1i, u28.15o, u29.4i ;24

*23.7:  #TP76.1i, u29.11o, u64.14i ;24

*23.8:  #TP77.1i, u35.8o, u64.17i  ;24

*23.9:  u29.13o, u35.10i  ;24

*25.1:  u04.5o, u13.6i ;26

*25.2:  u04.6o, u13.11i   ;26

*25.3:  u04.7o, u13.14i   ;26

*25.4:  u04.4o, u13.3i ;26

*29.1:  u69.3o, v56.11i   ;30

*29.2:  v01.31o, u64.18i  ;30

*29.3:  v01.15o, v33.13i  ;30

*29.4:  u69.8o, v34.11i   ;30

*29.5:  u87.8o, u69.1i ;30

*30.1:  u69.11o, u14.10i  ;31

*35.1:  v40.2o, u19.2i ;36

*35.2:  v40.5o, u19.4i ;36

*35.3:  v40.6o, u19.6i ;36

*35.4:  v40.9o, u19.8i ;36

*35.5:  v40.19o, u19.11i  ;36

*35.6:  v40.16o, u19.13i  ;36

*35.7:  v40.15o, u19.15i  ;36

*35.8:  v40.12o, u19.17i  ;36

12BitCarry:   u81.29i  ;03
12BitCarry:   u90.9o, #TP1.1i   ;04

12BitGen': u80.32o  ;03
12BitGen': u90.14i  ;04

12BitProp':   u80.35o  ;03
12BitProp':   u90.15i  ;04

18.1:   v51.2i, v52.2i, v53.2i  ;19
18.1:   v54.2i, v55.2i, v72.3i
18.1:   v70.18o, v50.2i

18.2:   v51.4i, v52.4i, v53.4i  ;19
18.2:   v54.4i, v55.4i, v72.4i
18.2:   v73.2i, v70.16o, v50.4i

18.3:   v51.6i, v52.6i, v53.6i  ;19
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18.3:   v73.4i, v70.14o, v50.6i

18.4:   v51.8i, v52.8i, v53.8i  ;19
18.4:   v54.8i, v55.8i, v72.8i
18.4:   v73.6i, v70.12o, v50.8i

18.5:   v51.17i, v52.17i, v53.17i  ;19
18.5:   v54.17i, v55.17i, v72.13i
18.5:   v73.8i, v70.3o, v50.17i

18.6:   v51.15i, v52.15i, v53.15i  ;19
18.6:   v54.15i, v55.15i, v72.14i
18.6:   v73.17i, v70.5o, v50.15i

18.7:   v51.13i, v52.13i, v53.13i  ;19
18.7:   v54.13i, v55.13i, v72.17i
18.7:   v73.15i, v70.7o, v50.13i

18.8:   v51.11i, v52.11i, v53.11i  ;19
18.8:   v54.11i, v55.11i, v72.18i
18.8:   v73.13i, v70.9o, v50.11i

4BitCarry: v08.29i  ;03
4BitCarry: u90.12o  ;04
4BitCarry: v07.12i  ;13

4BitGen':  v09.32o  ;03
4BitGen':  u90.3i   ;04

4BitProp': v09.35o  ;03
4BitProp': u90.4i   ;04

8BitCarry: u80.29i  ;03
8BitCarry: u50.2i, u90.11o   ;04
8BitCarry: v07.15i  ;13
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8BitGen':  v08.32o  ;03
8BitGen':  u90.1i   ;04

8BitProp': v08.35o  ;03
8BitProp': u90.2i   ;04

aD.0':  u63.15i, u87.2o, u62.1i ;04

aD.0:   u81.7i   ;03
aD.0:   u80.7i   ;03
aD.0:   v09.7i   ;03
aD.0:   v08.7i   ;03
aD.0:   u87.1i, u62.5i, u63.1i  ;04
aD.0:   v16.12o  ;10

aD.1:   u81.5i   ;03
aD.1:   u80.5i   ;03
aD.1:   v09.5i   ;03
aD.1:   v08.5i   ;03
aD.1:   u63.2i   ;04
aD.1:   v16.15o  ;10

aF.0:   u81.27i  ;03
aF.0:   u80.27i  ;03
aF.0:   v09.27i  ;03
aF.0:   v08.27i  ;03
aF.0:   u67.2o   ;10

aFh.1:  u81.28i  ;03
aFh.1:  u80.28i  ;03
aFh.1:  u99.10o  ;10

aFh.2:  u81.26i  ;03
aFh.2:  u80.26i  ;03
aFh.2:  u99.15o  ;10

aFl.1:  v08.28i  ;03
aFl.1:  v09.28i  ;03
aFl.1:  v16.16o  ;10

aFl.2:  v08.26i  ;03
aFl.2:  v09.26i  ;03
aFl.2:  u50.1i   ;04
aFl.2:  v16.19o  ;10

AllowMDR←: u61.3i, u43.3i ;07
AllowMDR←: v94.5o, E11 ;10

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AltUAddr': u18.7o   ;11

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AlwaysClk-a:  u99.9i   ;10
AlwaysClk-a:  u30.11i  ;10
AlwaysClk-a:  v21.2o   ;18
AlwaysClk-a:  v02.11i  ;29
AlwaysClk-a:  u14.11i  ;31

AlwaysClk-b:  u91.9i, u89.9i ;05

AlwaysClk-b:  u67.11i  ;10
AlwaysClk-b:  v21.4o   ;18
AlwaysClk-b:  u13.9i   ;26
AlwaysClk-b:  u47.9i   ;26
AlwaysClk-b:  u05.2i   ;28
AlwaysClk-b:  u28.11i  ;29

AlwaysClk-c:  v16.11i  ;10
AlwaysClk-c:  v17.11i  ;10
AlwaysClk-c:  v76.11i  ;15
AlwaysClk-c:  v62.11i  ;15
AlwaysClk-c:  v21.6o   ;18
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AlwaysClk-c:  v94.11i  ;29
AlwaysClk-c:  v95.9i   ;38

aSh.0:  u81.14i  ;03
aSh.0:  u80.14i  ;03
aSh.0:  v17.19o  ;10

aSh.1:  u81.13i  ;03
aSh.1:  u80.13i  ;03
aSh.1:  u99.2o   ;10

aSh.2:  u81.12i  ;03
aSh.2:  u80.12i  ;03
aSh.2:  u99.7o   ;10

aSl.0:  v08.14i  ;03
aSl.0:  v09.14i  ;03
aSl.0:  v17.12o  ;10

aSl.1:  v08.13i  ;03
aSl.1:  v09.13i  ;03
aSl.1:  v17.15o  ;10

aSl.2:  v08.12i  ;03
aSl.2:  v09.12i  ;03
aSl.2:  v17.16o  ;10

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Bank.0: u04.3i, v19.13o   ;26
Bank.0: u05.6i   ;28

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Bank.1: u04.2i, v19.14o   ;26
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Bank←': v19.9i   ;26

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Bx.0:   u21.2i   ;40
Bx.0:   u21.20i  ;40
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Bx.0:   u21.65o  ;40
Bx.0:   u20.65o  ;40
Bx.0:   u20.20i  ;40
Bx.0:   u20.2i   ;40

Bx.10:  v24.16o, J1.32 ;38
Bx.10:  u21.12i  ;40
Bx.10:  u21.30i  ;40
Bx.10:  u21.54o  ;40
Bx.10:  u20.54o  ;40
Bx.10:  u20.30i  ;40
Bx.10:  u20.12i  ;40

Bx.11:  v24.15o, J1.33 ;38
Bx.11:  u21.13i  ;40
Bx.11:  u21.31i  ;40
Bx.11:  u21.53o  ;40
Bx.11:  u20.53o  ;40
Bx.11:  u20.31i  ;40
Bx.11:  u20.13i  ;40

Bx.12:  v24.14o, J1.34 ;38
Bx.12:  u21.15i  ;40
Bx.12:  u21.32i  ;40
Bx.12:  u21.52o  ;40
Bx.12:  u20.52o  ;40
Bx.12:  u20.32i  ;40
Bx.12:  u20.15i  ;40

Bx.13:  v24.13o, J1.35 ;38
Bx.13:  u21.16i  ;40
Bx.13:  u21.34i  ;40
Bx.13:  u21.50o  ;40
Bx.13:  u20.50o  ;40
Bx.13:  u20.34i  ;40
Bx.13:  u20.16i  ;40

Bx.14:  v24.12o, J1.36 ;38
Bx.14:  u21.18i  ;40
Bx.14:  u21.49o  ;40
Bx.14:  u21.36o  ;40
Bx.14:  u20.36o  ;40
Bx.14:  u20.49o  ;40
Bx.14:  u20.18i  ;40

Bx.15:  v24.11o, J1.37 ;38
Bx.15:  u21.19i  ;40
Bx.15:  u21.48o  ;40
Bx.15:  u21.38o  ;40
Bx.15:  u20.38o  ;40
Bx.15:  u20.48o  ;40
Bx.15:  u20.19i  ;40

Bx.1:   v06.17o, J1.22 ;38
Bx.1:   u21.3i   ;40
Bx.1:   u21.21i  ;40
Bx.1:   u21.64o  ;40
Bx.1:   u20.64o  ;40
Bx.1:   u20.21i  ;40

Bx.1:   u20.3i   ;40

Bx.2:   v06.16o, J1.23 ;38
Bx.2:   u21.4i   ;40
Bx.2:   u21.22i  ;40
Bx.2:   u21.63o  ;40
Bx.2:   u20.63o  ;40
Bx.2:   u20.22i  ;40
Bx.2:   u20.4i   ;40

Bx.3:   v06.15o, J1.24 ;38
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Bx.3:   u21.23i  ;40
Bx.3:   u21.62o  ;40
Bx.3:   u20.62o  ;40
Bx.3:   u20.23i  ;40
Bx.3:   u20.5i   ;40

Bx.4:   v06.14o, J1.25 ;38
Bx.4:   u21.6i   ;40
Bx.4:   u21.24i  ;40
Bx.4:   u21.61o  ;40
Bx.4:   u20.61o  ;40
Bx.4:   u20.24i  ;40
Bx.4:   u20.6i   ;40

Bx.5:   v06.13o, J1.26 ;38
Bx.5:   u21.7i   ;40
Bx.5:   u21.25i  ;40
Bx.5:   u21.60o  ;40
Bx.5:   u20.60o  ;40
Bx.5:   u20.25i  ;40
Bx.5:   u20.7i   ;40

Bx.6:   v06.12o, J1.27 ;38
Bx.6:   u21.8i   ;40
Bx.6:   u21.26i  ;40
Bx.6:   u21.59o  ;40
Bx.6:   u20.59o  ;40
Bx.6:   u20.26i  ;40
Bx.6:   u20.8i   ;40

Bx.7:   v06.11o, J1.28 ;38
Bx.7:   u21.9i   ;40
Bx.7:   u21.27i  ;40
Bx.7:   u21.57o  ;40
Bx.7:   u20.57o  ;40
Bx.7:   u20.27i  ;40
Bx.7:   u20.9i   ;40

Bx.8:   v24.18o, J1.30 ;38
Bx.8:   u21.10i  ;40
Bx.8:   u21.28i  ;40
Bx.8:   u21.56o  ;40
Bx.8:   u20.56o  ;40
Bx.8:   u20.28i  ;40
Bx.8:   u20.10i  ;40

Bx.9:   v24.17o, J1.31 ;38
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Bx.9:    u21.11i  ;40
Bx.9:    u21.29i  ;40
Bx.9:    u21.55o  ;40
Bx.9:    u20.55o  ;40
Bx.9:    u20.29i  ;40
Bx.9:    u20.11i  ;40

Byte':   v46.1i   ;09
Byte':   u34.8o   ;12

Byte:    v95.10o  ;38
Byte:    u46.2i   ;38
Byte:    u46.4i   ;38
Byte:    v32.5i   ;38

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C2Clk:   v05.11o  ;18

CarryOut:  u81.33o  ;03
CarryOut:  u63.6i   ;04
CarryOut:  v07.14i  ;13

CIN-SE-wrSU': u62.12i  ;04
CIN-SE-wrSU': u72.1i   ;05
CIN-SE-wrSU': u68.3o   ;10

CIN-SE-wrSU:  u68.2o   ;10
CIN-SE-wrSU:  v04.1i   ;18

CIN-SE: v09.29i  ;03
CIN-SE: u90.13i  ;04
CIN-SE: u63.12i  ;04
CIN-SE: u63.5i, u63.4i ;04
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CIN←pc16:  u72.11o  ;12
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CIN←pc16X':   u62.13i  ;04
CIN←pc16X':   u15.11o  ;11
CIN←pc16X':   u72.12i  ;12

CIN←pc16Z':   u18.12o  ;11
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Click.1:   E103, u73.17i  ;16

Click.2:   E104, u73.1i   ;16
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ClrIntErr':   u45.3i   ;17
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ClrKFlags':   v57.7o, E187   ;11

ClrRefReg':   v57.9o, E186   ;11

CSA.00':   v25.16i  ;20
CSA.00':   v10.16i  ;20
CSA.00':   v27.16i  ;20
CSA.00':   v12.16i  ;20
CSA.00':   v14.16i  ;20
CSA.00':   v29.16i  ;20
CSA.00':   v26.16i  ;20
CSA.00':   v11.16i  ;20
CSA.00':   v13.16i  ;20
CSA.00':   v28.16i  ;20
CSA.00':   v30.16i  ;20
CSA.00':   v15.16i  ;20
CSA.00':   u36.16i  ;21
CSA.00':   u55.16i  ;21
CSA.00':   u57.16i  ;21
CSA.00':   u38.16i  ;21
CSA.00':   u40.16i  ;21
CSA.00':   u59.16i  ;21
CSA.00':   u56.16i  ;21
CSA.00':   u37.16i  ;21
CSA.00':   u39.16i  ;21
CSA.00':   u58.16i  ;21
CSA.00':   u60.16i  ;21
CSA.00':   u41.16i  ;21
CSA.00':   u74.16i  ;22
CSA.00':   u92.16i  ;22
CSA.00':   u94.16i  ;22
CSA.00':   u76.16i  ;22
CSA.00':   u78.16i  ;22
CSA.00':   u96.16i  ;22
CSA.00':   u93.16i  ;22
CSA.00':   u75.16i  ;22
CSA.00':   u77.16i  ;22
CSA.00':   u95.16i  ;22
CSA.00':   u97.16i  ;22
CSA.00':   u79.16i  ;22
CSA.00':   u66.12o  ;27
CSA.00':   u05.12o  ;28

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CSParErr:  u45.17i  ;17
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CSParErr:  u01.15o  ;28

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CSWE.f':   u97.11i  ;22

Ct.0:   u49.2o, #TP65.1i  ;16
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SP.1:   v01.3o, v34.17i   ;30

SP.2:   v01.4o, v34.14i   ;30

SP.3:   v01.5o, v34.13i   ;30

SP.4:   v01.39o, v34.8i   ;30

SP.5:   v01.38o, v34.7i   ;30

SP.6:   v01.37o, v34.4i   ;30

SP.7:   v01.36o, v34.3i   ;30

SpActive:  u69.9i   ;30
SpActive:  u85.10o  ;32

StackErr:  u64.9o, u45.1i ;17

stackP.0:  u17.12i, v66.2o, v60.17i   ;06
stackP.0:  u16.1i   ;17

stackP.1:  v66.7o, u17.14i, v60.15i   ;06
stackP.1:  u16.2i   ;17

stackP.2:  v66.10o, u17.3i, v60.13i   ;06
stackP.2:  u16.3i   ;17

stackP.3:  v66.15o, u17.5i, v60.11i   ;06
stackP.3:  u16.4i   ;17

stackP←':  v66.1i   ;06
stackP←':  u52.10o  ;11

SUA.0:  u91.2o   ;05
SUA.0:  v42.7i   ;05
SUA.0:  v69.7i   ;05
SUA.0:  v41.7i   ;05
SUA.0:  v68.7i   ;05

SUA.1:  u91.7o   ;05
SUA.1:  v42.6i   ;05
SUA.1:  v69.6i   ;05
SUA.1:  v41.6i   ;05
SUA.1:  v68.6i   ;05

SUA.2:  u91.10o  ;05
SUA.2:  v42.5i   ;05
SUA.2:  v69.5i   ;05
SUA.2:  v41.5i   ;05
SUA.2:  v68.5i   ;05

SUA.3:  u91.15o  ;05
SUA.3:  v42.21i  ;05
SUA.3:  v69.21i  ;05
SUA.3:  v41.21i  ;05
SUA.3:  v68.21i  ;05

SUA.4:  u89.2o   ;05
SUA.4:  v42.1i   ;05
SUA.4:  v69.1i   ;05
SUA.4:  v41.1i   ;05
SUA.4:  v68.1i   ;05
SUA.4:  J1.16 ;38
SUA.4:  u21.41o  ;40
SUA.4:  u20.41o  ;40

SUA.5:  u89.7o   ;05
SUA.5:  v42.2i   ;05
SUA.5:  v69.2i   ;05
SUA.5:  v41.2i   ;05
SUA.5:  v68.2i   ;05
SUA.5:  J1.17 ;38
SUA.5:  u21.43o  ;40
SUA.5:  u20.43o  ;40

SUA.6:  u89.10o  ;05
SUA.6:  v42.3i   ;05
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SUA.6:  v69.3i   ;05
SUA.6:  v41.3i   ;05
SUA.6:  v68.3i   ;05
SUA.6:  J1.18 ;38
SUA.6:  u21.44o  ;40
SUA.6:  u20.44o  ;40

SUA.7:  u89.15o  ;05
SUA.7:  v42.4i   ;05
SUA.7:  v69.4i   ;05
SUA.7:  v41.4i   ;05
SUA.7:  v68.4i   ;05
SUA.7:  J1.19 ;38
SUA.7:  u21.45o  ;40
SUA.7:  u20.45o  ;40

Swc2':  #TP75.1i, v63.11o, v02.4i  ;16

Swc2:   #TP74.1i, v63.9o, v02.3i   ;16
Swc2:   u82.1i, u47.1i, v31.1i  ;26

Swc3':  v91.13i, v91.12i  ;14
Swc3':  v92.13i, v92.12i  ;14
Swc3':  v93.13i, v93.12i  ;14
Swc3':  v90.13i, v90.12i  ;14
Swc3':  v02.5o   ;16

Swc3:   v91.9i   ;14
Swc3:   v92.9i   ;14
Swc3:   v93.9i   ;14
Swc3:   v90.9i   ;14
Swc3:   v02.2o   ;16
Swc3:   u01.4i   ;28

SwTAddr':  v73.1i, v72.1i, E196 ;19
SwTAddr':  v73.19i

SwTAddr:   v76.1i   ;15
SwTAddr:   v62.1i   ;15
SwTAddr:   u73.8i   ;16
SwTAddr:   v97.12i  ;16
SwTAddr:   E96   ;19

TC.0:   v91.10i  ;14
TC.0:   v94.6o   ;15

TC.1:   v92.10i  ;14
TC.1:   v94.9o   ;15

TC.2:   v90.10i  ;14
TC.2:   v94.12o  ;15

TC.3:   v93.10i  ;14
TC.3:   v94.15o  ;15

TCWaitc1': v94.19o  ;18
TCWaitc1': u31.12i  ;18

TCX.0:  v62.12o, v45.12i  ;15

TCX.1:  v62.15o, v45.10i  ;15

TCX.2:  v62.16o, v45.6i   ;15

TCX.3:  v62.19o, v45.4i   ;15

TCY.0:  v45.11o, #TP61.1i, v94.7i  ;15

TCY.1:  v45.9o, #TP62.1i, v94.8i   ;15

TCY.2:  v45.7o, #TP63.1i, v94.13i  ;15

TCY.3:  #TP64.1i, v45.5o, v94.14i  ;15

TPC.00':   v74.11o, #TP45.1i ;15
TPC.00':   u08.13i  ;25
TPC.00':   u47.4i   ;26

TPC.01':   v74.9o, #TP46.1i  ;15
TPC.01':   u12.13i  ;25
TPC.01':   u47.5i   ;26

TPC.02':   v74.7o, #TP47.1i  ;15
TPC.02':   u09.13i  ;25
TPC.02':   u47.12i  ;26

TPC.03':   v74.5o, #TP48.1i  ;15
TPC.03':   u54.13i  ;25
TPC.03':   u47.13i  ;26

TPC.04':   v75.11o, #TP49.1i ;15
TPC.04':   u06.12i  ;25
TPC.04':   u82.4i   ;26

TPC.05':   v75.9o, #TP50.1i  ;15
TPC.05':   u10.12i  ;25
TPC.05':   u82.5i   ;26

TPC.06':   v75.7o, #TP51.1i  ;15
TPC.06':   u07.12i  ;25
TPC.06':   u82.12i  ;26

TPC.07':   v75.5o, #TP52.1i  ;15
TPC.07':   u11.12i  ;25
TPC.07':   u82.13i  ;26

TPC.08':   v44.11o, #TP53.1i ;15
TPC.08':   u08.12i  ;25
TPC.08':   v31.4i   ;26

TPC.09':   v44.9o, #TP54.1i  ;15
TPC.09':   u12.12i  ;25
TPC.09':   v31.5i   ;26

TPC.10':   v44.7o, #TP55.1i  ;15
TPC.10':   u09.12i  ;25
TPC.10':   v31.12i  ;26
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TPC.11':   v44.5o, #TP56.1i  ;15
TPC.11':   u54.12i  ;25
TPC.11':   v31.13i  ;26

TTLHigh-a: u68.1i   ;10
TTLHigh-a: u99.14i, u99.11i  ;10
TTLHigh-a: u99.6i, u99.3i
TTLHigh-a: u48.6i   ;14
TTLHigh-a: u88.5i   ;27
TTLHigh-a: v95.11i, v95.3i   ;38

TTLHigh-b: u88.6i   ;27
TTLHigh-b: v01.11i  ;30

TTLHigh-c: u88.7i   ;27
TTLHigh-c: u14.13i  ;31
TTLHigh-c: u14.4i, u14.1i ;32

VCC:    v08.10i, u80.10i, u81.10i  ;03
VCC:    v09.10i
VCC:    u88.15o, u88.14o, u88.13o  ;27
VCC:    u88.12o, u88.11o, u88.10o
VCC:    u88.9o, u88.16o
VCC:    #R2.1o   ;27
VCC:    #R1.1o   ;27
VCC:    u01.20o  ;28
VCC:    v01.40i  ;30
VCC:    f01.1i   ;36
VCC:    u51.16o  ;36
VCC:    #C28.2i, #C93.2i, #C51.2i  ;37
VCC:    #C90.2i, #C77.2i, #C63.2i
VCC:    #C30.2i, #C15.2i, #C14.2i
VCC:    #C13.2i, #C146.2i, #C132.2i
VCC:    #C144.2i, #C143.2i, #C142.2i
VCC:    #C4.2i, #C5.2i, #C7.2i
VCC:    #C31.2i, #C6.2i, #C8.2i
VCC:    #C32.2i, #C29.2i, #C10.2i
VCC:    #C16.2i, #C18.2i, #C19.2i
VCC:    #C20.2i, #C50.2i, #C9.2i
VCC:    #C119.2i, #C118.2i, #C117.2i
VCC:    #C116.2i, #C115.2i, #C114.2i
VCC:    #C53.2i, #C52.2i, #C44.2i
VCC:    #C46.2i, #C75.2i, #C73.2i
VCC:    #C72.2i, #C89.2i, #C3.2i
VCC:    #C68.2i, #C67.2i, #C66.2i
VCC:    #C86.2i, #C85.2i, #C84.2i
VCC:    #C83.2i, #C82.2i, #C81.2i
VCC:    #C104.2i, #C103.2i, #C102.2i
VCC:    #C101.2i, #C100.2i, #C99.2i
VCC:    #C42.2i, #C41.2i, #C40.2i
VCC:    #C39.2i, #C38.2i, #C37.2i
VCC:    #C59.2i, #C58.2i, #C57.2i
VCC:    #C56.2i, #C55.2i, #C54.2i
VCC:    #C71.2i, #C70.2i, #C69.2i
VCC:    #C123.2i, #C45.2i, #C95.2i
VCC:    #C76.2i, #C97.2i, #C91.2i
VCC:    #C92.2i, #C105.2i, #C78.2i
VCC:    #C27.2i, #C26.2i, #C25.2i
VCC:    #C24.2i, #C23.2i, #C22.2i

VCC:    #C147.2i, #C141.2i, #C148.2i
VCC:    #C150.2i, #C152.2i, #C151.2i
VCC:    #C137.2i, #C136.2i, #C135.2i
VCC:    #C138.2i, #C139.2i, #C140.2i
VCC:    #C49.2i, #C125.2i, #C126.2i
VCC:    u21.14i  ;40
VCC:    u21.58o  ;40
VCC:    u21.37o  ;40
VCC:    u20.37o  ;40
VCC:    u20.58o  ;40
VCC:    u20.14i  ;40
VCC:    #C64.2i, #C1.2i, #C62.2i   ;41
VCC:    #C60.2i, #C111.2i, #C36.2i
VCC:    #C33.2i, #C35.2i, #C34.2i
VCC:    #C149.2i, #C21.2i, #C17.2i
VCC:    #C48.2i, #C107.2i, #C74.2i
VCC:    #C113.2i, #C98.2i, #C153.2i
VCC:    #C43.2i, #C80.2i, #C79.2i
VCC:    #C96.2i, #C106.2i, #C94.2i
VCC:    #C87.2i, #C88.2i, #C61.2i
VCC:    #C65.2i, #C47.2i, #C145.2i
VCC:    #C133.2i, #C129.2i, #C130.2i
VCC:    #C127.2i, #C134.2i, #C122.2i
VCC:    #C110.2i, #C120.2i, #C121.2i
VCC:    #C112.2i, #C124.2i, #C131.2i
VCC:    #C108.2i, #C128.2i, #C109.2i
VCC:    #C2.2i, #C157.2i, #C158.2i
VCC:    #C154.2i, #C155.2i
VCC:    u42.20o, u02.16o  ;42
VCC:    #C11.1o, #C12.1o, f02.1i   ;42

Wait:   v38.3i   ;07
Wait:   v63.5i   ;16
Wait:   v97.6i, u35.4i, v20.8o, E17   ;18
Wait:   v86.15i  ;28

Waitc1':   v02.17i, u70.8o, v20.11i   ;18

Waitc2':   v02.18i, v02.16o, v20.10i  ;18

Waitc3':   v94.18i, v02.19o, v20.9i   ;18

WaitClk:   u81.15i, u80.15i  ;03
WaitClk:   v08.15i, v09.15i  ;03
WaitClk:   v66.9i   ;06
WaitClk:   v21.8o   ;18
WaitClk:   v19.2i   ;26
WaitClk:   u64.11i  ;29
WaitClk:   v33.11i, u85.9i   ;32

WaitPin':  v86.5o, u01.3i ;28

WPort:  v40.11i, u83.11i, u69.6o   ;36

WrIBFront: v65.11i  ;07
WrIBFront: v04.11o  ;18

WriteIB:   v37.11i, v78.11i  ;07
WriteIB:   v97.10o  ;18
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WriteLink':   u84.3i   ;15
WriteLink':   v04.6o   ;18

WriteRH':  v48.3i, v47.3i ;06
WriteRH':  v04.8o   ;18

WriteSU':  v42.20i  ;05
WriteSU':  v69.20i  ;05
WriteSU':  v41.20i  ;05
WriteSU':  v68.20i  ;05
WriteSU':  v04.3o   ;18

WriteTC':  v45.3i   ;15
WriteTC':  v05.8o   ;18

WriteTPC': v75.3i, v74.3i, v44.3i  ;15
WriteTPC': v22.8o   ;18

WrTPCHigh':   E91, v72.11i   ;19

WrTPCLow:  v22.9i, E191, v22.10i   ;18

X.00:   E41, u81.22i   ;03
X.00:   v84.18o  ;05
X.00:   v37.3i   ;07
X.00:   v39.3o   ;08
X.00:   v88.15o  ;08
X.00:   v49.14i  ;13
X.00:   v36.18o  ;36
X.00:   v06.2i   ;38

X.01:   E141, u81.23i  ;03
X.01:   v84.16o  ;05
X.01:   v37.4i   ;07
X.01:   v39.5o   ;08
X.01:   v82.15o  ;08
X.01:   v36.16o  ;36
X.01:   v06.3i   ;38

X.02:   E42, u81.24i   ;03
X.02:   v84.14o  ;05
X.02:   v37.7i   ;07
X.02:   v39.7o   ;08
X.02:   v81.15o  ;08
X.02:   v36.14o  ;36
X.02:   v06.4i   ;38

X.03:   E142, u81.25i  ;03
X.03:   v84.12o  ;05
X.03:   v37.8i   ;07
X.03:   v39.9o   ;08
X.03:   v80.15o  ;08
X.03:   v36.12o  ;36
X.03:   v06.5i   ;38

X.04:   E43, u80.22i   ;03
X.04:   v84.3o   ;05
X.04:   v37.13i  ;07
X.04:   v61.3o   ;08
X.04:   v88.14o  ;08
X.04:   v23.14i  ;13
X.04:   v36.3o   ;36
X.04:   v06.6i   ;38

X.05:   E143, u80.23i  ;03
X.05:   v84.5o   ;05
X.05:   v37.14i  ;07
X.05:   v61.5o   ;08
X.05:   v82.14o  ;08
X.05:   v36.5o   ;36
X.05:   v06.7i   ;38

X.06:   E44, u80.24i   ;03
X.06:   v84.7o   ;05
X.06:   v37.17i  ;07
X.06:   v61.7o   ;08
X.06:   v81.14o  ;08
X.06:   v36.7o   ;36
X.06:   v06.8i   ;38

X.07:   E144, u80.25i  ;03
X.07:   v84.9o   ;05
X.07:   v37.18i  ;07
X.07:   v61.9o   ;08
X.07:   v80.14o  ;08
X.07:   v36.9o   ;36
X.07:   v06.9i   ;38

X.08:   E45, v08.22i   ;03
X.08:   v83.18o  ;05
X.08:   v48.12i  ;06
X.08:   v39.18o  ;06
X.08:   v78.3i   ;07
X.08:   v88.12o  ;08
X.08:   v59.4o   ;09
X.08:   v46.4o   ;09
X.08:   v60.18o  ;09
X.08:   v23.13i  ;13
X.08:   v34.2o   ;30
X.08:   v35.18o  ;36
X.08:   v03.18o  ;36
X.08:   v24.2i   ;38

X.09:   E145, v08.23i  ;03
X.09:   v83.16o  ;05
X.09:   v48.10i  ;06
X.09:   v39.16o  ;06
X.09:   v78.4i   ;07
X.09:   v82.12o  ;08
X.09:   v59.7o   ;09
X.09:   v46.7o   ;09
X.09:   v60.16o  ;09
X.09:   v23.15i  ;13
X.09:   v34.5o   ;30
X.09:   v35.16o  ;36
X.09:   v03.16o  ;36
X.09:   v24.3i   ;38
```

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X.10:   E46, v08.24i   ;03
X.10:   v83.14o  ;05
X.10:   v39.14o  ;06
X.10:   v48.6i   ;06
X.10:   v78.7i   ;07
X.10:   v81.12o  ;08
X.10:   v59.9o   ;09
X.10:   v46.9o   ;09
X.10:   v60.14o  ;09
X.10:   v49.15i  ;13
X.10:   v34.6o   ;30
X.10:   v35.14o  ;36
X.10:   v03.14o  ;36
X.10:   v24.4i   ;38

X.11:   E146, v08.25i  ;03
X.11:   v83.12o  ;05
X.11:   v39.12o  ;06
X.11:   v48.4i   ;06
X.11:   v78.8i   ;07
X.11:   v80.12o  ;08
X.11:   v59.12o  ;09
X.11:   v46.12o  ;09
X.11:   v60.12o  ;09
X.11:   v07.13i  ;13
X.11:   v34.9o   ;30
X.11:   v35.12o  ;36
X.11:   v03.12o  ;36
X.11:   v24.5i   ;38

X.12:   E47, v09.22i   ;03
X.12:   v83.3o   ;05
X.12:   v60.3o, v61.18o   ;06
X.12:   v47.12i  ;06
X.12:   v78.13i  ;07
X.12:   v88.11o  ;08
X.12:   v64.4o   ;09
X.12:   v85.18o  ;09
X.12:   v77.2i   ;13
X.12:   v34.12o  ;30
X.12:   v35.3o   ;36
X.12:   v03.3o   ;36
X.12:   v24.6i   ;38

X.13:   E147, v09.23i  ;03
X.13:   v83.5o   ;05
X.13:   v60.5o, v61.16o   ;06
X.13:   v47.10i  ;06
X.13:   v78.14i  ;07
X.13:   v82.11o  ;08
X.13:   v64.7o   ;09
X.13:   v85.16o  ;09
X.13:   v77.5i   ;13
X.13:   v34.15o  ;30
X.13:   v35.5o   ;36
X.13:   v03.5o   ;36
X.13:   v24.7i   ;38

X.14:   E48, v09.24i   ;03
X.14:   v83.7o   ;05
X.14:   v60.7o, v61.14o   ;06
X.14:   v47.6i   ;06
X.14:   v78.17i  ;07
X.14:   v81.11o  ;08
X.14:   v64.9o   ;09
X.14:   v85.14o  ;09
X.14:   v23.4i   ;13
X.14:   v34.16o  ;30
X.14:   v35.7o   ;36
X.14:   v03.7o   ;36
X.14:   v24.8i   ;38

X.15:   E148, v09.25i  ;03
X.15:   v83.9o   ;05
X.15:   v60.9o, v61.12o   ;06
X.15:   v47.4i   ;06
X.15:   v78.18i  ;07
X.15:   v80.11o  ;08
X.15:   v64.12o  ;09
X.15:   v85.12o  ;09
X.15:   v49.4i   ;13
X.15:   v49.13i  ;13
X.15:   v34.19o  ;30
X.15:   v35.9o   ;36
X.15:   v03.9o   ;36
X.15:   v24.9i   ;38

XBus←IB':  v38.2i   ;07
XBus←IB':  v59.15i  ;09
XBus←IB':  v64.15i  ;09
XBus←IB':  u33.6o   ;12

XBus←SU':  u87.11i, u72.3o, v83.1i ;05
XBus←SU':  v84.1i

XBus←SU:   u87.10o, v83.19i, v84.19i  ;05

XByte': u53.8o, u46.10i   ;12

Xhigh←0:   v39.19i, v61.19i  ;08
Xhigh←0:   u46.8o   ;12

Y.00:   u81.39o, E49   ;03
Y.00:   v42.15i  ;05
Y.00:   v88.4i   ;08
Y.00:   u83.3i   ;36

Y.01:   u81.38o, E149  ;03
Y.01:   v42.13i  ;05
Y.01:   v82.4i   ;08
Y.01:   u83.4i   ;36

Y.02:   u81.37o, E52   ;03
Y.02:   v42.11i  ;05
Y.02:   v81.4i   ;08
Y.02:   u83.7i   ;36
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Y.03:   u81.36o, E152  ;03
Y.03:   v42.9i   ;05
Y.03:   v80.4i   ;08
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