High Speed Input/Output Board

Logic Drawings

HSIO Board

1. HSIO0 - this page
2. pHSIO01 - drawings of fuses
3. HSIO02.sily - Display controller parts list
4. HSIO03.sily - Display controller parts list
5. HSIO04.sily - Disk controller parts list
6. HSIO05.sily - Disk controller parts list
7. HSIO06.sily - Stichweld layout
8. HSIO07.sily - proposed PWB layout

Display Controller

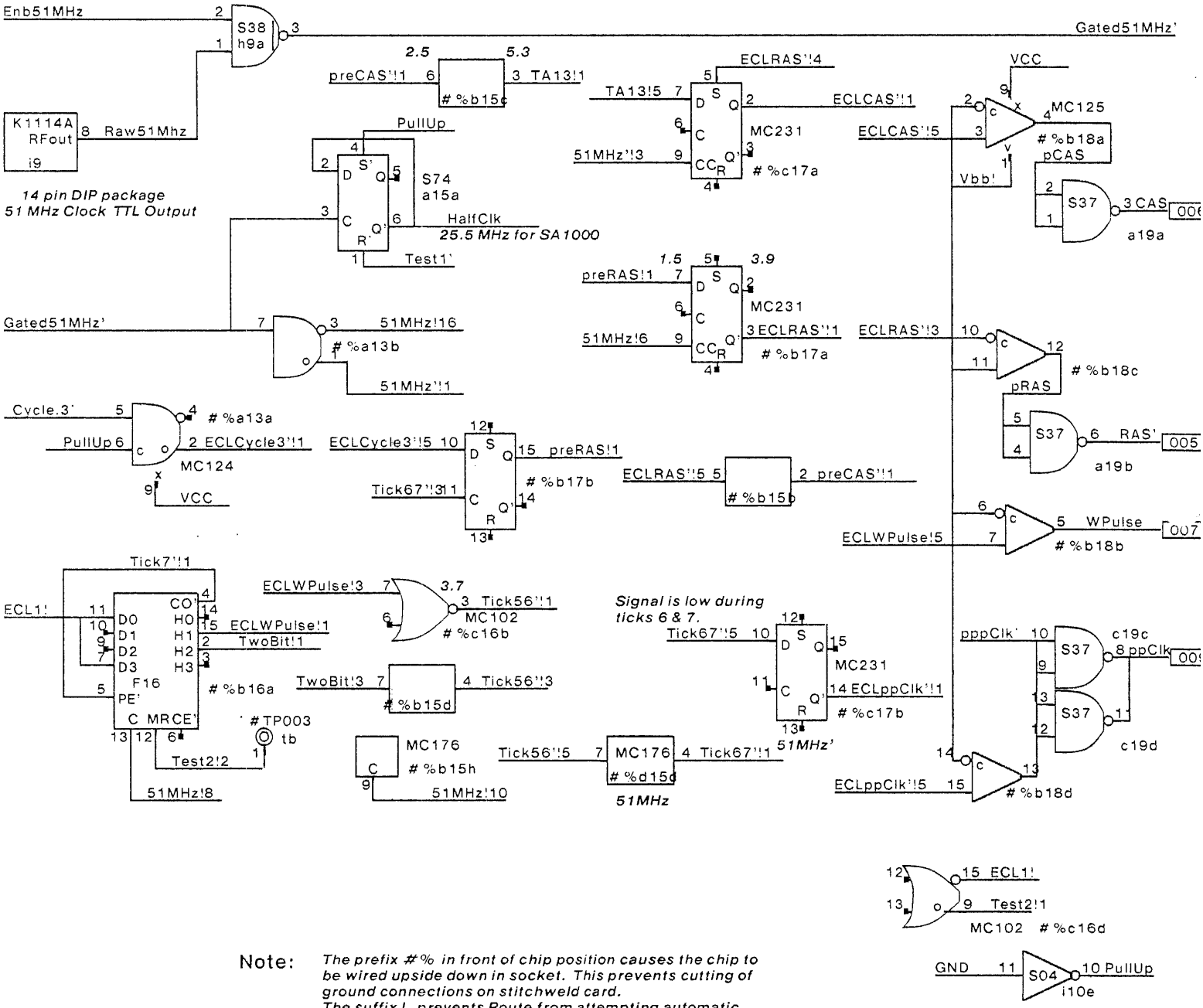
1. HSIO22 - 51 MHz Clock Dividers and ECL Terminators
2. HSIO23 - Cycles, Clicks and Display counter
3. HSIO24 - Display Output Machine and Control register
4. HSIO25 - Data FIFO and Border Register
5. HSIO26 - Control FIFO Data Path
6. HSIO27 - Read Machine; Word Counter & End Conditions
7. HSIO28 - LCAS & LRAS' Generation
8. (p|s)HSIO29 - Discretes, Connectors

Disk Controller

8. HSIO47 - Control and Write Data registers
9. HSIO48 - Status / Test Multiplexer, ReadData Register
10. HSIO49 - Service Request, Overrun and Word Status Buffer
11. HSIO50 - Serializer / DeSerializer
12. HSIO51 - Field/ Word Machine
13. HSIO52 - MFM Encoding, Pre-Compensation and Address Mark Gen.
14. HSIO53 - Disk Output Buffers and Drivers
15. HSIO54 - Logic for Phase Decoder
16. HSIO55 - Disk Input Buffers and Receivers
17. HSIO56 - Miscellaneous Input Clocks and Multiplexing
18. HSIO57 - Data Separator and Address Mark Detection
19. HSIO58 - Input Multiplexer
20. sHSIO59 - Disk Cables Connections for stichweld card
21. pHSIO59 - DiskCables, Terminators for PWB card
22. sHSIO60 - Discrete Phase Decoder Oscillator, Stichweld version
23. pHSIO60 - Discrete Phase Decoder Oscillator, PWB version
24. sHSIO61 - Discrete Phase comparator, Stichweld Version
25. pHSIO61 - Discrete Phase comparator, PWB version

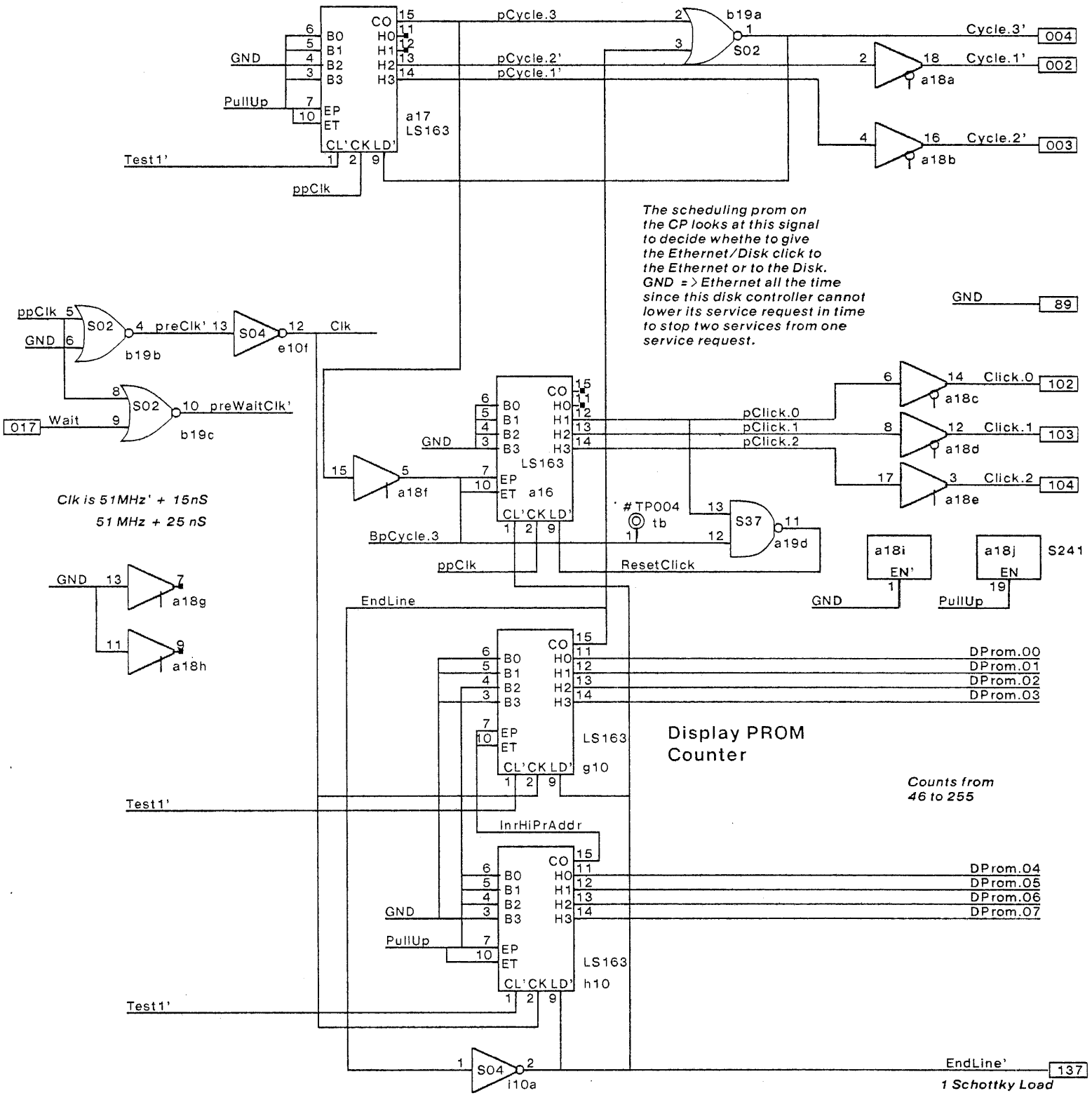
Other Documentation

This file is in:	[Iris]<Workstation>HSIO>HSIO-Rev-R.press	All logic drawings in Press format
	[Iris]<Workstation>HSIO>HSIO-R.dm	All design Automation info about HSIO board
	[Iris]<Workstation>HSIO>HSIO-R.wl	Wirelist for this rev of HSIO board
	[Iris]<Workstation>HSIO>DDC-Rev-R.DocDm	Disk Documentation in Sil and Bravo formats
	[Iris]<Workstation>HSIO>DDC-Rev-R.press	All Disk Documentation in Press format
	[IRIS]<Workstation>HSIO>Proms>DDCProms-Rev-A.dm	Disk Prom Programs
	[Iris]<Workstation>HSIO>WSD-Rev-C.DocDm	Display Documentation drawings, Timing Diagrams
	[Iris]<Workstation>HSIO>WSD-Rev-C.press	All Display Logic, Timing diagrams in Press format
	[Iris]<Workstation>HSIO>Proms>DisplayProms-Rev-A.dm	Display Prom Programs

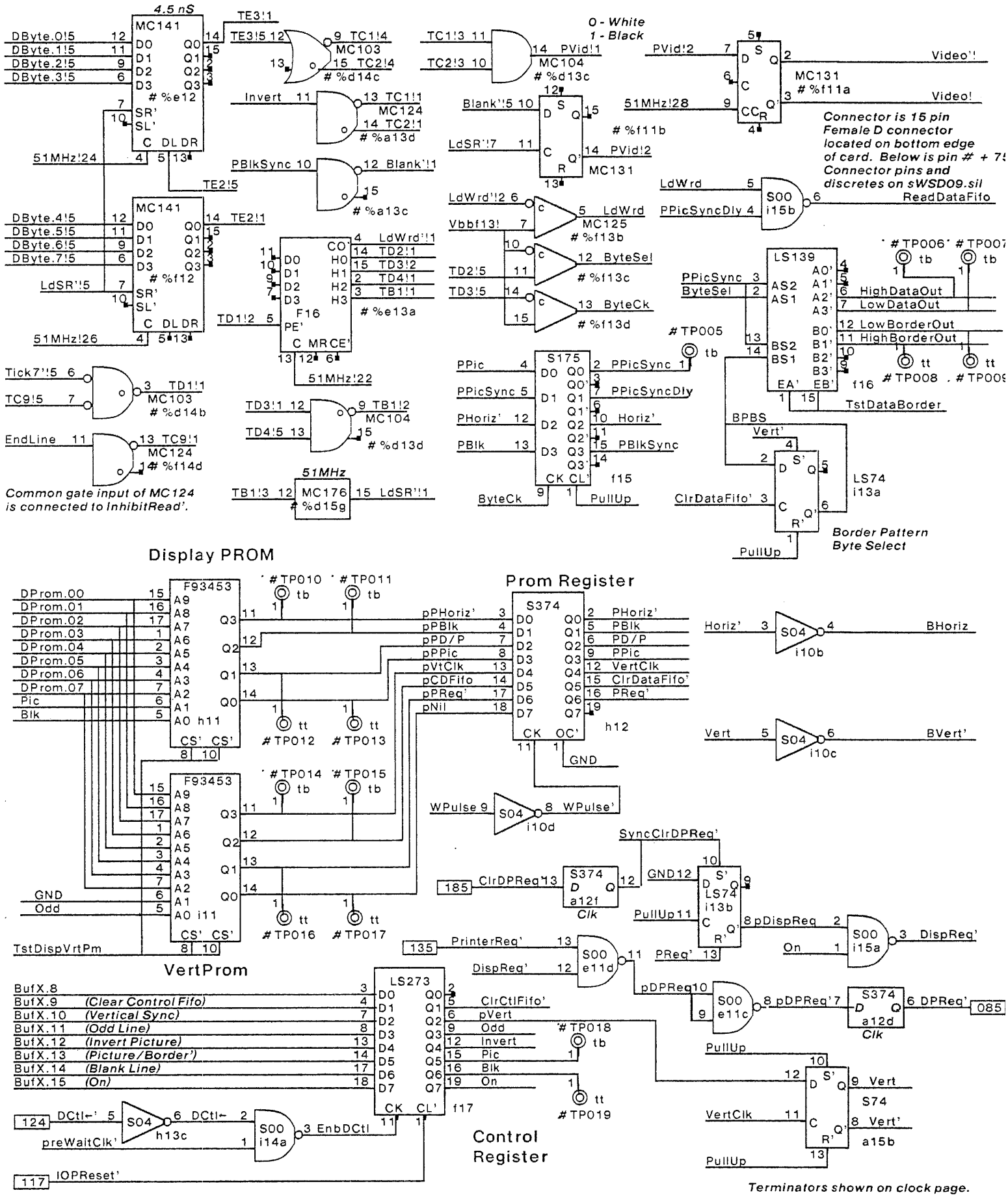


Note: *The prefix #% in front of chip position causes the chip to be wired upside down in socket. This prevents cutting of ground connections on stitchweld card.*
The suffix ! prevents Route from attempting automatic terminator assignment since DO stitchweld card has none defined.
Subnet wiring order for a net is done by appending to the net name a ! followed by the wiring sequence number of the node in the net.
Automatic terminator assignment is inhibited by use of ! as the last character in the character string of the net. This must occur after the subnet feature if it is also being used.

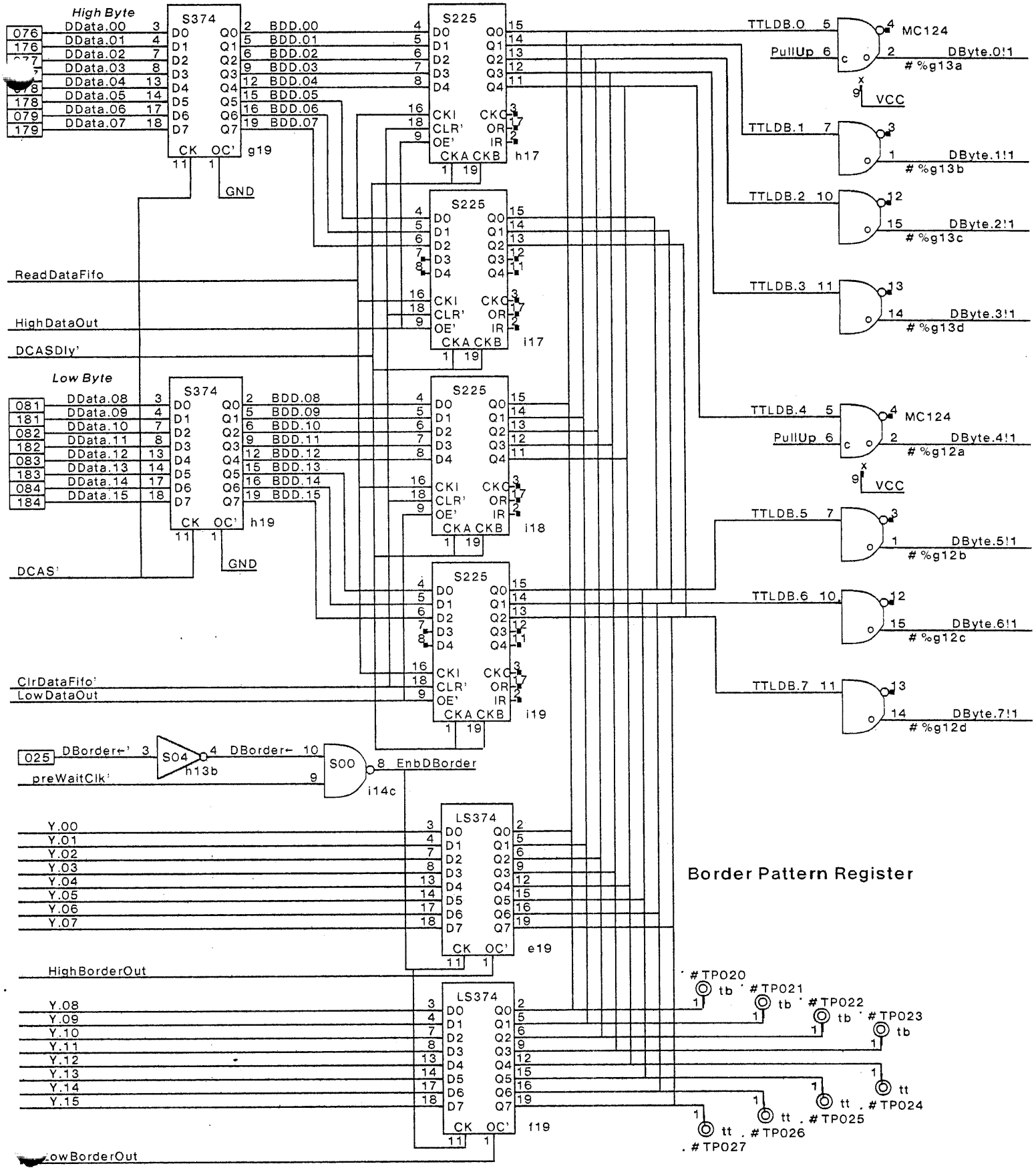
XEROX SDD	Project WS	51 MHz Clock Dividers	File sHSIO22.sil	Designer Crane	Rev R	Date 10/22/80	Page 22



XEROX SDD	Project WS	Cycles, Clicks, & Display Counter	File sHSIO23.sil	Designer Crane	Rev R	Date 10/22/80	Page 23

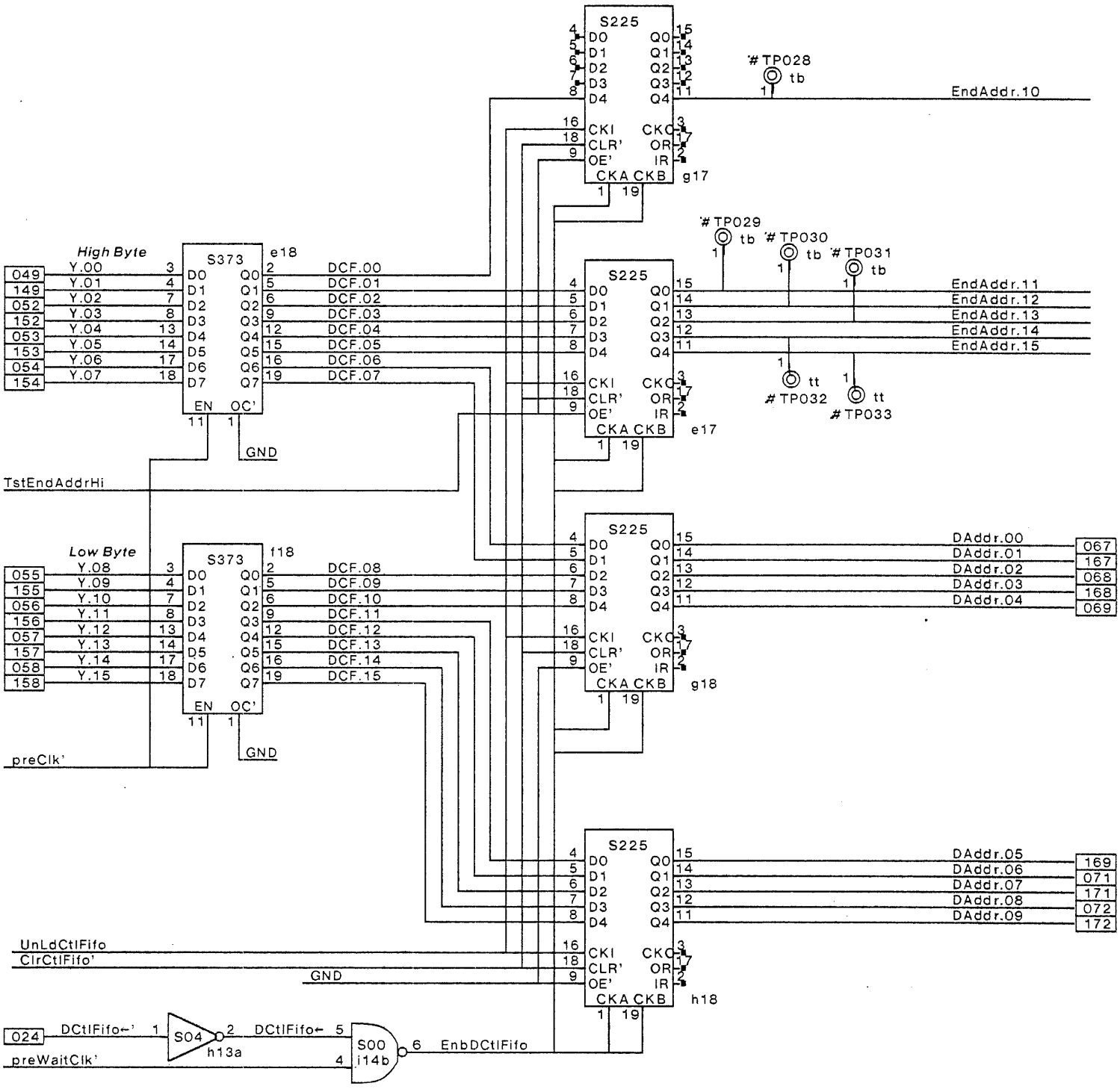


XEROX SDD	Project WS	Display Output Machine and Control Register	File sHSIO24.sil	Designer Crane, Davies	Rev R	Date 10/22/80	Page 24

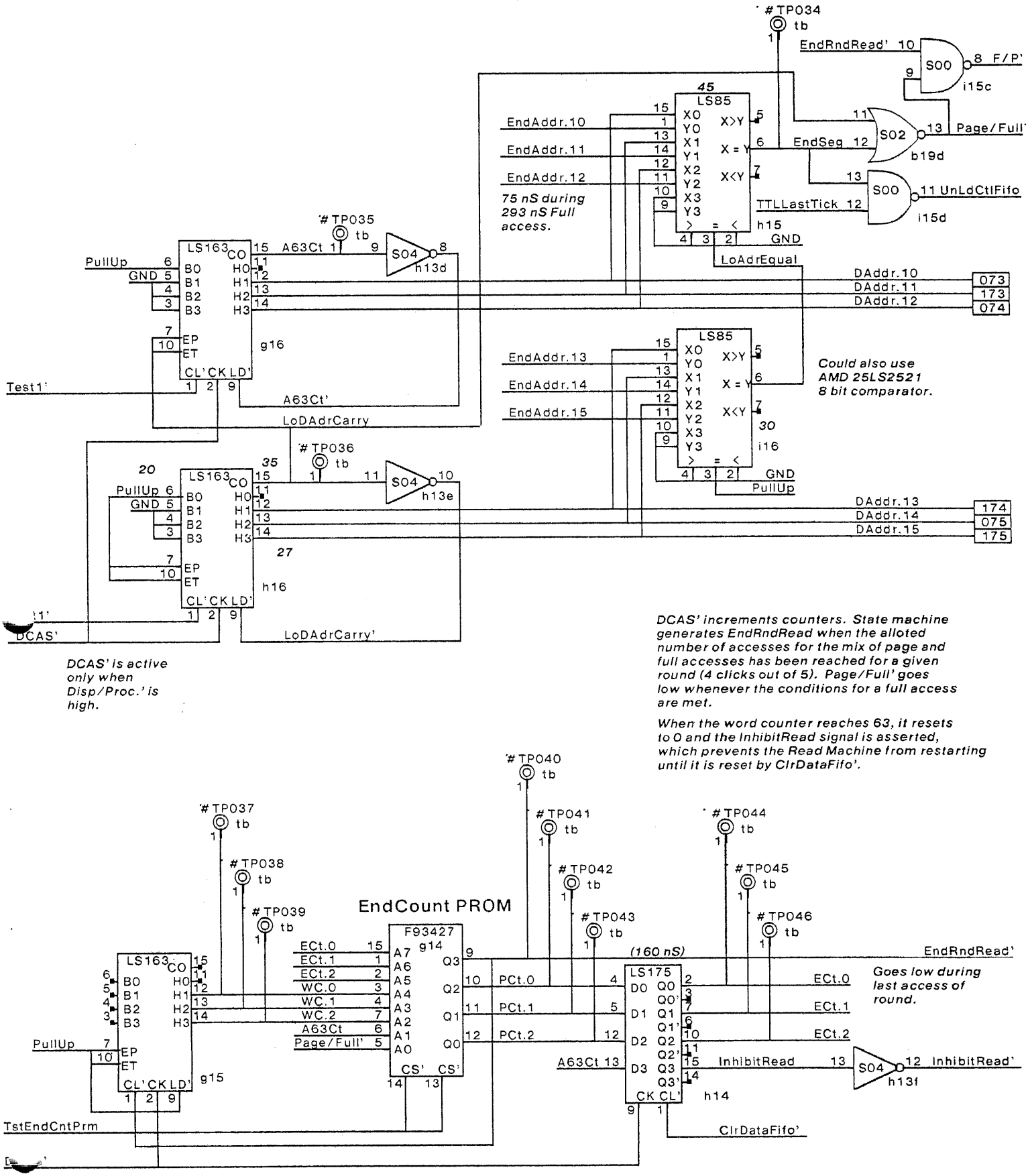


EndLine goes low once per horizontal line.
DCASDly' is DCAS' delayed by 20 nS.
Read signal goes low for 20 nS before low data byte is latched by the shift register.

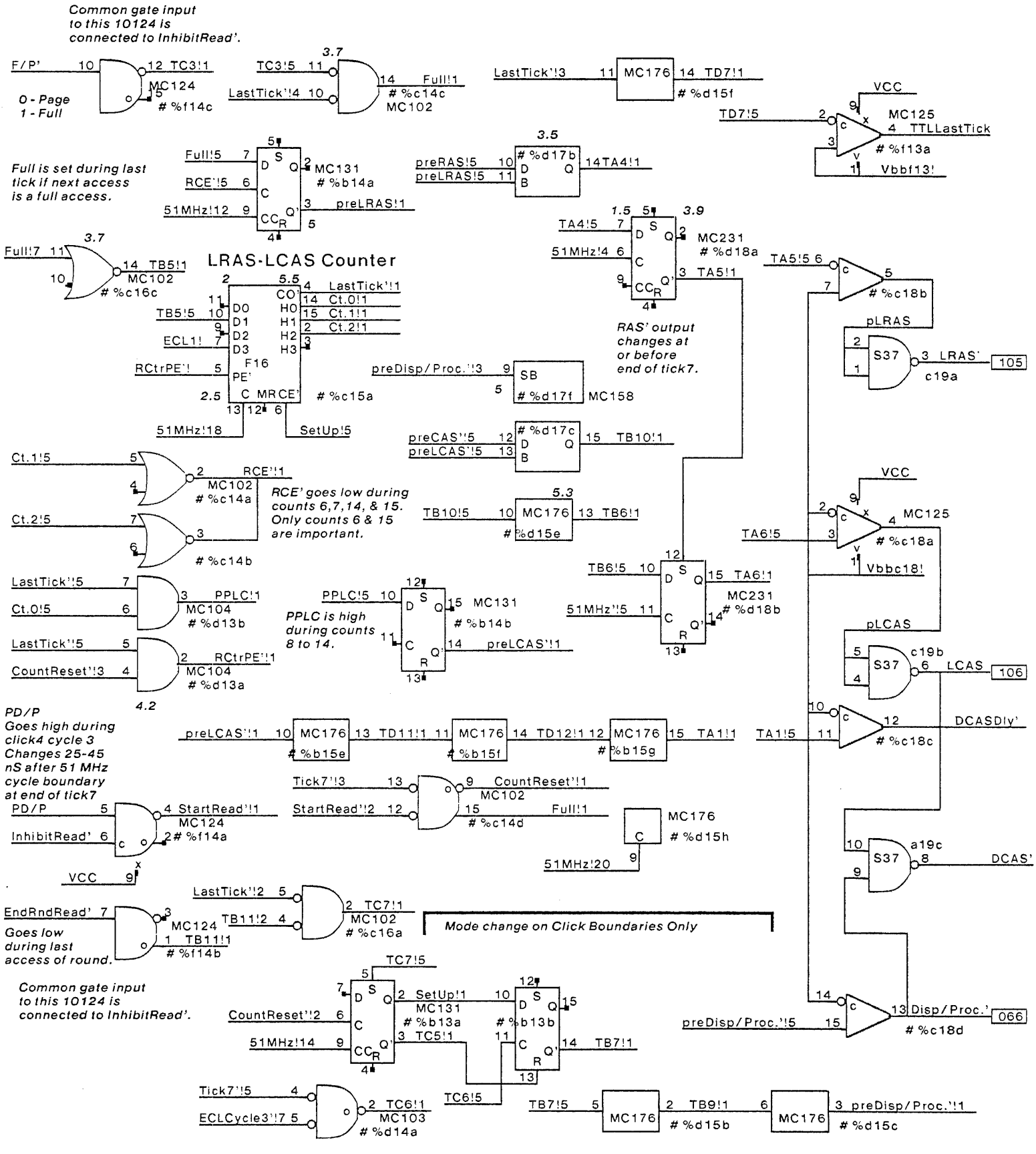
XEROX SDD	Project WS	Data FIFO and Border Register	File sHSIO25.sil	Designer Crane	Rev R	Date 10/22/80	Page 25



XEROX SDD	Project WS	Control FIFO Data Path	File sHSIO26.sil	Designer Crane	Rev R	Date 10/22/80	Page 26



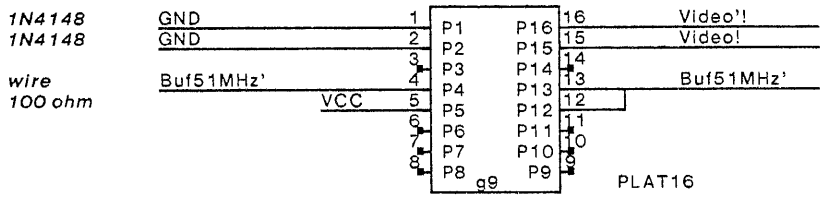
XEROX SDD	Project WS	Read Machine: Word Counter & End Conditions	File sHSIO27.sil	Designer Crane	Rev R	Date 10/22/80	Page 27

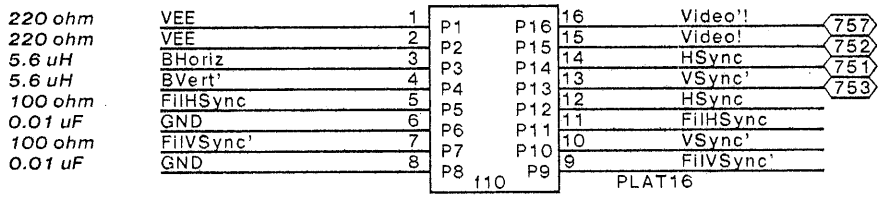


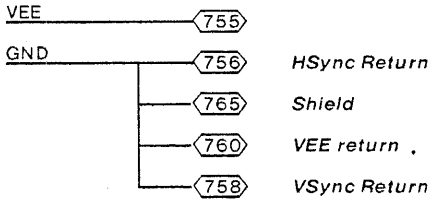
Terminators are shown on the clock page.

XEROX SDD	Project WS	LCAS & LRAS' Generation	File sHSIO28.sil	Designer Crane	Rev R	Date 10/22/80	Page 28

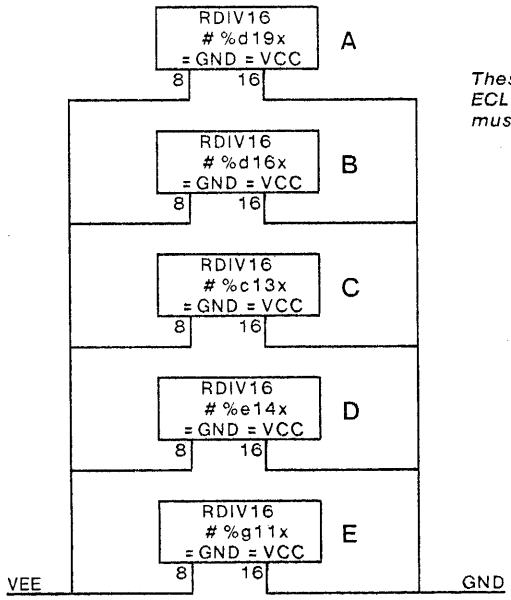
This is a platform of discretes used to filter the video, Hsync and VSync' signals







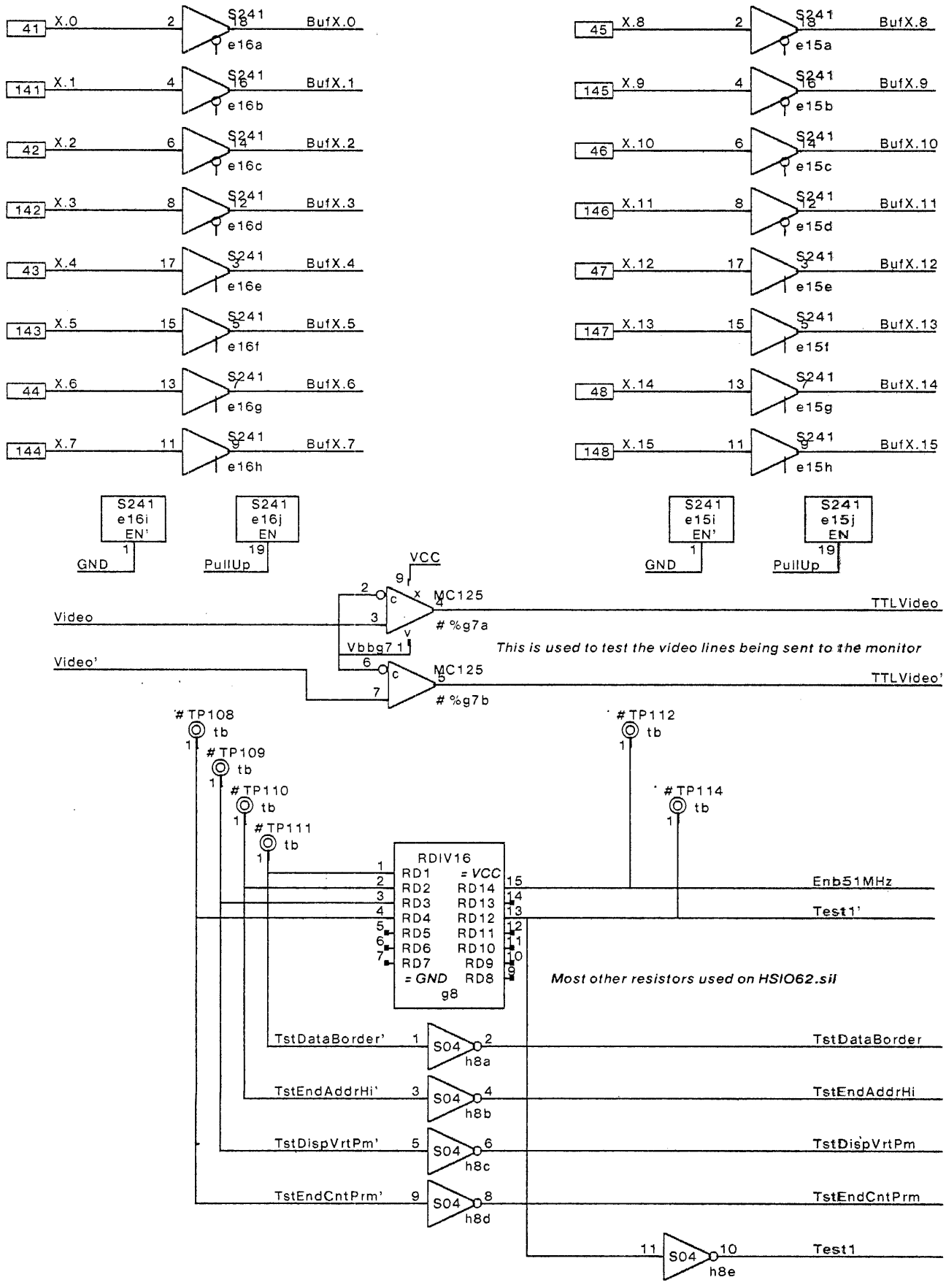
The connector is a 15 pin Female D connector located on the bottom edge of the card. The pin numbers shown are the actual pin number + 750.



These RDIV16's are being used as ECL terminators, so their power connections must change to reflect ECL conventions.

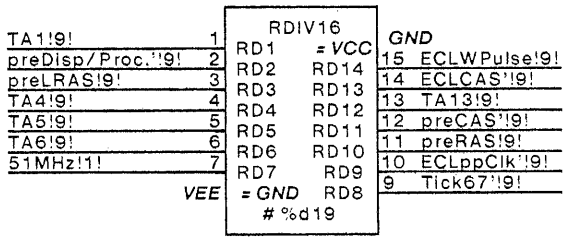
XEROX SDD	Project	Dandelion Display Controller	File	Designer	Rev	Date	Page
	Dandelion	Discretes, Connectors for Stichweld controller	sHSIO29.sil	Crane, Davies	R	10/22/80	29

Buffer X bus to reduce loading.

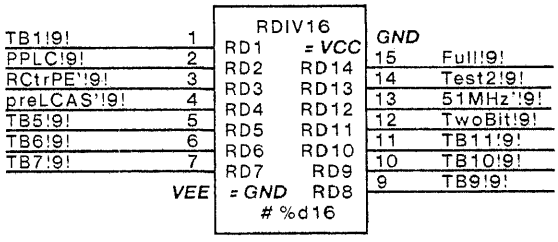


XEROX SDD	Project Dandelion	Testability Signals	File sHSIO30.sil	Designer Davies	Rev R	Date 10/22/80	Page 30

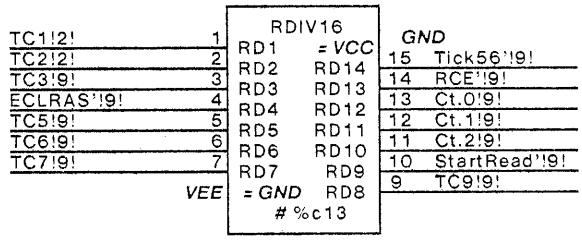
A



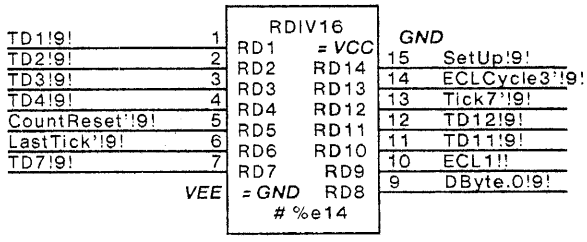
B



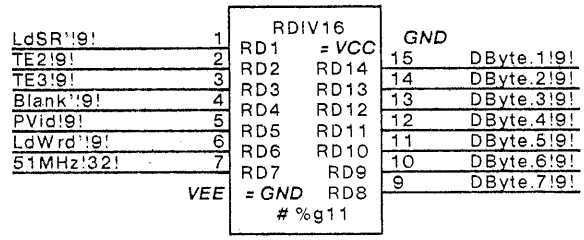
C



D



E

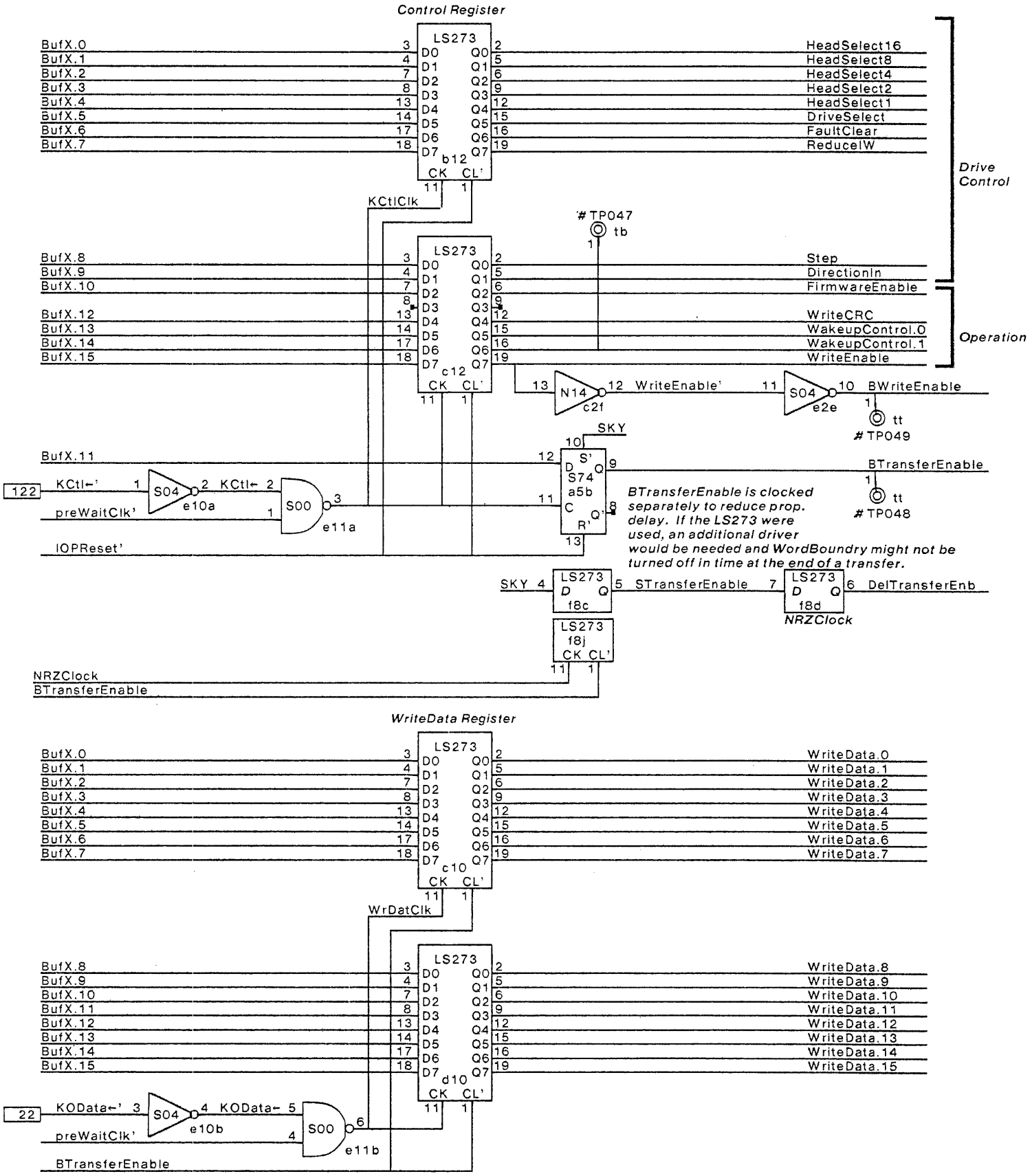


Termination Packages A, B, C, D, E above are 100 ohm termination to -2 V
Allen-Bradley part no. 316E161261

Pin 16 on each termination package is connected to GND and Pin 8 to VEE (-5.2 V). This is done on pWSD09.sil and sWSD09.sil where there is more room. This connection make the termination compatible with normal ECL power rules.

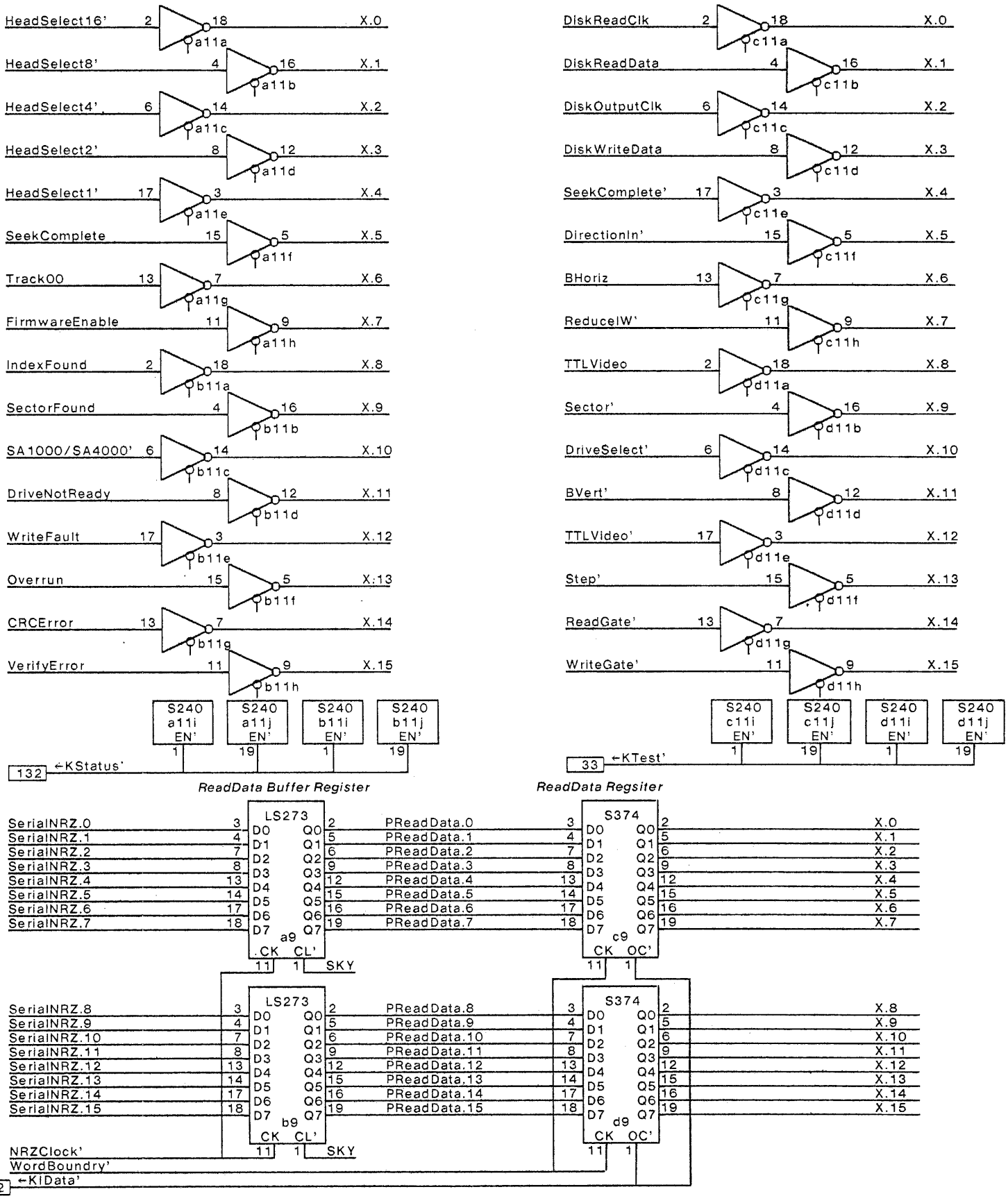
Note:

The prefix #% in front of chip position causes the chip to be wired upside down in socket. This prevents cutting of ground connections on stitchweld card.
The suffix ! prevents Route from attempting automatic terminator assignment since DO stitchweld card has none defined. Subnet wiring order for a net is done by appending to the net name a ! followed by the wiring sequence number of the node in the net. Automatic terminator assignment is inhibited by use of ! as the last character in the character string of the net. This must occur after the subnet feature if it is also being used.

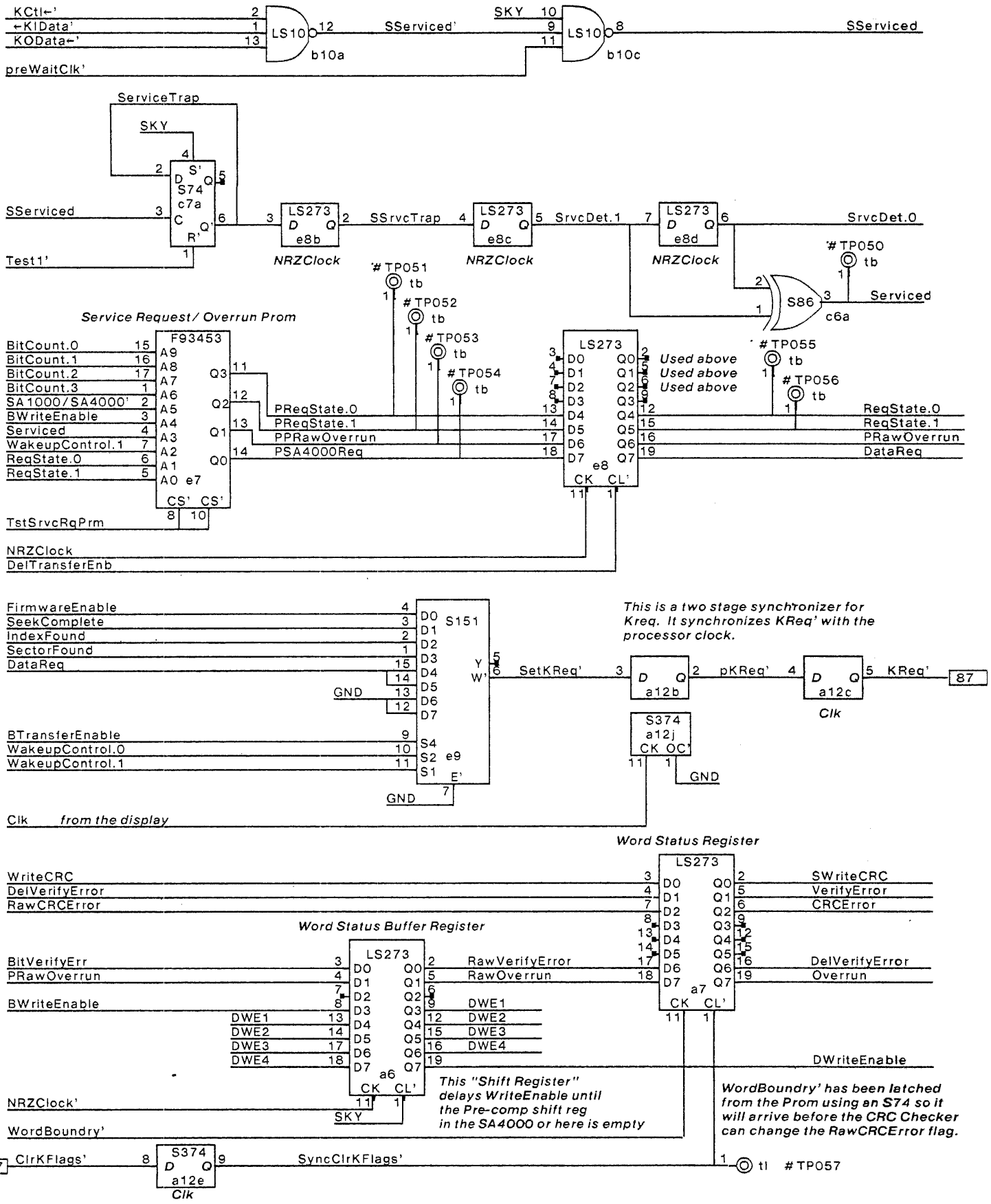


XEROX SDD	Project: Dandelion	Dandelion Disk Controller: Control and Write Data Regs.	File: sHSIO47.sil	Designer: Davies	Rev: R	Date: 10/22/80	Page: 47

Status/Test Multiplexer

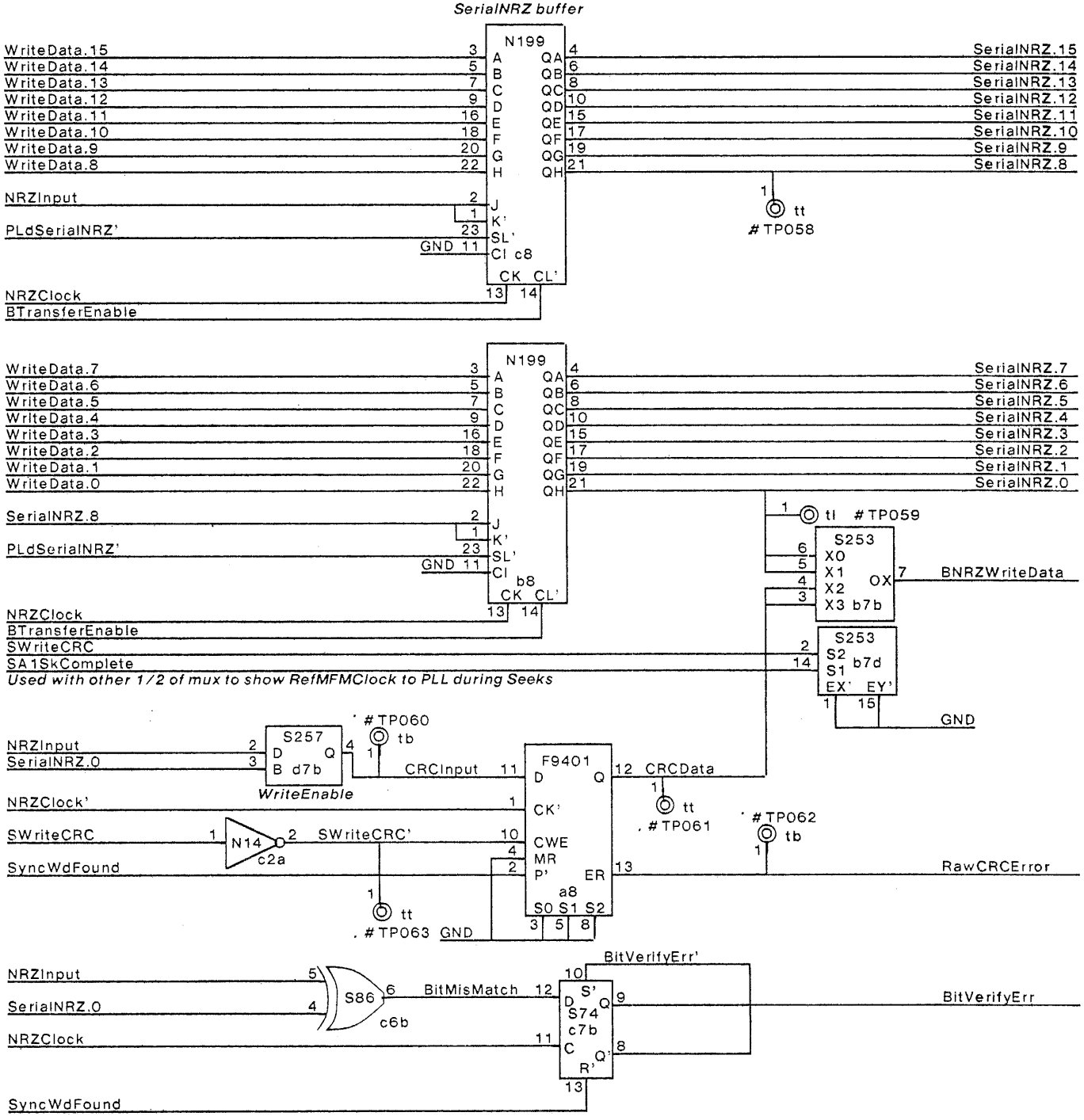


XEROX SDD	Project	Dandelion Disk Controller	File	Designer	Rev	Date	Page
	Dandelion	Status/Test Mux, ReadData Reg	sHSIO48.sil	Davies	R	10/22/80	48

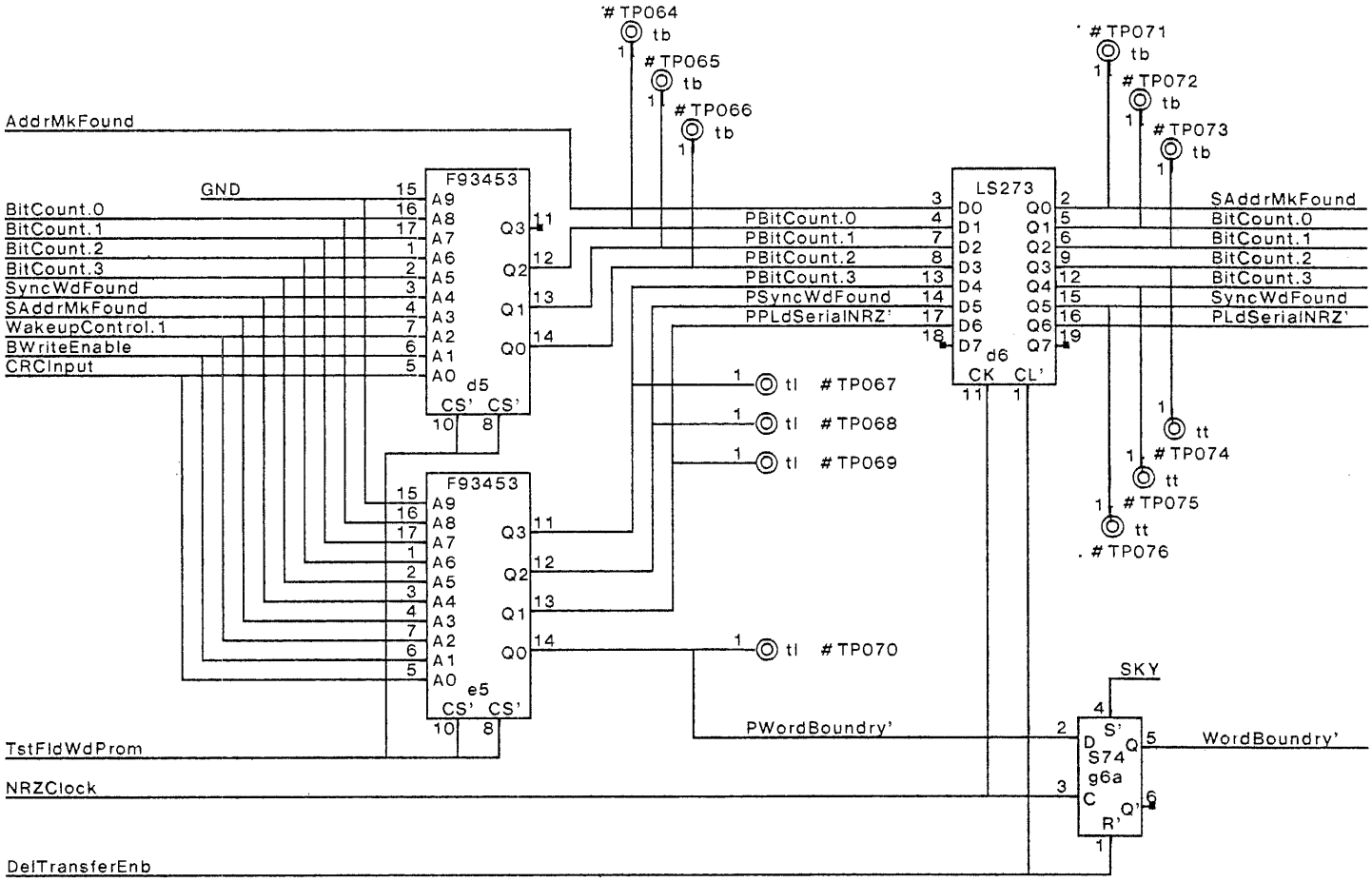


XEROX SDD	Project	Dandelion Disk Controller	File	Designer	Rev	Date	Page
	Dandelion	Srv. Req, Overrun, Word Stat.	sHSI049.sil	Davies	R	10/22/80	49

SerialNRZ Shift Register and Error Checking

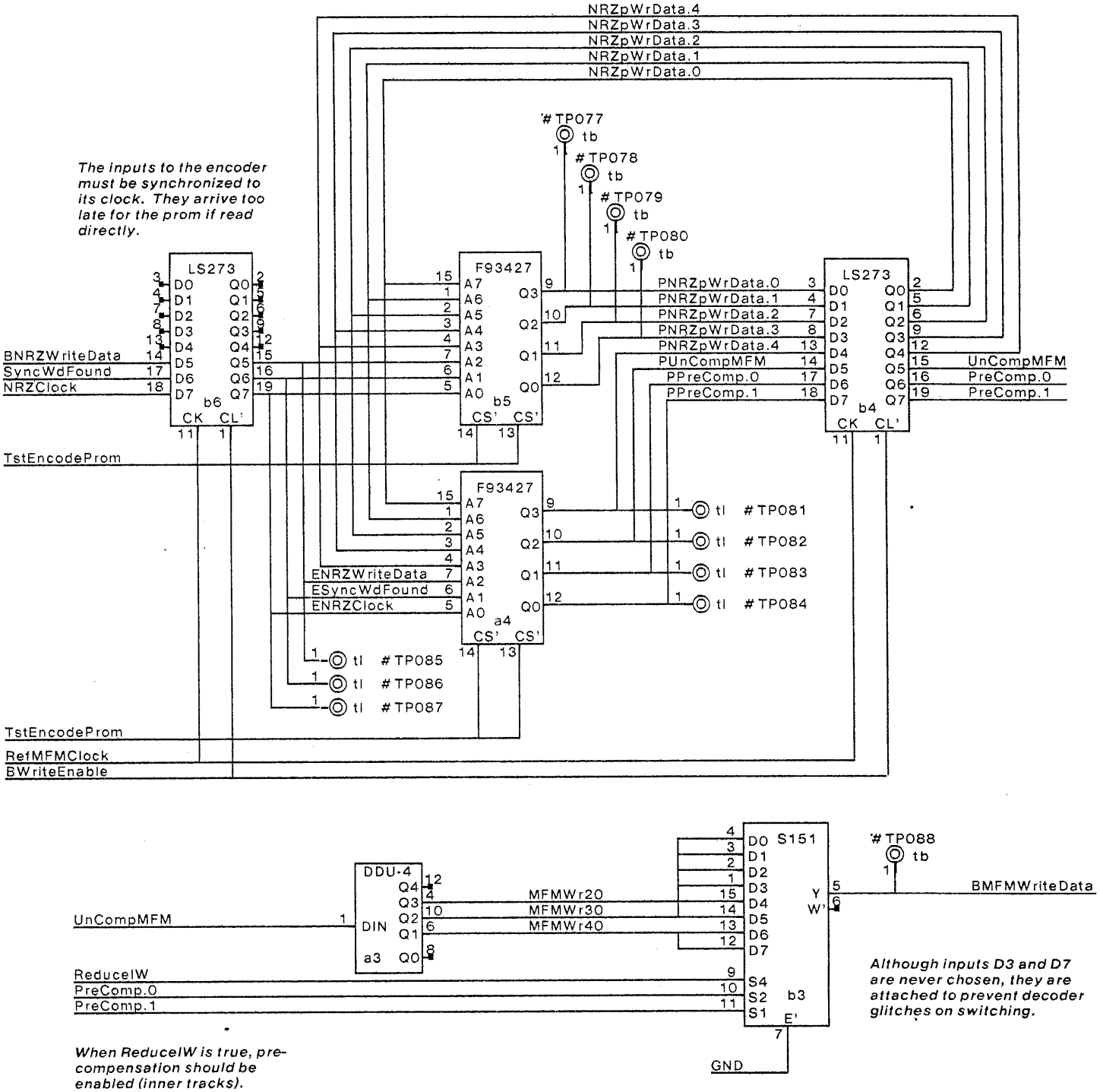


XEROX SDD	Project	Dandelion Disk Controller	File	Designer	Rev	Date	Page
	Dandelion	Serializer/DeSerializer	sHSIO50.sil	Davies	R	10/22/80	50

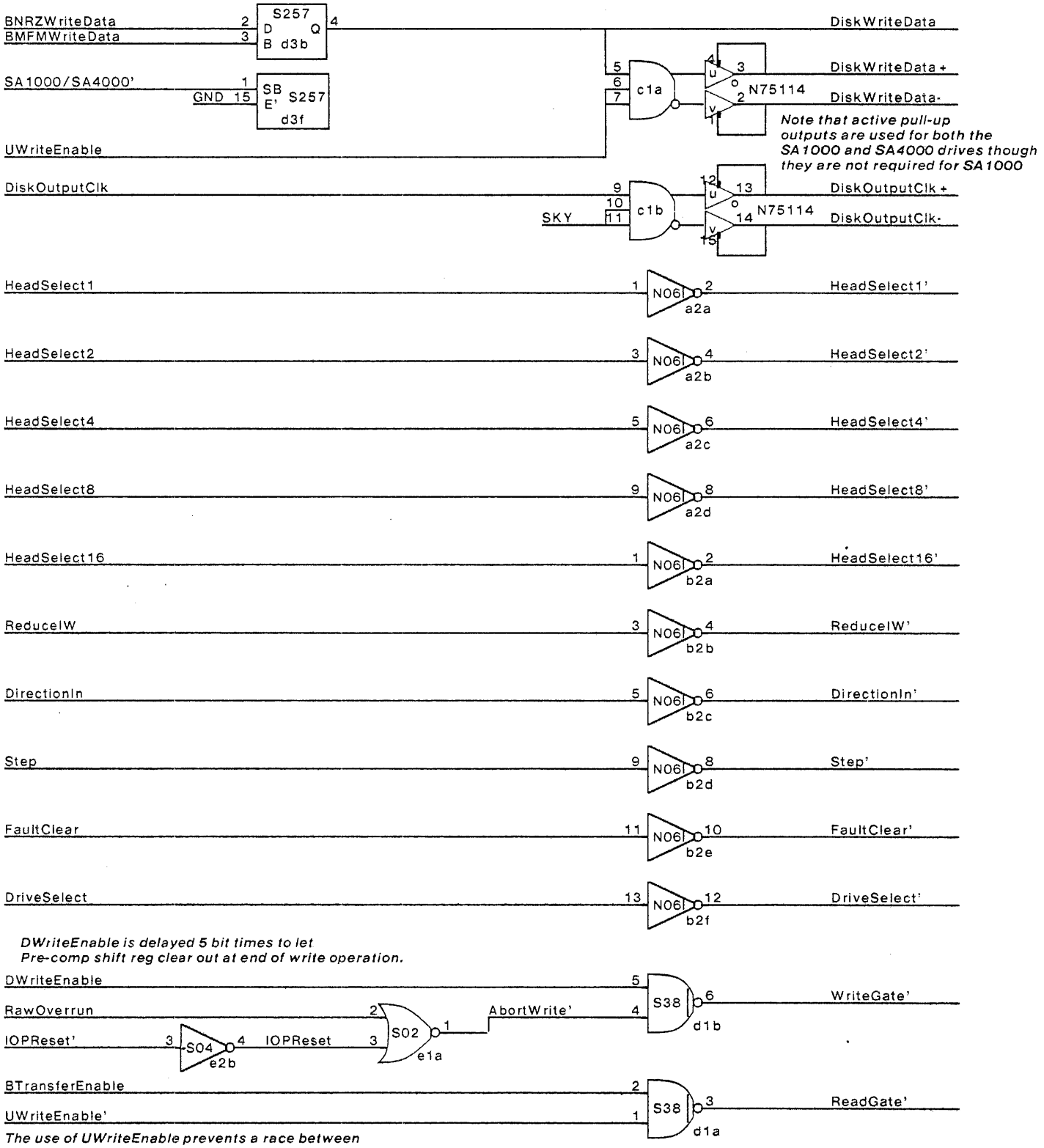


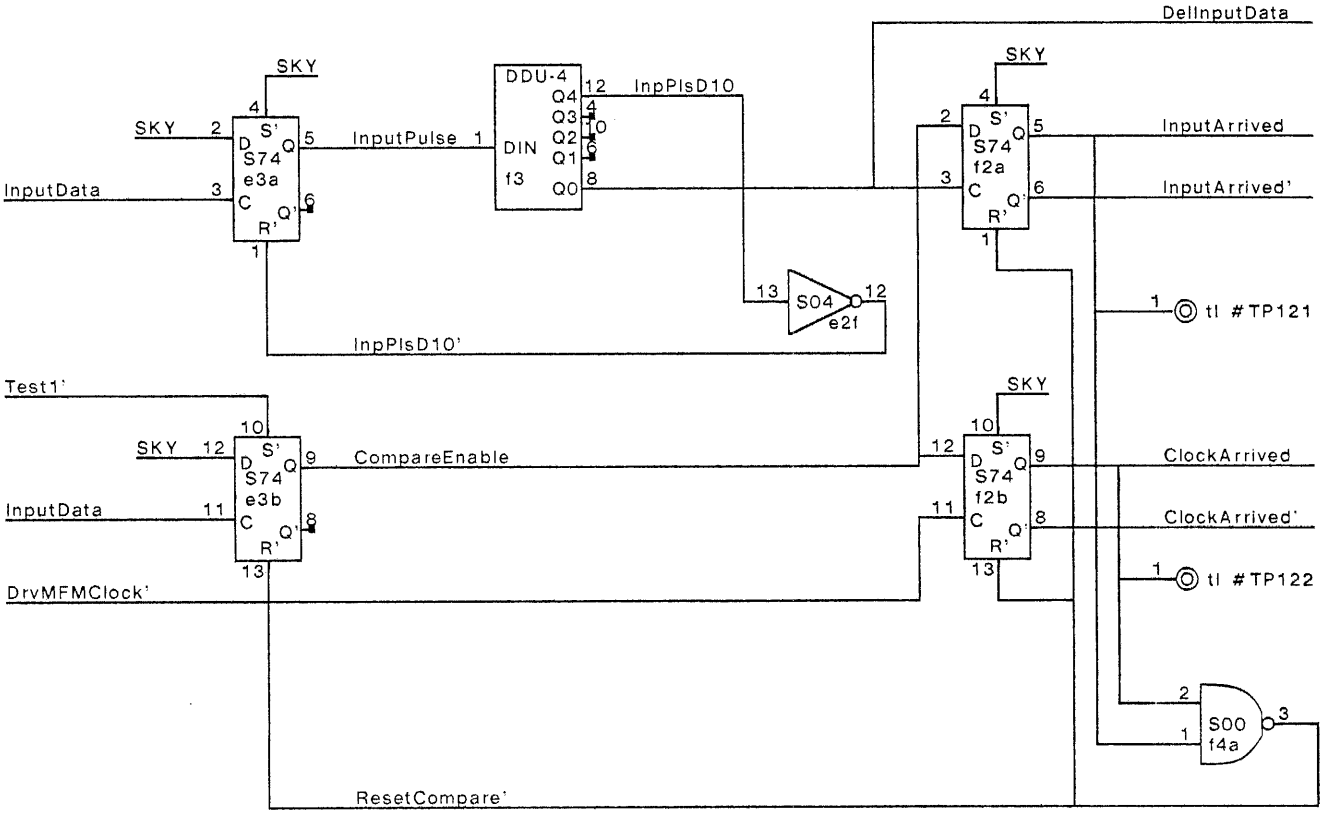
Using an S74 instead of the LS273 speeds up WordBoundry' so it will change before the RawCRCError indicator from the 9401 CRC Checker. This allows us to latch the CRCError signal directly using WordBoundry'. The RawCRCError signal is too slow to latch into the Word Status buffer register using NRZClock'. There is then a race between WordBoundry' and RawCRCError after NRZClock rises. Using the faster S74 here ensures WordBoundry' wins.

XEROX SDD	Project: Dandelion	Dandelion Disk Controller: Field and Word State Machine	File: sHSIO51.sil	Designer: Davies	Rev: R	Date: 10/22/80	Page: 51

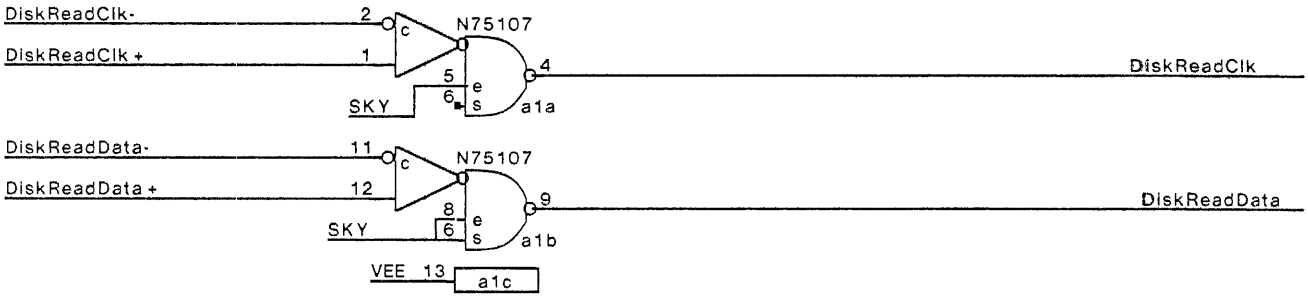


XEROX SDD	Project: Dandelion	Dandelion Disk Controller: MFM Encoding, PreComp, Address Mark Generation	File: sHSIO52.sil	Designer: Davies	Rev: R	Date: 10/22/80	Page: 52

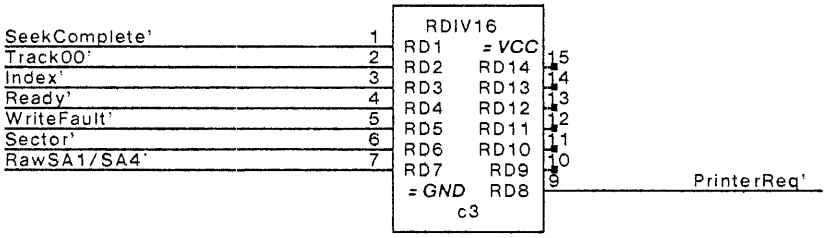

BNRZWriteData
BMFMWriteData
S257
D Q
B d3b
DiskWriteData
SA1000/SA4000'
GND
SB
E'
S257
d3f
c1a
N75114
DiskWriteData+
DiskWriteData-
Note that active pull-up outputs are used for both the SA1000 and SA4000 drives though they are not required for SA1000
UWriteEnable
DiskOutputClk
SKY
c1b
N75114
DiskOutputClk+
DiskOutputClk-
HeadSelect1
HeadSelect1'
HeadSelect2
HeadSelect2'
HeadSelect4
HeadSelect4'
HeadSelect8
HeadSelect8'
HeadSelect16
HeadSelect16'
ReduceIW
ReduceIW'
DirectionIn
DirectionIn'
Step
Step'
FaultClear
FaultClear'
DriveSelect
DriveSelect'
N06
a2a
a2b
a2c
a2d
b2a
b2b
b2c
b2d
b2e
b2f
DWriteEnable is delayed 5 bit times to let
Pre-comp shift reg clear out at end of write operation.
DWriteEnable
RawOverrun
IOPReset'
S04
e2b
IOPReset
S02
e1a
AbortWrite'
S38
d1b
WriteGate'
BTransferEnable
UWriteEnable'
S38
d1a
ReadGate'
The use of UWriteEnable prevents a race between
WriteGate' and ReadGate'. If BWriteEnable were used, there would be
a race between BTransferEnable and BWriteEnable when finishing a write op
that could glitch ReadGate', causing a WriteFault. Since BTransferEnable is faster than UWriteEnable, there is a ~20 ns glitch
in ReadGate at the beginning of a Write Op. This causes NRZClock to pause, but only temporily.



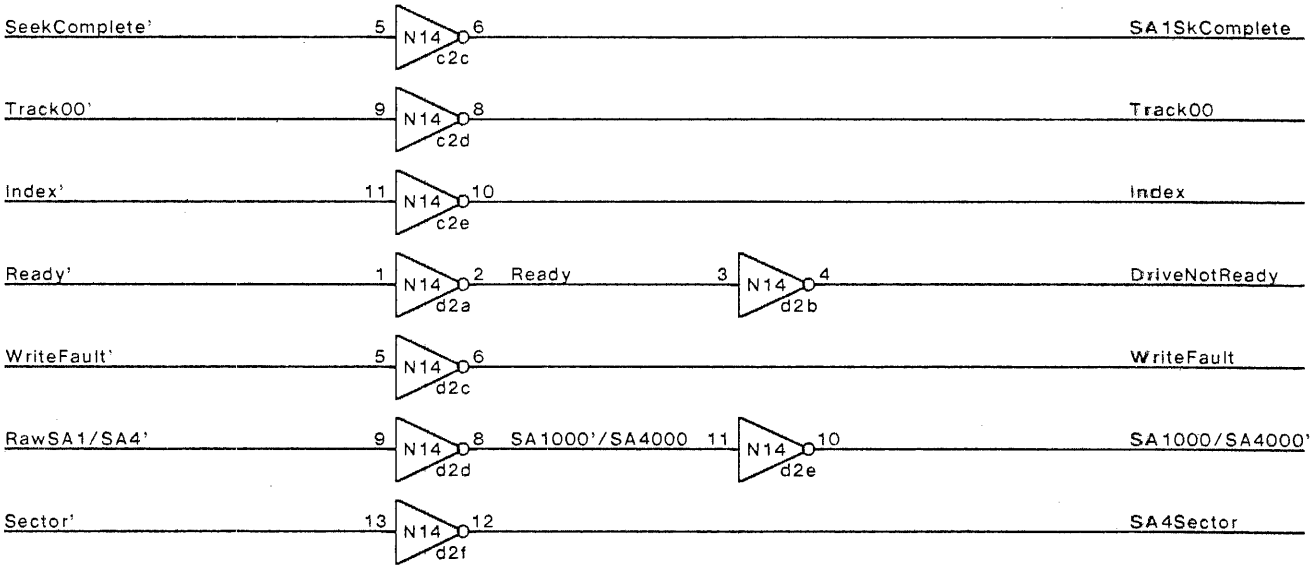
XEROX SDD	Project	Dandelion Disk Controller	File	Designer	Rev	Date	Page
	Dandelion	Phase Decoder Logic	sHSIO54.sil	Davies	R	10/22/80	54



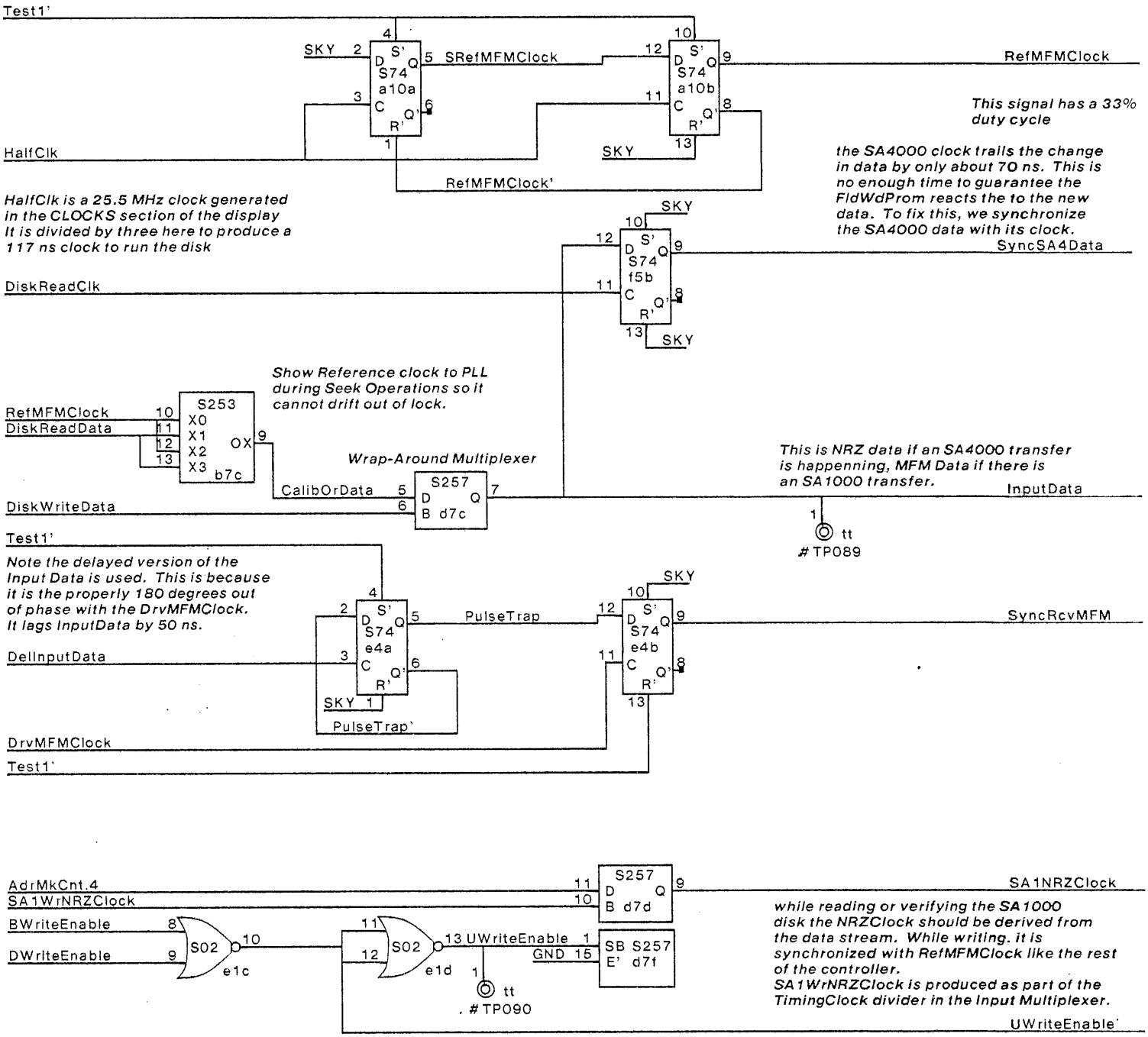
This is a Beckman RPack number 898-5-R220/330.



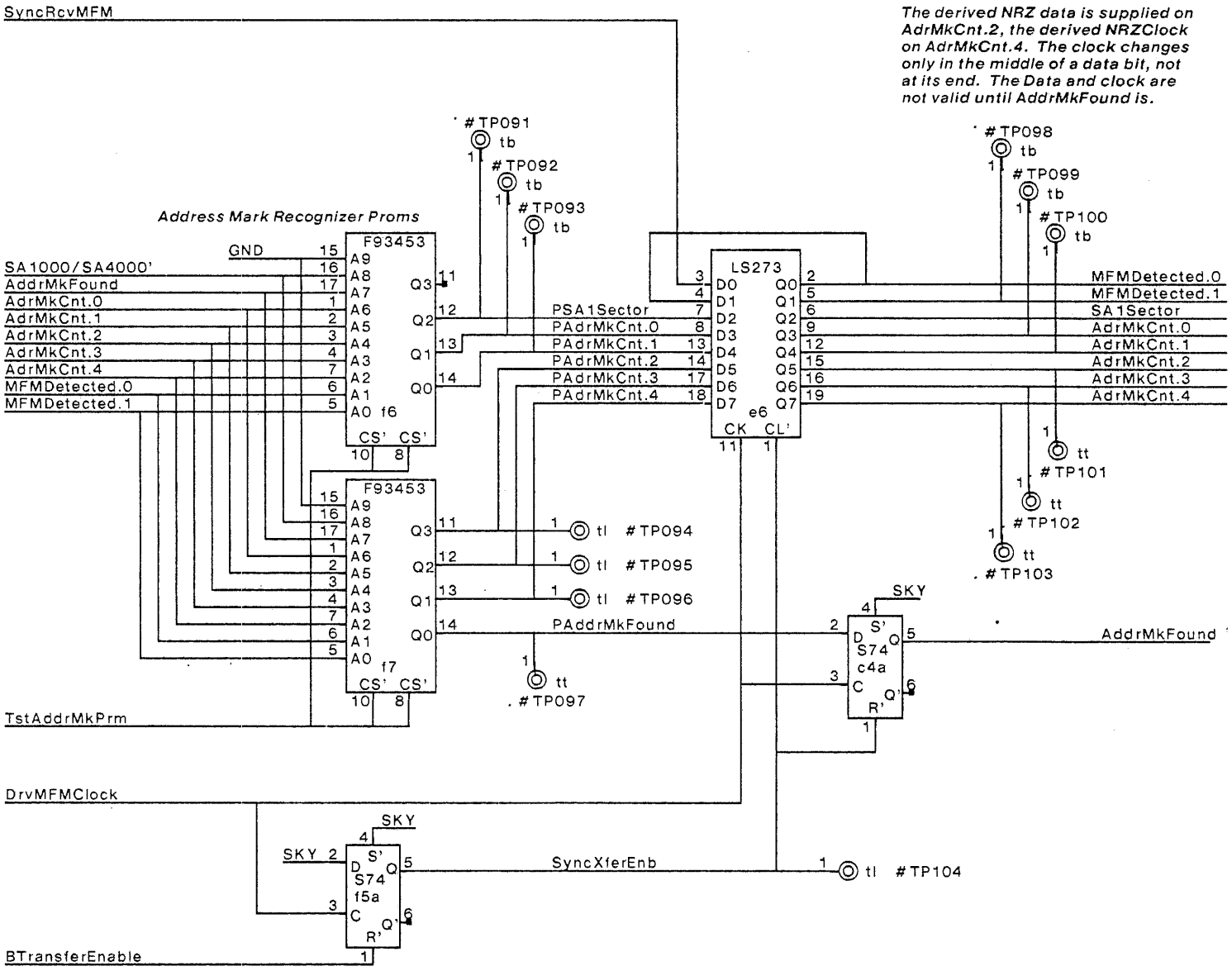
Pull this up so display request will work even if Options board is unplugged.



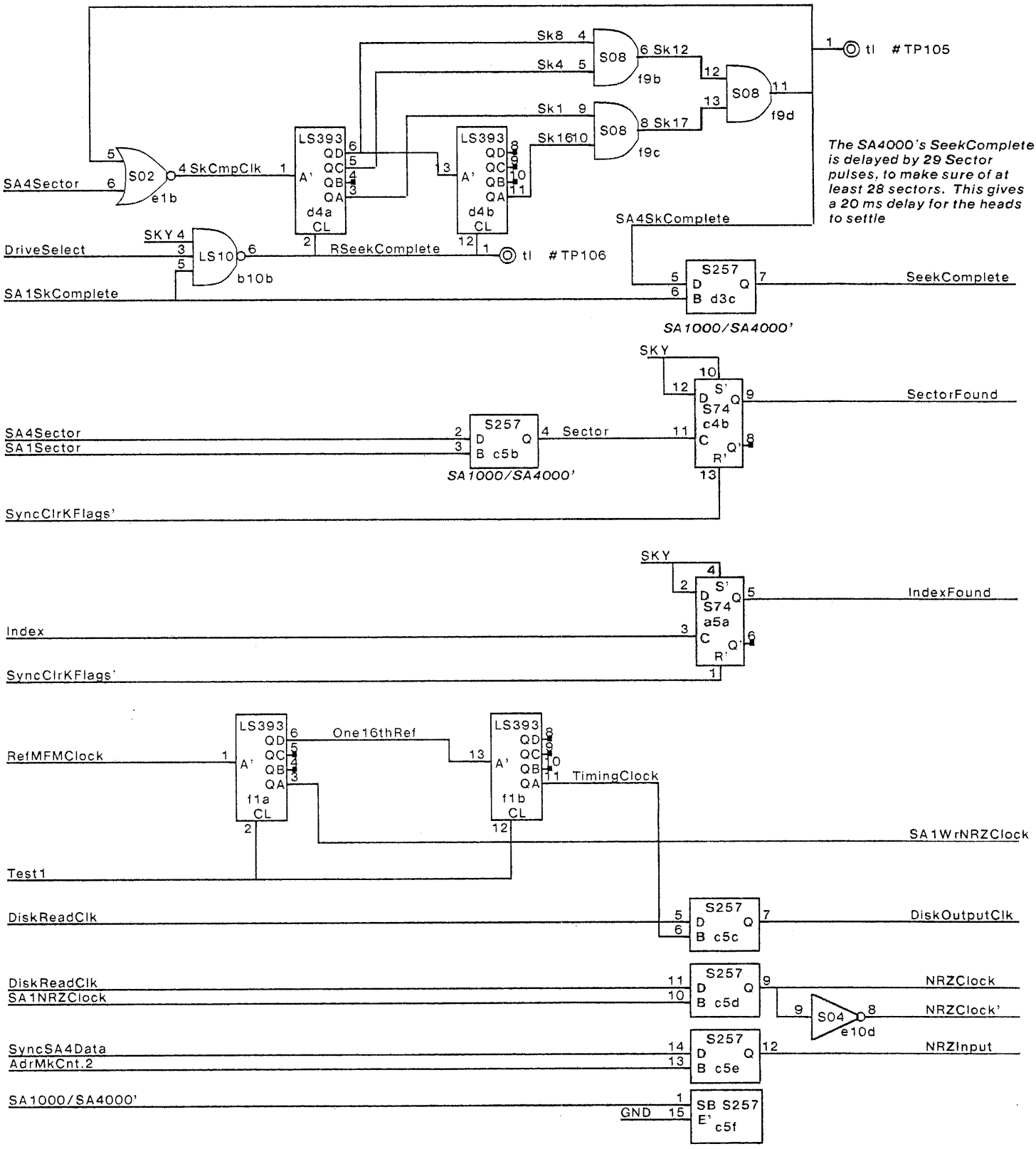
XEROX SDD	Project: Dandelion	Dandelion Disk Controller: Input Buffers and Receivers	File: sHSIO55.sil	Designer: Davies	Rev: R	Date: 10/22/80	Page: 55



XEROX SDD	Project	Dandelion Disk Controller	File	Designer	Rev	Date	Page
	Dandelion	Misc. Input Clocks and Mux.	sHSI056.sil	Davies	R	10/22/80	56

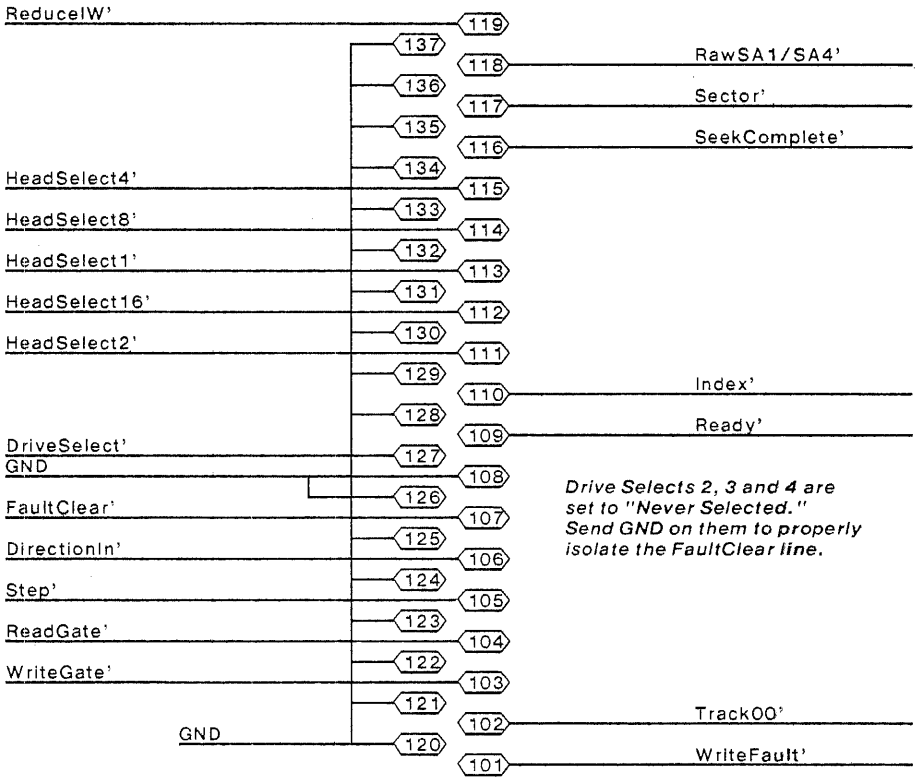


XEROX SDD	Project: Dandelion	Dandelion Disk Controller: Data Sep. and Addr Mk Detect.	File: sHSIO57.sil	Designer: Davies	Rev: R	Date: 10/22/80	Page: 57



XEROX SDD	Project: Dandelion	Dandelion Disk Controller: Input Multiplexer	File: sHSI058.sil	Designer: Davies	Rev: R	Date: 10/22/80	Page: 58

The 50 pin cable to the SA1000 drive has been reduced 10 37 lines so the 37 pin connector on the stichweld board may be used.
The connector on the stichweld board is a 37 pin female in the TOP position. Its pins are numbered 101-137
Signals not referenced on the drive's 50 pin cable are not connected to the stichweld poard.



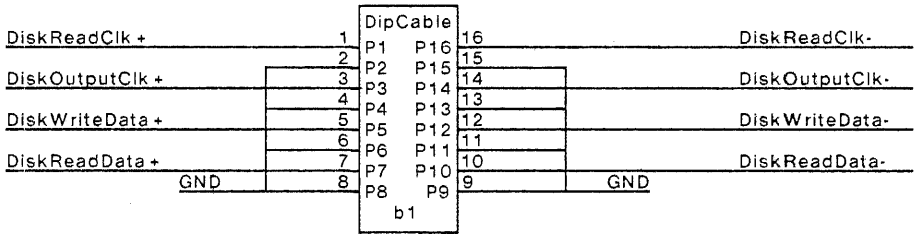
Drive Selects 2, 3 and 4 are set to "Never Selected." Send GND on them to properly isolate the FaultClear line.

37 pin conn	50 pin cable
119	2 *
137	3
118	4
136	5
117	6
135	7
116	8
134	9
115	10
133	11
114	12
132	13
113	14
131	15
112	16
130	17
111	18
129	19
110	20
128	21
109	22
127	26 *
108	28 *
126	30 *
107	32 *
125	33
106	34
124	35
105	36
123	37
104	38
122	39
103	40
121	41
102	42
120	43
101	44 *

In addition, GND to pins 1,23, 25,27 29, 31 and 45 of 50 conductor cable

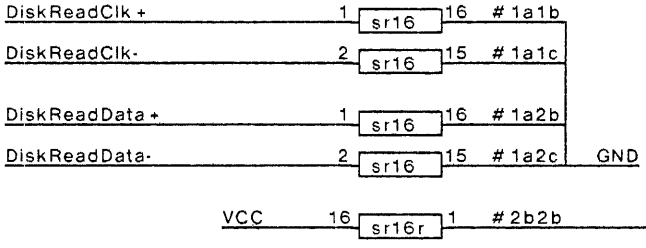
** Breaks in consecutive numbering*

The 16 pin data cable is installed in a DIP socket



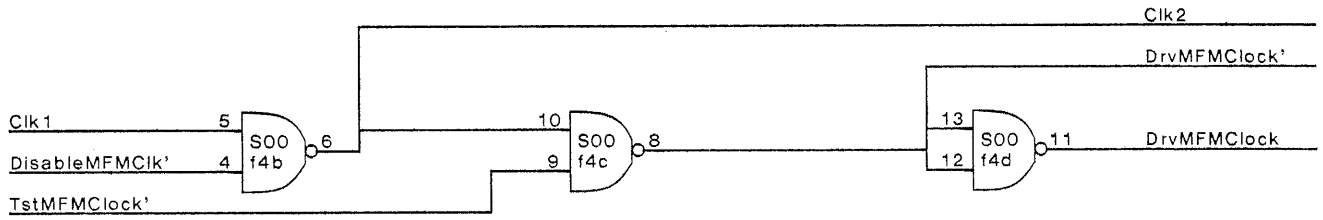
16 pin conn	20 pin cable
1	5
16	6
2	7
15	8
3	9
14	10
4	11
13	12
5	13
12	14
6	15
11	16
7	17
10	18
8	19
9	20

This is called "DConn"



These termination resistors are mounted in the unused holes of 20 pin sockets holding 14 pin chips. They are each 51 ohms.

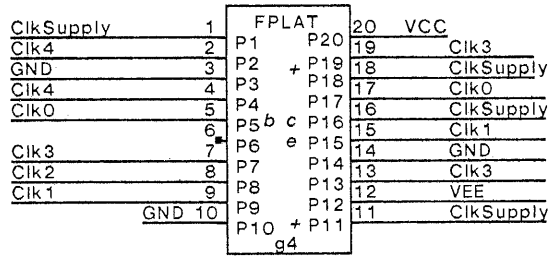
This resistor supplies logical one to the board It is also 51 ohms



C103 is a 1.0 uF tantalum capacitor

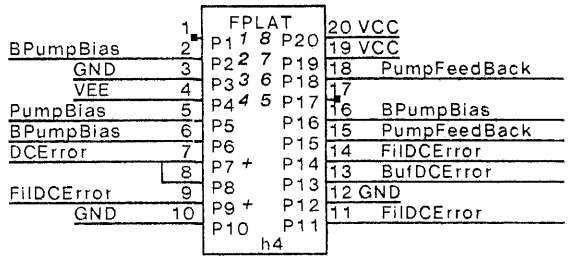
L101, 22 uH
L102, 12 uH
C108, 1.0uF
R111, 100 ohm
Q101, 2N5770

C118, 150 pF
R110, 470 ohm
R103, 510 ohm
C107, 0.1 uF



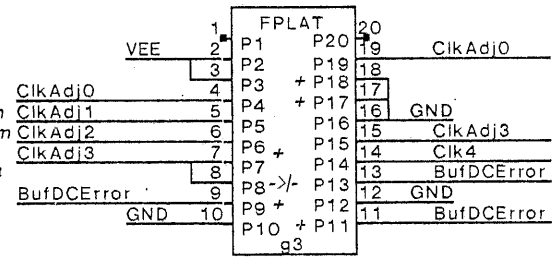
LM741

R127, 1.0 KOhm
C134, 0.47 uF
C132, 0.027 uF
R117, 510 ohm
C131, 0.0027 uF
R126, 110 ohm



C119 is a 1.0 uF tantalum capacitor
CR103 is an MV1404 VariCap, used to control the oscillator frequency.

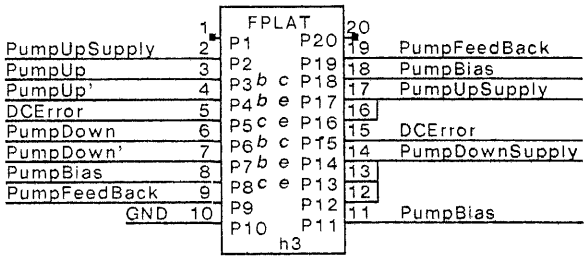
R112, 510 ohm
C120, 0.1 uF
C119, 1.0 uF
R105, 4.7 KOhm
R113, 200 KOhm
C122, 0.1 uF
CR103, MV1404
C124, 47 pf
C123, 100 pF



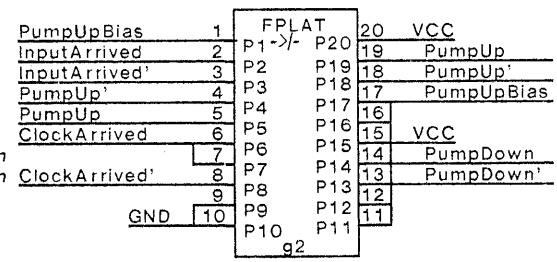
R125, 2.0 KOhm
Q103, 2N5771
Q102, 2N5771

Q105, 2N5770
Q104, 2N5770

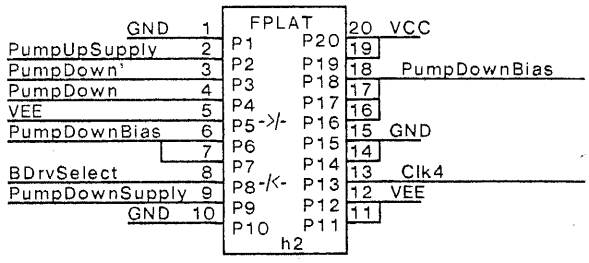
R138, 2.0 KOhm
R128, 100 ohm



CR102, 1N5221
R123, 910 ohm
R122, 910 ohm
R115, 200 ohm
R116, 200 ohm
R120, 510 ohm
R132, 1.1 KOhm
R134, 1.1 KOhm
C121, 0.1 uF
R114, 150 ohm

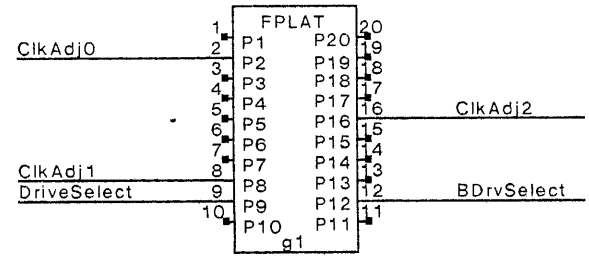


C133, 0.1 uF
R124 180 ohm
R135, 200 ohm
R133, 200 ohm
CR104, 1N5221
C140, 0.1 uF
R136, 180 ohm
CR101, 1N4148
R137, 240 ohm
C141, 0.1 uF

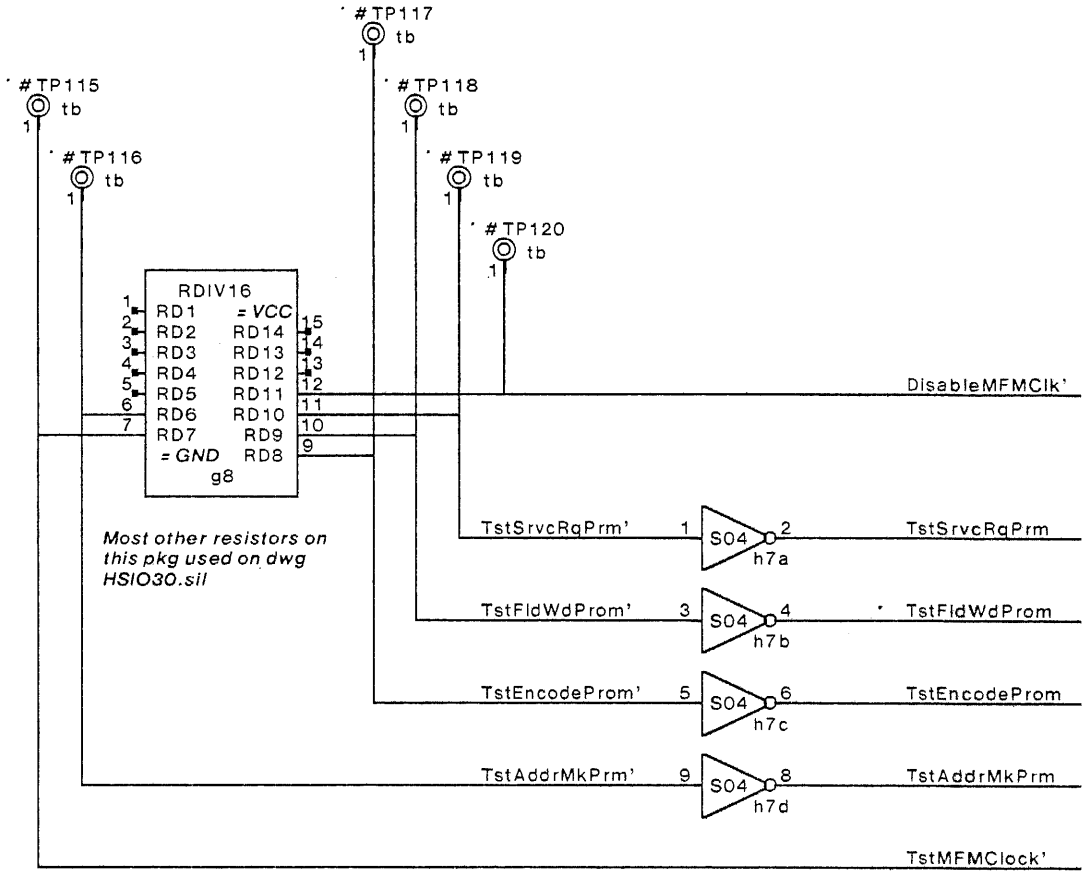


P100,
5K, 3/4 W
potentiometer

R109, 270 ohm



XEROX SDD	Project: Dandelion	Dandelion Disk Controller: Discrete Phase Comparator	File: sHSIO60.sil	Designer: Davies	Rev: R	Date: 10/22/80	Page: 60


#TP115
tb
1
#TP116
tb
1
#TP117
tb
1
#TP118
tb
1
#TP119
tb
1
#TP120
tb
1
RDIV16
RD1
RD2
RD3
RD4
RD5
RD6
RD7
= GND
= VCC
RD14
RD13
RD12
RD11
RD10
RD9
RD8
g8
Most other resistors on this pkg used on dwg HSIO30.sil
DisableMFMClk'
TstSrvcRqPrm'
S04
h7a
TstSrvcRqPrm
TstFldWdProm'
S04
h7b
TstFldWdProm
TstEncodeProm'
S04
h7c
TstEncodeProm
TstAddrMkPrm'
S04
h7d
TstAddrMkPrm
TstMFMClock'