Dandelion I/O Processor

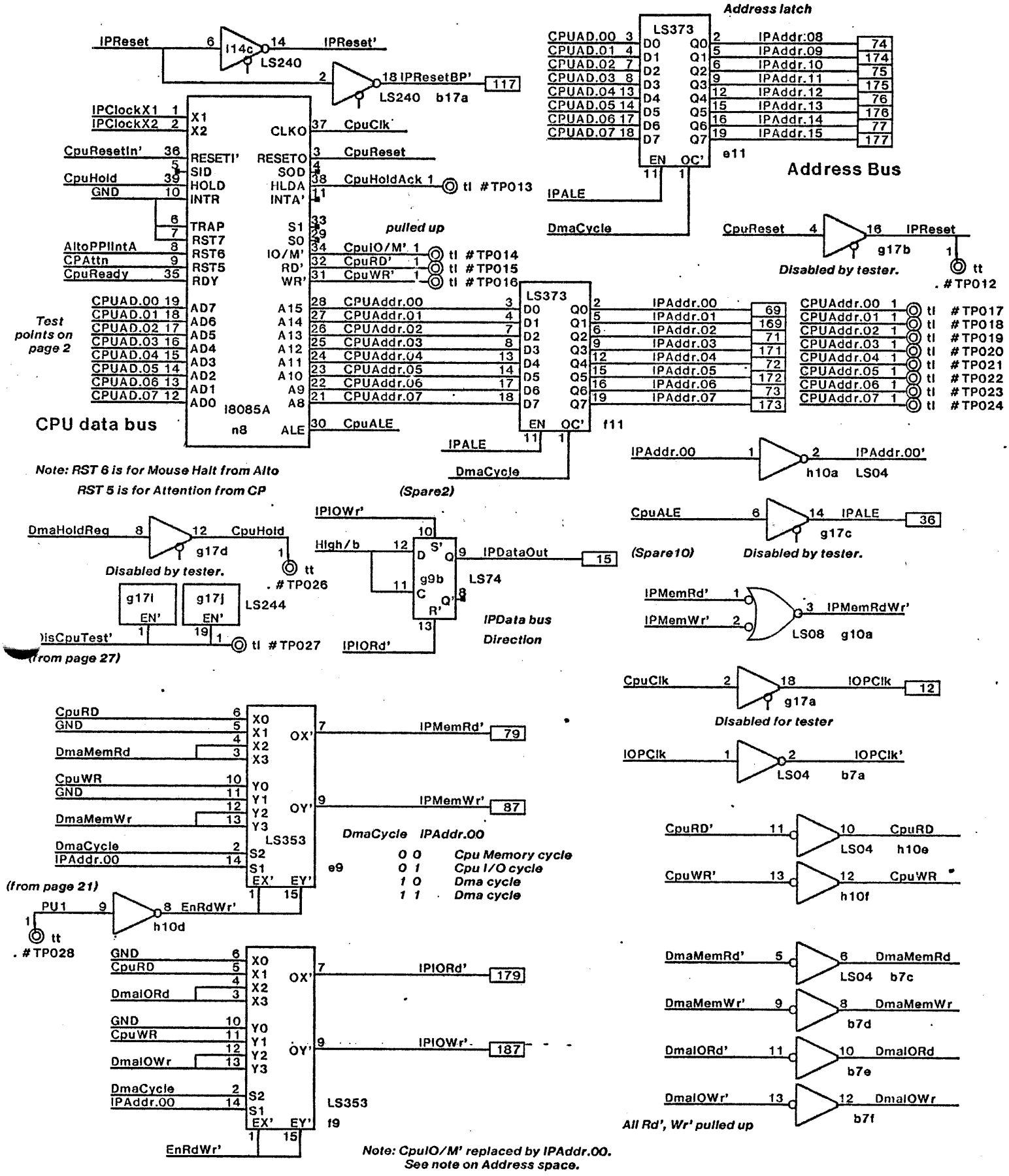
Logic Drawings

	Drawing	File
1.	CPU	DandIOP01.sil
2.	PROM, memory control	DandIOP02.sil
3.	4K RAM memory Banks 0 - 3	DandIOP03.sil
4.	4K RAM memory Banks 4 - 7	DandIOP04.sil
5.	I/O Control, memory control	DandIOP05.sil
6.	I/O Data Bus control	DandIOP06.sil
7.	DMA controller	DandIOP07.sil
8.	Floppy Disk Controller	DandIOP08.sil
9.	Floppy Disk Controller Write Comp.	DandIOP09.sil
10.	Floppy Disk Controller Miscellaneous	DandIOP10.sil
11.	Floppy Disk Receivers/Drivers	DandIOP11.sil
12.	Floppy Disk Controller Data Separator	DandIOP12.sil
13	Dma Test register	DandIOP13.sil
14.	Interrupt Request register	DandIOP14.sil
15.	CP control, Control store	DandIOP15.sil
16.	CP-IOP port - 1	DandIOP16.sil
17.	CP-IOP port - 2	DandIOP17.sil
18.	Keyboard Interface	DandIOP18.sil
19.	Mouse Interface	DandIOP19.sil
20.	Time-of-Day/Maintenance Panel interface	DandIOP20.sil
21.	Miscellaneous CPU control	DandIOP21.sil
22.	Printer Interface	DandIOP22.sil
23.	4K RAM memory Banks 8 - 11	DandIOP23.sil
24.	4K RAM memory Banks 12 - 15	DandIOP24.sil
25.	Time-of-Day clock - 1	DandIOP25.sil
26.	Time-of-Day clock - 2	DandIOP26.sil
27.	Discretes, I/O Connectors - 1	sDandIOP27.sil, pDandIOP27.sil
28.	I/O Connectors - 2	sDandIOP28.sil, pDandIOP28.sil
29.	Fuses, Power supply, Connectors (PC)	pDandIOP29.sil

Note: An "s" prefix indicates a stitchweld-specific drawing, a "p" indicates a PC-specific drawing.

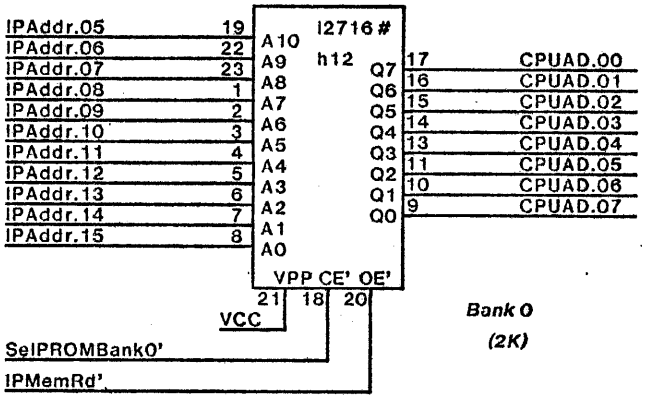
Documentation Drawings

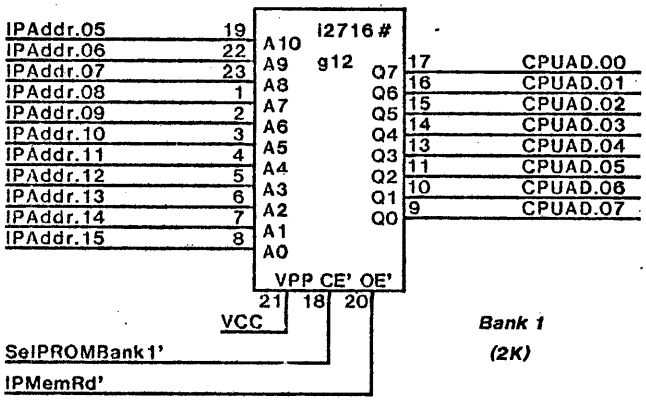
Drawing		File
0.	Drawings - Logic	DandIOP00.silx
0a.	Drawings - Documentation	DandIOP00a.silx
Timing:		
30.	Timing: Cpu-FDC	DandIOP30.silx
31.	Timing: Cpu-Mem	DandIOP31.silx
32.	Timing: Dma-FDC	DandIOP32.silx
33.	IOP-CP Communication	DandIOP33.silx
35.	Alto-IOP Communication - 1	DandIOP35.silx
36.	Alto-IOP Communication - 2	DandIOP36.silx
39.	FDC Write Comp. Timing	DandIOP39.silx
Loading:		
40.	Signal Loading - 1	DandIOP40.silx
41.	Signal Loading - 2	DandIOP41.silx
42.	Signal Loading - 3	DandIOP42.silx
Construction:		
50.	Board stuffing sheet (stitchweld)	DandIOP50.silx
51.	Board layout (stitchweld)	DandIOP51.silx
52.	Board layout (PC)	DandIOP52.silx
53.	PC Layout Notes	DandIOP53.silx
54.	List of Test Pads	DandIOP54.silx
55.	Keyboard Cable (stitchweld)	DandIOP55.silx
56	Floppy Disk Signal Cable, Misc. cable (sw)	DandIOP56.silx
57.	Floppy Disk Cables (stitchweld)	DandIOP57.silx
58.	IOP Platforms (stitchweld)	DandIOP58.silx
59.	IOP Platforms (stitchweld)	DandIOP59.silx
Notes:		
60.	Revision History - 1	DandIOP60.silx
61.	Revision History - 2	DandIOP61.silx
62.	Revision History - 3	DandIOP62.silx
63.	Design Notes	DandIOP63.silx
Programming:		
70.	I/O Processor Address space - Memory	DandIOP70.silx
71.	I/O Processor Address space - I/O	DandIOP71.silx
72.	I/O Control and Status Register Formats	DandIOP72.silx
75.	CP IOP Task programming	DandIOP75.silx
Block Diagrams:		
80.	IOP Data Paths	DandIOP80.silx
81.	IOP Control	DandIOP81.silx
82.	Floppy Disk Controller Block Diagram	DandIOP82.silx
83.	CP-IOP port block diagram	DandIOP83.silx
Parts:		
	IOP parts list - 1	IOPParts1-G.sil
	IOP parts list - 2	IOPParts2-G.sil

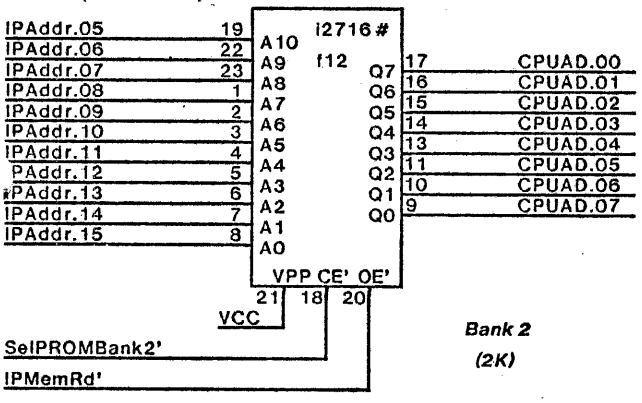


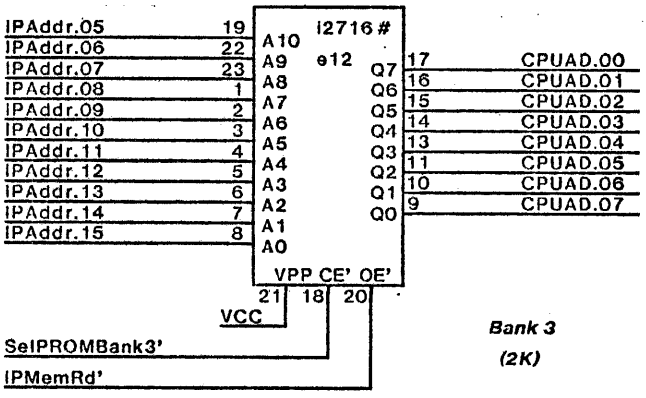
XEROX SDD	Project: Dandelion	I/O Processor CPU	File: DandIOP01.sil	Designer: Ogus	Rev: J	Date: 5/8/80	Page: 01

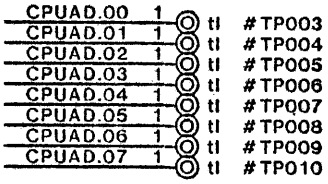
Prom





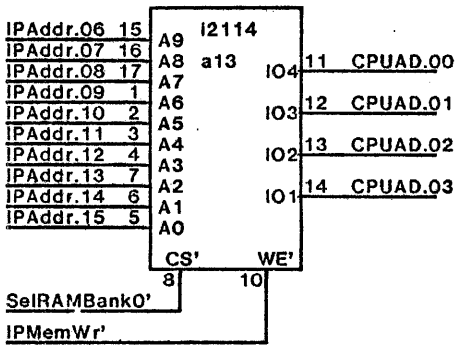


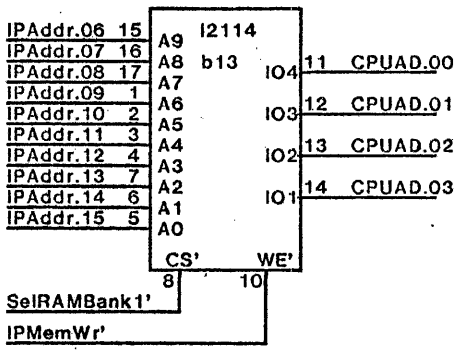


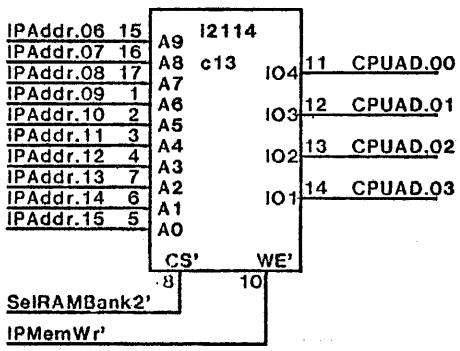


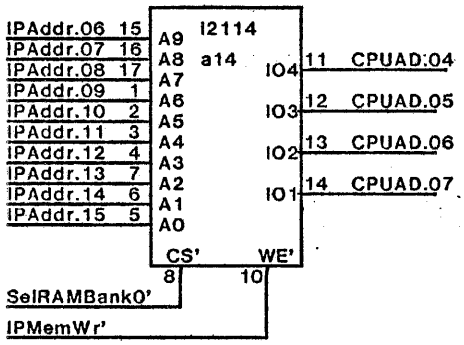
XEROX SDD	Project: Dand/IOP	I/O Processor PROM	File: DandIOP02.sil	Designer: Ogus	Rev: J	Date: 5/8/80	Page: 02

RAM - Banks 0 - 3

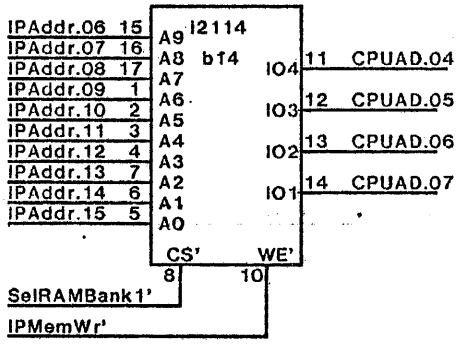




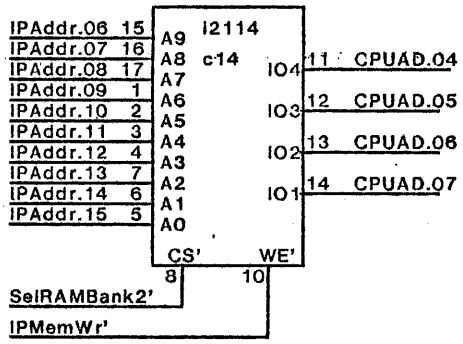




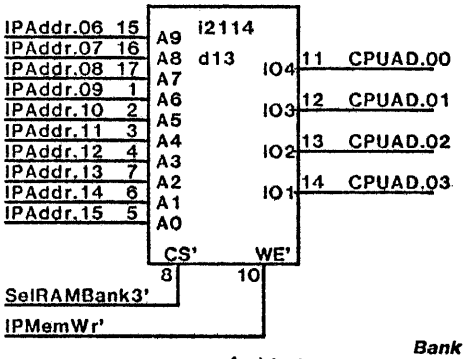
Bank 0



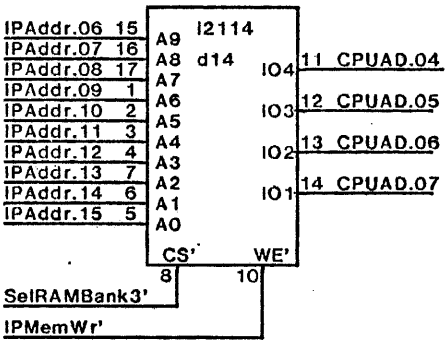
Bank 1



Bank 2

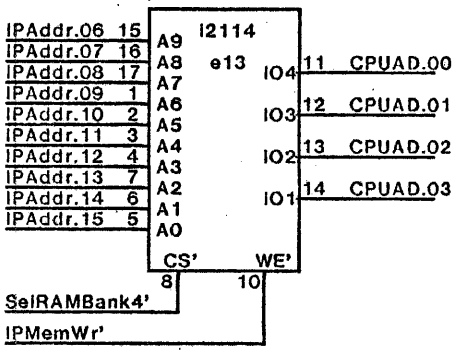


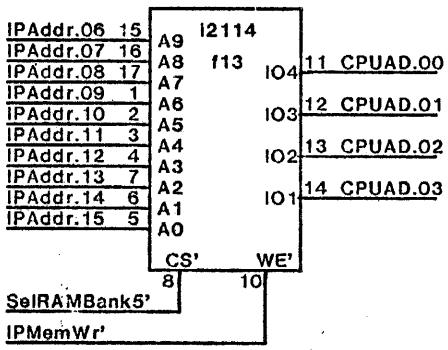
Bank 3

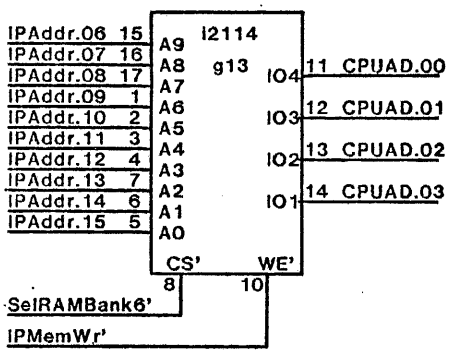


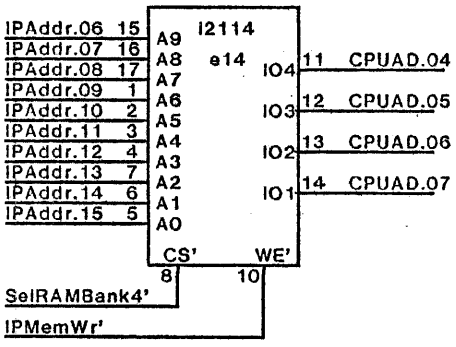
XEROX SDD	Project: Dand/IOP	I/O Processor 4K RAM Memory-Banks 0 - 3	File: DandIOP03.sil	Designer: Ogus	Rev: J	Date: 10/24/79	Page: 03

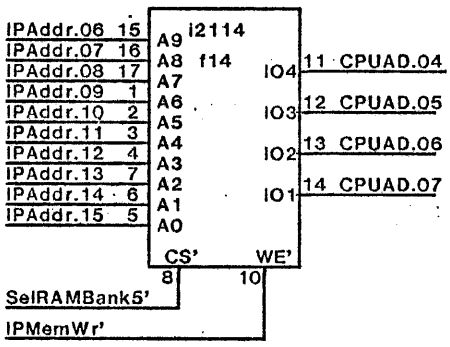
RAM - Banks 4 - 7

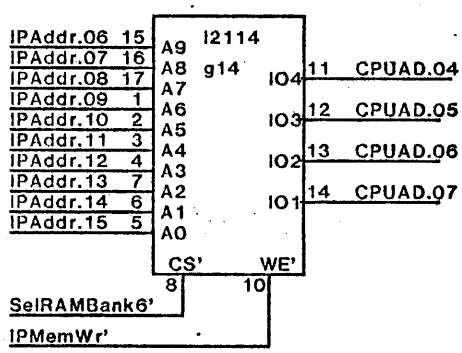




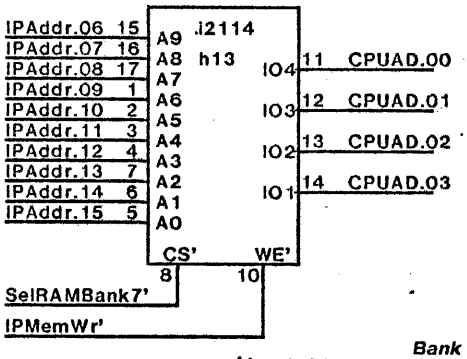


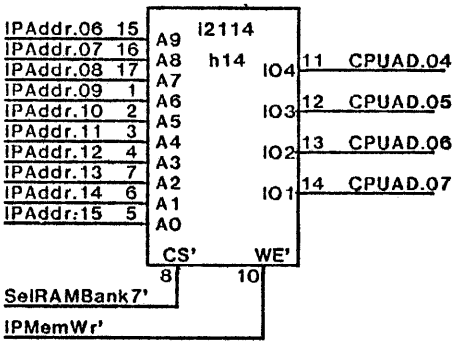






Bank 4 *Bank 5* *Bank 6*



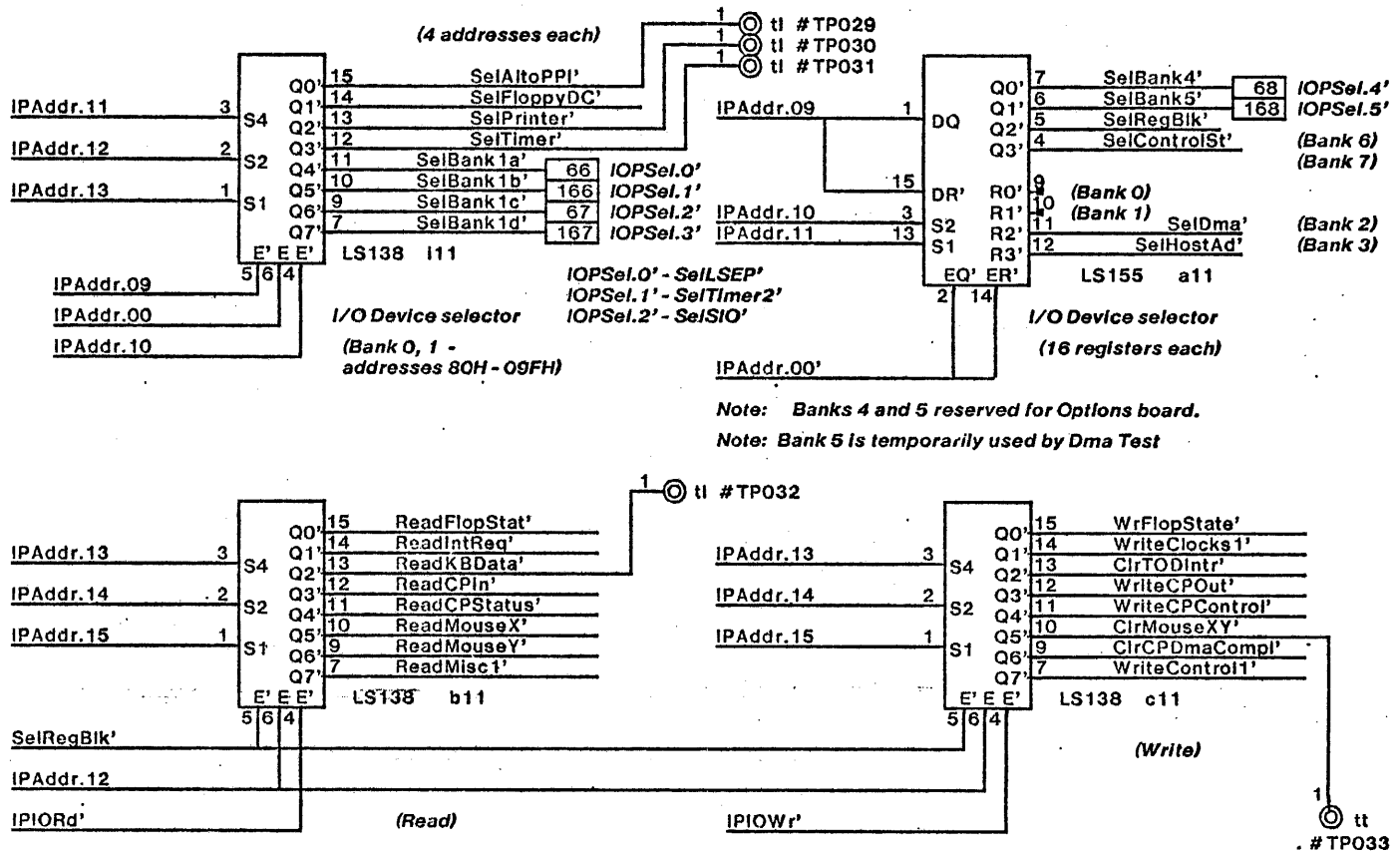


Bank 7

XEROX SDD	Project Dandelion	I/O Processor 4K RAM Memory-Banks 4-7	File DandIOP04.sil	Designer Ogus	Rev J	Date 10/24/79	Page 04

I/O Control

(Depends on Addr[0] = Addr[8], etc. for I/O. IPAddr[0] = 1 for I/O addresses.)

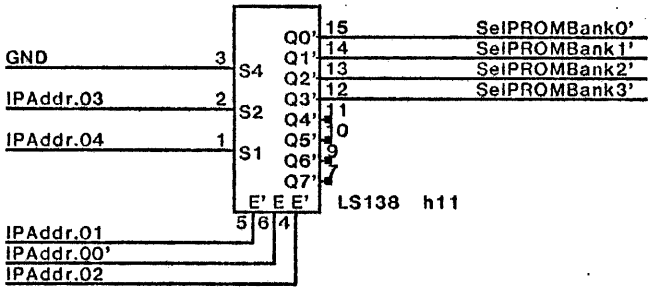


Note: Banks 4 and 5 reserved for Options board.

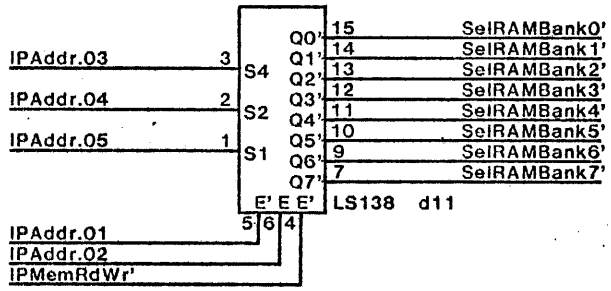
Note: Bank 5 is temporarily used by Dma Test

Single Register Block
(Bank 6, registers 8-15, addresses 0E3H - 0EFH)

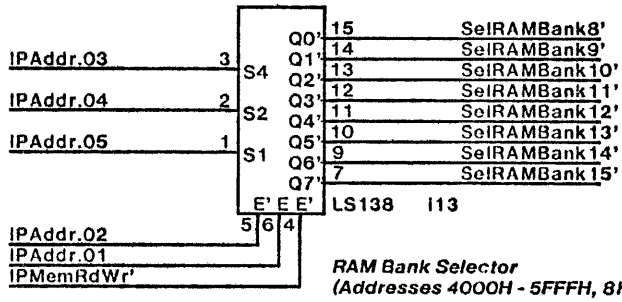
Memory Control



PROM Bank Selector
(Addresses Bank 0: 0 - 7FFH,
Bank 1: 800H - 0FFFH,
Bank 2: 1000H - 17FFH,
Bank 3: 1800H - 1FFFH)

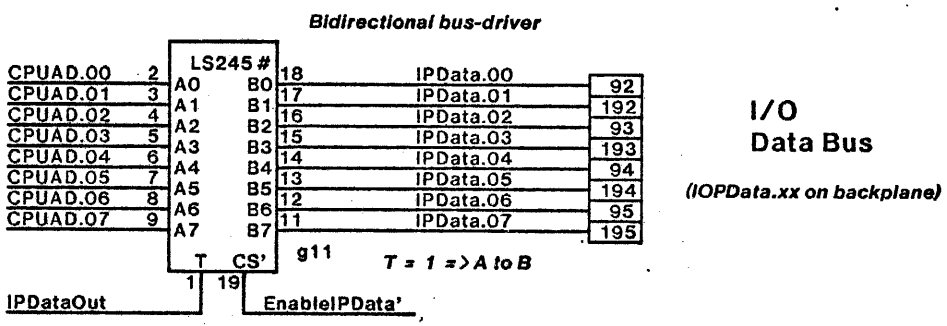


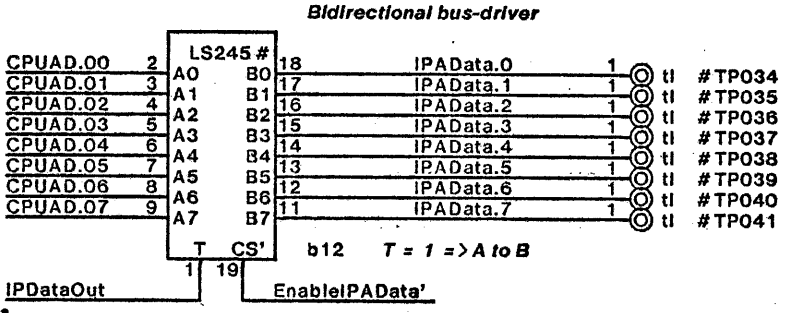
RAM Bank Selector
(Addresses 2000H - 3FFFH, 8K)

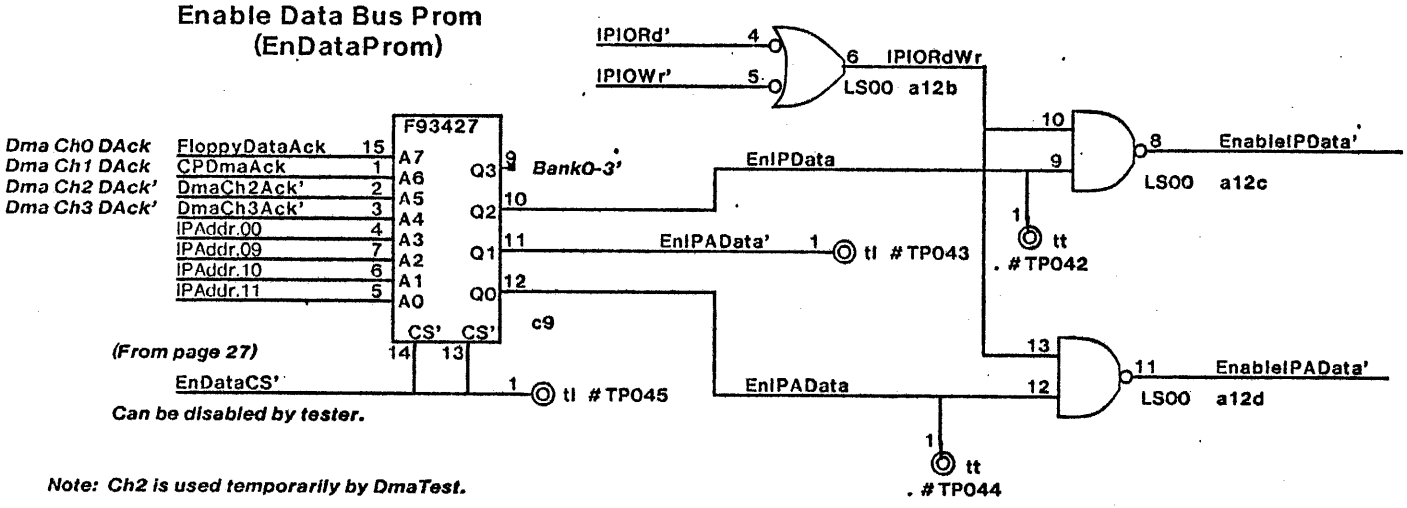


RAM Bank Selector
(Addresses 4000H - 5FFFH, 8K)

XEROX SDD	Project: Dandelion	I/O Processor I/O Control, memory Control	File: DandIOP05.sil	Designer: Ogus	Rev: J	Date: 5/9/80	Page: 05



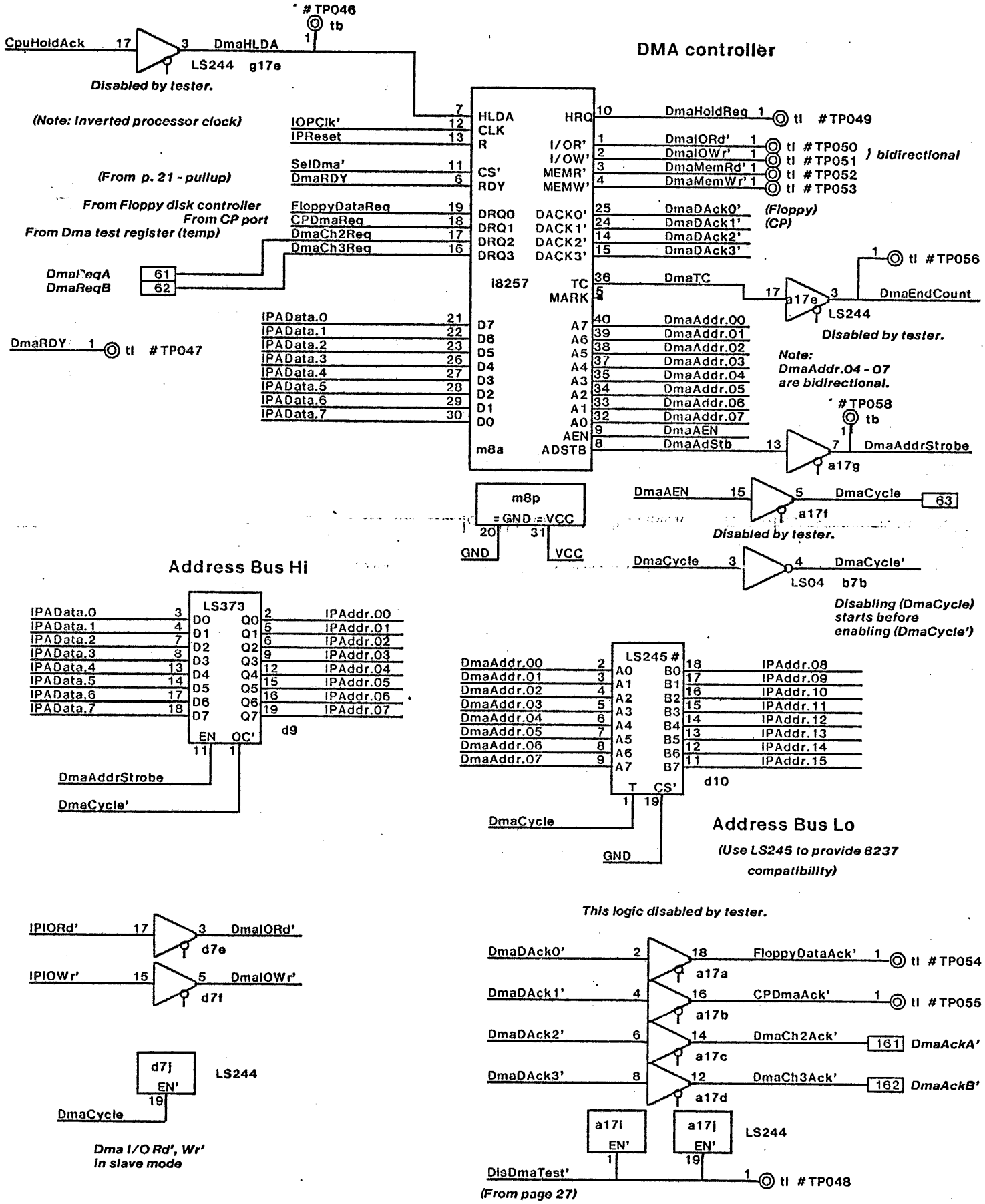




Note: Ch2 is used temporarily by DmaTest.

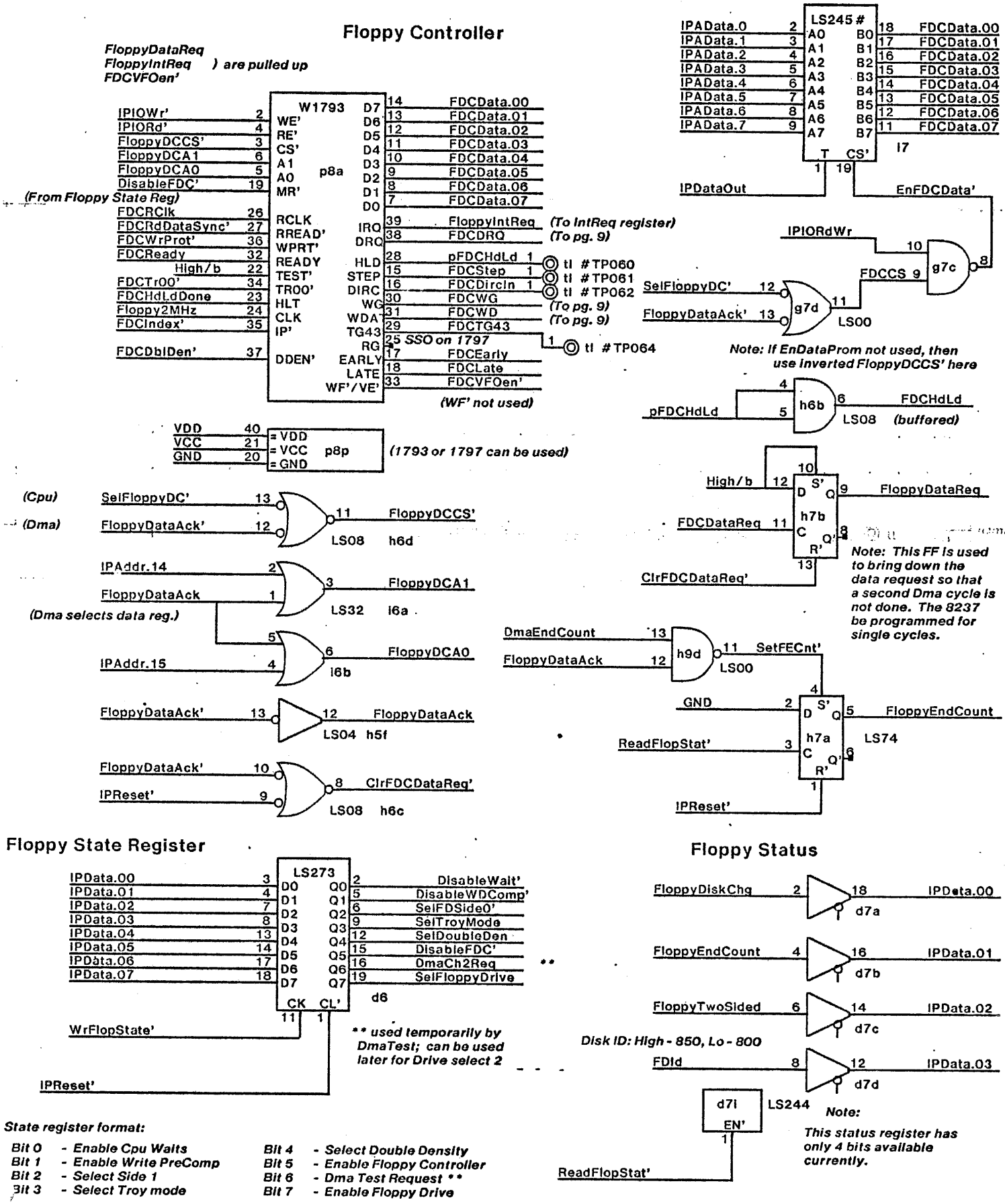
Note: Do not use DMA memory addresses in the I/O Address space.

XEROX SDD	Project	I/O Processor	File	Designer	Rev	Date	Page
	Dandelion	I/O Data Bus Control	DandIOP06.sil	Ogus	J	5/8/80	06



XEROX SDD	Project Dandelion	I/O Processor DMA Controller	File DandIOP07.sil	Designer Ogus	Rev J	Date 5/9/80	Page 07

Floppy Controller



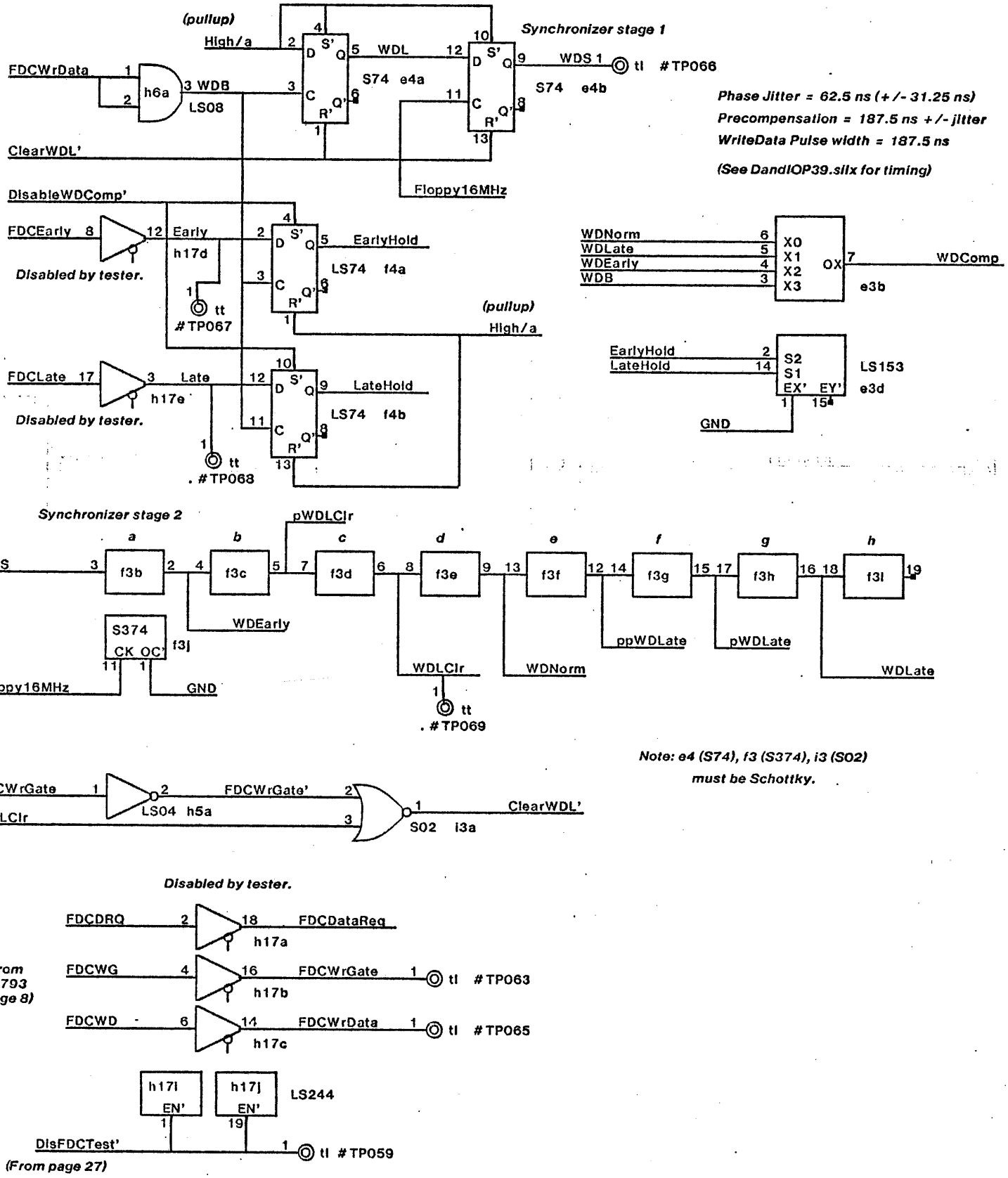
Floppy State Register

Floppy Status

State register format:

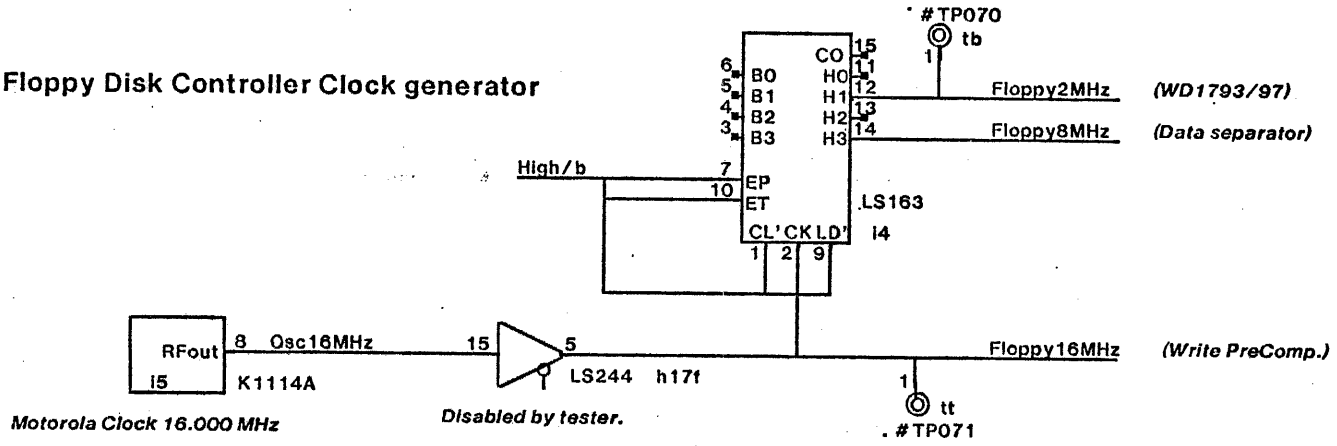
Bit 0	- Enable Cpu Waits	Bit 4	- Select Double Density
Bit 1	- Enable Write PreComp	Bit 5	- Enable Floppy Controller
Bit 2	- Select Side 1	Bit 6	- Dma Test Request **
Bit 3	- Select Troy mode	Bit 7	- Enable Floppy Drive

XEROX SDD	Project Dandelion	I/O Processor Floppy Controller	File DandIOP08.sil	Designer Ogus	Rev J	Date 5/9/80	Page 08

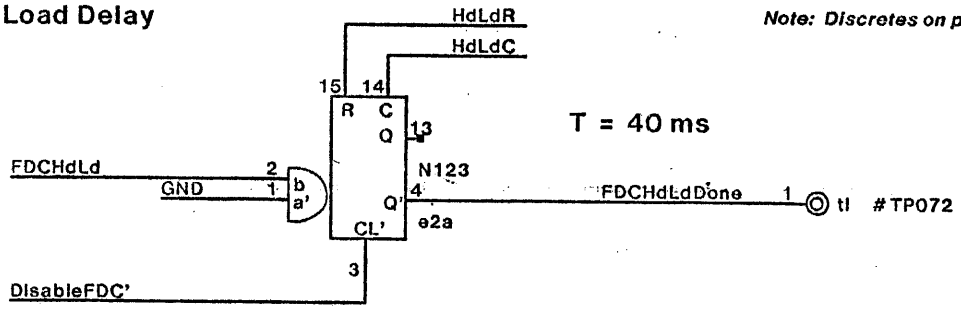


XEROX SDD	Project Dandelion	I/O Processor Floppy Controller Write Comp.	File DandIOP09.sil	Designer Ogus	Rev J	Date 5/8/80	Page 09

Floppy Disk Controller Clock generator

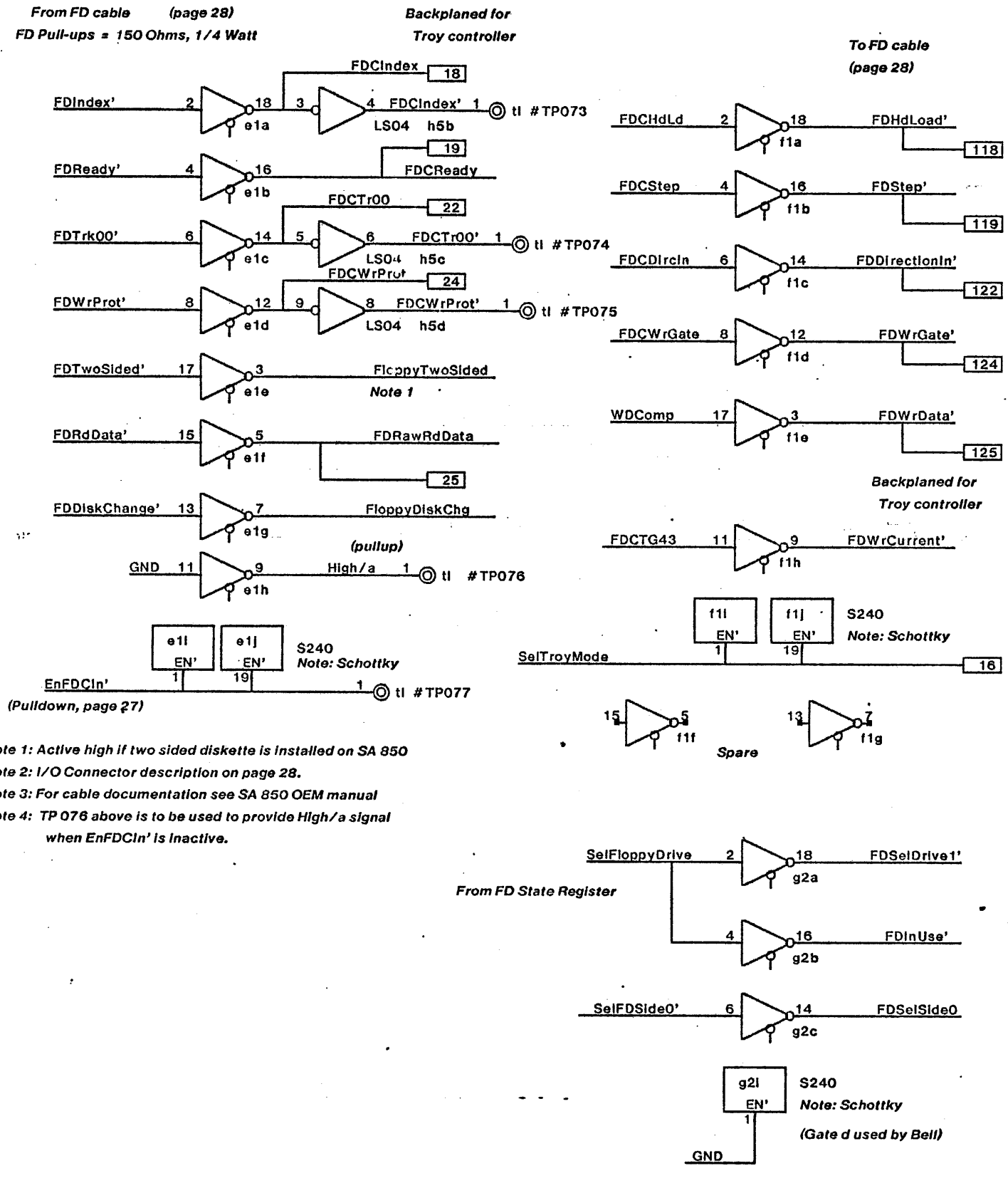


Head Load Delay



Note: Discretes on page 27

XEROX SDD	Project: Dandelion	I/O Processor Floppy Controller Miscellaneous	File: DandIOP10.sil	Designer: Ogus	Rev: J	Date: 5/8/80	Page: 10



Note 1: Active high if two sided diskette is installed on SA 850

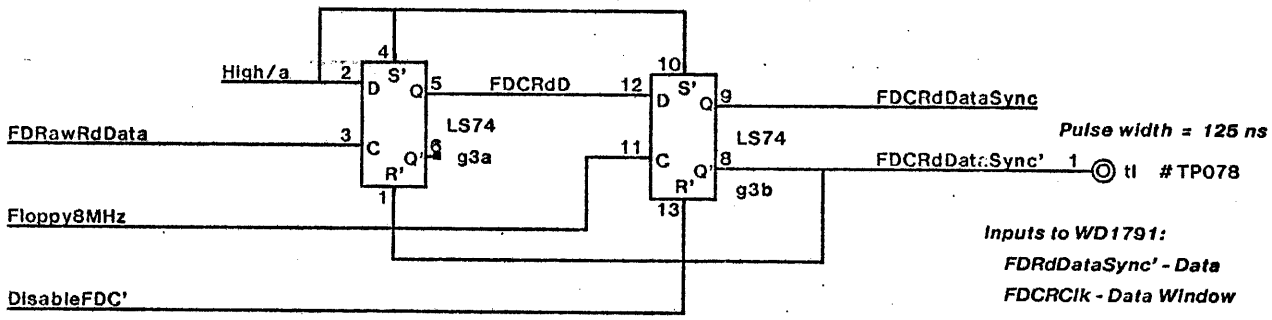
Note 2: I/O Connector description on page 28.

Note 3: For cable documentation see SA 850 OEM manual

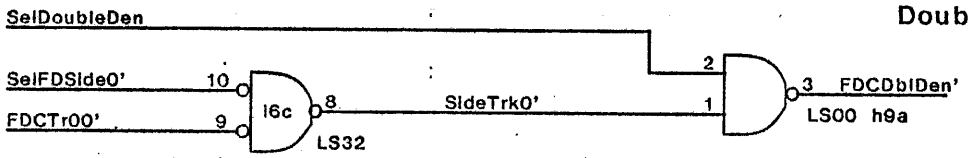
Note 4: TP 076 above is to be used to provide High/a signal when EnFDCIn' is inactive.

XEROX SDD	Project: Dandelion	I/O Processor Floppy Disk Receivers/Drivers	File: DandIOP11.sil	Designer: Ogus	Rev: J	Date: 5/9/80	Page: 11

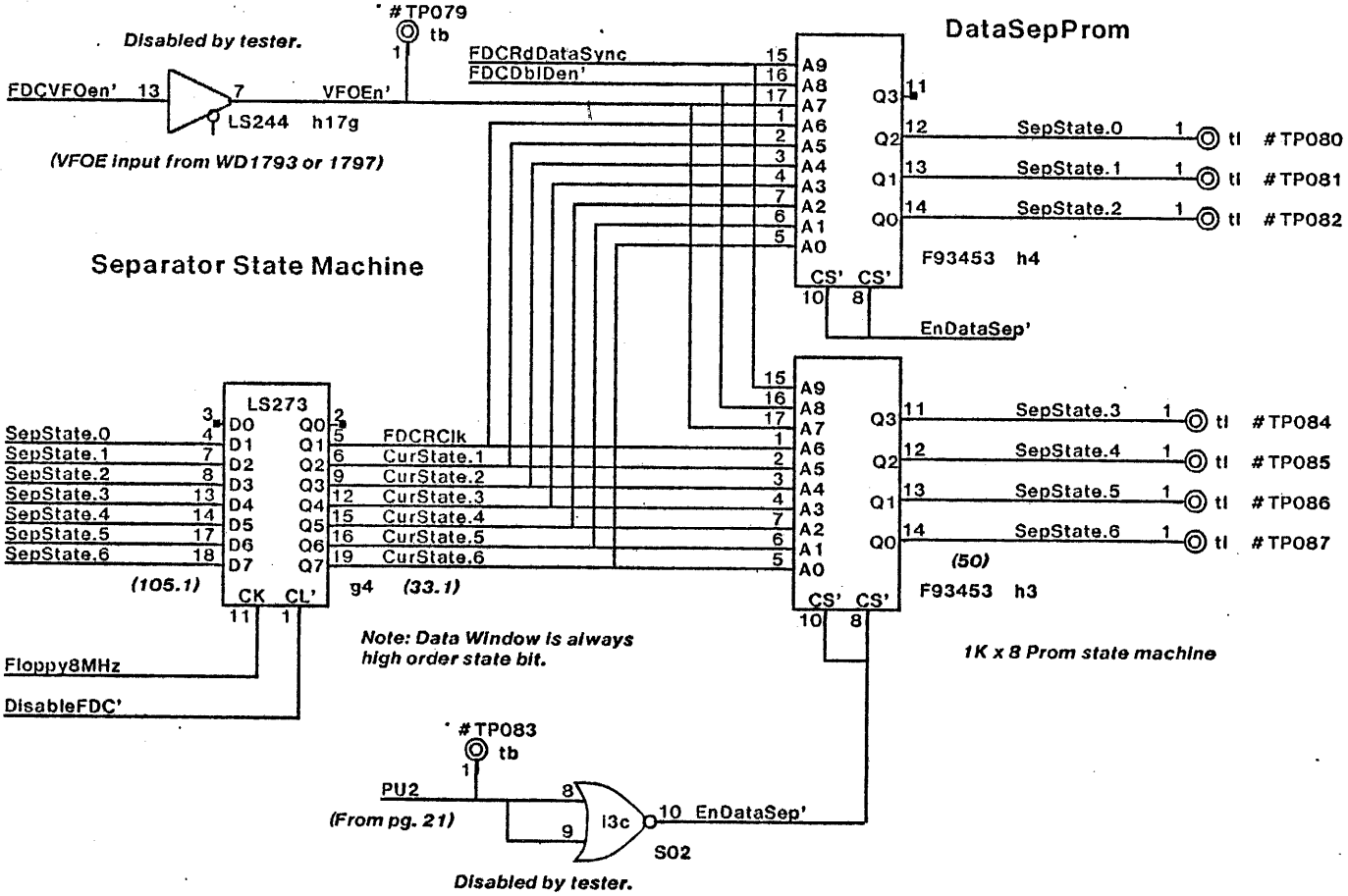
Raw Read Data synchronizer and pulse shaper



Double density selection



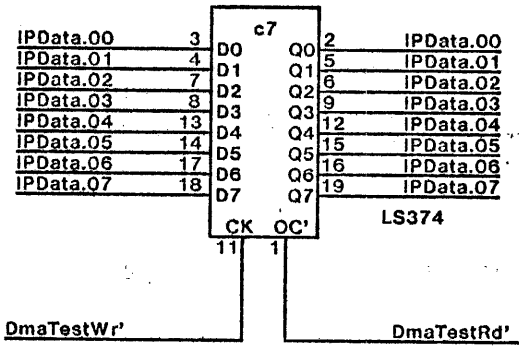
DDen = SelDoubleDen . (SelSide0.Track00)'

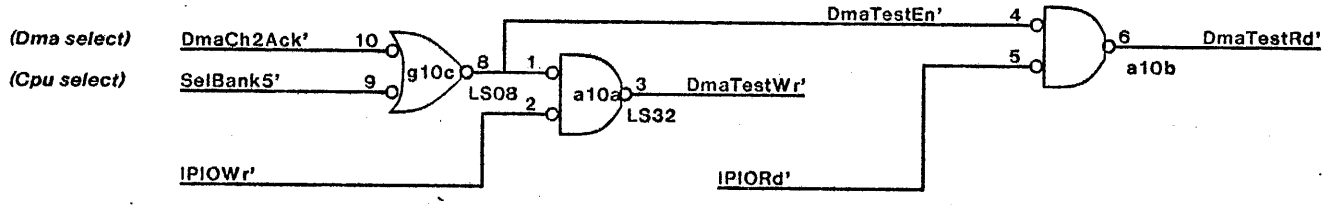


XEROX SDD	Project Dandelion	I/O Processor Floppy Data Separator	File DandIOP12.sil	Designer Ogus	Rev J	Date 5/8/80	Page 12

DMA Test Register

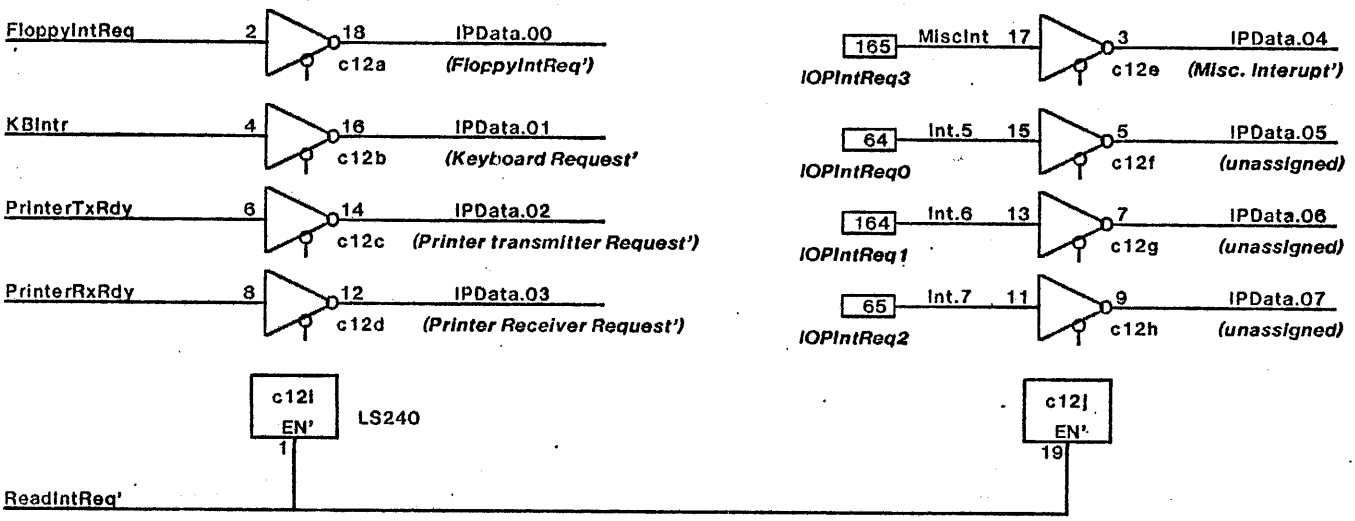
For testing Dma controller independently of Floppy disk.
This register uses Dma channel 2 temporarily, and SelBank5' to enable.
Can be removed later.





XEROX SDD	Project Dandelion	I/O Processor DMA Test	File DandIOP13.sil	Designer Ogus	Rev J	Date 2/22/80	Page 13

Interrupt Request Register



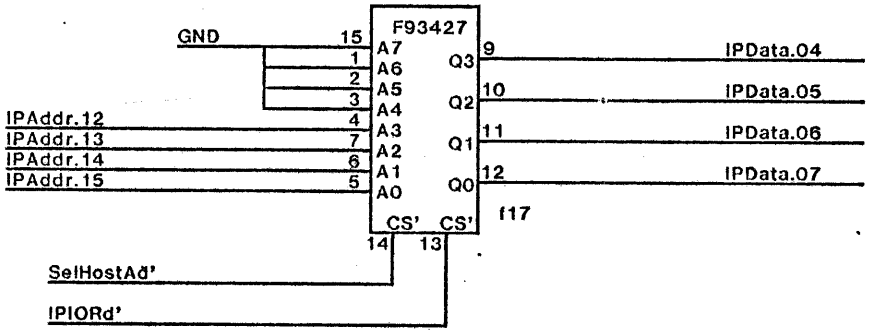
This register contains the interrupt requests of various devices.
To read true value of the requests, XOR with XOR vector = 1111 1111 (0FFH)

Temporary:

IOPIntReq0 - RS232C - Options
IOPIntReq1 - LSEP UART Tx - Options
IOPIntReq2 - LSEP UART Rx - Options
IOPIntReq3 - Miscellaneous interrupt (from Timer)

Host Address Prom

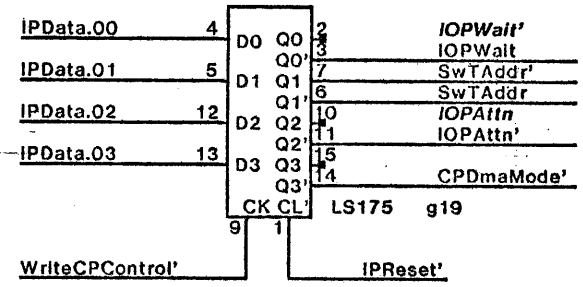
(HostAddrProm)



Host address is 48 bits long, stored in addresses 0 - 11 of the Prom.
Address 12 should contain a 4-bit checksum of the address.
Host address Prom has the 16 I/O Bank 3 addresses.

I/O address	*Host address bits*
0B0H	*0:3*
/	/
0BCH	*44:47*
0BDH	*checksum*

Central processor control
CP port control

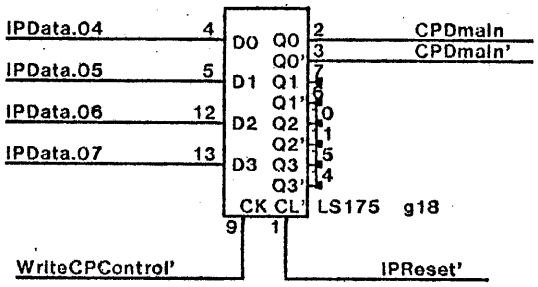


(IOPWait and SwTAddr should be true after booting)

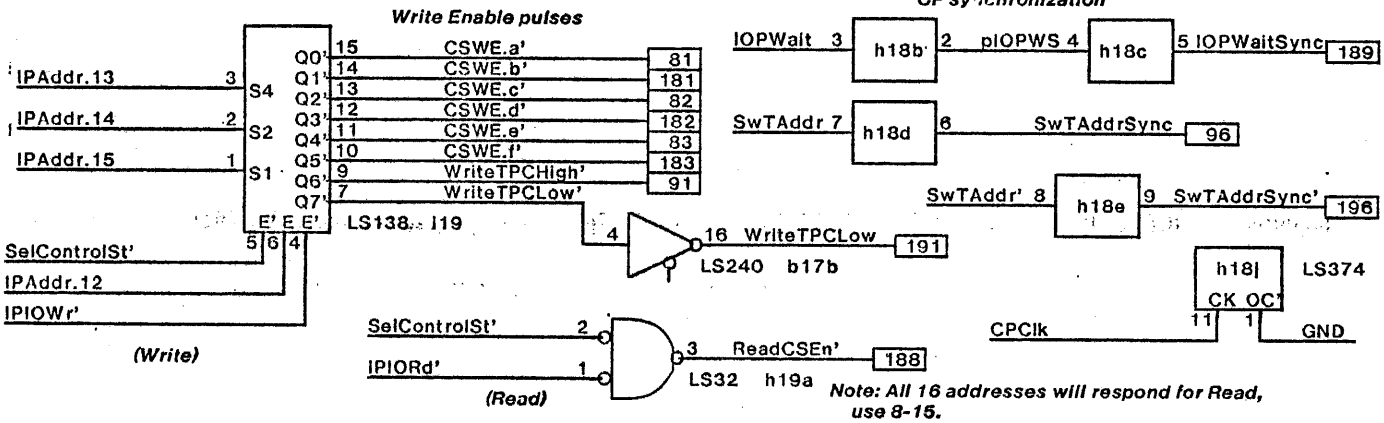
Data:

- *Bit 0 - Enable CP (remove Wait)*
- *Bit 1 - Switch TPC address from NIAX*
- *Bit 2 - Set CP Attention*
- *Bit 3 - Set Dma Mode for CP port*
- *Bit 4 - Set Dma Mode for CPport as Input/output'*

Normal state of register is 1100 0xxx



Control Store handling

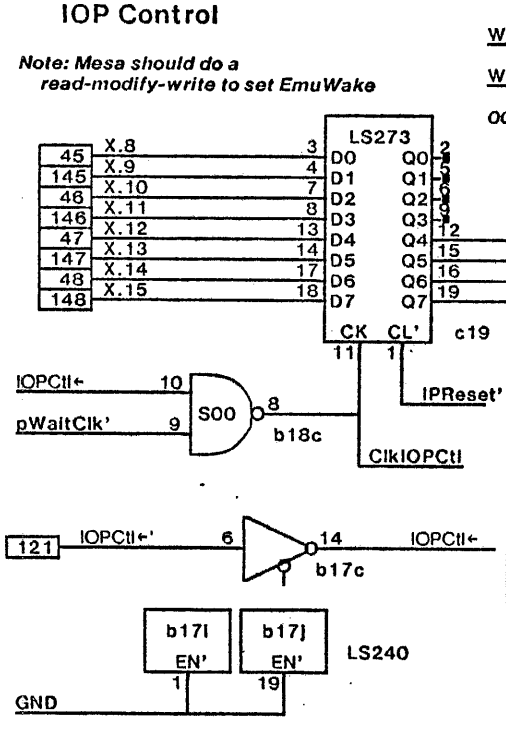


(Bank 7, registers 8-15, addresses OF8 - OFFH)

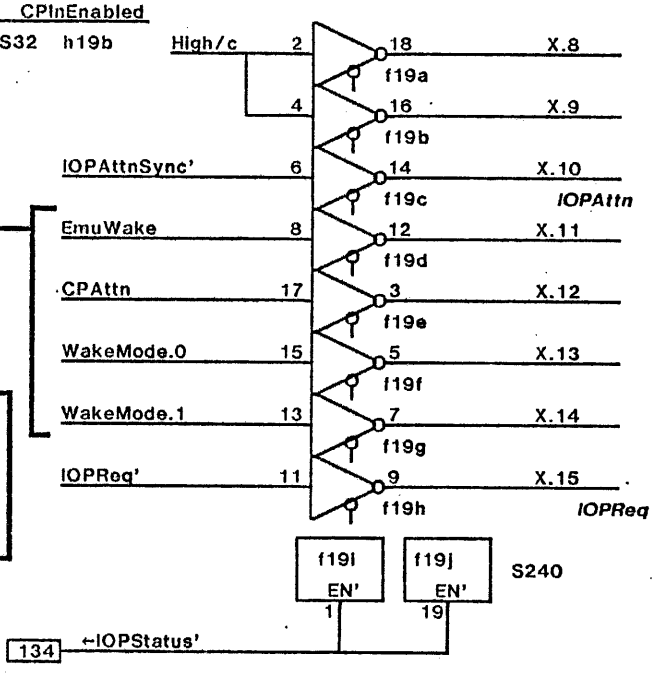
Central Processor registers

IOP Control

Note: Mesa should do a read-modify-write to set EmuWake

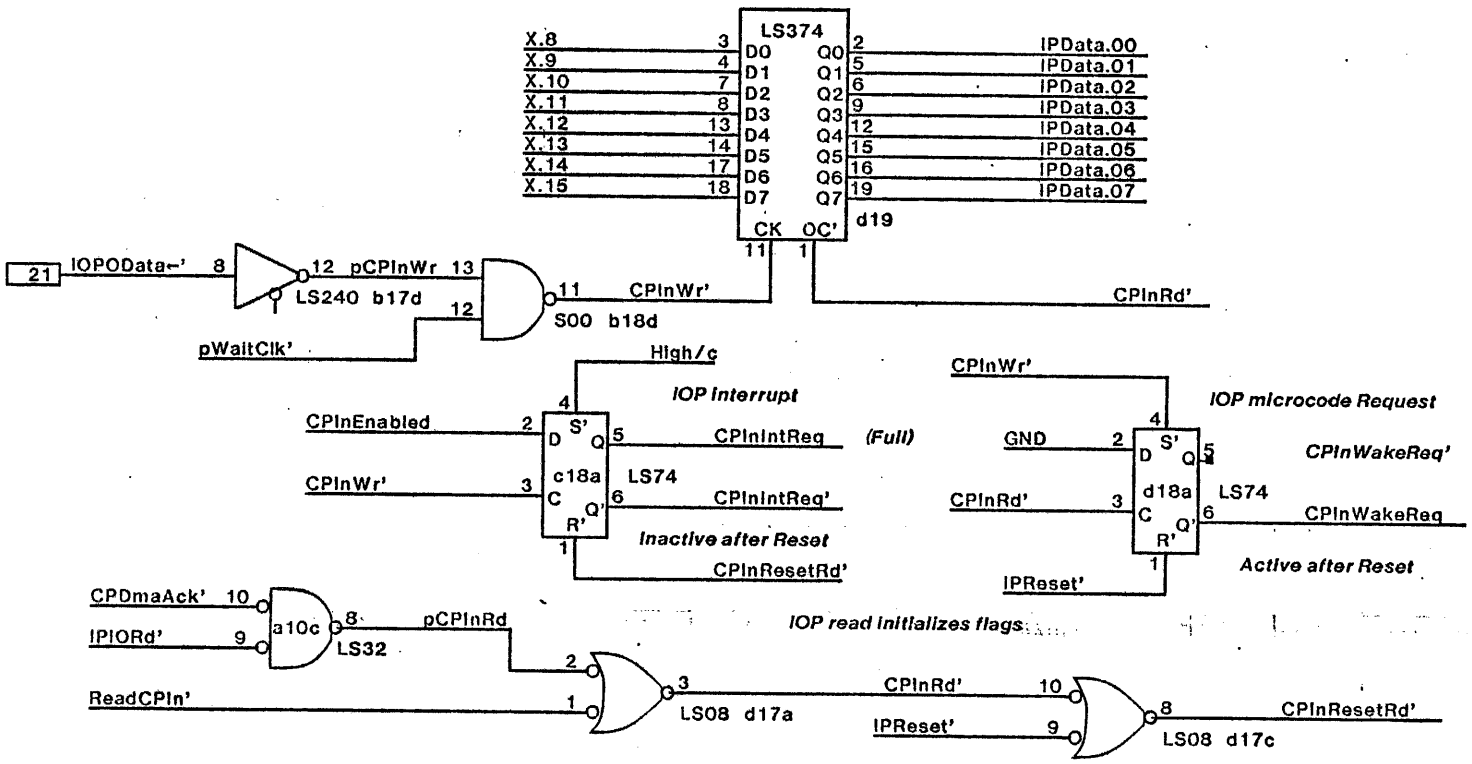


IOP Status

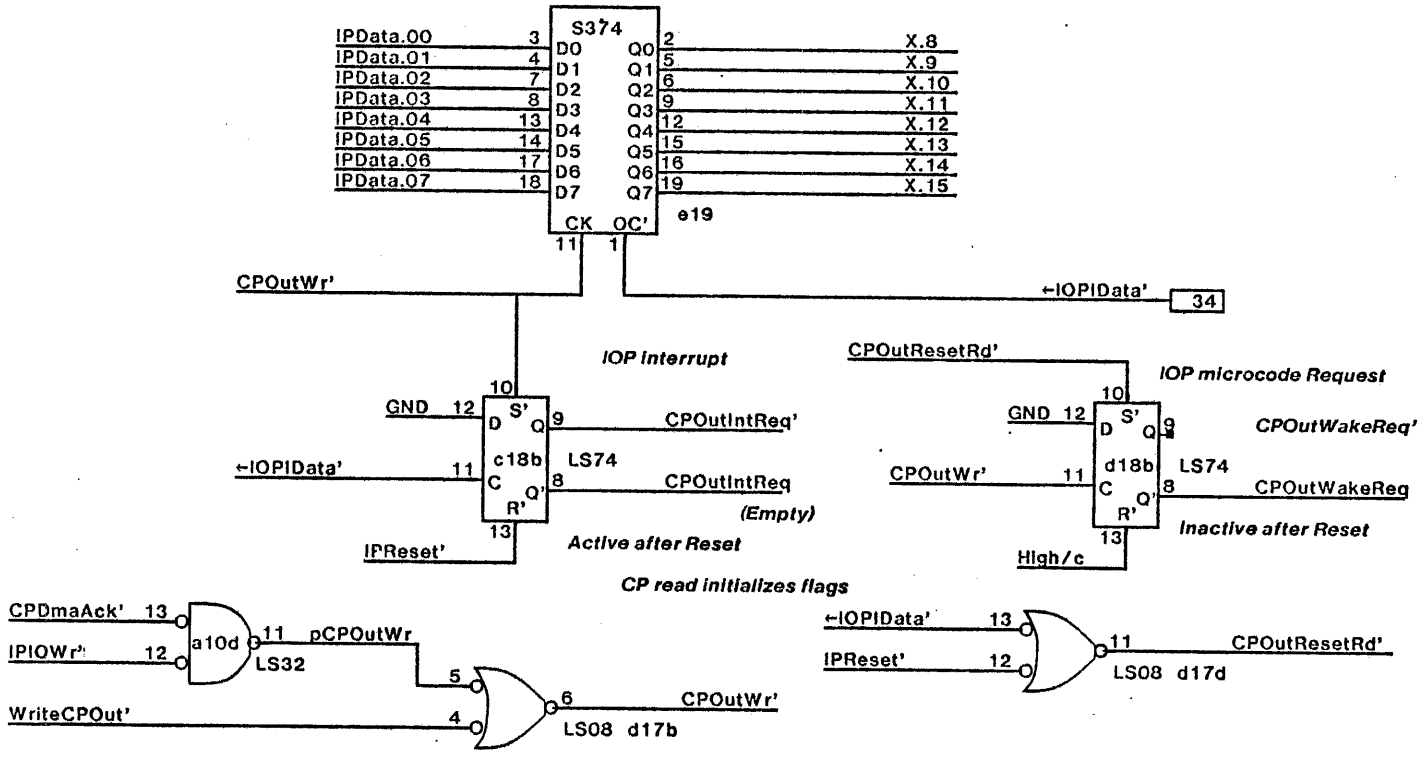


XEROX SDD	Project: Dandelion	I/O Processor CP Control and Control Store	File: DandIOP15.sil	Designer: Ogus	Rev: J	Date: 5/8/80	Page: 15

CPIn *(From CP)*

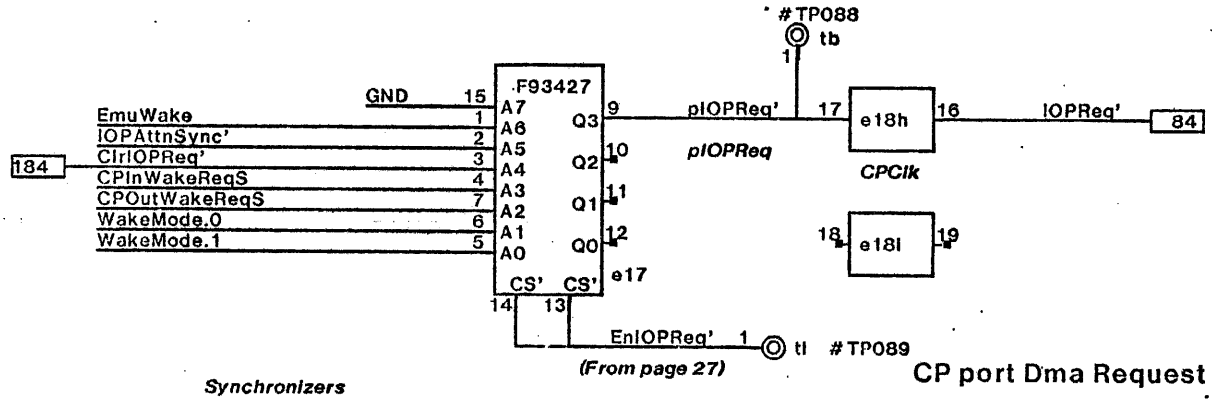


CPOut *(To CP)*

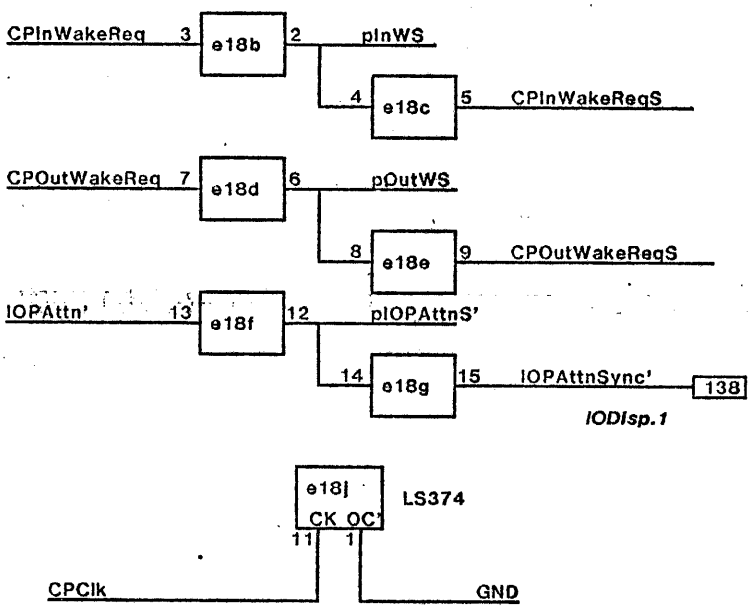


XEROX SDD	Project Dandelion	I/O Processor CP-IOP port	File DandIOP16.sil	Designer Ogus	Rev J	Date 2/26/80	Page 16

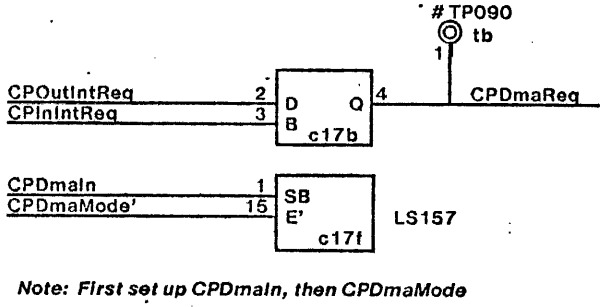
IOPReq



Synchronizers

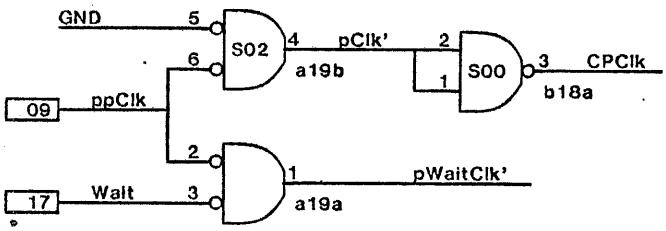


CP port Dma Request

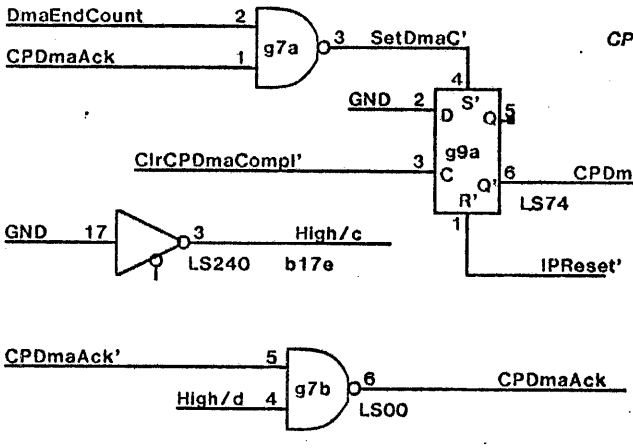


Note: First set up CPDmaIn, then CPDmaMode

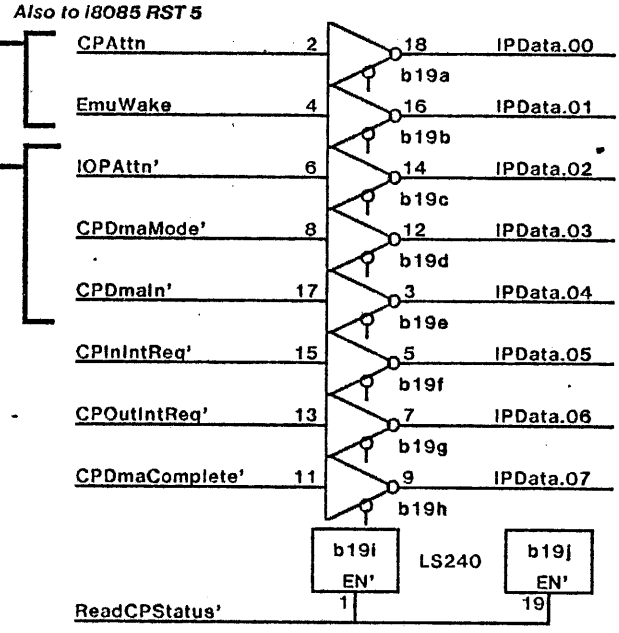
CP Clock



CP port Dma Complete

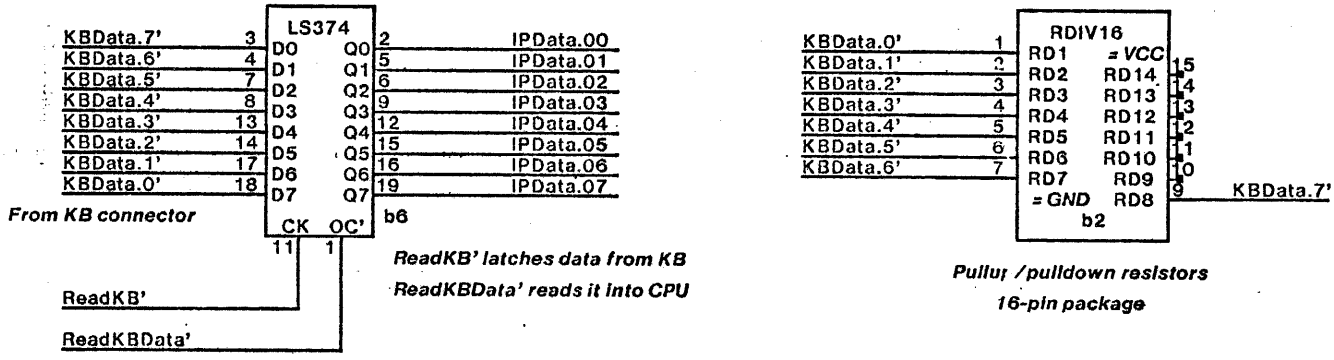


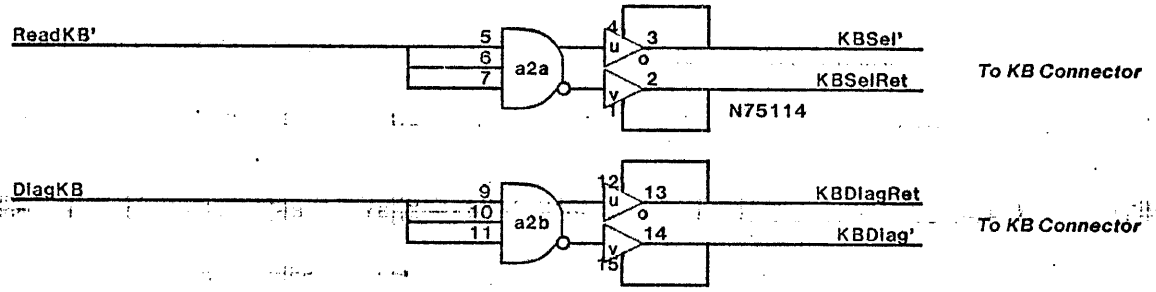
CP port status

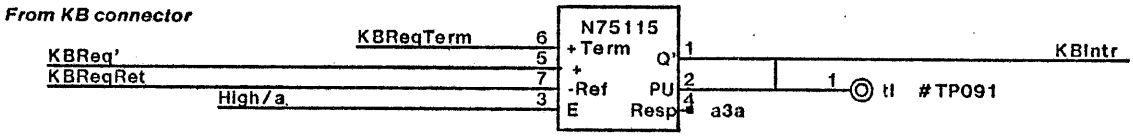


XEROX SDD	Project: Dandelion	I/O Processor CP-IOP port - 2	File: DandIOP17.sil	Designer: Ogus	Rev: J	Date: 5/8/80	Page: 17

Keyboard Data







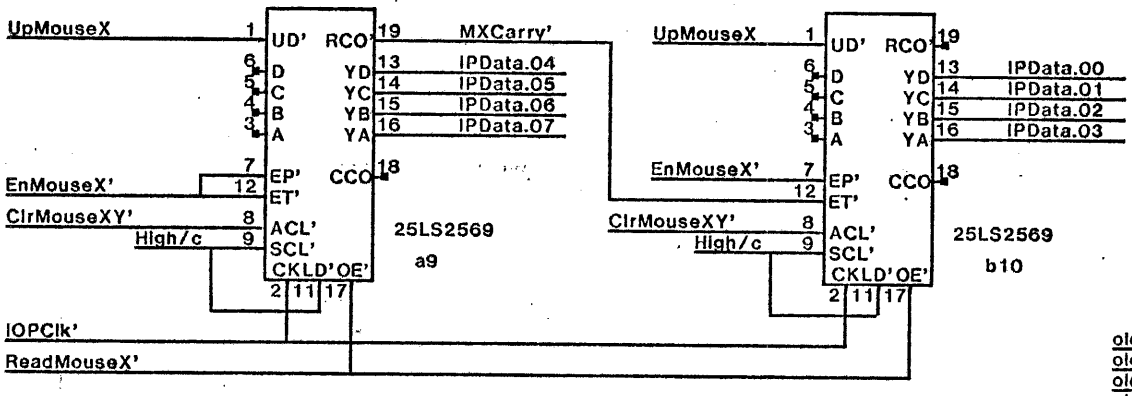
KBReqTerm connected through 1000 pF capacitor to KBReqRet

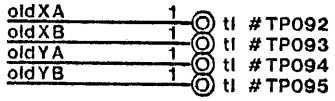
(see page 27)

Bell circuit on page 27.

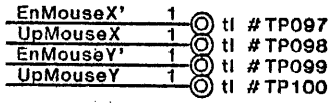
XEROX SDD	Project Dandelion	I/O Processor Keyboard Interface	File DandIOP18.sil	Designer Ogus	Rev J	Date 5/8/80	Page 18

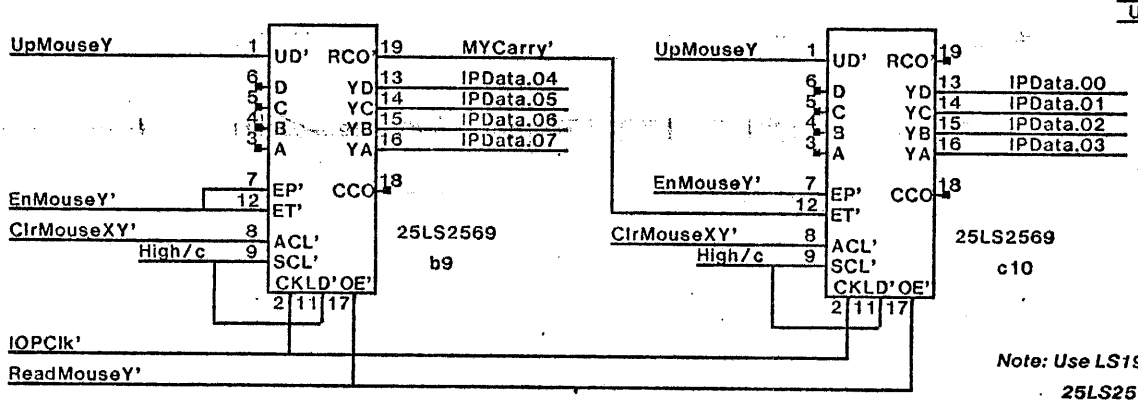
X-coordinate





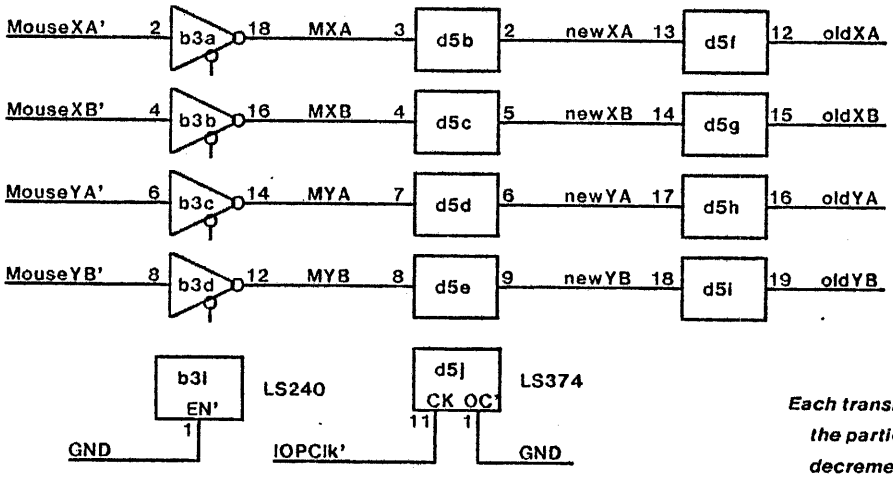
Y-coordinate



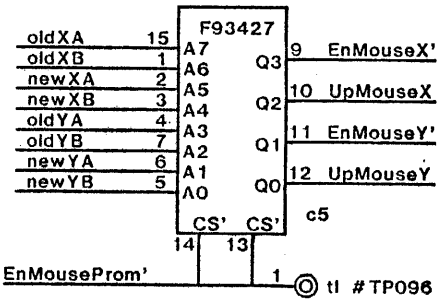


Note: Use LS191 + LS244 if not 25LS2569

From KB connector *New sample* *Old sample*



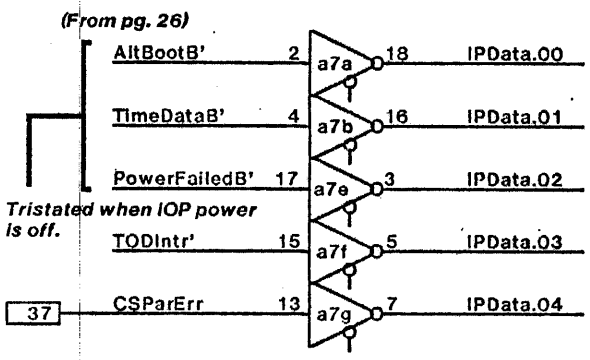
MouseProm



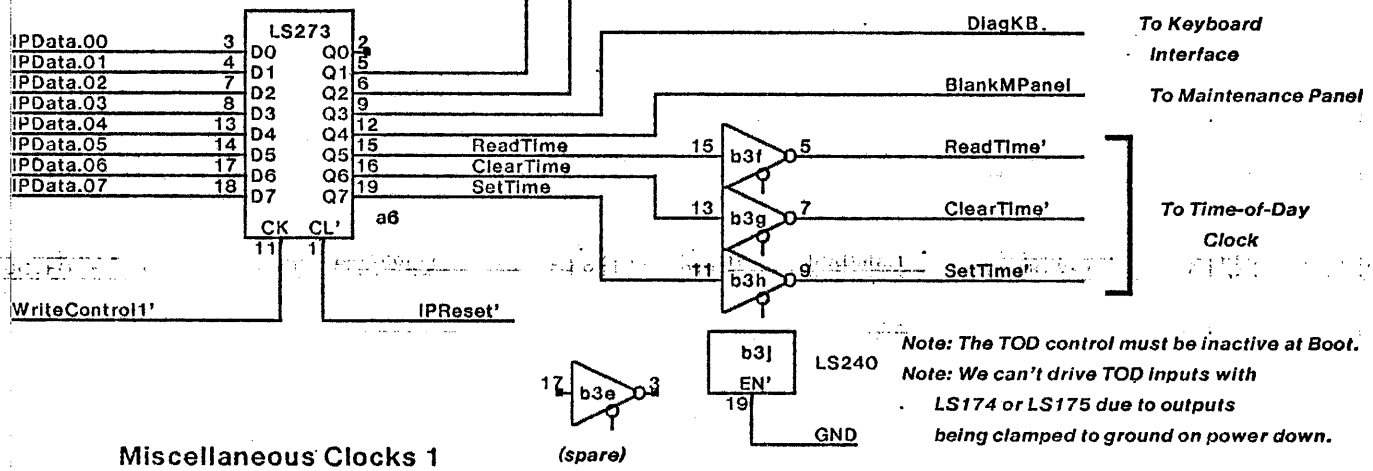
Each transition of XA or XB (YA or YB) causes the particular counter to be incremented or decremented. The samples are made with the inverted processor clock to ensure that the counters are stable when a read or clear of the counters is done.

XEROX SDD	Project Dandelion	I/O Processor Mouse interface	File DandIOP19.sil	Designer Ogus	Rev J	Date 5/8/80	Page 19

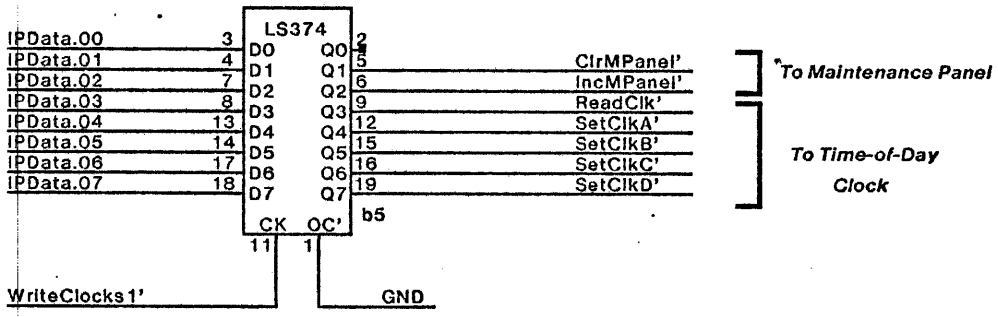
Miscellaneous Input 1



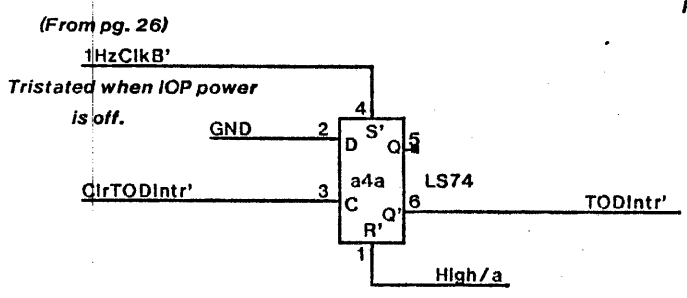
Miscellaneous control 1



Miscellaneous Clocks 1



Time-of-Day 1 second interrupt



Procedure to read time:

- *Wait for TODIntr to be set*
- *When set, clear and wait for it to be set again*
- *read time*

(maximum delay = 2 seconds)

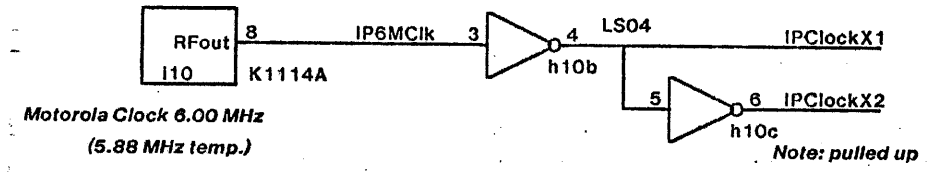
Alternative:

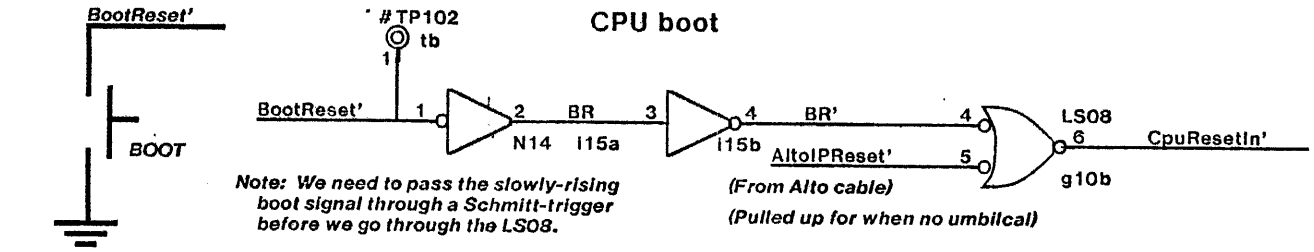
- *clear TODIntr (if being set will not be cleared)*
- *wait until set*
- *read time*

(maximum delay = 1 second)

XEROX SDD	Project: Dandelion	I/O Processor TOD/MP interface, misc. reg.	File: DandIOP20.sil	Designer: Ogus	Rev: J	Date: 5/8/80	Page: 20

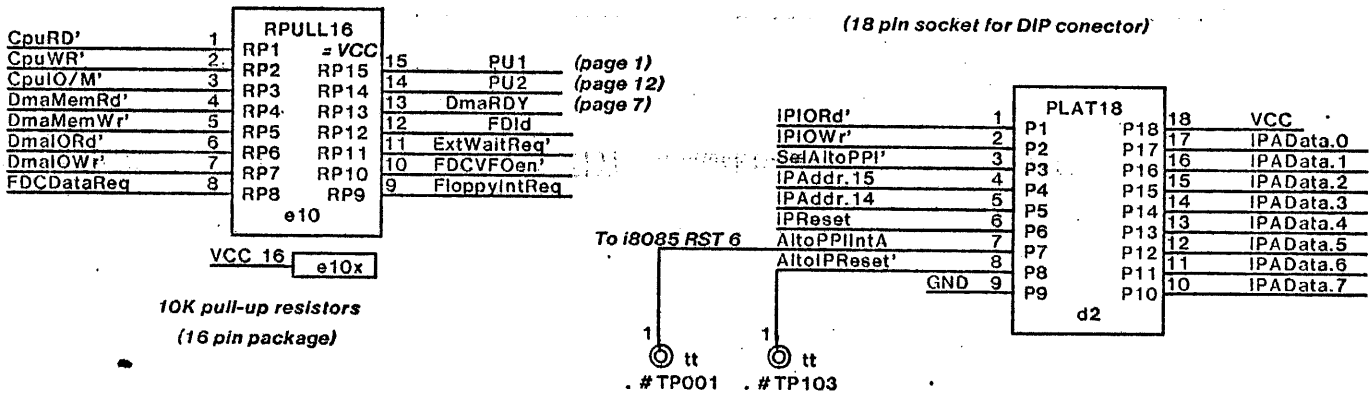
IOP CPU Clock generator

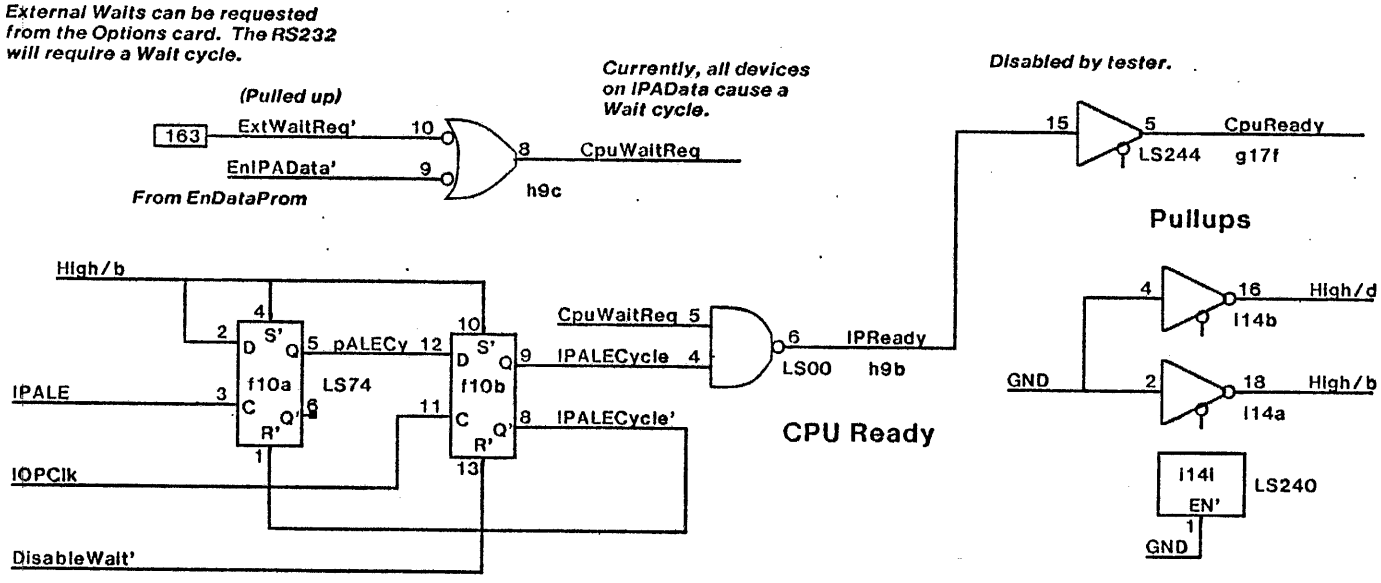




Dip Cable to Alto-IOP interface

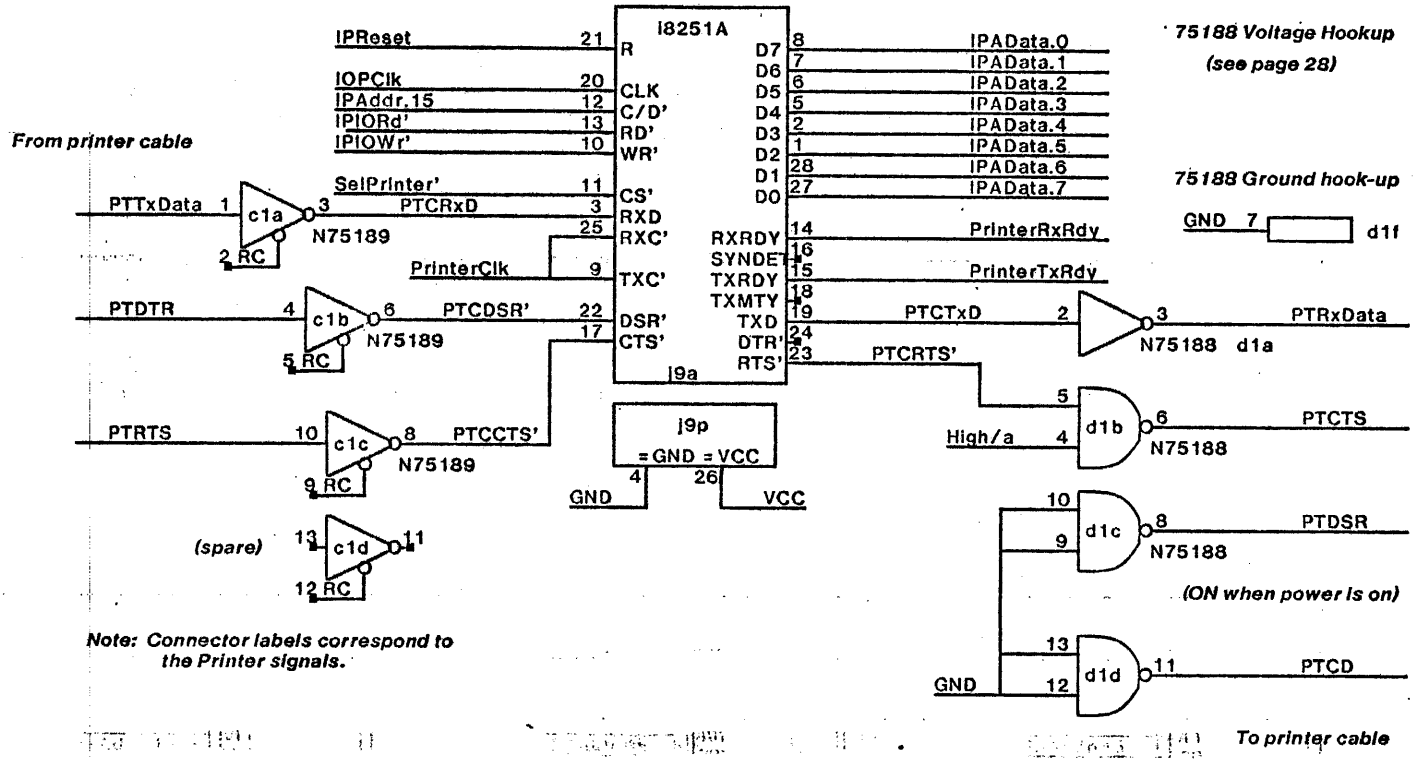
(18 pin socket for DIP conector)





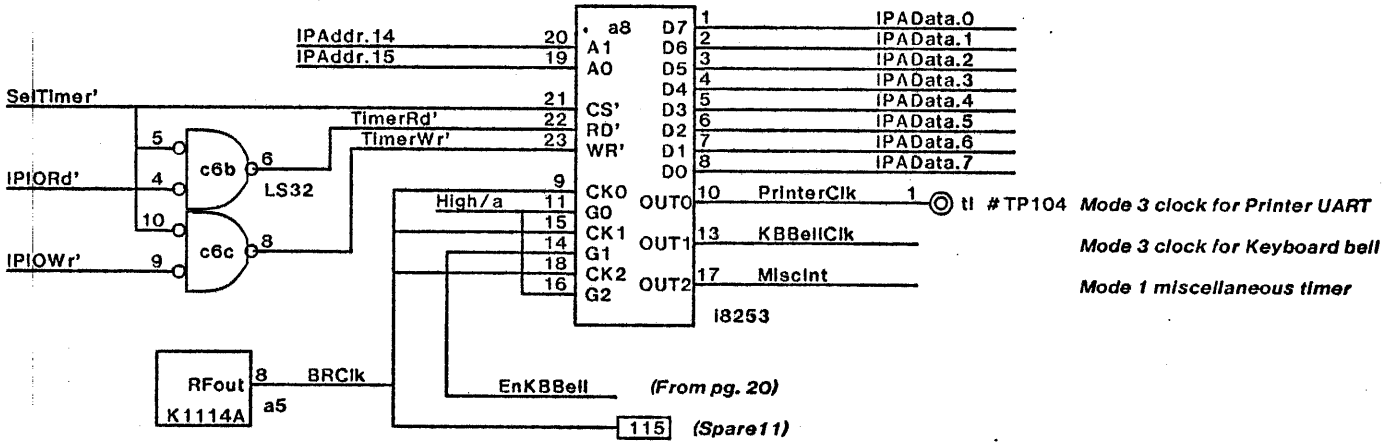
XEROX SDD	Project Dandelion	I/O Processor Miscellaneous CPU control	File DandIOP21.sil	Designer Ogus	Rev J	Date 5/8/80	Page 21

Printer UART

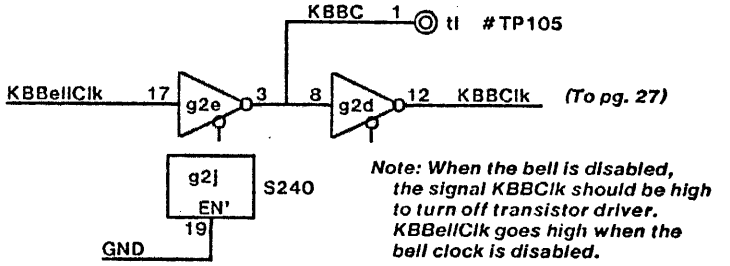


Note: Due to a design shortcoming the RD' and WR' lines of the 8253-5 must be externally qualified.

Baud-rate generator

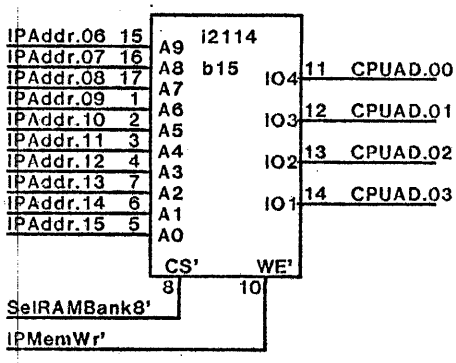


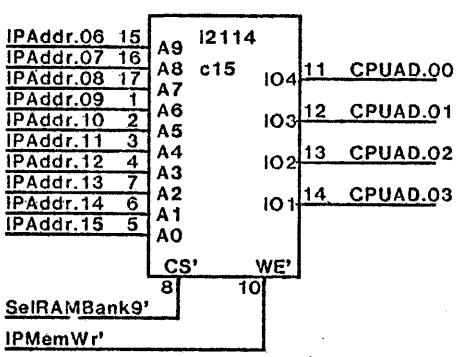
Baud-rate oscillator (1.8432 MHz)

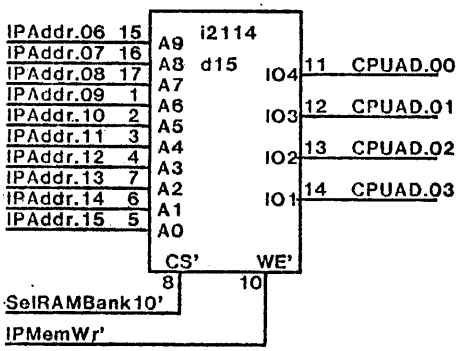


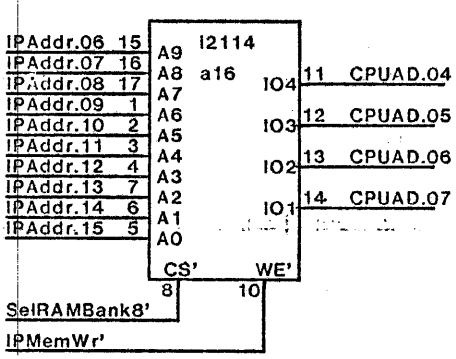
XEROX SDD	Project Dandelion	I/O Processor Diablo Priner Interface	File DandIOP22.sil	Designer Ogus	Rev J	Date 5/9/80	Page 22

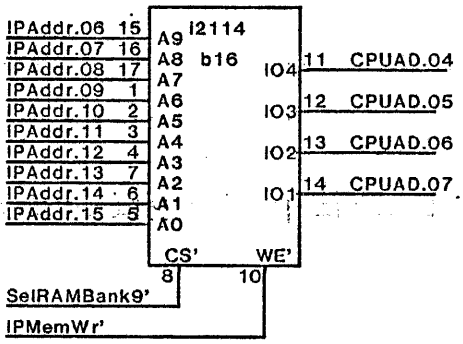
RAM - Banks 8 - 11

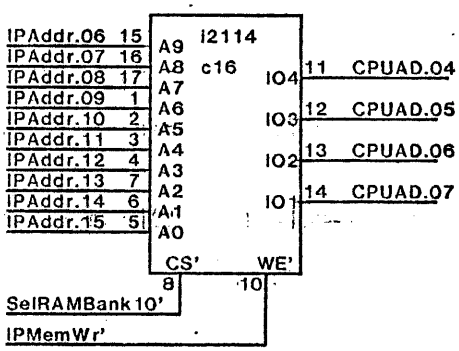




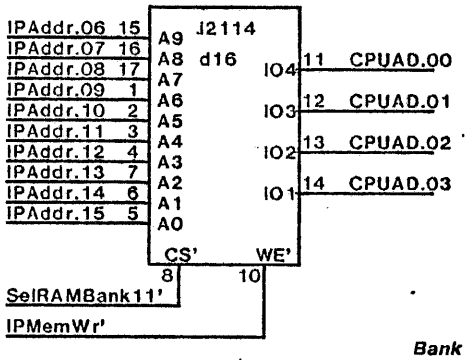


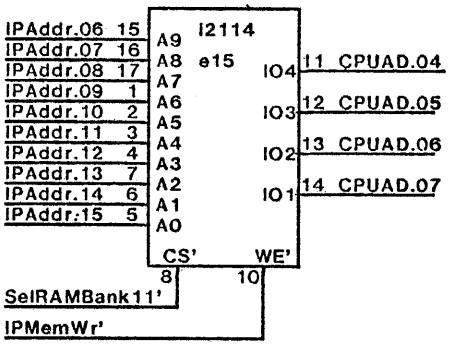






Bank 8 *Bank 9* *Bank 10*

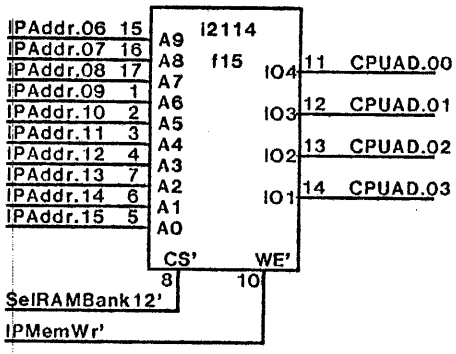


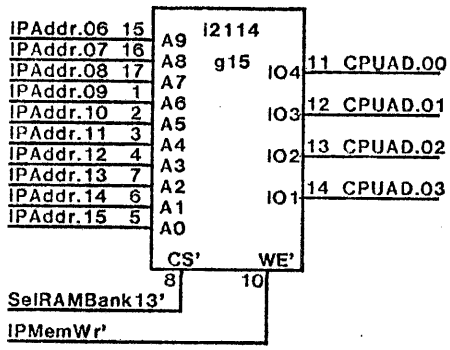


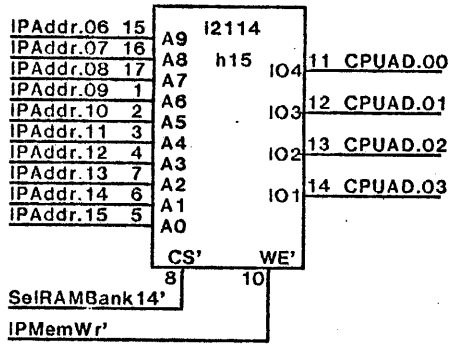
Bank 11

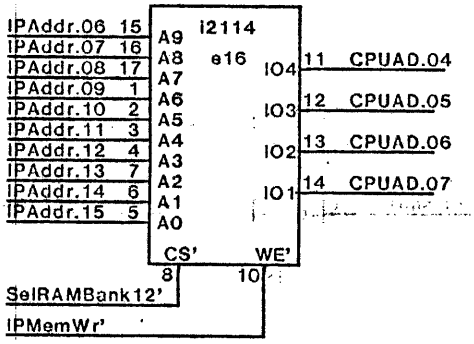
XEROX SDD	Project Dandelion	I/O Processor 4K RAM Memory-Banks 8-11	File DandIOP23.sil	Designer Ogus	Rev J	Date 2/26/80	Page 23

RAM - Banks 12 - 15

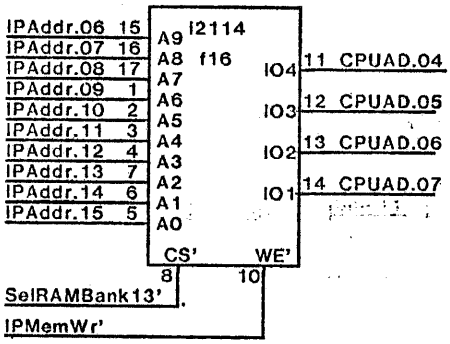




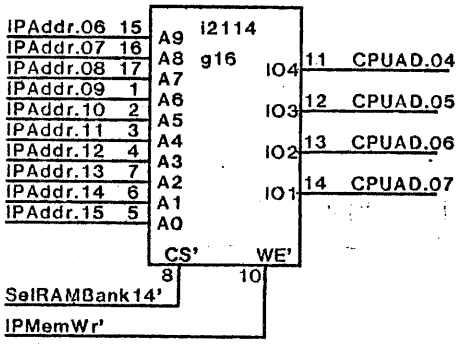




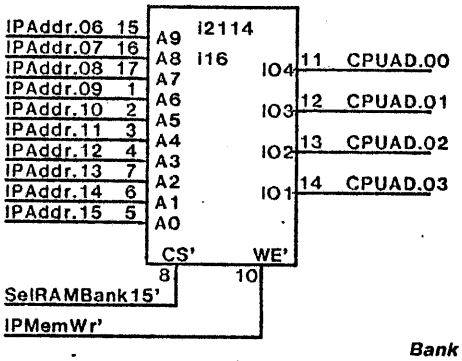
Bank 12



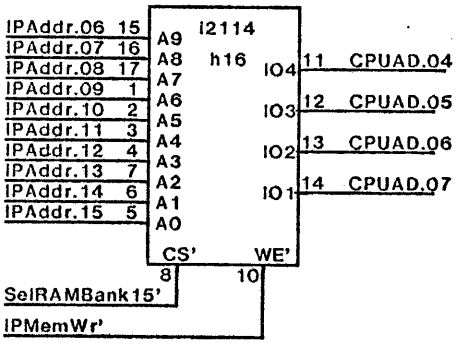
Bank 13



Bank 14

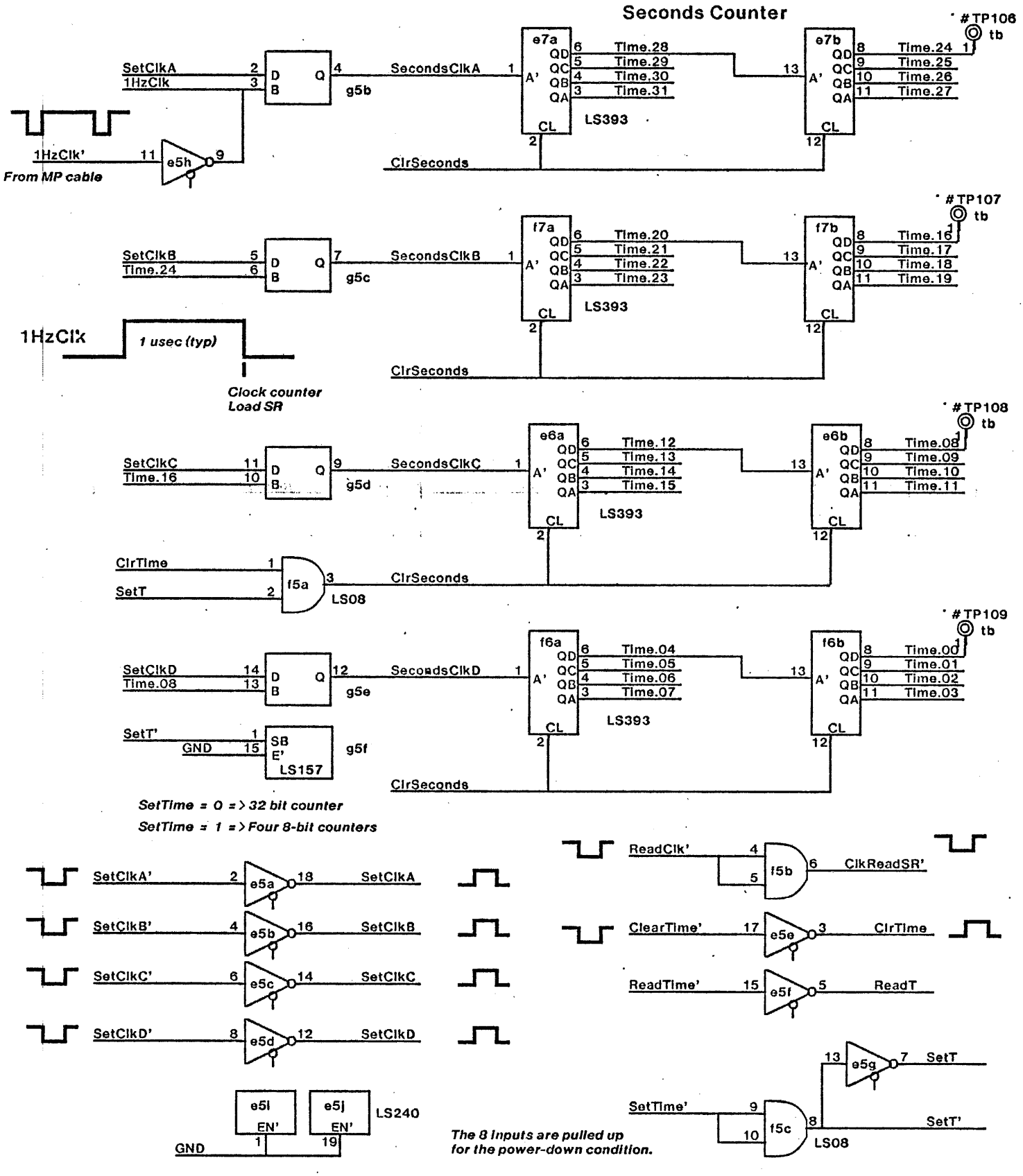


Bank 15



XEROX SDD	Project: Dandelion	I/O Processor 4K RAM Memory-Banks 12-15	File: DandIOP24.sil	Designer: Ogus	Rev: J	Date: 2/26/80	Page: 24

Note: All the logic on this page is powered from the Maintenance panel +5V supply, MVcc (see page 26)

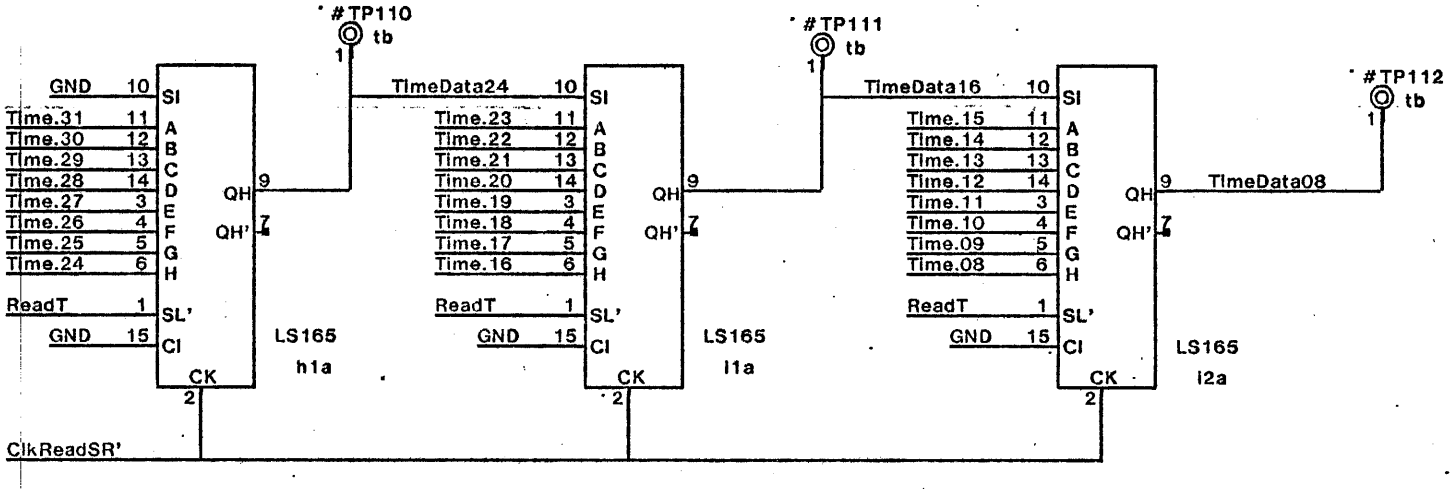


XEROX SDD	Project: Dandelion	I/O Processor Time-of-Day Clock - 1	File: DandIOP25.sil	Designer: Ogus	Rev: J	Date: 5/8/80	Page: 25

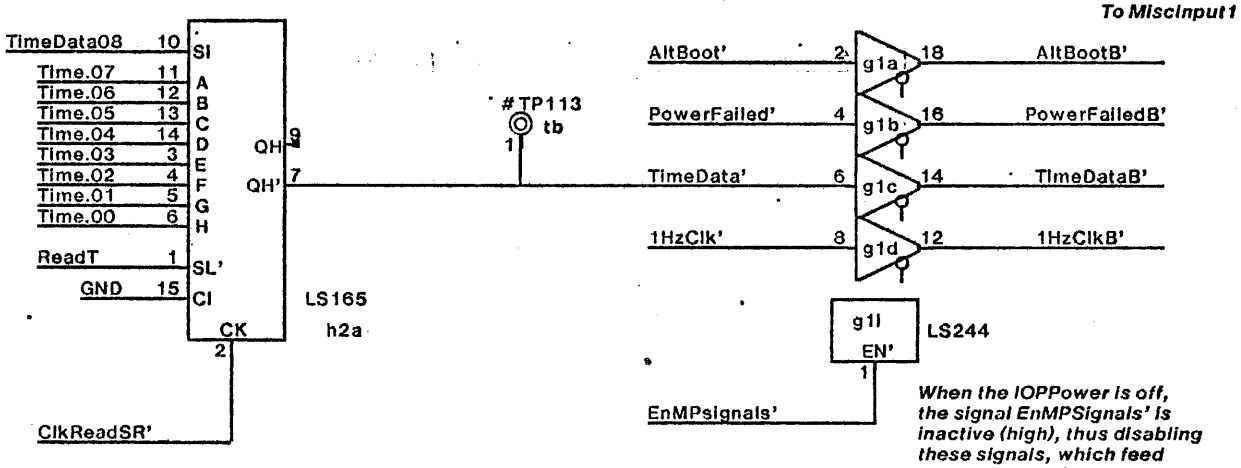
Note: All the logic on this page is powered from the Maintenance panel +5V supply, MVcc

Time Read Shift Register

ReadTime = 0 =>
Shift register parallel loads Seconds Counter
ReadTime = 1 =>
Shift register in serial shift mode, ClkReadSR' clock

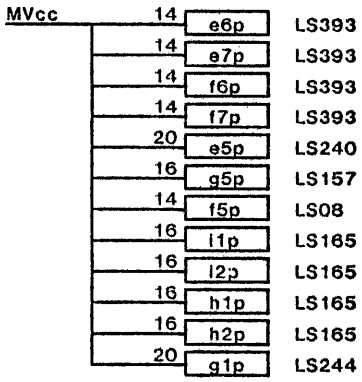


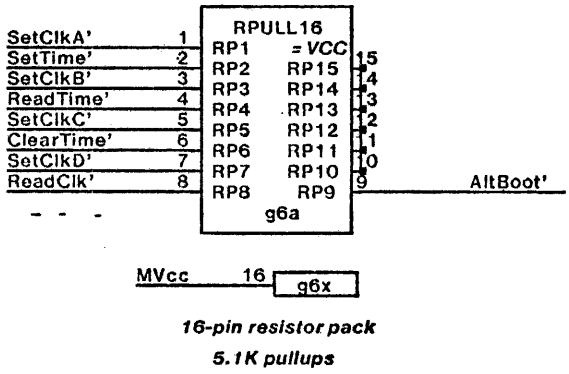
To MiscInput1



When the IOPPower is off, the signal EnMPSignals' is inactive (high), thus disabling these signals, which feed unpowered logic.

Power for Time-of-day clock from Maintenance Panel



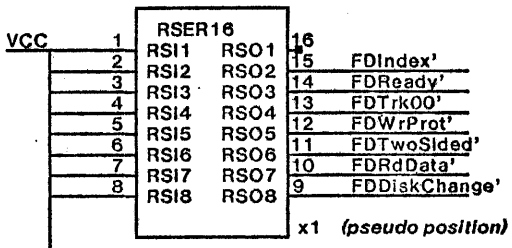


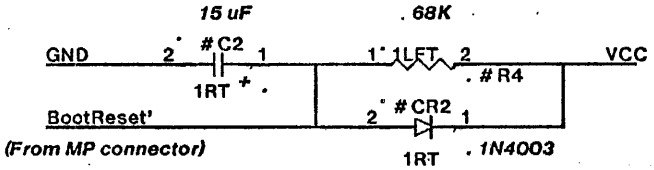
16-pin resistor pack
5.1K pullups

XEROX SDD	Project: Dandelion	I/O Processor Time-of-Day Clock - 2	File: DandIOP26.sil	Designer: Ogus	Rev: J	Date: 5/8/80	Page: 26

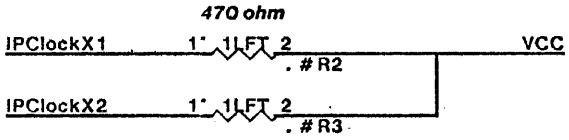
DISCRETE COMPONENTS

Pullups, 150 ohm, 1/4 watt
Allen-Bradley 316B151

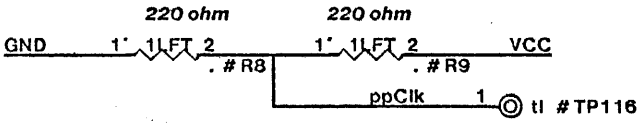




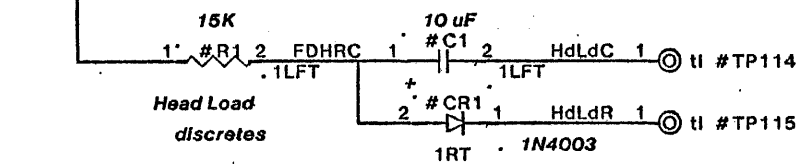
Boot button and Power-up time constant



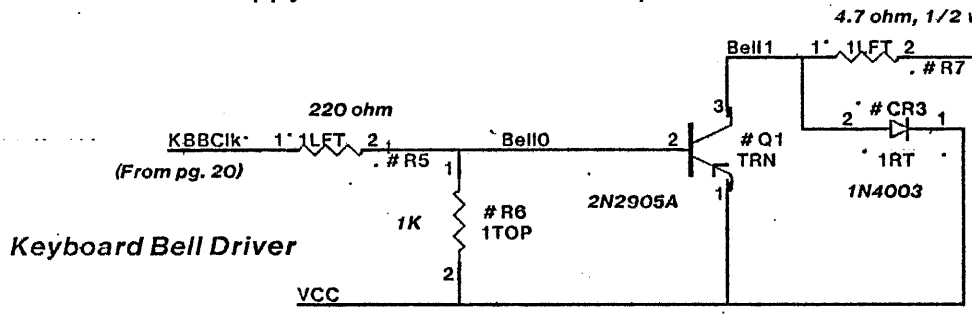
CPU clock driver pull-ups



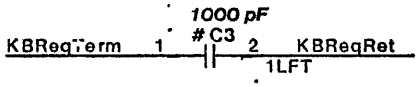
ppClk termination



Miscellaneous Floppy Controller discrete components

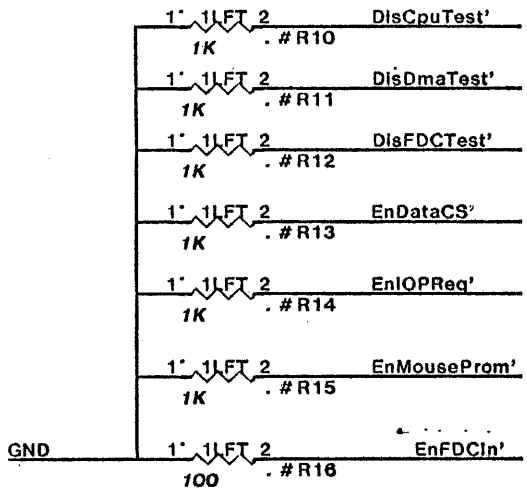


Keyboard Bell Driver

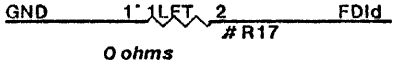


Keyboard Request Line

Discretes for Testability

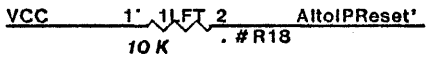


Floppy Disk jumper



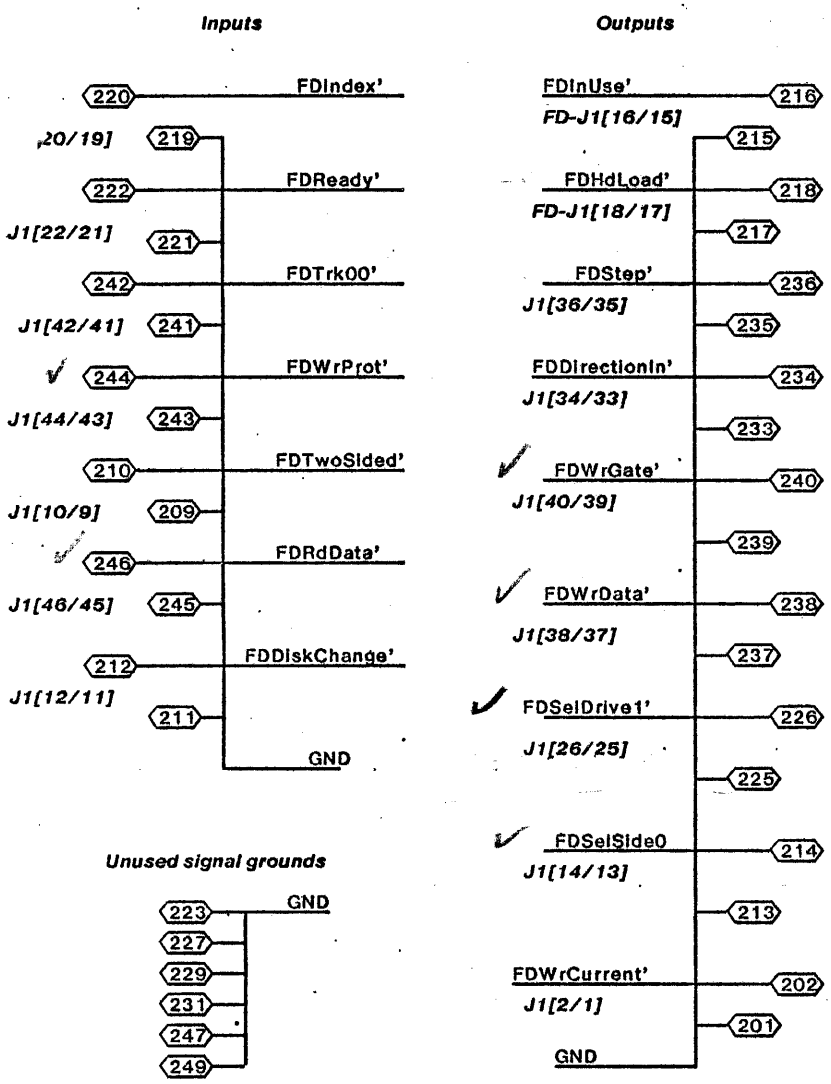
Jumper in: SA 850 drive
Jumper removed: SA 800 drive

Pullup for Reset line from Alto



(Needed for when no Alto is connected)

XEROX SDD	Project: Dandelion	I/O Processor PC discretes	File: pDandIOP27.sil	Designer: Ogus	Rev: J	Date: 5/9/80	Page: 27



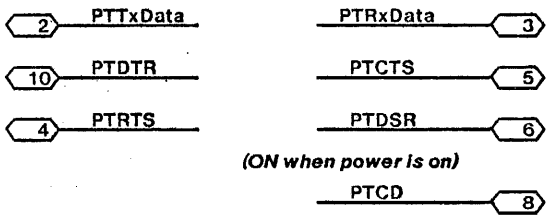
Floppy Disk Cable Connector

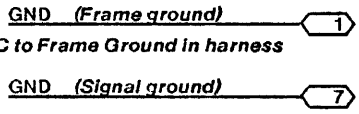
50-pin male connector

Xerox 713W14820

(Subtract 200 from above pin numbers to get physical pin number)

(Printer)





Note: Currently NC to Frame Ground in harness

Note: Connector labels correspond to the Printer signals.

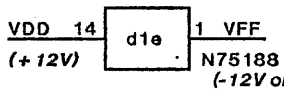
RS-232-C DCE port Cable Connector

10-pin male connector

Xerox 713W12220

(Above pin numbers are same as physical pin numbers)

75188 Voltage hookup

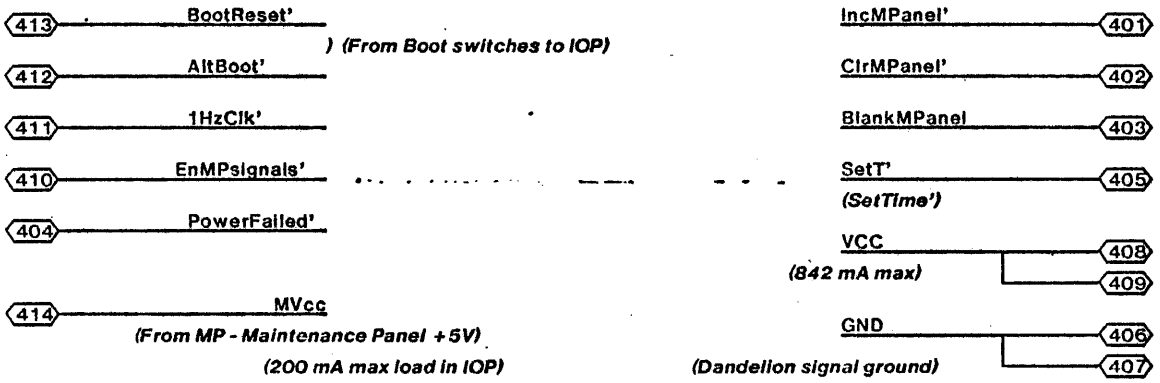


Maintenance Panel Cable Connector

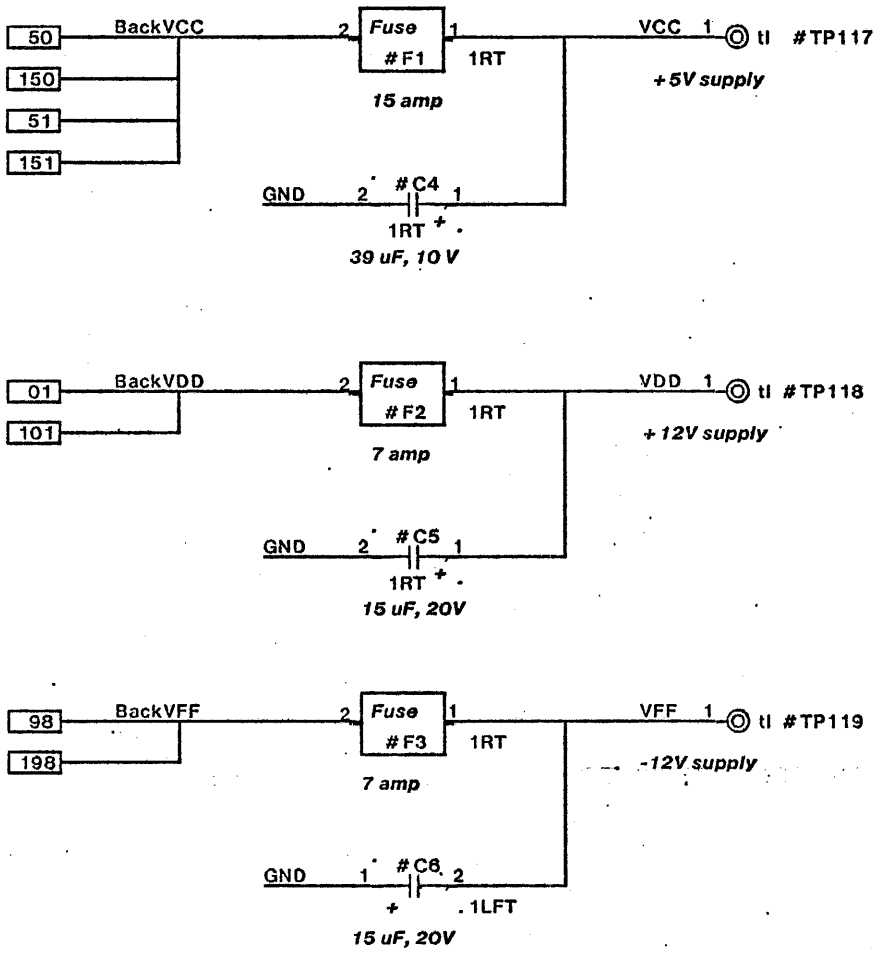
14-pin male connector

Xerox 713W13320

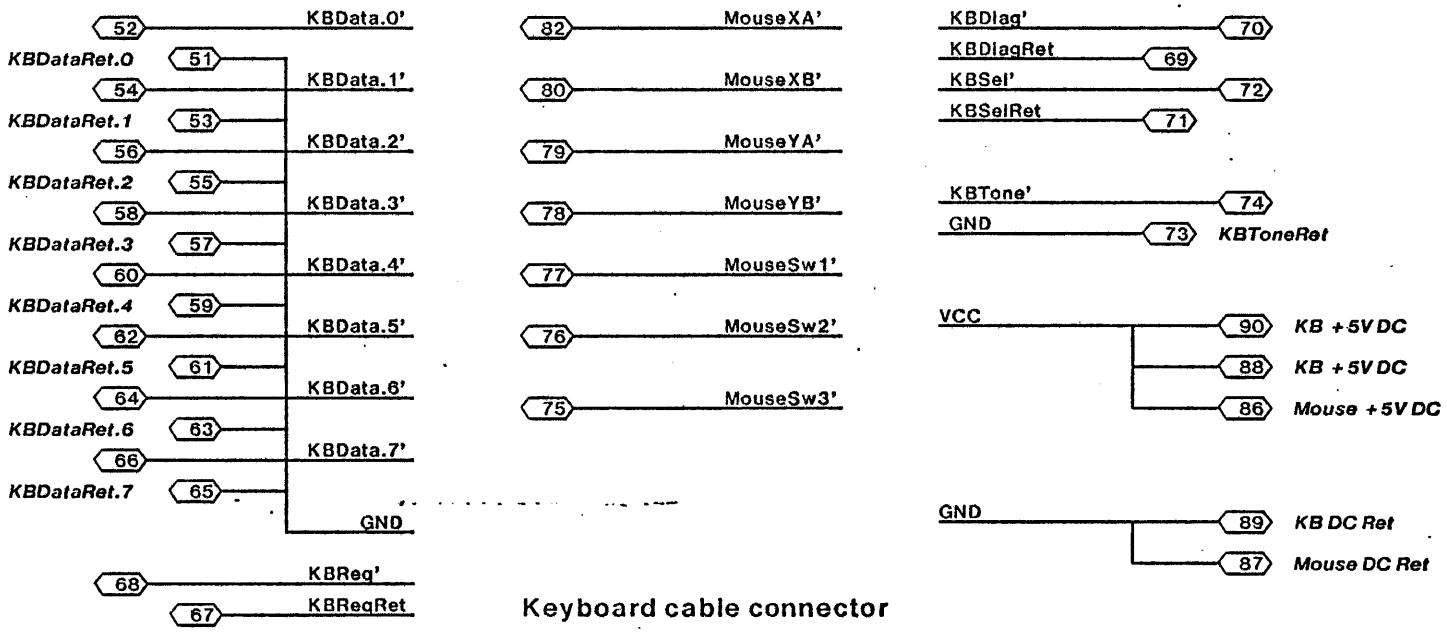
(Subtract 400 from pin numbers to get physical pin number)



XEROX SDD	Project Dandelion	I/O Processor I/O Connectors - 2	File pDandIOP28.sil	Designer Ogus	Rev J	Date 4/14/80	Page 28



CABLES



Keyboard cable connector

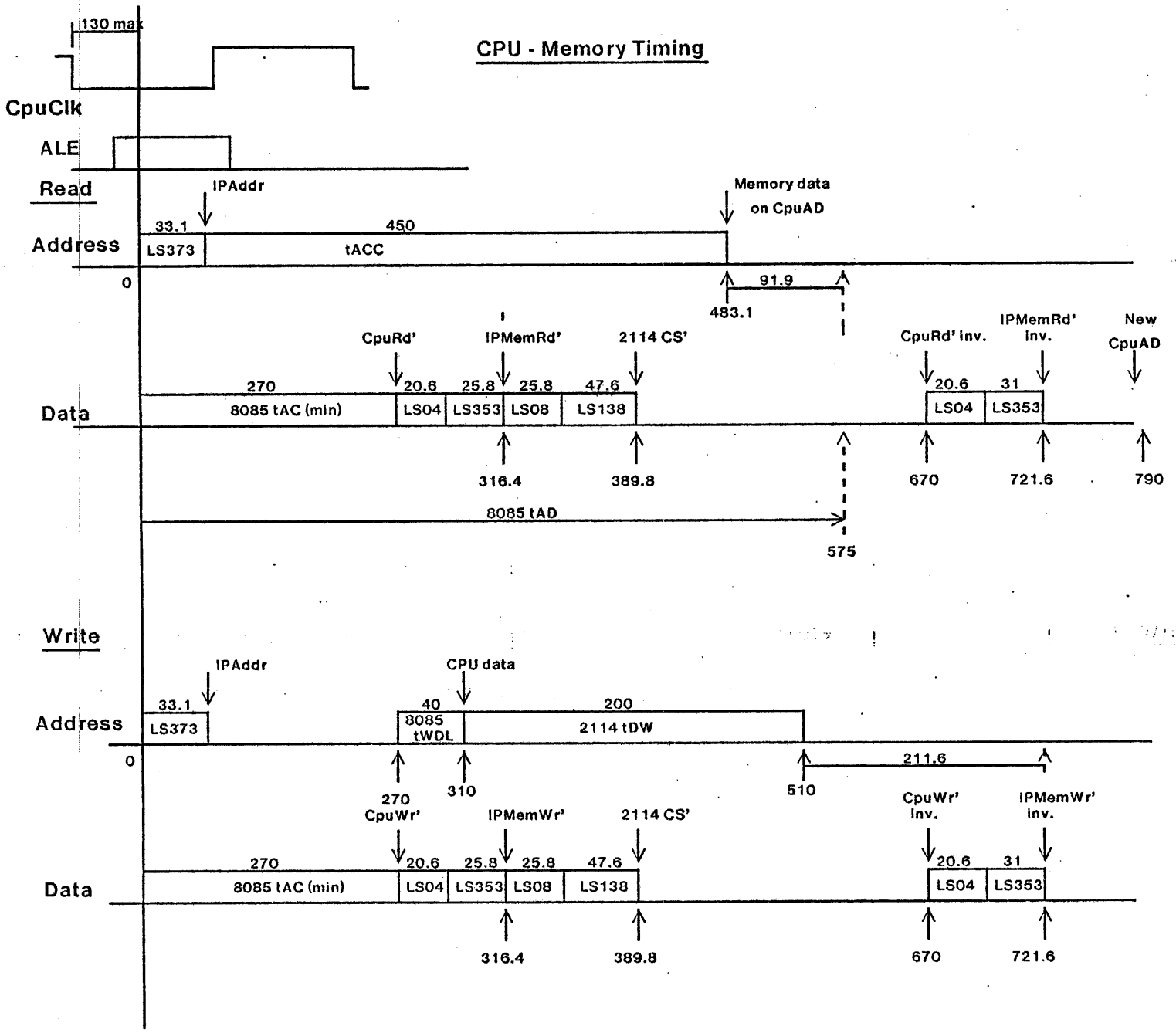
40-pin male connector

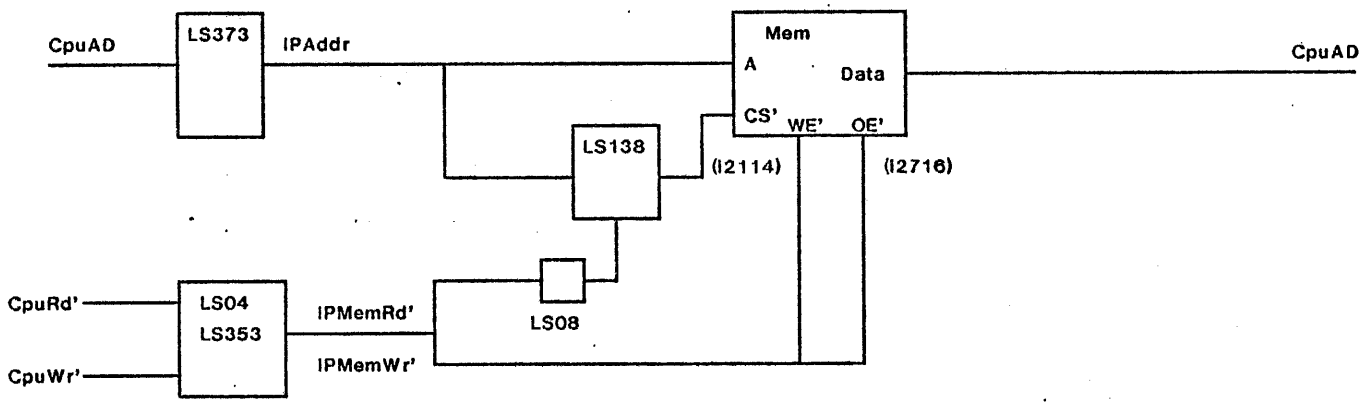
Xerox 713W12720

(Subtract 50 from above pin numbers to get physical pin number)

XEPOX SDD	Project Dandelion	Power Supply and Fuses Keyboard cable connector	File pDandlOP29.sil	Designer Ogus	Rev J	Date 5/8/80	Page 29

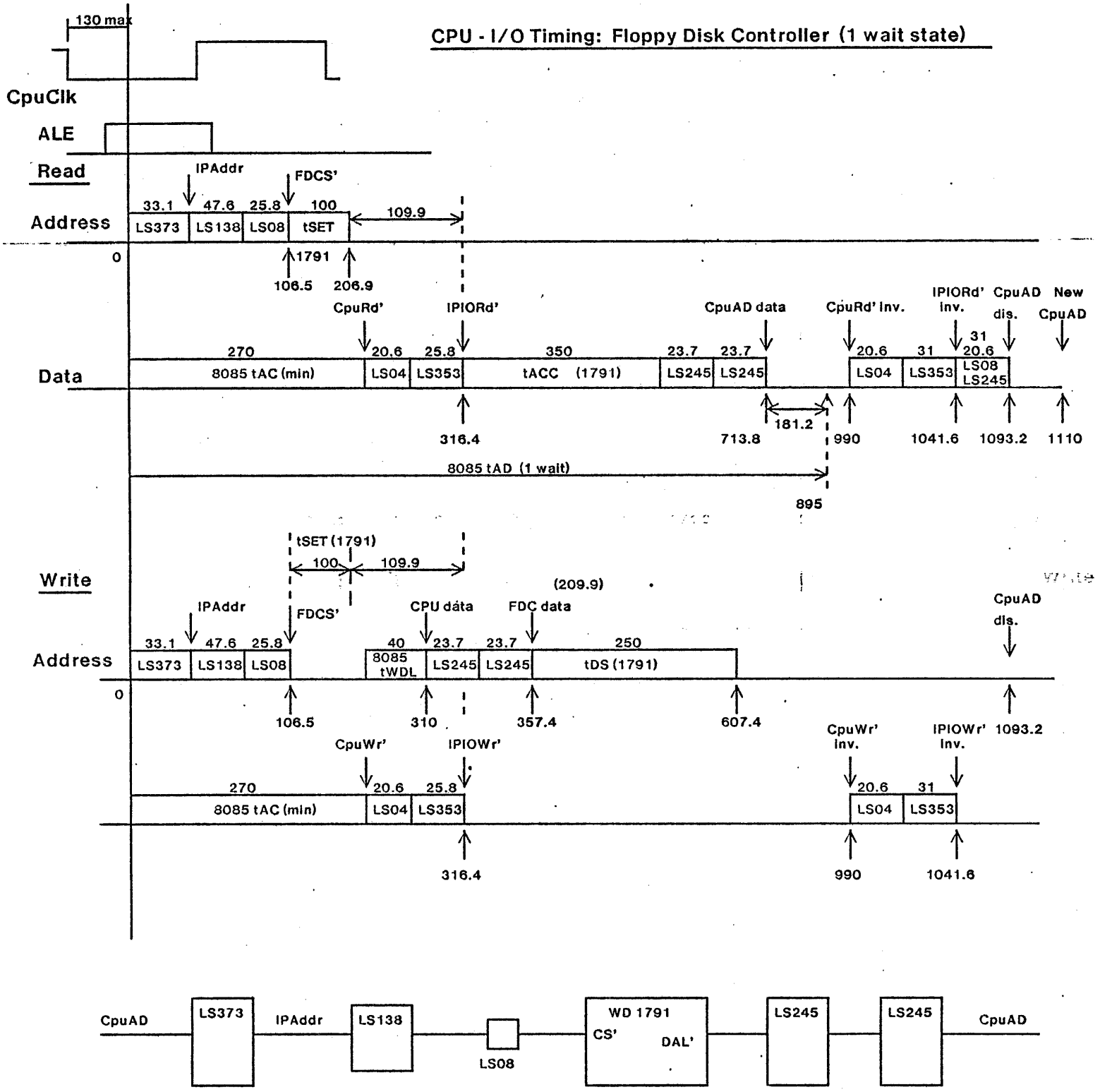
CPU - Memory Timing





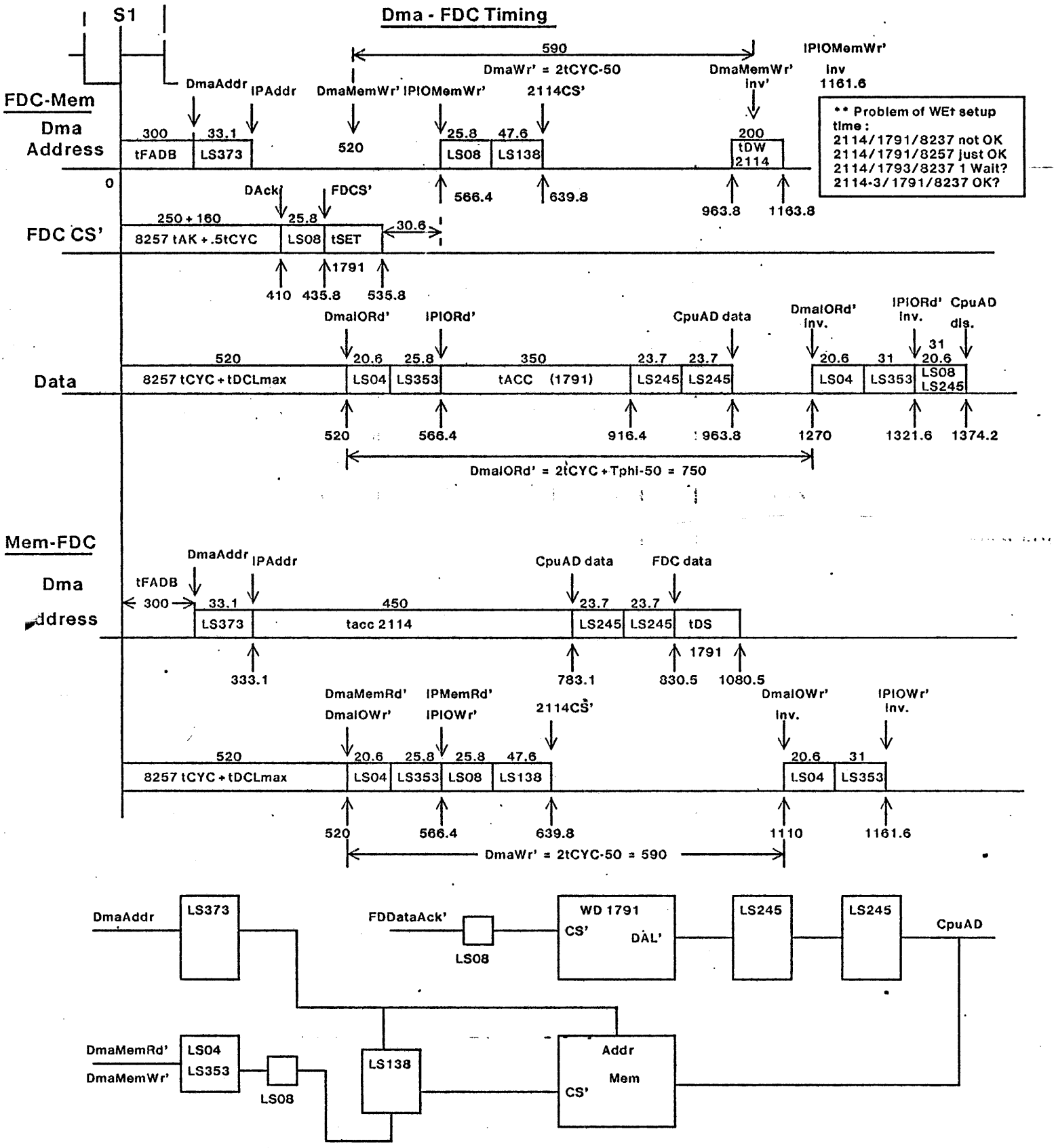
XEROX SDD	Project: Dandelion	I/O Processor CPU timing: Cpu-Mem	File: DandIOP30.silx	Designer: Ogus	Rev: F	Date: 3/3/80	Page: 30

CPU - I/O Timing: Floppy Disk Controller (1 wait state)



XEROX SDD	Project: Dandelion	I/O Processor CPU timing: Cpu-FDC	File: DandIOP31.silx	Designer: Ogus	Rev: F	Date: 3/3/80	Page: 31

2114-3 or 1793 OK

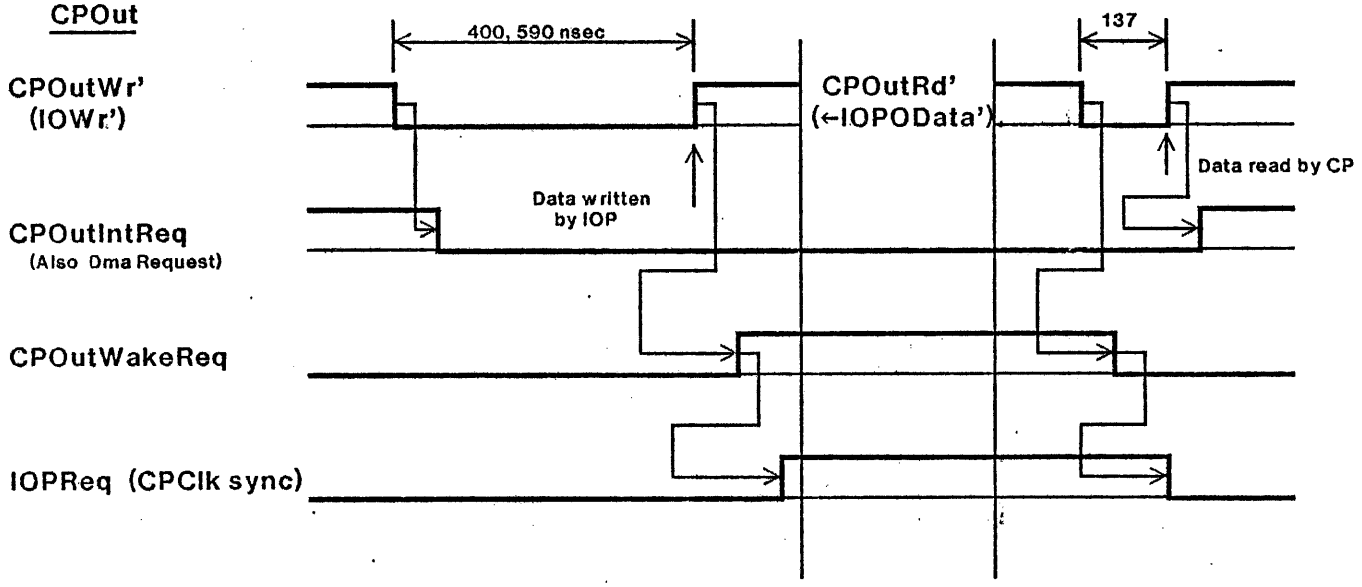


XEROX SDD	Project Dand/IOP	I/O Processor Dma-FDC Timing	File DandIOP32.silx	Designer Ogus	Rev D	Date 8/9/79	Page 32

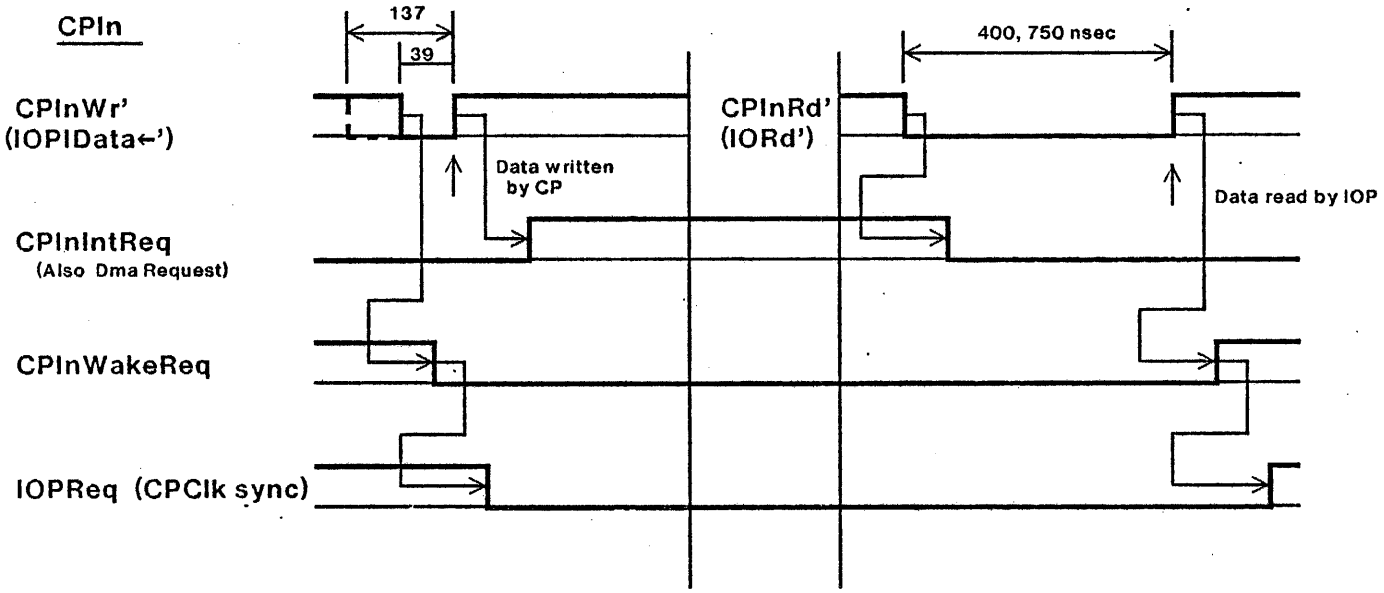
IOP - CP communication - Port timing

Timing Diagrams (not to scale)

CPOut



CPIn

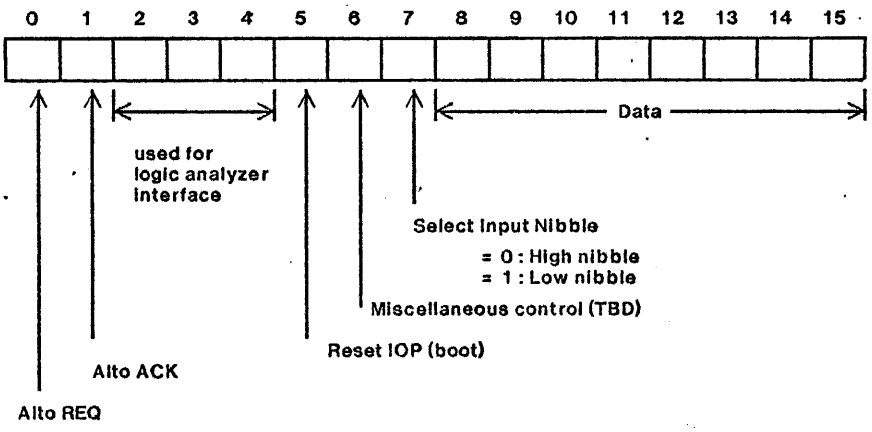


XEROX SDD	Project	I/O Processor	File	Designer	Rev	Date	Page
	Dandelion	CP port timing	DandIOP33.silx	Ogus	E	10/25/79	33

ALTO-DANDELION Communication via Umbilical

Alto Operations

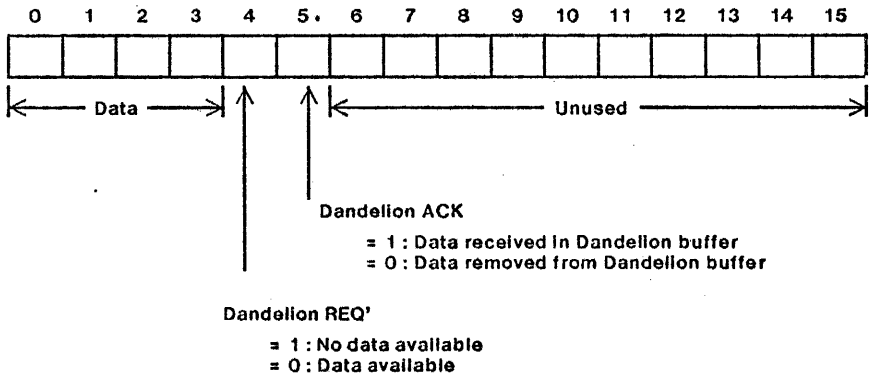
Output:



Sequence of Output operation:

- Output data to UTILOUT
- Alto Request (Set AltoREQ = 1) (UTILOUT[0])
- Read Dandelion ACK
  DandelionACK = 1 means data received.
- Remove Alto Request (Set AltoREQ = 0)
- Read Dandelion ACK
  DandelionACK = 0 means data accepted.

Input:



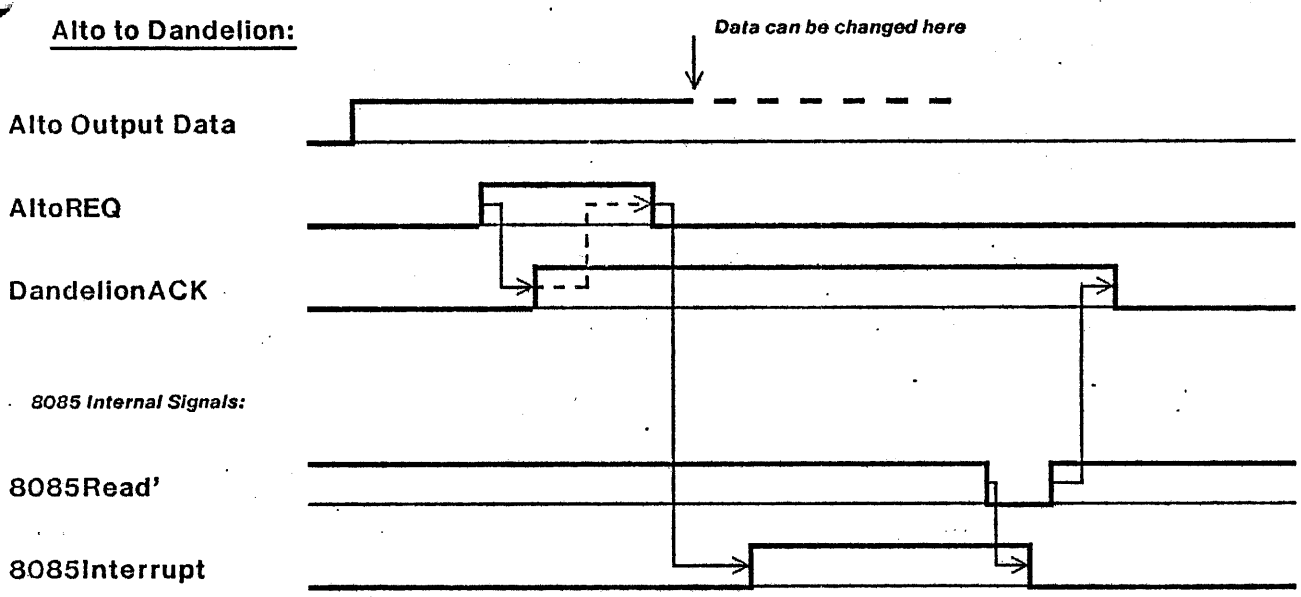
Sequence of Input Operation:

- Poll Dandelion REQ (UTILIN[4])
  DandelionREQ' = 0 means data is available.
- Set SelectInputNibble = 0 (UTILOUT[7])
- Read high data nibble (UTILIN[0:3])
- Set SelectInputNibble = 1 (UTILOUT[7])
- Read low data nibble (UTILIN[0:3])
- Alto Acknowledge (Set AltoACK = 1)
- Poll Dandelion REQ'
  Dandelion REQ' = 1 means ACK has been received.
- Remove Alto Acknowledge (Set Alto ACK = 0)

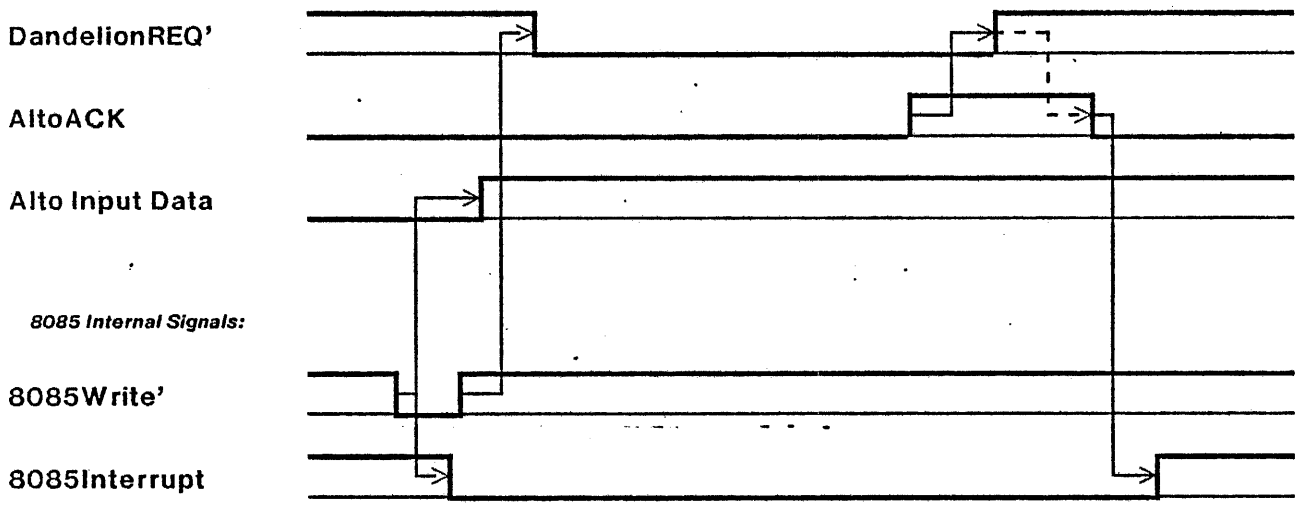
ALTO-DANDELION Communication via Umbilical

Timing Diagrams (not to scale)

Alto to Dandelion:



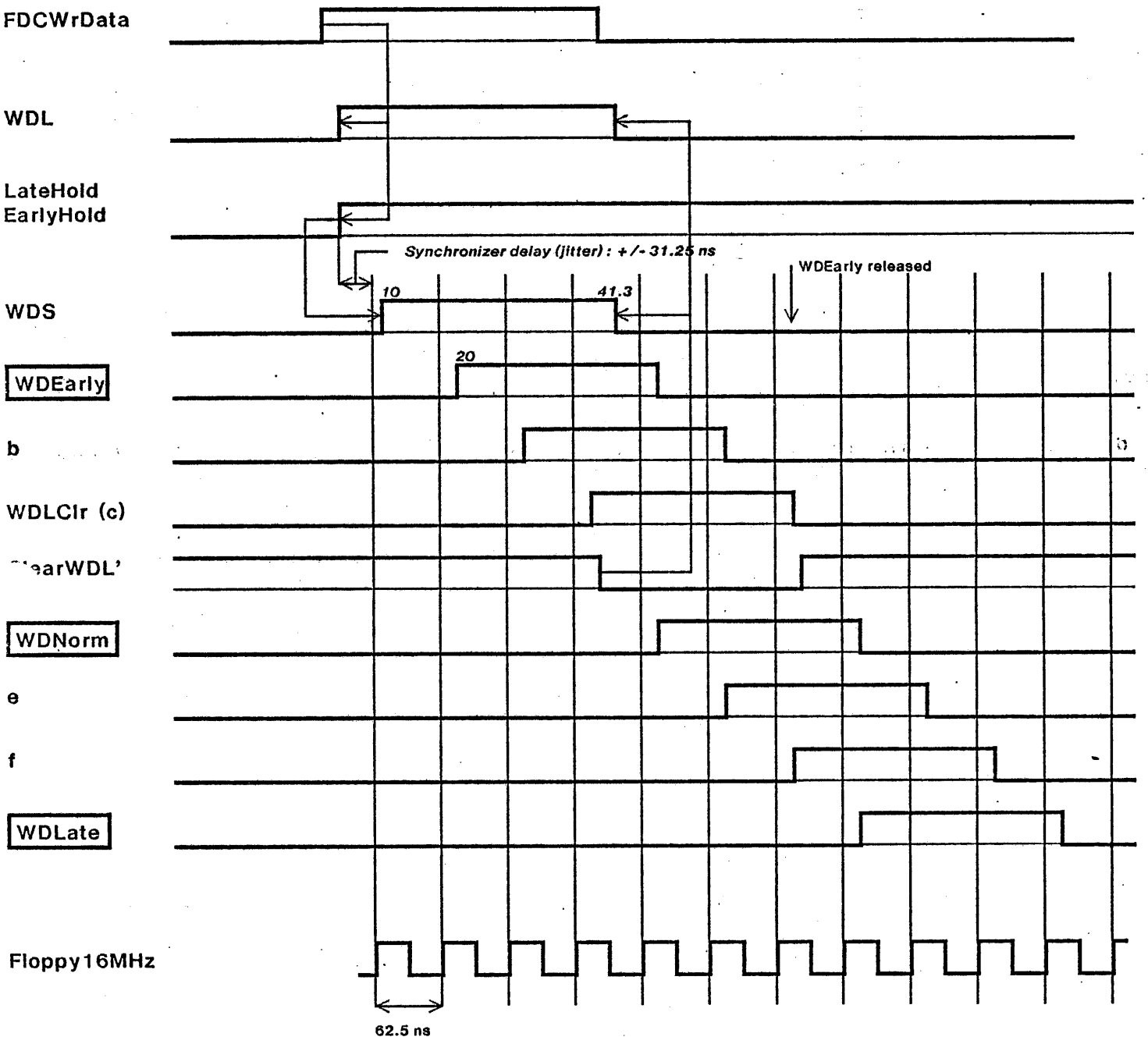
Dandelion to Alto:



Dandelion I/O Processor Floppy Disk Controller

WritePre-compensation Timing Circuit

(See DandIOP09.sil for circuit)



Phase Jitter = +/- 31.25 ns

Precompensation = 187.5 ns +/- jitter

WriteData Pulse width = 187.5 ns

XEROX SDD	Project Dand/IOP	I/O Processor Timing Floppy Controller Write Comp.	File DandIOP39.silx	Designer Ogus	Rev D	Date 6/4/79	Page 39

IPData Loads

(* = smallest margin drivers)

Page	Chip	Position	High (uA)	Low (uA) (in, tri)	
6	LS245 (bi)	g11	20	200, 20	Drive: 15000 24000
8	LS273 (in)	d6	20	400	
	LS241 (out)	d7	20	0, 20 (tri)	Drive: 15000 24000
13	LS374 (in)	c7	20	400	
	LS374 (out)	c7	20	0, 20 (tri)	Drive: 2600 24000
14	LS240 (out)	c12	20	0, 20 (tri)	Drive: 15000 24000
	F93427 (out)	f17	100	0, 100 (tri)	Drive: 2000 16000 *
15	LS175 (in)	g19	20	400	
16	LS174 (out)	d19	20	0, 20 (tri)	Drive: 2600 24000
	S374 (in)	e19	50	250	
17	LS240 (out)	b19	20	0, 20 (tri)	Drive: 15000 24000
18	LS374 (out)	b6	20	0, 20 (tri)	Drive: 2600 24000
19	LS2569 (out)	a/b,9/10	40	0, 40 (tri)	Drive: 2600 8000 *
20	LS240 (out)	a7	20	0, 20 (tri)	Drive: 15000 24000
	LS174 (in)	a6	20	400	
	LS374 (in)	b5	20	400	
Backplane					
	LS244 (in)		20	200	
	LS244 (in)		20	200	
	LS374 (in)		20	400	
	LS251 (out)		20	0, 20 (tri)	Drive: 2600 8000

	2650	Fixed input loads
530	3450	LS245 drive, all other bi or out are tristate
	3650	LS245 input

IPAData Loads

Page	Chip	Position	High (uA)	Low (uA) (in, tri)	
6	LS245 (bi)	b12	20	200, 20	Drive: 15000 24000
7	i8257 (bi)	m8	10	10	Drive: 150 1600
7	LS373 (in)	d9	20	400	
8	LS245 (bi)	i7	20	200, 20	Drive: 15000 24000
21	i8255 (bi)	d2	10	10	Drive: 400 2500
22	i8251A (bi)	j9	10	10	Drive: 400 2200
22	i8253-5 (bi)	a8	10	10	Drive: 400 2200

100	460	LS245 drive, other LS245 tristate
100	640	LS245 drive, other LS245 input
100	660	Mos drive, one LS245 input, 1 LS245 tristate

IPAddr Loads

Page	Chip	Position	High (uA)	Low (uA) (in, tri)		
1	LS373 (out)	f11, e11	20	0, 20 (tri)	IPAddr.00-15	Drive: 2600 24000
	LS04 (in)	h10	20	400	IPAddr.00 only	
	LS353 (in)	e9	20	400	IPAddr.00 only	
	LS353 (in)	f9	20	400	IPAddr.00 only	
2	I2716 (in)	e,f,g,h12	40	40	IPAddr.05-15 only	
3,4	I2114 (in)	a,b,c,d,e,f,g13,14	160	160	IPAddr.06-15 only	(16 chips)
23,24	I2114 (in)	a,b,c,d,e,f,g15,16	160	160	IPAddr.06-15 only	(16 chips)
5	LS138 (in)	h11	20	400	IPAddr.01-04 only	
	LS138 (in)	d11	20	400	IPAddr.01-05 only	
	LS138 (in)	I13	20	400	IPAddr.01-05 only	
	LS138 (in)	I11	20	400	IPAddr.00,09-13 only	
	LS138 (in)	b11	20	400	IPAddr.12-15 only	
	LS138 (in)	c11	20	400	IPAddr.12-15 only	
	LS155 (in)	a11	40	800	IPAddr.09 only	
	LS155 (in)	a11	20	400	IPAddr.10-11 only	
6	F93427 (in)	c9	40	250	IPAddr.00,01 only	
7	LS373 (out)	d9	20	0, 20 (tri)	IPAddr.00-07 only	Drive: 2600 24000
	LS245 (bi)	d10	20	200	IPAddr.08-15 only	Drive: 15000 24000
8	LS32 (in)	I6	20	400	IPAddr.14,15 only	
14	F93427 (in)	f17	40	250	IPAddr.12-15 only	
15	LS138 (in)	I19	20	400	IPAddr.12-15 only	
21	I8255 (in)	d2	10	10	IPAddr.14,15 only	
22	I8251A (in)	j9 (Alto port)	10	10	IPAddr.15 only	
	I8253-5 (in)	a8	10	10	IPAddr.14,15 only	
plane	LS241 (in)		20	200	IPAddr.13-15 only	
			140	1870	IPAddr.00	
			140	1870	IPAddr.01	
			480	2010	IPAddr.13	
			530	2440	IPAddr.15	

CpuAD bus loading

Page	Chip	Position	High (uA)	Low (uA) (in, tri)		
1	I8085	n8	10	10		Drive: 400 2000
	LS373 (in)	e11	20	400		
2	I2716 (out)	e,f,g,h12	40	40	(4 chips)	Drive: 400 2100
3,4	I2114 (bi)	a,b,c,d,e,f,g13,14	80	80	(8 chips)	Drive: 1000 2100
23,24	I2114 (bi)	a,b,c,d,e,f,g15,16	80	80	(8 chips)	Drive: 1000 2100
6	LS245 (in)	g11	20	200		
	LS245 (in)	b12	20	200		
			260	1000	8085, 2114, or 2716 drive	

IPMemRd', IPMemWr', IPIORd', IPIOWr' loads

Page	Chip	Position	High (uA)	Low (uA) (in, tri)			
1	LS353 (out)	e9	--	--	MemRd, MemWr	Drive: 2600	8000
	LS353 (out)	f9	--	--	IORd, IOWr	Drive: 2600	8000
	LS08 (in)	g10	20	400	MemRd, MemWr		
	LS74 (in) (S',R')	g9	40	800	IORd, IOWr		
2	I2716 (in)	e,f,g,h12	40	40	MemRd		
3,4	I2114 (in)	a-h,13,14	160	160	MemWr	(16 chips)	
23,24	I2114 (in)	a-h,15,16	160	160	MemWr	(16 chips)	
5	LS138 (in)	b11, c11	20	400	IORd, IOWr		
6	LS08 (in)	a12	20	400	IORd, IOWr		
7	LS241 (in)	d7	20	200	IORd, IOWr		
8	WD1791 (in)	p8	10	10	IORd, IOWr		
13	LS32 (in)	a10	20	400	IORd, IOWr		
14	F93427 (in)	f17	40	250	IORd		
15	LS138 (in)	i19	20	400	IOWr		
	LS32 (in)	h19	20	400	IORd		
16	LS32 (in)	a10	20	400	IORd, IOWr		
21	I8255 (in)	d2	10	10	IORd, IOWr		
22	I8251A (in)	j9	10	10	IORd, IOWr		
	I8253-5 (in)	a8	10	10	IORd, IOWr		
			60	440	IPMemRd'		
			340	720	IPMemWr'		
			240	3290	IPIORd'		
			200	3040	IPIOWr'		

XEROX SDD	Project: Dandelion	I/O Processor Signal Loading - 3	File: DandIOP42.silx	Designer: Ogus	Rev: F	Date: 3/3/80	Page: 42

1 / 101	10 / 110	20 / 120	30 / 130	40 / 140	50 / 150	51 / 151	60 / 160	70 / 170	80 / 180	90 / 190	100 / 200
+12v "VDD"	gnd "GND" = ▽	gnd	gnd	gnd	+5V "VCC"	+5V "VCC"	gnd	gnd	gnd	gnd	-5V "VEE"

	a	b	c	d	e	f	g	h	i	
	S02 @2 pClk', pWaitClk'	LS240 CPPort Stat.	LS273 @ IOP Control	LS374 CPIn	S374 CPOut	S240 IOP Status	LS175 CPControl-1	LS32 @2 ReadCSEn'	LS138 CSWE, WrTPC	19
18		S00 @ CPClk, Qual	LS74 CPInWakeReq CPOutWakeReq	LS74 CPInIntReq CPOutIntReq	LS374 @ IOPReq., CPClk sync		LS175 @ CPControl-2	LS374 @ IOPW, SwTAd sync		18
17	LS244 @ Dma tester	LS240 @2 Misc , High/c	LS157 @ CPDmaReq	LS08	F93427 IOPReq.	F93427 HAddrProm	LS244 @ Cpu tester	LS244 @ FDC tester	FPLAT Tester	17
16	RAM-B1 i2114	i2114	i2114	i2114	RAM-B2 i2114	i2114	i2114	i2114	i2114	16
15	14	i2114	i2114	i2114	i2114	i2114	i2114	i2114	@ 7414 Boot Schmitt	15
14	RAM-A1 i2114	i2114	i2114	i2114	RAM-A2 i2114	i2114	i2114	i2114	LS240 @ High/b, d IPReset'	14
13	i2114	i2114	i2114	i2114	i2114	i2114	i2114	i2114	LS138 RAM-B Sel.	13
12		a LS00 @ Enable IPData, IPAData	b LS245 IPAData bus	c LS240 @ Int Req Reg.	e PROM i2716 PROM Bank 3	f i2716 PROM Bank 2	g i2716 PROM Bank 1	h i2716 PROM Bank 0		12
11	LS155 I/O Select Bank 2, 3	LS138 I/O Select Reg. Read	LS138 I/O Select Reg. Write	LS138 RAM-A Sel.	LS373 Address Lo	LS373 Address Hi	LS245 IPData bus	LS138 PROM Select	LS138 I/O Select Bank 0	11
10	LS32 CPIn,Out, Dma Test	LS2569 MouseX Hi	LS2569 MouseY Hi	LS245 DMA Addr Lo	RPULL16 @ 10K pullups	LS74 Cpu Ready	LS08 DmaTest, CpuResetIn' IPIORdWr',DmaC	LS04 @ IPAddr.00 IPClock, CpuRd'/Wr'	K1114A Clock (5.88MHz) 6 MHz)	10
9	LS2569 MouseX Lo	LS2569 MouseY Lo	F93427 EnIPDataProm	LS373 DMA Addr HI	LS353 IPIORd' IPIOWr'	LS353 IPMemRd' IPMemWr'	LS74 IPDataOut CP Dma EndC	LS00	PLAT16 @ Misc. comp.	9
8		a i8253-5 @ Baud Rate Generator	b c i8257-5 m8 DMA controller		e f i8085A n8 CPU		g h WD 1793-01 p8 Floppy Controller			8
7	LS240 @ Misc Input 1	LS04 Dma invert.	LS374 Dma Test	LS244 @ FDC status Dma IORd,IOWr	# LS393 Time24-31	# LS393 Time16-23	LS00 @ CP Dma EndC FDC data en.	LS74 FIDC DataReq FDC End Cnt	LS245 FDC-IPAData	7
6	LS273 @ Misc Control 1	LS374 KB data	LS32 @2 8253 Rd,Wr,	LS273 FDC State	# LS393 Time08-15	# LS393 Time00-07	# RPULL16 @ 5.1K pullups	LS08	LS32 @	6
5	K1114A Clock (1.8432 MHz)	LS374 Misc Clocks 1	F93427 Mouse Prom	LS374 Mouse state	# LS240 Time-of-day receivers	# LS08 @ Time-of-day receivers	# LS157 Time-of-day clock mux.	LS04	K1114A Clock (16 MHz)	5
4	LS74 @ TOD Intr.	PLAT16 KB compon.	Printer Control		S74 Write Comp.	LS74 Write Comp.	LS273 Data Sep.	F93453 Data Sep.	LS163 Clock Divider	4
3	N75115 @ KBReq Rcvr	LS240 Mouse X,Y rec. Misc. Contr.1	i8251A Printer UART j9		LS153 @ Write Comp.	S374 Write Comp.	LS74 Data Sep.	F93453 Data Sep.	S02 @	3
2	N75114 KB Sel Diag Driver	RDIV16 KB data res. Pullup/down	DipSocket MPanel Connector	PLAT18 Alto Control Connector	N123 @ Head Load	FPLAT Pullups	S240 @ Drivers	# LS165 TimeSR 0-7	# LS165 TimeSR8-15	2
1	FPLAT KB Conn. 1	FPLAT KB Conn. 2	N75189 @ Printer Rcvr	N75188 Printer Dvr	S240 Receivers High/a	S240 @ Drivers	# LS244 @ MP receivers	# LS165 TimeSR24-31	# LS165 TimeS16-23	1
	a	b	c	d	e	f	g	h	i	

DIP Orient. 1

I/O Connector (25 pin female)

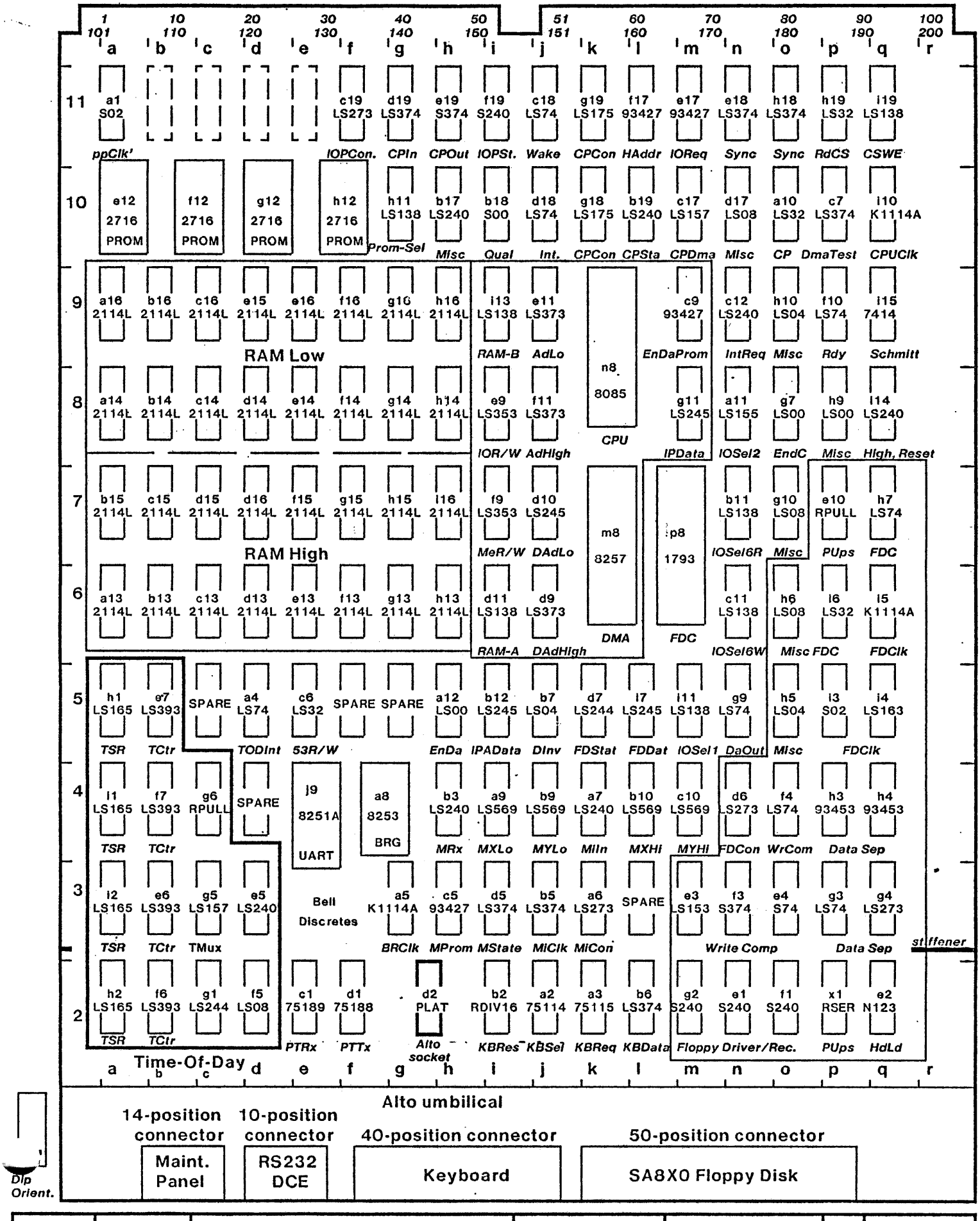
I/O Connector(37 pin female)

= MVcc power

Chip positions used: 159

Chip positions left: 8

XEROX SDD	Project Dandelion	IOP board layout (stitcheld)	File DandIOP51.silx	Designer Ogus	Rev I	Date 4/21/80



XEROX SDD	Project: Dandelion	IOP module PC layout detail	File: DandIOP52.silx	Designer: Ogus	Rev: H	Date: 3/24/80

PC Layout notes

1. Filter capacitors: 1 per 3 chip positions
   1 per 2 chip positions for 2114L, 2716
   1 per 8085, 8257, 1793/7, 8251, 8253

2. Spare chip positions at PC locations c5, f5, g5, d4, l3
   Unused chip positions b11, c11, d11, e11 (can be made spare)

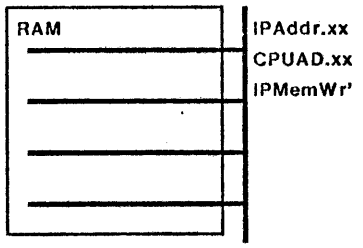
3. CP clocks:
   Chip S02 at PC location a11 should not be moved.
   Resistors R8 and R9 should be as close to backplane edge-connector pin 9 as possible.
   Clock qualifier chip is at i10 - position is acceptable.

4. FD1793/97: Either a FD1793 or an FD1797 can be plugged into stitchweld position p8 .

5. Board stiffener is to be placed between PC rows 2 and 3, so that the Alto umbilical socket (PC location h2) is on the I/O connector side of the stiffener. Alto Umbilical socket is an 18-pin socket.

6. ***Important***:
   The time-of-day clock chips (boxed at lower left side of layout) receive their Vcc power from the Maintenance Panel connector. They are NOT to be powered by the board Vcc. Ground pin is the same as the board ground. The signal, MVcc, originating from the Maintenance Panel connector is already wired to the appropriate Vcc pins of the affected chips. The affected chips are:
   PC locations: a2, b2, c2, d2, a3, b3, c3, d3, a4, b4, c4, a5, b5.

7. The nets IPAddr.xx (16 nets), IPData.xx (8 nets), IPAData.xx (8 nets), CPUAD.xx (8 nets), IPMemWr' (1 net),
   are long nets with many nodes, and the maximum length should be minimized as best as possible. If necessary, a hand layout of these busses should be done. For example:
   The RAM memory should have the busses, IPAddr.xx, CPUAD.xx, and IPMemWr' laid out as follows, to shorten themaximum length



8. Voltages used by this board: +5 V, +12 V, -12V.
9. All locations to be provided with IC sockets.
10. Note the positions of the Maintenance Panel and RS-232-C DCE connectors. They have been reversed in position from previous board drawings.
11. High/a, High/b, High/c, and High/d, are constant high signals, and can be interchanged if necessary.

I/O Processor Test Pads

Test Pad	Signal	Page	Test Pad	Signal	Page	Test Pad	Signal	Page
1	AltoPPIIntA	21	41	IPAData.7	6	81	SepState.1	12
2	CPAttn	15	42	EnIPData	6	82	SepState.2	12
3	CPUAD.00	2	43	EnIPAData'	6	83	PU2	12
4	CPUAD.01	2	44	EnIPAData	6	84	SepState.3	12
5	CPUAD.02	2	45	EnDataCS'	6	85	SepState.4	12
6	CPUAD.03	2	46	DmaHLDA	7	86	SepState.5	12
7	CPUAD.04	2	47	DmaRDY	7	87	SepState.6	12
8	CPUAD.05	2	48	DisDmaTest'	7	88	pIOPReq'	17
9	CPUAD.06	2	49	DmaHoldReq	7	89	EnIOPReq'	17
10	CPUAD.07	2	50	DmaIORd'	7	90	CPDmaReq	17
11	(unassigned)	--	51	DmaIOWr'	7	91	KBIntr	18
12	IPReset	1	52	DmaMemRd'	7	92	oldXA	19
13	CpuHoldAck	1	53	DmaMemWr'	7	93	oldXB	19
14	CpuIO/M'	1	54	FloppyDataAck'	7	94	oldYA	19
15	CpuRD'	1	55	CPDmaAck'	7	95	oldYB	19
16	CpuWR'	1	56	DmaEndCount	7	96	EnMouseProm'	19
17	CPUAddr.00	1	57	(unassigned)	--	97	EnMouseX'	19
18	CPUAddr.01	1	58	DmaAddrStrobe	7	98	UpMouseX	19
19	CPUAddr.02	1	59	DisFDCTest'	9	99	EnMouseY'	19
20	CPUAddr.03	1	60	pFDCHdLd	8	100	UpMouseY	19
21	CPUAddr.04	1	61	FDCStep	8	101	EnKBBell	20
22	CPUAddr.05	1	62	FDCDirCln	8	102	BootReset'	21
23	CPUAddr.06	1	63	FDCWrGate	9	103	AltoIPReset'	21
24	CPUAddr.07	1	64	FDCTG43	8	104	PrinterClk	22
25	(unassigned)	--	65	FDCWrData	9	105	KBBC	22
26	CpuHold	1	66	WDS	9	106	Time.24	25
27	DisCpuTest'	1	67	Early	9	107	Time.16	25
28	PU1	1	68	Late	9	108	Time.08	25
29	SelAltoPPI'	5	69	WDLClr	9	109	Time.00	25
30	SelPrinter'	5	70	Floppy2MHz	10	110	TimeData24	26
31	SelTimer'	5	71	Floppy16MHz	10	111	TimeData16	26
32	ReadKBData'	5	72	FDCHdLdDone	10	112	TimeData08	26
33	ClrMouseXY'	5	73	FDCIndex'	11	113	TimeData'	26
34	IPAData.0	6	74	FDCTr00'	11	114	HdLdC	27
35	IPAData.1	6	75	FDCWrProt'	11	115	HdLdR	27
36	IPAData.2	6	76	High/a	11	116	ppClk	27
37	IPAData.3	6	77	EnFDCIn'	11	117	VCC	29
38	IPAData.4	6	78	FDCRdDataSync'	12	118	VDD	29
39	IPAData.5	6	79	VFOEn'	12	119	VFF	29
40	IPAData.6	6	80	SepState.0	12			

Dandelion I/O Processor

Revision History

Rev. A to Rev. B

1. Signals on A and B ports of LS245 (g11) switched to account for correct sense of CpuS1 signal. (T = 1 => A to B) (pg. 1)
2. Enable (pin 1) of LS240 connected to GND. (pg. 1)
3. Prom macro changed for I2716 (h12), to reverse data bus connection. (pg. 2)
4. Ports PA, PB, and data bus reversed on I8255A (j9) with macro change. (pg. 5).

Rev. B to Rev. C

1. DMA controller added (pg. 7).
2. Floppy Disk controller added (pgs. 8-12).
3. New bus organization (see page 00c)
4. Address space change, to allow both memory or normal I/O mapping. IPAddr.00 on e8, f8, pin 14 (pg. 1).
5. IPDataOut signal (c6b, pin 9, pg. 1).
6. CPUReady signal to insert wait state for FDC, and DMA (slave). (pg. 6)
7. Change in generation of IPMemRd', IPMemWr', IPIORd', IPIOWr'. This removes the LS257 to avoid the output glitches which occur when device goes from tristate to active. (Gary Miller, Intel, 987-8086, 6/20/79) (pg. 1).
8. New I/O address decoding (pg. 5)
9. Page 5 renumbered to 13.

Rev. C to Rev. D.

Bug Fixes

1. Added inverters for CpuRd', CpuWr', DmaMemRd', DmaMemWr', DmaIORd', and DmaIOWr' and replaced LS253 with LS353 to fix multiplexor glitch when S2, S1 lines change. (page 1)
2. Fixed pullups for FloppyIntReq, FDCVFOen' (i6, page 6).
3. Removed boot switch backplane signal (pg. 6).
4. Buffered FDCHdLd (page 8).
5. IPReset' now clears FloppyDataReq and FloppyEndCount (page 8).
6. HdLd one-shot: e2a.1 to GND (page 10).
7. InUse signal to drive removed (drive can be jumpered), FDCTG43 and DiskChange signals added (page 11).

Additions

1. CP control and control store read/write, TPC/TC read and TPC write added (page 15).
2. Backplane connections added.
3. Separate IntReq register added (page 14). FloppyIntReq moved there.

Rev. D to Rev. E *(10/25/79)*

Bug Fixes

1. LS353 inputs to GND instead of Vcc (page 1)
2. Pullup for FDCDataReq.

Additions/Changes

1. Reorganization of bus structure. Two I/O data busses, IPData (TTL) and IPAData (MOS). This is due to loading reasons for the MOS devices.
2. Added CP Port, keyboard, Mouse interfaces, Printer, maintenance panel, time-of-day clock interface.
3. Increase Prom to 8K, RAM to 16K.
3. Alto module moved off IOP board.

Stitchweld Board History

S/N 001: A, B, stripped, E
S/N 002: B, C, D, scrapped
S/N 003: F
S/N 004: H

Dandelion I/O Processor

Revision History - 2

Rev. E to Rev. F

New Functions:
Redesign of maintenance panel, incorporation of time-of-day clock in IOP (pg. 24, 25)
Host address prom (pg. 14)
Backplane signals for Options IOP.

General:
All signals are named.
Separate pages for discretes and I/O connectors, different versions for PC and SW boards.
Backplane conforms to Backplane Rev. B.
Keyboard interface changed (pg.18)
Mouse front end redesigned (pg. 19)
CPStatus has new CSParErr, CPControl inputs (pg. 15)
IPData and IPAData bus enable logic changed (pg. 6)
SKY signals renamed to High.
Part substitutions as recommented by CP&T made.

Bug Fixes:
Enable of FDCData bus changed to avoid interference with Dma controller (pg.8)
pWaitClk' generated and used (pg. 15-17)
WakeMode inputs inverted on IOPReq prom (pg. 17)

Page 1: IPMemRd', IPIORd' BP changed 86, 186 to 79, 179.
LS240: b19h changed to b17a. b17d inverter added for IOPClk to BP 12.

Page 5: SelBank1a' - 1d', SelBank4, 5, backplaned.
I/O address banks renamed: 0a to 0, 0b to 1, ... 3a to 6, 3b to 7.
SelDma' moved to Bank 2, SelControlStore' renamed, moved to bank 6.

Page 6: EnIPData, EnIPAData generation changed. EnDataProm (c9) added. a12a, c9a, c9b, c6a removed.
Signal IPIORdWr named.

Page 7: DmaCycle backplaned.
DmaCh2Req, DmaCh3Req, DmaCh2Ack', DmaCh3Ack' named and backplaned.
DmaTest uses Ch2 signals. DmaTestReq/Ack' removed.

Page 8: FDCVFOen LS04 moved to pg. 12.
Bug fix for EnFDCData. Added LS00 g7d, g7c.
FDCId meaning changed to indicate 800/850 drive.
DmaTestReq in Floppy state renamed to DmaCh2Req.

Page 9: EY' on LS153 disconnected. LS253 replaced by LS153.

Page 10: S163 replaced by LS163.
Discretes moved to pg. 27

Page 11: I/O connector moved to pg. 27.
InUse added. SelDrive1, InUse, SelSide0 S240 always enabled
10 signals backplaned for Troy.

Page 12: FDCVFOen LS04 moved from pg. 8.

Page 13: DmaTestAck', SelDmaTest renamed to DmaCh2Ack', SelBank5'

Page 14: HostAddr prom added. Int5-7 backplaned.

Page 15: SwTAddr sense changed in CPControl = => IOPKernel change.
IOPWait, SwTAddr, SwTAddr' synced to CPClk before backplane. WrTPCLow' inverted before backplane.
Control Store write addresses permuted = => IOPKernel change.
LS240 b19 changed to b17. S00 (a19) moved to b18.
IOPStatus permuted. PWaitClk' used instead of pClk'

Page 16: S00 a19 moved to b18. LS240 b19 moved to b17. pWaitClk' used instead of pClk'.

Page 17: Bug fix WakeMode permutation on IOPReq prom. IOPAttn backplane changed from 139 to 138 (IODisp.1).
Extend CPPort status to include CSParErr, CPControl inputs.
Add pWaitClk'. S02 in a19, move S00 to b18.

Page 18: Moved KB connector to pg. 27.
Change KBSel', KBDiag' drivers from 74265 to 75114. FPLAT to RDIV16. Connector 1000pF capacitor between 75115 pins 6,7.

Page 19: Added new mouse front end (MouseProm). Moved MiscInput1 to pg. 20.

Page 20: MP connector moved to pg 27. MiscInput1 moved from pg. 19. MiscControl1 LS174 replaced by LS273.
KBBell changed by addition of discrete amplifier.
MiscClocks1 addition of SetClkD'. 1HzIntr' renamed 1HzClkB'.

Page 21: Floppy discretes moved to pg 27. FPLAT renamed RPULL16, PLAT18.
CPUReady changed. IPAData always causes Wait cycle, ExtWaitReq' available form backplane.

Page 22: KBBell clock added

Page 25, 26, 27, 28: New

Rev. F to Rev G ***3/25/80. Rev. G submitted to first etch.***

Bug Fixes: Added Schmitt trigger to BootReset' signal path to fix power boot problems (pg. 21)
Renamed ReadTime (e5.5, LS240) to ReadT since it is different from ReadTime (pg. 25, 26)
Added inverter to BellClk driver to cause driver to be off when bell is disabled (pg.20, 22).

Changes:
Backplaned IPDataOut (pg. 1), BRClk (pg. 22).
Moved CSParErr and TODIntr' to MiscInputs. Added EmuWake to CPStatus (pg. 14, 17, 20)

Dandelion I/O Processor

Revision History - 3

Rev. G to Rev. H *4/14/80. Minor changes, input to etch.*

Bug Fixes: PTCRxD line did not exist. Incorrectly connected to PTCTxD. Printer control (page 22).
Printer cable pin 20 incorrect on PC cable. Corrected to pin 10 (page p28).

Changes:
Backplaned IPALE (page 1) to pin 36 for use with State Analyzer.
ReadKB moved from MiscClocks to MiscControl (pg. 20)

Rev. H to Rev. I *4/21/80. Incorporation of Testability additions. Input to etch. No test pads in this Rev.*

Changes: Incorporation of testability features suggested by Fortiage memo.
Addition of miscellaneous timer for use as interrupt by CPU.

Page 1:
Isolation of CpuClk, CpuReset, CpuALE, DmaHoldReq with LS244 buffers under tester control.
Tester control of LS353 Enable inputs.
Change in IOPClk generation.

Page 6:
Tester control of EnDataProm CS' inputs.

Page 7:
Isolation of CpuHoldAck, DAck0-3', DmaEndCount, DmaAEN, DmaAddrStrobe by LS244 buffers under tester control.
DmaCycle generations changed.

Pages 8, 9, 10, 11, 12:
Isolation of FDCDataReq, FDCWrGate, FDCWrData with LS244 buffers under tester control.
Isolation of FDCEarly, FDCLate. Floppy16MHz generation changed.
Floppy cable receivers can be disabled under tester control.
FDCVFOen' isolated. Floppy proms can be disabled by tester.

Page 14:
MiscInt fed to Bit 4 of Int Req register.

Page 17:
IOPReq prom can be disabled by tester.

Page 19:
MouseProm can be disabled by tester.

Page 21:
CpuReady isolated by LS244 buffer

Page 22:
Extra timer added from 8253.

Page 27:
Keyboard cable moved to page 29 (PC only).
Tester discretes added. JUmper for Floppy disk Id added (PC only).

Rev. I to Rev. J *5/8/80. Incorporation of test pads. Input to etch 1.*

Changes: Incorporation of test pads.

Page 27:

Addition of 10K resistor to AltoIPReset' to pull up to Vcc when Alto not connected (PC only).

Dandelion I/O Processor

Design Notes

General

Wait states forced for all devices on IPAData. External WaitReq available for RS232 Z80-SIO.

CPU

1. See notes on memory address space (pg. 70, 71.
2. Mem, I/O Rd'/Wr' decoding changed to avoid LS257 potential glitching.

Floppy Disk Controller

1. WD1791 chip used temporarily. Eventually will use 1797 or 1793-01.
   This has the following effects:
   - inverted data bus - compensate in software.
   - no VFOE signal available (dummy one generated) for separator.
   - Side Select signal generated by Floppy Control register.
   - DMA worst case timing in DMA write: 1791 and 2114 has write setup time problem. (see page 32)
     1793-01/51 with 2114, or 1791 with 2114-3 OK.

   Current plan is to upgrade to use 1793-01 and not take advantage of the extra 1797 features.
   1797 can be plugged into same position.
2. Need 1 wait state with FDC chips and full-speed 8085A
3. Need FloppyDataReq latch when using 8257 DMA controller.
4. Floppy EndCount latch implemented to check correct DMA completion. Could be removed if not needed.
5. Floppy status register implemented to read external Floppy status. FloppyIntReq is in a common IntReq register.
6. Write compensation: Note jitter characteristics. Could use delay line or WD2143 if not tolerable.
   Currently a Disable write comp. in control register. Later,
   DisableWDComp' = [(DDen' or TG43')' . EnableWDComp]'
7. WriteCurrent signal not provided for drive (from TG43). Supplied in Rev. D
9. Select Drive 2 and Select Troy mode signals available.
10. Read Separator synchronizer has only one stage. When next reblowing Prom add a second stage (D0-Q0 of LS273). Feed DataSync' through LS273, Q0 to 1791 RData', Prom should expect comlement of RData.

DMA controller

1. Wait state required in slave mode.
2. Use extended write.
3. Intel 8257 chip used currently. Later could use 8237 controller.
   This provides programmable single byte transfer (see FloppyDataeq latch above).
4. Fully buffered address, control, and data buses.
5. Dma Test register added to channel 2 to allow Dma testing. The Dma Req is temporarily taken from Floppy State Register, using signal SelFloppyDrive2.
6. DmaTest register temporarily uses the whole of I/O bank 5 addresses.
7. DAck0' and DACK1' are fully loaded (80 uA, 1.6 mA)

CP port

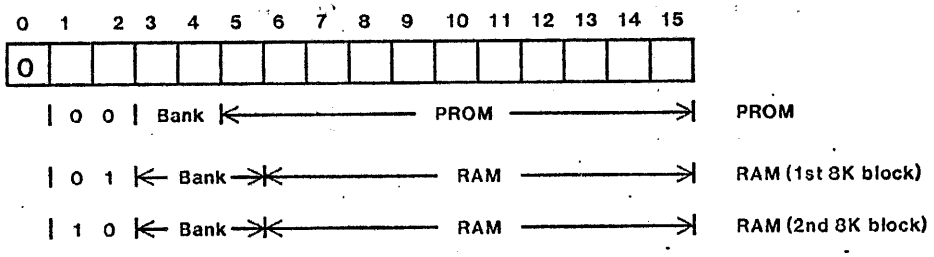
See programming description (pg. 72, 75)

TOD clock

Time-of-day clock has potential problem if IOP is powered and maintenance panel cable is unplugged. This is because there is some logic which is unpowered (in the TOD clock) which is driven by powered logic (in the IOP). This problem is to be described in a memo and will be further investigated.

Dandelion I/O Processor Address Space

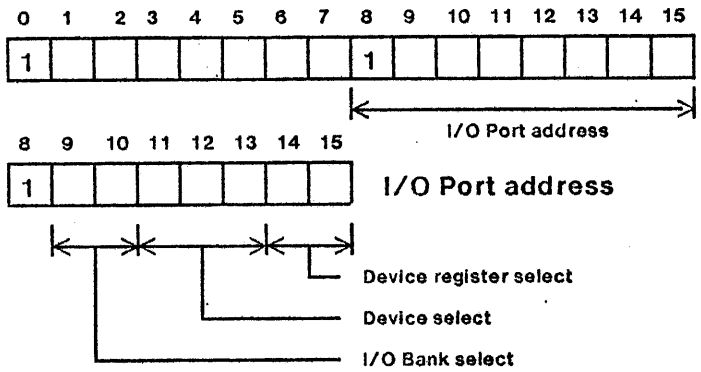
Normal memory address space



Bank	Type	Address Range (Hex)				Addr[1:2]
0	PROM	0	-	7FF	(2K)	0
1	PROM	800	-	0FFF	(2K)	0
2	PROM	1000	-	17FF	(2K)	0
3	PROM	1800	-	1FFF	(2K)	0
0	RAM	2000	-	23FF	(1K)	1
1	RAM	2400	-	27FF	(1K)	1
2	RAM	2800	-	2BFF	(1K)	1
3	RAM	2C00	-	2FFF	(1K)	1
4	RAM	3000	-	33FF	(1K)	1
5	RAM	3400	-	37FF	(1K)	1
6	RAM	3800	-	3BFF	(1K)	1
7	RAM	3C00	-	3FFF	(1K)	1
0	RAM	4000	-	43FF	(1K)	2
1	RAM	4400	-	47FF	(1K)	2
2	RAM	4800	-	4BFF	(1K)	2
3	RAM	4C00	-	4FFF	(1K)	2
4	RAM	5000	-	53FF	(1K)	2
5	RAM	5400	-	57FF	(1K)	2
6	RAM	5800	-	5BFF	(1K)	2
7	RAM	5C00	-	5FFF	(1K)	2

Dandelion I/O Processor Address Space

I/O Address Space



Notes:

1. I/O Ports can be reached using:

   a) IN or OUT instructions using port address:

   P = 80H + p, where 0 <= p <= 7FH (128)

   b) Memory reference instructions using address:

   A = 8000H + P, where P is given above.

   Note that bit 8 being 1 is not required by the hardware.

2. Bank addresses (hex):

Bank	*Address*	*Data bus*
Bank 0	80 - 8F	IPAData
Bank 1	90 - 9F	IPData
Bank 2	A0 - AF	IPAData
Bank 3	B0 - BF	IPData
Bank 4	C0 - CF	IPData
Bank 5	D0 - DF	IPData
Bank 6	E0 - EF	IPData
Bank 7	F0 - FF	IPData

3. Addresses in Banks 4 and 5 are reserved for the OPTIONS card. DmaTest temporarily uses bank 5.

Address (Hex)	Bank	
80	0	Alto PPI-A
81	0	Alto PPI-B
82	0	Alto PPI-C
83	0	Alto PPI-Control
84	0	Floppy Status (Read)
84	0	Floppy Command (Write)
85	0	Floppy Track (R, W)
86	0	Floppy Sector (R, W)
87	0	Floppy Data (R, W)
0E8	6	Floppy Control reg. (Write)
0E8	6	Floppy Status (ext.) (Read)
88	0	Printer data (R, W)
89	0	Printer Control (Write)
89	0	Printer Status (Read)
8A, 8B	0	(Same as 88, 89)
8C	0	Timer Counter 0 (R,W)
8D	0	Timer Counter 1 (R,W)
8E	0	Timer Counter 2 (R,W)
8F	0	Timer Mode (Write)
Dma 8257		
0A0	2	DMA Ch-0 Address
0A1	2	DMA Ch-0 Count
0A2	2	DMA Ch-1 Address
0A3	2	DMA Ch-1 Count
0A4	2	DMA Ch-2 Address
0A5	2	DMA Ch-2 Count
0A6	2	DMA Ch-3 Address
0A7	2	DMA Ch-3 Count
0A8	2	DMA Mode Set (Write)
0A8	2	DMA Status (Read)
0A9 - 0AF	2	Invalid
Temp:		
0D0	5	Dma Test register (R, W)
0D1 - 0DF	5	Invalid (DmaTest)
0B0	3	Host Address
0B1	3	Host Address
0B2	3	Host Address
|		|
0BC	3	Host Address
0BD	3	Host Address checksum
0BE - 0BF	3	Available in HA prom

Address (Hex)	Bank	
0E0 - 0E7	6	(unused)
0E9		Interrupt Request register (read)
0EA	6	Keyboard data (read)
0EB	6	CPIn (read)
0EC	6	CPStatus (read)
0ED	6	Mouse X (read)
0EE	6	Mouse Y (read)
0EF	6	Misc Inputs 1 (read)
0E9	6	Misc. Clocks 1 (write)
0EA	6	TOD Interrupt (clear)
0EB	6	CPOut (write)
0EC	6	Central processor Control (write)
0ED	6	Mouse XY (clear)
0EE	6	CP Dma Complete (clear)
0EF	6	Misc. Control 1 (write)
0F0 - 0F7	7	(Unavailable for Read)
0F8	7	Control Store Byte 0 (R, W)
0F9	7	Control Store Byte 1 (R, W)
0FA	7	Control Store Byte 2 (R, W)
0FB	7	Control Store Byte 3 (R, W)
0FC	7	Control Store Byte 4 (R, W)
0FD	7	Control Store Byte 5 (R, W)
0FE	7	TPC High (Addr, High 5 bits data') (W)
0FE	7	TC [0:3],,TPC[0:3]' (Read)
0FF	7	TPC Low (Low 7 bits data') (Write)
0FF	7	TPC[4:11]' (Read)

I/O Control and Status Registers

Write Registers

Bit	Floppy Control	Misc. Control 1	Misc. Clocks 1	CP Control	TPCHigh	TPCLow
Address (Hex)	E8	EF	E9	EC	FE	FF
0	Enable Wait cycles	(unused)	(unused)	IOPWait'	TPCAddr.0	(unused)
1	Enable Write Comp.	ReadKB	Clear MPanel	SwTAddr'	TPCAddr.1	TPCData.05'
2	Select Side 1	Enable Bell	Inc. MPanel	IOPAttn	TPCAddr.2	TPCData.06'
3	Select Troy Mode	Diagnose KB	Read Time Clk	CP DmaMode	TPCData.00'	TPCData.07'
4	Select Double Den.	Blank MPanel	Set Time ClkA	CP Dma In	TPCData.01'	TPCData.08'
5	Enable Floppy contr.	Read Time	Set Time ClkB	(unused)	TPCData.02'	TPCData.09'
6	Dma Ch 2 Request *	Clear Time	Set Time ClkC	(unused)	TPCData.03'	TPCData.10'
7	Select Drive 1	Set Time	Set Time ClkD	(unused)	TPCData.04'	TPCData.11'
0 = MSB 7 = LSB	* temporarily, later Select Drive 2		⊓			

Read Registers

Bit	Floppy Ext. Status	Misc. Inputs 1	Interrupt Req.	CP Status	TPCHigh	TPCLow
Address (Hex)	E8	EF	E9	EC	FE	FF
0	Disk Change	Alternate Boot	Floppy Req'	CP Attn' **	TC.0	TPCData.04'
1	Floppy End Count	Serial Time	Keyboard Req'	EmuWake' **	TC.1	TPCData.05'
2	Two-sided *	Misc. Interrupt	Printer Tx Req'	IOPAttn *	TC.2	TPCData.06'
3	Floppy ID **	Time 1 sec Req	Printer Rx Req'	CP DmaMode *	TC.3	TPCData.07'
4	(unused)	CS ParError'	(unused) *	CP Dma In *	TPCData.00'	TPCData.08'
5	(unused)	Mouse Sw 1	(unused) *	CPIn Int. Req.	TPCData.01'	TPCData.09'
6	(unused)	Mouse Sw 2	(LSEP UART Tx')	CPOut Int.Req	TPCData.02'	TPCData.10'
7	(unused)	Mouse Sw 3	(LSEP UART Rx')	CP Dma Compl.	TPCData.03'	TPCData.11'
0 = MSB 1 = LSB	* SA 850 only ** 0 = 800, 1 = 850		* Reserved for RS232	* From CPControl ** From IOPControl		

Notes:

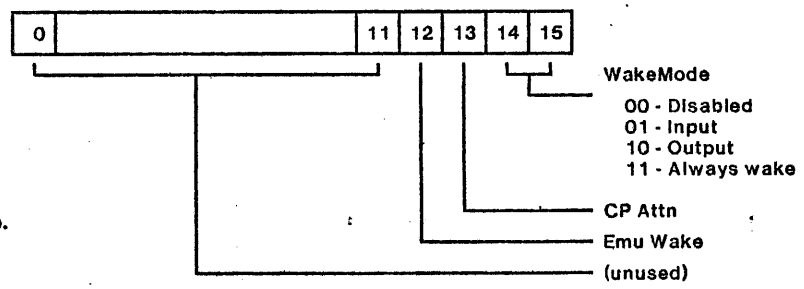
1. LSI devices control and status registers not shown here.
2. All numbers are decimal, except where indicated otherwise.
3. Single quote after name indicates active low value, e.g. TPCData.00'

XEROX SDD	Project	I/O Processor	File	Designer	Rev	Date	Page
	Dandelion	I/O Control and Status Registers	DandIOP72.silx	Ogus	1	4/22/80	72

CP IOP Task Programming

IOP Control Register

IOPCtl ← in any cycle

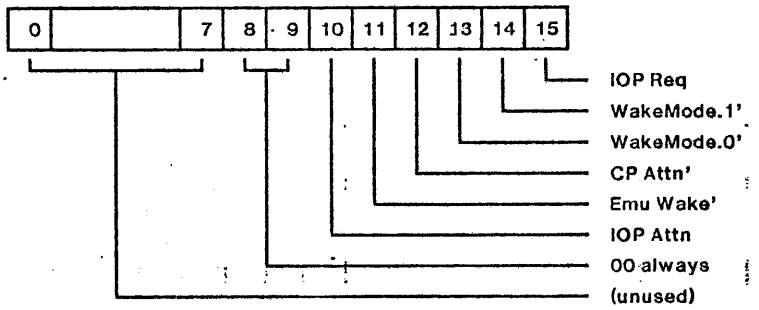


This register controls the mode of the IOP interface.
When disabled, EmuWake or IOPAttn will cause task wakeup.
Input mode, input data full will cause task wakeup.
output mode, output data empty will cause task wakeup.
always wake mode, wakeup always active.

CPAttn causes a service request to the IOP.
Emu Wake should be set by the emulator when task wakeup is required.
Note: Emu Wake should be set by the emulator in one click by a read-modify-write.

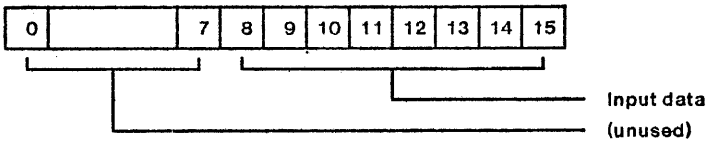
IOP Status Register

← IOPStatus in any cycle



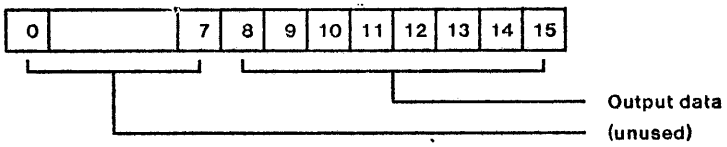
IOPIData Register

← IOPIData in any cycle



IOPOData Register

IOPOData ← in any cycle



Programming Notes.

1. IOP port can be used on a polling or wakeup basis. The kernel task can use the port with the polling method.
   The IOP task uses the wakeup method.

2. Polling Method.

   Poll IOP Request in IOP Status to determine when to transfer data.
   After writing IOP Control, IOPReq is not valid in the next cycle.

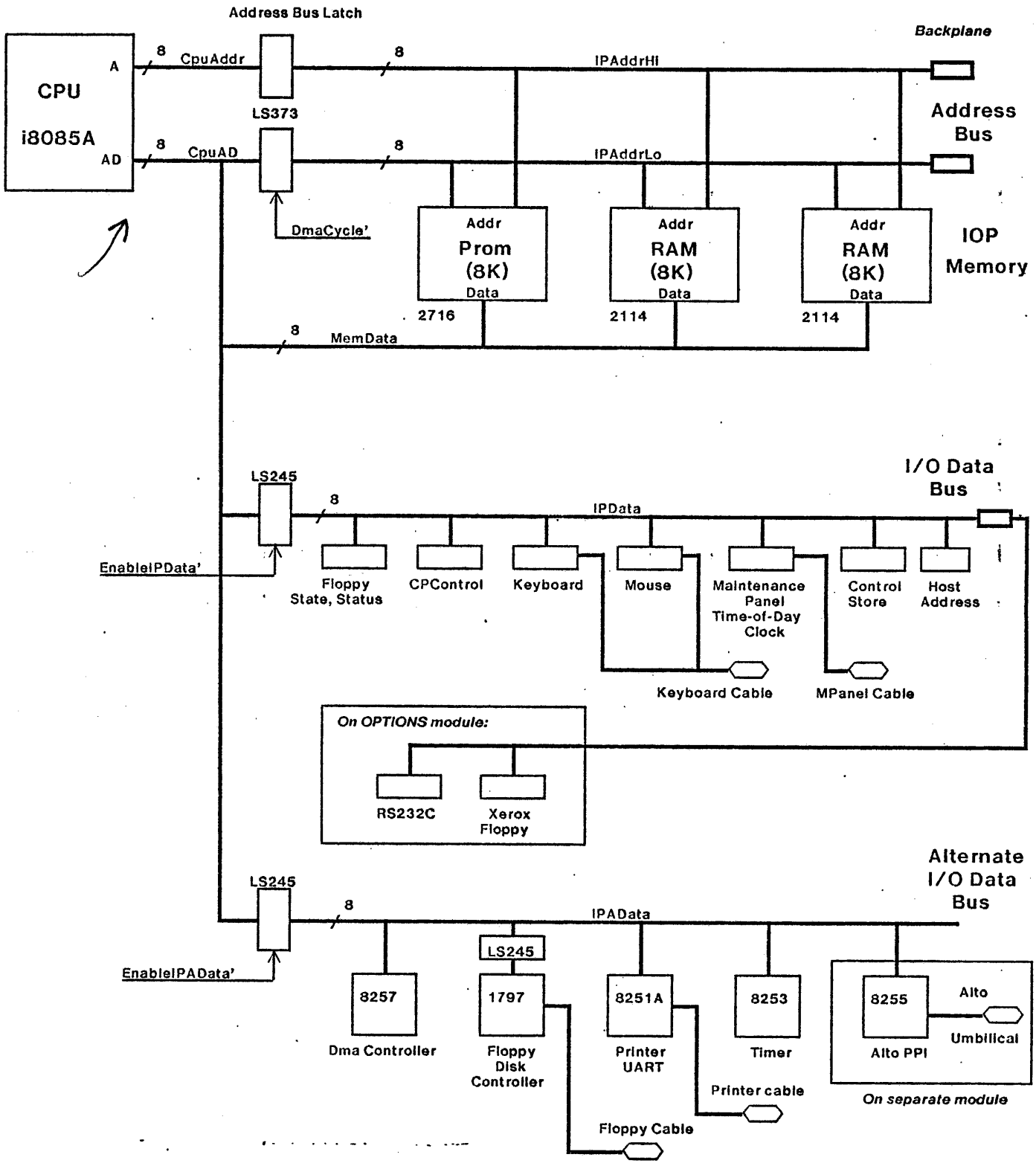
```
i.e.   IOPCtl ← k          ,c*; {Write Control register}
       Noop                ,c*; {IOPReq NOT valid in this instruction}
       R ← IOPStatus       ,c*; {IOPReq now valid in IOPStatus}
```

   After reading or writing data, IOPReq is not valid for 3 cycles.

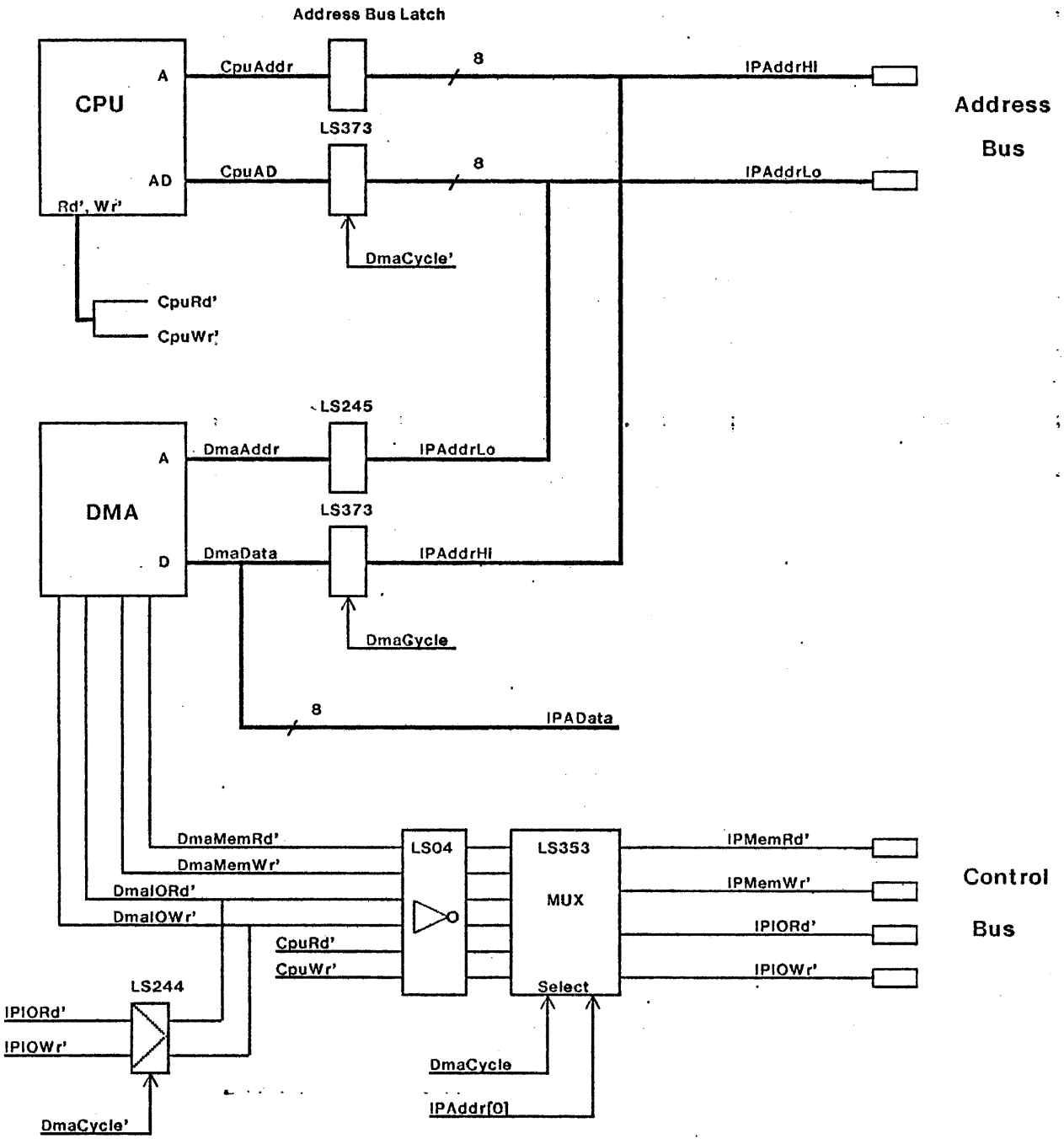
```
i.e.   IOPOData ← R        ,c*; {Write output data}
       Noop                ,c*; {IOPReq NOT valid in this instruction}
       Noop                ,c*; {IOPReq NOT valid in this instruction}
       Noop                ,c*; {IOPReq NOT valid in this instruction}
       R ← IOPStatus       ,c*; {IOPReq now valid in IOPStatus}
```

3. Wakeup method.

   When in input or output mode, the transfer of data will cause the task wakeup to be removed.
   The wakeup will be re-asserted when the appropriate data conditions are true again (see IOPControl above)



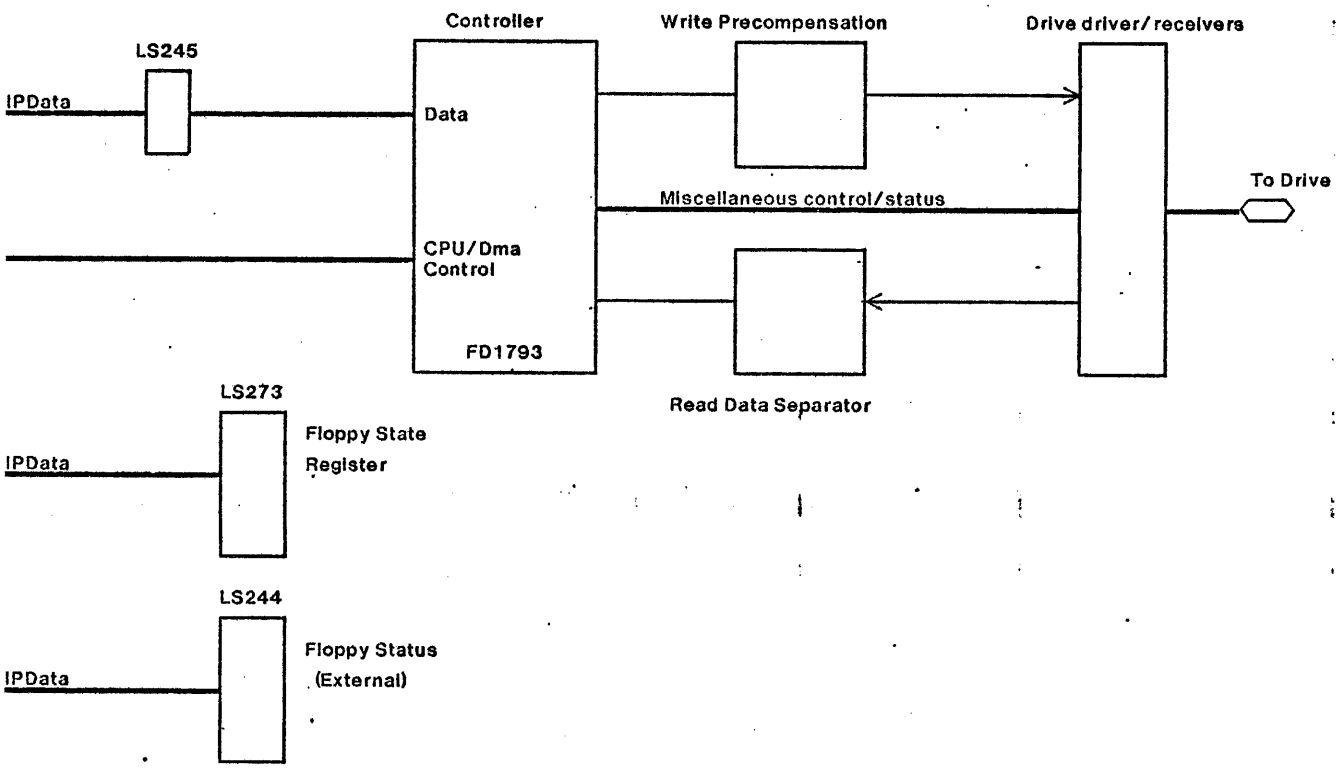
XEROX SDD	Project: Dandelion	I/O Processor Data Paths	File: DandIOP80.silx	Designer: Ogus	Rev: F	Date: 2/26/80	Page: 80



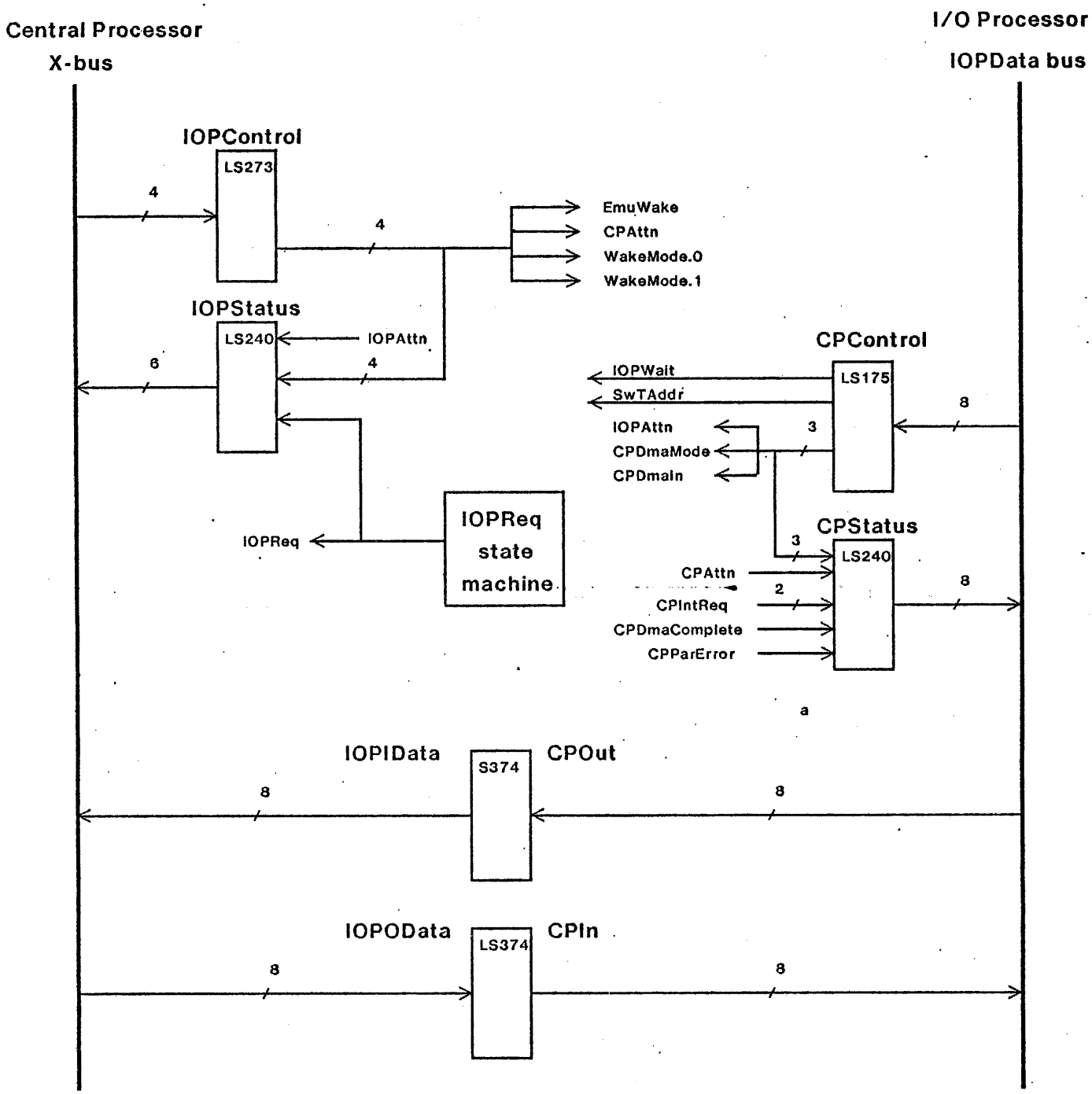
XEROX SDD	Project Dandelion	I/O Processor Control Organization	File DandIOP81.silx	Designer Ogus	Rev F	Date 2/26/80	Page 81

I/O Processor Floppy Disk Controller

Block Diagram



XEROX SDD	Project Dandelion	I/O Processor Floppy Controller Block Diag.	File DandIOP82.silx	Designer Ogus	Rev F	Date 2/26/80	Page 82



XEROX SDD	Project Dandelion	I/O Processor CP - IOP port block diagram	File DandIOP83.silx	Designer Ogus	Rev F	Date 2/26/80	Page 83

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El Segundo, California 90245

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MATERIAL LIST

ML	Drawing No.	Rev.
		A

Rev.	Drawing Title
Dwg. No.	**Dandelion IOP Parts list for Revision G** File: IOPParts1-G.sil in : [IRIS]<Workstation>IOP>IOPParts-G.dm
ML	

Model No.	Date	Sheet
	3/25/80	1 of 2

Item No.	Drawing Title		Drawing No.	No. Req.	Remarks
	Integrated Circuit	i8085A		1	Intel microprocessor
		i8257-5 (Alt: AMD 9517-4)		1	Dma controller
		i8251A		1	UART
		i8253-5		1	Timer
		FD1797 (Alt: FD1793-01)		1	Western Digital Floppy Disk controller
		i2114L		32	low power 2114, 450 nsec 1k x 4 RAM
		i2716		4	2Kx8 Prom
		F93427		4	256x4 Prom
		F93453		2	1024x4 Prom
		SN74S00		1	
		SN74S02		2	
		SN74S74		1	
		SN74S240		4	
		SN74S374		2	
		SN74LS00		3	
		SN74LS04		3	
		SN74LS08		4	
		SN74LS32		4	
		SN74LS74		8	
		SN74LS138		7	
		SN74LS153		1	
		SN74LS155		1	
		SN74LS157		2	
		SN74LS163		1	
		SN74LS165		4	
		SN74LS175		2	
		SN74LS240		7	
		SN74LS244		2	
		SN74LS245		4	
	Integrated Circuit	SN74LS273		4	

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MATERIAL LIST

ML	Drawing No.	Rev. B

Rev. No.

Drawing Title

Dandelion IOP parts list for Revision G

File: IOPParts2-G.sil
In: [IRIS]<Workstation>IOP>IOPParts-G.dm

Model No. | Date 3/25/80 | Sheet 2 Of 2

ML

Item No.	Drawing Title		Drawing No.	No. Req.	Remarks
	Integrated Circuit	SN74LS353		2	
		SN74LS373		3	
		SN74LS374		7	
		SN74LS393		4	
		SN74LS569		4	or Am25LS2569
		SN7414		1	
		SN74123		1	
		SN75114		1	
		SN75115		1	
		SN75188		1	
	Integrated Circuit	SN75189		1	
	Oscillator	K1114A, 6.000 MHz		1	Motorola or equiv. Alt.: 5.88 MHz
	Oscillator	K1114A, 16.000 MHz		1	Motorola or equiv.
	Oscillator	K1114A, 1.8432 MHz		1	Motorola or equiv.
	Capacitor	1000 pF, 25 V		1	
	Capacitor	1.0 uF, 10 uF, 39 uF, 25V		1 ea.	
	Capacitor	.1 uF bypass, 25V		1 per 3 chip positions	
	Capacitor	15 uF, 25V		2	VDD, VFF bypass
	Resistor	4.7 ohm, 1/2 watt		1	
	Resistor	150 ohm, 1/4 watt		7	(Stitchweld version only)
	Resistor	470 ohm, 1/4 watt		2	
	Resistor	220, 1K, 15K, 68K, 1/4 watt		1 ea.	
	DIP Resistor Network	150 ohm series 2% Allen Bradley 316B151		1	(PC version only)
	DIP Resistor Network	130/210 pullup-pulldown — 2% Allen Bradley 316E131211	- - -	1	
	DIP Resistor Network	15- 10K resistors 2% Allen Bradley 316A103		1	
	DIP Resistor Network	15- 5.1K resistors 2% Allen Bradley 316A512		1	
	Transistor	2N2905A		1	
	Diode	1N4003		3	
	Fuse	7 amp (2), 15 amp slow blow		3	
	Socket	18-pin DIP socket		1	Alto umbilical

Dandelion I/O Processor

Logic Drawings

	Drawing	File
1.	CPU	DandIOP01.sil
2.	PROM, memory control	DandIOP02.sil
3.	4K RAM memory Banks 0 - 3	DandIOP03.sil
4.	4K RAM memory Banks 4 - 7	DandIOP04.sil
5.	I/O Control	DandIOP05.sil
6.	I/O Data Bus control	DandIOP06.sil
7.	DMA controller	DandIOP07.sil
8.	Floppy Disk Controller	DandIOP08.sil
9.	Floppy Disk Controller Write Comp.	DandIOP09.sil
10.	Floppy Disk Controller Miscellaneous	DandIOP10.sil
11.	Floppy Disk Receivers/Drivers	DandIOP11.sil
12.	Floppy Disk Controller Data Separator	DandIOP12.sil
13	Dma Test register	DandIOP13.sil
14.	Interrupt Request register	DandIOP14.sil
15.	CP control, Control store	DandIOP15.sil
16.	CP-IOP port	DandIOP16.sil
17.	CP-IOP port - 2	DandIOP17.sil
18.	Keyboard Interface	DandIOP18.sil
19.	Mouse Interface	DandIOP19.sil
20.	Time-of-Day/Maintenance Panel interface	DandIOP20.sil
21.	Miscellaneous CPU control	DandIOP21.sil
22.	Printer Interface	DandIOP22.sil
23.	4K RAM memory Banks 8 - 11	DandIOP23.sil
24.	4K RAM memory Banks 12 - 15	DandIOP24.sil

Dandelion I/O Processor

Documentation Drawings

Drawing		File
0.	Drawings - Logic	DandIOP00.silx
0a.	Drawings - Documentation	DandIOP00a.silx
0b.	Revision History	DandIOP00b.silx
0c.	Design Notes	DandIOP00c.silx
Block Diagrams:		
0d.	IOP Data Paths	DandIOP00d.silx
0e.	IOP Control	DandIOP00e.silx
0f.	Floppy Disk Controller Block Diagram	DandIOP00f.silx
Timing:		
30.	Timing: Cpu-FDC	DandIOP30.silx
31.	Timing: Cpu-Mem	DandIOP31.silx
32.	Timing: Dma-FDC	DandIOP32.silx
33.	IOP-CP Communication	DandIOP33.silx
35.	Alto-IOP Communication - 1	DandIOP35.silx
36.	Alto-IOP Communication - 2	DandIOP36.silx
39.	FDC Write Comp. Timing	DandIOP39.silx
Loading:		
40.	Signal Loading - 1	DandIOP40.silx
41.	Signal Loading - 2	DandIOP41.silx
42.	Signal Loading - 3	DandIOP42.silx
Addressing:		
50.	I/O Processor Address space - Memory	DandIOP50.silx
51.	I/O Processor Address space - I/O	DandIOP51.silx
Construction:		
53.	IOP Platforms	DandIOP53.silx
54.	IOP Platforms	DandIOP54.silx
55.	Keyboard Cable	DandIOP55.silx
56	Floppy Disk Signal Cable, Misc. cable	DandIOP56.silx
57.	Floppy Disk Cables	DandIOP57.silx
60.	Board stuffing sheet	DandIOP60.silx
61.	Board layout	DandIOP61.silx

Dandelion I/O Processor

Revision History

Board History

S/N 001: A, B, stripped, E
S/N 002: B, C, D

Rev. A to Rev. B

1. Signals on A and B ports of LS245 (g11) switched to account for correct sense of CpuS1 signal. (T = 1 => A to B) (pg. 1)
2. Enable (pin 1) of LS240 connected to GND. (pg. 1)
3. Prom macro changed for i2716 (h12), to reverse data bus connection. (pg. 2)
4. Ports PA, PB, and data bus reversed on I8255A (j9) with macro change. (pg. 5).

Rev. B to Rev. C

1. DMA controller added (pg. 7).
2. Floppy Disk controller added (pgs. 8-12).
3. New bus organization (see page 00c)
4. Address space change, to allow both memory or normal I/O mapping. IPAddr.00 on e8, f8, pin 14 (pg. 1).
5. IPDataOut signal (c6b, pin 9, pg. 1).
6. CPUReady signal to insert wait state for FDC, and DMA (slave). (pg. 6)
7. Change in generation of IPMemRd', IPMemWr', IPIORd', IPIOWr'. This removes the LS257 to avoid the output glitches which occur when device goes from tristate to active. (Gary Miller, Intel, 987-8086, 6/20/79) (pg. 1).
8. New I/O address decoding (pg. 5)
9. Page 5 renumbered to 13.

Rev. C to Rev. D.

Bug Fixes

1. Added inverters for CpuRd', CpuWr', DmaMemRd', DmaMemWr', DmaIORd', and DmaIOWr' and replaced LS253 with LS353 to fix multiplexor glitch when S2, S1 lines change. (page 1)
2. Fixed pullups for FloppyIntReq, FDCVFOen' (i6, page 6).
3. Removed boot switch backplane signal (pg. 6).
4. Buffered FDCHdLd (page 8).
5. IPReset' now clears FloppyDataReq and FloppyEndCount (page 8).
6. HdLd one-shot: e2a.1 to GND (page 10).
7. InUse signal to drive removed (drive can be jumpered), FDCTG43 and DiskChange signals added (page 11).

Additions

1. CP control and control store read/write, TPC/TC read and TPC write added (page 15).
2. Backplane connections added.
3. Separate IntReq register added (page 14). FloppyIntReq moved there.

Rev. D to Rev. E *(10/25/79)*

Bug Fixes

1. LS353 inputs to GND instead of Vcc (page 1)
2. Pullup for FDCDataReq.

Additions/Changes

1. Reorganization of bus structure. Two I/O data busses, IPData (TTL) and IPAData (MOS). This is due to loading reasons for the MOS devices.
2. Added CP Port, keyboard, Mouse interfaces, Printer, maintenance panel, time-of-day clock interface.
3. Increase Prom to 4K, RAM to 16K.
3. Alto module moved off IOP board.

Dandelion I/O Processor

Design Notes

General

1. Rev E appears to have space for RS232-C DTE.

CPU

1. See notes on memory address space.
2. Mem, I/O Rd'/Wr' decoding changed to avoid LS257 potential glitching.

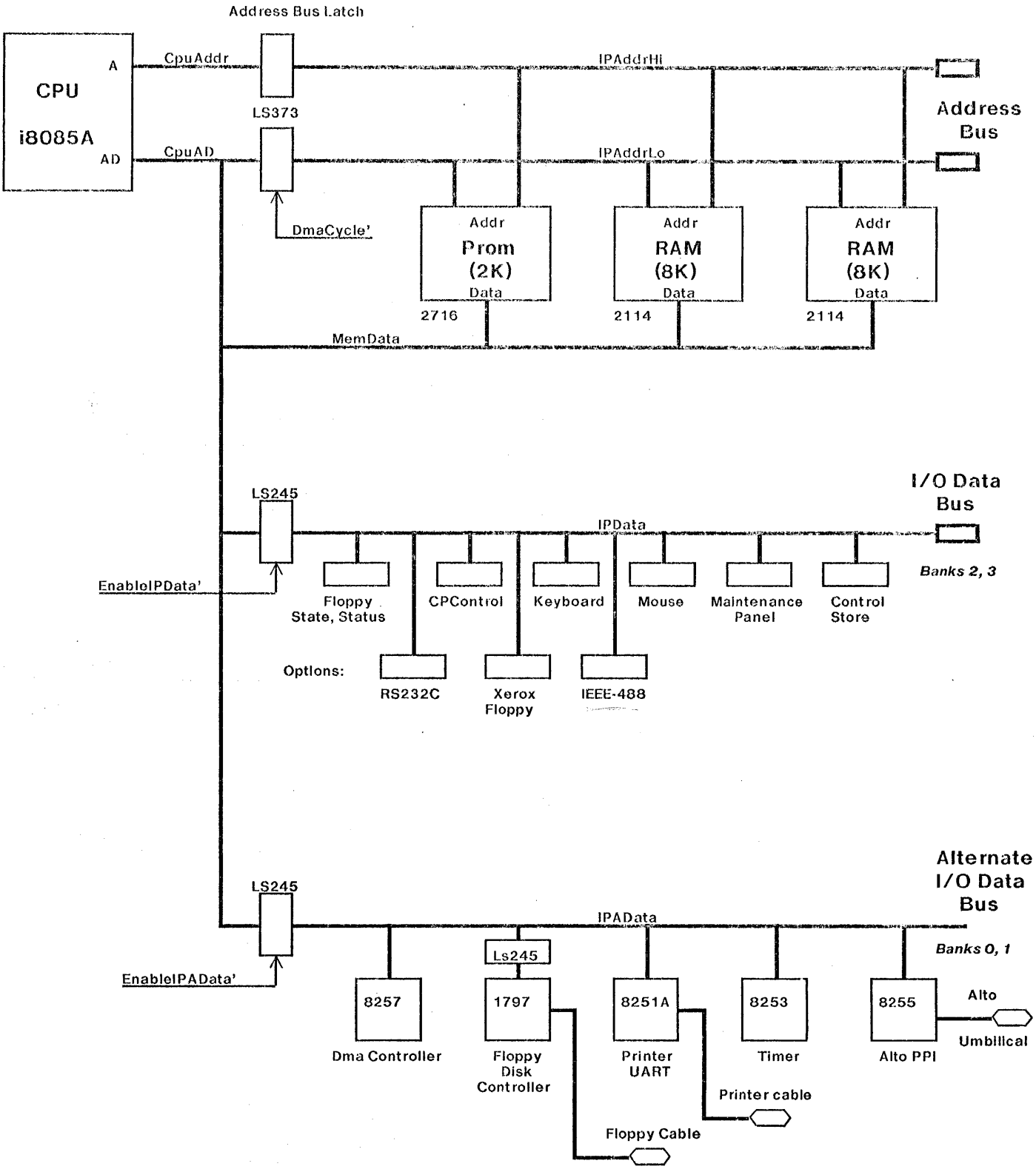
Floppy Disk Controller

1. WD1791 chip used temporarily. Eventually will use 1797 or 1793-01.
   This has the following effects:
   - inverted data bus - compensate in software.
   - no VFOE signal available (dummy one generated) for separator.
   - Side Select signal generated by Floppy Control register.
   - DMA worst case timing in DMA write: 1791 and 2114 has write setup time problem. (see page 32)
     1793-01/51 with 2114, or 1791 with 2114-3 OK.

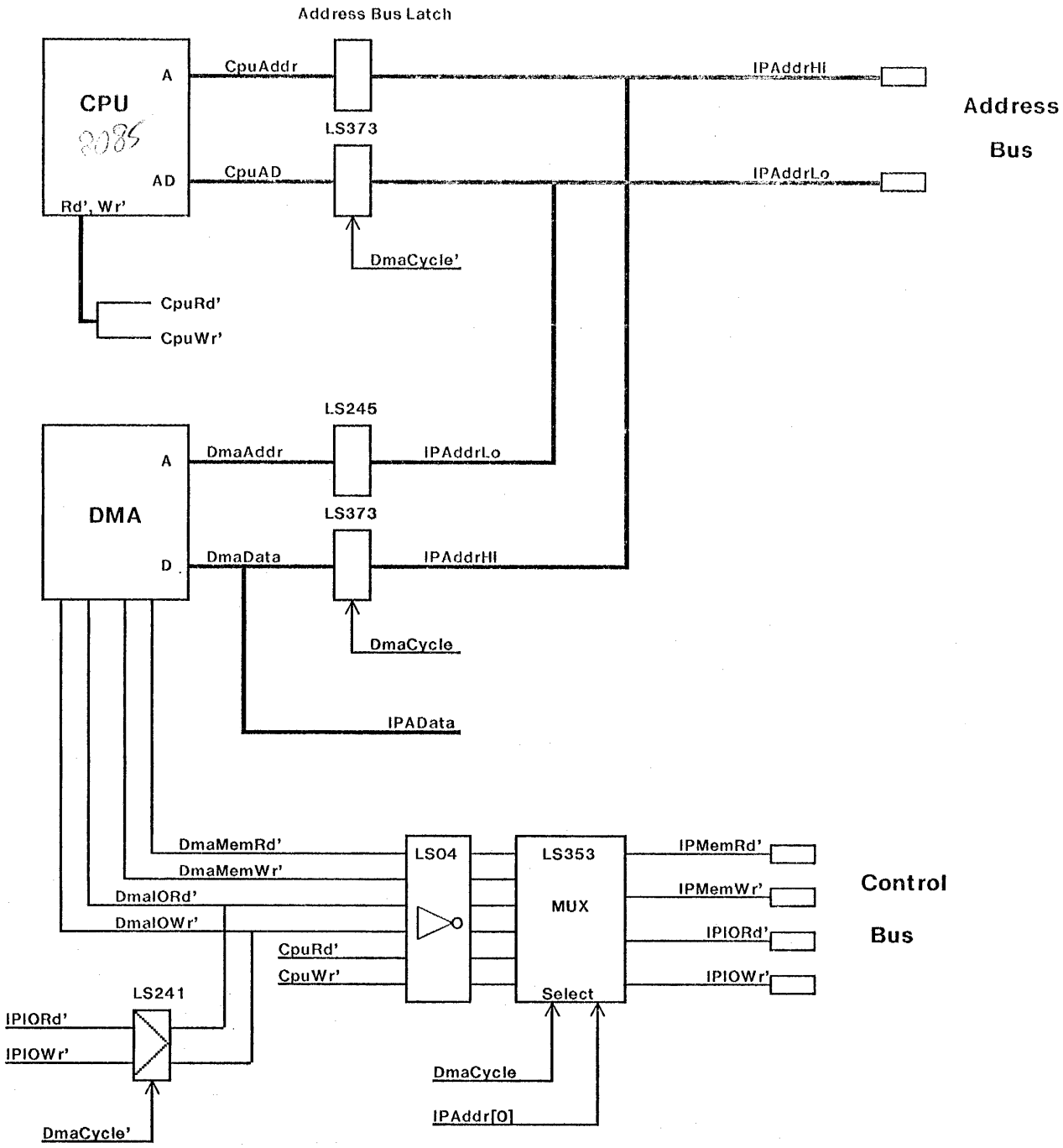
   Current plan is to upgrade to use 1793-01 and not take advantage of the extra 179/ features.
   1797 can be plugged into same position.
2. Need 1 wait state with FDC chips and full-speed 8085A
3. Need FloppyDataReq latch when using 8257 DMA controller.
4. Floppy EndCount latch implemented to check correct DMA completion. Could be removed if not needed.
5. Floppy status register implemented to read external Floppy status. FloppyIntReq is in
   a common IntReq register.
6. Write compensation: Note jitter characteristics. Could use delay line or WD2143 if not tolerable.
   Currently a Disable write comp. in control register. Later,
   DisableWDComp' = [(DDen' or TG43')' . EnableWDComp]'
7. WriteCurrent signal not provided for drive (from TG43). Supplied in Rev. D
8. FD cable is wired to provide ID bit to determine presence of drive.
9. Select Drive 2 and Select Troy mode signals available.
10. Read Separator synchronizer has only one stage. When next reblowing Prom add a second stage (D0-Q0 of LS273).
    Feed DataSync' through LS273, Q0 to 1791 RData', Prom should expect comlement of RData.

DMA controller

1. Wait state required in slave mode.
2. Use extended write.
3. Intel 8257 chip used currently. Later could use 8237 controller.
   This provides programmable single byte transfer (see FloppyDataeq latch above).
4. Fully buffered address, control, and data buses.
5. Dma Test register added to channel 2 to allow Dma testing. The Dma Req is temporarily taken from Floppy State Register,
   using signal SelFloppyDrive2.
6. DmaTest register temporarily uses the whole of I/O bank 1b addresses.
7. DAck0' and DACK1' are fully loaded (80 uA, 1.6 mA)



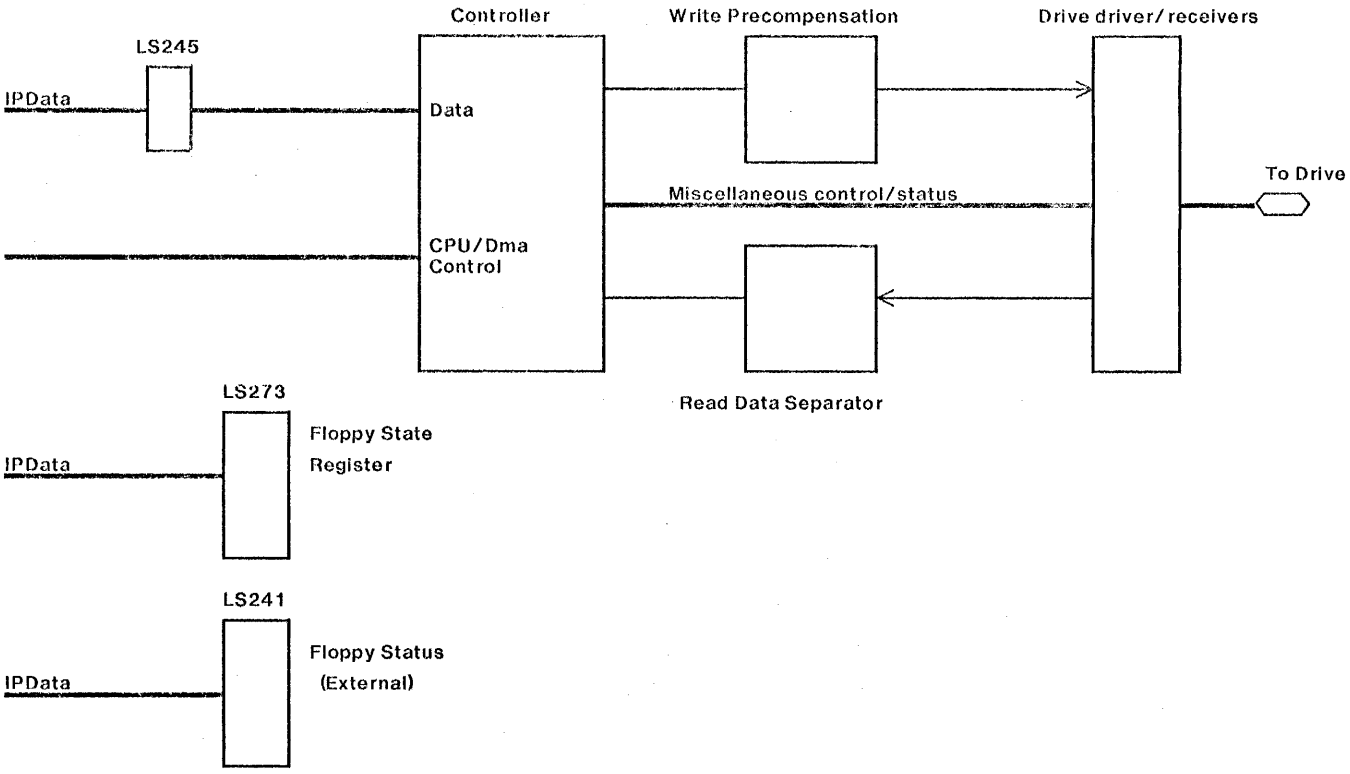
XEROX SDD	Project Dandelion	I/O Processor Data Paths	File DandIOP00d.silx	Designer Ogus	Rev E	Date 10/10/79	Page 00d



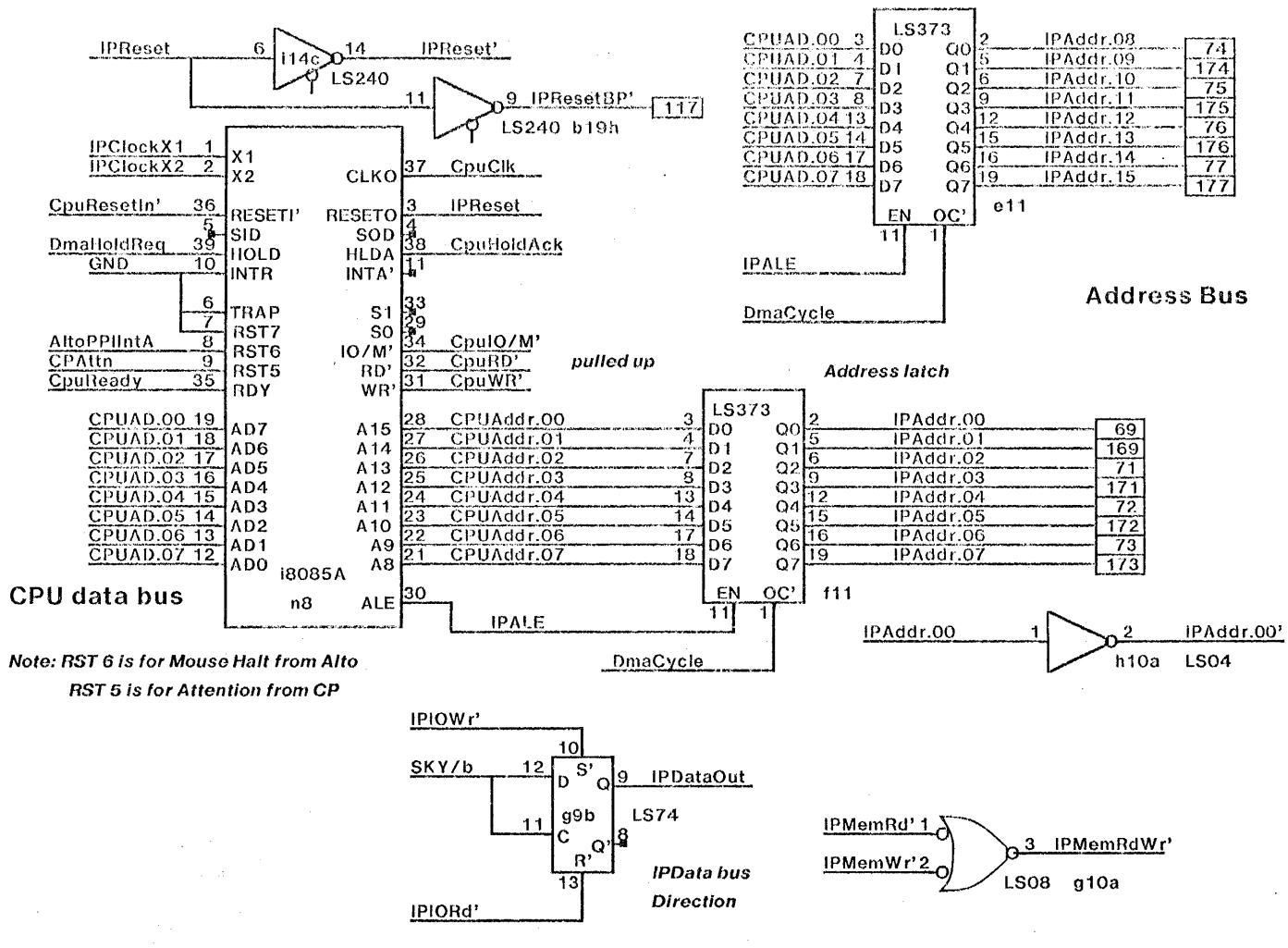
XEROX SDD	Project Dand/IOP	I/O Processor Control Organization	File DandIOP00e.silx	Designer Ogus	Rev E	Date 10/10/79	Page 00e

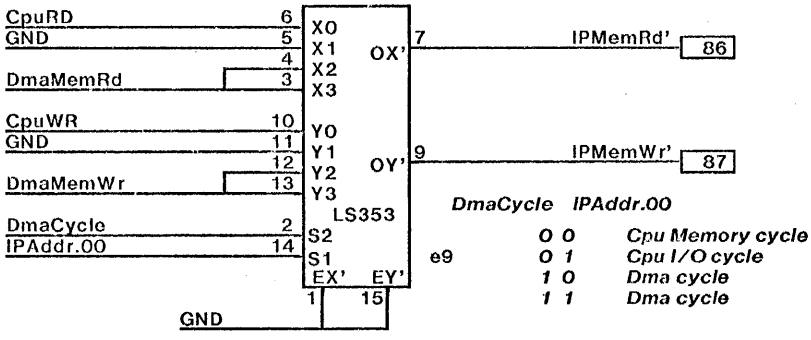
I/O Processor Floppy Disk Controller

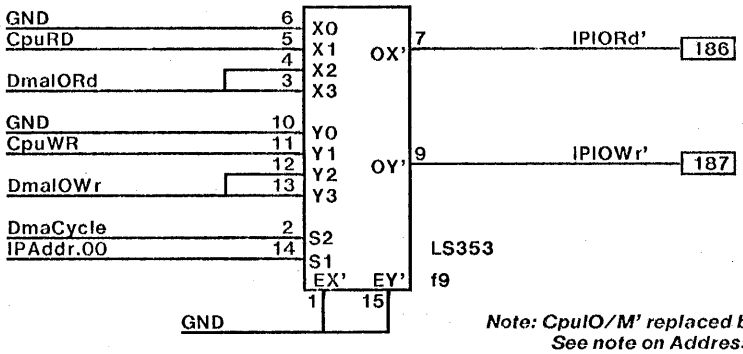
Block Diagram

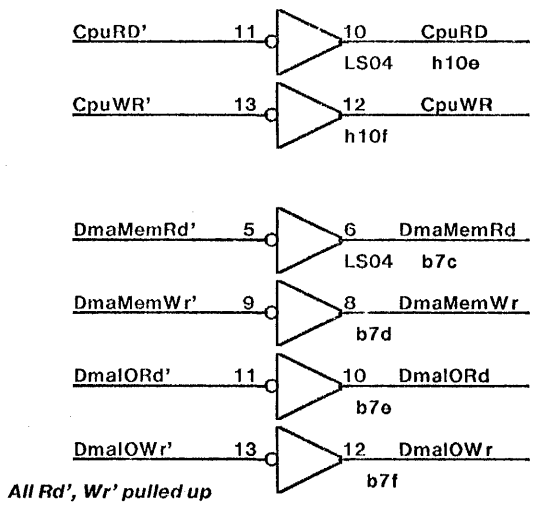


XEROX SDD	Project: Dandelion	I/O Processor Floppy Controller Block Diag.	File: DandIOP00f.silx	Designer: Ogus	Rev: E	Date: 10/4/79	Page: 00f



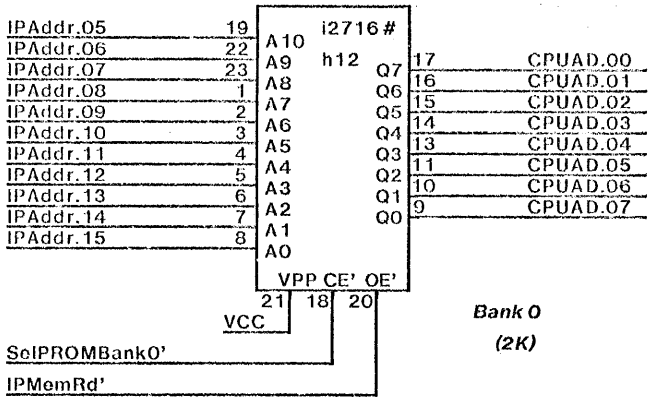


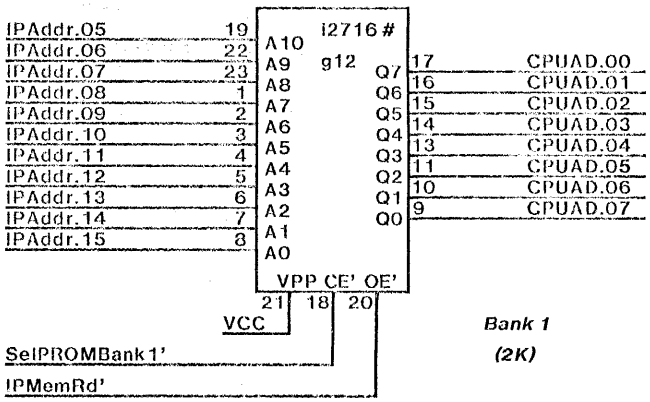


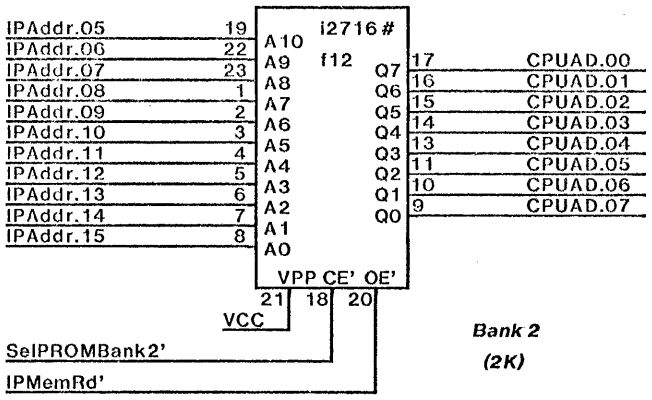


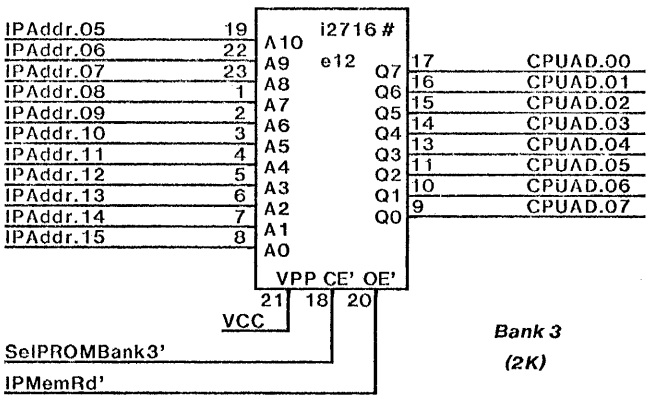
XEROX SDD	Project Dand/IOP	I/O Processor CPU	File DandIOP01.sil	Designer Ogus	Rev E	Date 10/24/79	Page 01

Prom



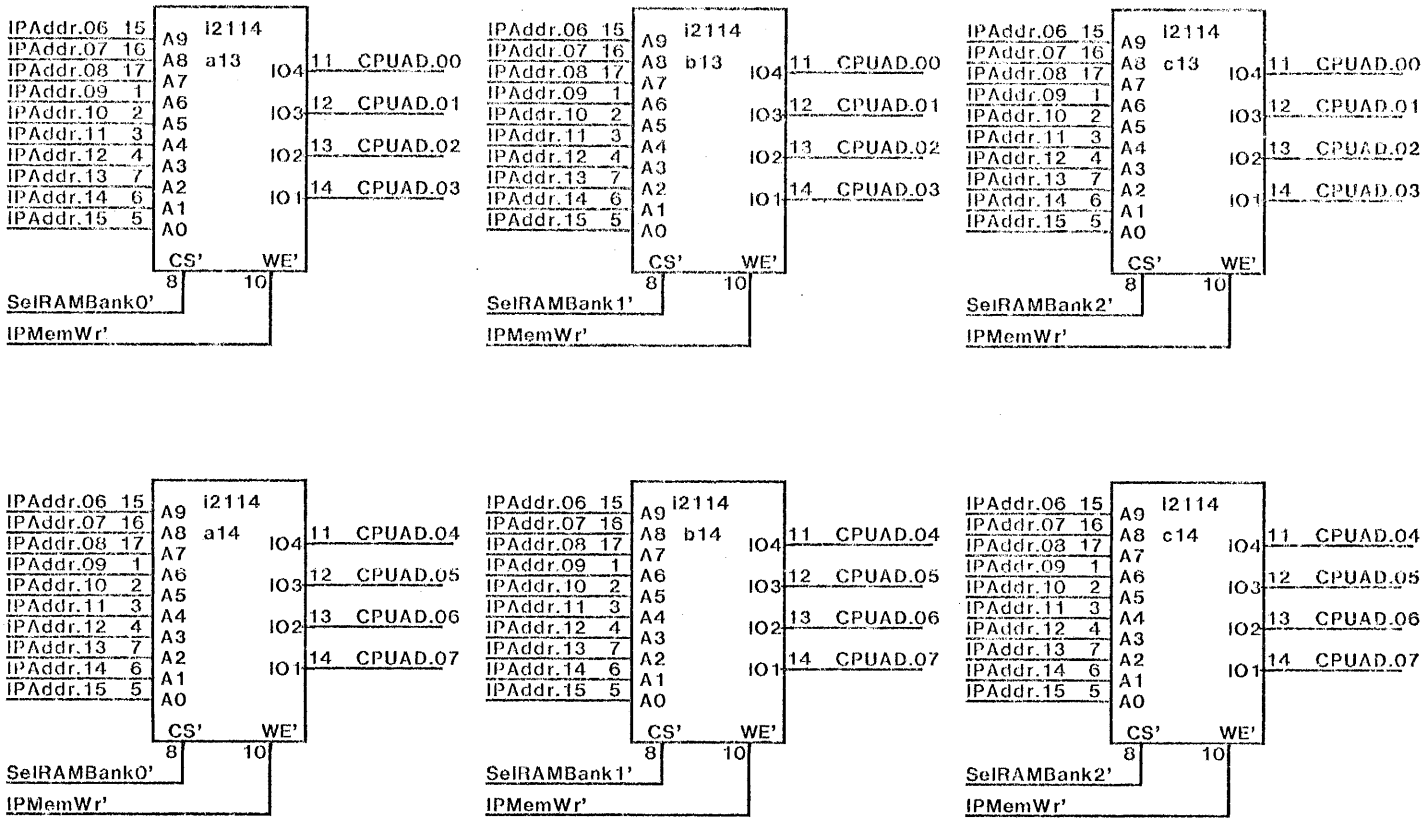




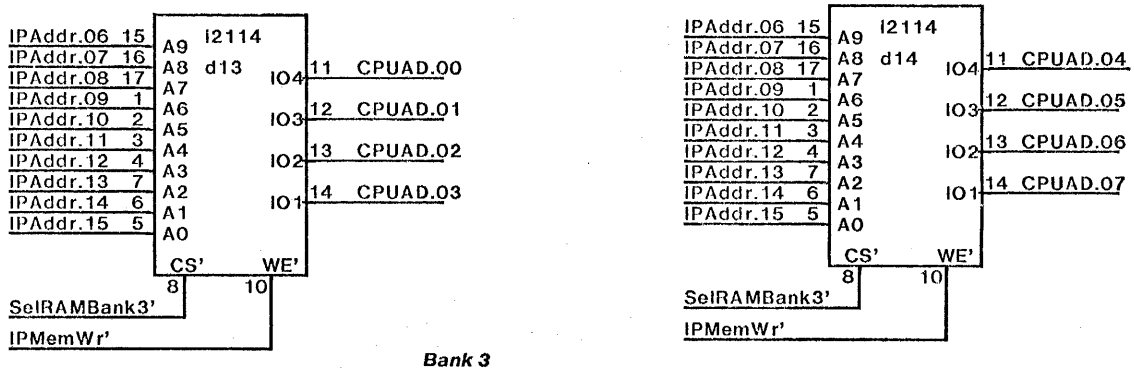


XEROX SDD	Project Dand/IOP	I/O Processor PROM	File DandIOP02.sil	Designer Ogus	Rev E	Date 10/24/79	Page 02

RAM - Banks 0 - 3



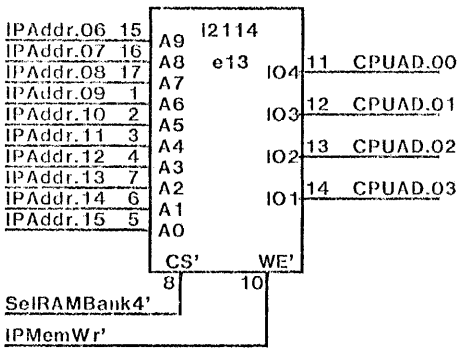
Bank 0 *Bank 1* *Bank 2*

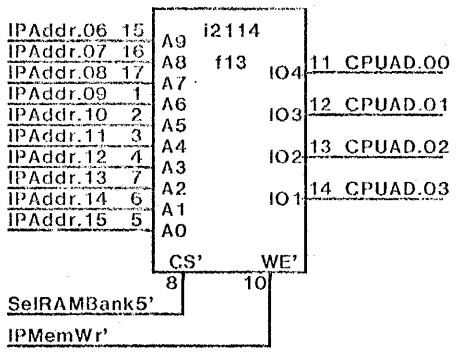


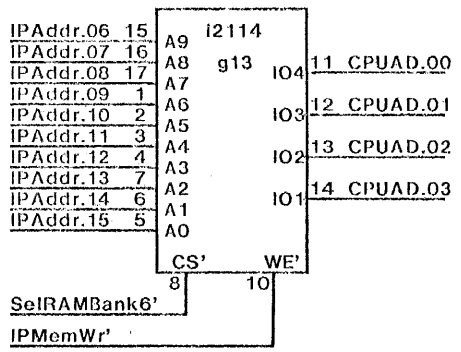
Bank 3

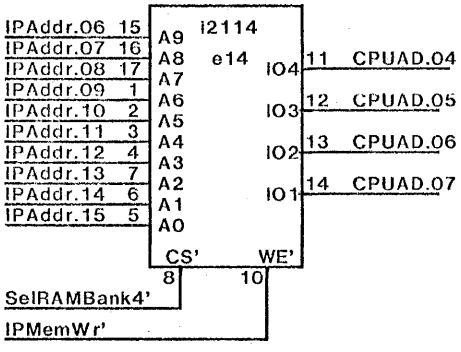
XEROX SDD	Project: Dand/IOP	I/O Processor 4K RAM Memory-Banks 0 - 3	File: DandIOP03.sil	Designer: Ogus	Rev: E	Date: 10/24/79	Page: 03

RAM - Banks 4 - 7

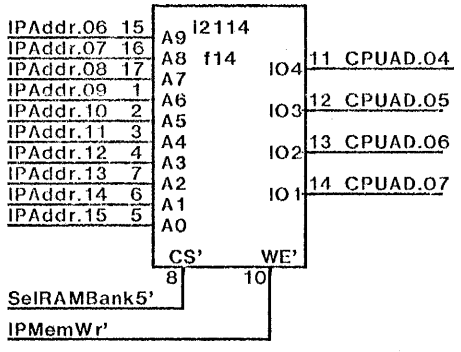




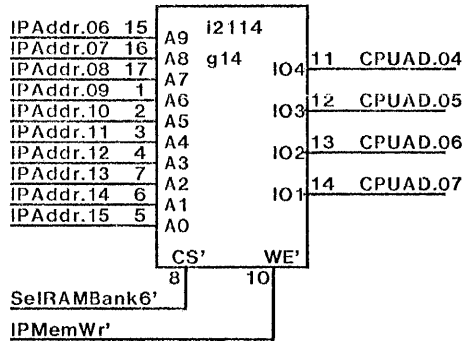




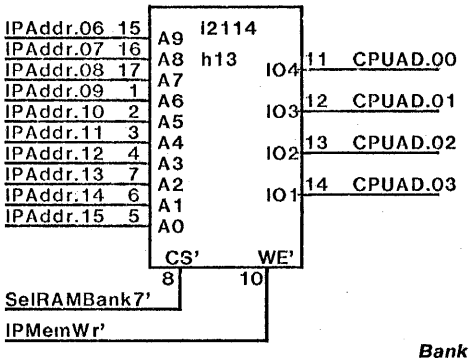
Bank 4



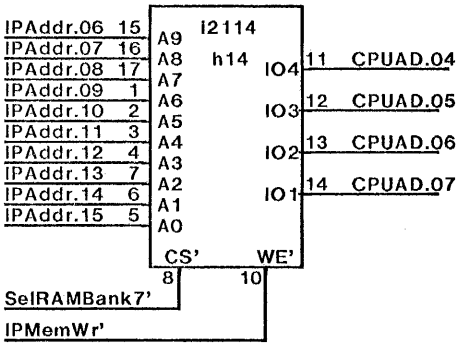
Bank 5



Bank 6



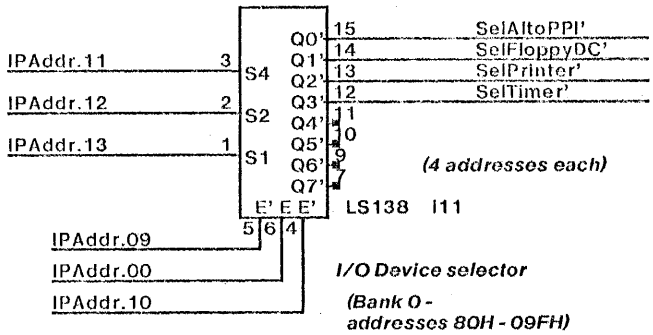
Bank 7



XEROX SDD	Project: Dandelion	I/O Processor 4K RAM Memory-Banks 4-7	File: DandIOP04.sil	Designer: Ogus	Rev: E	Date: 10/24/79	Page: 04

I/O Control

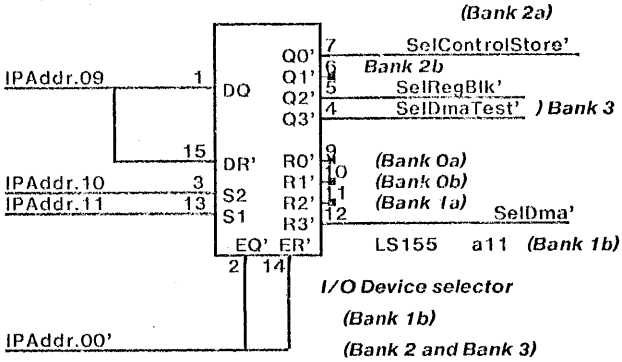
(Depends on Addr[0] = Addr[8], etc. for I/O. IPAddr[0] = 1 for I/O addresses.)



(4 addresses each)

I/O Device selector
(Bank 0 -
addresses 80H - 09FH)

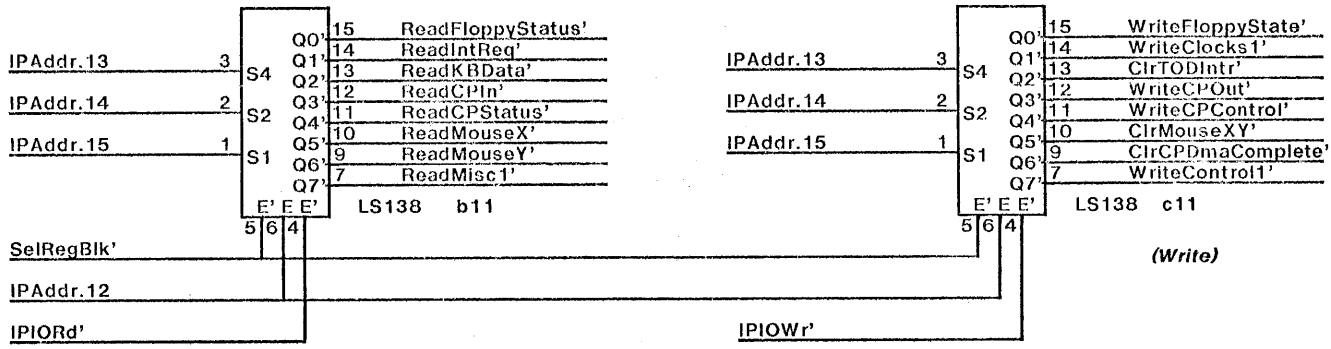
(Bank 2a)



Bank 2b
) Bank 3
(Bank 0a)
(Bank 0b)
(Bank 1a)
(Bank 1b)

I/O Device selector
(Bank 1b)
(Bank 2 and Bank 3)
(16 registers each)

Note: Bank 3B is temporarily used by SelDmaTest'

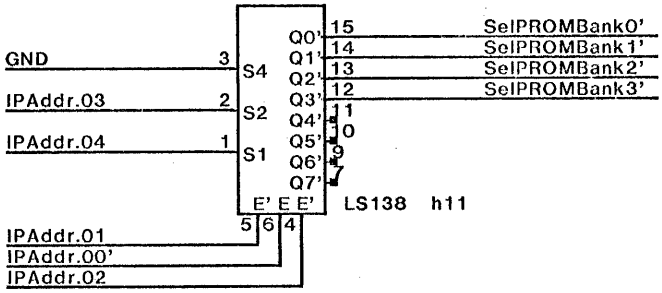


(Read)

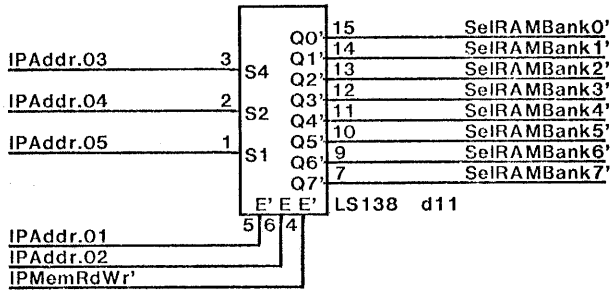
(Write)

Single Register Block
(Bank 3a, registers 8-15, addresses 0E8H - 0EFH)

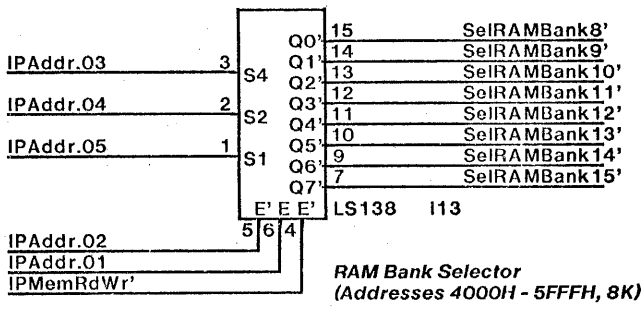
Memory Control



PROM Bank Selector
(Addresses Bank 0: 0 - 7FFH,
Bank 1: 800H - 0FFFH,
Bank 2: 1000H - 17FFH,
Bank 3: 1800H - 1FFFH)

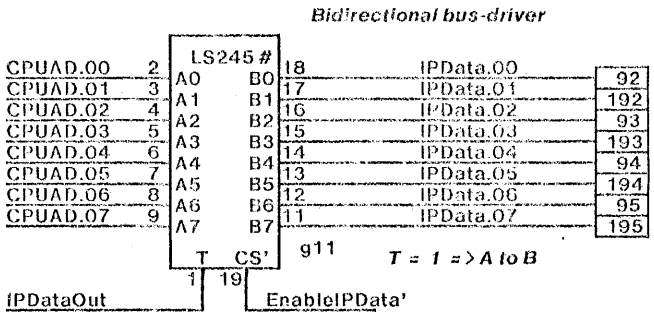


RAM Bank Selector
(Addresses 2000H - 3FFFH, 8K)

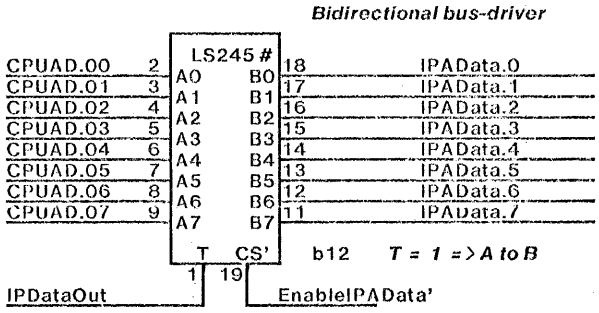


RAM Bank Selector
(Addresses 4000H - 5FFFH, 8K)

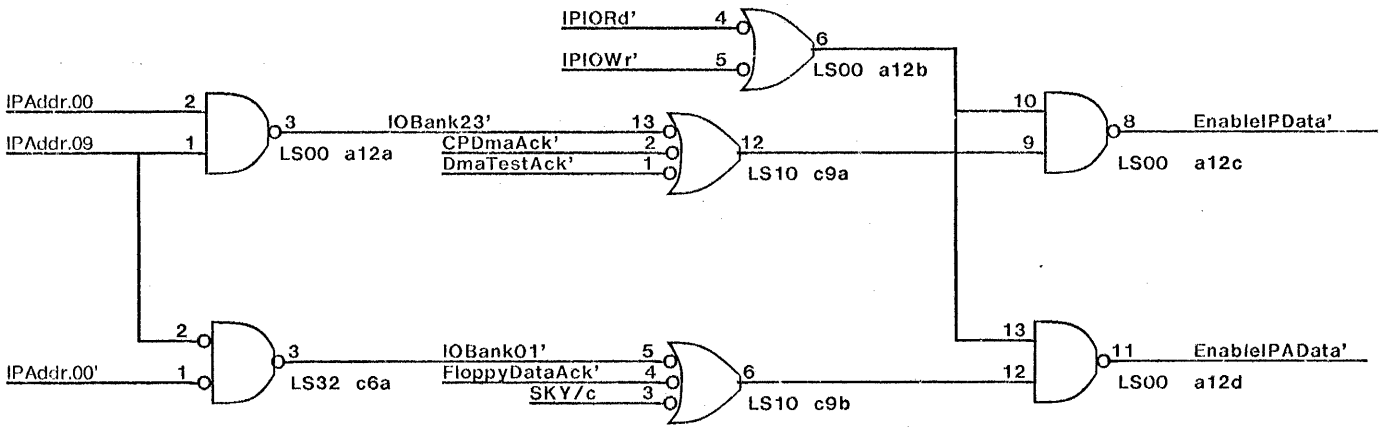
XEROX SDD	Project: Dandelion	I/O Processor I/O Control, memory Control	File: DandIOP05.sil	Designer: Ogus	Rev: E	Date: 10/24/79	Page: 05



I/O
Data Bus



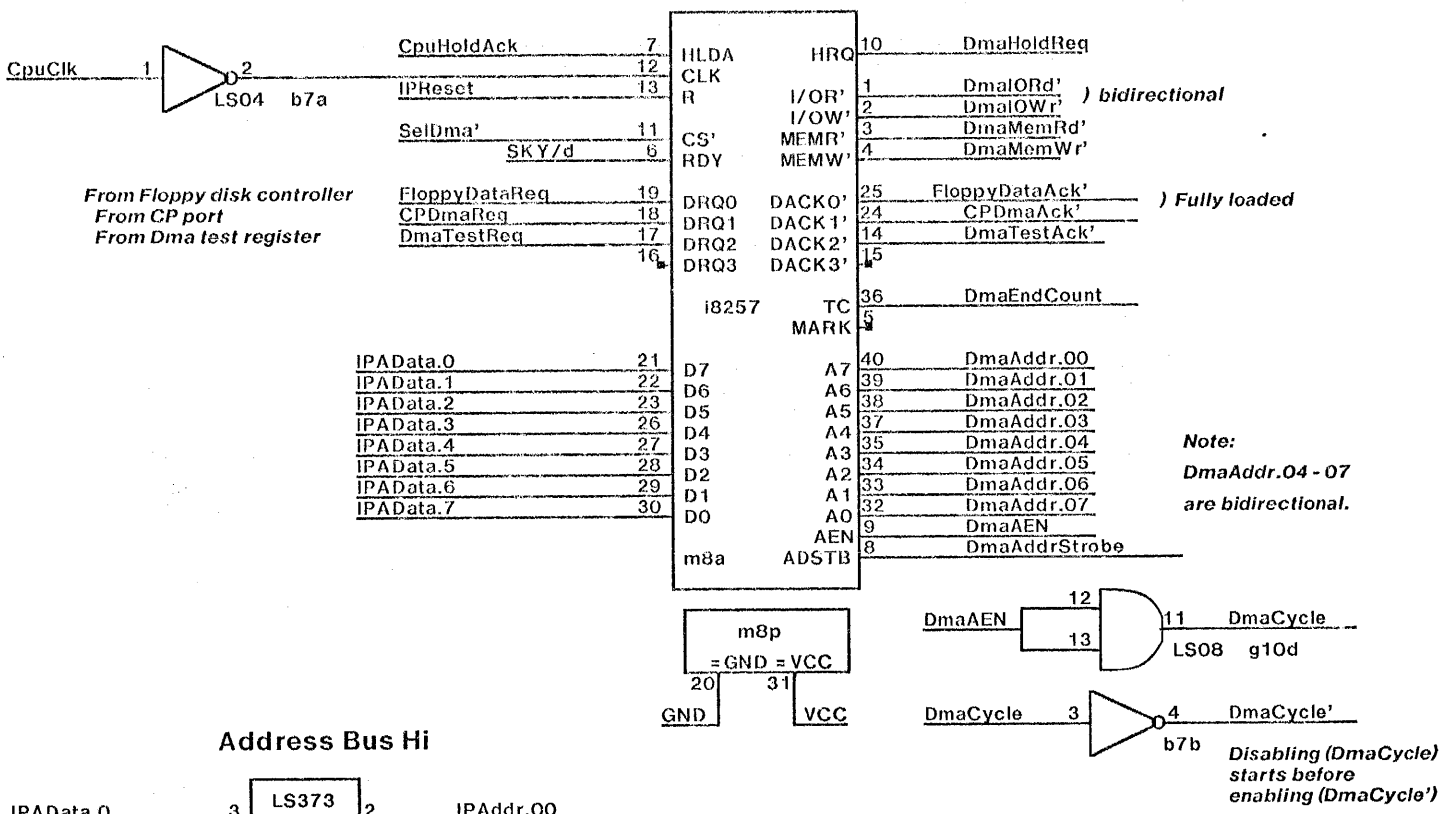
Alternate
I/O
Data Bus



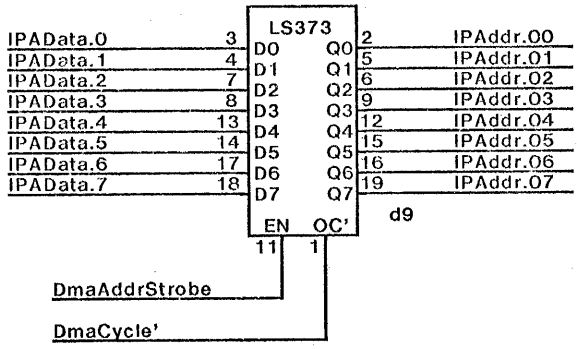
Note: Do not use DMA memory addresses in the I/O Address space.

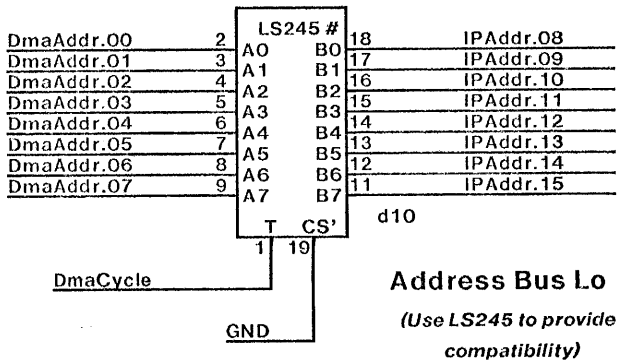
XEROX SDD	Project: Dandelion	I/O Processor I/O Data Bus Control	File: DandIOP06.sil	Designer: Ogus	Rev: E	Date: 10/25/79	Page: 06

DMA controller



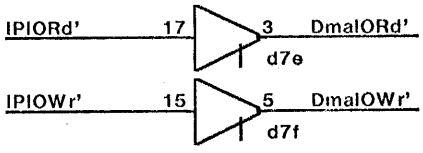
Address Bus Hi

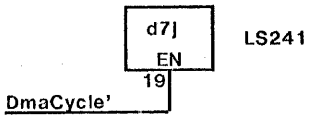




Address Bus Lo

(Use LS245 to provide 8237 compatibility)



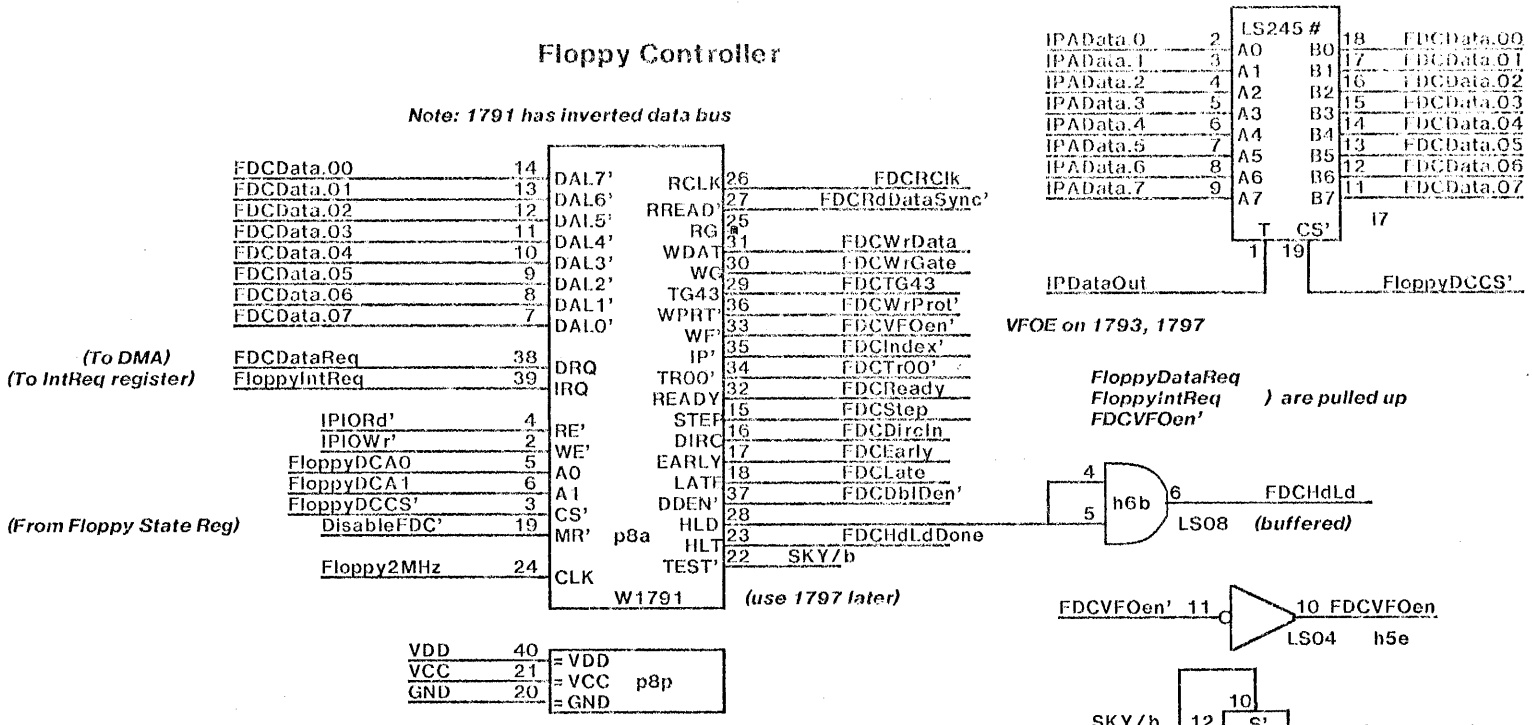


Dma I/O Rd', Wr'
In slave mode

XEROX SDD	Project	I/O Processor	File	Designer	Rev	Date	Page
	Dandelion	DMA Controller	DandIOP07.sil	Ogus	E	10/24/79	07

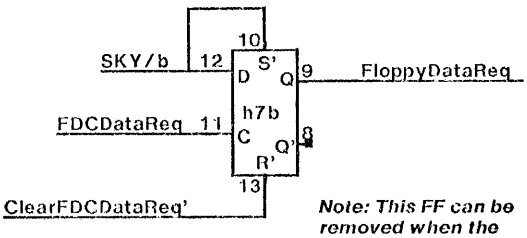
Floppy Controller

Note: 1791 has inverted data bus

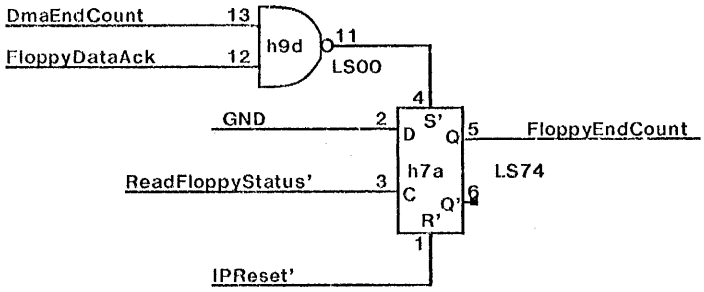


VFOE on 1793, 1797

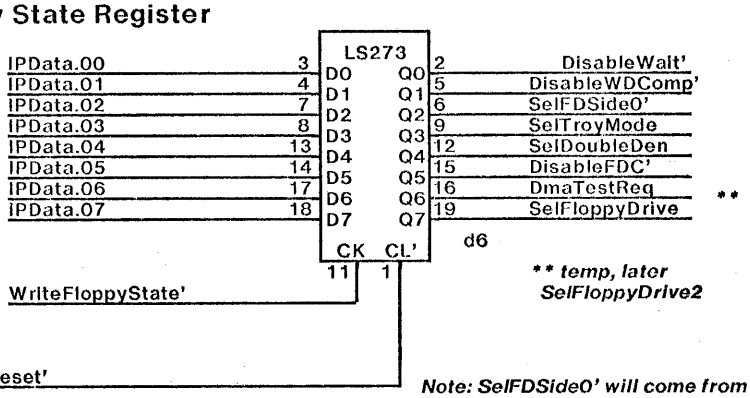
FloppyDataReq
FloppyIntReq) *are pulled up*
FDCVFOen'



Note: This FF can be removed when the 8237 DMA is used



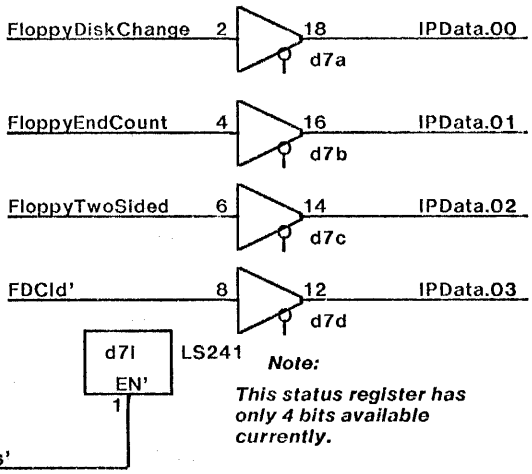
Floppy State Register



*** temp, later SelFloppyDrive2*

Note: SelFDSide0' will come from WD1797
VFOE will come from 1793 WF' output

Floppy Status



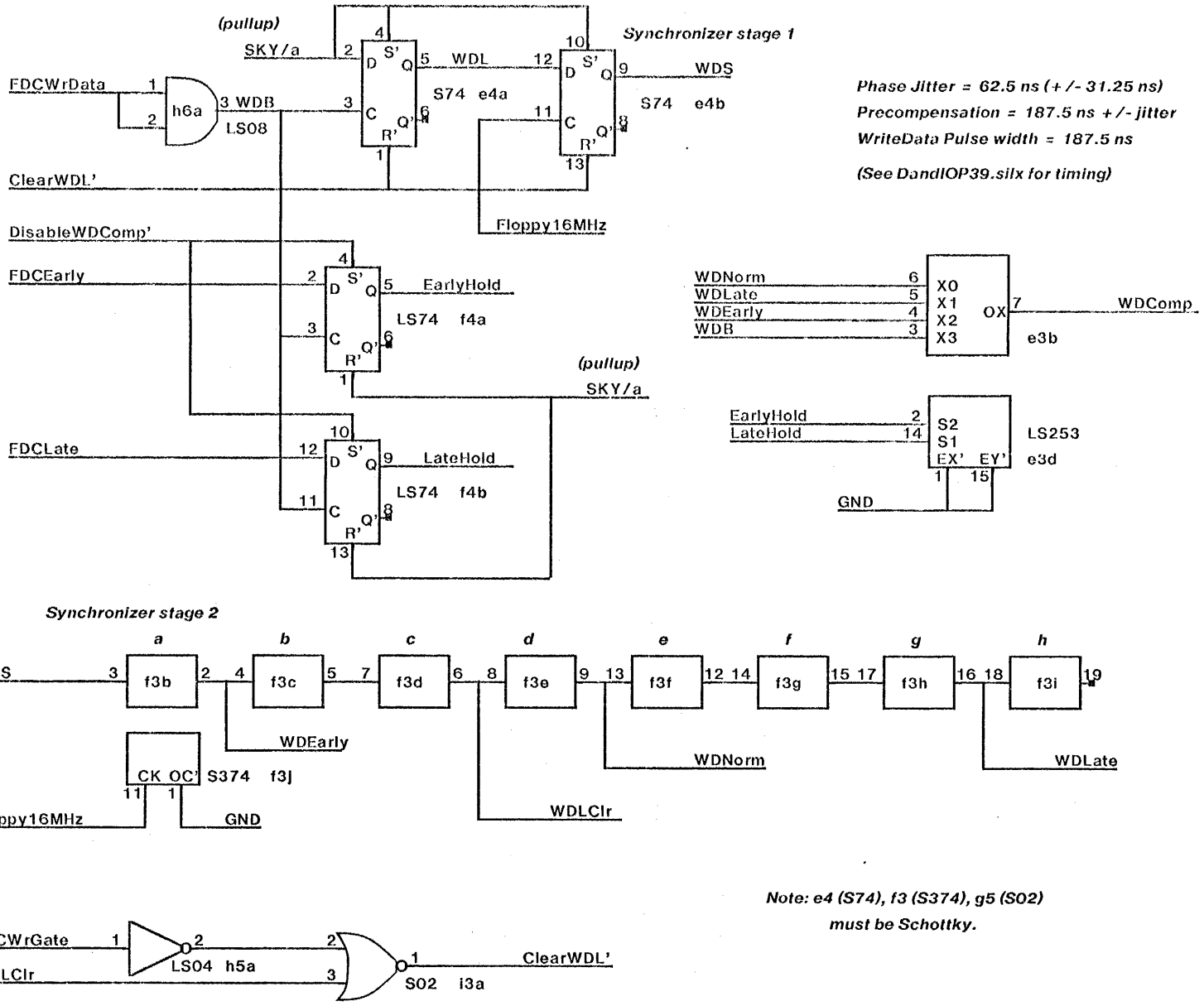
Note:

This status register has only 4 bits available currently.

State register format:

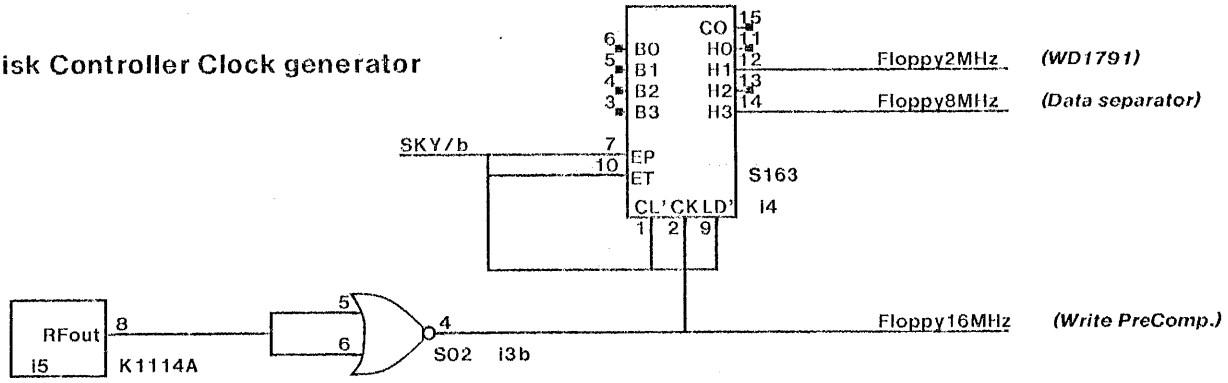
Bit 0	*- Enable Cpu Waits*	*Bit 4*	*- Select Double Density*
Bit 1	*- Enable Write PreComp*	*Bit 5*	*- Enable Floppy Controller*
Bit 2	*- Select Side 1*	*Bit 6*	*- Dma Test Request ***
Bit 3	*- Select Troy mode*	*Bit 7*	*- Enable Floppy Drive*

XEROX SDD	Project	I/O Processor	File	Designer	Rev	Date	Page
	Dandelion	Floppy Controller	DandIOP08.sil	Ogus	E	10/24/79	08



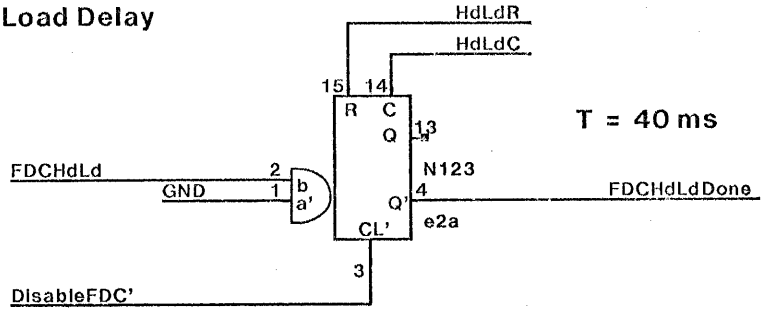
XEROX SDD	Project Dandelion	I/O Processor Floppy Controller Write Comp.	File DandIOP09.sil	Designer Ogus	Rev E	Date 10/24/79	Page 09

Floppy Disk Controller Clock generator

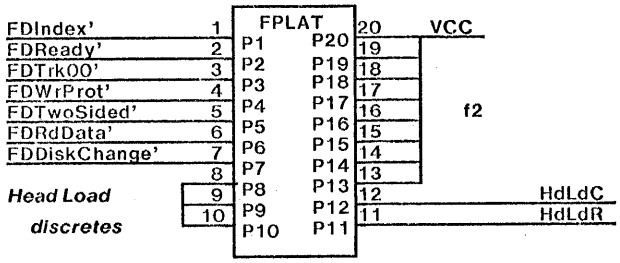


Motorola Clock 16.000 MHz

Head Load Delay



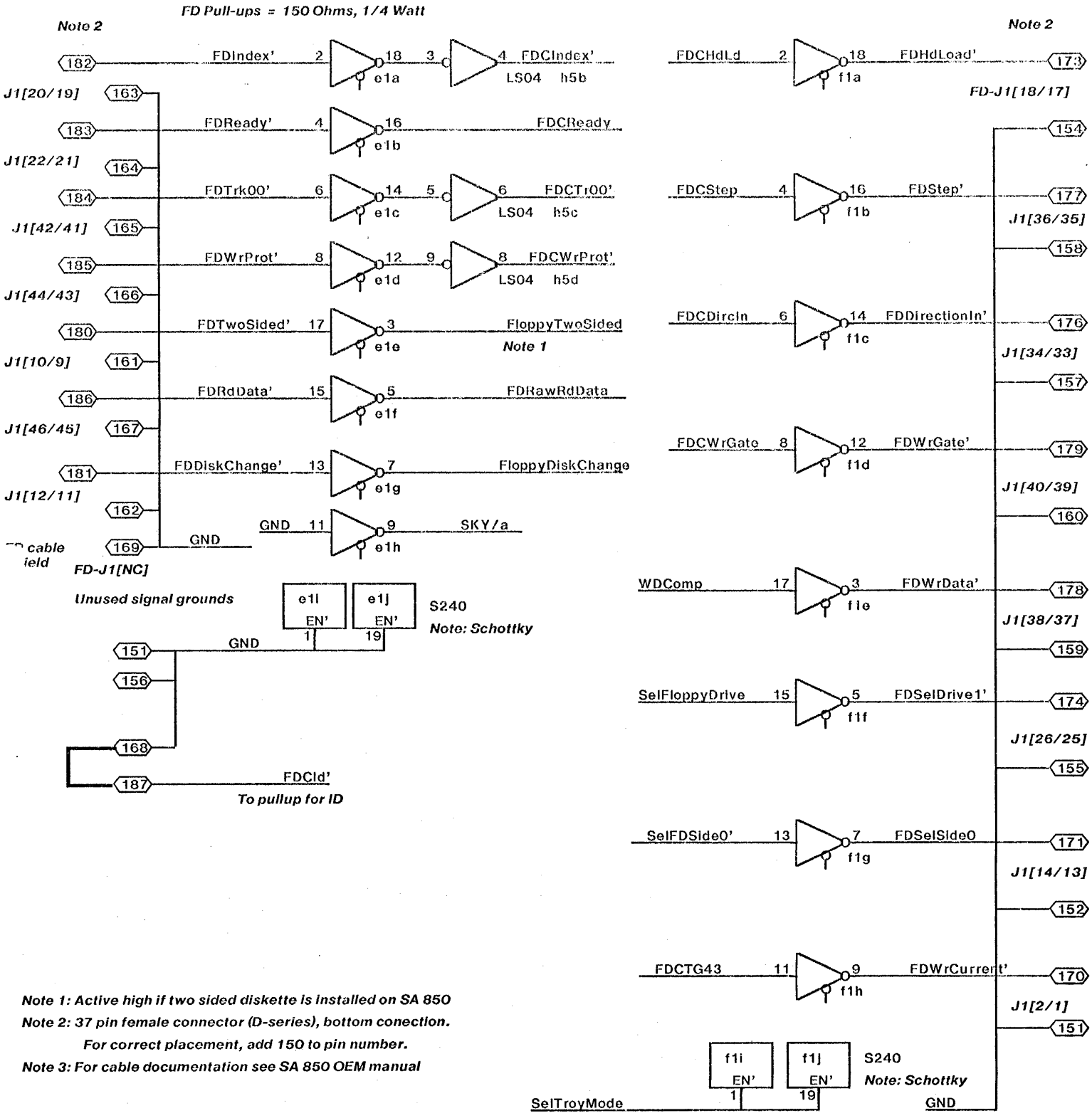
Pullups, 150, .25W



Miscellaneous Floppy Controller discrete components
(20 pin platform)

(Note: Still need to have FDId' pulled up)

XEROX SDD	Project Dandelion	I/O Processor Floppy Controller Miscellaneous	File DandIOP10.sil	Designer Ogus	Rev E	Date 10/24/79	Page 10



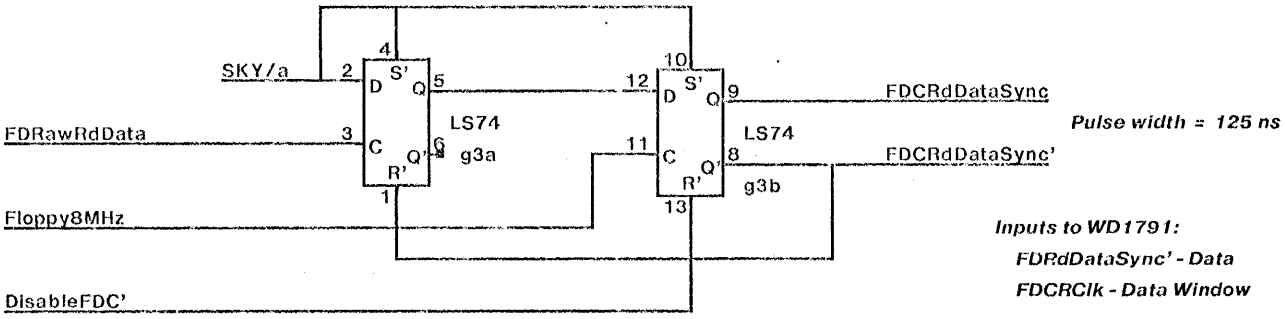
Note 1: Active high if two sided diskette is installed on SA 850

Note 2: 37 pin female connector (D-series), bottom conection.
For correct placement, add 150 to pin number.

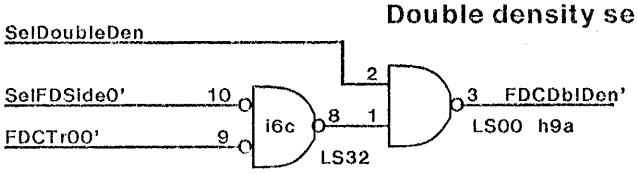
Note 3: For cable documentation see SA 850 OEM manual

XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dandelion	I/O Processor Floppy Disk Receivers/Drivers	DandIOP11.sil	Ogus	E	10/24/79	11

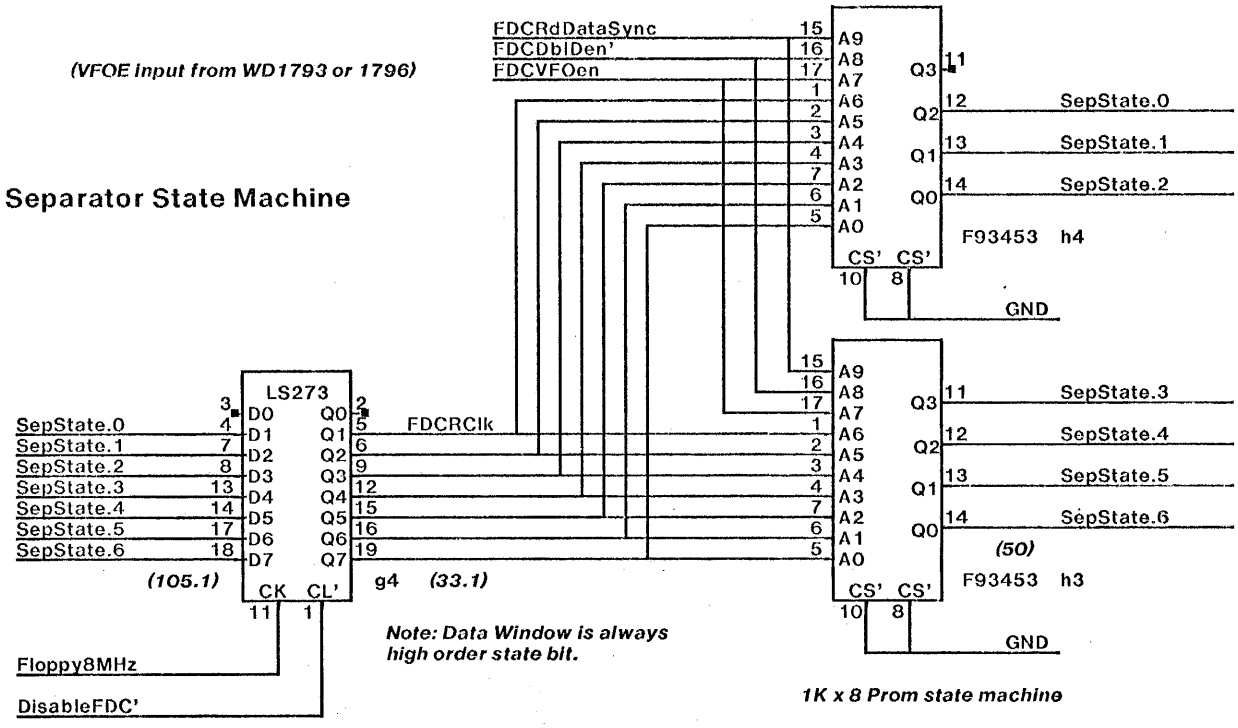
Raw Read Data synchronizer and pulse shaper



Double density selection



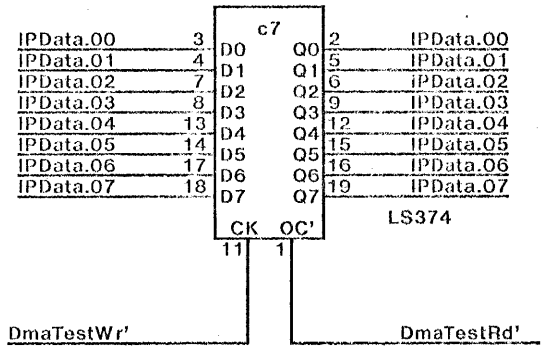
Separator State Machine

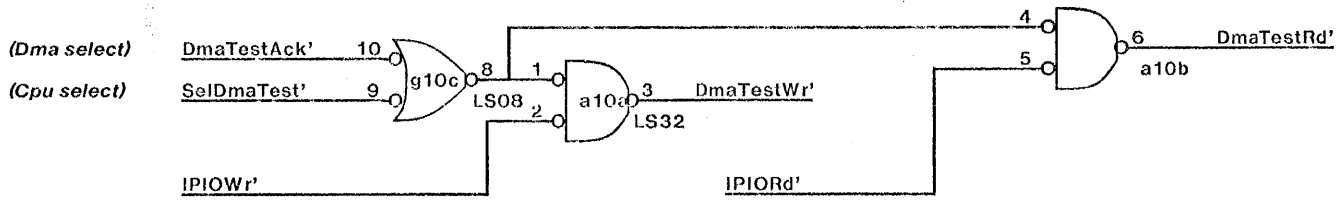


XEROX SDD	Project Dandelion	I/O Processor Floppy Data Separator	File DandIOP12.sil	Designer Ogus	Rev E	Date 10/24/79	Page 12

DMA Test Register

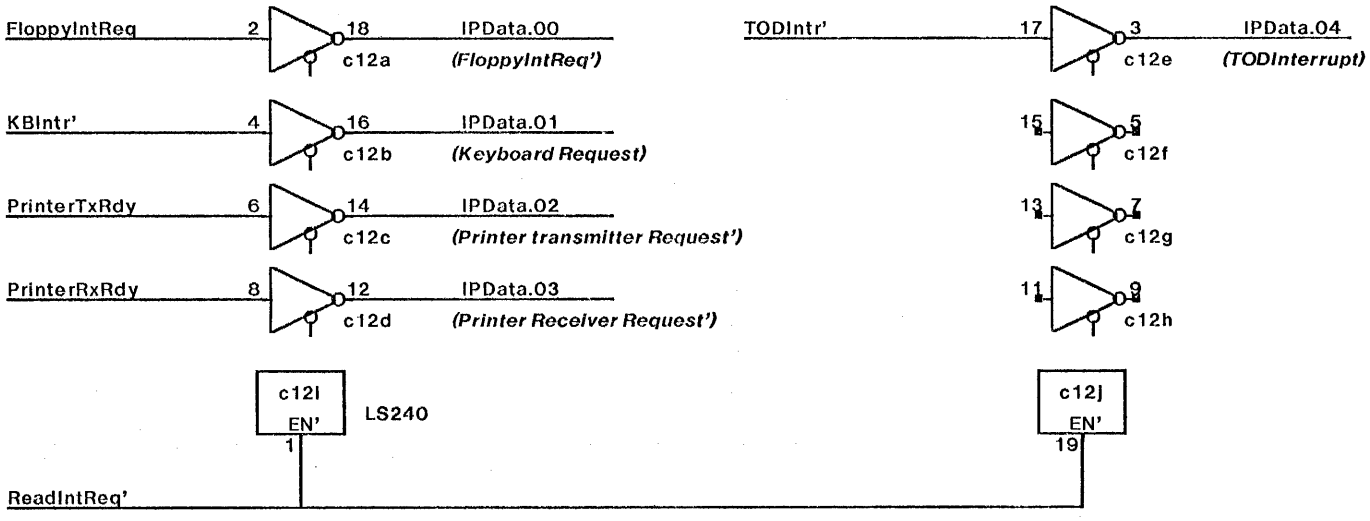
For testing Dma controller independently of Floppy disk.
Can be removed later.





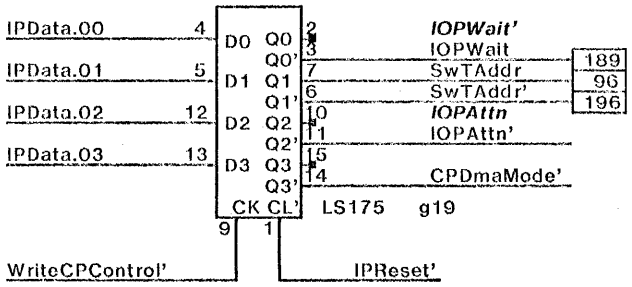
XEROX SDD	Project: Dandelion	I/O Processor DMA Test	File: DandIOP13.sil	Designer: Ogus	Rev: E	Date: 10/24/79	Page: 13

Interrupt Request Register



This register contains the Interrupt requests of various devices.

Central processor control
CP port control

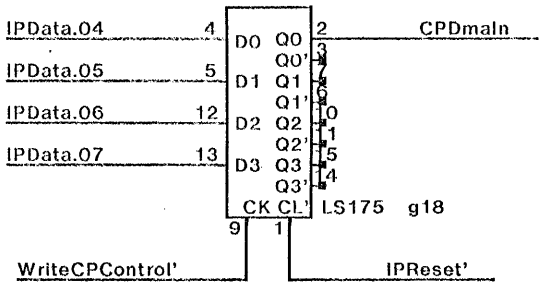


(IOPWait should be true after booting)

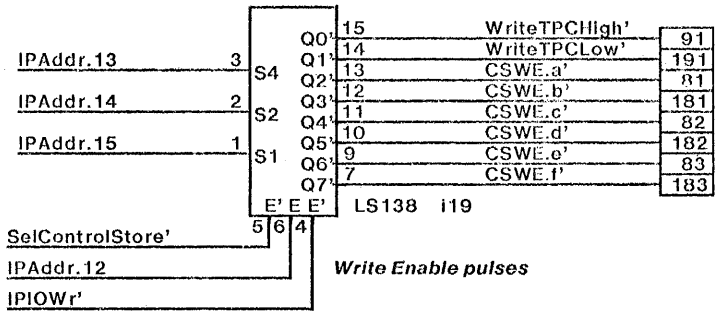
Data:

- *Bit 0 - Enable CP (remove Wait)*
- *Bit 1 - Switch TPC address from NIAX*
- *Bit 2 - Set CP Attention*
- *Bit 3 - Set Dma Mode for CP port*
- *Bit 4 - Set Dma Mode for CPport as input/output'*

Normal state of register is 1000 x xxx

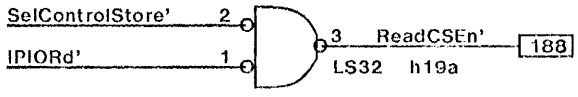


Control Store handling



Write Enable pulses

(Write)



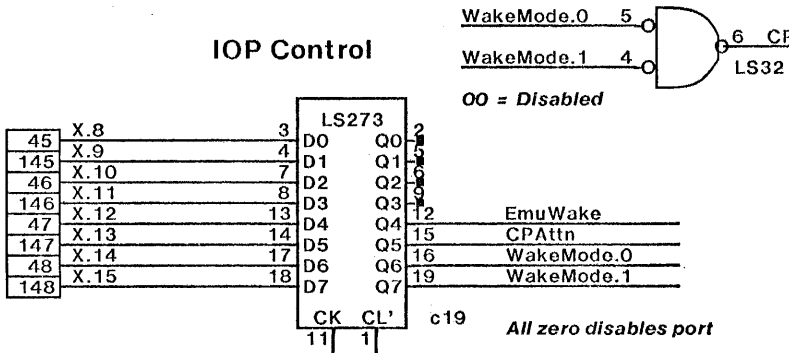
(Read)

Note: All 16 addresses will respond, use 8-15.

(Bank 2a, registers 8-15, addresses 0C8 - 0CFH)

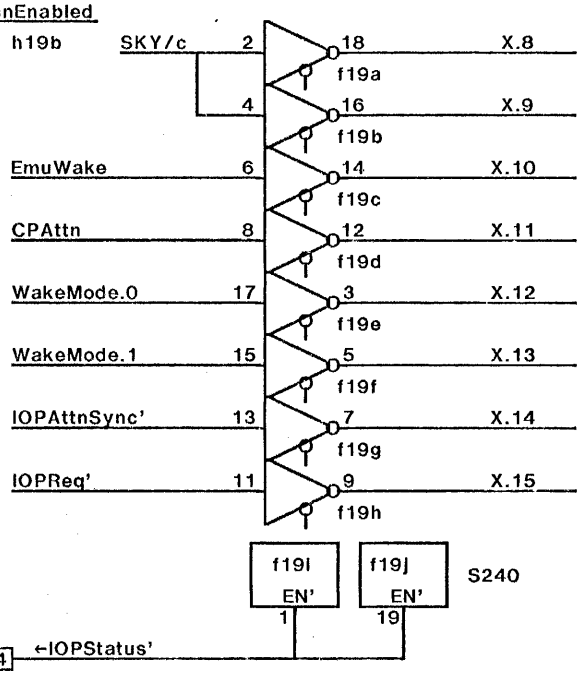
Central Processor registers

IOP Control



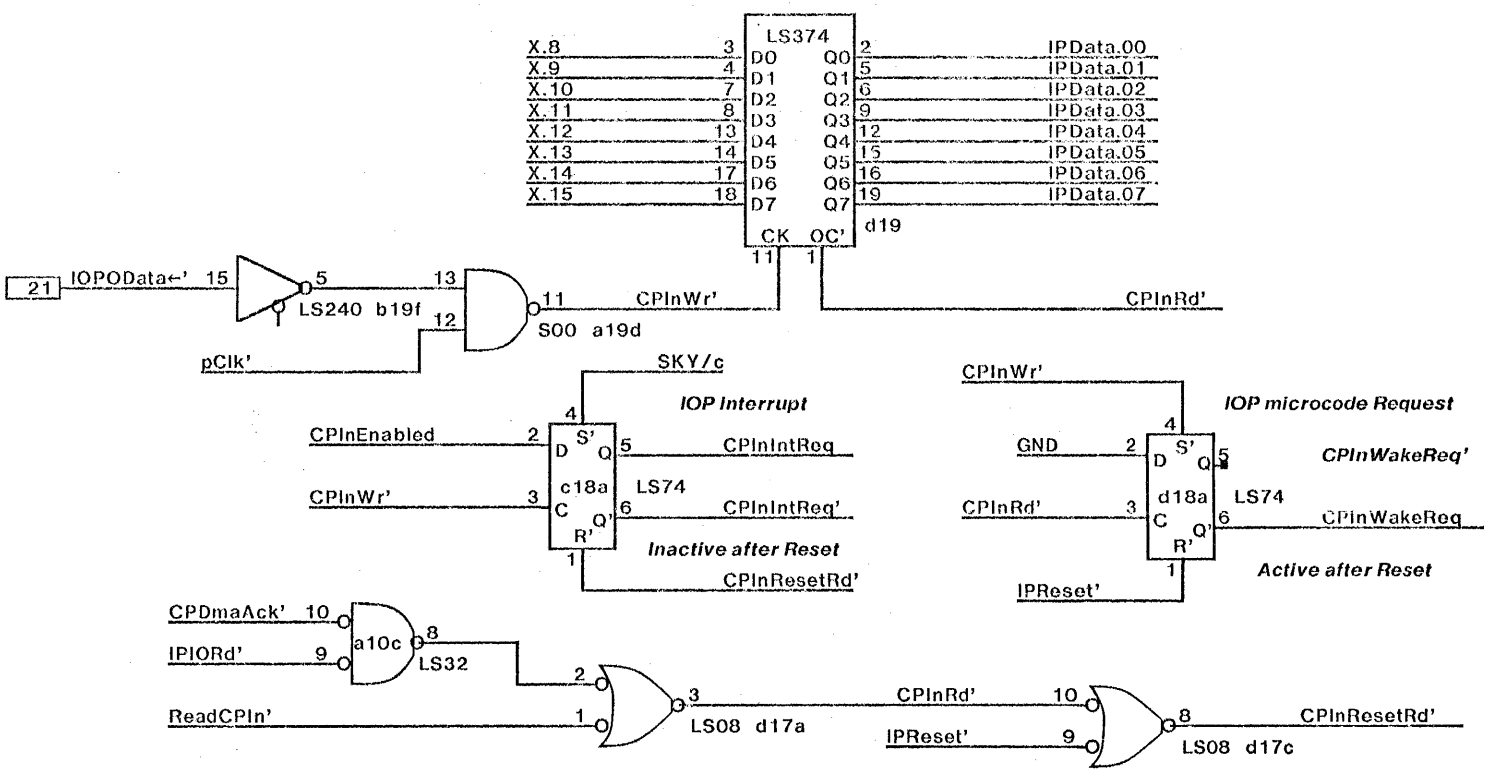
WakeMode:
00 = Disabled
01 = Input Mode
10 = Output Mode
11 = Always Wake up

IOP Status

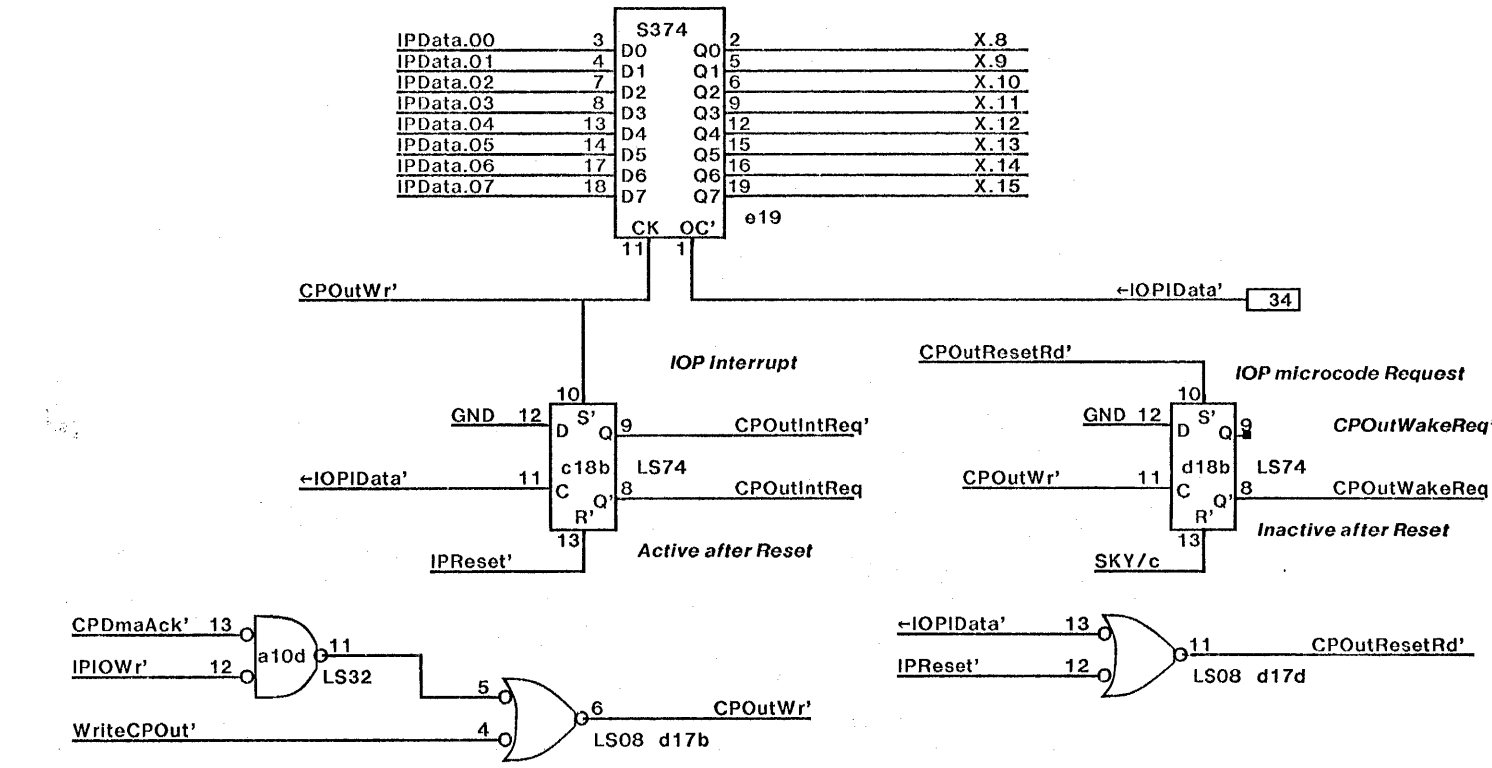


XEROX SDD	Project: Dandelion	I/O Processor CP Control and Control Store	File: DandIOP15.sil	Designer: Ogus	Rev: E	Date: 10/24/79	Page: 15

CPIn

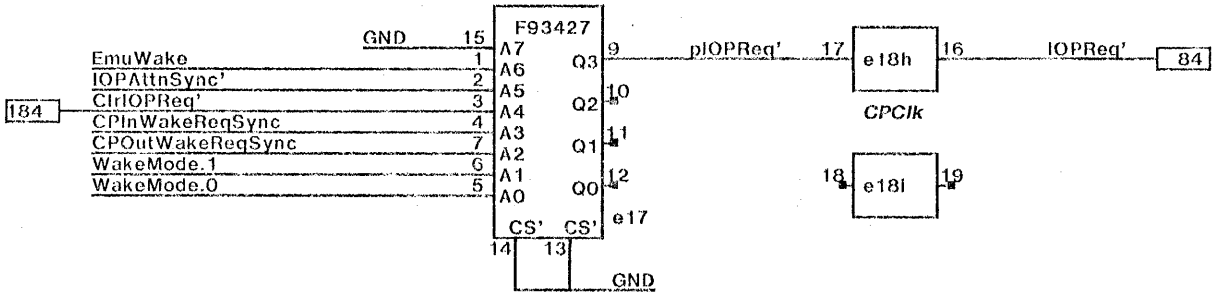


CPOut

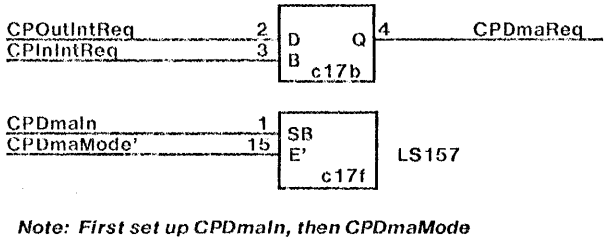


XEPOX SDD	Project Dandelion	I/O Processor CP-IOP port	File DandIOP16.sil	Designer Ogus	Rev E	Date 10/25/79	Page 16

IOPReq

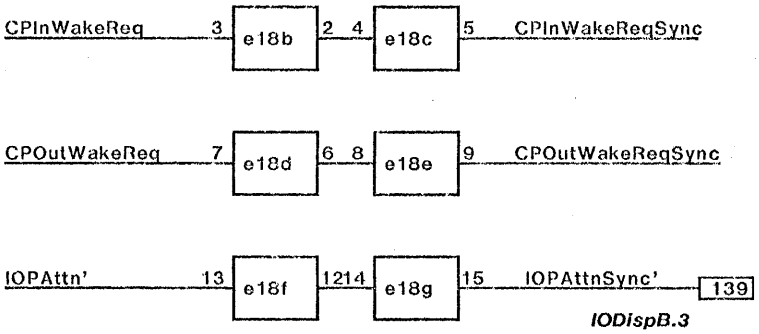


CP port Dma Request

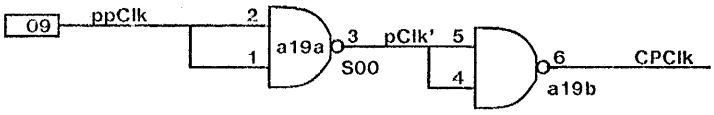


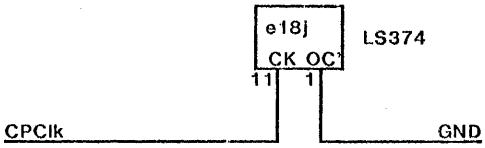
Note: First set up CPDmaIn, then CPDmaMode

Synchronizers

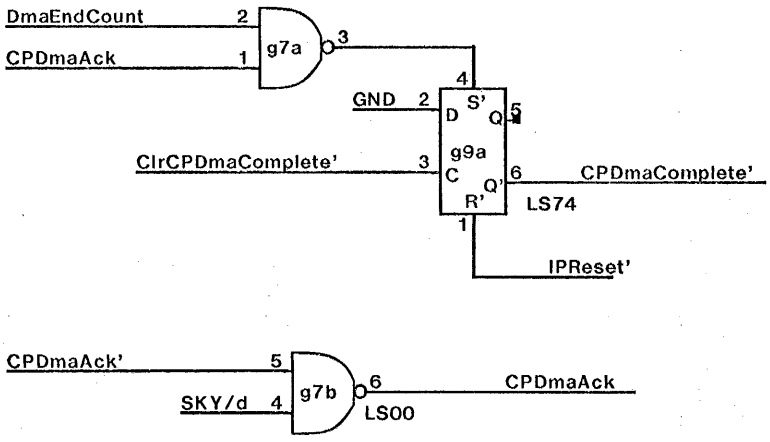


CP Clock

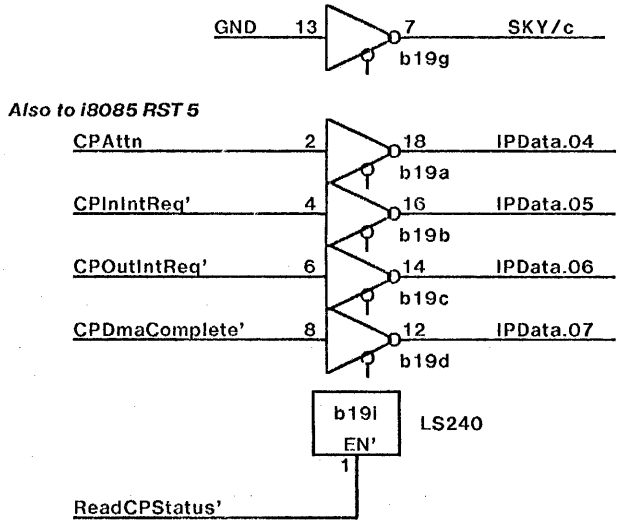




CP port Dma Complete

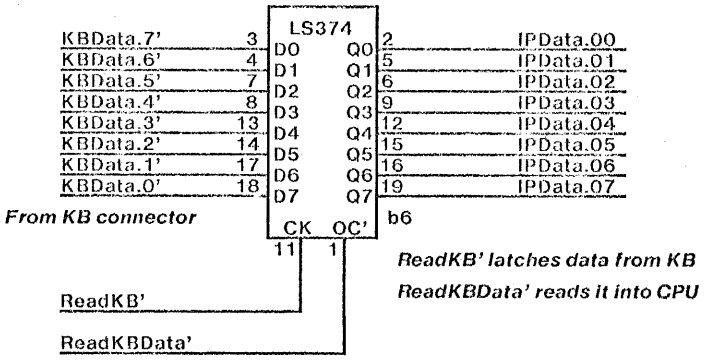


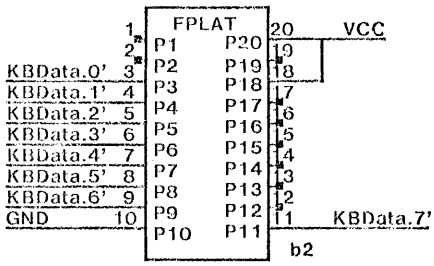
CP port status

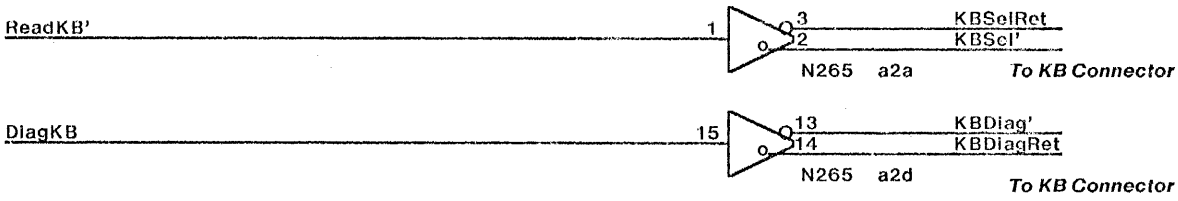


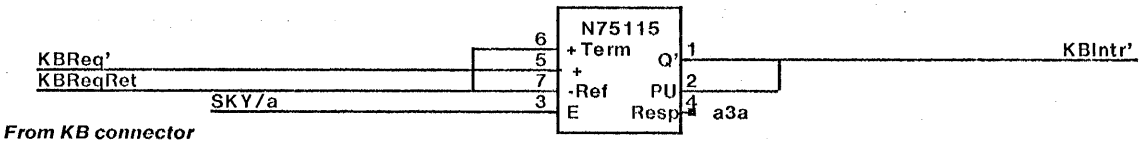
XEPOX SDD	Project: Dandelion	I/O Processor CP-IOP port - 2	File: DandIOP17.sil	Designer: Ogus	Rev: E	Date: 10/24/79	Page: 17

Keyboard Data





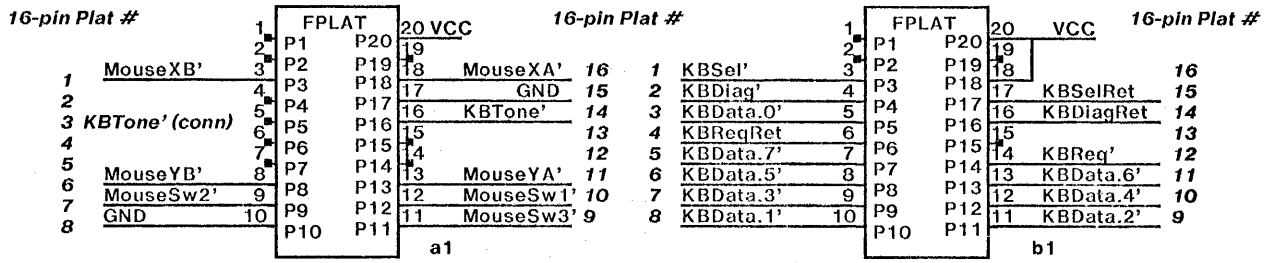




Keyboard cable connector

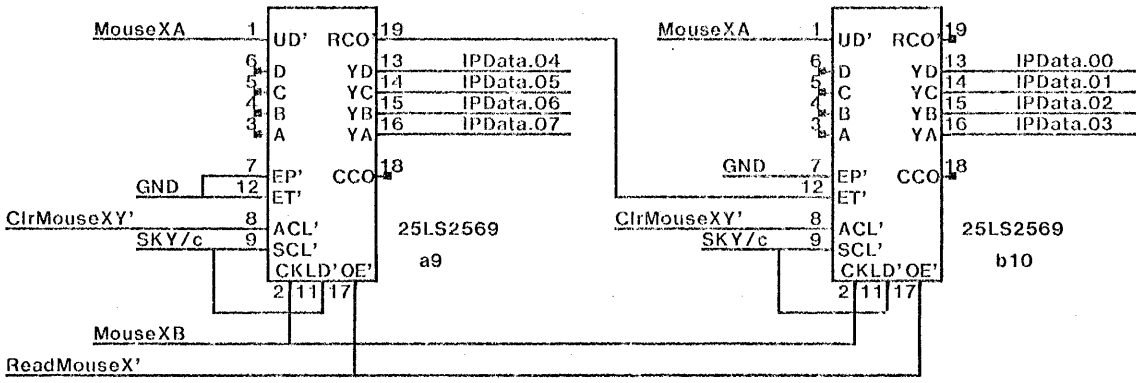
(2 16-pin DIP connectors)

(23 signals, +5V, GND)

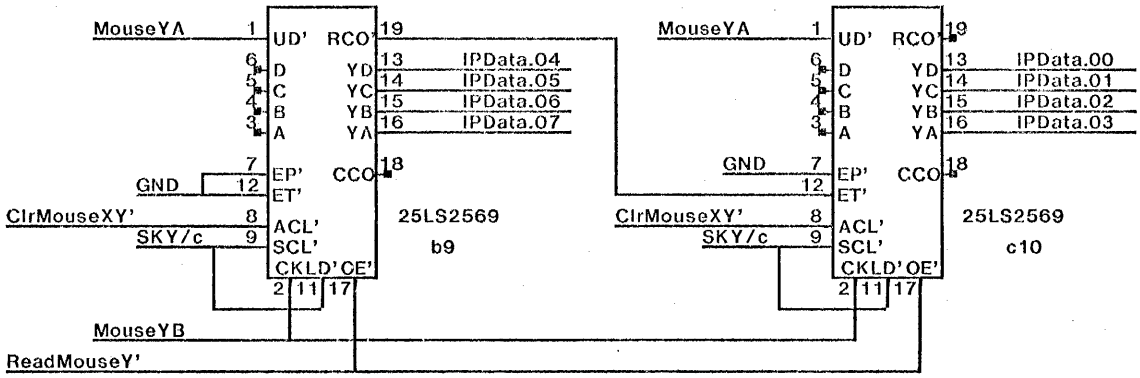


XEPOX SDD	Project Dandelion	I/O Processor Keyboard Interface	File DandIOP18.sil	Designer Ogus	Rev E	Date 10/24/79	Page 18

X-coordinate

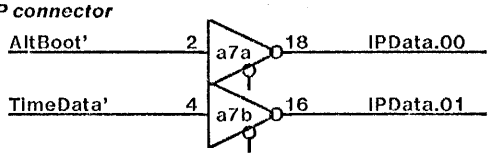


Y-coordinate

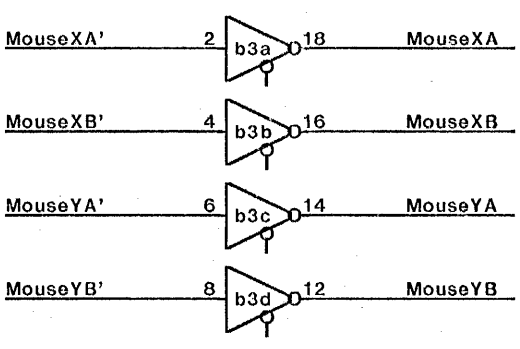


Miscellaneous Input 1

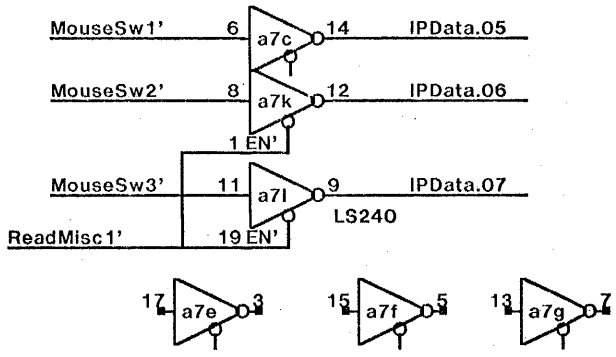
From MP connector



From KB connector

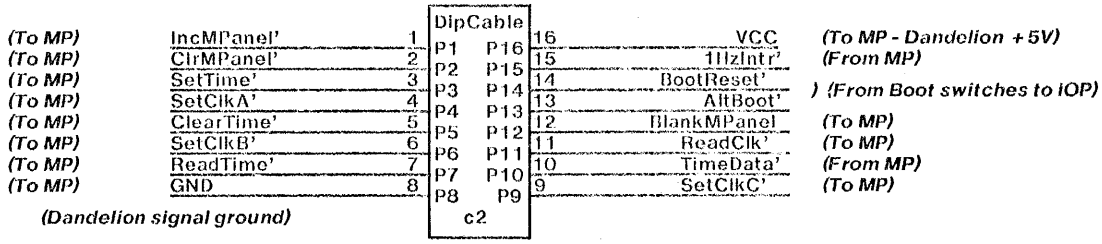


From KB connector

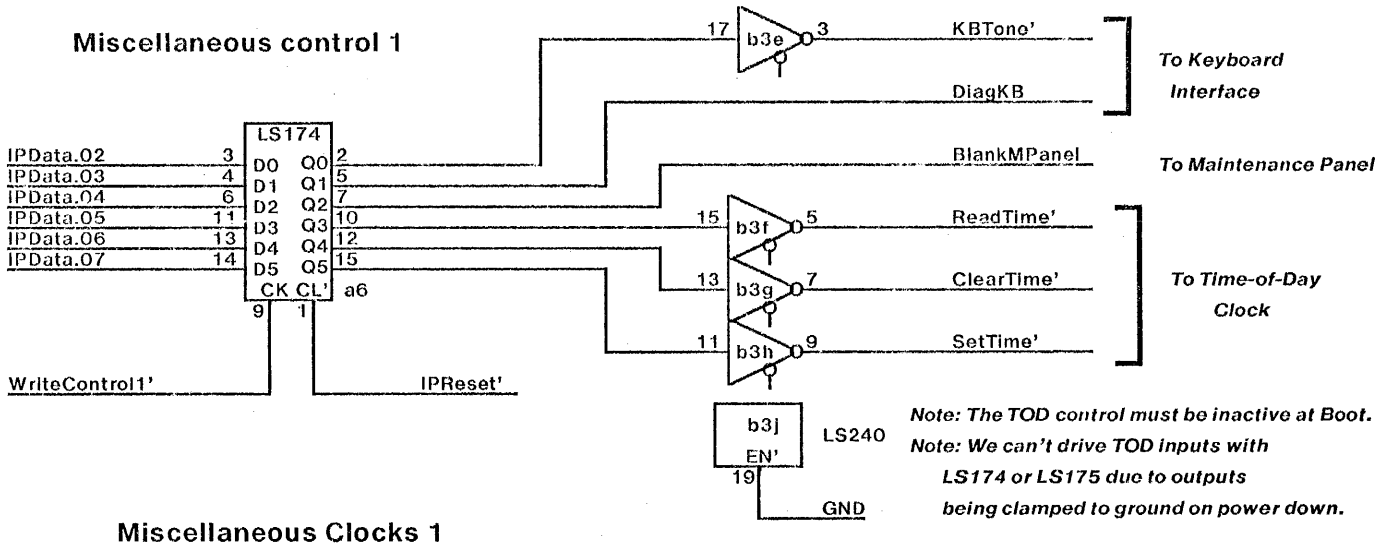


XEPOX SDD	Project Dandelion	I/O Processor Mouse interface	File DandIOP19.sil	Designer Ogus	Rev E	Date 10/24/79	Page 19

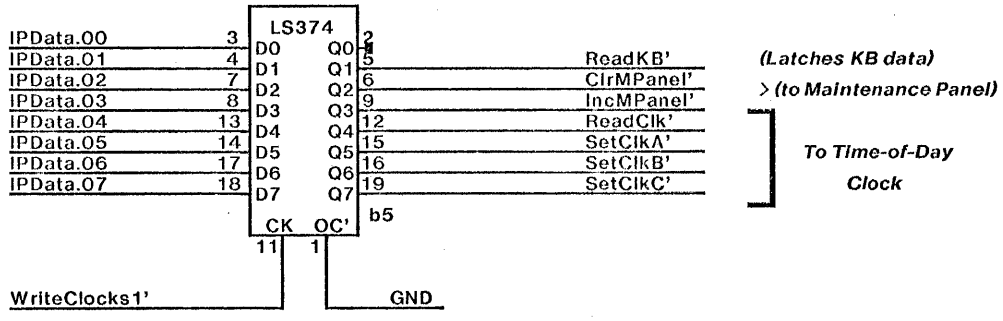
Cable connection to Maintenance panel



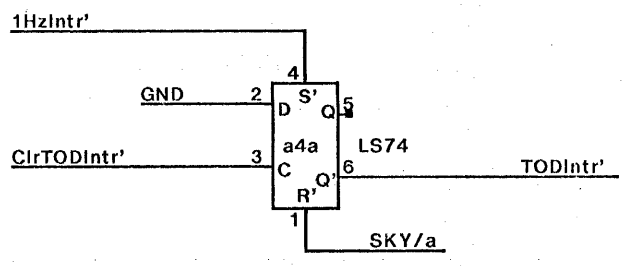
Miscellaneous control 1



Miscellaneous Clocks 1



Time-of-Day 1 second interrupt



Procedure to read time:

- *Wait for TODIntr to be set*
- *When set, clear and wait for it to be set again*
- *read time*

(maximum delay = 2 seconds)

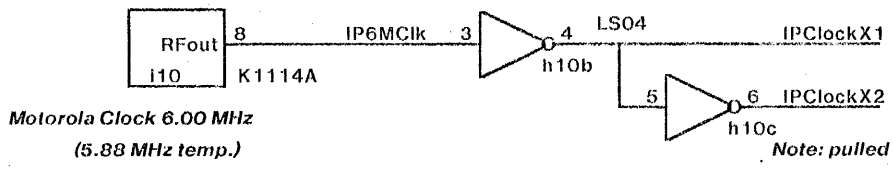
Alternative:

- *clear TODIntr (if being set will not be cleared)*
- *wait until set*
- *read time*

(maximum delay = 1 second)

XEPOX SDD	Project Dandelion	I/O Processor TOD/MP interface, misc. reg.	File DandIOP20.sil	Designer Ogus	Rev E	Date 10/24/79	Page 20

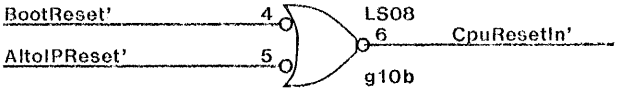
IOP CPU Clock generator

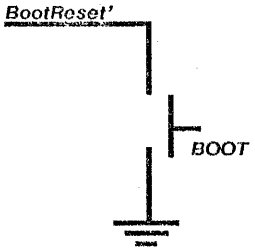


Motorola Clock 6.00 MHz
(5.88 MHz temp.)

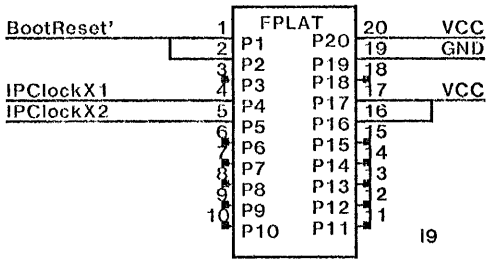
Note: pulled up

CPU boot





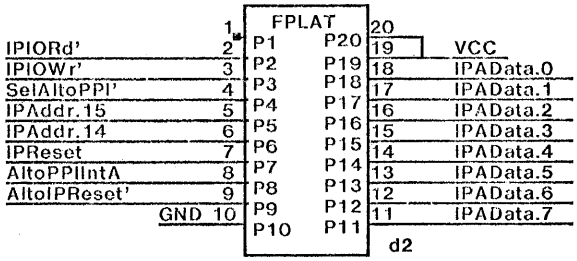
From MP connector



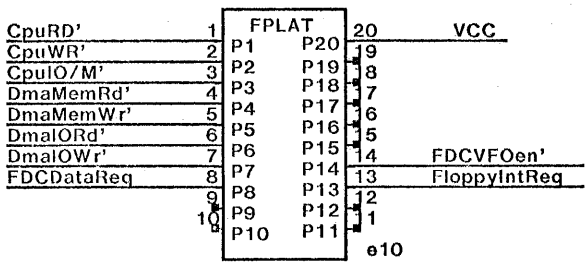
Miscellaneous discrete components
(16 pin platform)

Dip Cable to Alto-IOP interface

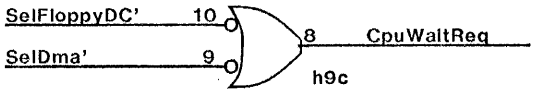
(18 pin platform or DIP connector)



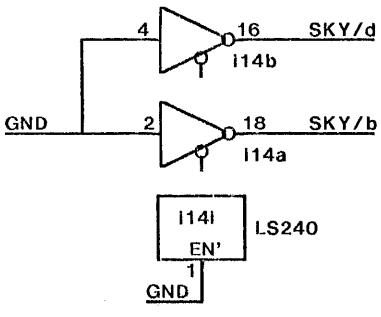
To i8085 RST 6

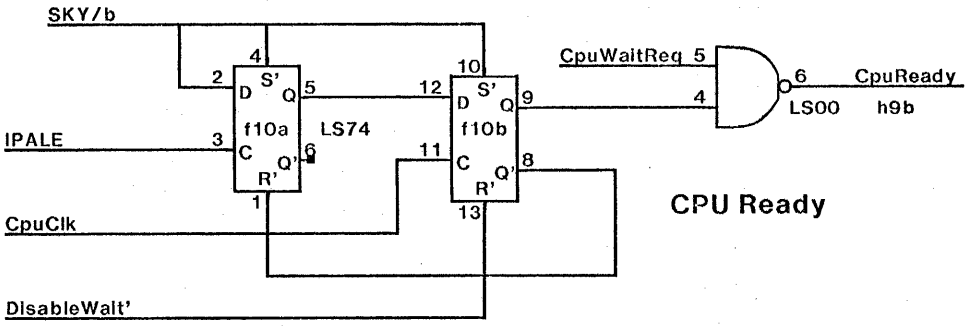


10K pull-up resistors
(16 pin package)



Pullups

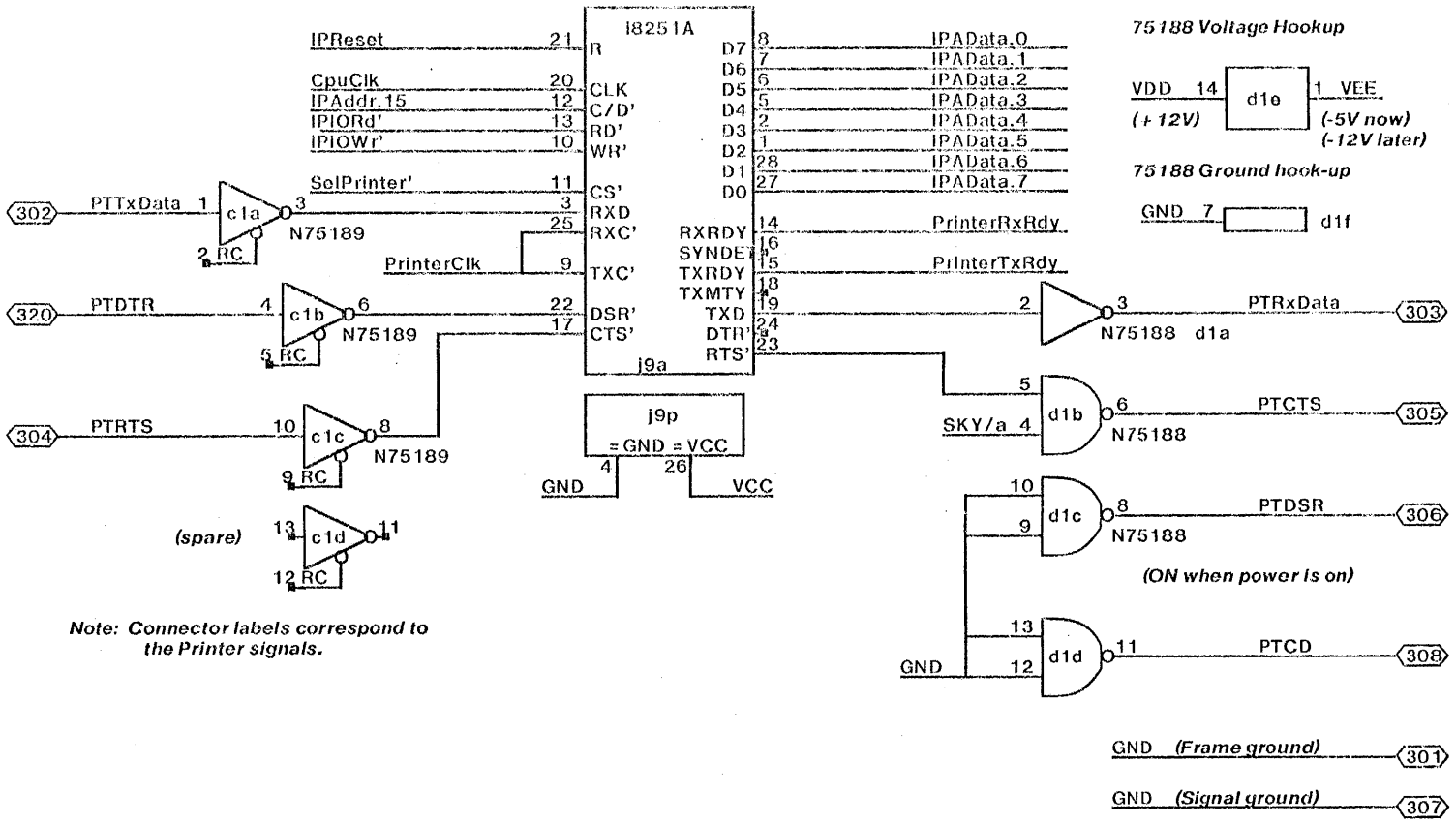




CPU Ready

XEROX SDD	Project: Dandelion	I/O Processor Miscellaneous CPU control	File: DandIOP21.sil	Designer: Ogus	Rev: E	Date: 10/24/79	Page: 21

Printer UART

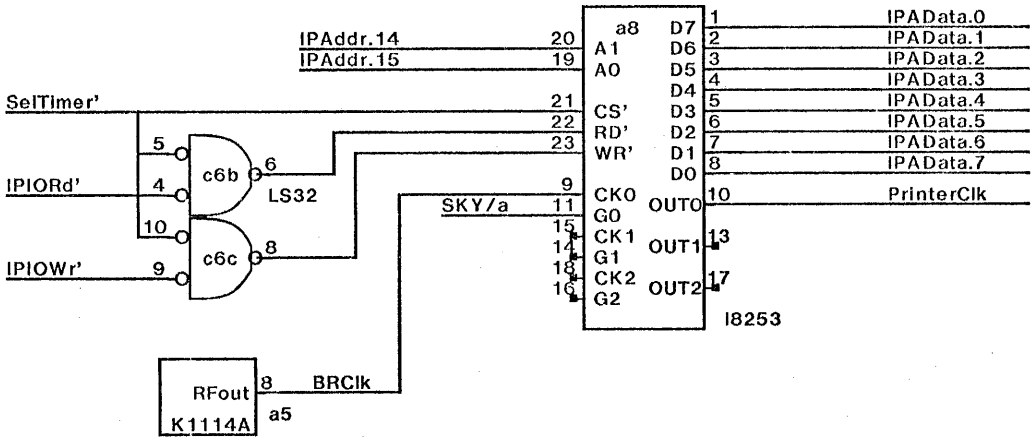


Note: Connector labels correspond to the Printer signals.

Note: Due to a design shortcoming the RD' and WR' lines of the 8253-5 must be externally qualified.

25 pin female connector located on top edge of board. Add 300 to pin number for proper placement.

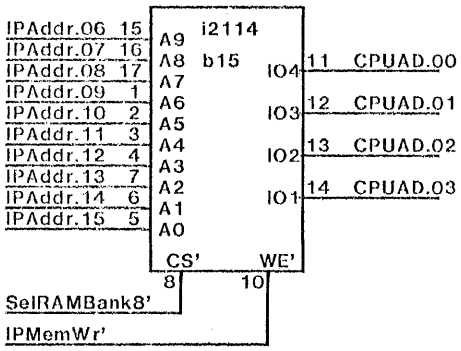
Baud-rate generator

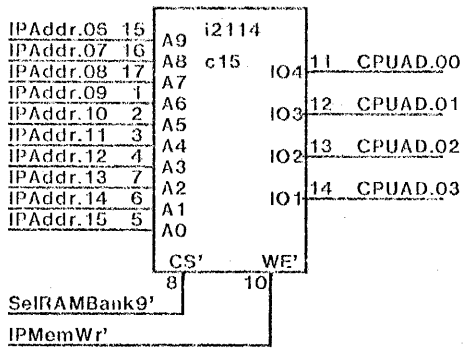


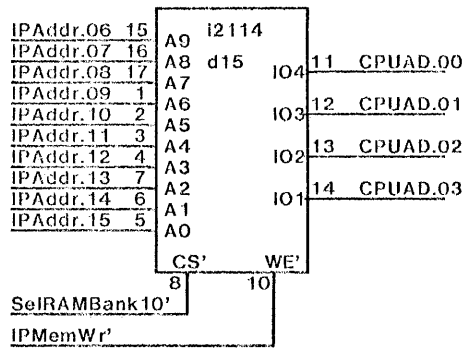
Baud-rate oscillator (1.8432 MHz)

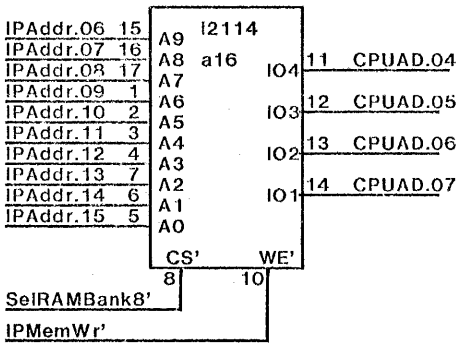
XEROX SDD	Project: Dandelion	I/O Processor Diablo Priner Interface	File: DandIOP22.sil	Designer: Ogus	Rev: E	Date: 10/24/79	Page: 22

RAM - Banks 8 - 11

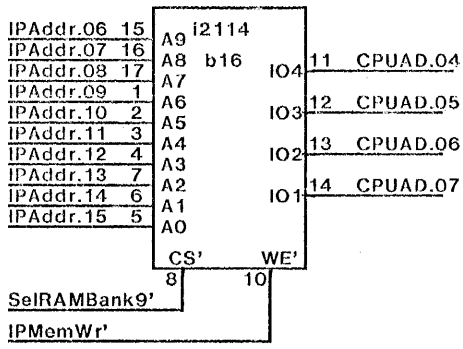




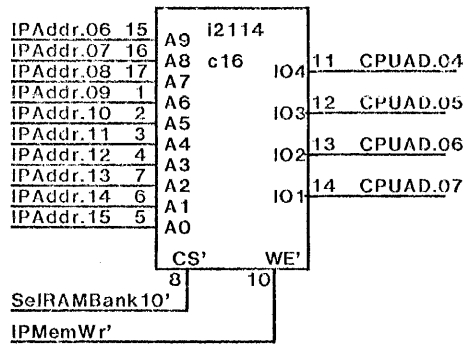




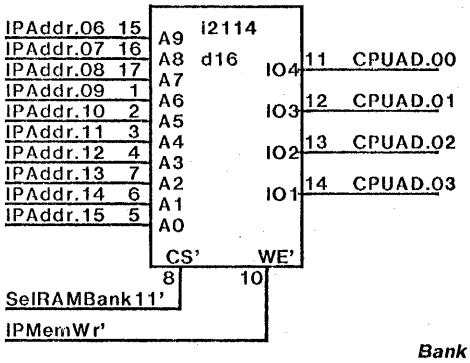
Bank 8

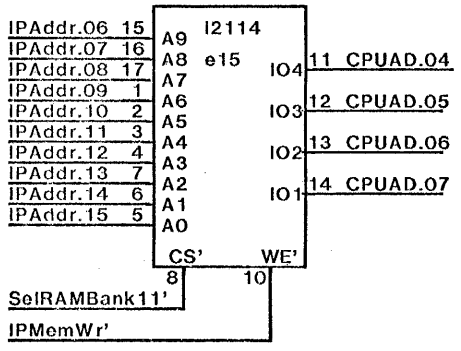


Bank 9



Bank 10

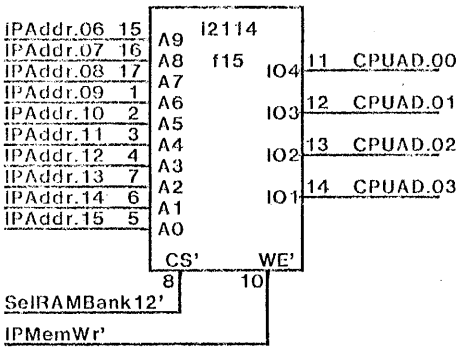


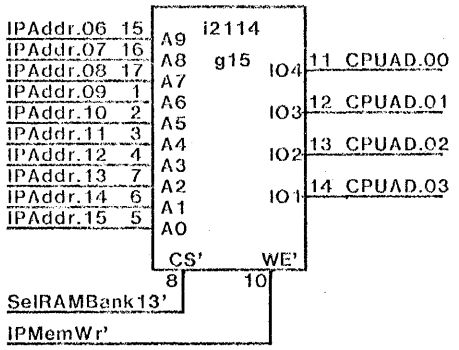


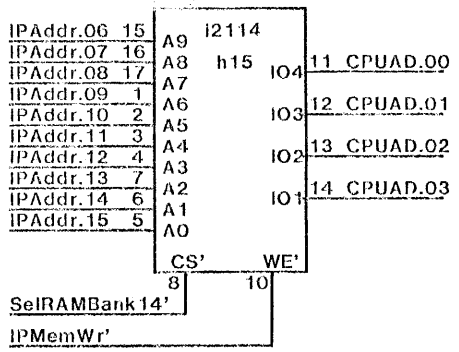
Bank 11

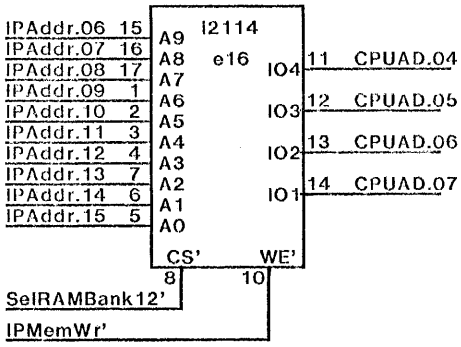
XEROX SDD	Project: Dand/IOP	I/O Processor 4K RAM Memory-Banks 8-11	File: DandIOP23.sil	Designer: Ogus	Rev: E	Date: 10/24/79	Page: 23

RAM - Banks 12 - 15

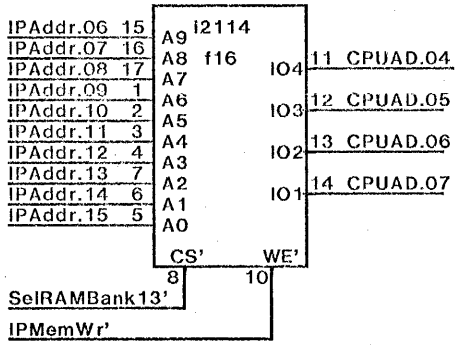




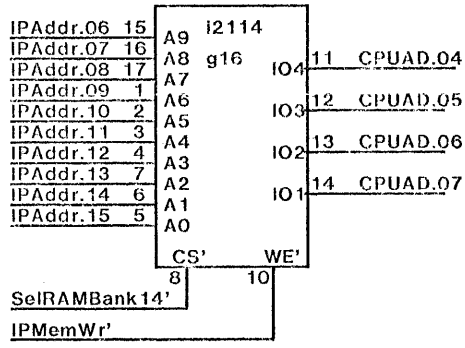




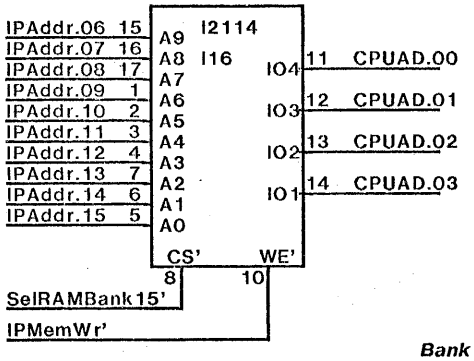
Bank 12

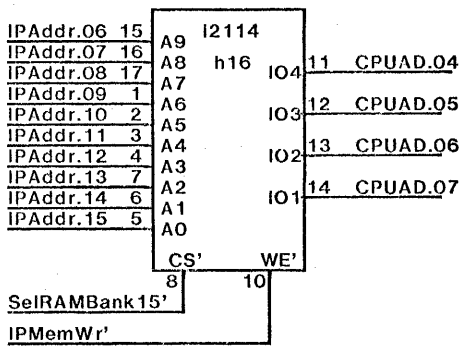


Bank 13



Bank 14

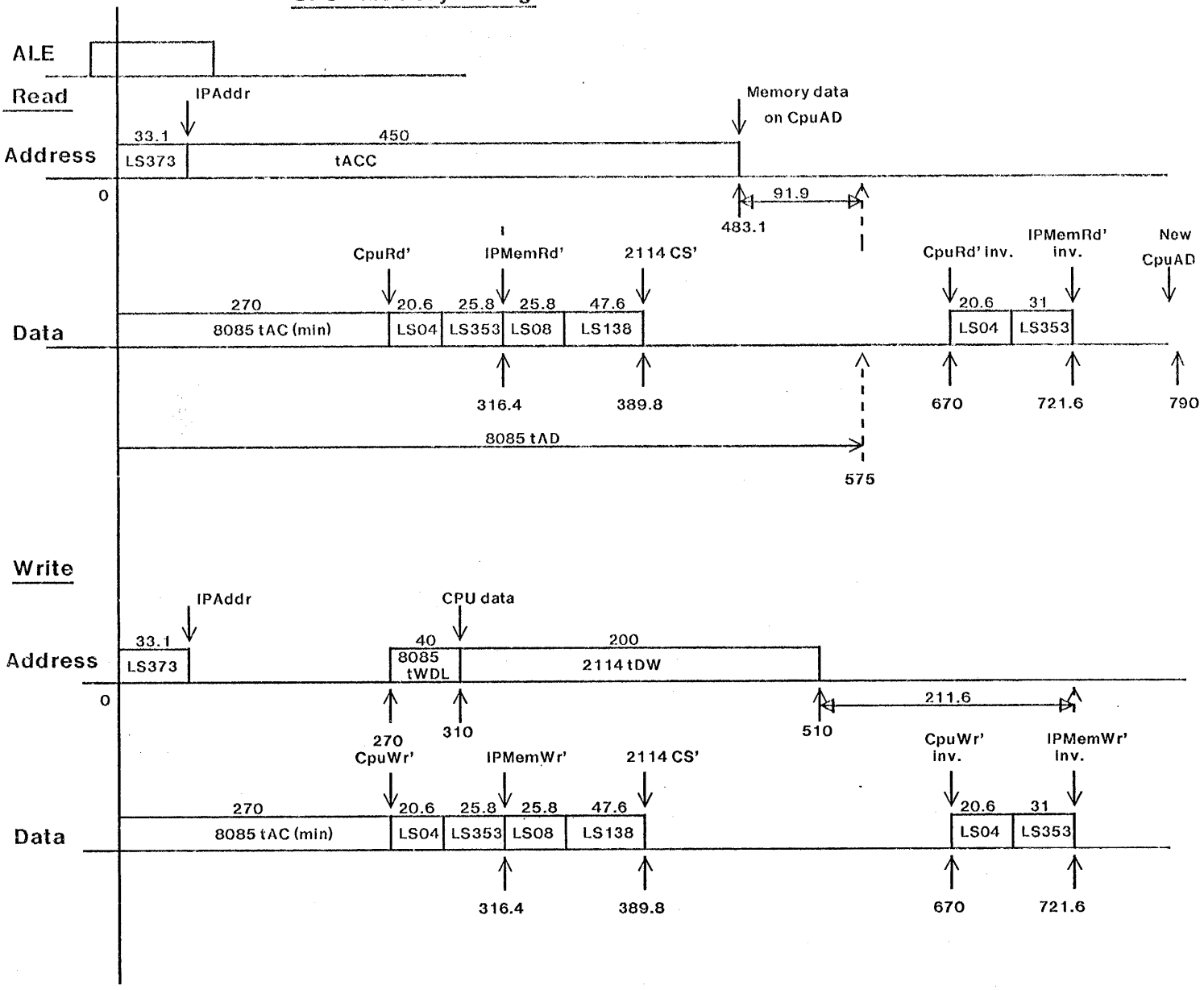


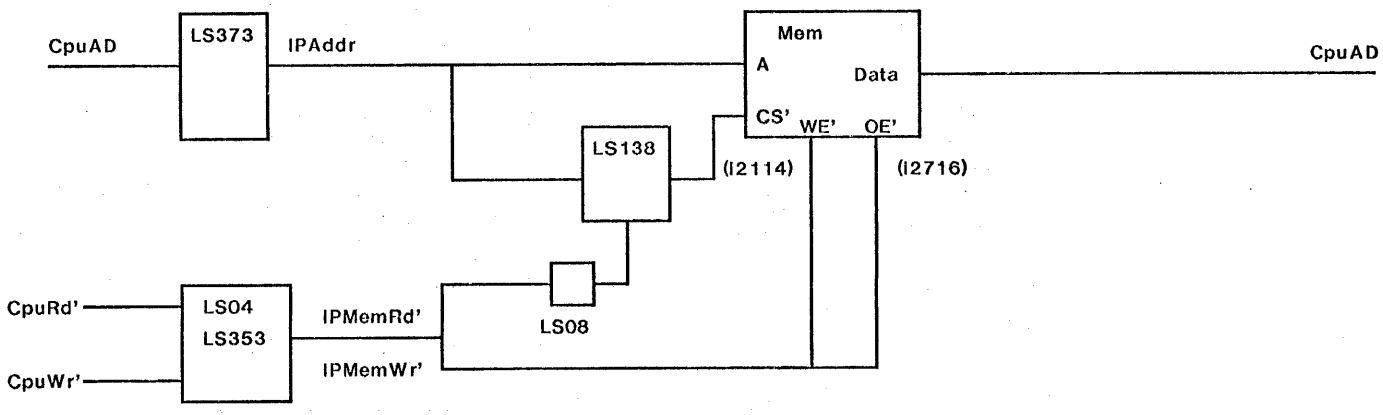


Bank 15

XEROX SDD	Project: Dand/IOP	I/O Processor 4K RAM Memory-Banks 12-15	File: DandIOP24.sil	Designer: Ogus	Rev: E	Date: 10/24/79	Page: 24

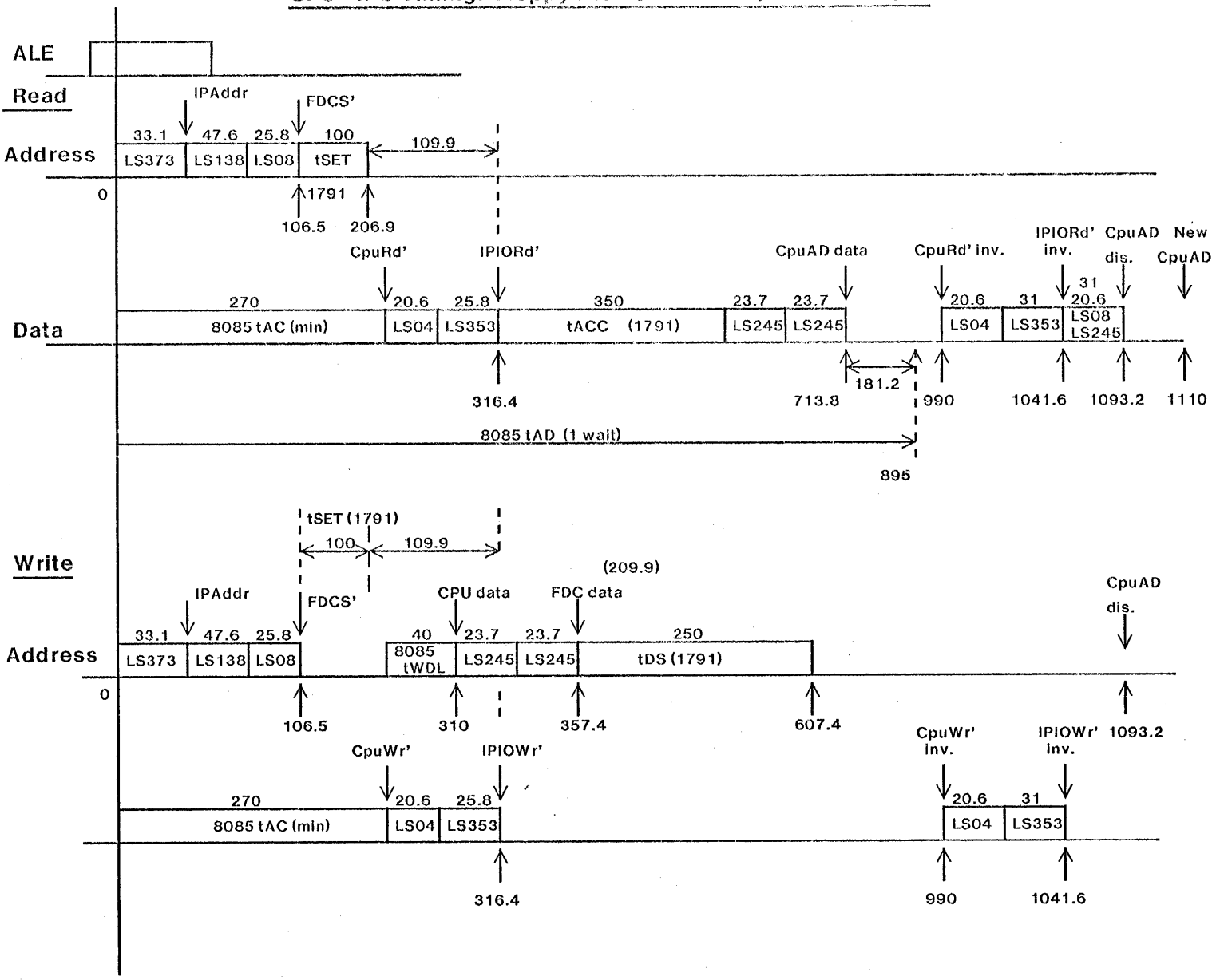
CPU - Memory Timing

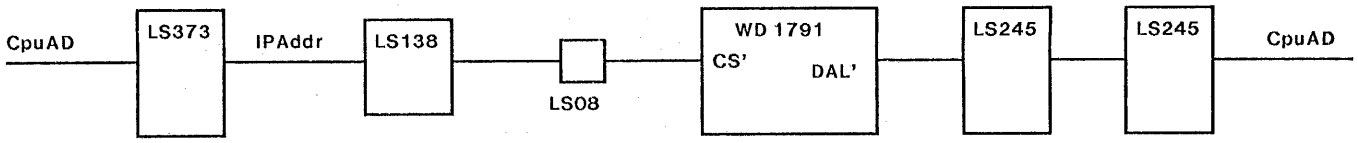




XEROX SDD	Project: Dandelion	I/O Processor CPU timing: Cpu-Mem	File: DandIOP30.silx	Designer: Ogus	Rev: E	Date: 8/9/79	Page: 30

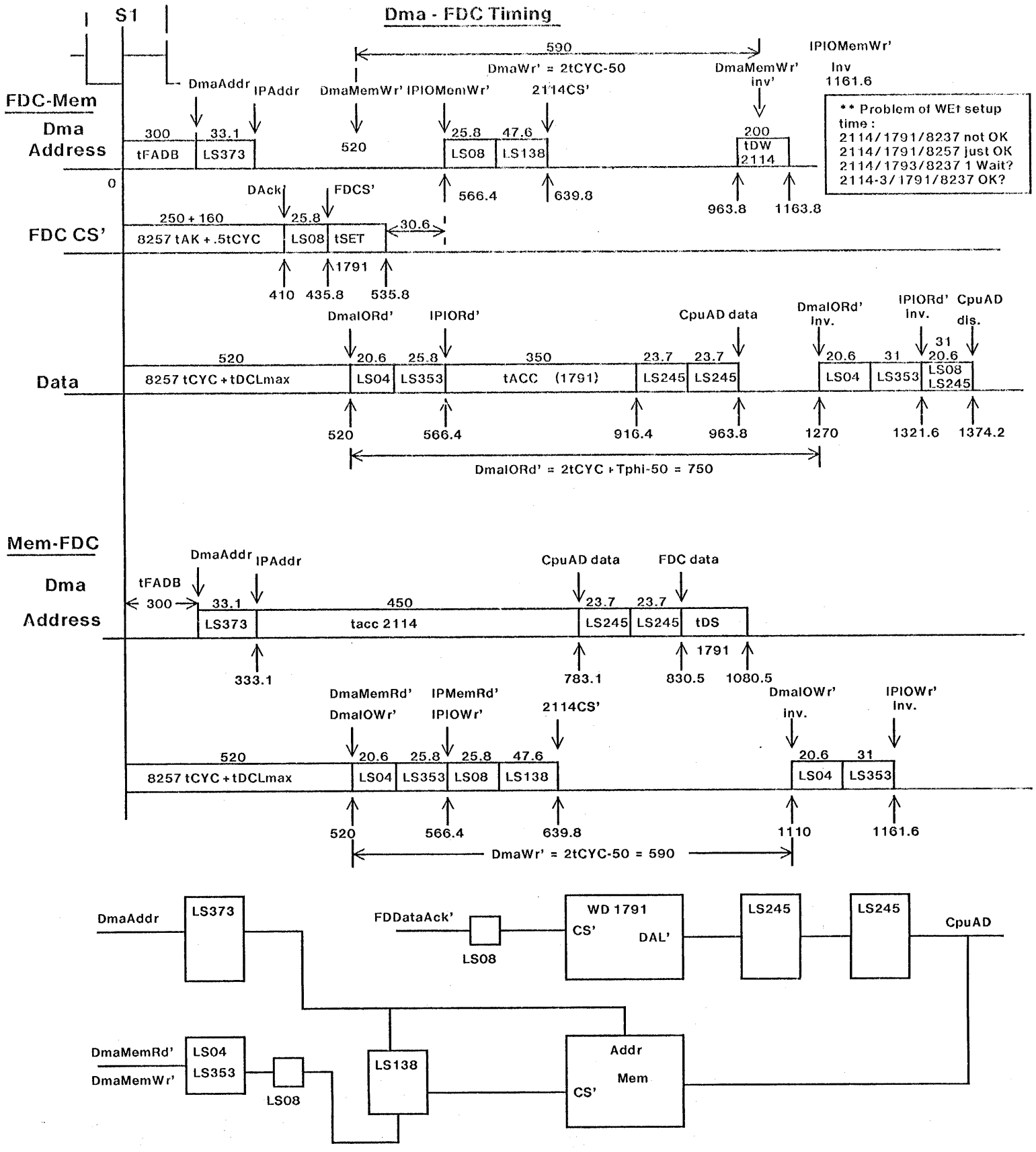
CPU - I/O Timing: Floppy Disk Controller (1 wait state)





XEROX SDD	Project: Dandelion	I/O Processor CPU timing: Cpu-FDC	File: DandIOP31.silx	Designer: Ogus	Rev: E	Date: 8/9/79	Page: 31

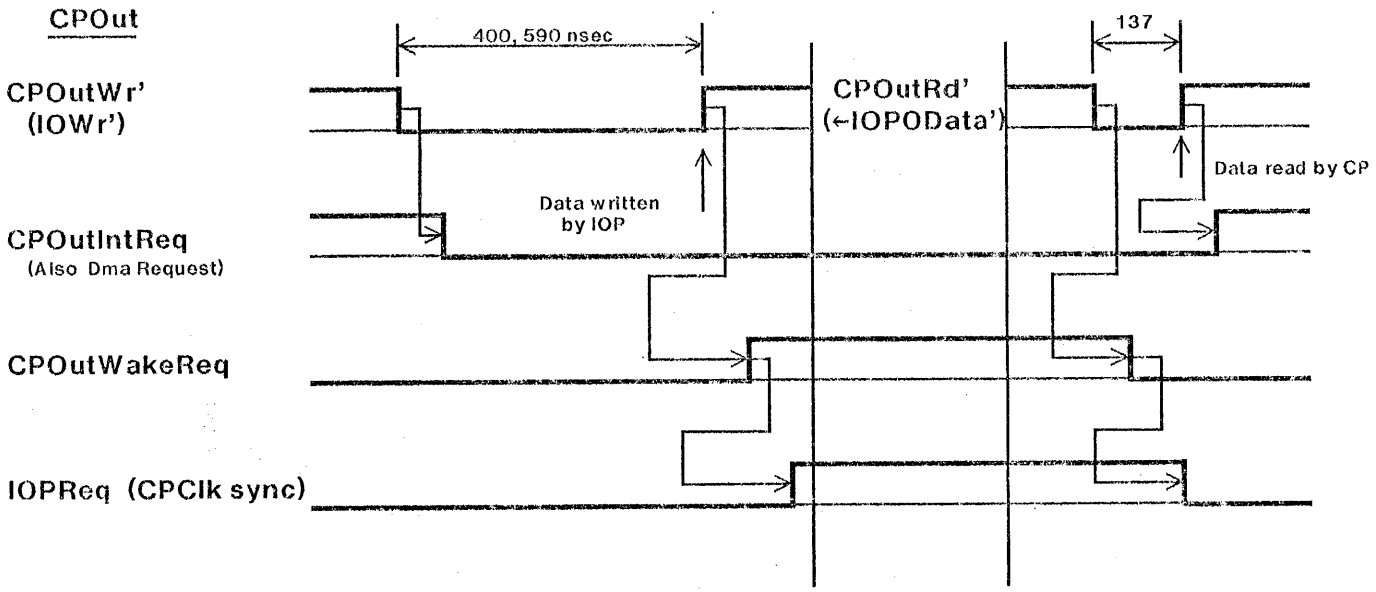
2114-3 or 1793 OK

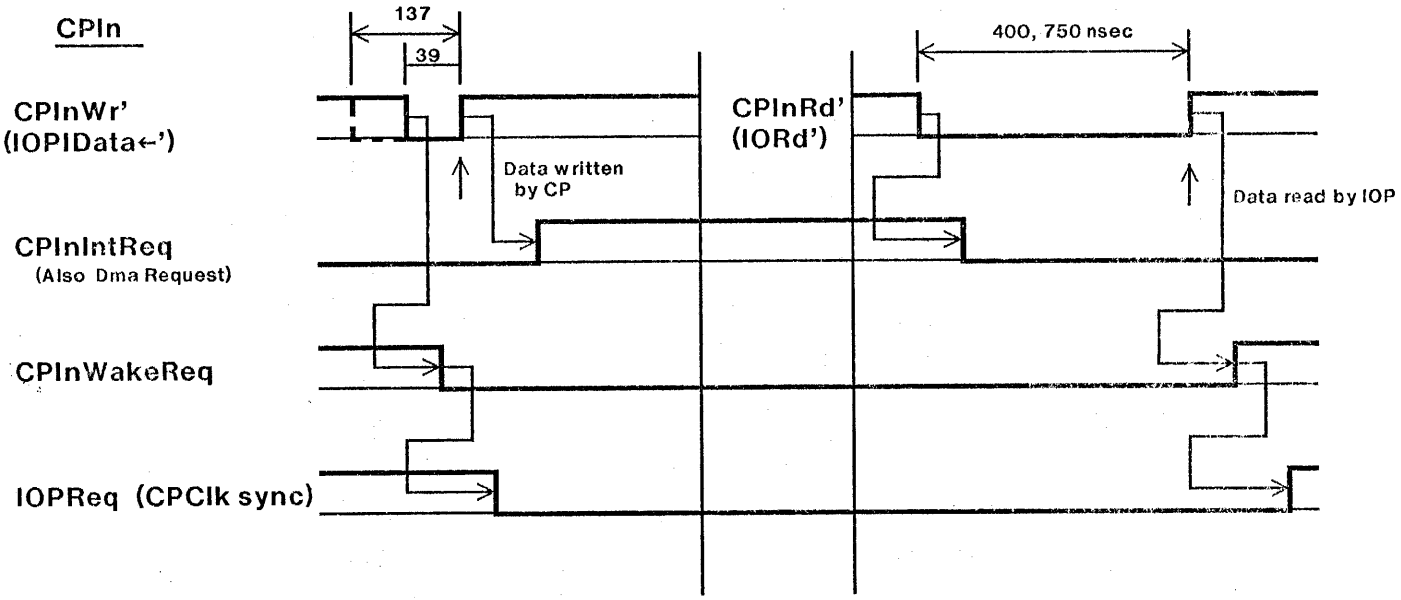


XEROX SDD	Project Dand/IOP	I/O Processor Dma-FDC Timing	File DandIOP32.silx	Designer Ogus	Rev D	Date 8/9/79	Page 32

IOP - CP communication - Port timing

Timing Diagrams (not to scale)





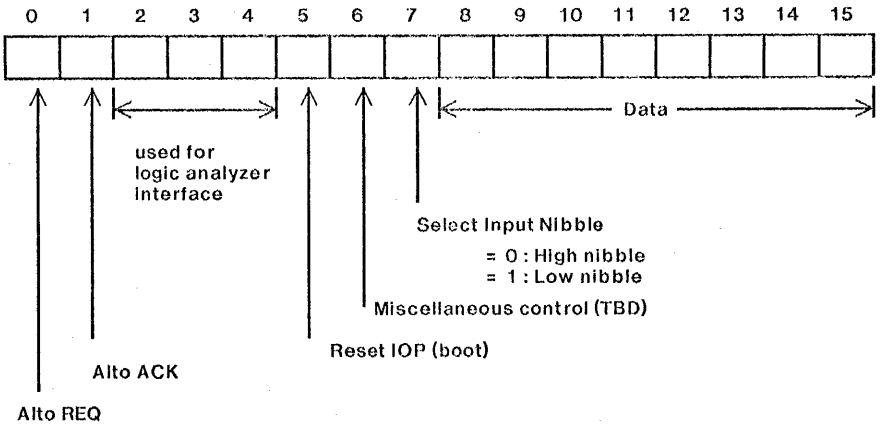
XEROX SDD	Project: Dandelion	I/O Processor CP port timing	File: DandIOP33.silx	Designer: Ogus	Rev: E	Date: 10/25/79	Page: 33

ALTO-DANDELION Communication via Umbilical

Alto Operations

Output:

UTILOUT
(177016B)

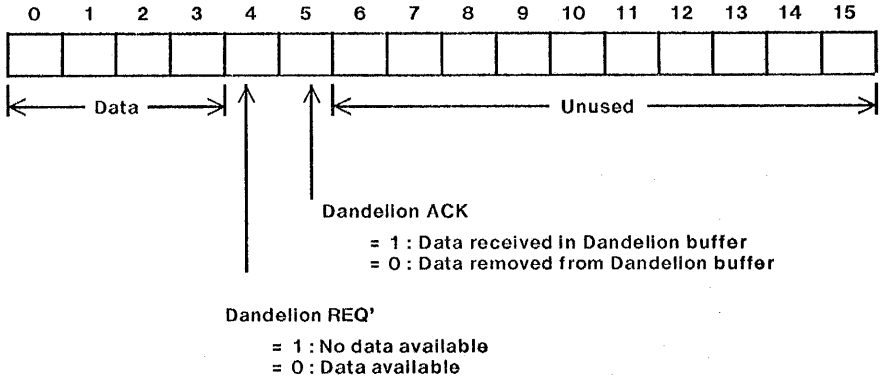


Sequence of Output operation:

- Output data to UTILOUT
- Alto Request (Set AltoREQ = 1) (UTILOUT[0])
- Read Dandelion ACK
  DandelionACK = 1 means data received.
- Remove Alto Request (Set AltoREQ = 0)
- Read Dandelion ACK
  DandelionACK = 0 means data accepted.

Input:

UTILIN
(177030B)



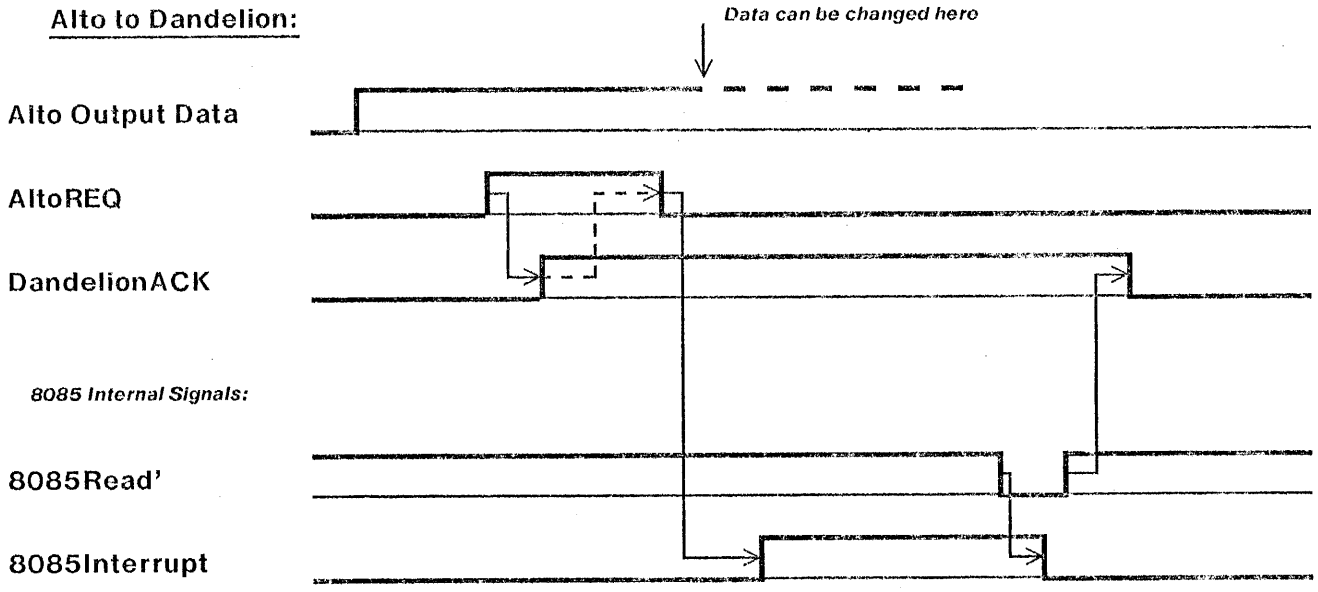
Sequence of Input Operation:

- Poll Dandelion REQ (UTILIN[4])
  DandelionREQ' = 0 means data is available.
- Set SelectInputNibble = 0 (UTILOUT[7])
- Read high data nibble (UTILIN[0:3])
- Set SelectInputNibble = 1 (UTILOUT[7])
- Read low data nibble (UTILIN[0:3])
- Alto Acknowledge (Set AltoACK = 1)
- Poll Dandelion REQ'
  Dandelion REQ' = 1 means ACK has been received.
- Remove Alto Acknowledge (Set Alto ACK = 0)

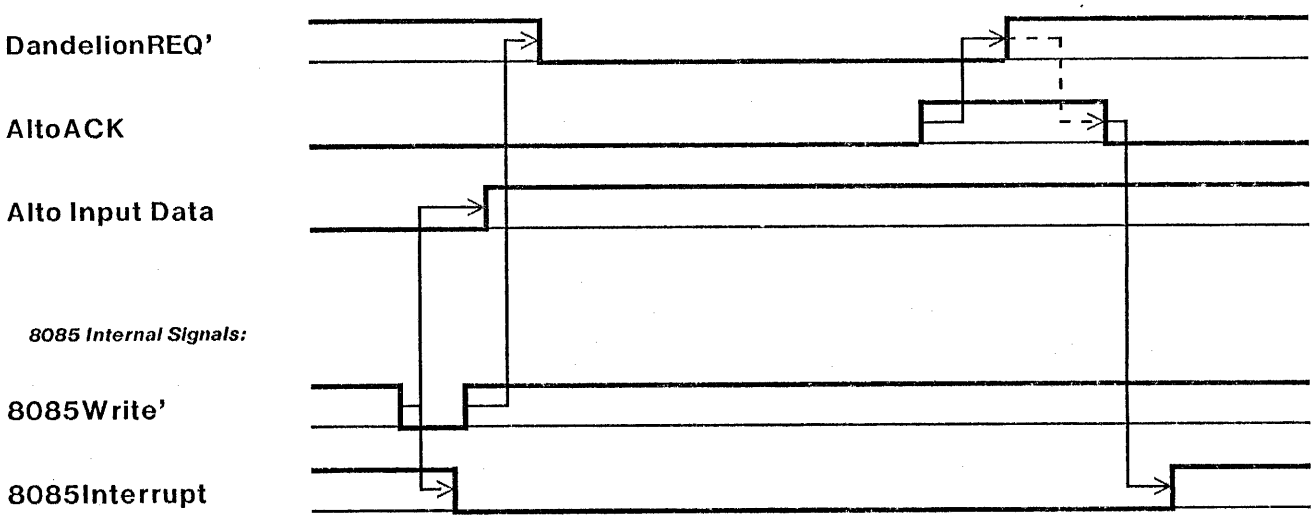
ALTO-DANDELION Communication via Umbilical

Timing Diagrams (not to scale)

Alto to Dandelion:



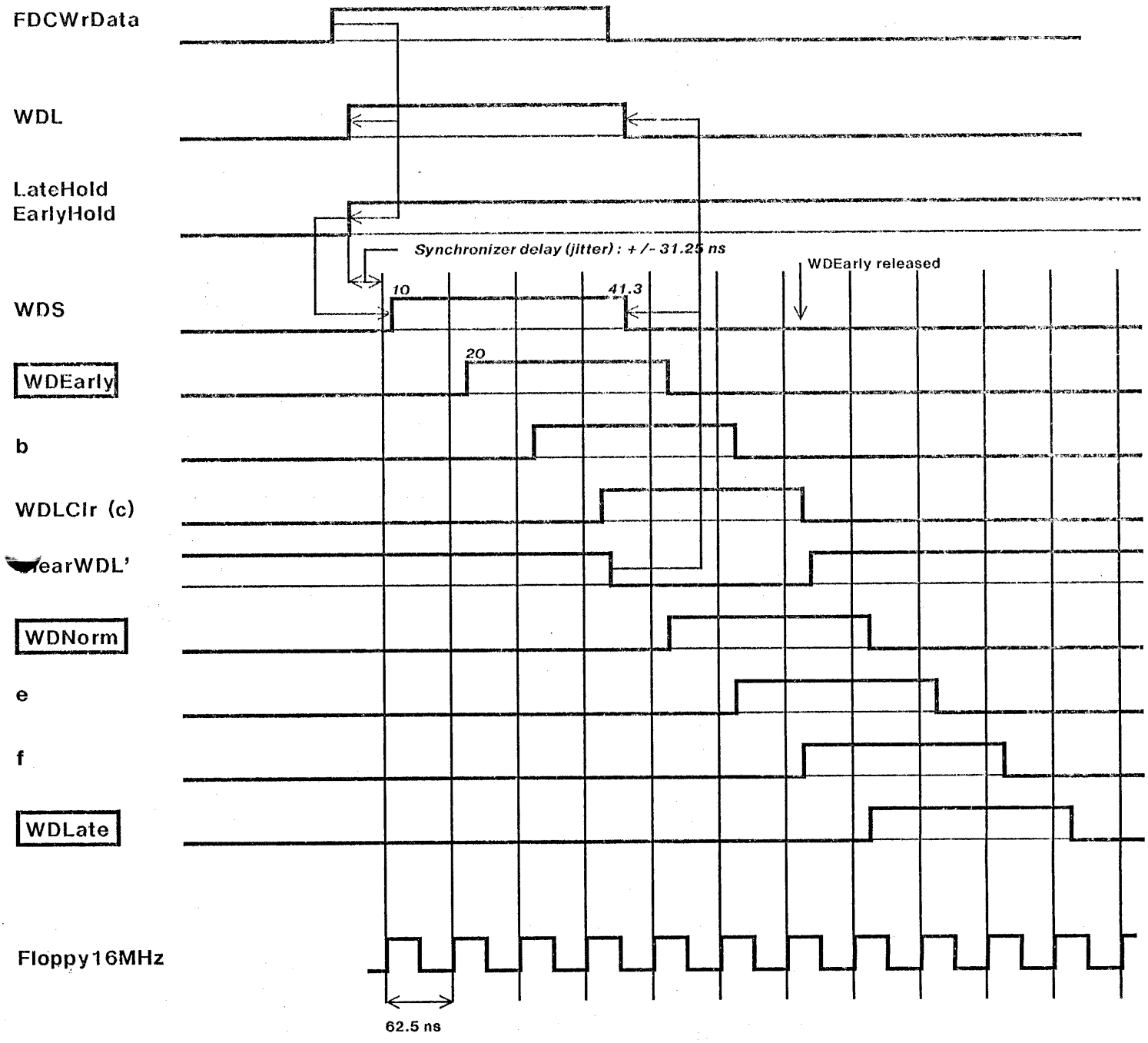
Dandelion to Alto:



Dandelion I/O Processor Floppy Disk Controller

WritePre-compensation Timing Circuit

(See DandIOP09.sil for circuit)



Phase Jitter = +/- 31.25 ns

Precompensation = 187.5 ns +/- jitter

WriteData Pulse width = 187.5 ns

XEROX SDD	Project Dand/IOP	I/O Processor Timing Floppy Controller Write Comp.	File DandIOP39.silx	Designer Ogus	Rev D	Date 6/4/79	Page 39

IPData Loads

(* = smallest margin driver)

Page	Chip	Position	High (uA)	Low (uA) (in, tri)	
6	LS245 (bi)	g11	20	200, 20	Drive: 15000 24000
8	LS273 (in)	d6	20	400	
	LS241 (out)	d7	20	0, 20 (tri)	Drive: 15000 24000
14	LS374 (in)	c9	20	400	
	LS374 (out)	c9	20	0, 20 (tri)	Drive: 2600 24000
	LS240 (out)	c12	20	0, 20 (tri)	Drive: 15000 24000
15	LS175 (in)	g19	20	400	
16	LS374 (out)	d19	20	0, 20 (tri)	Drive: 2600 24000
	S374 (in)	e19	50	250	
18	LS374 (out)	d19	20	0, 20 (tri)	Drive: 2600 24000
19	LS2569 (out)	a/b,9/10	20	0, 20 (tri)	Drive: 2600 8000 *
	LS240 (out)	a7	20	0, 20 (tri)	Drive: 15000 24000
20	LS174 (in)	a6	20	400	
	LS374 (in)	b5	20	400	
Backplane	LS241 (in)		20	200	
	LS241 (in)		20	200	
	LS374 (in)		20	400	
	LS251 (out)		20	0, 20 (tri)	Drive: 2600 8000

	2650	Fixed input loads
340	2810	LS245 drive, all other bi or out are tristate
	3010	LS245 input

IPAData Loads

Page	Chip	Position	High (uA)	Low (uA) (In, tri)	
6	LS245 (bi)	c7	20	200, 20	Drive: 15000 24000
7	i8257 (bi)	m8	10	10	Drive: 150 1600
7	LS373 (in)	d9	20	400	
8	LS245 (bi)	i7	20	200, 20	Drive: 15000 24000
21	i8255 (bi)	d2	10	10	Drive: 400 2500
22	i8251A (bi)	j9	10	10	Drive: 400 2200
22	i8253-5 (bi)	a8	10	10	Drive: 400 2200

100	460	LS245 drive, other LS245 tristate
100	640	LS245 drive, other LS245 input
100	660	Mos drive, one LS245 input, 1 LS245 tristate

IPAddr Loads

Page	Chip	Position	High (uA)	Low (uA) (in, tri)		
1	LS373 (out)	f11, e11	20	0, 20 (tri)	IPAddr.00-15	Drive: 2600 24000
	LS04 (in)	h10	20	400	IPAddr.00 only	
	LS353 (in)	e9	20	400	IPAddr.00 only	
	LS353 (in)	f9	20	400	IPAddr.00 only	
2	i2716 (in)	e,f,g,h12	40	40	IPAddr.05-15 only	
3,4	i2114 (in)	a,b,c,d,e,f,g13,14	160	160	IPAddr.06-15 only	(16 chips)
23,24	i2114 (in)	a,b,c,d,e,f,g15,16	160	160	IPAddr.06-15 only	(16 chips)
5	LS138 (in)	h11	20	400	IPAddr.01-04 only	
	LS138 (in)	d11	20	400	IPAddr.01-05 only	
	LS138 (in)	i13	20	400	IPAddr.01-05 only	
	LS138 (in)	i11	20	400	IPAddr.00,09-13 only	
	LS138 (in)	b11	20	400	IPAddr.12-15 only	
	LS138 (in)	c11	20	400	IPAddr.12-15 only	
	LS155 (in)	a11	20	400	IPAddr.09-11 only	
6	LS00 (in)	a12	20	400	IPAddr.00,01 only	
	LS32 (in)	c6	20	400	IPAddr.01 only	
7	LS373 (out)	d9	20	0, 20 (tri)	IPAddr.00-07 only	Drive: 2600 24000
	LS245 (bi)	d10	20	200	IPAddr.08-15 only	Drive: 15000 24000
8	LS32 (in)	i6	20	400	IPAddr.14,15 only	
15	LS138 (in)	i19	20	400	IPAddr.12-15 only	
21	i8255 (in)	d2	10	10	IPAddr.14,15 only	
22	i8251A (in)	j9	10	10	IPAddr.15 only	
	i8253-5 (in)	a8	10	10	IPAddr.14,15 only	
Backplane	LS241 (in)		20	200	IPAddr.13-15 only	
			120	2020	IPAddr.00	
			120	2020	IPAddr.01	
			440	1760	IPAddr.13	
			490	2190	IPAddr.15	

CpuAD bus loading

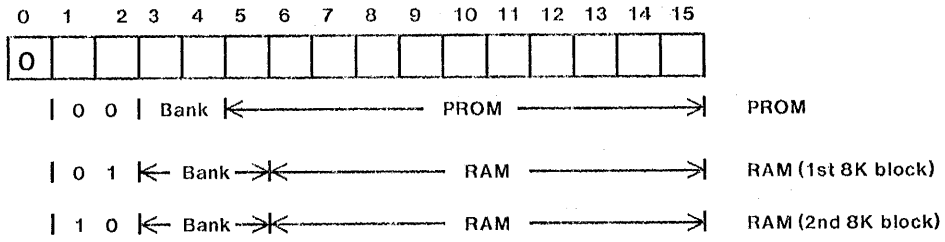
Page	Chip	Position	High (uA)	Low (uA) (in, tri)		
1	i8085	n8	10	10		Drive: 400 2000
	LS373 (in)	e11	20	400		
2	i2716 (out)	e,f,g,h12	40	40		Drive: 400 2100
3,4	i2114 (bi)	a,b,c,d,e,f,g13,14	80	80	(8 chips)	Drive: 1000 2100
23,24	i2114 (bi)	a,b,c,d,e,f,g15,16	80	80	(8 chips)	Drive: 1000 2100
6	LS245 (in)	g11	20	200		
	LS245 (in)	c7	20	200		
			260	1000	8085, 2114, or 2716 drive	

IPMemRd', IPMemWr', IPIORd', IPIOWr' loads

Page	Chip	Position	High (uA)	Low (uA) (in, tri)			
1	LS353 (out)	e9	--	--	MemRd, MemWr		Drive: 2600 8000
	LS353 (out)	f9	--	--	IORd, IOWr		Drive: 2600 8000
	LS08 (in)	g10	20	400	MemRd, MemWr		
	LS74 (in) (S',R')	g9	40	800	IORd, IOWr		
2	i2716 (in)	e,f,g,h12	40	40	MemRd		
3,4	i2114 (in)	a-h,13,14	160	160	MemWr	(16 chips)	
23,24	i2114 (in)	a-h,15,16	160	160	MemWr	(16 chips)	
5	LS138 (in)	b11, c11	20	400	IORd, IOWr		
6	LS08 (in)	a12	20	400	IORd, IOWr		
7	LS241 (in)	d7	20	200	IORd, IOWr		
8	WD1791 (in)	p8	10	10	IORd, IOWr		
14	LS32 (in)	a10	20	400	IORd, IOWr		
15	LS138 (in)	l19	20	400	IOWr		
	LS32 (in)	h19	20	400	IORd		
16	LS32 (in)	a10	20	400	IORd, IOWr		
21	i8255 (in)	d2	10	10	IORd, IOWr		
22	i8251A (in)	j9	10	10	IORd, IOWr		
	i8253-5 (in)	a8	10	10	IORd, IOWr		
			60	440	IPMemRd'		
			340	720	IPMemWr'		
			200	3040	IPIORd'		
			200	3040	IPIOWr'		

Dandelion I/O Processor Address Space

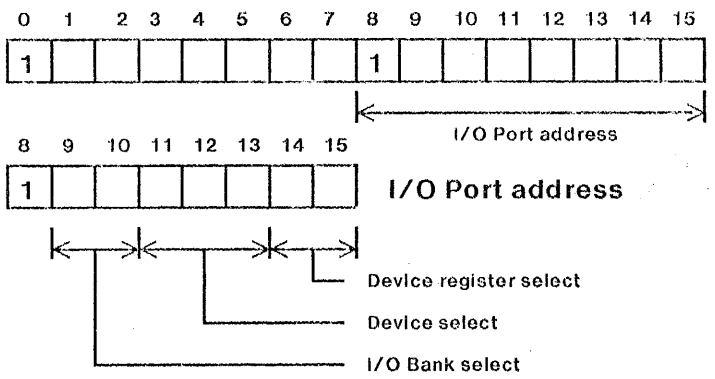
Normal memory address space



Bank	Type	Address Range (Hex)				Addr[1:2]
0	PROM	0	-	7FF	(2K)	0
1	PROM	800	-	0FFF	(2K)	0
2	PROM	1000	-	17FF	(2K)	0
3	PROM	1800	-	1FFF	(2K)	0
0	RAM	2000	-	23FF	(1K)	1
1	RAM	2400	-	27FF	(1K)	1
2	RAM	2800	-	2BFF	(1K)	1
3	RAM	2C00	-	2FFF	(1K)	1
4	RAM	3000	-	33FF	(1K)	1
5	RAM	3400	-	37FF	(1K)	1
6	RAM	3800	-	3BFF	(1K)	1
7	RAM	3C00	-	3FFF	(1K)	1
0	RAM	4000	-	43FF	(1K)	2
1	RAM	4400	-	47FF	(1K)	2
2	RAM	4800	-	4BFF	(1K)	2
3	RAM	4C00	-	4FFF	(1K)	2
4	RAM	5000	-	53FF	(1K)	2
5	RAM	5400	-	57FF	(1K)	2
6	RAM	5800	-	5BFF	(1K)	2
7	RAM	5C00	-	5FFF	(1K)	2

Dandelion I/O Processor Address Space

I/O Address Space



Notes:

1. I/O Ports can be reached using:

   a) IN or OUT instructions using port address:

   P = 80H + p, where 0 <= p <= 7FH (128)

   b) Memory reference instructions using address:

   A = 8000H + P, where P is given above.

   Note that bit 8 being 1 is not required by the hardware.

2. Addresses (hex):

Bank 0	80 - 9F
Bank 0a	*80 - 8F*
Bank 0b	*90 - 9F*
Bank 1	A0 - BF
Bank 1a	*A0 - AF*
Bank 1b	*B0 - BF*
Bank 2	C0 - DF
Bank 1a	*C0 - CF*
Bank 1b	*D0 - DF*
Bank 3	E0 - FF
Bank 3a	*E0 - EF*
Bank 3b	*F0 - FF*

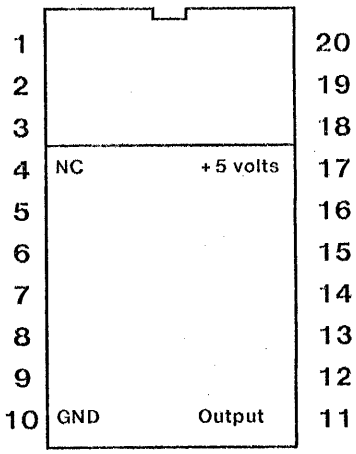
Address (Hex)	Bank	
80	0a	Alto PPI-A
81	0a	Alto PPI-B
82	0a	Alto PPI-C
83	0a	Alto PPI-Control
84	0a	Floppy Status (Read)
84	0a	Floppy Command (Write)
85	0a	Floppy Track (R, W)
86	0a	Floppy Sector (R, W)
87	0a	Floppy Data (R, W)
0E8	3a	Floppy Control reg. (Write)
0E8	3a	Floppy Status (ext.) (Read)
88	0a	Printer data (R, W)
89	0a	Printer Control (Write)
89	0a	Printer Status (Read)
8A, 8B	0a	(Same as 88, 89)
8C	0a	Timer Counter 0 (R,W)
8D	0a	Timer Counter 1 (R,W)
8E	0a	Timer Counter 2 (R,W)
8F	0a	Timer Mode (Write)
Dma 8257		
0B0	1b	DMA Ch-0 Address
0B1	1b	DMA Ch-0 Count
0B2	1b	DMA Ch-1 Address
0B3	1b	DMA Ch-1 Count
0B4	1b	DMA Ch-2 Address
0B5	1b	DMA Ch-2 Count
0B6	1b	DMA Ch-3 Address
0B7	1b	DMA Ch-3 Count
0B8	1b	DMA Mode Set (Write)
0B8	1b	DMA Status (Read)
0B9 - 0BF	1b	Invalid
0F0	3b	Dma Test register (R, W)
0F1 - 0FF	3b	Invalid (DmaTest)

Address (Hex)	Bank	
0C0 - 0C7	2a	(Unavailable for Read)
0C8	2a	TPC High (Addr, High 5 bits data') (W)
0C8	2a	TC [0:3],,TPC[0:3]' (Read)
0C9	2a	TPC Low (Low 7 bits data') (Write)
0C9	2a	TPC[4:11]' (Read)
0CA	2a	Control Store Byte 0 (R, W)
0CB	2a	Control Store Byte 1 (R, W)
0CC	2a	Control Store Byte 2 (R, W)
0CD	2a	Control Store Byte 3 (R, W)
0CE	2a	Control Store Byte 4 (R, W)
0CF	2a	Control Store Byte 5 (R, W)
0E9	3a	Interrupt Request register (read)
0EA	3a	Keyboard data (read)
0EB	3a	CPIn (read)
0EC	3a	CPStatus (read)
0ED	3a	Mouse X (read)
0EE	3a	Mouse Y (read)
0EF	3a	Misc Inputs 1 (read)
0E9	3a	Clocks 1 (write)
0EA	3a	TOD interrupt (clear)
0EB	3a	CPOut (write)
0EC	3a	Central processor Control (write)
0ED	3a	Mouse XY (clear)
0EE	3a	CP Dma Complete (clear)
0EF	3a	Control 1 (write)

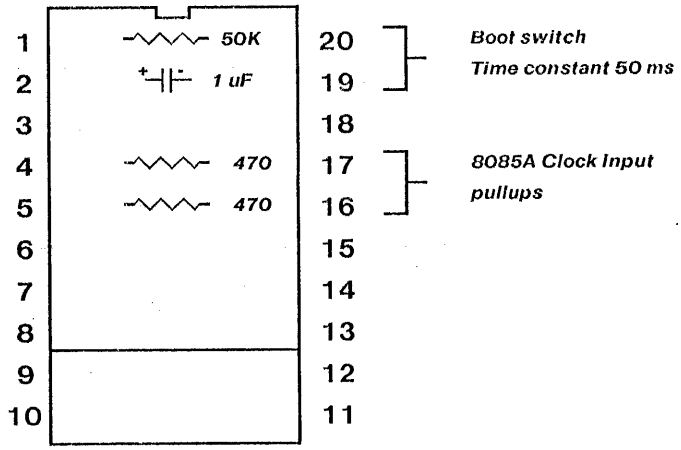
XEROX SDD	Project	File	Designer	Rev	Date	Page
	Dandelion I/O Processor Address Space I/O Address Space	DandIOP51.silx	Ogus	E	10/25/79	51

Clock i10
Crystal Clock in 14 pin
package right-aligned as shown.

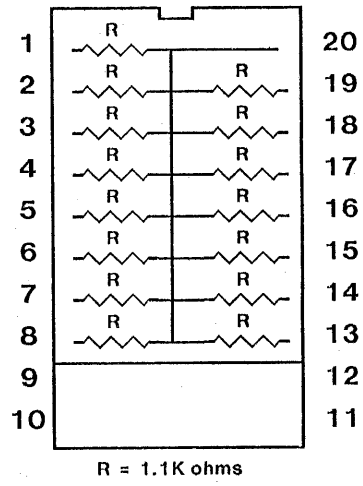
Motorola K1114A clock or equiv.
5.88 MHz (temp)



FPLAT i9
Miscellaneous components
16 pin platform
Left aligned as shown.
Resistors 1/4 watt, 5%



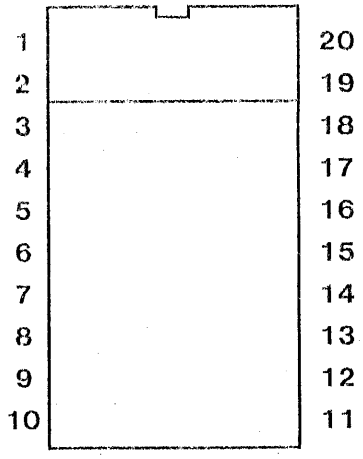
FPLAT e10
10K pullup resistors
16 pin package left-aligned as shown.
Allen-Bradley 316A103
or equivalent



R = 1.1K ohms

FPLAT b2
Pullup/pulldown resistors
16 pin package right aligned as shown.

Allen-Bradley 316E131211
or equivalent

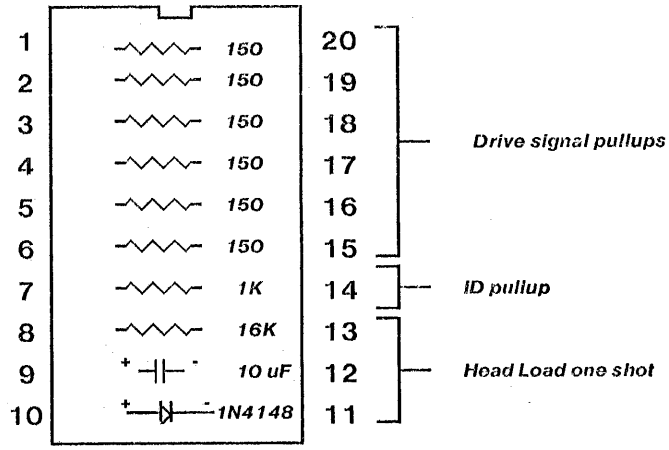


R 1 = 130 ohms, R2 = 210 ohms

FPLAT f2

Pullup resistors for
Floppy drive signals,
Head Load one-shot discretes
20-pin platfrom

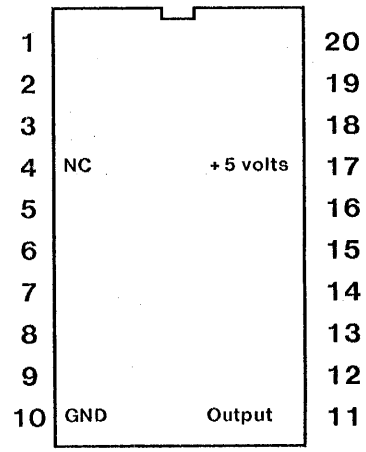
Resistors 1/4 watt, 5%



Clocks i5, a5

Floppy Controller Clock
Baud Rate Generator Clock
Crystal Clock in 14 pin
package right-aligned as shown.

Motorola K1114A
16 MHz, 1.8432 MHz



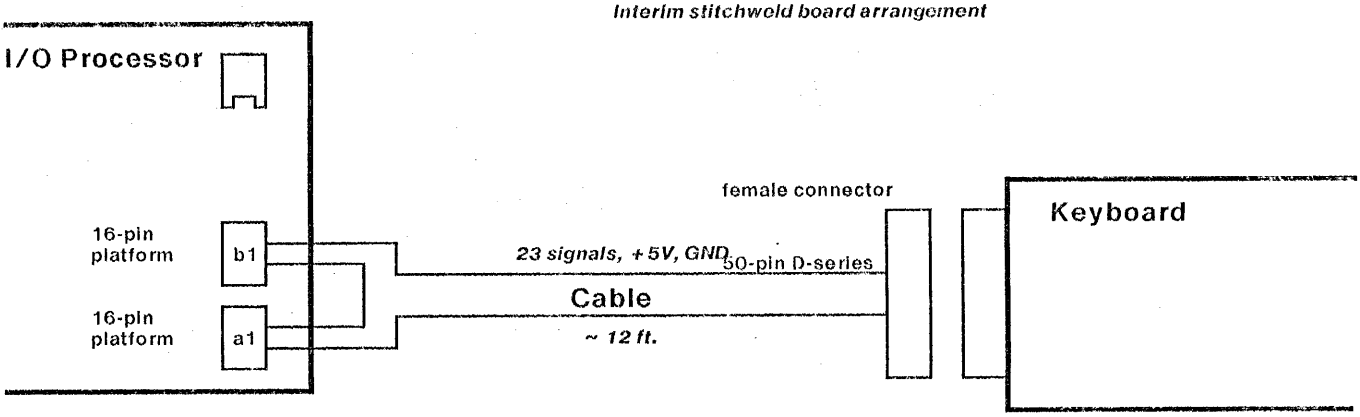
FPLAT a1, b1 : Keyboard Cable

DipSocket c2: Maintenance Panel Cable

FPLAT d2: Alto Control Cable

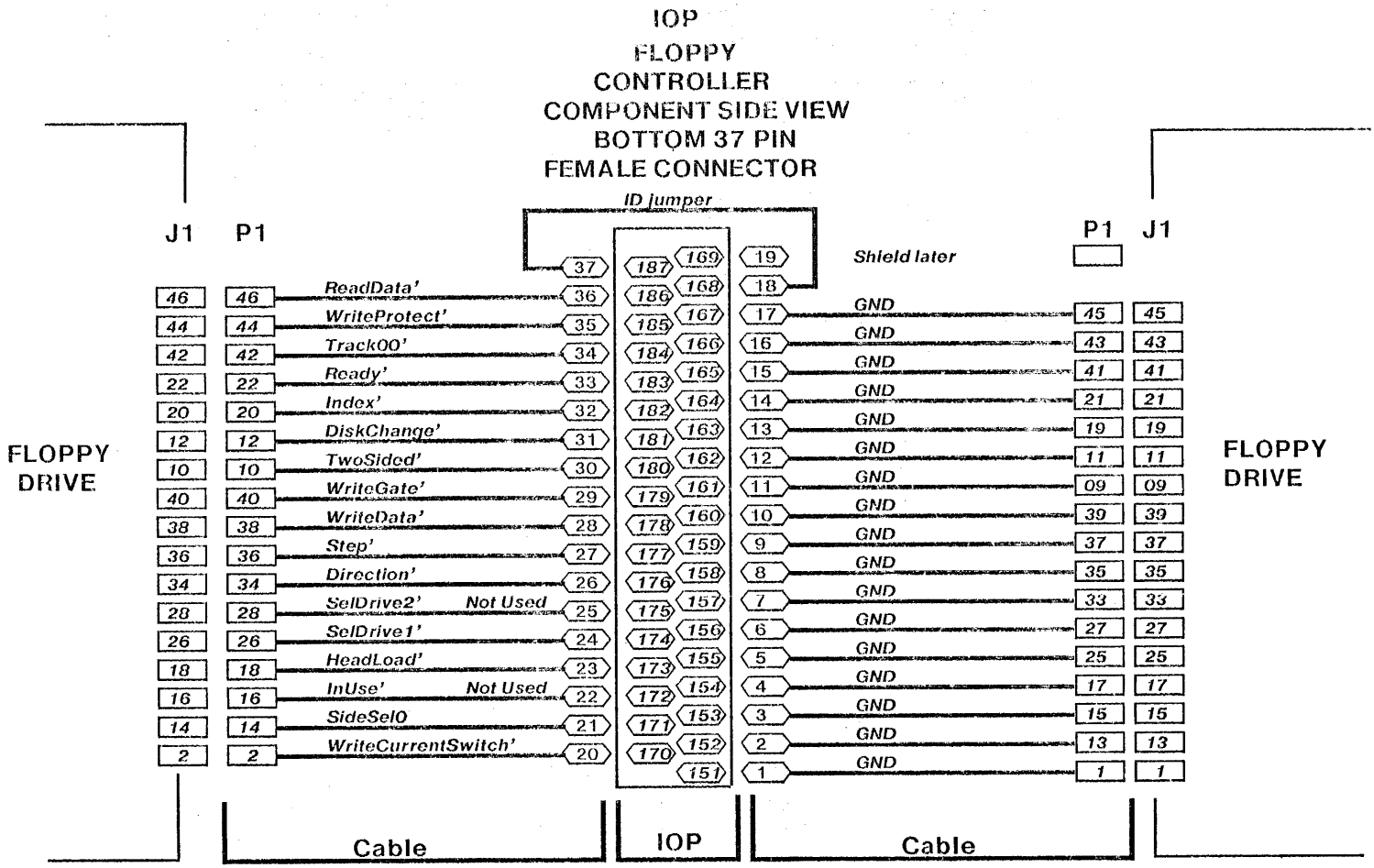
I/O Processor Keyboard Cable

Interim stitchweld board arrangement



Signal	IOP Connector pin		Keyboard Connector pin
	Platform a1	Platform b1	50-pin connector
KBData.0	—	3	39
KBData.1	—	8	2
KBData.2	—	9	3
KBData.3	—	7	4
KBData.4	—	10	5
KBData.5	—	6	6
KBData.6	—	11	7
KBData.7	—	5	8
KBSel	—	1	11
KBSelRet	—	15	28
KBDiag	—	2	10
KBDiagRet	—	14	27
KBReq	—	12	9
KBReqRet	—	4	26
Tone	3	—	46
ToneRet	15	—	45
MouseXA	16	—	48
MouseXB	1	—	50
MouseYA	11	—	16
MouseYB	6	—	15
MouseSW1	10	—	14
MouseSW2	7	—	13
MouseSW3	9	—	12
+5V	—	16	41, 42, 43
GND	8	—	19, 20,21,22,23,24,25,29,30,31,32, 33,34,40,47,49
No cable connection	*2,4,5,12,13*	*13*	*1,17,18,35,36,37,38,44*

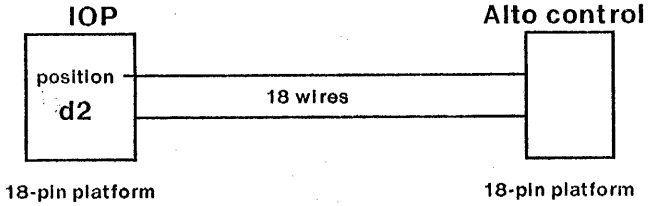
Note: On Platform a1, connect a 390 ohm resistor between pin 3 and 14



17 twisted pairs
1 jumper (2 pins)

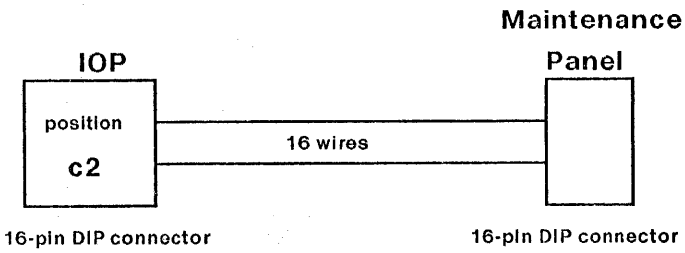
Note: On Edge J1, even numbers are on component side of board, odd numbers on non-component side

IOP to Alto control cable



One-to-One connection between 2 18 pin platforms

IOP-Maintenance Panel cable

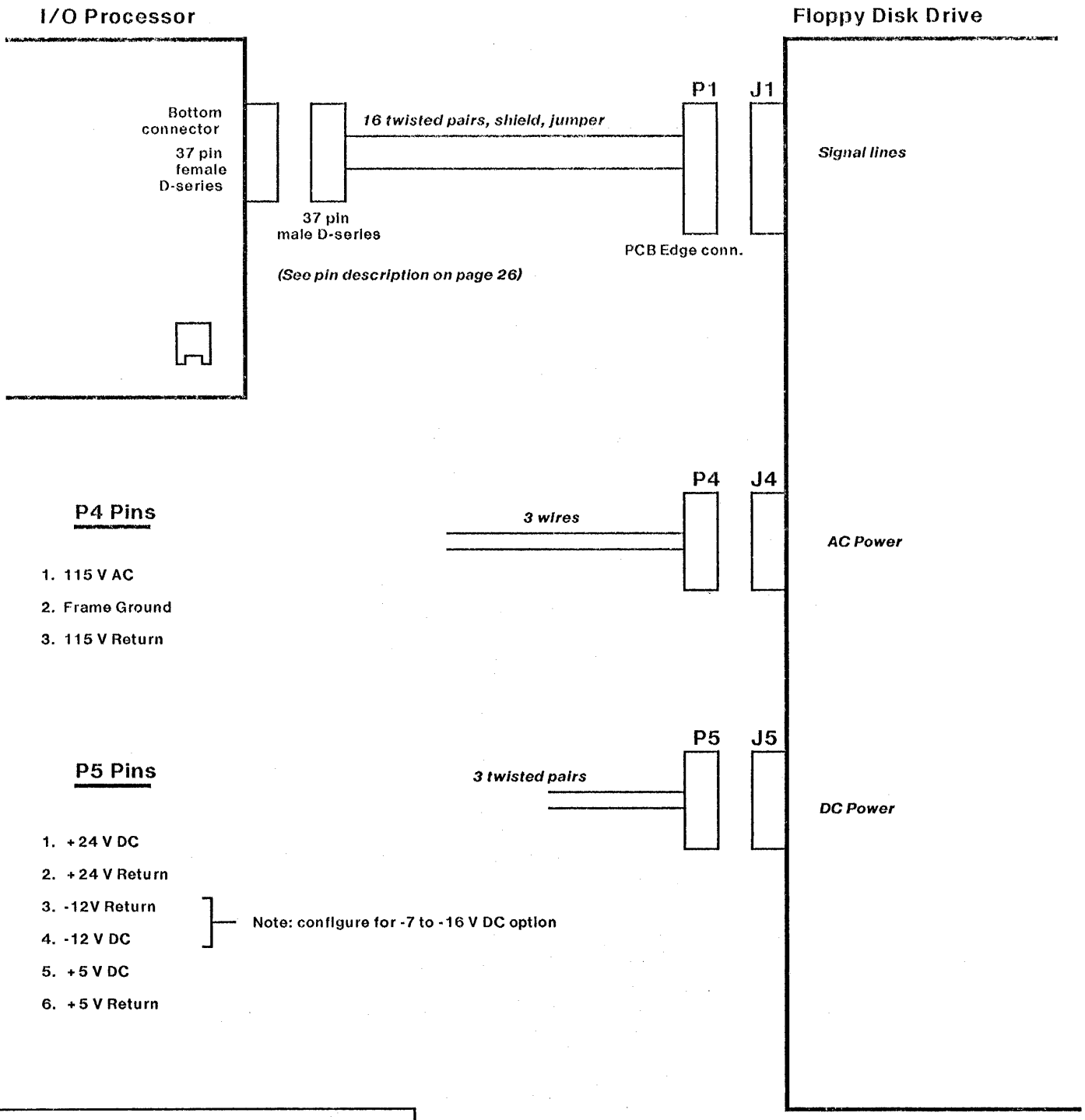


One-to-One connection between 2 16-pin DIP connectors

XEROX SDD	Project	I/O Processor Floppy Disk Signal Cable Misc. cables	File	Designer	Rev	Date	Page
	Dandelion		DandIOP56.silx	Ogus	E	10/25/79	56

I/O Processor

Floppy Disk Cabling



P4 Pins

1. 115 V AC
2. Frame Ground
3. 115 V Return

P5 Pins

1. +24 V DC
2. +24 V Return
3. -12V Return
4. -12 V DC
5. +5 V DC
6. +5 V Return

Note: configure for -7 to -16 V DC option

Note: See SA 850 OEM manual, pages 17, 18, 19, 20 for details of connectors.

1 10 20 30 40 50 51 60 70 80 90 100
101 110 150 151 200

Note: ● indicates where capacitors have to be removed and pin inserted.
Coordinate of pin 1 of large chips is indicated.

	a	b	c	d	e	f	g	h	i	
19	S00	LS240	LS273	LS374	S374	S240	LS175	LS32	LS138	19
18			LS74	LS74	LS374		LS175			18
17			LS157	LS08	F93427					17
16	i2114	i2114	i2114	i2114	i2114	i2114	i2114	i2114	i2114	16
15		i2114	i2114	i2114	i2114	i2114	i2114	i2114		15
14	i2114	i2114	i2114	i2114	i2114	i2114	i2114	i2114	LS240	14
13	i2114	i2114	i2114	i2114	i2114	i2114	i2114	i2114	LS138	13
12	LS00 a	LS245 b	LS240 c		i2716 e	i2716 f	i2716 g	i2716 h		12
11	LS155	LS138	LS138	LS138	LS373	LS373	LS245	LS138	LS138	11
10	LS32	LS2569	LS2569	LS245	10K resist. 16 ■	LS74	LS08	LS04	clock 6 MHz	10
9	LS2569	LS2569	LS10	LS373	LS353	LS353	LS74	LS00	FPLAT 16 ■	9
8	i8253-5 a	i8257 b c			i8085A e f		WD 1793 g h			8
7	LS240	LS04	LS374	LS241			LS00	LS74	LS245	7
6	LS174	LS374	LS32	LS273				LS08	LS32	6
5	clock 1.8432 MHz	LS374						LS04	clock 16 MHz	5
4	LS74		● i8251A c3.13 ●		S74	LS74	LS273	F93453	S163	4
3	75115	LS240			LS253	S374	LS74	F93453	S02	3
2	74265	FPLAT ■ 16	DipCable ■ 16	FPLAT ■ 18	N123	FPLAT 20				2
1	FPLAT ■ 16	FPLAT ■ 16	75189	75188	S240	S240				1
	a	b	c	d	e	f	g	h	i	

DIP Orient. 1

I/O Connector (25 pin female)

I/O Connector (37 pin female)

XEROX SDD	Project Dandelion	IOP board stuffing sheet	File DandIOP60.silx	Designer Ogus	Rev E	Date 10/25/79

1 / 101	10 / 110	20 / 120	30 / 130	40 / 140	50 / 150	51 / 151	60 / 160	70 / 170	80 / 180	90 / 190	100 / 200
+12v "VDD"	gnd "GND" = ⏚	gnd	gnd	gnd	+5V "VCC"	+5V "VCC"	gnd	gnd	gnd	gnd	-5V "VEE"

	a	b	c	d	e	f	g	h	i	
19	S00 CPClk	LS240 CPPort Stat, Misc , SKY/c	LS273 @ IOP Control	LS374 CPIn	S374 CPOut	S240 IOP Status	LS175 CPControl-1	LS32 @ ReadCSEn'	LS138 CSWE, WrTPC	19
18			LS74 CPInWakeReq CPOutWakeReq	LS74 CPInIntReq CPOutIntReq	LS374 IOPReq., CPClk sync		LS175 CPControl-2			18
17			LS157 @ CPDmaReq	LS08	F93427 IOPReq.					17
16	RAM-B1 I2114	I2114	I2114	I2114	RAM-B2 I2114	I2114	I2114	I2114	I2114	16
15	14	I2114	I2114	I2114	I2114	I2114	I2114	I2114		15
14	RAM-A1 I2114	I2114	I2114	I2114	RAM-A2 I2114	I2114	I2114	I2114	LS240 @ SKY/b, /d IPReset'	14
13	I2114	I2114	I2114	I2114	I2114	I2114	I2114	I2114	LS138 RAM-B Sel.	13
12	a LS00 Enable IPData, IPAData	b LS245 IPAData bus	c LS240 @ Int Req Reg.		e PROM I2716 PROM Bank 3	f I2716 PROM Bank 2	g I2716 PROM Bank 1	h I2716 PROM Bank 0		12
11	LS155 I/O Select Bank 2, 3	LS138 I/O Select Reg. Read	LS138 I/O Select Reg. Write	LS138 RAM-A Sel.	LS373 Address Lo	LS373 Address Hi	LS245 IPData bus	LS138 PROM Select	LS138 I/O Select Bank 0	11
10	LS32 @ CPIn,Out, Dma Test	LS2569 MouseX HI	LS2569 MouseY Hi	LS245 DMA Addr Lo	FPLAT @ Pull-up	LS74 Cpu Ready	LS08 DmaTest, CpuResetIn' IPIORdWr',DmaC	LS04 @ IPAddr.00 PClock,IPReset CpuRd'/Wr'	K1114A Clock (6 MHz)	10
9	LS2569 MouseX Lo	LS2569 MouseY Lo	LS10 @ Enable PData, IPADat	LS373 DMA Addr HI	LS353 IPIORd' IPIOWr'	LS353 IPMemRd' IPMemWr'	LS74 IPDataOut CP Dma EndC	LS00	FPLAT @ Misc. comp.	9
8	a i8253-5 Baud Rate Generator	b c i8257 m8 DMA controller			e f i8085A n8 CPU		g h WD 1793 p8 Floppy Controller			8
7	LS240 @ Misc Input 1	LS04 Dma Invert.	LS374 Dma Test	LS241 @ FDC status Dma IORd,IOWr			LS00 @ CP Dma EndC	LS74 FIDC DataReq FDC End Cnt	LS245 FDC-IPAData	7
6	LS174 Misc Control 1	LS374 KB data	LS32 @ 8253 Rd,Wr, EnIPAData	LS273 FDC State	k3			LS08	LS32 @	6
5	K1114A Clock (1.8432 MHz)	LS374 Misc Clocks 1						LS04	K1114A Clock (16 MHz)	5
4	LS74 @ TOD Intr.		Printer Control		S74 Write Comp.	LS74 Write Comp.	LS273 Data Sep.	F93453 Data Sep.	S163 Clock Divider	4
3	N75115 @ KBReq Rcvr	LS240 Mouse X,Y rec. Misc. Contr.1	i8251A Printer UART j9		LS253 @ Write Comp.	S374 Write Comp.	LS74 Data Sep.	F93453 Data Sep.	S02 @	3
2	N265 @ KB Sel Diag Driver	FPLAT KB data Pullup/down	DipSocket MPanel Connector	FPLAT Alto Control Connector	N123 @ Head Load	FPLAT Pullups				2
1	FPLAT KB Conn. 1	FPLAT KB Conn. 2	N75189 Printer Rcvr	N75188 Printer Dvr	S240 @ Receivers SKY/a	S240 Drivers	k8		20	1
	a	b	c	d	e	f	g	h	i	

DIP Orient. 1

I/O Connector (25 pin female)

I/O Connector(37 pin female)

Chip positions used: 136
Chip positions left: 31

XEROX SDD	Project Dandelion	IOP board layout (modified D0 board)	File DandIOP61.silx	Designer Ogus	Rev E	Date 10/23/79