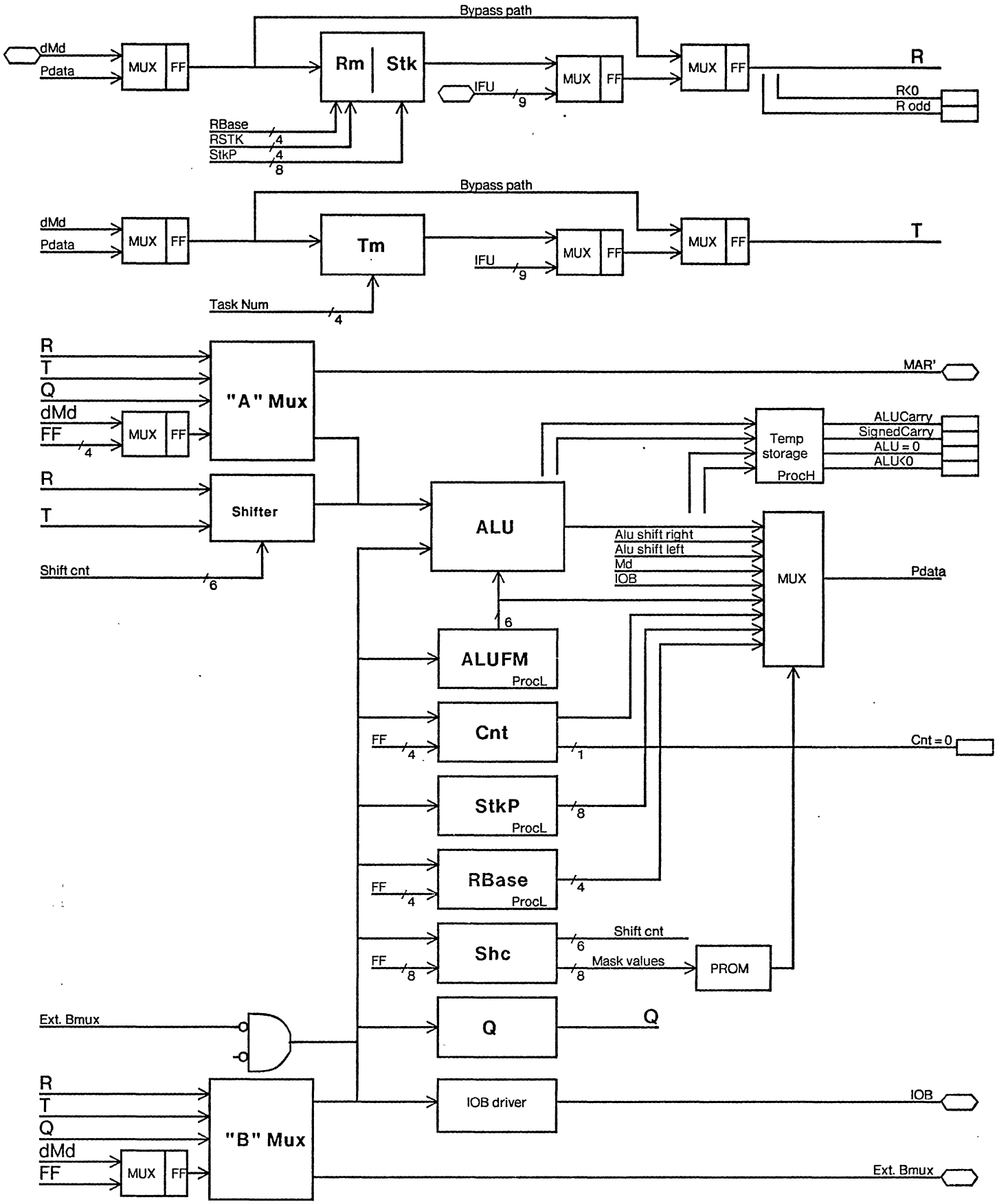
DORADO SCHEMATICS

Low Byte

PROCESSOR

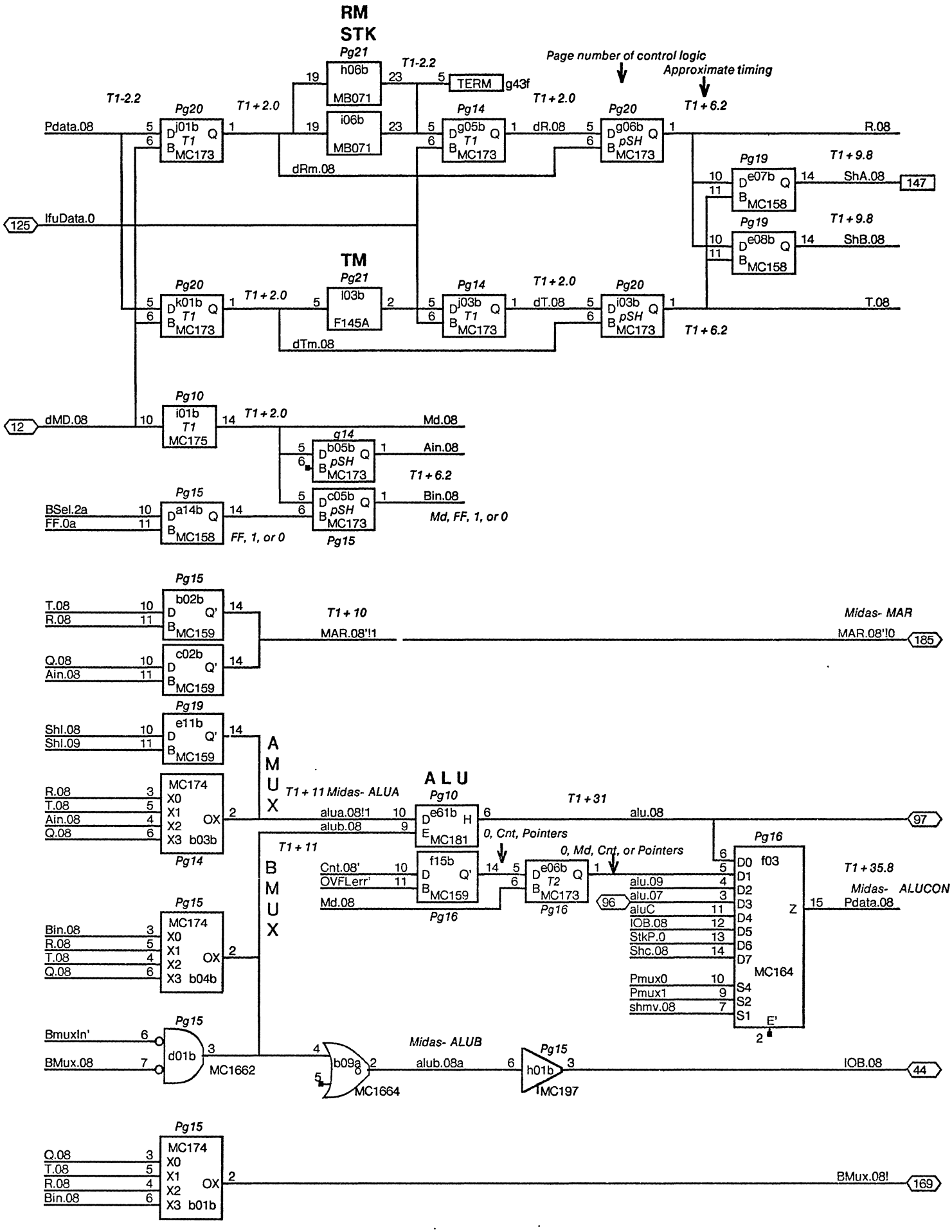
JUMP [126] WITH 100Ω TO -2V
L.L.Ø

Table of contents

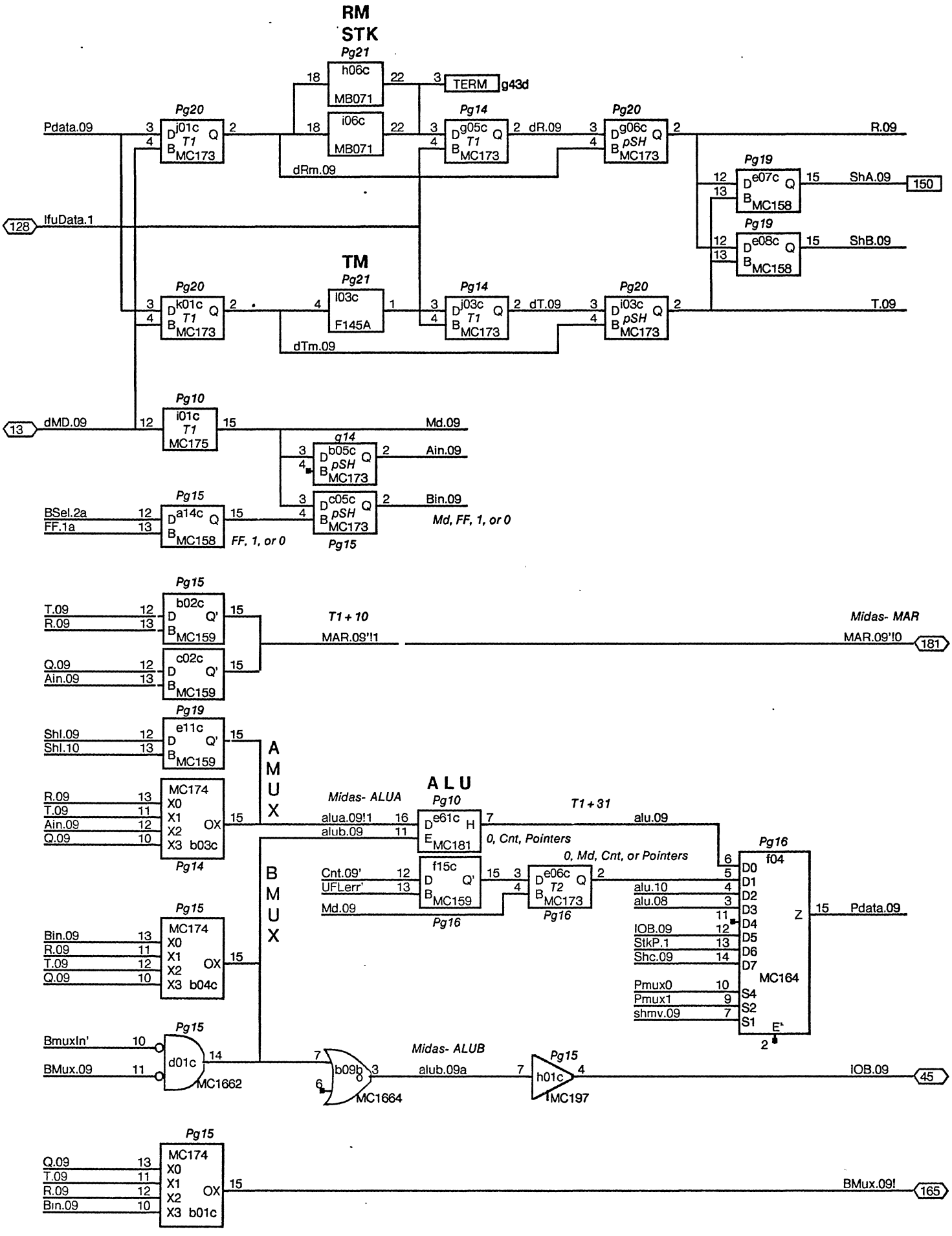


Note: all busses 16 wide unless noted otherwise

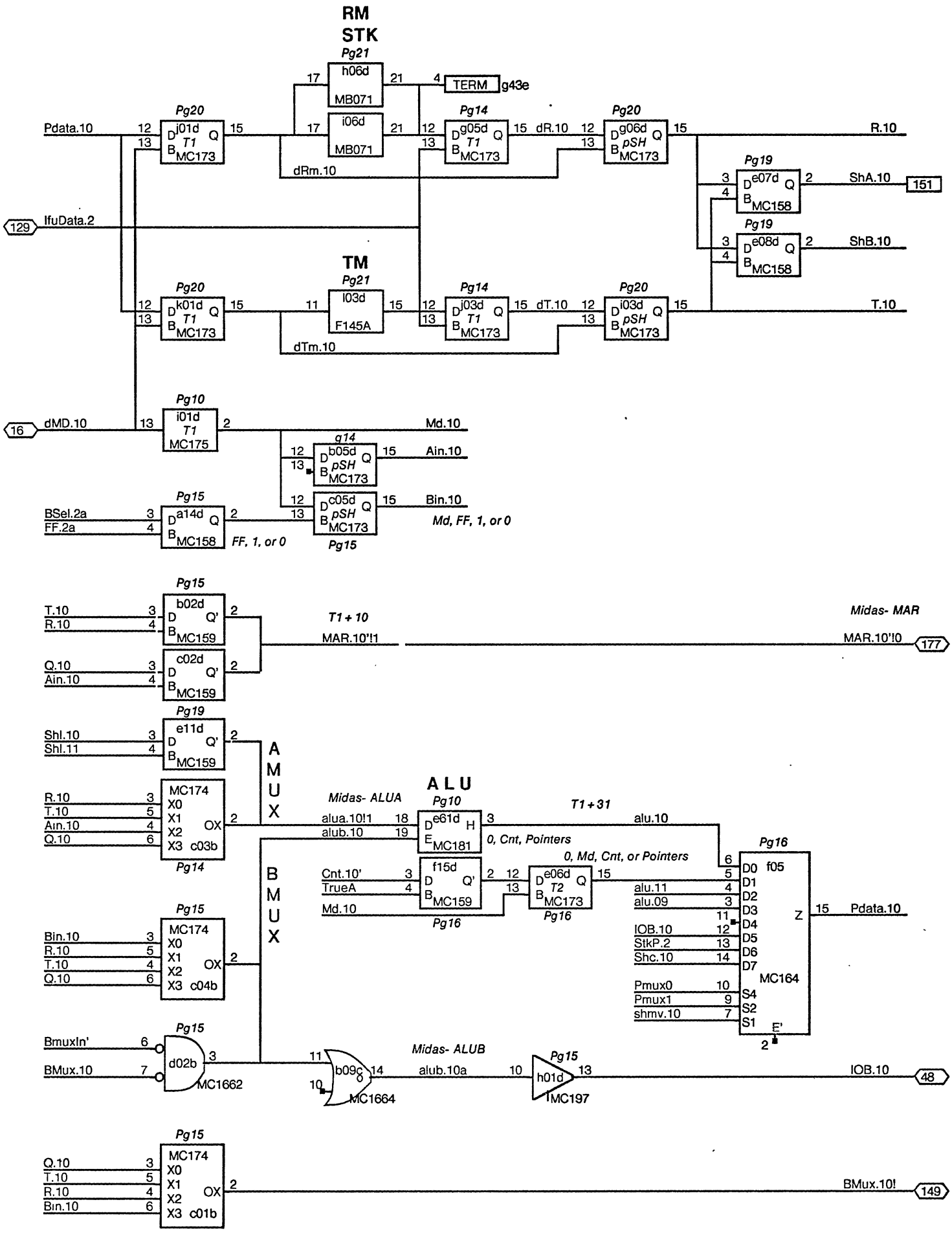
XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Block Diagram	ProcL01.sil	R Bates	Ci	6/27/79	01



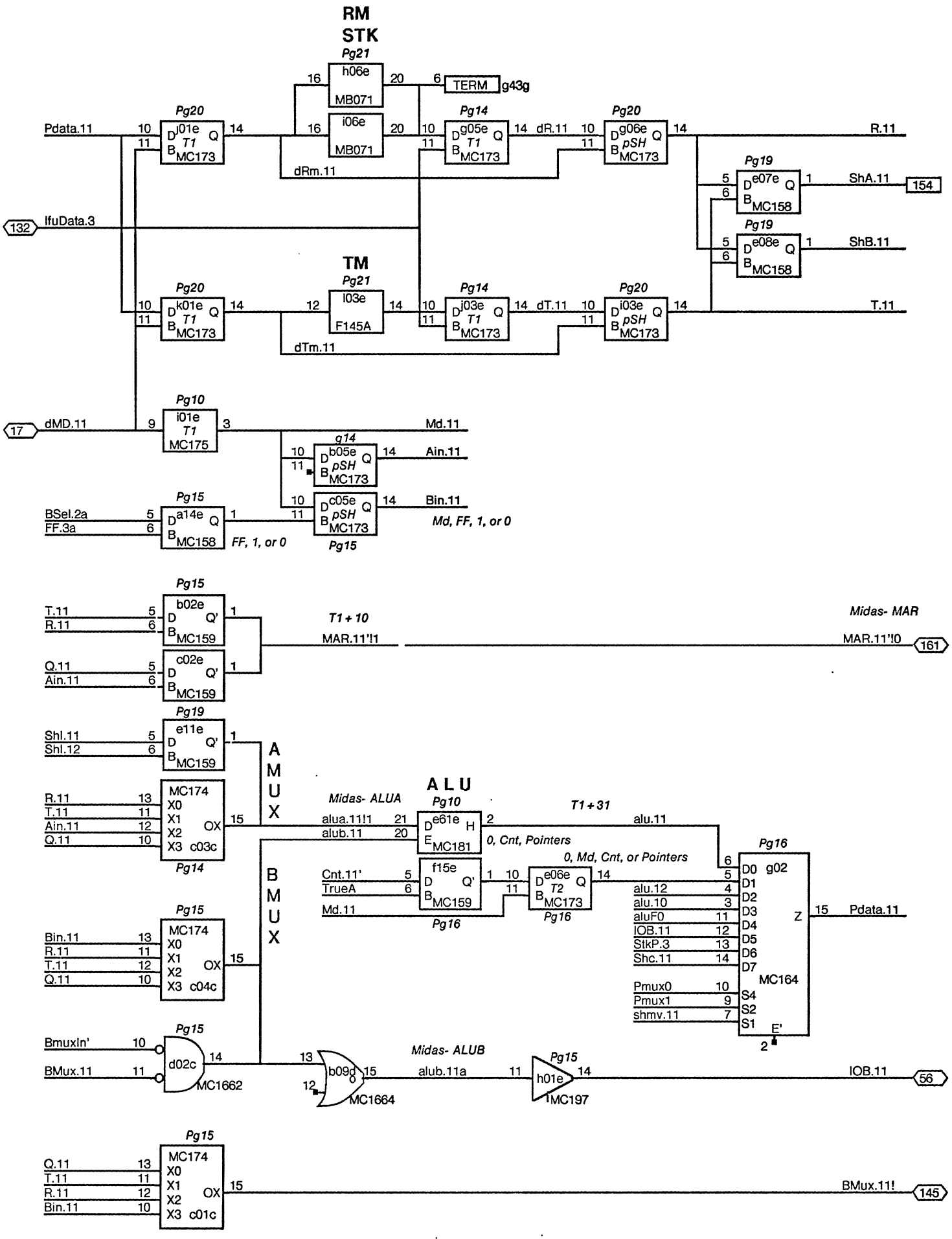
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 08	ProcL02.sil	R Bates	Ci	6/27/79	02



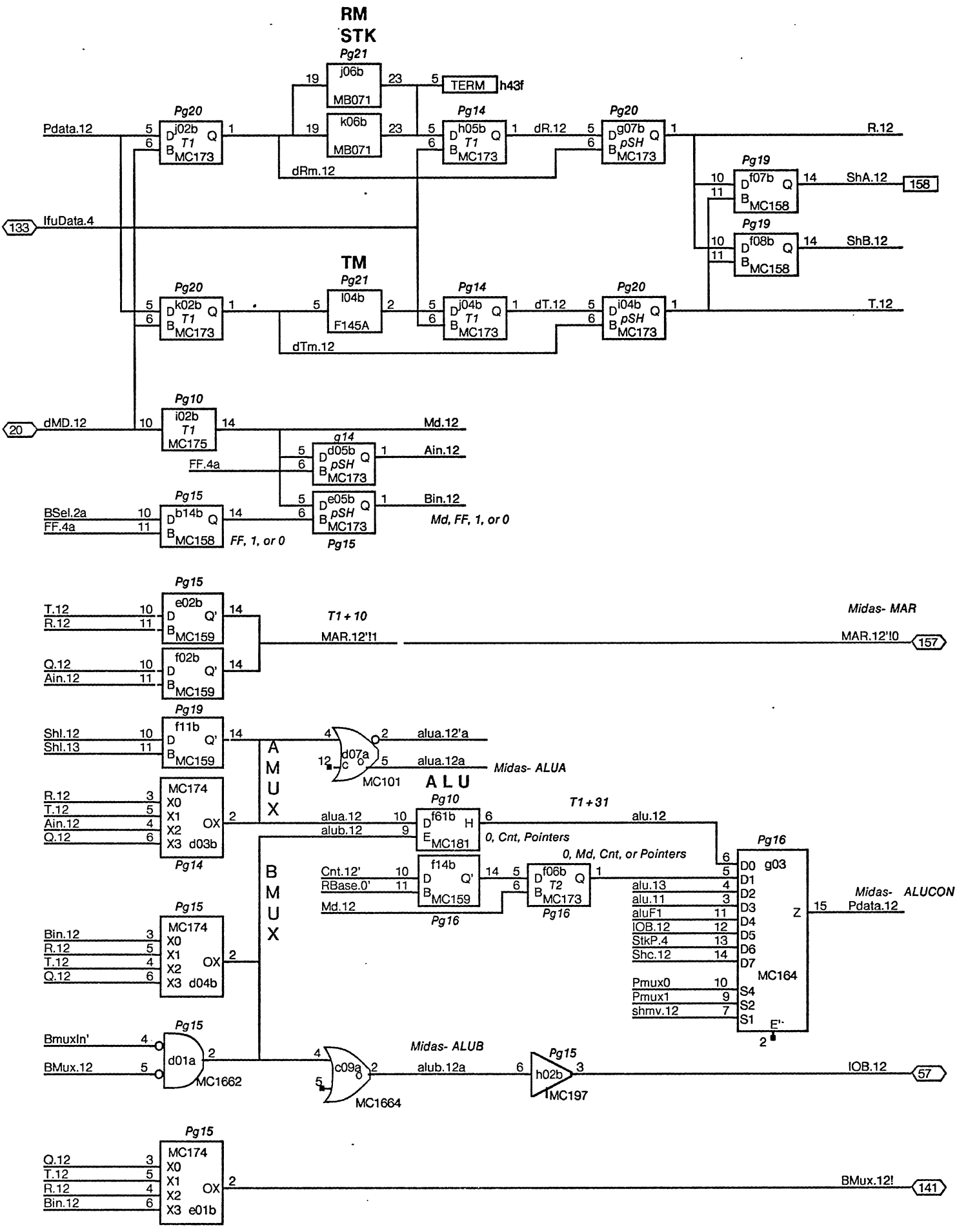
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 09	ProcL03.sil	R Bates	Ci	6/27/79	03



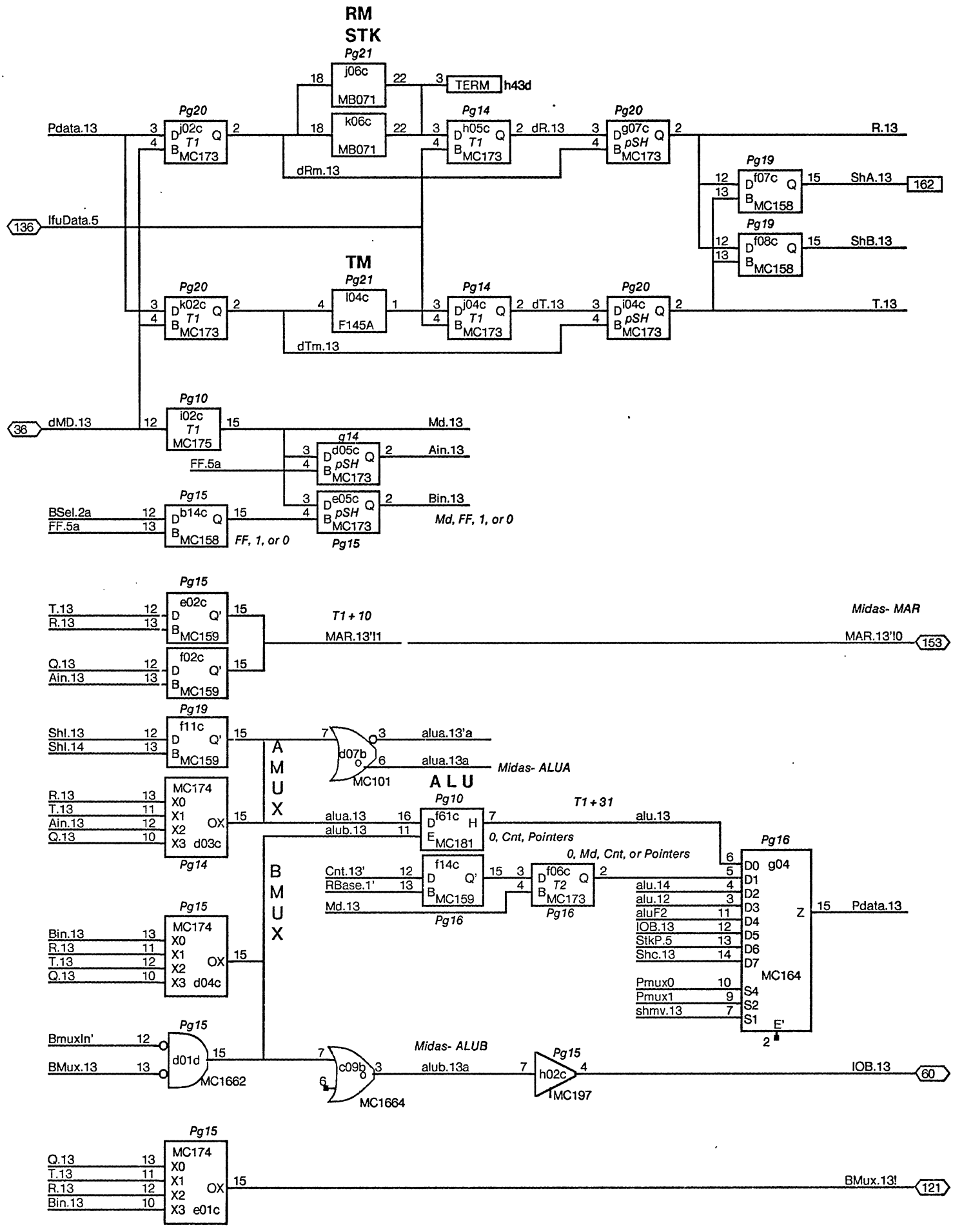
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 10	ProcL04.sil	R Bates	Ci	6/27/79	04



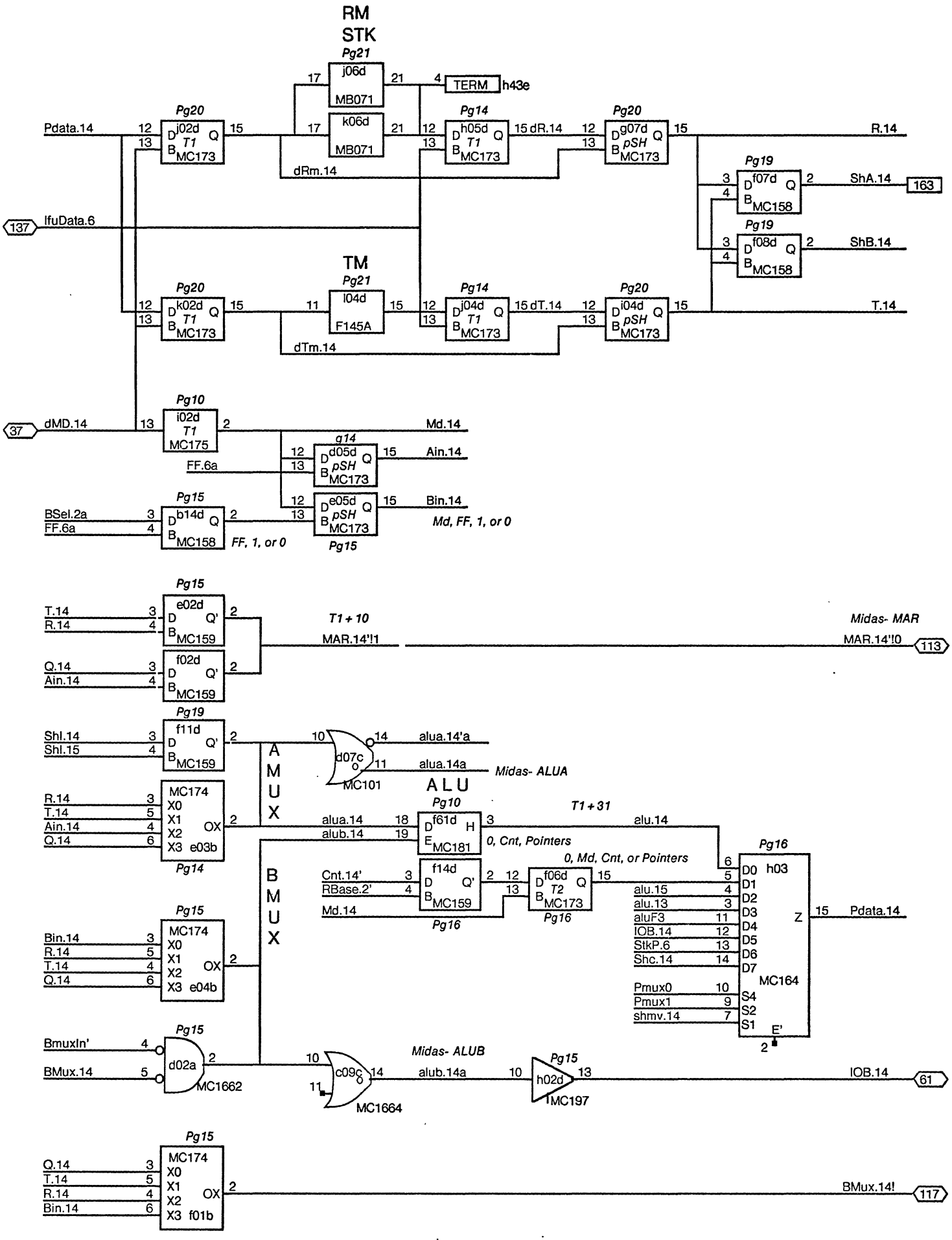
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 11	ProcL05.sil	R Bates	Ci	6/27/79	05



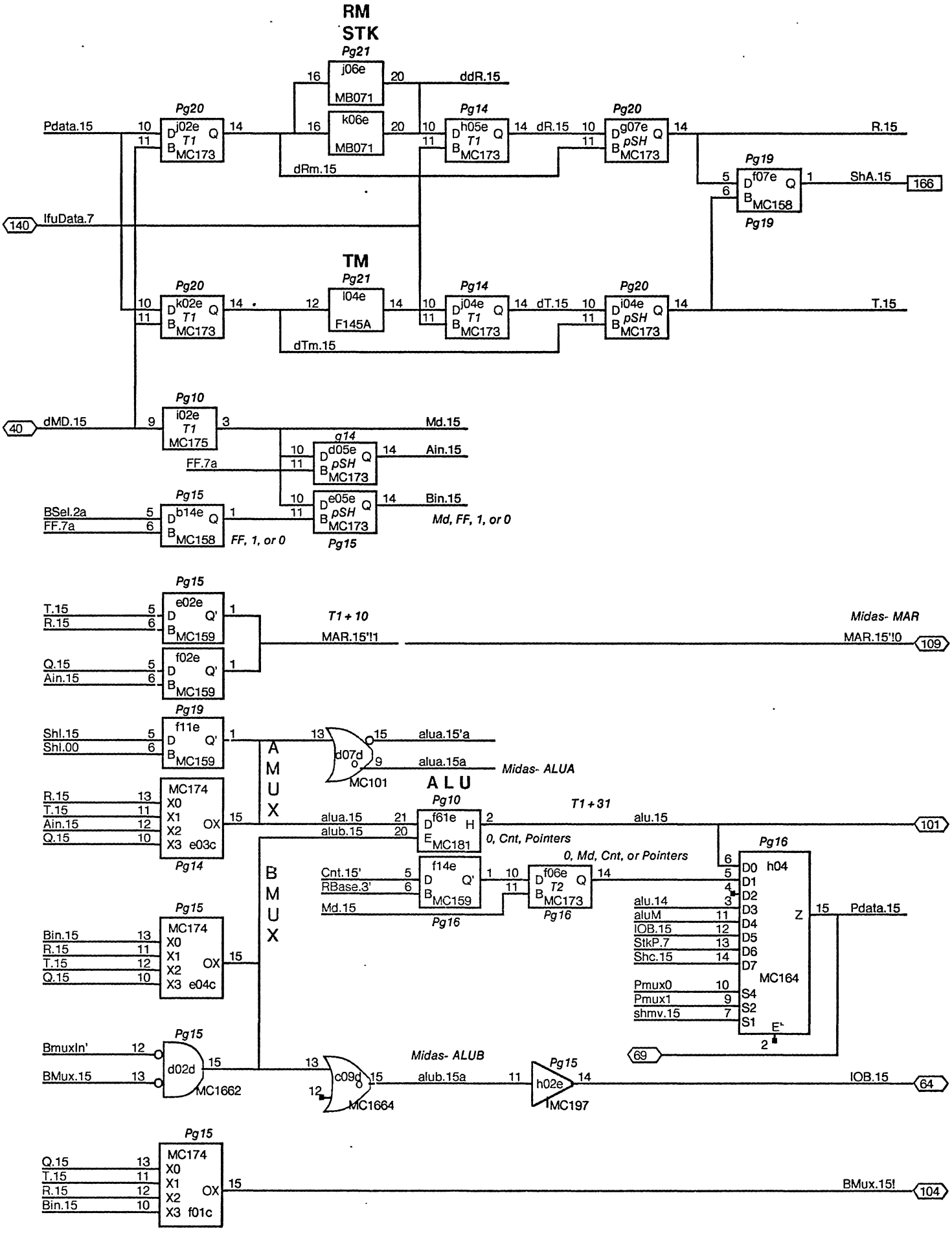
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 12	ProcL06.sil	R Bates	Ci	6/27/79	06



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 13	ProcL07.sil	R Bates	Ci	6/27/79	07



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 14	ProcL08.sil	R Bates	Ci	6/08/79	08



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 15	ProcL09.sil	R Bates	Ci	6/27/79	09

ALU delays

Logical function to output = 11.9

Arithmetic operation to data = 20.0

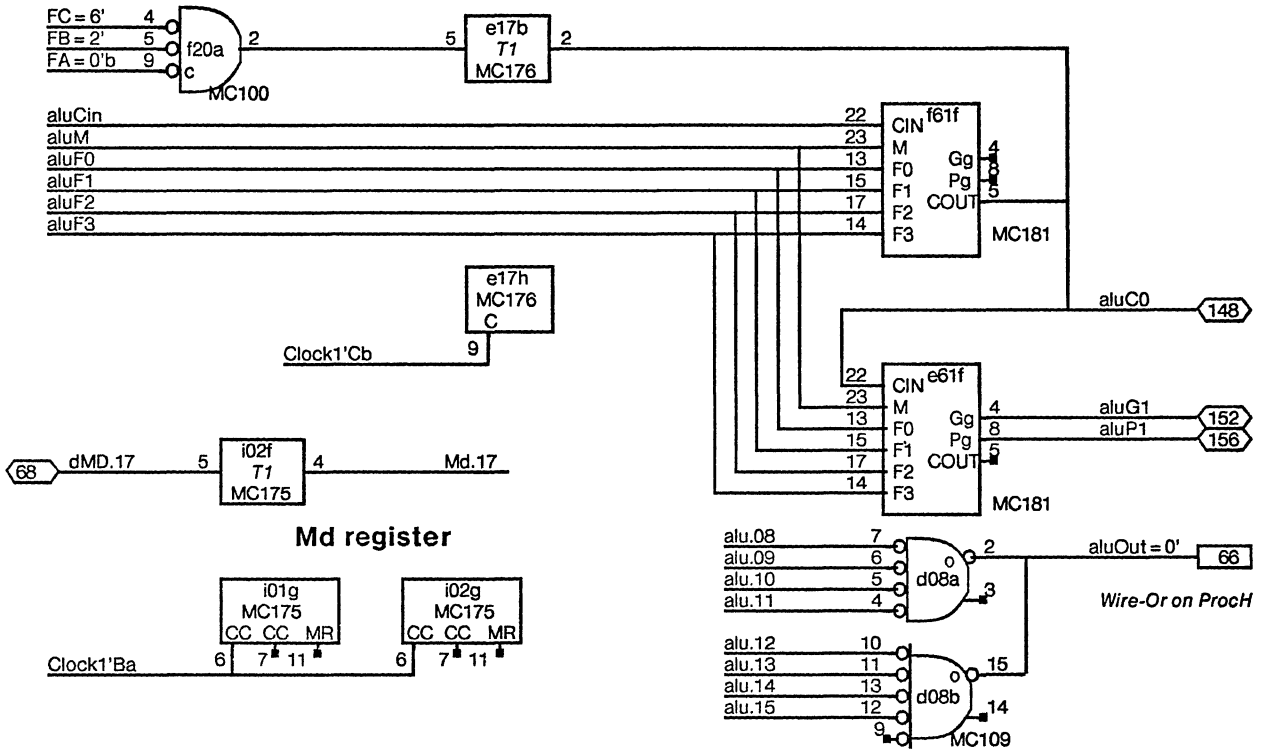
Arithmetic operation to carry = 17.9

ALU output *(assuming 10.2 ns to output of BMux)*

Logical Function = 22.0

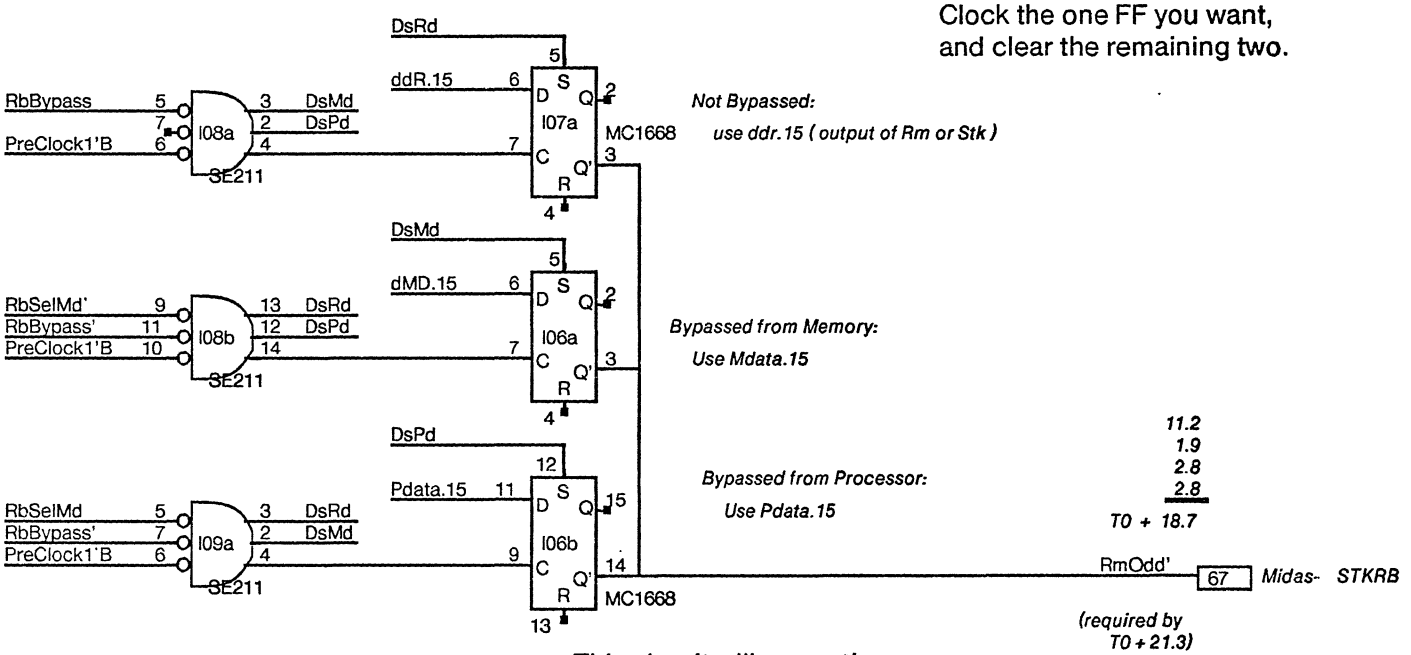
Arithmetic operation to data = 30.1

Arithmetic operation to carry = 28.0



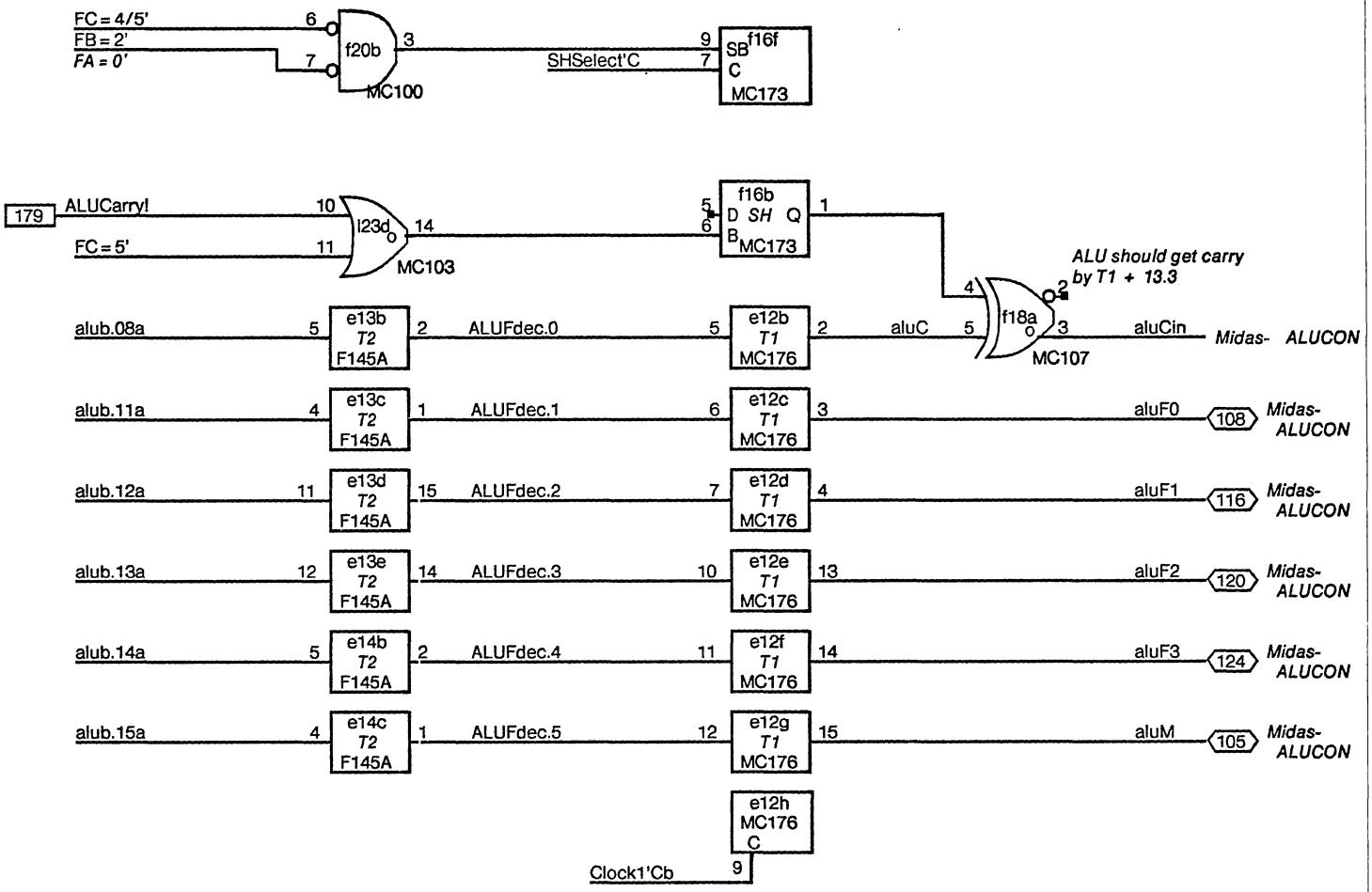
Fast Branch on Rm odd

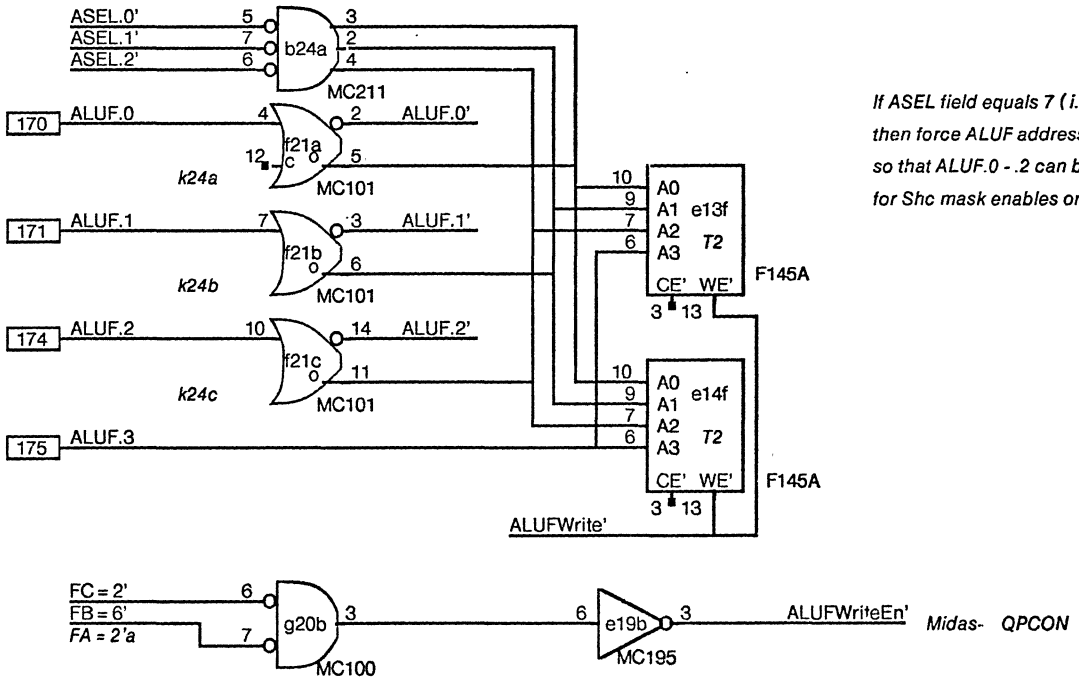
Clock the one FF you want, and clear the remaining two.



This circuit will correctly bypass R from Pdata or Mdata When "RIsIfData" is in effect, the fast branch will be based on the contents of the addressed RM or STK, bypassed if necessary.

FF = Cin xor 1
or
FF = Cin xor Cout

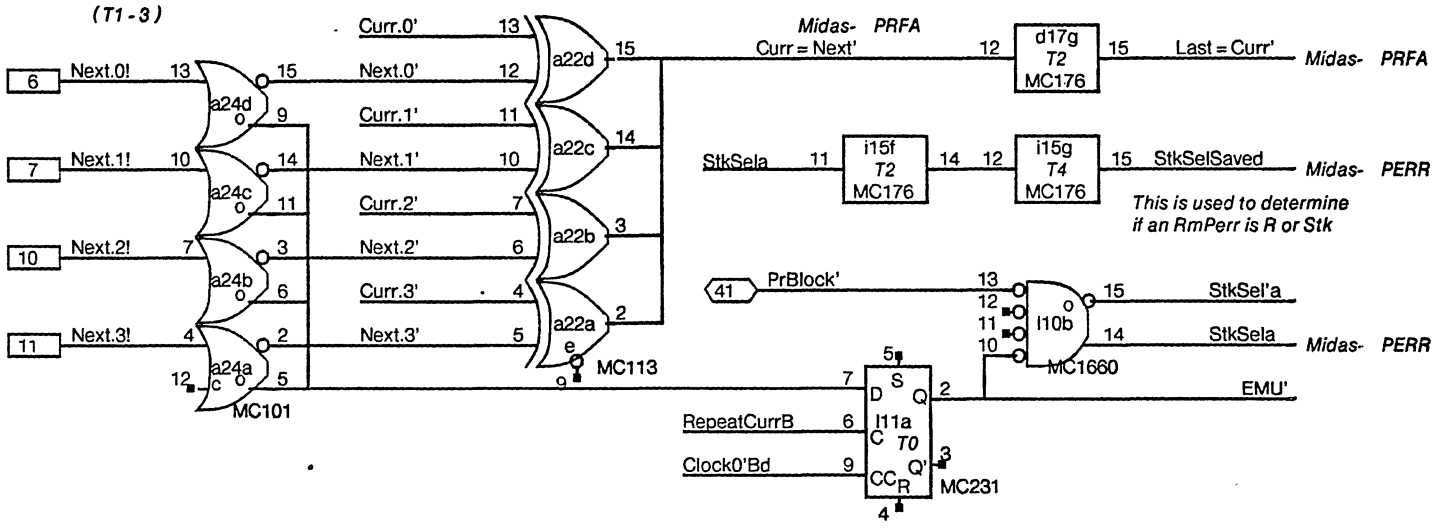


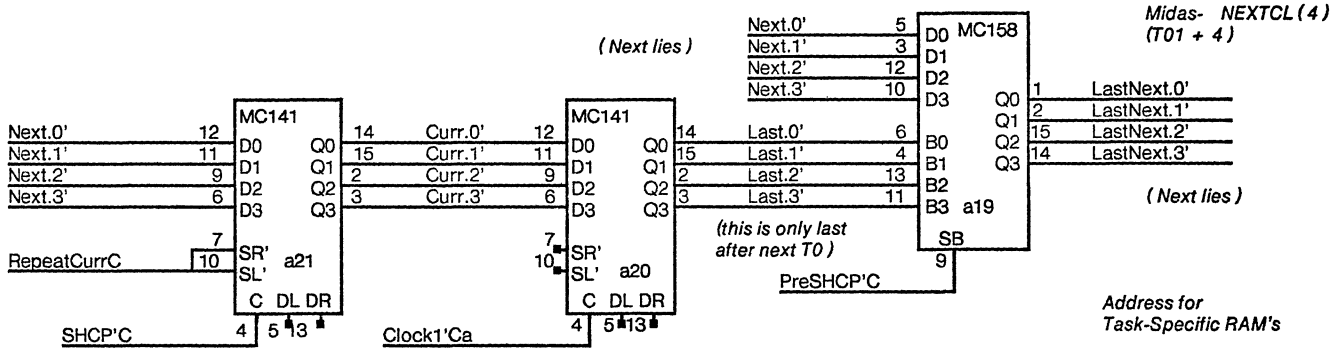


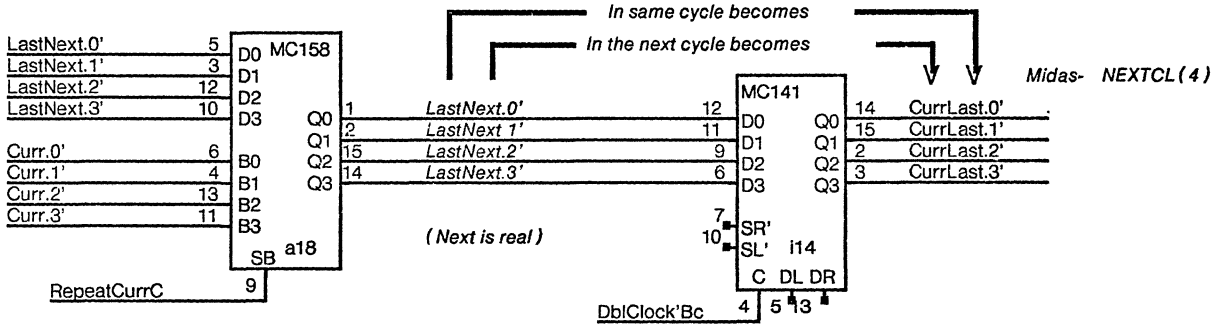
If ASEL field equals 7 (i.e. Shift)
then force ALUF address to 16 or 17
so that ALUF.0 - .2 can be used
for Shc mask enables on page 17

NOTE: Moving k24 to f21 saves 0.4 ns

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	ALU FUNCTION RAM	ProcL11.sil	R Bates	Ci	6/27/79	11



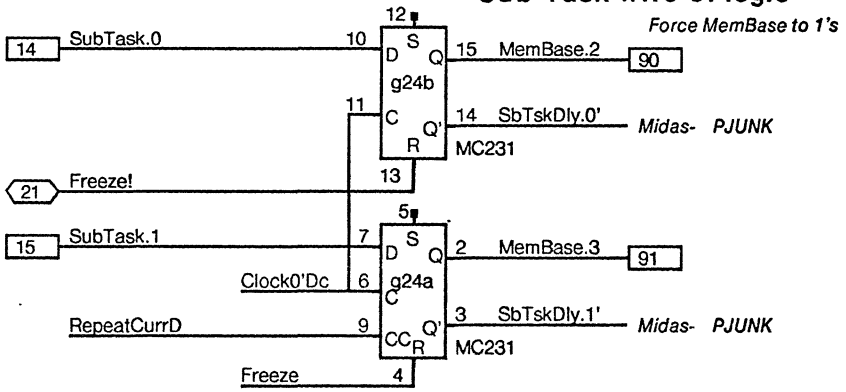




"RepeatCurrent" is asserted on certain occasions when the value on the NEXT bus may be invalid ("Next Lies") due to the combination of Block and Hold.

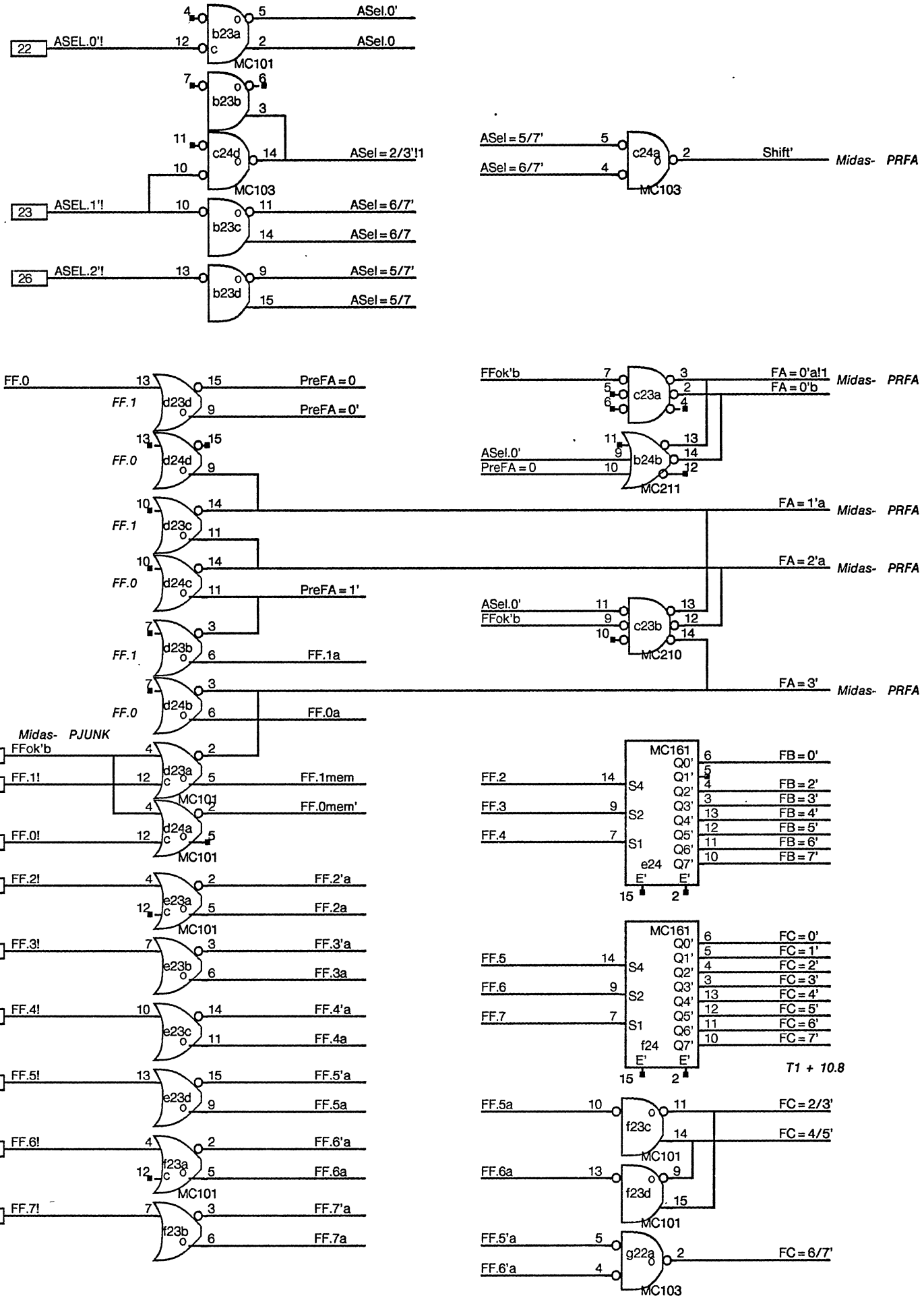
Task number tracking logic

Sub-Task wire-or logic



RBase is forces to 1's on Pages 24 & 25

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Task logic	ProcL12.sil	R. Bates	Ci	6/27/79	12



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Function Field Decoding	ProcL13.sil	R Bates	Ci	6/27/79	13

AMux decoding

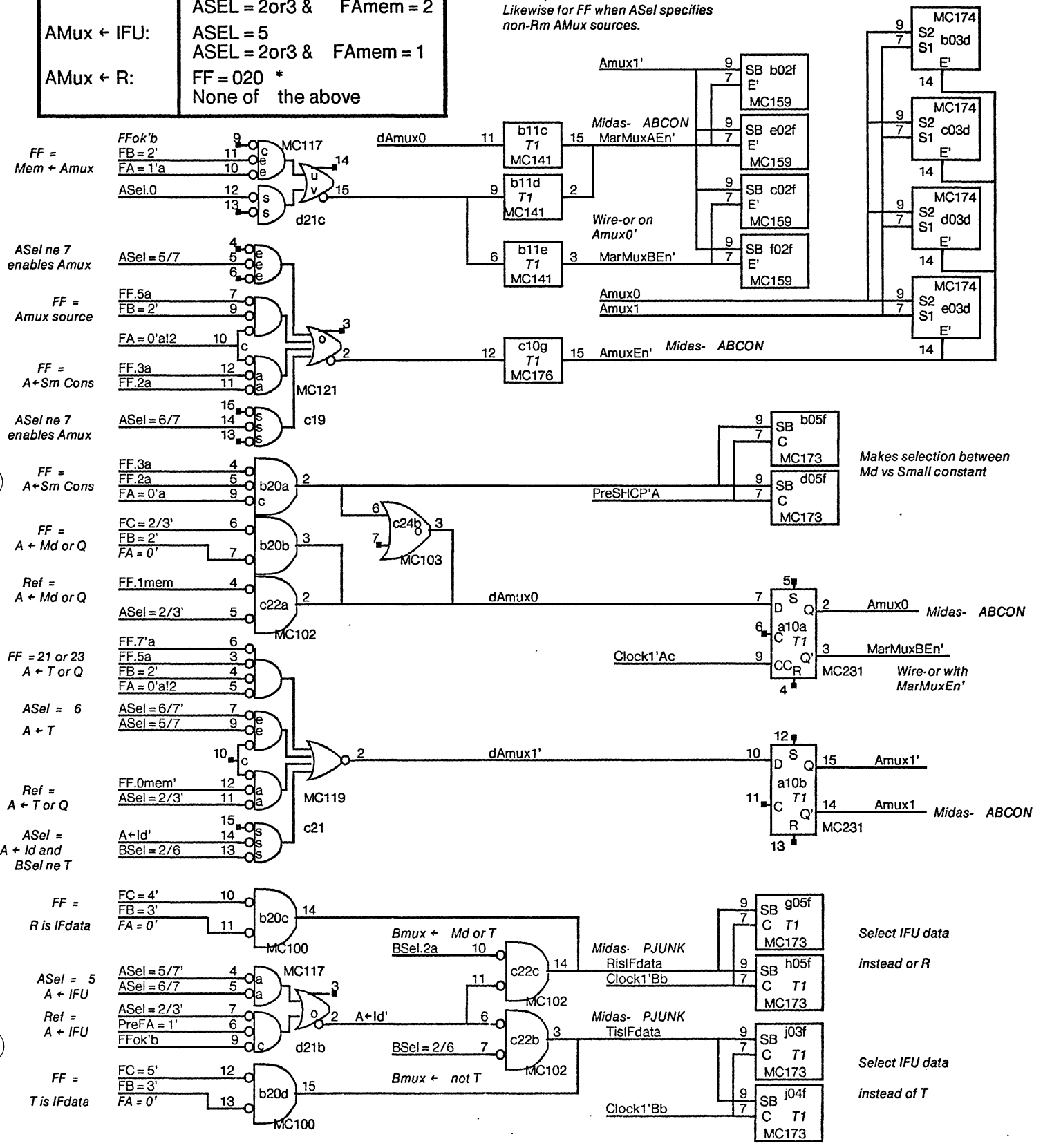
AMux ← FF:	FF = 0-17 *
AMux ← T:	FF = 021 * ASEL = 2or3 & FAmem = 3 ASEL = 6
AMux ← Md:	FF = 022 * ASEL = 2or3 & FAmem = 0
AMux ← Q:	FF = 023 * ASEL = 2or3 & FAmem = 2
AMux ← IFU:	ASEL = 5 ASEL = 2or3 & FAmem = 1
AMux ← R:	FF = 020 * None of the above

* The Amux is disabled by ASEL = 7 unless one of these codes are in effect

NOTE: ASel selects and FF selects for the AMux are "OR'd" by this hardware. Thus ASel codes selecting non-Rm sources of Amux must not be used when an FF specifies an ASel source. Likewise for FF when ASel specifies non-Rm AMux sources.

AMux encoding

Mux Input	Source
0	R or IFU data
1	T or IFU data
2	Md or Small Const.
3	Q



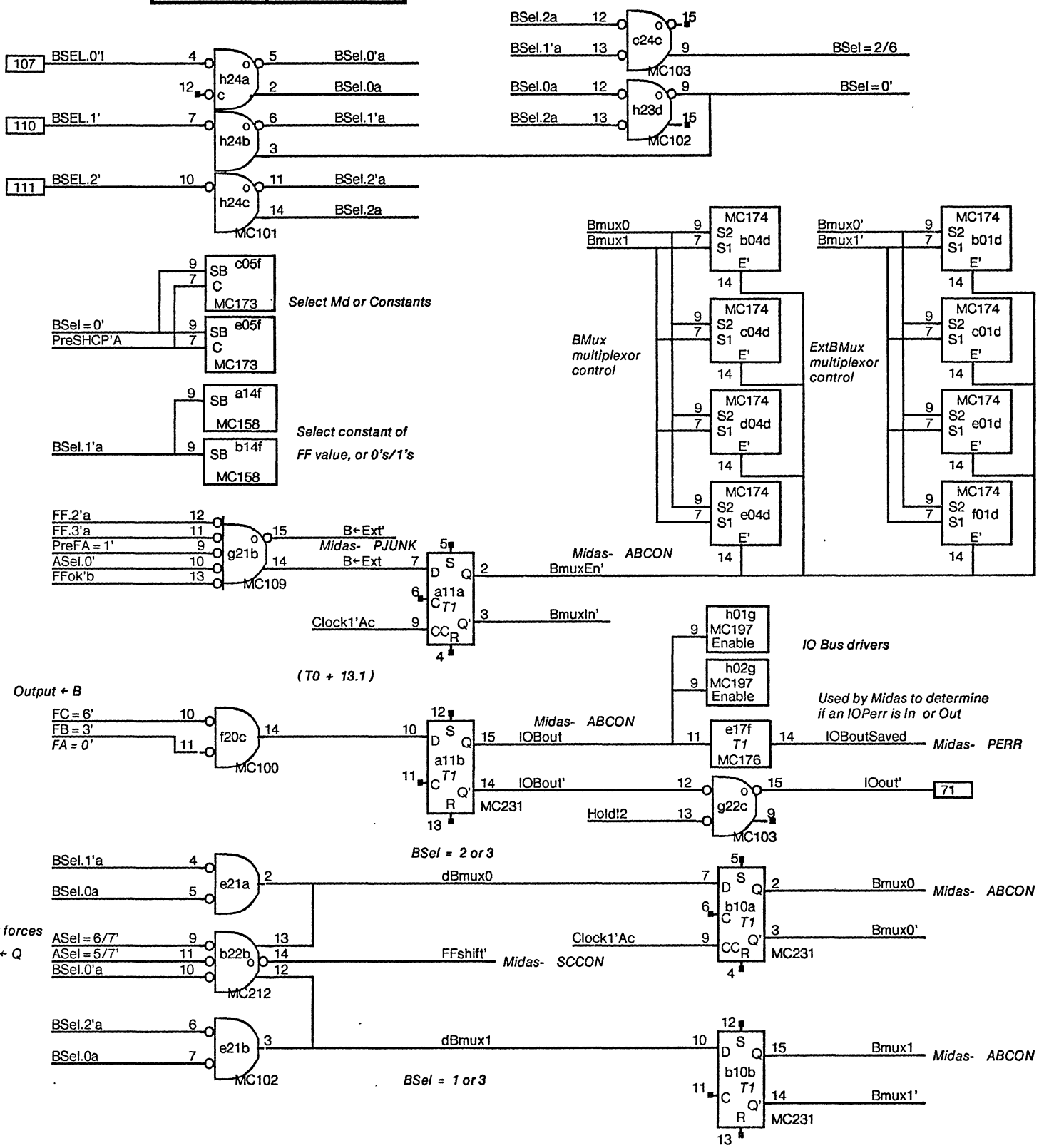
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	"A" Multiplexor Control	ProcL14.sil	R. Bates	Ci	6/27/79	14

BSEL field decoding

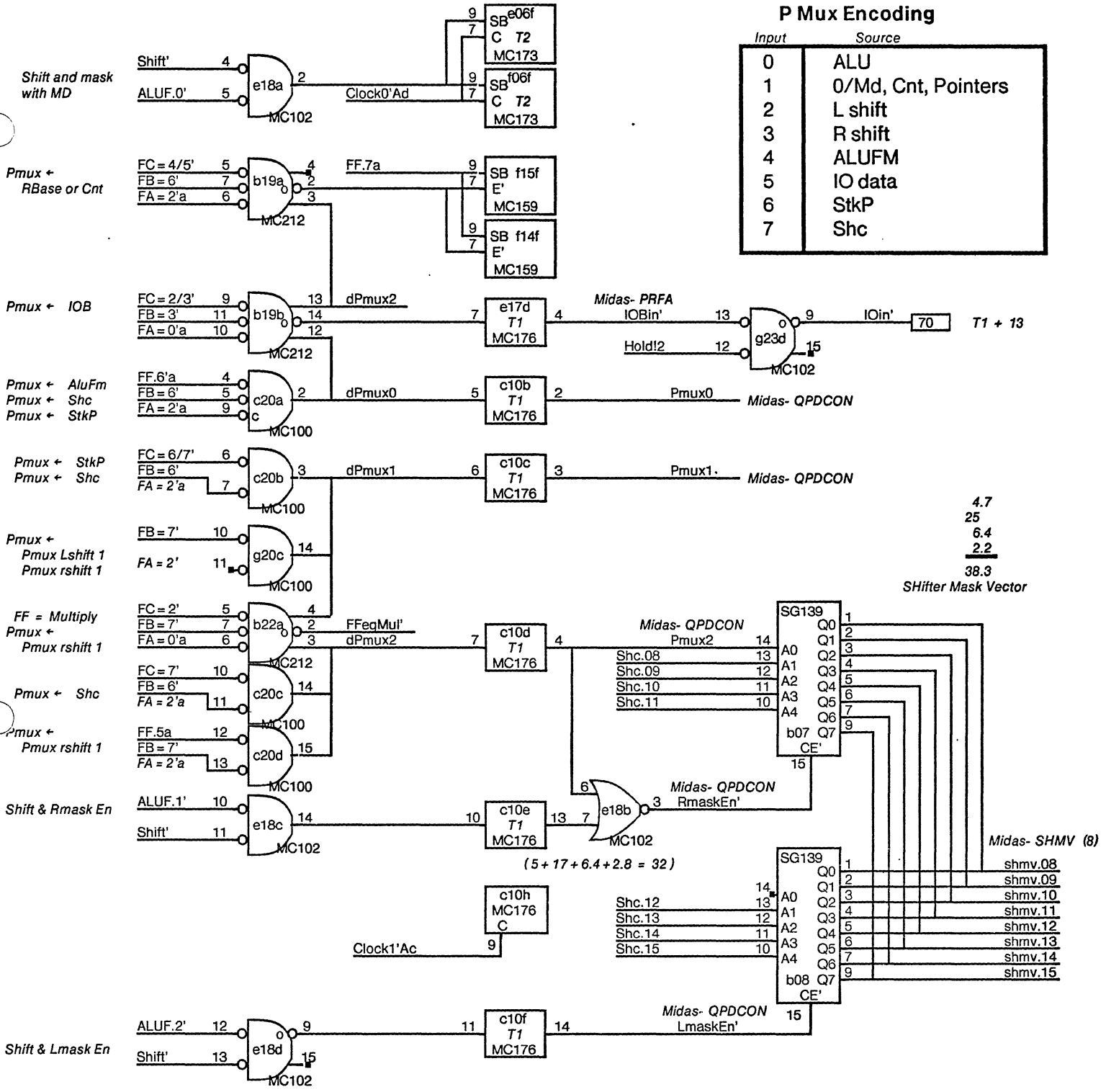
BSEL	INTERNAL	EXTERNAL
0	Md	--
1	R	--
2	T	Hold←B
3	Q	Q ← B
4	0,,FF	--
5	377,FF	--
6	FF,,0	--
7	FF,,377	--

BMux encoding

BMux	
0	Md or Constant
1	R
2	T
3	Q



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	"B" Multiplexor & Cont.	ProcL15.sil	R Bates	Ci	6/27/79	15



NOTE: The prom patterns are designed so that a one into address bit 0 will produce all 1's on the output. This allows the odd address inputs to Pmux to be selected.

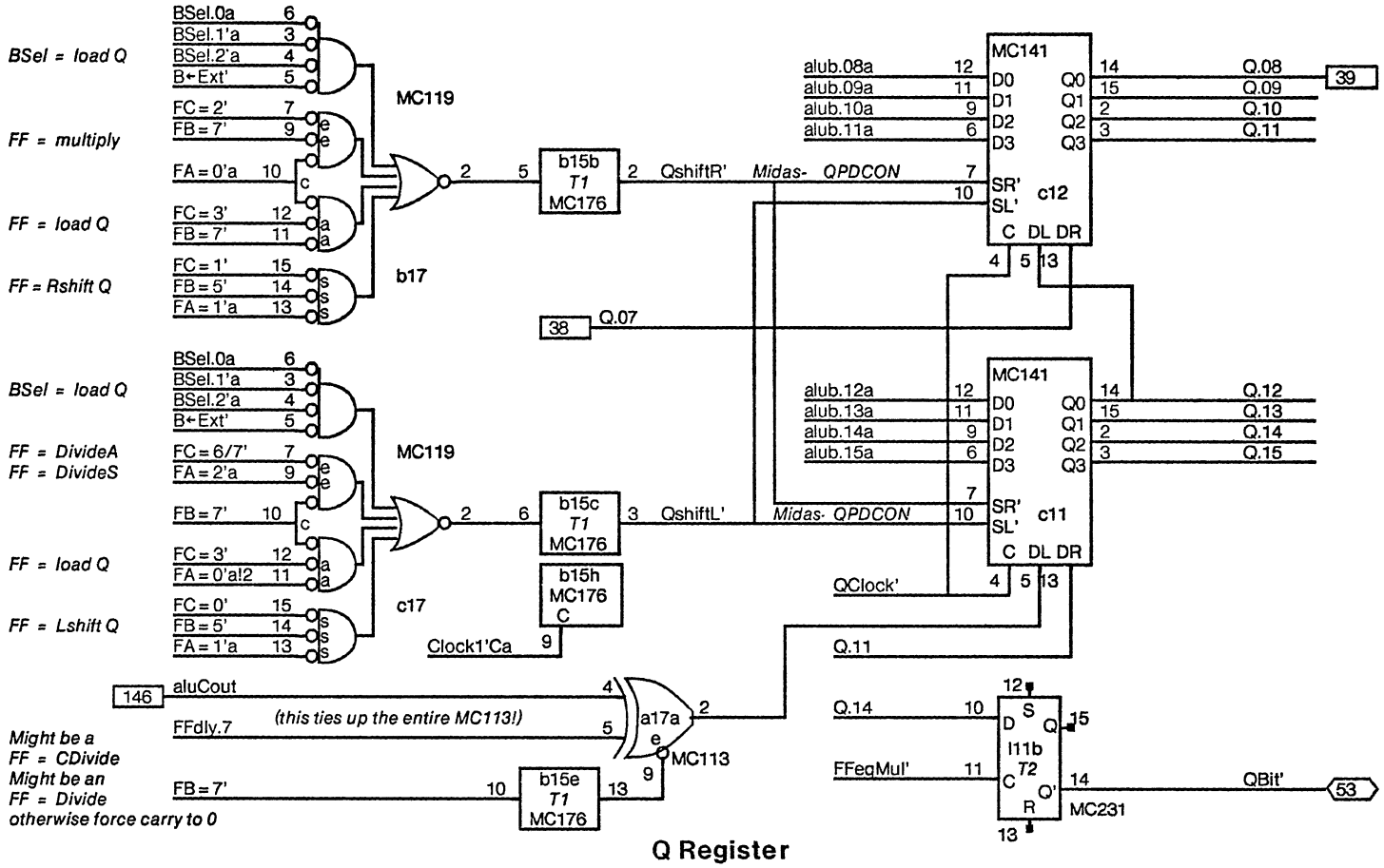
Lmask

Shc.12-15	Shmv bits 08	09	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
11	1	0	0	0	0	0	0	0
12	1	1	0	0	0	0	0	0
13	1	1	1	0	0	0	0	0
14	1	1	1	1	0	0	0	0
15	1	1	1	1	1	0	0	0
16	1	1	1	1	1	1	0	0
17	1	1	1	1	1	1	1	0
20- 37	1	1	1	1	1	1	1	1

Rmask

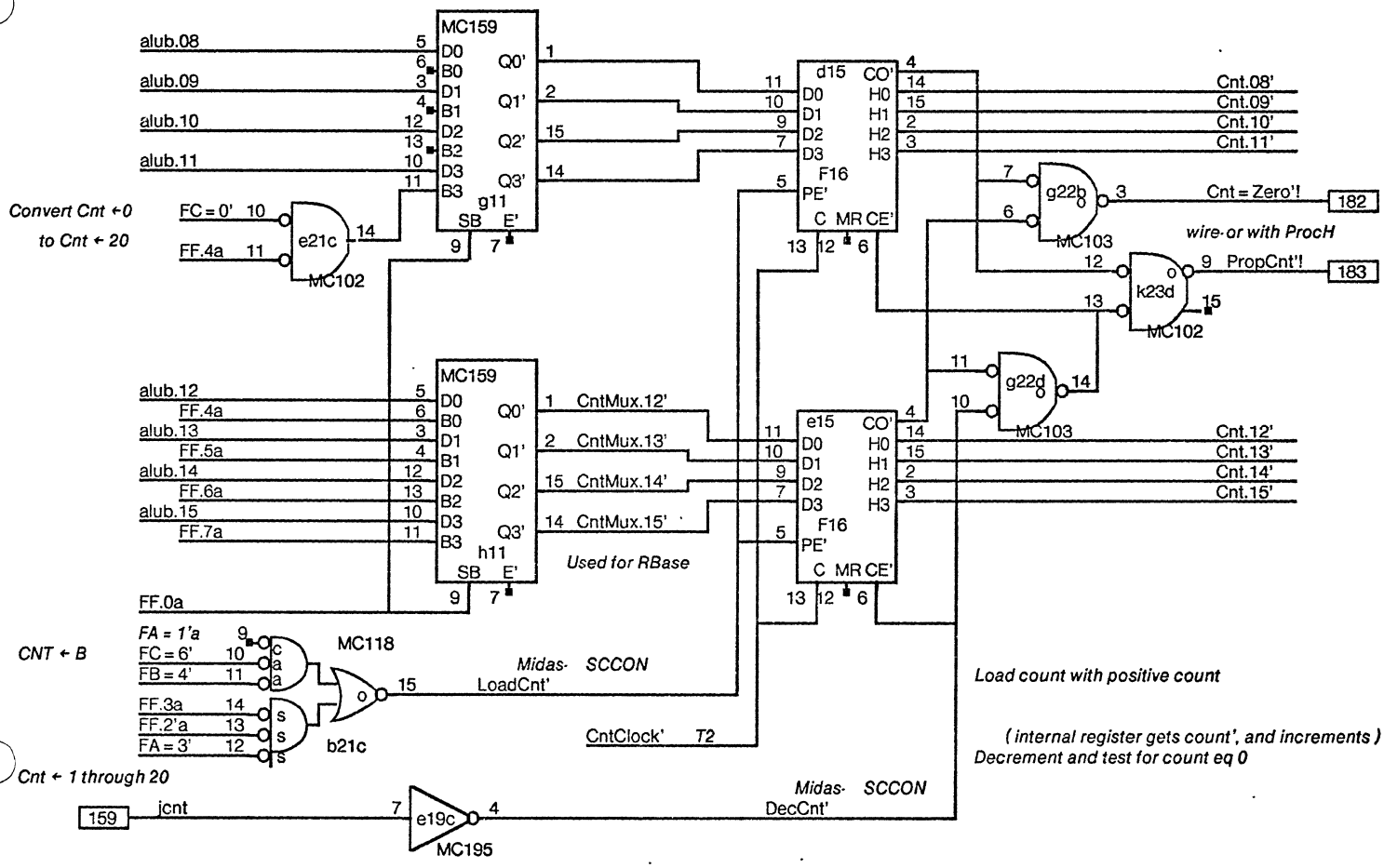
Shc.08-11	Shmv bits 08	09	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	1
3	0	0	0	0	0	1	1	1
4	0	0	0	0	1	1	1	1
5	0	0	0	1	1	1	1	1
6	0	0	1	1	1	1	1	1
7	0	1	1	1	1	1	1	1
10	1	1	1	1	1	1	1	1
11	1	1	1	1	1	1	1	1
12	1	1	1	1	1	1	1	1
13	1	1	1	1	1	1	1	1
14	1	1	1	1	1	1	1	1
15	1	1	1	1	1	1	1	1
16	1	1	1	1	1	1	1	1
17	1	1	1	1	1	1	1	1
20- 37	1	1	1	1	1	1	1	1

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Proc Multiplexor & Shift mask Prom	ProcL16.sil	R Bates	Ci	6/27/79	16

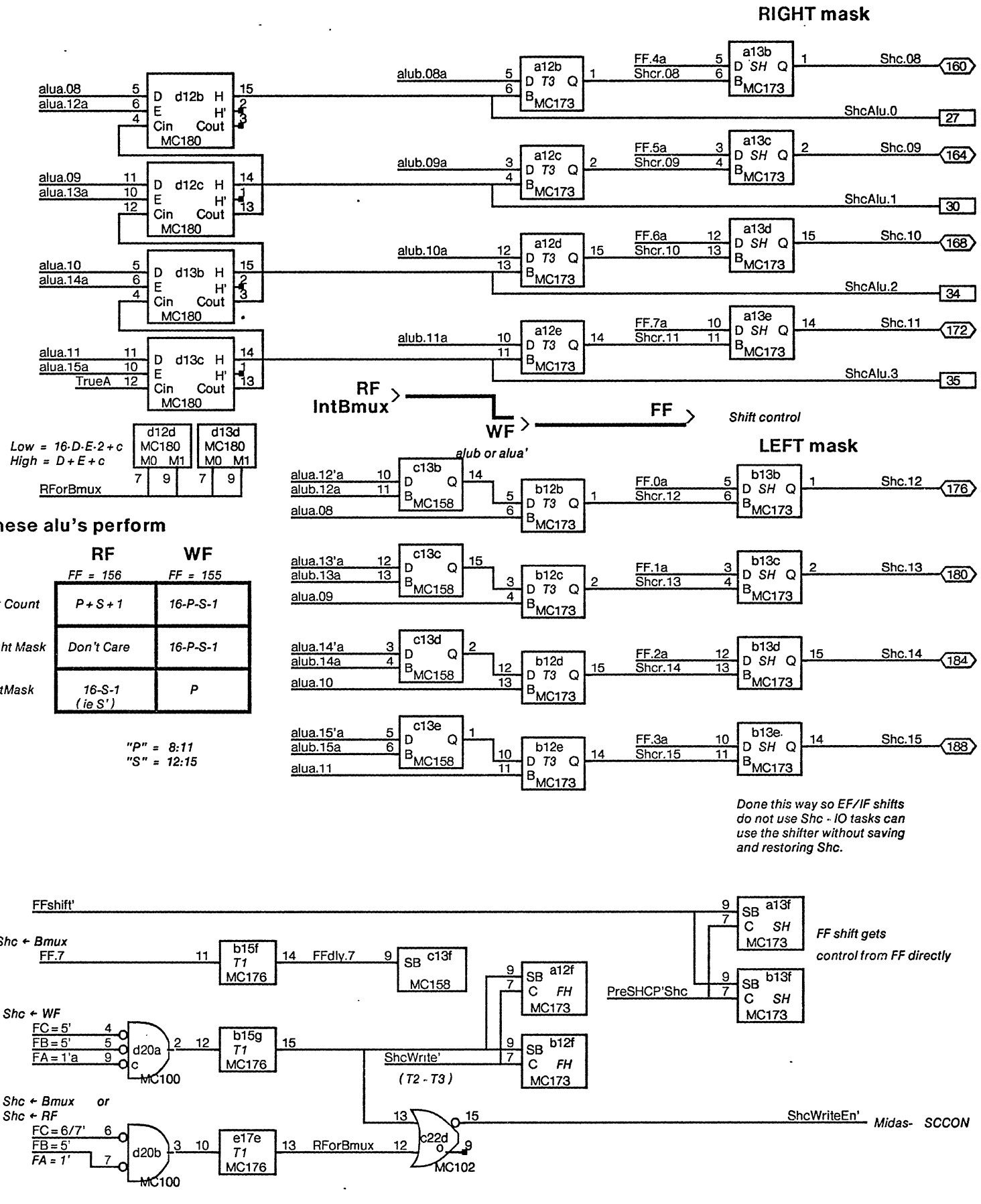


Q Register

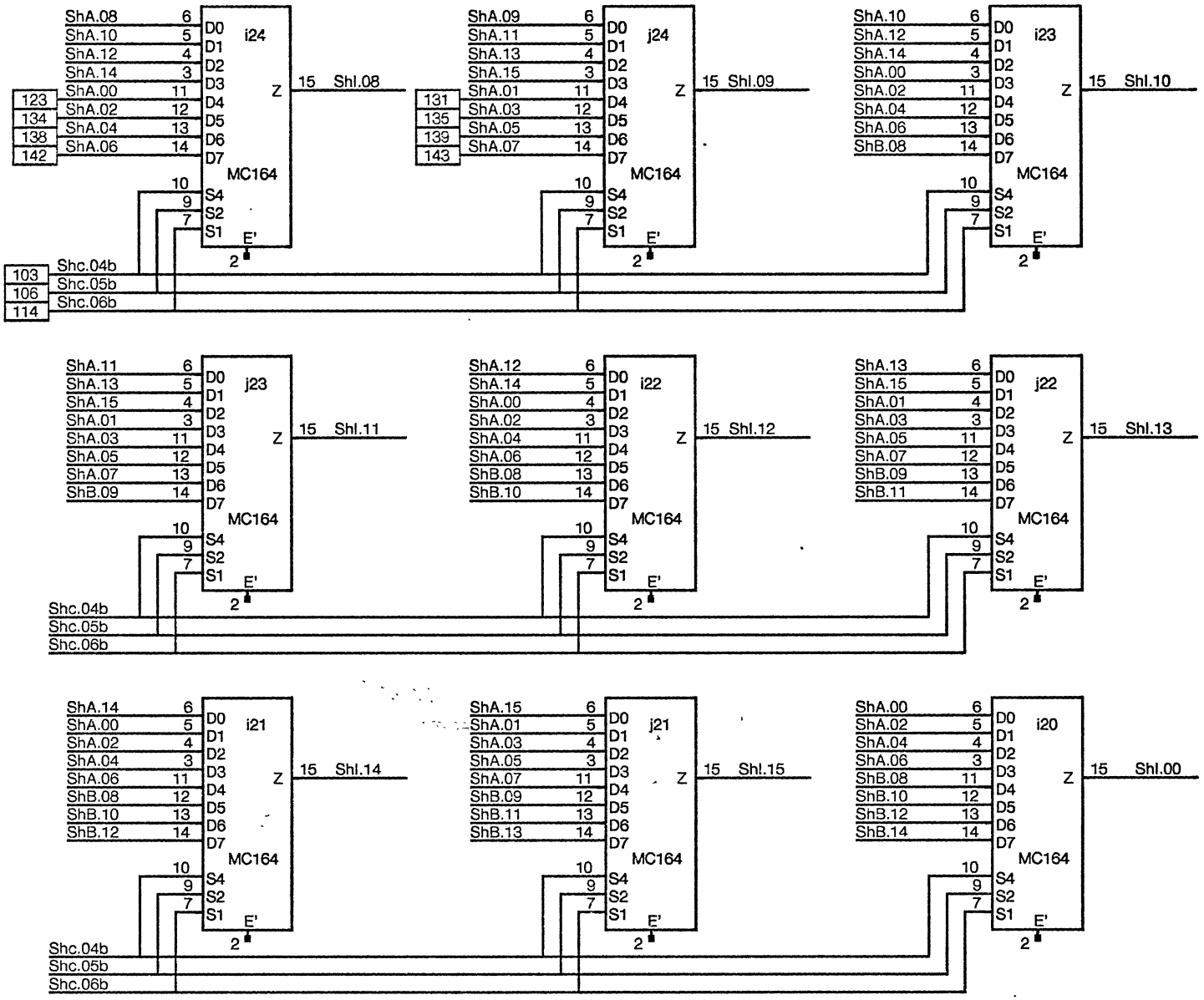
Count Register

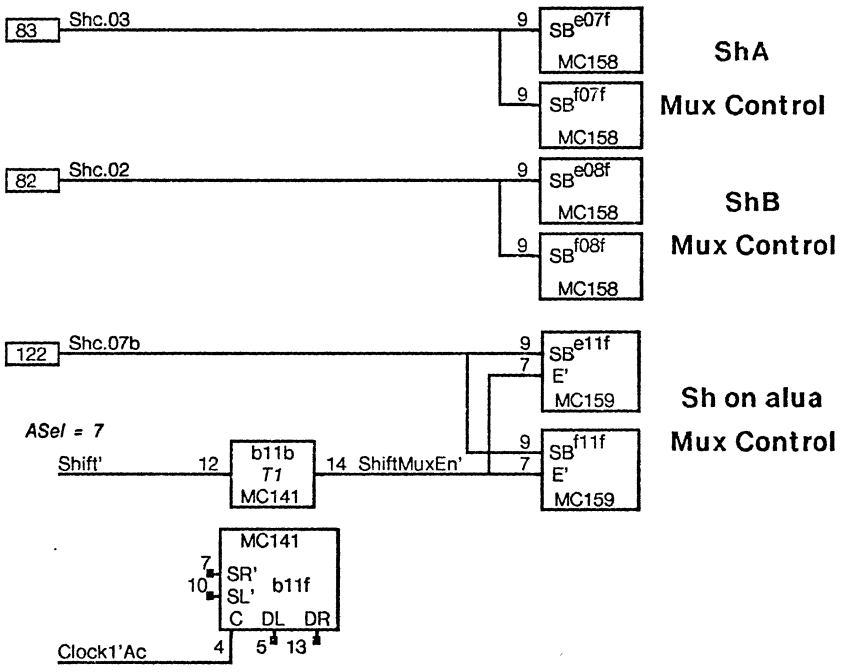


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Q Register and Task Simulator	ProcL17.sil	R Bates	Ci	6/27/79	17

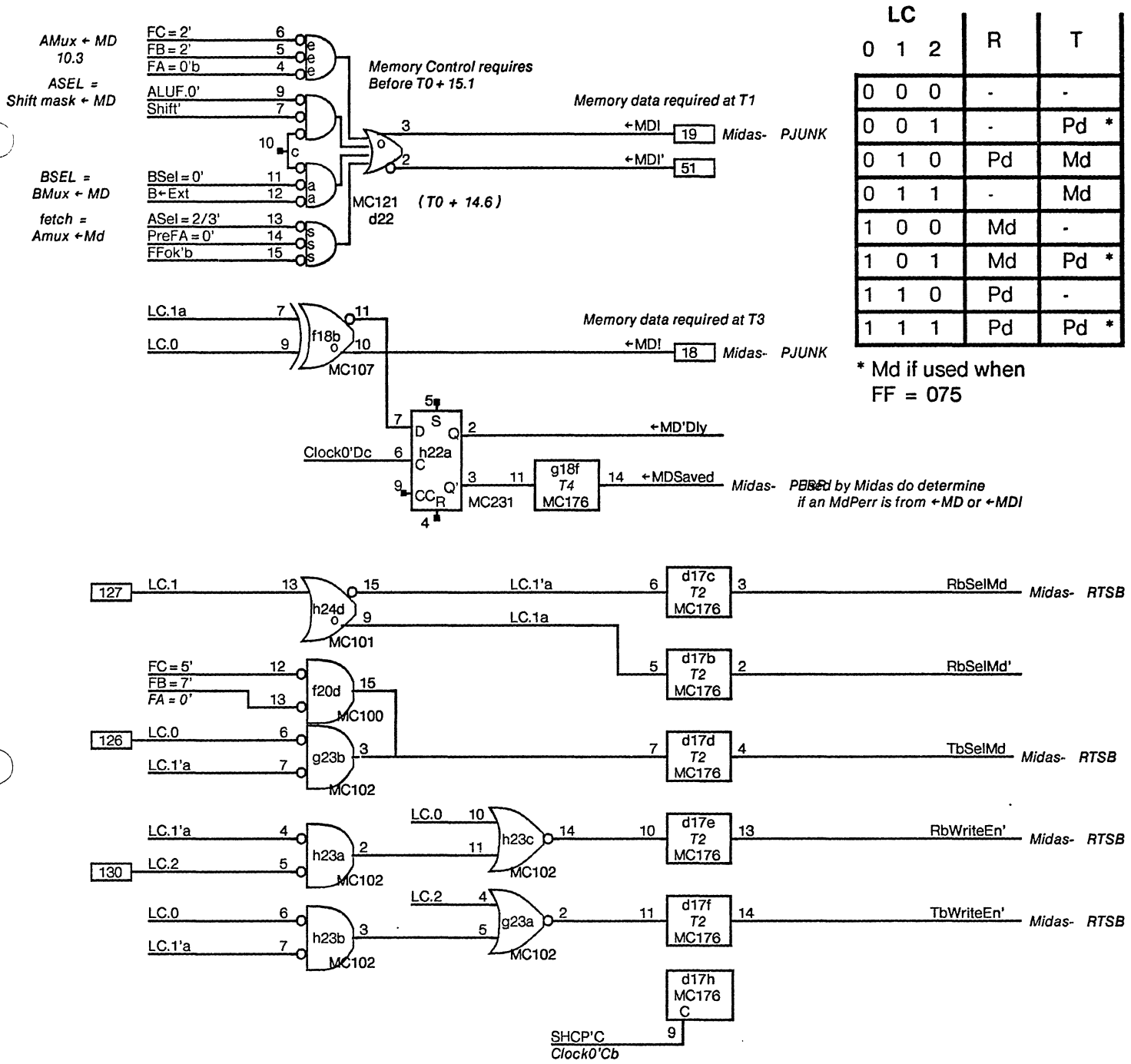


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Shift Register Control	ProcL18.sil	R Bates	Ci	6/27/79	18



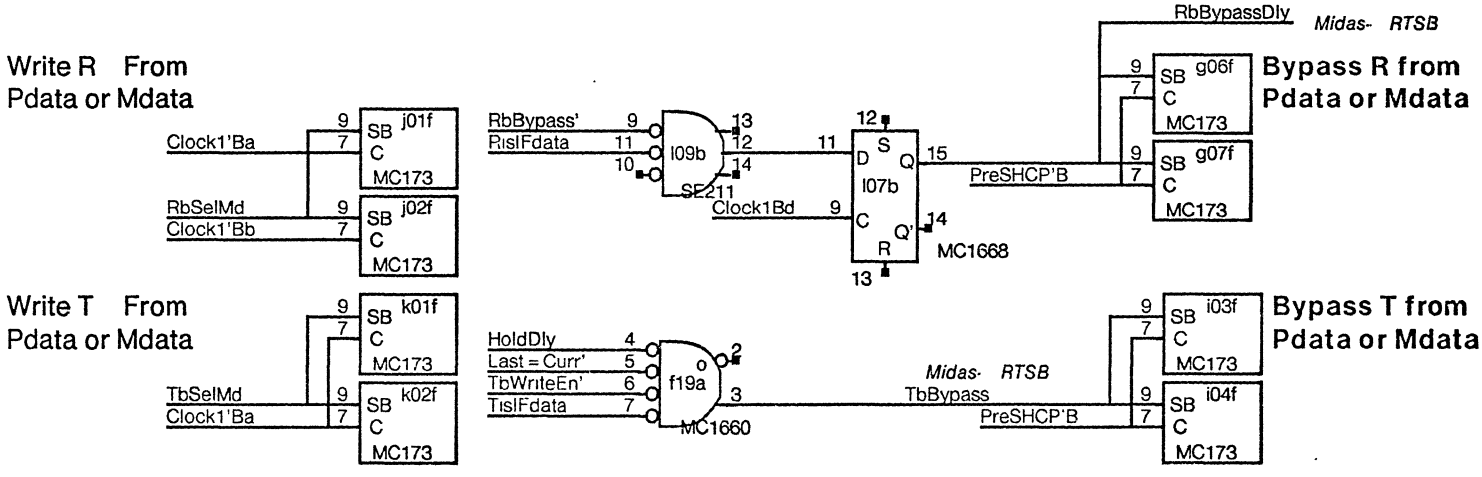


Shc.02	Shc.03	Shc.04 - .07
0	0	16 bit Left cycle of R
0	1	16 bit Left cycle of R,,T
1	0	16 bit Left cycle of T,,R
1	1	16 bit Left cycle of T

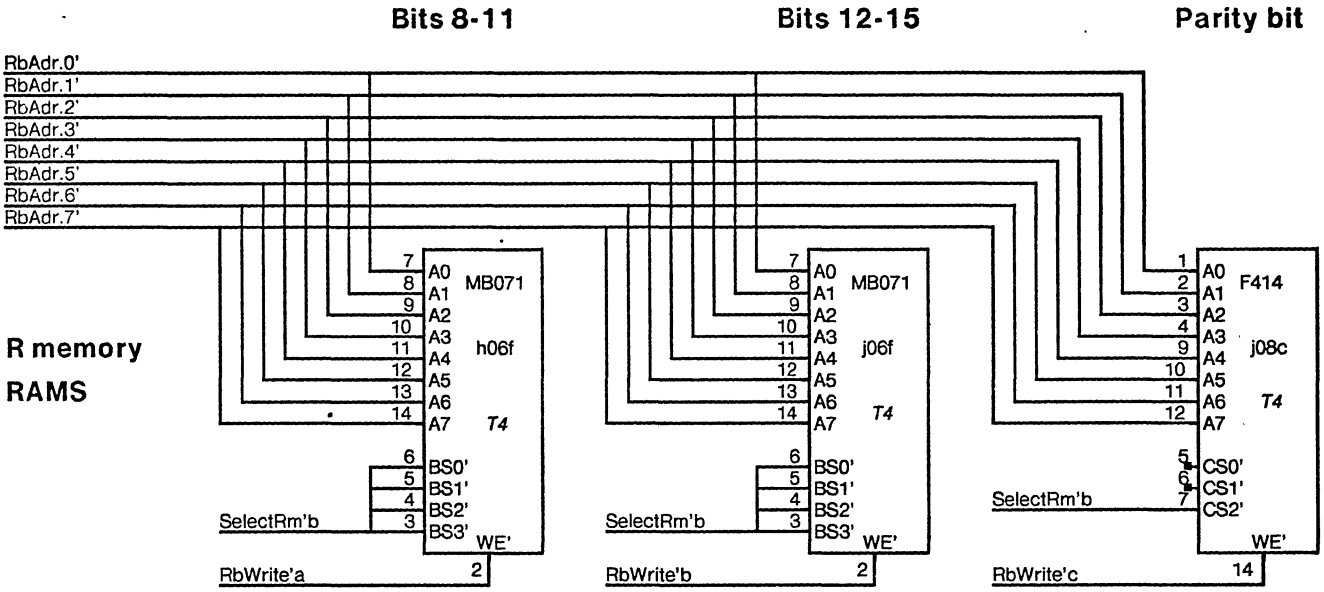


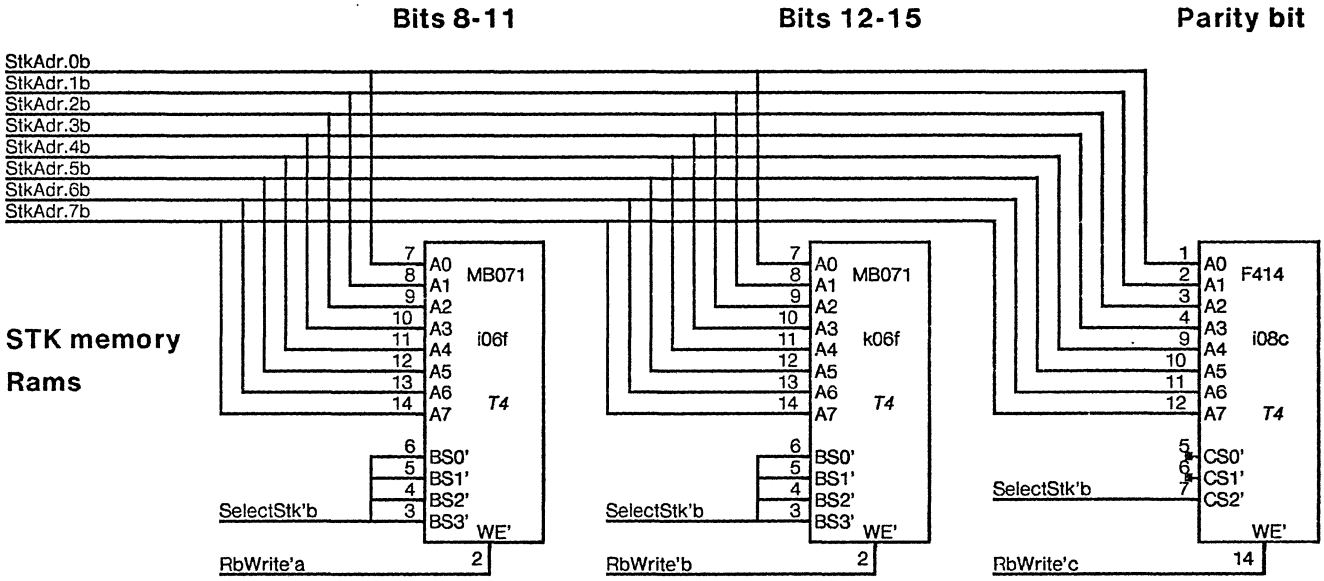
LC 0	LC 1	LC 2	R	T
0	0	0	-	-
0	0	1	-	Pd *
0	1	0	Pd	Md
0	1	1	-	Md
1	0	0	Md	-
1	0	1	Md	Pd *
1	1	0	Pd	-
1	1	1	Pd	Pd *

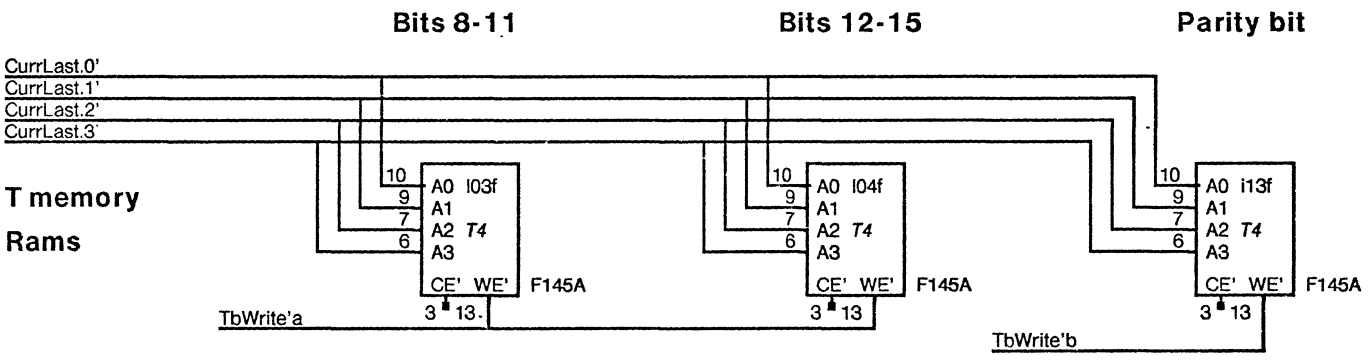
* Md if used when FF = 075



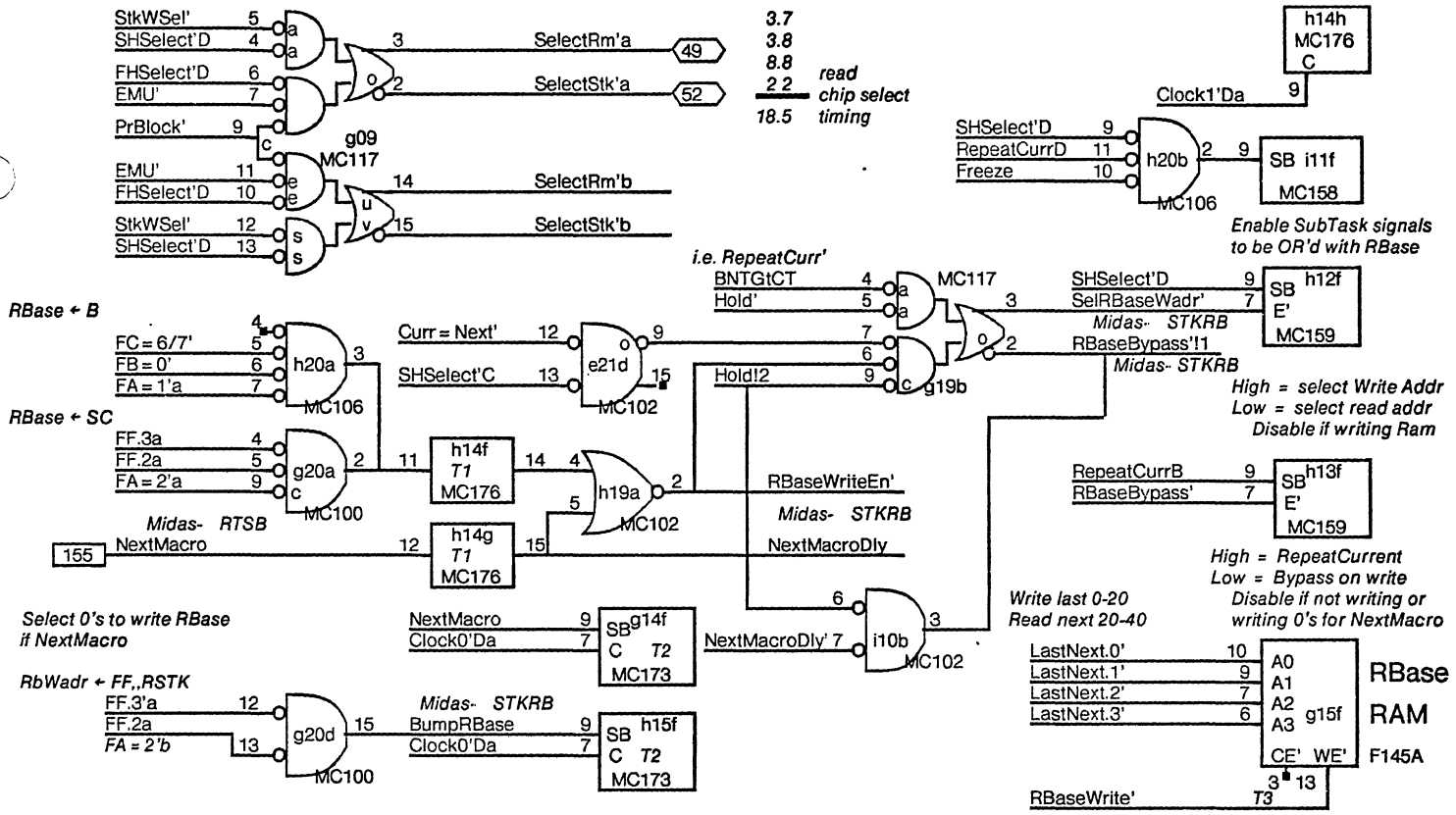
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	LC FIELD RAM ADDRESSES	ProcL20.sil	R Bates	Ci	6/27/79	20







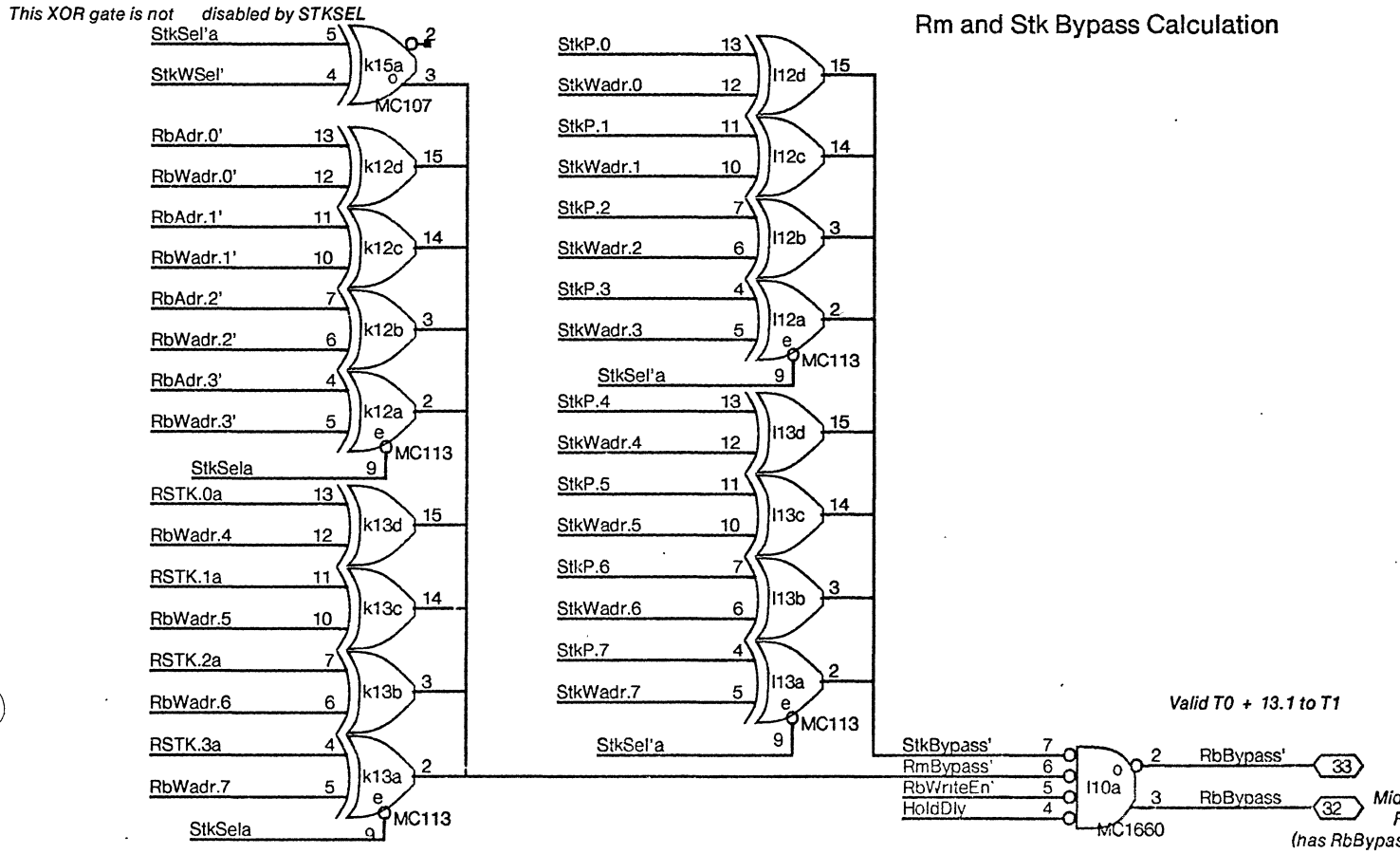
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	RM & STK addressing	ProcL21.sil	R Bates	Ci	6/27/79	21



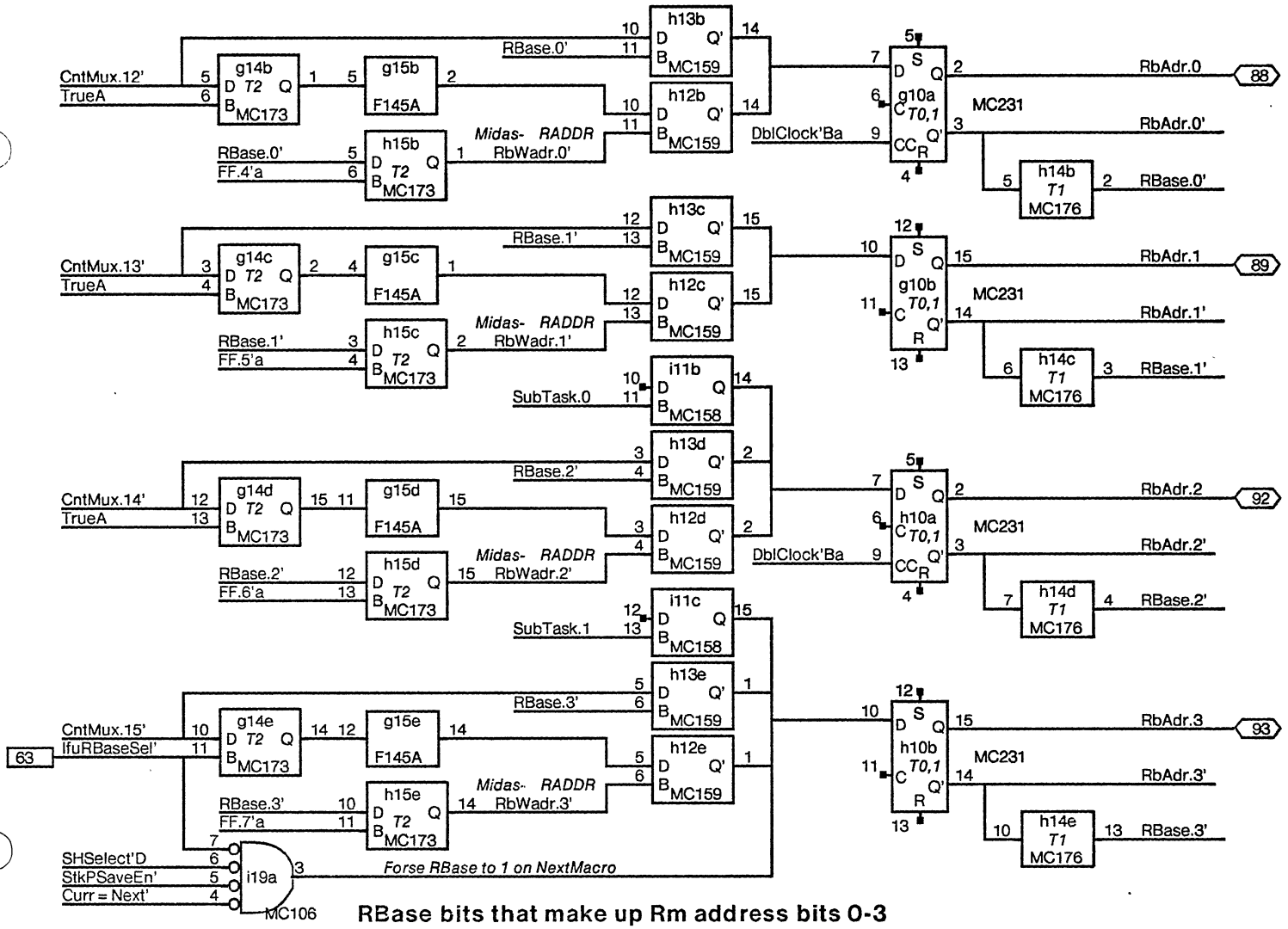
RBase & Control for bits 0 - 3 of the Rm address

RSTK & Control for bits 4 - 7 of the Rm address

Rm and Stk Bypass Calculation

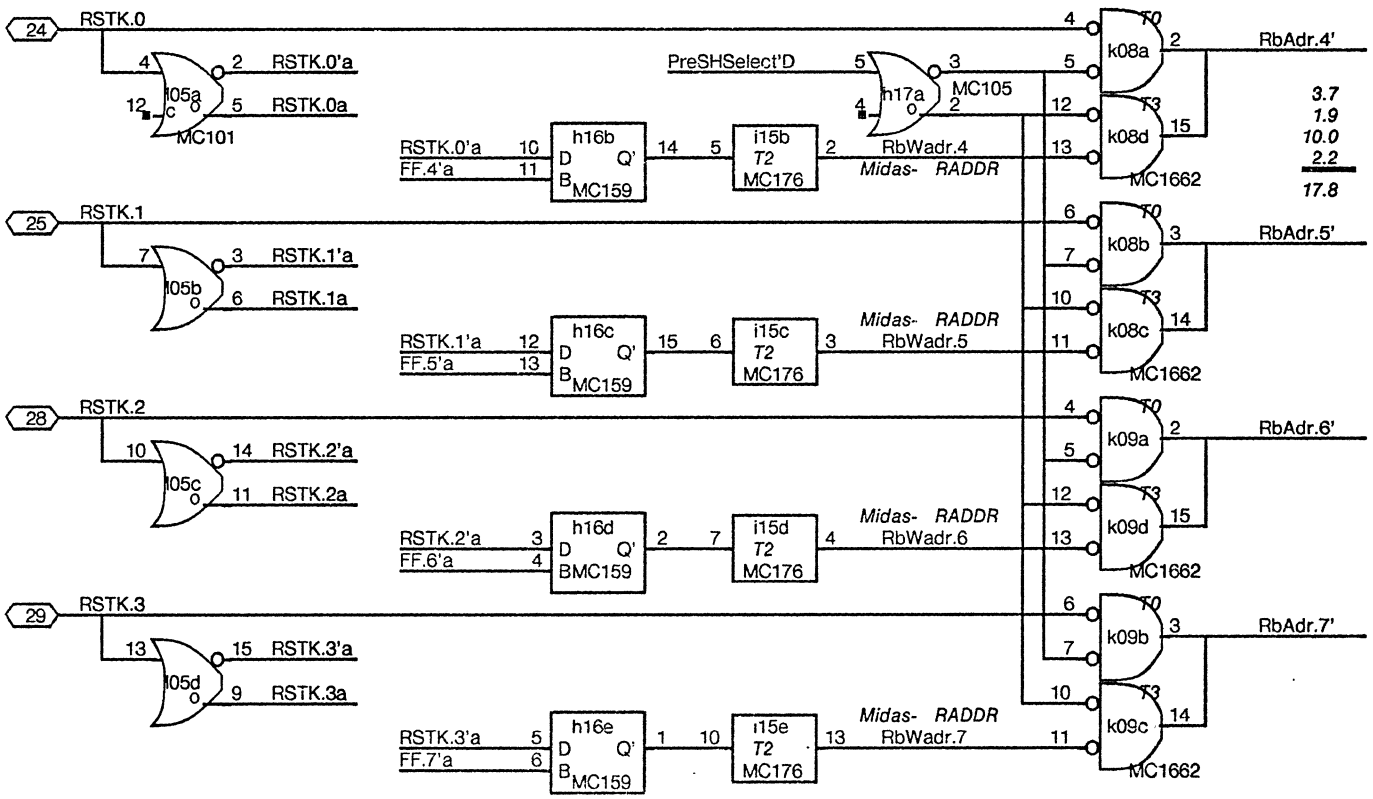


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	RBase & RSTK Cont. plus Rm & Stk Bypass	ProcL22.sil	R Bates	Ci	1/21/80	22

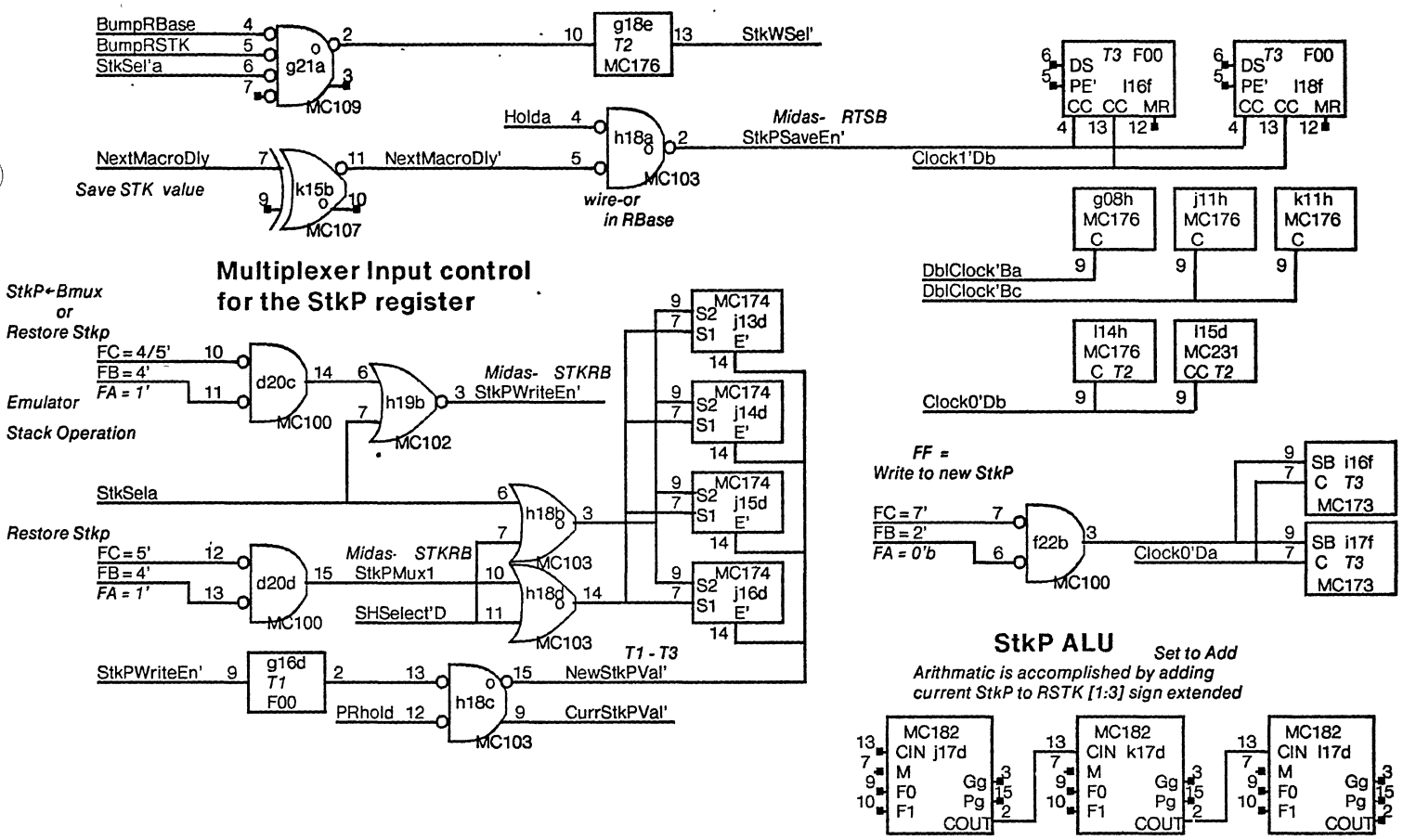


RBase bits that make up Rm address bits 0-3

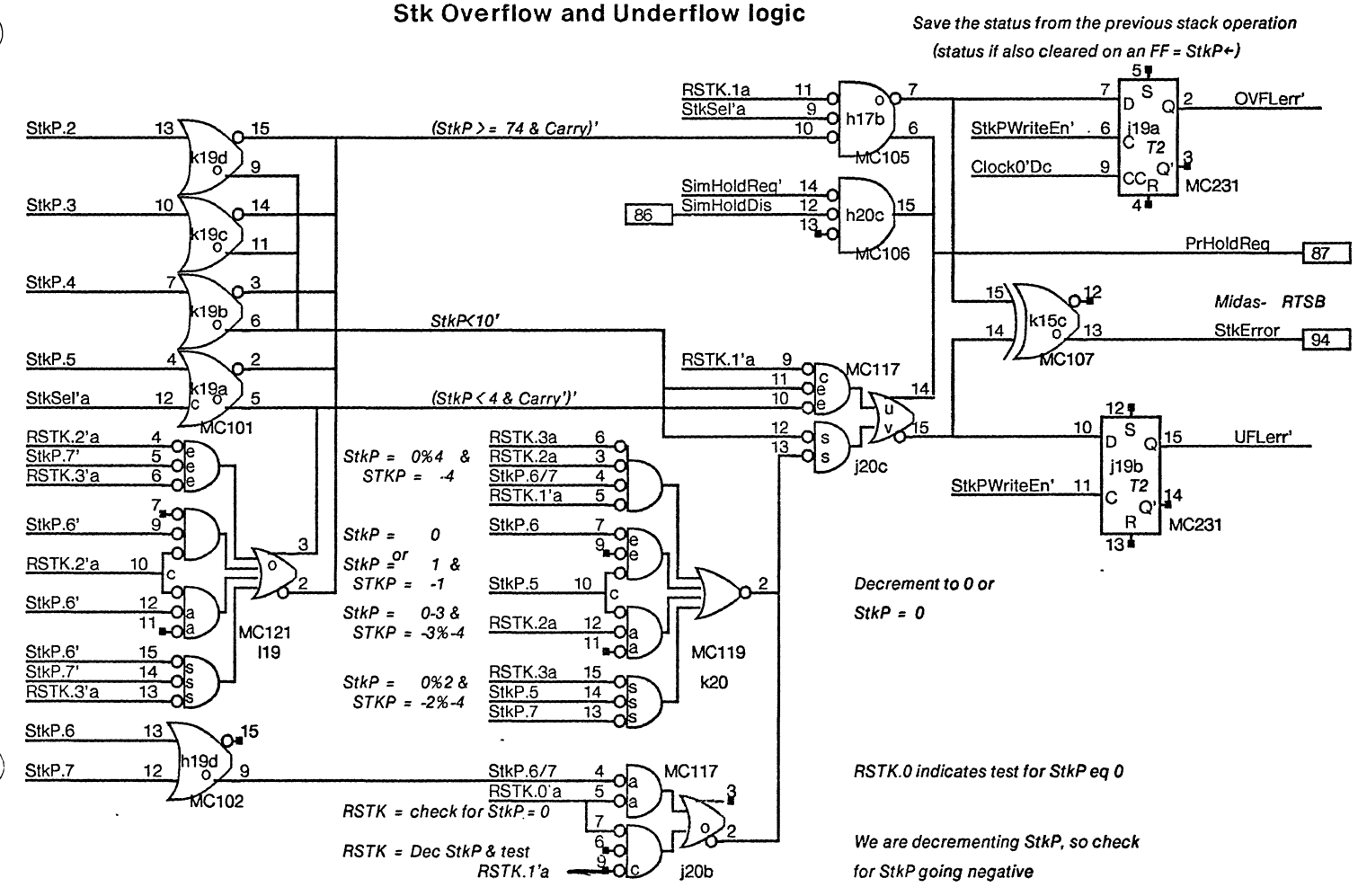
RSTK bits that make up Rm address bits 4-7



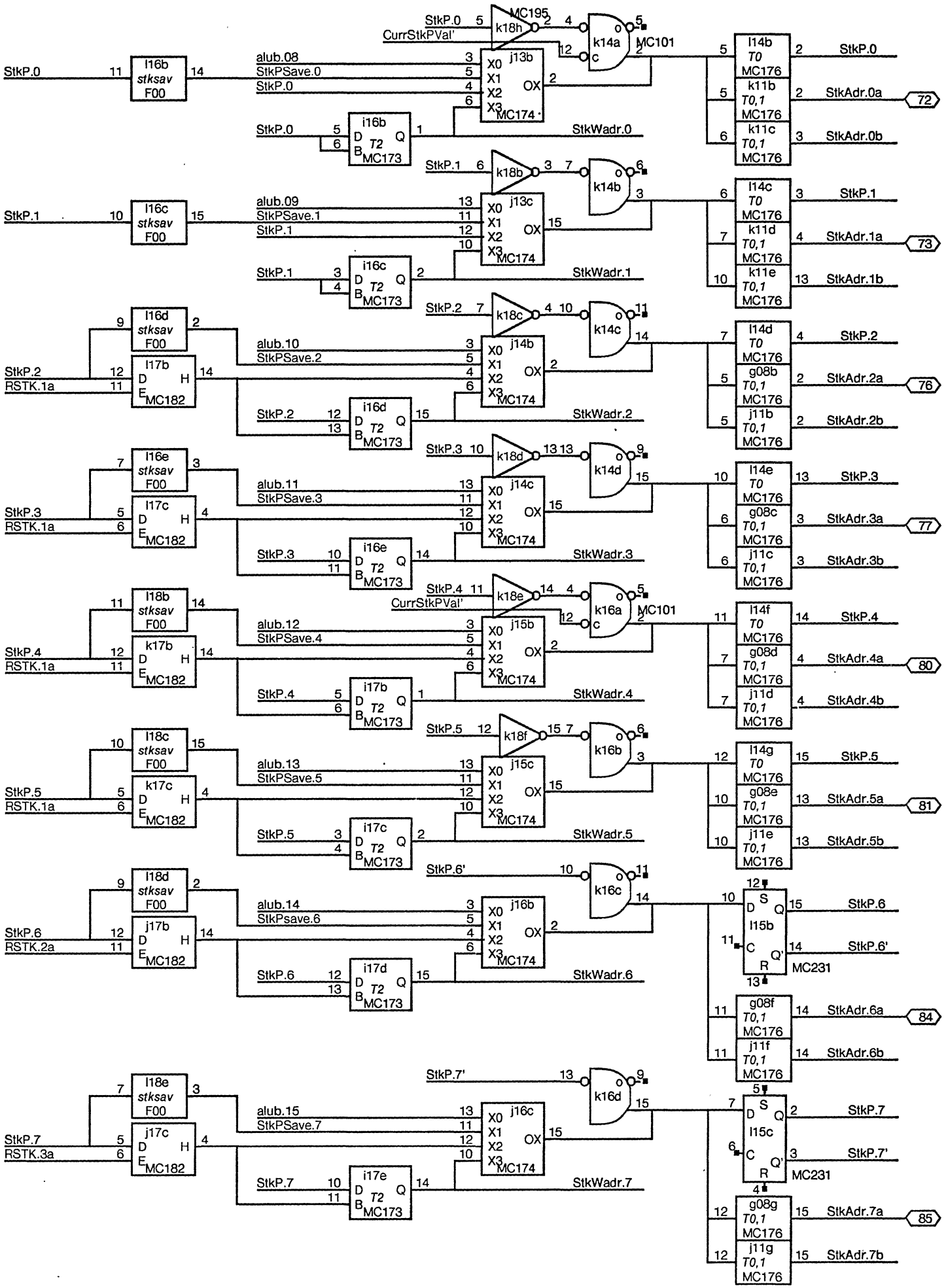
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	R memory Address logic	ProcL23.sil	R Bates	Ci	1/21/80	23



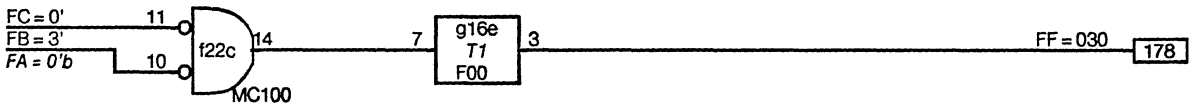
StkP & Control for bit 0 - 7 of the Stk address



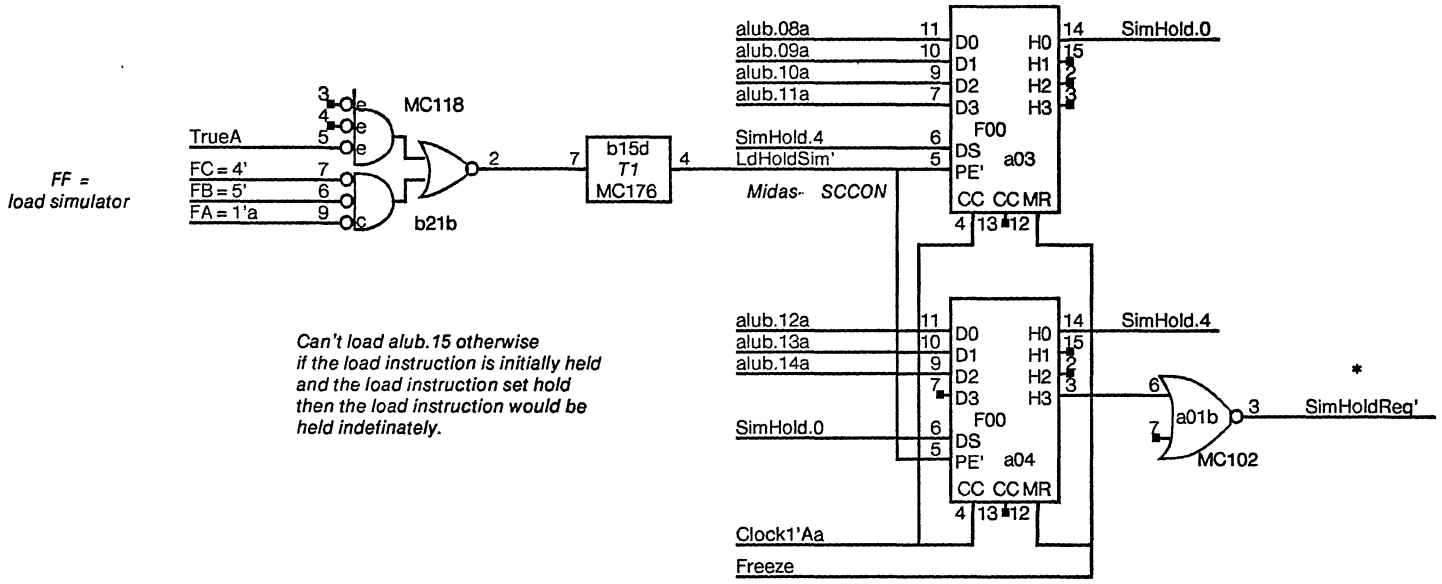
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Stk Control and Overflow / Underflow Ck	ProcL24.sil	R Bates	Ci	1/21/80	24



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	STK memory Address logic	ProcL25.sil	R Bates	Ci	6/28/79	25

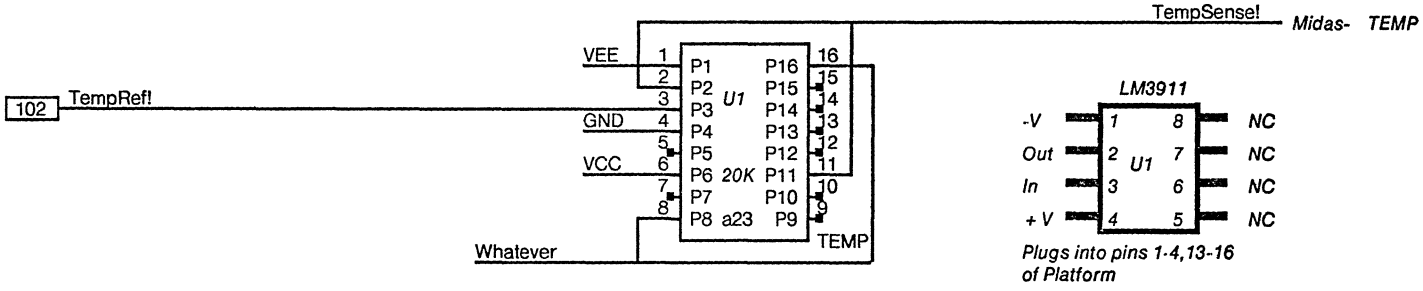


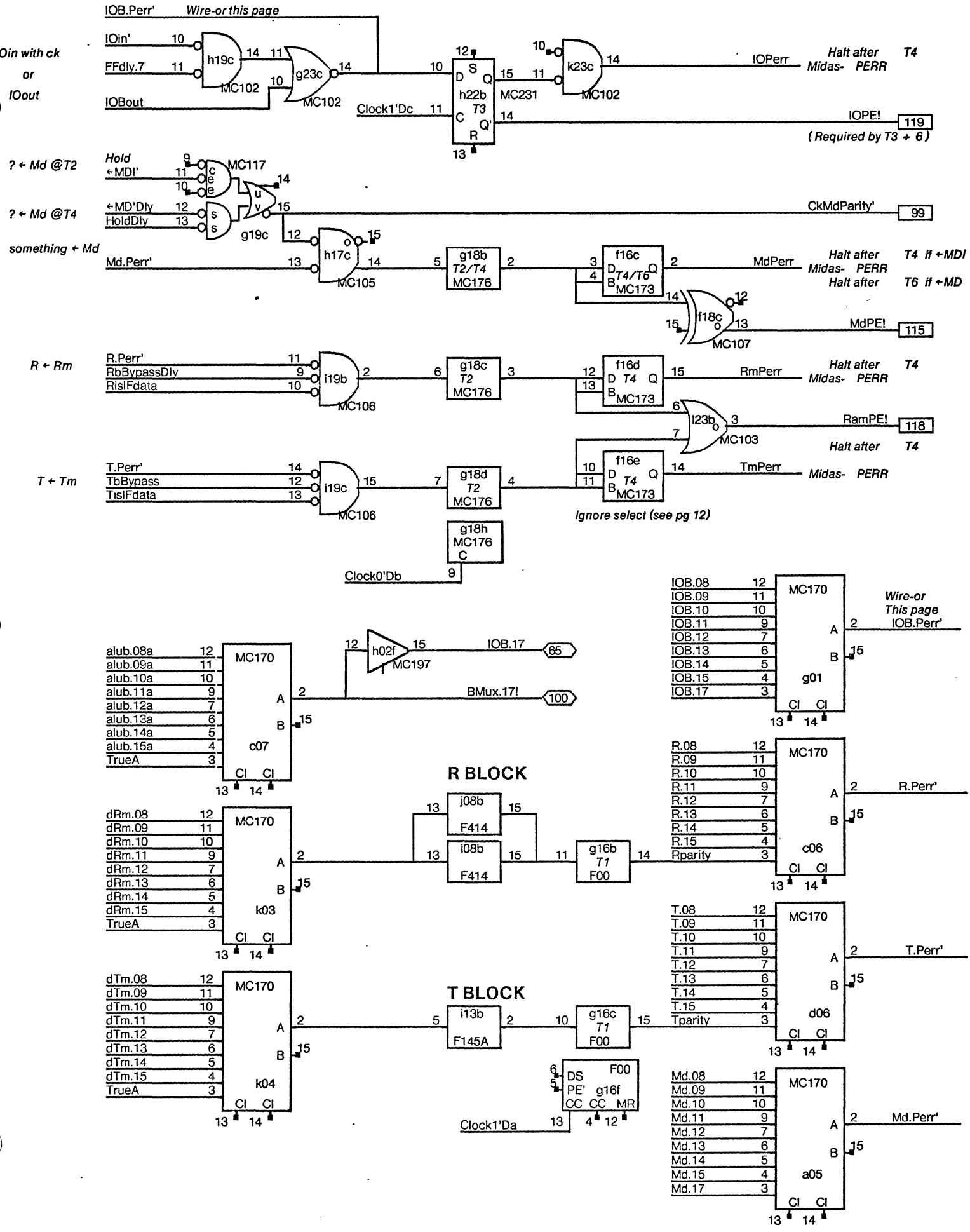
Spare FF Decode



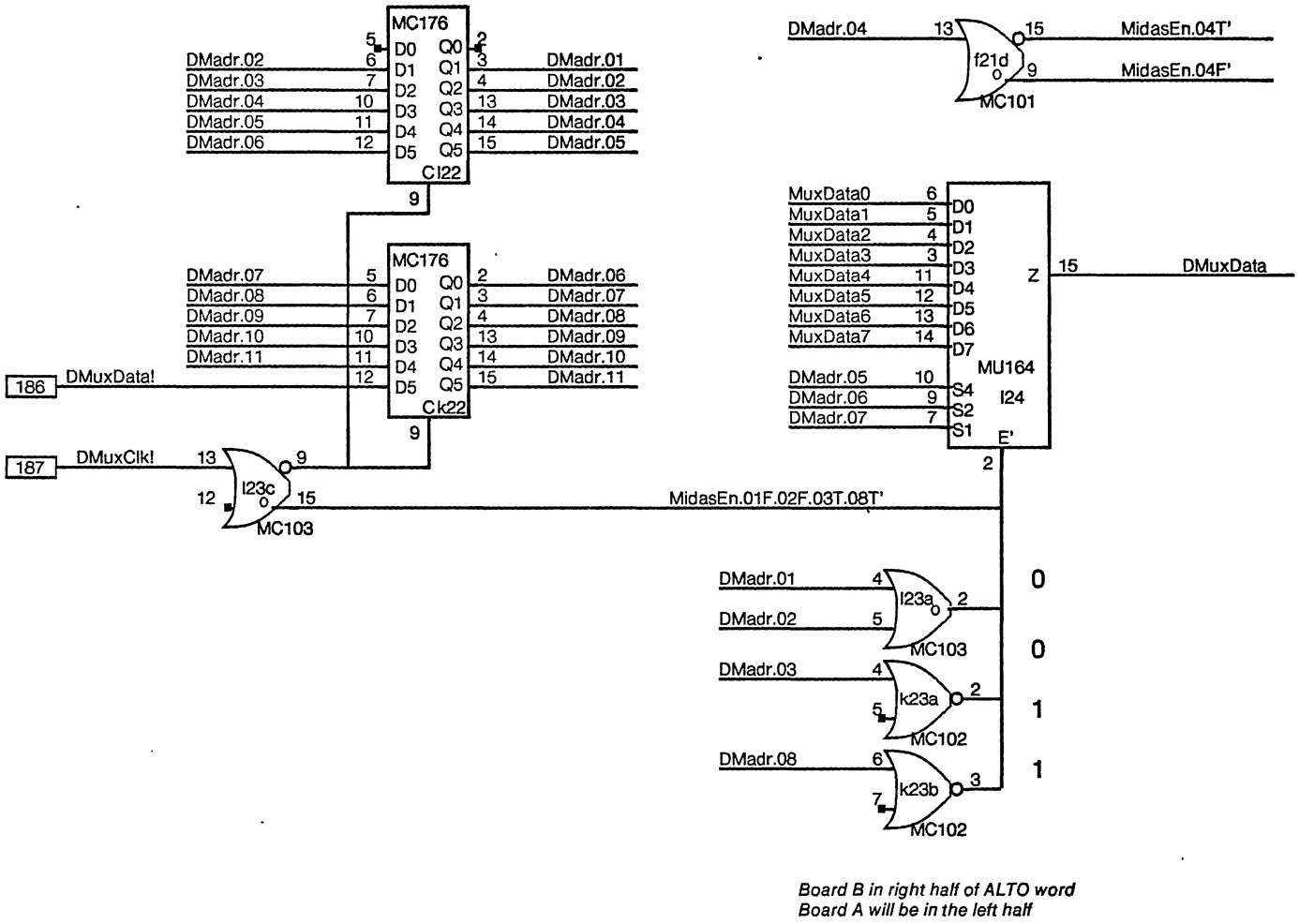
Hold Simulator

Temperature Sensing Ckt





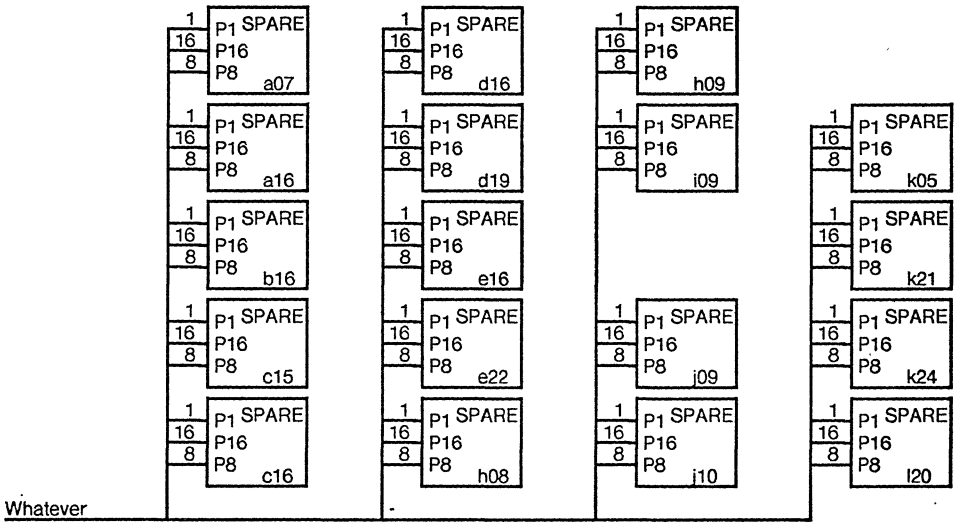
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Parity Logic	ProcL27.sil	R Bates	Ci	6/27/79	27



Board B in right half of ALTO word
Board A will be in the left half

Midas Control

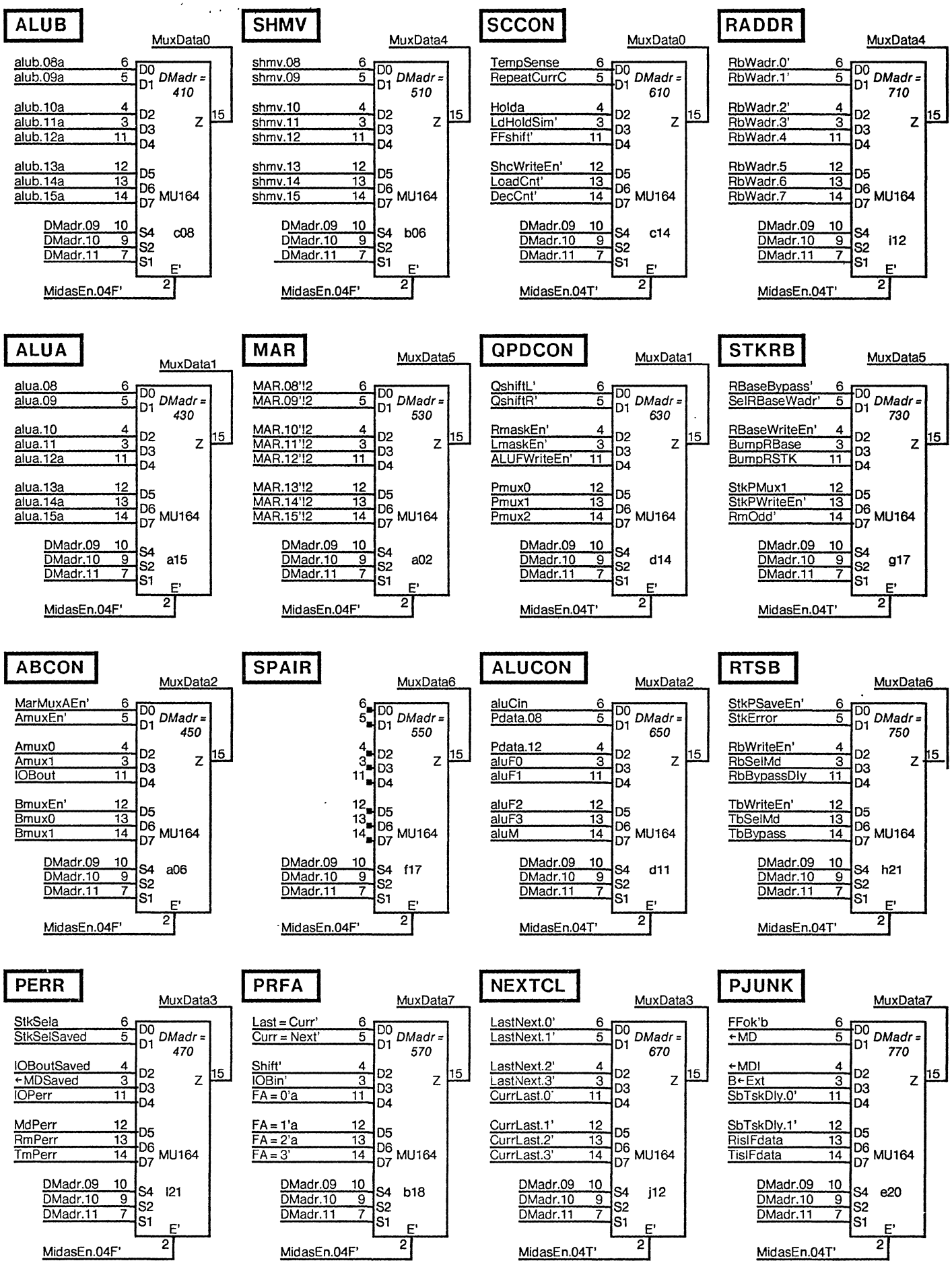
Spair Socket Declarations



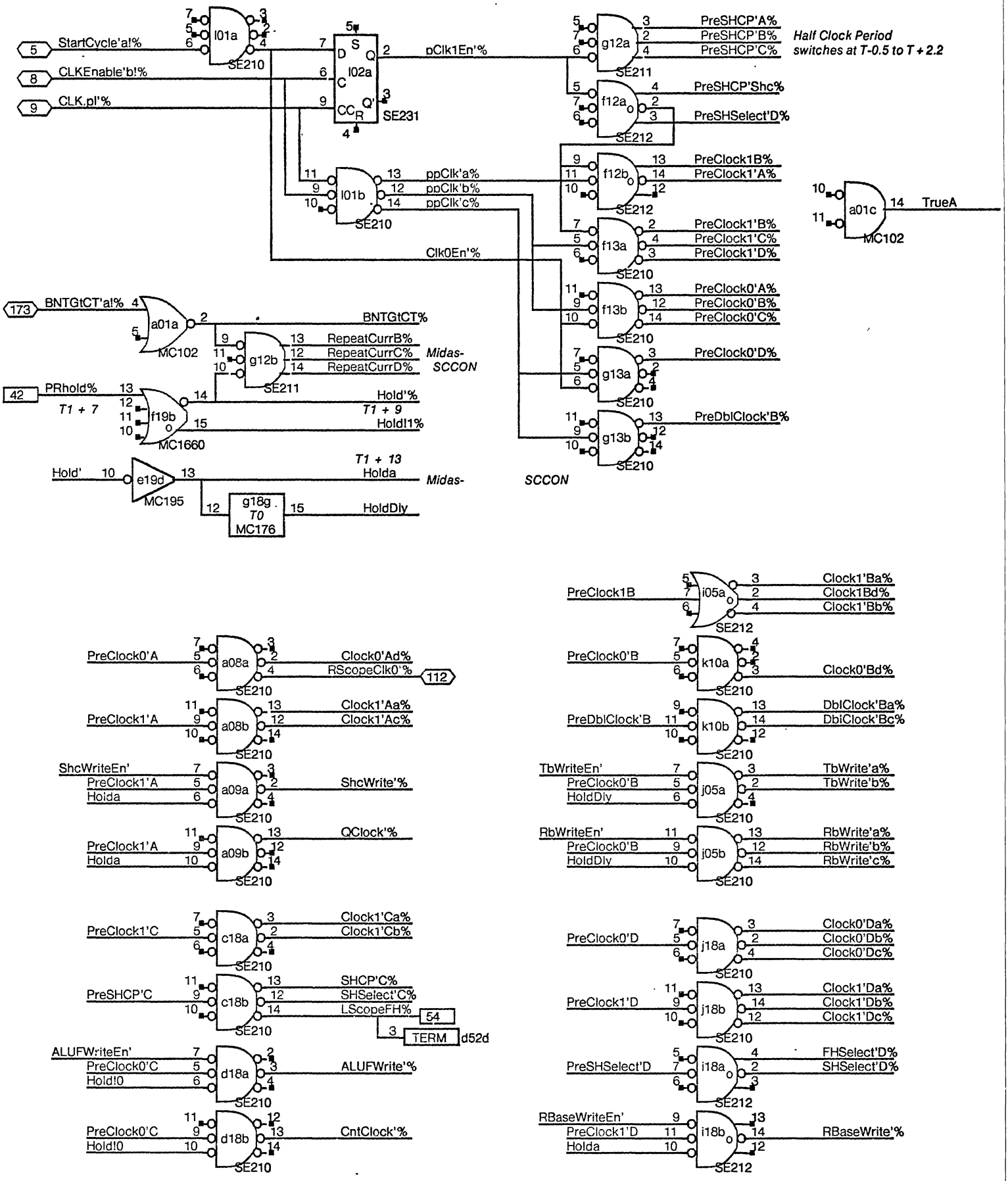
These should be the entire collection of unused locations.

This declaration will cause holes to be drilled in these locations on multiwire boards.

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Midas Control	ProcL28.sil	R Bates	Ci	1/21/80	28



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	DMUX MUFFLERS	ProcL29.sil	R Bates	Ci	6/27/79	29



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	CLOCK DRIVERS	ProcL30.sil	R Bates	Ci	6/27/79	30

The Following Signals are provided 50 ohm termination values

by the addition of 100 ohm 1/4 w descrete resistors in parallel with the normal sip

StkSel'a
StkSela
RbAdr.0'
RbAdr.1'
RbAdr.2'
RbAdr.3'
RSTK.0a
RSTK.1a
RSTK.2a
RSTK.3a
RbWadr.0'
RbWadr.1'
RbWadr.2'
RbWadr.3'
RbWadr.4'
RbWadr.5'
RbWadr.6'
RbWadr.7'

For additional information or the rework instructions see
[IVY]<DoradoLogic>ProcL-MWRev-Ch-to-Ci-Rework.sil

-2v TIOA IOB IOB Clk +12v

	A (184)	B (168)	C (152)	D (136)	E (120)	F (102)	G (84)	H (68)	I (52)	J (36)	K (20)	L	
1	MC102	Ex Bmux MC174 X	Ex Bmux MC174 X	Ex Bmux MC1662 X	Ex Bmux MC174 X	Ex Bmux MC174 X	IOB par. MC170 X	IOB MC197 X	Md MC175 X	dRm Reg. MC173 X	dTm Reg. MC173 X	Clocks SE210	1
41	MAR MU164 X	Mar Mux MC159 X	Mar Mux MC159 X	Ex Bmux MC1662 X	Mar Mux MC159 X	Mar Mux MC159 X	Pdata MC164 X	IOB MC197 X	Md MC175 X	dRm Reg. MC173 X	dTm Reg. MC173 X	Clocks SE231	2
2	SimTW F00 X	Amux MC174 X	Amux MC174 X	Amux MC174 X	Amux MC174 X	Pdata MC164 X	Pdata MC164 X	Pdata MC164 X	T Reg. MC173 X	dT Reg. MC173 X	dRm Par. MC170 X	T Mem. MC145 X	3
42	SimTW F00 X	Bmux MC174 X	Bmux MC174 X	Bmux MC174 X	Bmux MC174 X	Pdata MC164 X	Pdata MC164 X	Pdata MC164 X	T Reg. MC173 X	dT Reg. MC173 X	dT par. MC170 X	T Mem. MC145 X	4
3	Md Parity MC170 X	Amux In MC173 X	Bmux In MC173 X	Amux In MC173 X	Bmux In MC173 X	Pdata MC164 X	dR Reg. MC173 X	dR Reg. MC173 X	Clocks SE212	Clocks SE210		RSTK MC101	5
43	Mux Cont MU164	Shmv MU164 X	R Parity MC170 X	T Parity MC170 X	Pdata in MC173 X	Pdata in MC173 X	R Reg. MC173 X	Rm Mem. MB071 X	Stk Mem. MB071 X	Rm Mem. MB071 X	Stk Mem. MB071 X	Rodd MC1668	6
4		Shmv MC139 X	alub Par MC170 X	alua-a MC101 X	ShA MC158 X	ShA MC158 X	R Reg. MC173 X					Rodd MC1668	7
44	Clocks SE210	Shmv MC139 X	alub MU164 X	alu = 0 MC109	AhB MC158 X	AhB MC158 X	StkPadr T01 MC176 X		Stk parity F414 X	Rm parity F414 X	RbAdr MC1662 X	Rodd MC211	8
5	Clocks SE210	alub-a MC1664 X	alub-a MC1664 X	alu MC181 X		alu MC181 X	R/stk sel MC117 X				RbAdr MC1662 X	Rodd MC211	9
45	Amux T1 MC231	Bmux T1 MC231	Mux T1 MC176				RbAdr MC231 X	RbAdr MC231 X	RBase MC102		Clocks SE210	RbBypass MC1660	10
10	Amux T1 MC231	Mux T1 MC141	Q Reg. MC141 X	ALUFM MU164 X	alua sh MC159 X	alua sh MC159 X	CntMux MC159 X	CntMux MC159 X	RBase MC158 X	StkAdr T01 MC176	StkAdr T01 MC176	Misc. MC231	11
46	Shc MC173 X	Shc MC173 X	Q Reg. MC141 X	Shc MC180 X	ALUFM MC176	Clocks SE212	Clocks SE211	RBase MC159 X	RmWadr MU164 X	NextLast MU164 X	RmBypass MC113 X	StkBypass MC113 X	12
12	Shc MC173 X	Shc MC173 X	Shc MC158 X	Shc MC180 X	ALUFM MC145 X	Clocks SE210	Clocks SE210	RBase MC159 X	T mem-P MC145 X	StkAdr MC174 X	RmBypass MC113 X	StkBypass MC113 X	13
13	Bmux In MC158 X	Bmux In MC158 X	Shc MU164 X	P mux MU164 X	ALUFM MC145 X	Pdata in MC159 X	RBase MC173 X	RbAdr T1 MC176	CurrLast' MC141 X	StkAdr MC174 X	StkAdr MC158 X	StkP MC176 X	14
47	alua MU164 X	Q Reg. MC176		Cnt Reg. F16 X	Cnt Reg. F16 X	Pdata in MC159 X	RBase MC145 X	RBase MC173 X	RBase T0 MC176	StkAdr MC174 X	Misc. MC107	StkP MC231 X	15
14						aluCin MC173	Parity T1 F00	RBase MC159 X	StkAdr MC173 X	StkAdr MC174 X	StkAdr MC158 X	StkPsave F00 X	16
48	Q Reg. MC113 X	Q Reg. MC119 X	Q Reg. MC119 X	Misc. T0 MC176	Misc. T1 MC176	SPAIR MU164 X	Rm cont MU164 X	Misc. MC105	StkAdr MC173 X	StkP MC182 X	StkP MC182	StkP MC182 X	17
15	LastNext' MC158 X	FA MU164 X	Clocks SE210	Clocks SE210	P mux MC102	Misc. MC107	Misc. T0 MC176	RBase MC103	Clocks SE212	Clocks SE210	StkP MC195 X	StkPsave F00 X	18
49	LastNext' MC158 X	Misc. MC212	Amux MC121 X		Misc MC195	MC1660	Parity MC117	Misc. MC102	Parity MC106	Ovfl-Ufl MC231	Ovfl-Ufl MC101	Ovfl-Ufl MC121 X	19
16	Last' MC141 X	FA = 0 MC100	FA = 2 MC100	FA = 1 MC100	Misc. MU164 X	FA = 0 MC100	FA = 2 MC100	FA = 0 MC106	Shl MC164 X	Ovfl-Ufl MC117 X	Ovfl-Ufl MC119 X		20
50	Curr' MC141 X	FA = 1 MC118	Amux MC119 X	Amux MC117 X	Misc. MC102	ALUF MC101	B←Ext MC109	Rm cont MU164 X	Shl MC164 X	Shl MC164 X		Parity MU164 X	21
17	Next = Curr MC113 X	P mux MC212	Misc. MC102	←MDI MC121 X		FA = 0 MC100	Misc. MC103	Parity MC231	Shl MC164 X	Shl MC164 X	Midas MC176 X	Midas MC176 X	22
51	Temp LM3911 X	ASel MC101	FF dec MC210	FF dec. MC101 X	FF-a MC101 X	FF-a MC101 X	Misc MC102	LC dec. MC102	Shl MC164 X	Shl MC164 X	Misc. MC102	Misc. MC103	23
18	Next MC101 X	ALUF MC211	Misc. MC103	FF dec. MC101 X	FF dec. MC161 X	FF dec. MC161 X	MemBase MC231	BSel dec. MC101	Shl MC164 X	Shl MC164 X		Midas MU164 X	24
52	A 10	B 26	C 42	D 58	E 74	F 92	G 110	H 126	I 142	J 158	K 174	L	

-5v Muffler +5v

Spare = 19

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Board Layout	ProcL32.sil	R. Bates	Ci	3/18/80	32

Use Dorado Proms to define the following Proms:

Board Name	Prom Name	location
PorcL	Lmask (low bite)	b07
	Rmask (low bite)	b08

Page Numbers: Yes First Page: 1
Columns: 2 Edge Margin: .8" Between Columns: .0"
Heading:
ProcL-mwRev-Ci.ps
COMPONENTS:

F00:	24	25	26	27		
F145A:	2	3	4	5	6	7
	8	9	11	21	22	23
	27					
F16:	17					
F414:	21	27				
MB071:	2	3	4	5	6	7
	8	9	21			
MC100:	10	11	14	15	16	18
	20	22	24	26		
MC101:	6	7	8	9	11	12
	13	15	20	23	24	25
	28					
MC102:	14	15	16	17	18	20
	22	24	26	27	28	30
MC103:	11	13	14	15	17	24
	27	28				
MC105:	23	24	27			
MC106:	22	23	24	27		
MC107:	11	20	22	24	27	
MC109:	10	15	24			
MC113:	12	17	22			
MC117:	14	22	24	27		
MC118:	17	26				
MC119:	14	17	24			
MC121:	14	20	24			
MC141:	12	14	17	19		
MC158:	2	3	4	5	6	7
	8	9	12	15	18	19
	22	23				
MC159:	2	3	4	5	6	7
	8	9	14	16	17	19
	22	23				
MC161:	13					
MC164:	2	3	4	5	6	7
	8	9	19			
MC1660:	12	20	22	30		
MC1662:	2	3	4	5	6	7
	8	9	23			
MC1664:	2	3	4	5	6	7
	8	9				
MC1668:	10	20				
MC170:	27					
MC173:	2	3	4	5	6	7
	8	9	11	14	15	16
	18	20	22	23	24	25
	27					
MC174:	2	3	4	5	6	7
	8	9	14	15	24	25
MC175:	2	3	4	5	6	7
	8	9	10			
MC176:	10	11	12	14	15	16
	17	18	20	22	23	24
	25	26	27	28	30	
MC180:	18					
MC181:	2	3	4	5	6	7
	8	9	10			
MC182:	24	25				
MC195:	11	17	25	30		
MC197:	2	3	4	5	6	7
	8	9	15	27		
MC210:	13					
MC211:	11	13				
MC212:	15	16				
MC231:	12	14	15	17	20	23
	24	25	27			
MU164:	28	29				
SE210:	30					
SE211:	10	20	30			
SE212:	30					

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SE231:          30
SG139:          16
SPARE:          28
TEMP:           26
TERM:            2       3       4       5       6       7
                 8      30

SIGNAL NAMES:

+:              2(1)    3(1)    4(1)    5(1)    6(1)    7(1)
                8(1)    9(1)   10(1)   11(1)   12(1)   13(1)
               14(1)   15(1)   16(1)   17(1)   18(1)   19(1)
               20(1)   21(1)   22(1)   23(1)   24(1)   25(1)
               26(1)   27(1)   28(1)   29(1)   30(1)
Ain.08:         2(3)
Ain.09:         3(3)
Ain.10:         4(3)
Ain.11:         5(3)
Ain.12:         6(3)
Ain.13:         7(3)
Ain.14:         8(3)
Ain.15:         9(3)
alu.07:         2(1)
alu.08:         2(1)    3(1)   10(1)
alu.09:         2(1)    3(1)    4(1)   10(1)
alu.10:         3(1)    4(1)    5(1)   10(1)
alu.11:         4(1)    5(1)    6(1)   10(1)
alu.12:         5(1)    6(1)    7(1)   10(1)
alu.13:         6(1)    7(1)    8(1)   10(1)
alu.14:         7(1)    8(1)    9(1)   10(1)
alu.15:         8(1)    9(1)   10(1)
alua.08:       18(2)   29(1)
alua.08!1:      2(1)
alua.09:       18(2)   29(1)
alua.09!1:      3(1)
alua.10:       18(2)   29(1)
alua.10!1:      4(1)
alua.11:       18(2)   29(1)
alua.11!1:      5(1)
alua.12:        6(1)
alua.12'a:      6(1)   18(1)
alua.12a:       6(1)   18(1)   29(1)
alua.13:        7(1)
alua.13'a:      7(1)   18(1)
alua.13a:       7(1)   18(1)   29(1)
alua.14:        8(1)
alua.14'a:      8(1)   18(1)
alua.14a:       8(1)   18(1)   29(1)
alua.15:        9(1)
alua.15'a:      9(1)   18(1)
alua.15a:       9(1)   18(1)   29(1)
alub.08:        2(1)   17(1)   25(1)
alub.08a:       2(1)   11(1)   17(1)   18(1)   26(1)   27(1)
               29(1)
alub.09:        3(1)   17(1)   25(1)
alub.09a:       3(1)   17(1)   18(1)   26(1)   27(1)   29(1)
alub.10:        4(1)   17(1)   25(1)
alub.10a:       4(1)   17(1)   18(1)   26(1)   27(1)   29(1)
alub.11:        5(1)   17(1)   25(1)
alub.11a:       5(1)   11(1)   17(1)   18(1)   26(1)   27(1)
               29(1)
alub.12:        6(1)   17(1)   25(1)
alub.12a:       6(1)   11(1)   17(1)   18(1)   26(1)   27(1)
               29(1)
alub.13:        7(1)   17(1)   25(1)
alub.13a:       7(1)   11(1)   17(1)   18(1)   26(1)   27(1)
               29(1)
alub.14:        8(1)   17(1)   25(1)
alub.14a:       8(1)   11(1)   17(1)   18(1)   26(1)   27(1)
               29(1)
alub.15:        9(1)   17(1)   25(1)
alub.15a:       9(1)   11(1)   17(1)   18(1)   27(1)   29(1)
aluC:           2(1)   11(1)
aluC0:         10(1)
ALUCarry!:     11(1)
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aluCin:          10(1)   11(1)   29(1)
aluCout:         17(1)
ALUF.0:          11(1)
ALUF.0':         11(1)   16(1)   20(1)
ALUF.1:          11(1)
ALUF.1':         11(1)   16(1)
ALUF.2:          11(1)
ALUF.2':         11(1)   16(1)
ALUF.3:          11(1)
aluF0:            5(1)   10(1)   11(1)   29(1)
aluF1:            6(1)   10(1)   11(1)   29(1)
aluF2:            7(1)   10(1)   11(1)   29(1)
aluF3:            8(1)   10(1)   11(1)   29(1)
ALUFdec.0:       11(1)
ALUFdec.1:       11(1)
ALUFdec.2:       11(1)
ALUFdec.3:       11(1)
ALUFdec.4:       11(1)
ALUFdec.5:       11(1)
ALUFWrite':      11(1)
ALUFWrite'%:     30(1)
ALUFWriteEn':    11(1)   29(1)   30(1)
aluG1:           10(1)
aluM:             9(1)   10(1)   11(1)   29(1)
aluOut=0':       10(1)
aluP1:           10(1)
Amux0:           14(2)   29(1)
Amux1:           14(2)   29(1)
Amux1':          14(2)
AmuxEn':         14(1)   29(1)
ASel.0:          13(1)   14(1)
ASEL.0':         11(1)
ASel.0':         13(3)   15(1)
ASEL.0'!:        13(1)
ASEL.1':         11(1)
ASEL.1'!:        13(1)
ASEL.2':         11(1)
ASEL.2'!:        13(1)
ASel=2/3':       14(3)   20(1)
ASel=2/3'!1:     13(1)
ASel=5/7:        13(1)   14(2)
ASel=5/7':       13(2)   14(1)   15(1)
ASel=6/7:        13(1)   14(2)
ASel=6/7':       13(2)   14(1)   15(1)
A←Id':           14(2)
Bin.08:           2(3)
Bin.09:           3(3)
Bin.10:           4(3)
Bin.11:           5(3)
Bin.12:           6(3)
Bin.13:           7(3)
Bin.14:           8(3)
Bin.15:           9(3)
BMux.08:          2(1)
BMux.08!:         2(1)
BMux.09:          3(1)
BMux.09!:         3(1)
BMux.10:          4(1)
BMux.10!:         4(1)
BMux.11:          5(1)
BMux.11!:         5(1)
BMux.12:          6(1)
BMux.12!:         6(1)
BMux.13:          7(1)
BMux.13!:         7(1)
BMux.14:          8(1)
BMux.14!:         8(1)
BMux.15:          9(1)
BMux.15!:         9(1)
BMux.17!:        27(1)
Bmux0:           15(2)   29(1)
Bmux0':          15(2)
Bmux1:           15(2)   29(1)
Bmux1':          15(2)
BmuxEn':         15(1)   29(1)
BmuxIn':          2(1)    3(1)    4(1)    5(1)    6(1)    7(1)
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CurrLast.3':    12(1)   21(1)   29(1)
CurrStkPVal':   24(1)   25(2)
dAmux0:         14(2)
dAmux1':        14(1)
DblClock'Ba:    23(2)   24(1)
DblClock'Ba%:   30(1)
DblClock'Bc:    12(1)   24(1)
DblClock'Bc%:   30(1)
dBmux0:         15(1)
dBmux1:         15(1)
ddR.15:          9(1)   10(1)
DecCnt':        17(1)   29(1)
DMadr.01:       28(2)
DMadr.02:       28(3)
DMadr.03:       28(3)
DMadr.04:       28(3)
DMadr.05:       28(3)
DMadr.06:       28(3)
DMadr.07:       28(3)
DMadr.08:       28(3)
DMadr.09:       28(2)   29(16)
DMadr.10:       28(2)   29(16)
DMadr.11:       28(2)   29(16)
dMD.08:          2(1)
dMD.09:          3(1)
dMD.10:          4(1)
dMD.11:          5(1)
dMD.12:          6(1)
dMD.13:          7(1)
dMD.14:          8(1)
dMD.15:          9(1)   10(1)
dMD.17:         10(1)
DMuxClk!:       28(1)
DMuxData:       28(1)
DMuxData!:      28(1)
dPmux0:         16(1)
dPmux1:         16(1)
dPmux2:         16(2)
dR.08:           2(1)
dR.09:           3(1)
dR.10:           4(1)
dR.11:           5(1)
dR.12:           6(1)
dR.13:           7(1)
dR.14:           8(1)
dR.15:           9(1)
dRm.08:          2(1)   27(1)
dRm.09:          3(1)   27(1)
dRm.10:          4(1)   27(1)
dRm.11:          5(1)   27(1)
dRm.12:          6(1)   27(1)
dRm.13:          7(1)   27(1)
dRm.14:          8(1)   27(1)
dRm.15:          9(1)   27(1)
DsMd:           10(3)
DsPd:           10(3)
DsRd:           10(3)
dT.08:           2(1)
dT.09:           3(1)
dT.10:           4(1)
dT.11:           5(1)
dT.12:           6(1)
dT.13:           7(1)
dT.14:           8(1)
dT.15:           9(1)
dTm.08:          2(1)   27(1)
dTm.09:          3(1)   27(1)
dTm.10:          4(1)   27(1)
dTm.11:          5(1)   27(1)
dTm.12:          6(1)   27(1)
dTm.13:          7(1)   27(1)
dTm.14:          8(1)   27(1)
dTm.15:          9(1)   27(1)
EMU':           12(1)   22(2)
FA=0'a:         14(1)   16(2)   17(1)   29(1)
FA=0'a!1:       13(1)
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FA=0'a!2:       14(2)   17(1)
FA=0'b:         10(1)   13(1)   20(1)   22(1)
FA=1'a:         13(1)   14(1)   17(2)   18(1)   22(1)   26(1)
                29(1)
FA=2'a:         13(1)   16(2)   17(1)   22(1)   29(1)
FA=3':          13(1)   17(1)   29(1)
FB=0':          13(1)   22(1)
FB=2':          10(1)   11(1)   13(1)   14(4)   20(1)   24(1)
FB=3':          13(1)   14(2)   15(1)   16(1)   26(1)
FB=4':          13(1)   17(1)   24(2)
FB=5':          13(1)   17(2)   18(2)   26(1)
FB=6':          11(1)   13(1)   16(4)
FB=7':          13(1)   16(3)   17(4)   20(1)
FC=0':          13(1)   17(2)   26(1)
FC=1':          13(1)   17(1)
FC=2':          11(1)   13(1)   16(1)   17(1)   20(1)
FC=2/3':        13(1)   14(1)   16(1)
FC=3':          13(1)   17(2)
FC=4':          13(1)   14(1)   26(1)
FC=4/5':        11(1)   13(1)   16(1)   24(1)
FC=5':          11(1)   13(1)   14(1)   18(1)   20(1)   24(1)
FC=6':          10(1)   13(1)   15(1)   17(1)
FC=6/7':        13(1)   16(1)   17(1)   18(1)   22(1)
FC=7':          13(1)   16(1)   24(1)
FF.0:           13(1)
FF.0!:          13(1)
FF.0a:           2(1)   13(1)   17(1)   18(1)
FF.0mem':       13(1)   14(1)
FF.1!:          13(1)
FF.1a:           3(1)   13(1)   18(1)
FF.1mem:        13(1)   14(1)
FF.2:           13(1)
FF.2!:          13(1)
FF.2'a:         13(1)   15(1)   17(1)   22(1)
FF.2a:           4(1)   13(1)   14(2)   18(1)   22(2)
FF.3:           13(1)
FF.3!:          13(1)
FF.3'a:         13(1)   15(1)   22(1)
FF.3a:           5(1)   13(1)   14(2)   17(1)   18(1)   22(2)
FF.4:           13(1)
FF.4!:          13(1)
FF.4'a:         13(1)   23(2)
FF.4a:           6(2)   13(1)   17(2)   18(1)
FF.5:           13(1)
FF.5!:          13(1)
FF.5'a:         13(2)   23(2)
FF.5a:           7(2)   13(2)   14(2)   16(1)   17(1)   18(1)
FF.6:           13(1)
FF.6!:          13(1)
FF.6'a:         13(2)   16(1)   23(2)
FF.6a:           8(2)   13(2)   17(1)   18(1)
FF.7:           13(1)   18(1)
FF.7!:          13(1)
FF.7'a:         13(1)   14(1)   23(2)
FF.7a:           9(2)   13(1)   16(1)   17(1)   18(1)
FF=030:         26(1)
FFdly.7:        17(1)   18(1)   27(1)
FFeqMul':       16(1)   17(1)
FFok'b:         13(3)   14(1)   15(1)   20(1)   29(1)
FFshift':       15(1)   18(1)   29(1)
FHSelect'D:     22(2)
FHSelect'D%:    30(1)
Freeze:         12(1)   22(1)   26(1)
Freeze!:        12(1)
Gnd:             2(1)    3(1)    4(1)    5(1)    6(1)    7(1)
                 8(1)    9(1)   10(1)   11(1)   12(1)   13(1)
                14(1)   15(1)   16(1)   17(1)   18(1)   19(1)
                20(1)   21(1)   22(1)   23(1)   24(1)   25(1)
                26(1)   27(1)   28(1)   29(1)   30(1)
GND:            26(1)
Hold!0:         30(2)
Hold!1%:        30(1)
Hold!2:         15(1)   16(1)   22(1)
Hold':          22(1)   30(1)
Hold'%:         30(1)
Holda:          24(1)   29(1)   30(4)
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HoldDly:        20(1)   22(1)   27(1)   30(3)
IfuData.0:       2(1)
IfuData.1:       3(1)
IfuData.2:       4(1)
IfuData.3:       5(1)
IfuData.4:       6(1)
IfuData.5:       7(1)
IfuData.6:       8(1)
IfuData.7:       9(1)
IfuRBaseSel':   23(1)
IOB.08:          2(2)   27(1)
IOB.09:          3(2)   27(1)
IOB.10:          4(2)   27(1)
IOB.11:          5(2)   27(1)
IOB.12:          6(2)   27(1)
IOB.13:          7(2)   27(1)
IOB.14:          8(2)   27(1)
IOB.15:          9(2)   27(1)
IOB.17:         27(2)
IOB.Perr':      27(2)
IOBin':         16(1)   29(1)
IOBout:         15(1)   27(1)   29(1)
IOBout':        15(1)
IOBoutSaved:    15(1)   29(1)
IOin':          16(1)   27(1)
IOout':         15(1)
IOPE!:          27(1)
IOPerr:         27(1)   29(1)
jcnt:           17(1)
Last.0':        12(1)
Last.1':        12(1)
Last.2':        12(1)
Last.3':        12(1)
Last=Curr':     12(1)   20(1)   29(1)
LastNext.0':    12(2)   22(1)   29(1)
LastNext.1':    12(2)   22(1)   29(1)
LastNext.2':    12(2)   22(1)   29(1)
LastNext.3':    12(2)   22(1)   29(1)
LC.0:           20(4)
LC.1:           20(1)
LC.1'a:         20(4)
LC.1a:          20(2)
LC.2:           20(2)
LdHoldSim':     26(1)   29(1)
LmaskEn':       16(1)   29(1)
LoadCnt':       17(1)   29(1)
LScopeFH%:      30(1)
MAR.08'!0:       2(1)
MAR.08'!1:       2(1)
MAR.08'!2:      29(1)
MAR.09'!0:       3(1)
MAR.09'!1:       3(1)
MAR.09'!2:      29(1)
MAR.10'!0:       4(1)
MAR.10'!1:       4(1)
MAR.10'!2:      29(1)
MAR.11'!0:       5(1)
MAR.11'!1:       5(1)
MAR.11'!2:      29(1)
MAR.12'!0:       6(1)
MAR.12'!1:       6(1)
MAR.12'!2:      29(1)
MAR.13'!0:       7(1)
MAR.13'!1:       7(1)
MAR.13'!2:      29(1)
MAR.14'!0:       8(1)
MAR.14'!1:       8(1)
MAR.14'!2:      29(1)
MAR.15'!0:       9(1)
MAR.15'!1:       9(1)
MAR.15'!2:      29(1)
MarMuxAEn':     14(1)   29(1)
MarMuxBEn':     14(2)
Md.08:           2(2)   27(1)
Md.09:           3(2)   27(1)
Md.10:           4(2)   27(1)
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Md.11:            5(2)   27(1)
Md.12:            6(2)   27(1)
Md.13:            7(2)   27(1)
Md.14:            8(2)   27(1)
Md.15:            9(2)   27(1)
Md.17:           10(1)   27(1)
Md.Perr':        27(2)
MdPE!:           27(1)
MdPerr:          27(1)   29(1)
MemBase.2:       12(1)
MemBase.3:       12(1)
MidasEn.01F.02F.03T.08T':        28(1)
MidasEn.04F':    28(1)   29(8)
MidasEn.04T':    28(1)   29(8)
MuxData0:        28(1)   29(2)
MuxData1:        28(1)   29(2)
MuxData2:        28(1)   29(2)
MuxData3:        28(1)   29(2)
MuxData4:        28(1)   29(2)
MuxData5:        28(1)   29(2)
MuxData6:        28(1)   29(2)
MuxData7:        28(1)   29(2)
NewStkPVal':     24(1)
Next.0!:         12(1)
Next.0':         12(3)
Next.1!:         12(1)
Next.1':         12(3)
Next.2!:         12(1)
Next.2':         12(3)
Next.3!:         12(1)
Next.3':         12(3)
NextMacro:       22(2)
NextMacroDly:    22(1)   24(1)
NextMacroDly':   22(1)   24(1)
OVFLerr':         2(1)   24(1)
pClk1En'%:       30(1)
Pdata.08:         2(2)   29(1)
Pdata.09:         3(2)
Pdata.10:         4(2)
Pdata.11:         5(2)
Pdata.12:         6(2)   29(1)
Pdata.13:         7(2)
Pdata.14:         8(2)
Pdata.15:         9(2)   10(1)
Pmux0:            2(1)    3(1)    4(1)    5(1)    6(1)    7(1)
                  8(1)    9(1)   16(1)   29(1)
Pmux1:            2(1)    3(1)    4(1)    5(1)    6(1)    7(1)
                  8(1)    9(1)   16(1)   29(1)
Pmux2:           16(1)   29(1)
ppClk'a%:        30(1)
ppClk'b%:        30(1)
ppClk'c%:        30(1)
PrBlock':        12(1)   22(1)
PreClock0'A:     30(1)
PreClock0'A%:    30(1)
PreClock0'B:     30(3)
PreClock0'B%:    30(1)
PreClock0'C:     30(2)
PreClock0'C%:    30(1)
PreClock0'D:     30(1)
PreClock0'D%:    30(1)
PreClock1'A:     30(3)
PreClock1'A%:    30(1)
PreClock1'B:     10(3)
PreClock1'B%:    30(1)
PreClock1'C:     30(1)
PreClock1'C%:    30(1)
PreClock1'D:     30(2)
PreClock1'D%:    30(1)
PreClock1B:      30(1)
PreClock1B%:     30(1)
PreDblClock'B:   30(1)
PreDblClock'B%:  30(1)
PreFA=0:         13(2)
PreFA=0':        13(1)   20(1)
PreFA=1':        13(1)   14(1)   15(1)
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PreSHCP'A:       14(1)   15(1)
PreSHCP'A%:      30(1)
PreSHCP'B:       20(2)
PreSHCP'B%:      30(1)
PreSHCP'C:       12(1)   30(1)
PreSHCP'C%:      30(1)
PreSHCP'Shc:     18(1)
PreSHCP'Shc%:    30(1)
PreSHSelect'D:   23(1)   30(1)
PreSHSelect'D%:  30(1)
PRhold:          24(1)
PRhold%:         30(1)
PrHoldReq:       24(1)
PropCnt'!:       17(1)
Q.07:            17(1)
Q.08:             2(4)   17(1)
Q.09:             3(4)   17(1)
Q.10:             4(4)   17(1)
Q.11:             5(4)   17(2)
Q.12:             6(4)   17(1)
Q.13:             7(4)   17(1)
Q.14:             8(4)   17(2)
Q.15:             9(4)   17(1)
QBit':           17(1)
QClock':         17(1)
QClock'%:        30(1)
QshiftL':        17(1)   29(1)
QshiftR':        17(1)   29(1)
R.08:             2(5)   27(1)
R.09:             3(5)   27(1)
R.10:             4(5)   27(1)
R.11:             5(5)   27(1)
R.12:             6(5)   27(1)
R.13:             7(5)   27(1)
R.14:             8(5)   27(1)
R.15:             9(5)   27(1)
R.Perr':         27(2)
RamPE!:          27(1)
RbAdr.0:         23(1)
RbAdr.0':        21(1)   22(1)   23(1)
RbAdr.1:         23(1)
RbAdr.1':        21(1)   22(1)   23(1)
RbAdr.2:         23(1)
RbAdr.2':        21(1)   22(1)   23(1)
RbAdr.3:         23(1)
RbAdr.3':        21(1)   22(1)   23(1)
RbAdr.4':        21(1)   23(1)
RbAdr.5':        21(1)   23(1)
RbAdr.6':        21(1)   23(1)
RbAdr.7':        21(1)   23(1)
RBase.0':         6(1)   23(3)
RBase.1':         7(1)   23(3)
RBase.2':         8(1)   23(3)
RBase.3':         9(1)   23(3)
RBaseBypass':    22(1)   29(1)
RBaseBypass'!1:  22(1)
RBaseWrite':     22(1)
RBaseWrite'%:    30(1)
RBaseWriteEn':   22(1)   29(1)   30(1)
RbBypass:        10(1)   22(1)
RbBypass':       10(2)   20(1)   22(1)
RbBypassDly:     20(1)   27(1)   29(1)
RbSelMd:         10(1)   20(2)   29(1)
RbSelMd':        10(1)   20(1)
RbWadr.0':       22(1)   23(1)   29(1)
RbWadr.1':       22(1)   23(1)   29(1)
RbWadr.2':       22(1)   23(1)   29(1)
RbWadr.3':       22(1)   23(1)   29(1)
RbWadr.4:        22(1)   23(1)   29(1)
RbWadr.5:        22(1)   23(1)   29(1)
RbWadr.6:        22(1)   23(1)   29(1)
RbWadr.7:        22(1)   23(1)   29(1)
RbWrite'a:       21(2)
RbWrite'a%:      30(1)
RbWrite'b:       21(2)
RbWrite'b%:      30(1)
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RbWrite'c:      21(2)
RbWrite'c%:     30(1)
RbWriteEn':     20(1)   22(1)   29(1)   30(1)
RepeatCurrB:    12(1)   22(1)
RepeatCurrB%:   30(1)
RepeatCurrC:    12(2)   29(1)
RepeatCurrC%:   30(1)
RepeatCurrD:    12(1)   22(1)
RepeatCurrD%:   30(1)
RForBmux:       18(2)
RisIFdata:      14(1)   20(1)   27(1)   29(1)
RmaskEn':       16(1)   29(1)
RmBypass':      22(1)
RmOdd':         10(1)   29(1)
RmPerr:         27(1)   29(1)
Rparity:        27(1)
RScopeClk0'%:   30(1)
RSTK.0:         23(1)
RSTK.0'a:       23(2)   24(1)
RSTK.0a:        22(1)   23(1)
RSTK.1:         23(1)
RSTK.1'a:       23(2)   24(2)
RSTK.1a:        22(1)   23(1)   24(1)   25(4)
RSTK.2:         23(1)
RSTK.2'a:       23(2)   24(2)
RSTK.2a:        22(1)   23(1)   24(2)   25(1)
RSTK.3:         23(1)
RSTK.3'a:       23(2)   24(2)
RSTK.3a:        22(1)   23(1)   24(2)   25(1)
SbTskDly.0':    12(1)   29(1)
SbTskDly.1':    12(1)   29(1)
SelectRm'a:     22(1)
SelectRm'b:     21(3)   22(1)
SelectStk'a:    22(1)
SelectStk'b:    21(3)   22(1)
SelRBaseWadr':  22(1)   29(1)
ShA.00:         19(5)
ShA.01:         19(4)
ShA.02:         19(5)
ShA.03:         19(4)
ShA.04:         19(5)
ShA.05:         19(4)
ShA.06:         19(5)
ShA.07:         19(4)
ShA.08:          2(1)   19(1)
ShA.09:          3(1)   19(1)
ShA.10:          4(1)   19(2)
ShA.11:          5(1)   19(2)
ShA.12:          6(1)   19(3)
ShA.13:          7(1)   19(3)
ShA.14:          8(1)   19(4)
ShA.15:          9(1)   19(4)
ShB.08:          2(1)   19(4)
ShB.09:          3(1)   19(3)
ShB.10:          4(1)   19(3)
ShB.11:          5(1)   19(2)
ShB.12:          6(1)   19(2)
ShB.13:          7(1)   19(1)
ShB.14:          8(1)   19(1)
Shc.02:         19(1)
Shc.03:         19(1)
Shc.04b:        19(3)
Shc.05b:        19(3)
Shc.06b:        19(3)
Shc.07b:        19(1)
Shc.08:          2(1)   16(1)   18(1)
Shc.09:          3(1)   16(1)   18(1)
Shc.10:          4(1)   16(1)   18(1)
Shc.11:          5(1)   16(1)   18(1)
Shc.12:          6(1)   16(1)   18(1)
Shc.13:          7(1)   16(1)   18(1)
Shc.14:          8(1)   16(1)   18(1)
Shc.15:          9(1)   16(1)   18(1)
ShcAlu.0:       18(1)
ShcAlu.1:       18(1)
ShcAlu.2:       18(1)
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ShcAlu.3:       18(1)
SHCP'C:         12(1)   20(1)
SHCP'C%:        30(1)
Shcr.08:        18(1)
Shcr.09:        18(1)
Shcr.10:        18(1)
Shcr.11:        18(1)
Shcr.12:        18(1)
Shcr.13:        18(1)
Shcr.14:        18(1)
Shcr.15:        18(1)
ShcWrite':      18(1)
ShcWrite'%:     30(1)
ShcWriteEn':    18(1)   29(1)   30(1)
ShI.00:          9(1)   19(1)
ShI.08:          2(1)   19(1)
ShI.09:          2(1)    3(1)   19(1)
ShI.10:          3(1)    4(1)   19(1)
ShI.11:          4(1)    5(1)   19(1)
ShI.12:          5(1)    6(1)   19(1)
ShI.13:          6(1)    7(1)   19(1)
ShI.14:          7(1)    8(1)   19(1)
ShI.15:          8(1)    9(1)   19(1)
Shift':         13(1)   16(3)   19(1)   20(1)   29(1)
ShiftMuxEn':    19(1)
shmv.08:         2(1)   16(1)   29(1)
shmv.09:         3(1)   16(1)   29(1)
shmv.10:         4(1)   16(1)   29(1)
shmv.11:         5(1)   16(1)   29(1)
shmv.12:         6(1)   16(1)   29(1)
shmv.13:         7(1)   16(1)   29(1)
shmv.14:         8(1)   16(1)   29(1)
shmv.15:         9(1)   16(1)   29(1)
SHSelect'C:     11(1)   22(1)
SHSelect'C%:    30(1)
SHSelect'D:     22(4)   23(1)   24(1)
SHSelect'D%:    30(1)
SimHold.0:      26(2)
SimHold.4:      26(2)
SimHoldDis:     24(1)
SimHoldReq':    24(1)   26(1)
StartCycle'a!%: 30(1)
StkAdr.0a:      25(1)
StkAdr.0b:      21(1)   25(1)
StkAdr.1a:      25(1)
StkAdr.1b:      21(1)   25(1)
StkAdr.2a:      25(1)
StkAdr.2b:      21(1)   25(1)
StkAdr.3a:      25(1)
StkAdr.3b:      21(1)   25(1)
StkAdr.4a:      25(1)
StkAdr.4b:      21(1)   25(1)
StkAdr.5a:      25(1)
StkAdr.5b:      21(1)   25(1)
StkAdr.6a:      25(1)
StkAdr.6b:      21(1)   25(1)
StkAdr.7a:      25(1)
StkAdr.7b:      21(1)   25(1)
StkBypass':     22(1)
StkError:       24(1)   29(1)
StkP.0:          2(1)   22(1)   25(5)
StkP.1:          3(1)   22(1)   25(5)
StkP.2:          4(1)   22(1)   24(1)   25(4)
StkP.3:          5(1)   22(1)   24(1)   25(4)
StkP.4:          6(1)   22(1)   24(1)   25(4)
StkP.5:          7(1)   22(1)   24(3)   25(4)
StkP.6:          8(1)   22(1)   24(2)   25(3)
StkP.6':        24(3)   25(2)
StkP.6/7:       24(2)
StkP.7:          9(1)   22(1)   24(2)   25(3)
StkP.7':        24(2)   25(2)
StkPMux1:       24(1)   29(1)
StkPSave.0:     25(1)
StkPSave.1:     25(1)
StkPSave.2:     25(1)
StkPSave.3:     25(1)
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StkPSave.4:     25(1)
StkPSave.5:     25(1)
StkPsave.6:     25(1)
StkPSave.7:     25(1)
StkPSaveEn':    23(1)   24(1)   29(1)
StkPWriteEn':   24(4)   29(1)
StkSel'a:       12(1)   22(3)   24(3)
StkSela:        12(2)   22(2)   24(1)   29(1)
StkSelSaved:    12(1)   29(1)
StkWadr.0:      22(1)   25(1)
StkWadr.1:      22(1)   25(1)
StkWadr.2:      22(1)   25(1)
StkWadr.3:      22(1)   25(1)
StkWadr.4:      22(1)   25(1)
StkWadr.5:      22(1)   25(1)
StkWadr.6:      22(1)   25(1)
StkWadr.7:      22(1)   25(1)
StkWSel':       22(3)   24(1)
SubTask.0:      12(1)   23(1)
SubTask.1:      12(1)   23(1)
T.08:            2(5)   27(1)
T.09:            3(5)   27(1)
T.10:            4(5)   27(1)
T.11:            5(5)   27(1)
T.12:            6(5)   27(1)
T.13:            7(5)   27(1)
T.14:            8(5)   27(1)
T.15:            9(5)   27(1)
T.Perr':        27(2)
TbBypass:       20(1)   27(1)   29(1)
TbSelMd:        20(2)   29(1)
TbWrite'a:      21(1)
TbWrite'a%:     30(1)
TbWrite'b:      21(1)
TbWrite'b%:     30(1)
TbWriteEn':     20(2)   29(1)   30(1)
TempRef!:       26(1)
TempSense:      29(1)
TempSense!:     26(1)
TisIFdata:      14(1)   20(1)   27(1)   29(1)
TmPerr:         27(1)   29(1)
Tparity:        27(1)
TrueA:           4(1)    5(1)   18(1)   23(3)   26(1)   27(3)
                30(1)
UFLerr':         3(1)   24(1)
VCC:            26(1)
VEE:            26(1)
Whatever:       26(1)   28(1)
←MD:            29(1)
←MD!:           20(1)
←MD'Dly:        20(1)   27(1)
←MDI:           20(1)   29(1)
←MDI':          20(1)   27(1)
←MDSaved:       20(1)   29(1)
```