DOLCH
LOGIC INSTRUMENTS

OPERATOR'S MANUAL FOR

AREA TRACE OPTION (ATO)

AND

EXTENDED AREA TRACE OPTION (EATO)

PUBLICATION NUMBER: 108330NA

DOLCH
LOGIC INSTRUMENTS

CHANGES TO THIS MANUAL

This manual will be changed periodically to keep it current with improvements as we make them. Changes start with Service Notes that alert field service technicians to critical problem areas and changes in maintenance procedures. After a series of these notes are issued or a critical one is issued, we will publish change pages. which are the remove-the-old and insert-the-new type. When the company prepares a change package. it sends announcements to its users. The change packages are available upon request and without charge.

Record of Changes

The record of Changed Pages lists all the pages in this book. that are deleted. changed pages, added pages, and foldout pages.

Reader Comment Form

We have supplied the reader comment form (at the back of this manual) to get feedback from our customers. If you are dissatisfied with this publication, we want to hear from you. Tell us about inaccurate information. typographical errors, or missing information. If you know a way to improve a procedure. please let us know about that, too. When filling out the form. please be specific and give the page number. line reference, and the paragraph number, if possible.

RECORD OF CHANGES

CHANGE NUMBER	DATE	TITLE OR BRIEF DESCRIPTION	ENTERED BY (NAME, DEPT.)

WARRANTY

All Dolch Instruments products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, per exceptions as noted in the price lists. In the event of a breach of Dolch Instruments warranty, Dolch Instruments shall have the right in its discretion either to replace or repair the defective goods. There shall be no other remedy for breach of the warranty. In no event shall Dolch Instruments be liable for the cost of processing, lost profits, injury to goodwill, or any special. consequential or incidental damages. The foregoing warranty is exclusive of all other warranties. whether expressed or implied, including any warranty or merchantability or fitness for a particular purpose.

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Dolch Area Trace Option (ATO) and the Extended Area Trace Option (EATO) allow for the selective recording of specific parts of a microprocessor program, based upon a 16-bit address. Only areas (or address ranges) programmed in the AREA TRACE MENU are recorded by the analyzer; all other areas are ignored.

NOTE

When the EATO is installed, the 2K and Latch Modes are not available. When the ATO is installed, the 2K Mode is not used, but the Latch Mode is still available. For both the ATO and EATO, the maximum clock rate is 100 nS (10 MHz).

1.2.1 Area Trace Option

Up to ten specific areas of interest may be programmed for dynamic, non-sequential recording. This allows for more effective use of the Logic Analyzer's memory, and enhances data analysis. A typical application would be to selectively choose areas of programs whose operation or funtion is not completely understood. This way routines that jump to unanticipated locations, for example, can be easily isolated by comparing them with known areas.

1.2.2 Extended Area Trace Option

In addition to those features offered by the ATO, the EATO allows the user to view data entering memory a few samples before (History) and a few samples after (Future) the area programmed for trace. This is the only functional difference between the two options. In terms of hardware, the EATO requires the replacement of more Input PCBs with Extended Area Trace PCBs in the host analyzer.

1.2.3 Statistical Analysis

Software revisions "D" and later provide the additional capability of statistical analysis of recorded data in the Source Memory. The results of this analysis may be displayed in graphic or tabular form. The number of recorded samples which fall within each programmed area, and their percentage of the total samples, is displayed.

1.2 ATO/EATO REFERENCE DATA

Table 1-1 shows specifications for both the ATO and EATO.

TABLE 1-1. ATO/EATO Specifications
POWER REQUIREMENTS: None needed. ATO and EATO use the host Logic Analyzer's power supplies.
AREA: NUMBER - 10 areas may be selected for tracing within the memory locations 0000 to FFFF WIDTH - 1 to 65,536 addresses. LIMITS - Area limits are selected by programming upper and lower ranges on keyboard or by remote control.
EXTENDED AREA: HISTORY - Used only in EATO. User may select up to seven samples of data recorded before a specified area. FUTURE - Used only in EATO. User may select up to seven samples of data after a specified area.
INPUTS: CHANNEL GROUPS - Pods E & F only are used for ATO. F7 is MSB and E0 is LSB. All Pod groups are used by EATO. PROBES - Personality Probes are used to interface the Host Analyzer to microprocessor or SUT.
SAMPLING: Area Trace ON - 10 MHz max. Area Trace OFF - 20 MHz max. Min. Clock pulse width - 25 nS.

SECTION 2

INSTALLATION

2.1 GENERAL

The ATO and EATO consist of hardware and software that are to be installed and tested at the factory.

2.2 INITIAL TURN-ON/CHECK-OUT

After the power-up, the software directory should display the following:

9.4851 - 08 X - AREA TRACE OPTION

("X" is the sotware revision number.)

SECTION 3

THEORY OF OPERATION

3.1 GENERAL

This section is divided into two parts: a functional description and a theory of operation. The description is for both the ATO and the EATO.

3.2 FUNCTIONAL DESCRIPTION

We will briefly leave the realm of high-tech documentation to explain the functional relationship between normal logic analyzer operation and the ATO and EATO. Figure 3-1 shows a simplified (albeit non-technical) illustration of a logic analyzer. As an example, in the FREE RUN mode, the analyzer's control logic causes sampling of data from the System Under Test (SUT) in accordance to a program entered through the operator controls. The analyzer simply fills its memory with data to the limit of its capacity when a recording is begun. Various methods of analysis are then available to the operator. This is fine if all data to be extracted from the SUT can be contained in the analyzer memory.

Most times this is not a useful method of capturing complex operations, such as loops, subroutines, interrupts, jumps to other fields, etc. A means ot optimizing the memory capacity of the analyzer is offered with the ATO. With this option, the analyzer can be instructed to ignore (open the memory lid and throw away) all extranneous or unwanted data, and store only those of particular interest.

3.2.1 Area Trace Function

Figure 3-2 shows the operation of the ATO in flowchart form. Up to ten areas of data can be stored away in memories labled "Area Containers" in the illustration. The total number of addresses cannot exceed 64K, so the individual containers are equally divided into 10 parts. The size of the containers can, of course, be smaller. For large programs the area segments can be programmed to trace data in a sequential manner. Note that the areas programmed for trace can be defined in any size or shape desired.

The ATO provides vastly more capabilities than the standard analyzer functions because the operator can trace only that data of interest, rather than having to rely on luck. It is not so good if you are interested in how all these pieces relate to one another (unless you already know!). The Extended Area Trace Option is especially useful for such "detective" work.

3.2.2 Extended Area Trace Function

The EATO provides all capabilites of the ATO, in addition to the ability to examine a programmable number of samples before and/or after the areas traced. Figure 3-3 shows the EATO operation in flowchart form.

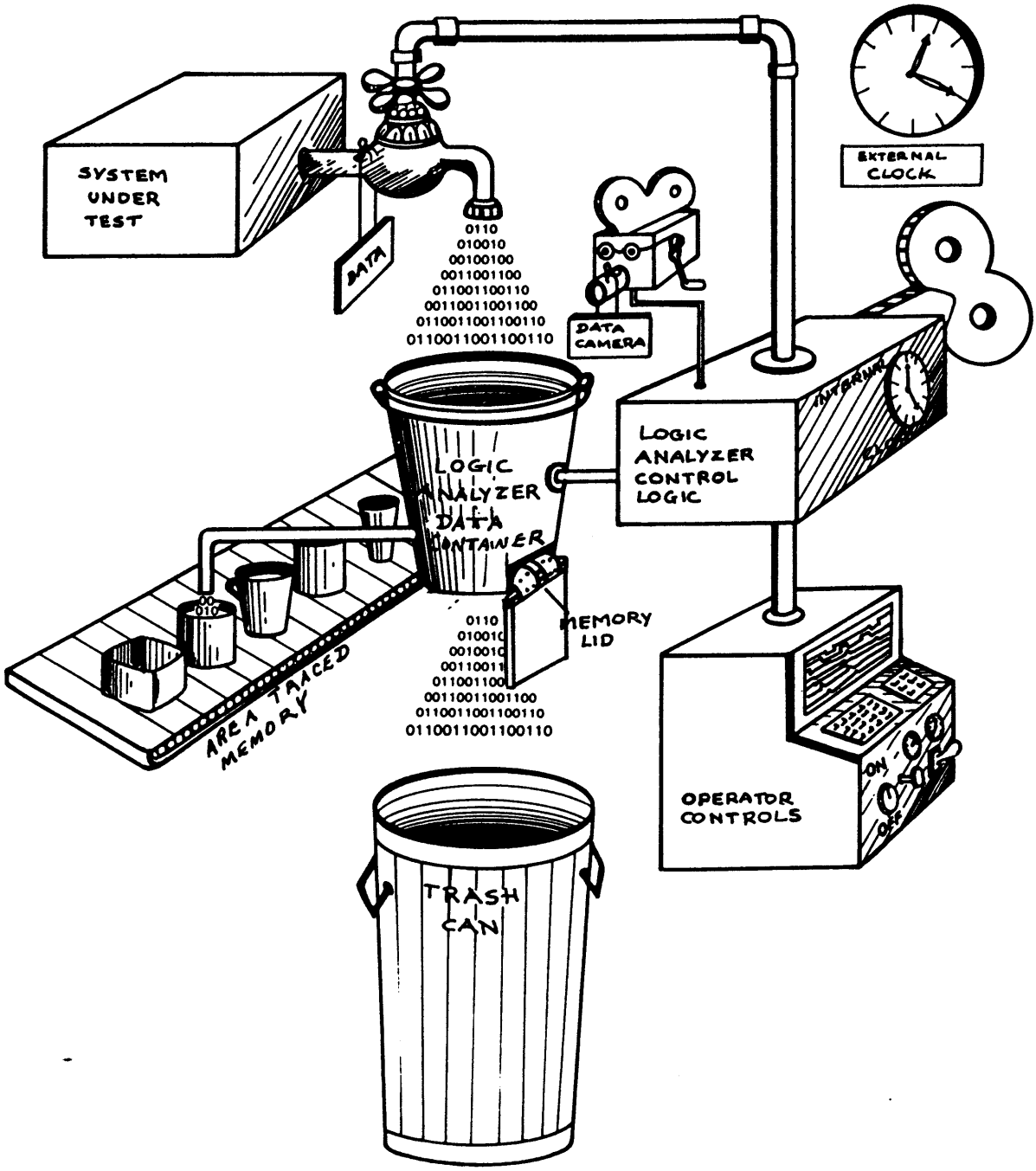


Figure 3-1. Logic Analyzer Functional Illustration

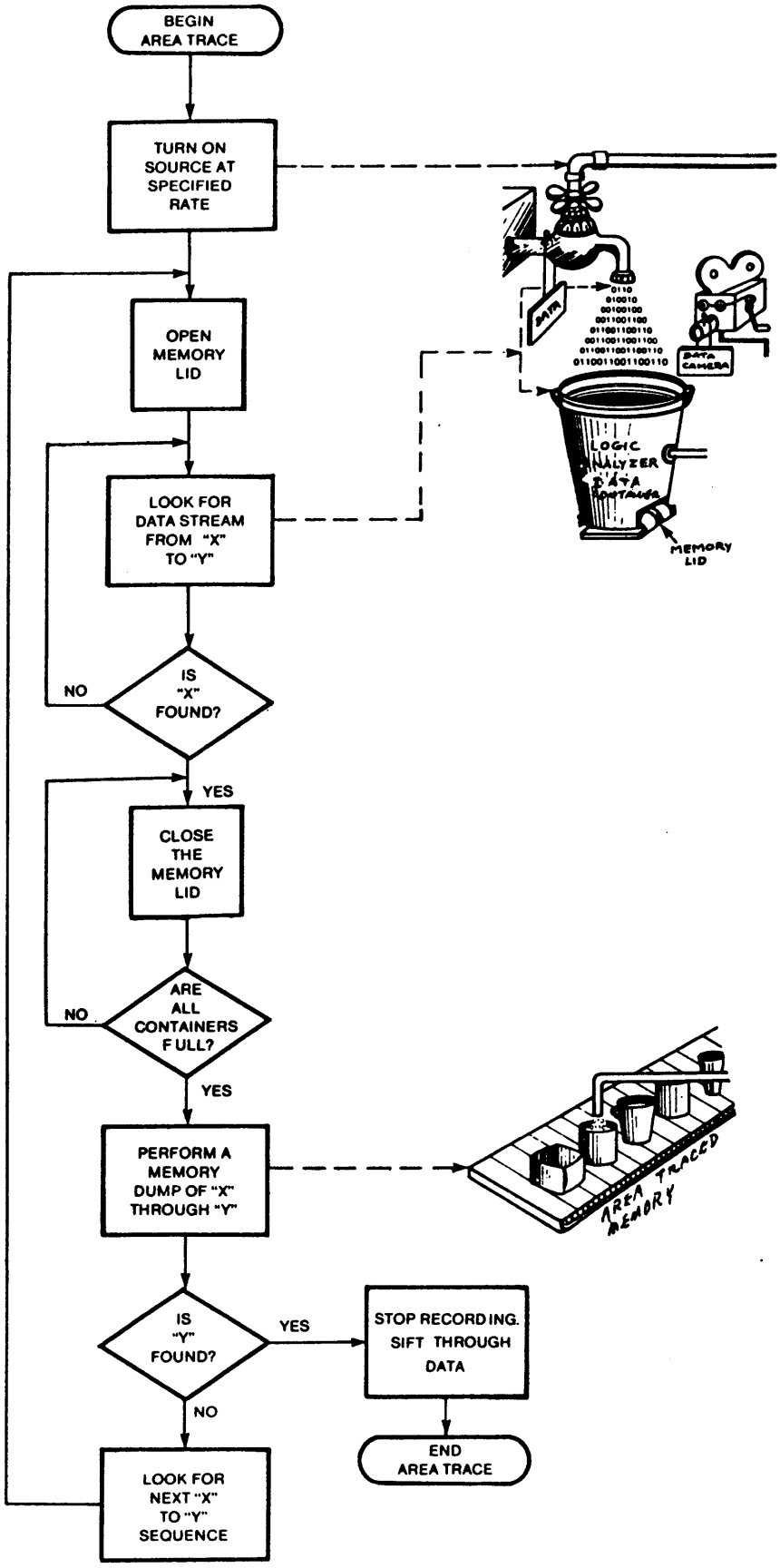


Figure 3-2. Area Trace Operation

As an example of the importance of this feature, note the following sentence: THE SUBROUTINES ARE HARDWARE ORIENTED. Imagine that this data is analogous to a stream of information coming from the SUT. With the ATO, the operator would possibly select this portion of the sentence: ROUTINES ARE HARD. This message is valid, but obviously does not reveal the full context of the sentence. With the EATO, the area selected could be extended by several samples either before (History) or after (Future) the area defined. This would allow for the following variations: ROUTINES ARE HARDWARE, or THE SUBROUTINES ARE HARD".

Note that the total number of programmed samples must not exceed seven. This means that the operator can select 3 "FUTURE" and 4 "HISTORY" samples, 7 "HISTORY" and 0 "FUTURE", and so on. Thus, it can be seen that the EATO is wonderful for everything from analyzing program jumps to finding marigolds in moonbeams! (EDITOR'S NOTE: The writer of section 3.2 has been reassigned to other duties.)

3.3 THEORY OF OPERATION

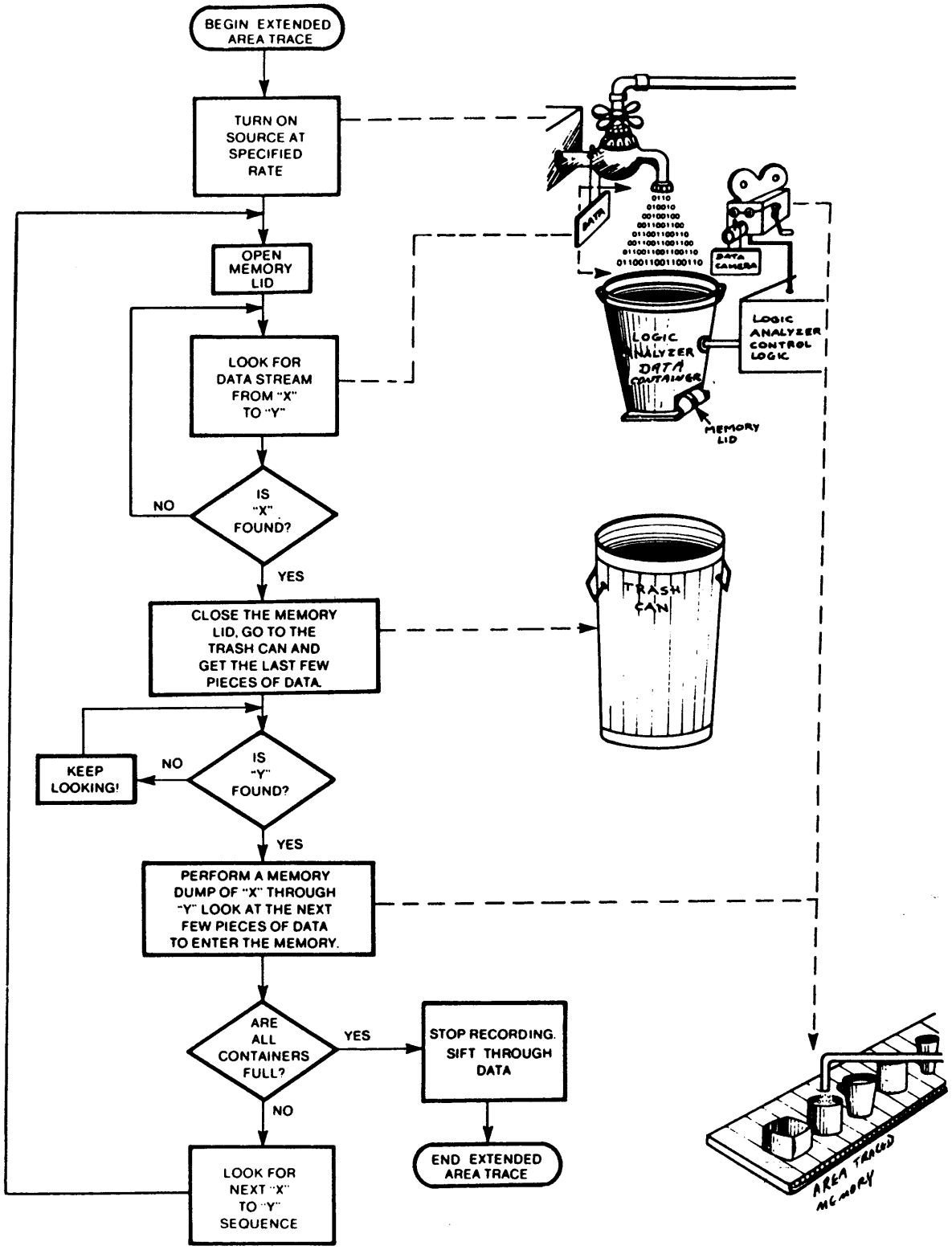
In this section we will return to the realm of high-tech documentation to explain the theory of operation of the ATO and the EATO. This discussion is linked to functional block diagrams that are keyed to the following text.

3.3.1 ATO PCB

The Area Trace PCB is similar to a standard Input PCB (without the glitch capturing circuits), with the addition of a counter/latch and four Word And Area Recognizer RAMs (each 16K). These RAMs are loaded with the specified area information before recording begins, and then sample the input data stream during recording. If the incoming data matches that specified, an enable signal is sent to both the Trigger PCB and the DAB (SBLA) PCBs, and a recording is allowed for the duration of the area. This action is represented by Figure 3-2, where the "Data Camera" recognizes the first word of the area, causes the "Memory Lid" to close, looks for the last word in the area, and then a memory dump is performed to the "Area Containers".

See Figure 3-4 for a functional block diagram of the ATO PCB. The Standard Area Trace Option requires the installation of a PROM onto the Memory 2 PCB, which holds the program for the AREA TRACE MENU and clock qualification data, and the replacement of the Input PCB E&F with the Standard Area Trace PCB.

3.3.1.1. ATO PCB Functional Block. Input data enters from Pod E and Pod F, ①, and is translated from ECL to TTL level through the Receiver/Buffer circuits, ②. These signals then pass through Buffers, ③, to the Latch/Counters, ④. During recording, input data is latched into these ICs by a clock signal derived from the Timebase PCB called "0 LATCH F" and "0 LATCH E". Once latched, data goes to the DAB PCBs for recording, ⑧.



* Number is pre-programmed used for "HISTORY"

** Number is pre-programmed used for "FUTURE"

Figure 3-3. Extended Area Trace Operation

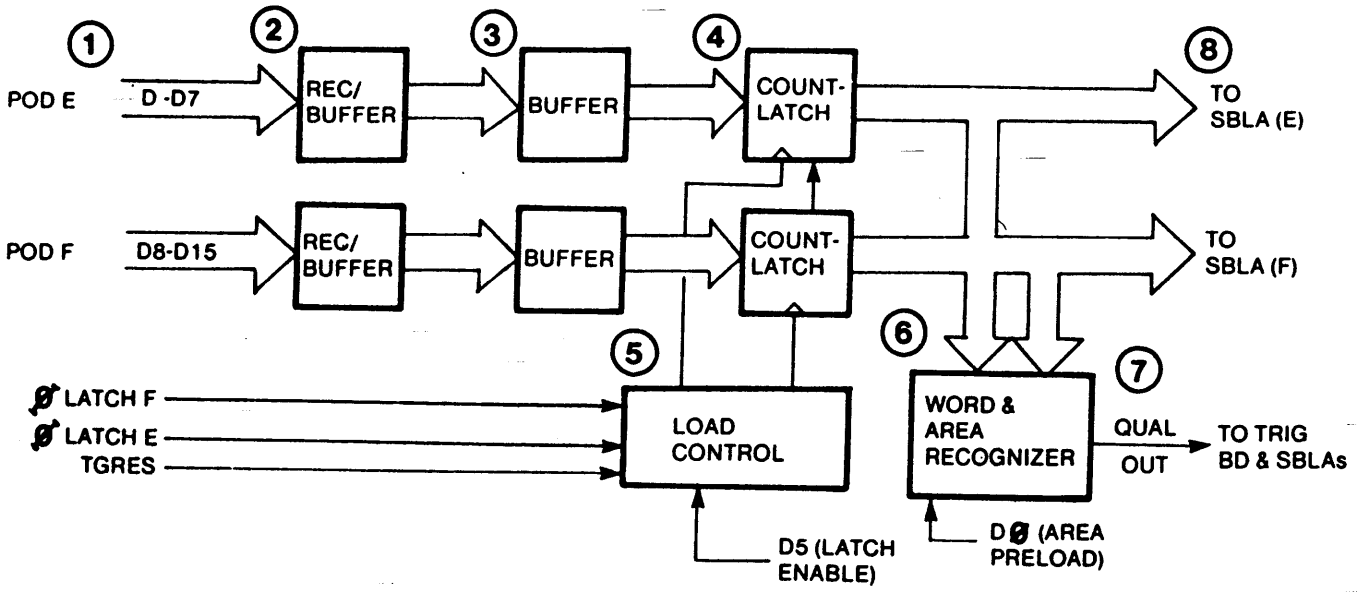


Figure 3-4. Area Trace PCB Functional Block

The Latch/Counters, ④, are also used to load the area trace "Word And Area Recognizer" RAMs, ⑤. This is done by clearing the counters with the "TRIGGER RESET" (TGRES) signal. When cleared, a count enable signal from the Data Bus forces the Counters to count. Simultaneously, a count signal from the address lines (which goes into the Load Control, ⑤) A0-A7 is decoded by a PROM and is applied to the clock input of the Counters. Area Trace information is sent to the Word And Area Recognizer, as the Counters are counting, from the Data Bus. The RAMs are write-enabled only when the Load Control PROM is instructed to decode the address lines. This decode signal originates from the CPU PCB.

Only after the Word And Area Recognizer information has been written into the RAMS, are the Latch/Counters returned to the latch mode. It is then that a recording can take place. Input data is thus sampled by the address lines of the RAMs. Any data which matches the stored information causes the "QUALIFY OUT", ⑦, signal to go to the Trigger and remaining three DAB PCBs. This causes the delay counter on the Trigger PCB, and the DAB RAMs to be active only on data which is to be recorded.

3.3.2 EATO PCBs

The EATO requires the installation of two PROMs onto the Memory 2 PCB, a Master Extended Area Trace PCB that replaces the Standard Input E&F (or Standard Area Trace PCB), and two Slave Extended Area Trace PCBs that replace the Standard Input PCBs for A&B, and C&D. (EDITOR'S NOTE: The writer of section 3.2 wanted to use acronyms for the two board configurations of the EATO. He was flatly rejected.)

Each Slave Extended Area Trace PCB has eight dual 8-bit shift registers (labled "Delay Registers" in Figure 3-5), which delay the data coming out of the Input Latches by 8 recording clock cycles. Thus, all Input PCBs must be replaced because they must all equally postpone the input data. This delay makes the data available for recording after the specified trace area has been identified by the Master Extended Area Trace PCB. The Slave Extended Area Trace PCBs have elements of the Standard Input PCB and the Master Extended Area Trace PCB. Simply put, they must also perform as Standard Input PCBs when the EATO is not selected.

3.3.2.1. Master EATO PCB Functional Block. Figure 3-5 shows a functional block diagram of the Master Extended Area Trace PCB. Shaded blocks indicate those parts of circuitry that the Slave Extended Area Trace PCBs do not share with the Master. The Master EATO PCB has two additional shift registers, which are used to control the delay of the qualification signal to both the Trigger and two Slave EATO PCBs. These shift registers, as with the Standard ATO PCB, are loaded with the number of samples before the recording begins. They are also instructed how to set the actual delay that achieves the specified number of samples. These parts of circuitry are represented in Figure 3-5 as circle numbers ⑥, ⑧, ⑨, and ⑩, respectively.

With the exception of some portions of the Area And Word Recognizer, 6 , the Delay Control, ⑧, and the Delay Registers, ⑩, circuits, the Master EATO PCB operates in the same manner as the Standard ATO PCB. Therefore, only these differences will be discussed.

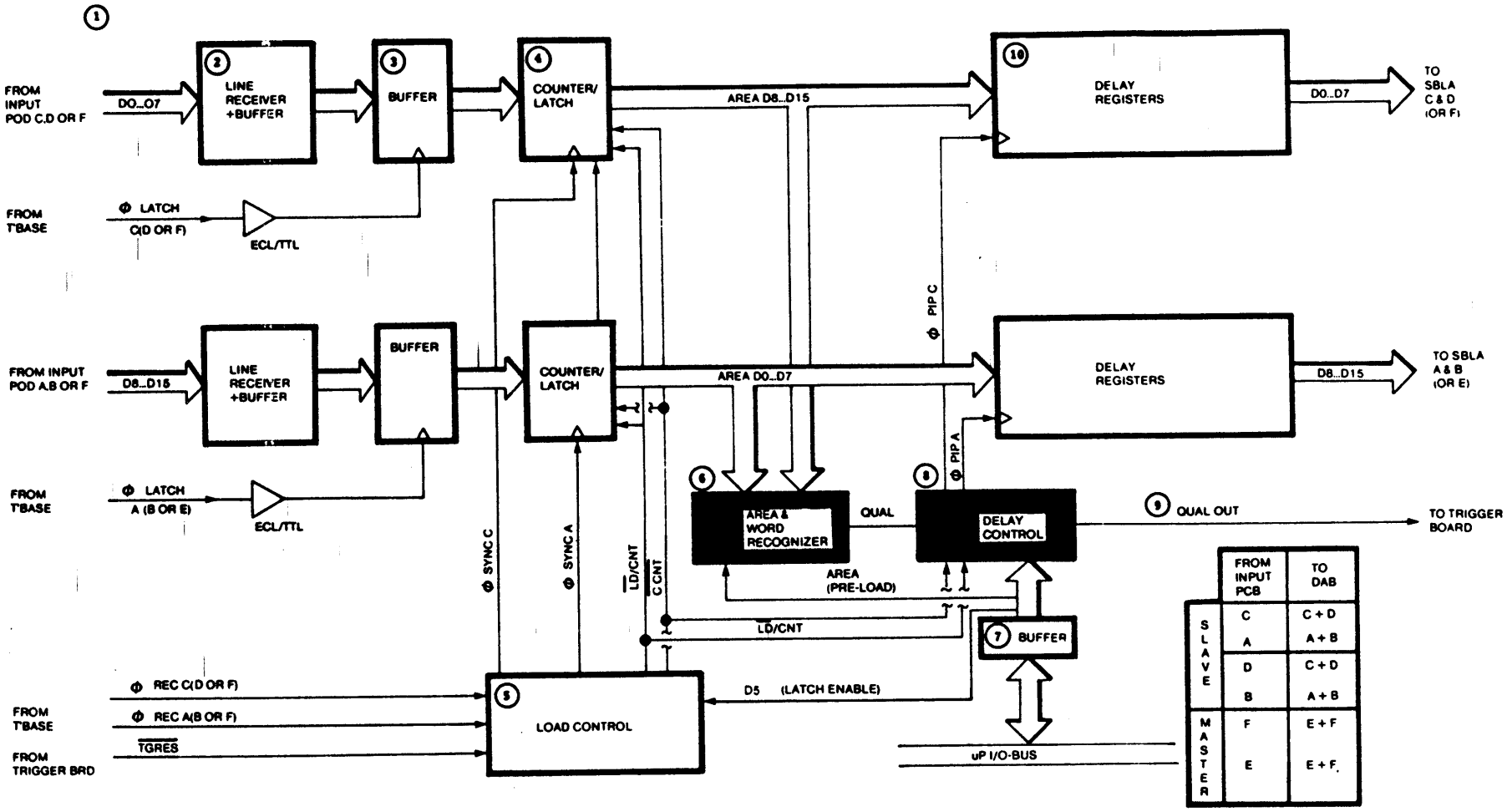


Figure 3-5. Master Area Trace PCB Functional Block

Incoming data is delayed when it is received from the Counter/Latches, 4 , by the Delay Registers, which are 8-bit (serial in-serial out) shift registers. Each register is enabled by a gated signal originating from TGRES and the Data Bus line D3. Each register is clocked by recording clock E or F. When recording, all data to the Slave EATO PCBs is thus postponed by eight clock cycles, which allows the time needed to record up to seven data samples prior to entering the specified trace area. This action is at the heart of the operation referred to as "History" and "Future". Put in simpler terms, these shift registers allow the host analyzer to both "go to the trash can" for history, and to "look at data with the Data Camera" to find the future samples. (EDITOR'S EDITOR'S NOTE: The writer of section 3.2 is now manager of the documentation department.)

Figure 3-6 shows how the "History" Delay operates. This function is analogous to the analyzer being told when to shut the "Memory Lid" and how many samples to get from the "Trash Can" in Figure 3-3. The same gated signal that enables the Delay Registers, ⑩ , also enables the Shift Register in the Word And Area Recognizer circuit, ⑥ . A 3-bit signal from the Data Bus Latch (D0, D1, D2) selects the pre-trace delay in the History Delay Data Selector. As the QUALIFY signal leaves the 64K RAMs, it is passed to the Delay Control, ⑧ , through the Shift Register and History Delay Data Selector. The number of History samples programmed is derived from the Load Control, ⑤ , which provides a clock signal for the F1 Latch.

Figure 3-7 shows how the "Future" Delay operates. This function is analogous to the analyzer being told to look for the next few pieces of data that will enter the "Memory Bucket" with the "Data Camera" in Figure 3-3. Again, the TGRES/D3 signal is applied to the Shift Registers to enable them, and the QUALIFY signal from the History Delay Data Selector (in ⑥), which latches them into the sample mode. The "Future" delay information is clocked into the Latch by the clock signal F2, which comes from the Load Control circuit, 5 . During recording, this information is entered into the Shift Registers (parallel in-parallel out) and their associated Gates. At the end of each block of qualified data, the QUALIFY signal is shifted the programmed number of clock cycles, extending the signal BEYOND THE QUALIFIED RANGE. This shift from the qualified area thus causes "Future" data to be sampled after each block of the area desired.

By combining the "History" delay and "Future" delay, the QUALIFY signal is consequently extended up to seven clock cycles. This results in a recording which includes samples before and after the selected block of data. Figure 3-8 illustrates this point.

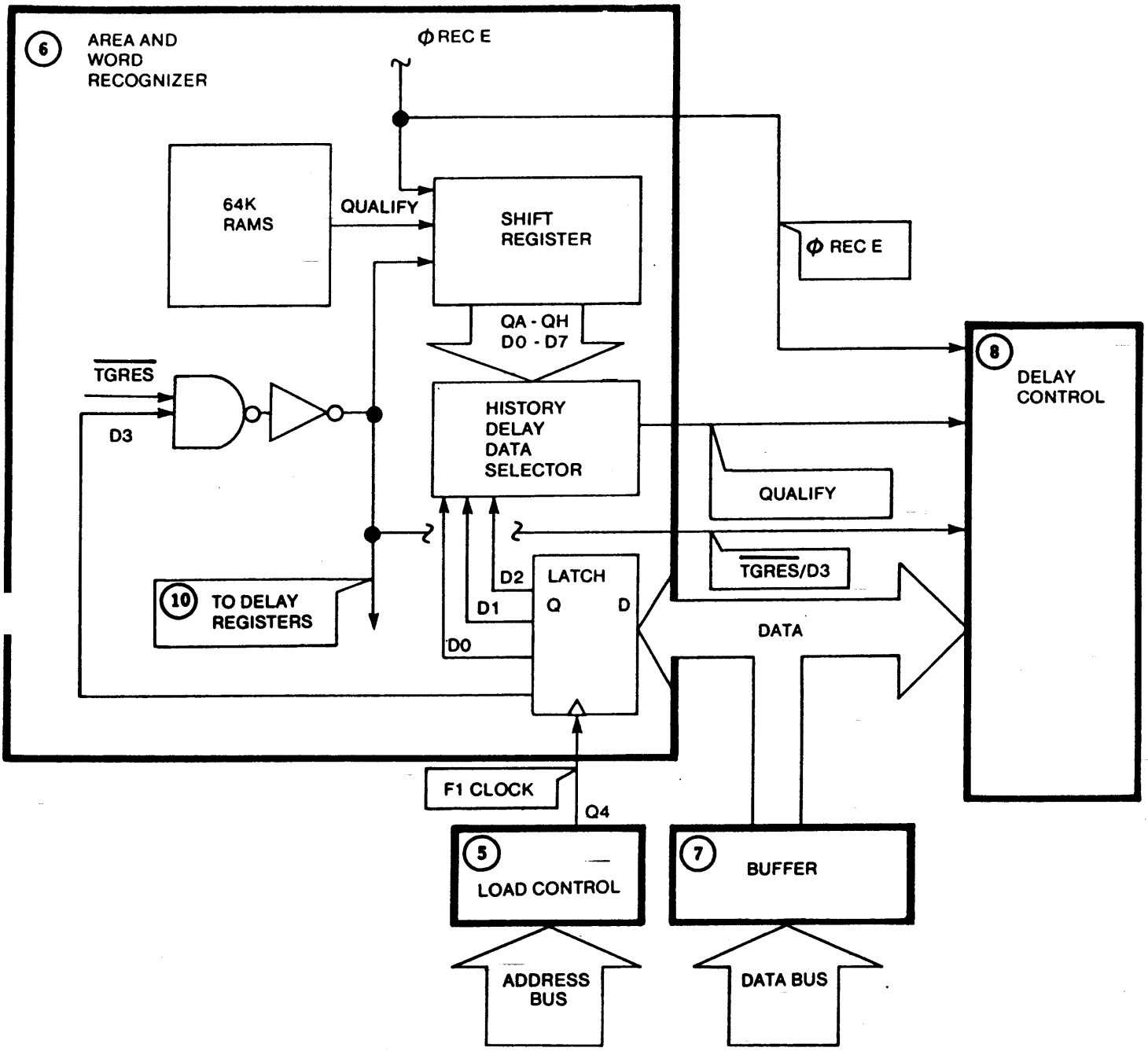


Figure 3-6. History Delay Operation

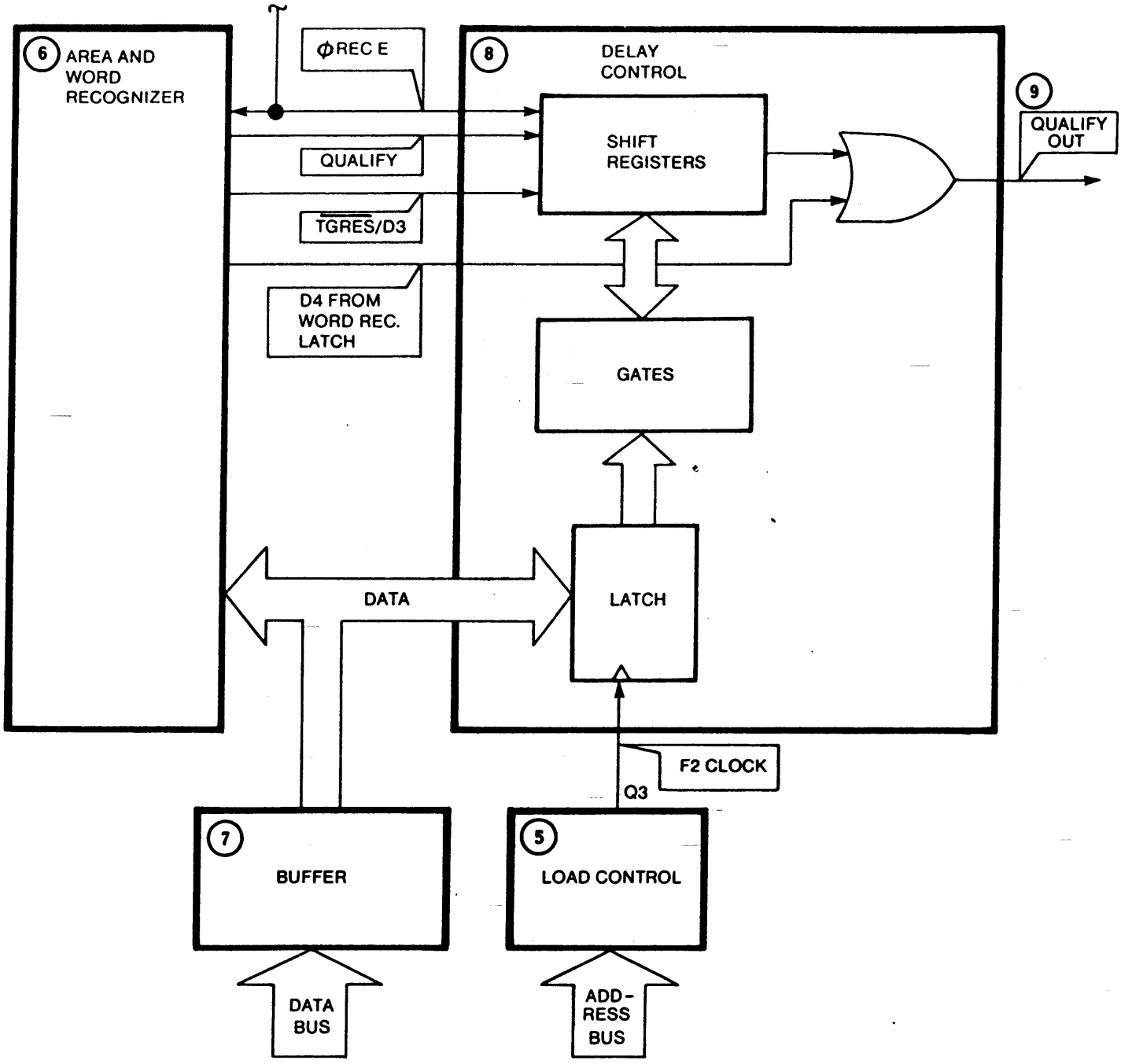


Figure 3-7. Future Delay Operation

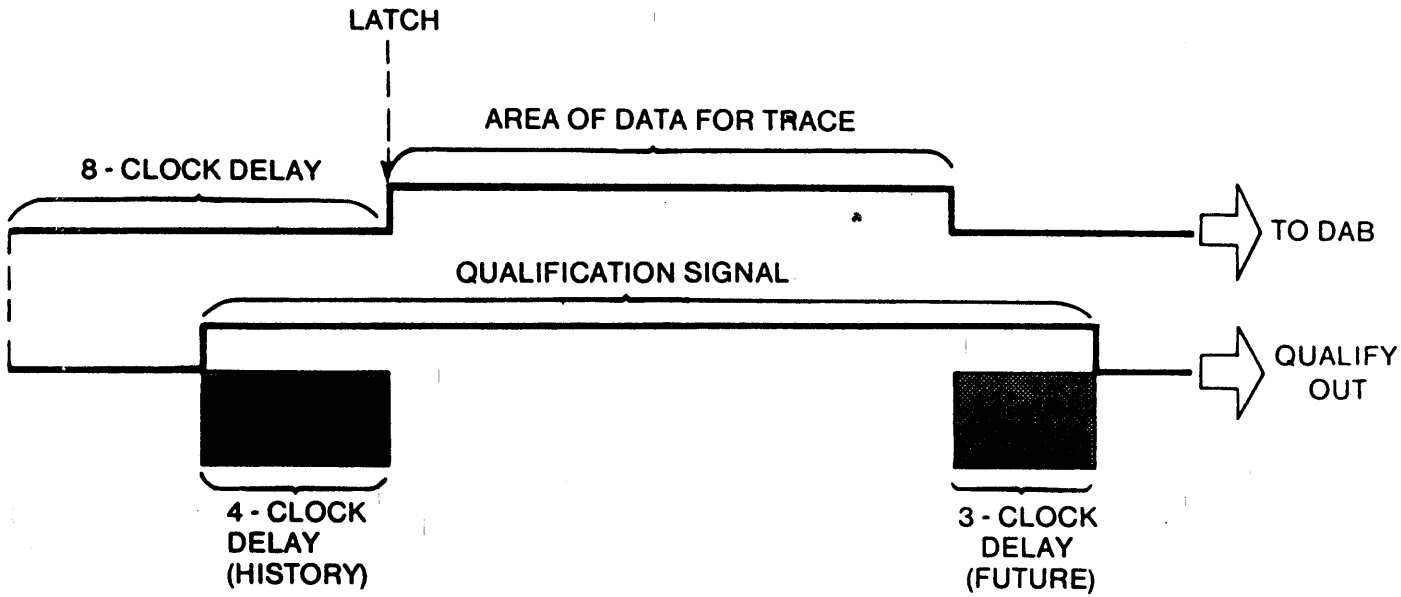


Figure 3-8. History And Future

SECTION 4

OPERATING PROCEDURES

4.1 INTRODUCTION

The means of accessing and operating the ATO and EATO are presented in this section. Refer to the host analyzer Operator's Manual for details on controls and displays used with the analyzer.

The ATO and EATO offer three displays:

- MENU
- VIEW (HISTOGRAM)
- TABLE

The MENU is used for programming parameters. The VIEW and TABLE are used to analyze the results of the areas traced; VIEW shows a bar graph representation and the TABLE gives results in tabular form.

4.2 OPERATING CONTROLS

The ATO/EATO is accessed in the following manner:

1. Set the Power Switch ON. Verify that the "POWER UP SELF TEST COMPLETE!" display shows the AREA TRACE as an identified software package.

2. Press the MENU pushbutton until the AREA TRACE MENU is displayed.

To gain access to the VIEW and TABLE Displays, enter the AREA TRACE MENU and press the "HOME" pushbutton. Press the "ROLL" pushbutton once for the "VIEW" Display, and press it again to access the "TABLE" Display. To return to the AREA TRACE MENU, press the "ROLL" pushbutton a third time.

4.2.1 ATO/EATO Display

Figure 4-1 shows the display as it appears on the CRT for both the ATO and EATO. Table 4-1 identifies the elements of the display.

4.2.2 VIEW Display

Figure 4-2 shows the VIEW display. Table 4-2 identifies elements of the display.

4.2.3 TABLE Display

Figure 4-3 shows the TABLE display. Table 4-3 identifies elements of the display.

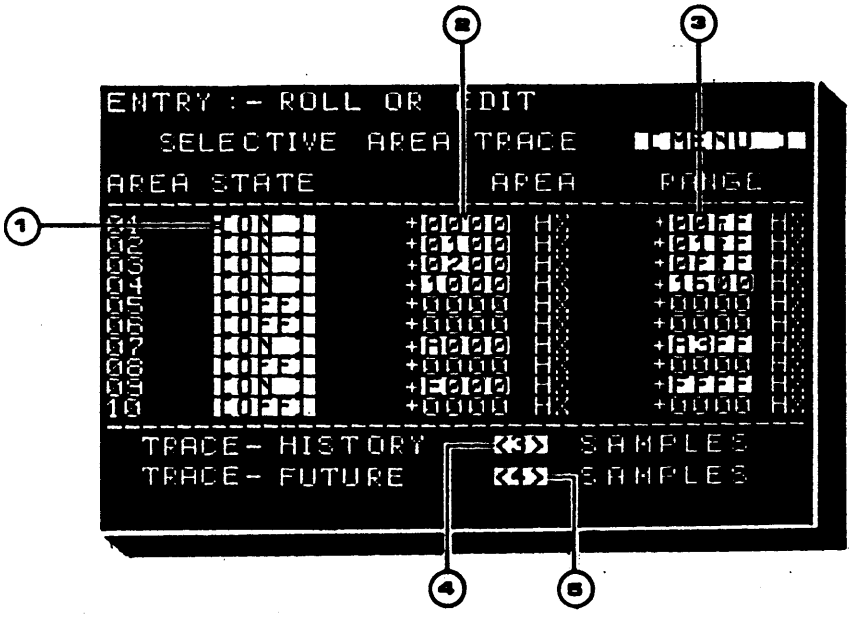


Figure 4-1. Area Trace Menu

TABLE 4-1. Area Trace Menu Elements

LOC. COR.	FIELD HEADING	PARAMETERS	DESCRIPTION
1	TRACE POD	E+F (ON) ---(OFF)	Indicates status of Pod Group for recording.
2	RANGE	FROM (0000-FFFF)	First two digits assign the value for E Pod. The last two digits assign the value for F Pod. These values mark the beginning location of the area to be traced.
3		TO (0000-FFFF)	Pod Assignment is the same as for Item 2. These values mark the end location of the area to be traced.
4	TRACE HISTORY	0 - 7	Field used to program the number of locations to be sampled before the area traced.
5	TRACE FUTURE	0 - 7	Field used to program the number of locations to be sampled after the area traced.

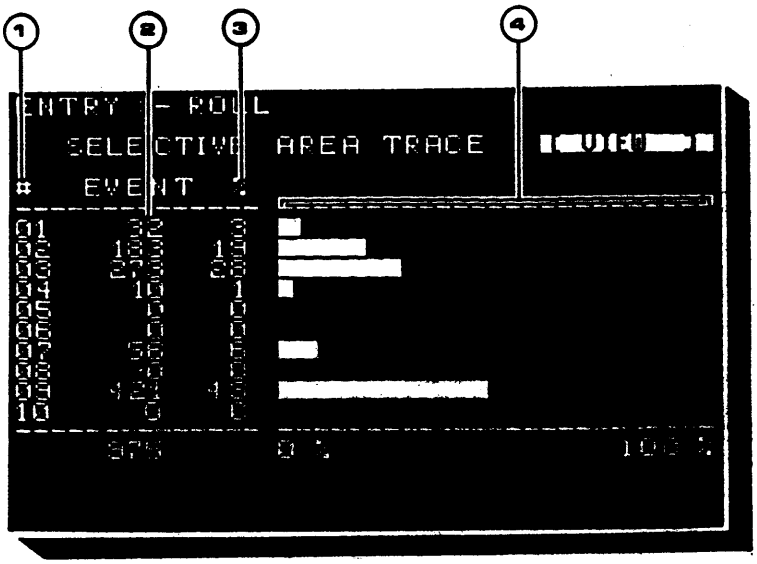


Figure 4-2. Area Trace View Display

Table 4-2. VIEW DISPLAY Elements

LOC. COR.	FIELD HEADING	PARAMETERS	DESCRIPTION
1	#	1 - 10	Number assigned to area traced.
2	EVENT	0 - 1000	Indicates number of times an area occurred.
3	%	0 - 100	Indicates the percentage of the total memory the area occupies.
4	GRAPH		Bar graph indicating percentage of memory for each area traced.

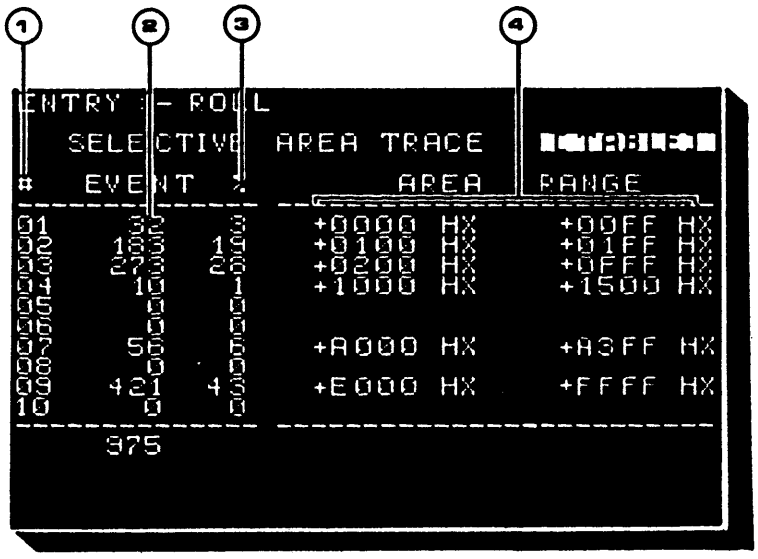


Figure 4-3. Area Trace Table Display

Table 4-3. TABLE DISPLAY Elements

LOC. COR.	FIELD HEADING	PARAMETERS	DESCRIPTION
1	#	1 - 10	Number assigned to area traced.
2	EVENT	0 - 1000	Indicates number of times an area occurred.
3	%	0 - 100	Indicates the percentage of the total memory the area occupies.
4	AREA	0000-FFFF	Indicates the addresses of the area traced.

4.3 MODES OF OPERATION

The ATO/EATO must be programmed before a recording is begun. Note that the "HISTORY" and "FUTURE" fields are displayed on the menu, but are non-functioning with the Standard ATO installed. Once a recording has been made, the areas traced may be velwed with either the TIMING DIAGRAM or the LIST DISPLAY. All memory and search functions are available after the recording.

4.3.1 Operating Procedures

After power up test completion, the AREA TRACE MENU can be programmed from either the keyboard, GPIB, or RS-232 interfaces. It is recommended that all other aspects of the recording are programmed prior to operating the AREA TRACE MENU. See the host analyzer's Section 5, Operating Procedures for details of Pre-Record programming procedures.

4.3.1.1. Programming From The Keyboard. Program the AREA TRACE MENU using the standard procedures found in Section 5 in the host analyzer's Operator's Manual under Basic Programming Rules. Proceed as follows:

1. Use the "EDIT" pushbuttons to move the Cursor to the fields desired.

2. Use the "ROLL" pushbutton to turn Pod Groups ON and OFF.

3. To enter FROM/TO addresses:
   A) Press the "ENTER" pushbutton.
   B) Enter the value desired for the first blinking Cursor field with "ENTRY" group pushbuttons.
   C) Use "EDIT" pushbutton Cursor controls to move to next digit field.
   D) When all values are set, press the "ENTER" pushbutton.

4. To enter TRACE - HISTORY/FUTURE sample numbers:
   A) Use the "dec - 8" pushbutton to lower a value displayed.
   B) Use the "inc - 9" pushbutton to raise a value displayed.

5. Press the "HOME" pushbutton and then press tne "ROLL" pushbutton. The Analysis cycle is begun, and is indicated by the flasning inverse video message "ANALYZER IS ACTIVE!". The "VIEW" display is shown at the completion of this action.

4.3.1.2 Further Analysis. Any number of data analysis can be made once the recorded data is in the Source Memory. A particular area of interest can be divided into several smaller sub-areas, and the analysis can be repeated without the need to make a second recording. For example, assume that data in the area range from 0200 to OFFF is traced in area #03. To see a further breakdown of that data, perform the following steps:

1. Enter the AREA TRACE MENU using the "ROLL" pushbutton.

2. Advance the cursor to AREA STATE #01 and turn it ON. Set area from 0200 to 0250.

3. Advance the cursor to AREA STATE #02 and turn it ON. Set area from 0250 to 0350.

4. Advance the cursor to AREA STATE #03 and turn it ON. Set area from 0350 to 0FFF.

5. Press and release the "ROLL" pushbutton. The Analyzer will begin another analysis cycle and then show the results in the "VIEW" display.

Note that previously recorded data can be uploaded from a computer through the GPIB or Serial Interface and analyzed at a later time. Recording and analysis function are completely separate.

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