# EMULOGIC

# 6502

# User's Guide Supplement

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# 6502 USER'S GUIDE SUPPLEMENT


This document supplements the ECL-3211 System User's Guide by providing operational information specific to the emulation of 6502 and compatible microprocessors. This document describes special set-up procedures, conditions, and limitations to be noted when emulating the 6502. It is assumed here that the reader has read the User's Manual and is already familiar with the details of the 6502. Ready access to the technical literature is a plus.

This supplement covers five general areas.

1) Installation

2) Initialization

3) Abbreviations                    (p.3)

4) Unique Features                  (p.7)

5) Electrical (DC) Characteristics  (p.11)


## *** INSTALLATION ***

System installation instructions will be found in the User's Manual.


## *** INITIALIZATION **

Type on the keyboard "RUN L01500" to load the Emulation Software into the ECL-3211. (The "RUN" command is discussed in the User's Guide.) Note that a user can use the Operating System's RENAME function to give the file a name the user would prefer. Additionally, a Command File can be created which can invoke L01500.

There are no special initialization instructions for the 6502.

## SYSTEM DISPLAY

These are seen on the top half of the display when using the Emulation Software.  All of these registers and flags can be loaded with user prefered values with the SET Command or ALTER mode as described in the User Manual or HELP file.

| *** | *** DESCRIPTION *** | |
|-----|---------------------|---|
| PC | Program Counter | 16 bits/4 hex digits |
| X | Index Register X | 8 bits/2 hex digits |
| S | Status Register | 8 bits/2 hex digits |
| | | |
| A | Accumulator | 8 bits/2 hex digits |
| Y | Index Register Y | 8 bits/2 hex digits |
| P | Stack Pointer | 8 bits/2 hex digits |
| | | |
| N | Negative Result (Sign) | Status bit 7 |
| V | Overflow | Status bit 6 |
| - | -- | -- |
| B | Break | Status bit 4 |
| D | Decimal Mode (BCD) | Status bit 3 |
| I | Interrupt enable/disable | Status bit 2 |
| Z | Zero | Status bit 1 |
| C | Carry | Status bit 0 |

TRACE DISPLAY              Note:   Low=0    High=1   Don't Care=X

"1" and "0" refer to ELECTRICAL,
NOT logical levels; though for
ECL-3211 functions logical and
electrical coincide.

These are seen when examining the Trace.

***    *** DESCRIPTION ***

IQ      Interrupt Request-L

NM      Non-Maskable Interrupt-L

RS      Reset-L

RY      Ready

RD      Read/Write-L

SO      Set Overflow

BA      Bus Available; generated by the ECL-3211, a "0" indicates that
                      the Data Bus is Tristate.

SY      Sync

BREAKPOINT DISPLAY                    Note: Low=0    High=1    Don't care=X

These are seen when examining or setting Breakpoints.

| | |
|---|---|
| E0-E7 | Pod External Input 0-7 |
| SW1 | Logical Switch 1 |
| | External Trigger 1 |
| SW2 | Logical Switch 2 |
| | External Trigger 2 |
| SW3 | Logical Switch 3 |
| SW4 | Logical Switch 4 |
| ROM | ROM access; "1" means trigger on a read from an address designated as ROM. |
| SYNC | SYNC; A "1" indicates the fetch of the first byte of an Op Code as a Breakpoint Condition. |
| CO1 | "1" selects Counter 1 expired |
| CO2 | "1" selects Counter 2 expired |
| ADDR | Program Counter; 16 bits |
| DATA | Data; 8 bits |
| IRQ | Interrupt Request-L |
| NMI | Non-Maskable Interrupt-L |
| RES | Reset-L |
| RDY | Ready |
| READ | Read/Write-L |
| SO | Set Overflow |
| BA | Bus Available; a "0" selects as a Breakpoint condition the Data Bus being Tristate. |
| PH=JMP | The 6502 Pod performs Phantom Jumps as a Breakpoint Action. |

LO1500

The file name for the Emulation Software is LO1500.  It is accessed through the Operating System hosted by the ECL-3211's CPU.

RESET

The ECL-3211's RESET command resets the 6502 Pod only, and does  not  reset the Target.  A Reset generated by the Target has effect during emulation only.

NO TARGET

Not having the 6502 Pod deployed in a target will not affect the  operation of  the  Emulator  in  any  way,  assuming  the user does not try to access resources in the Target.

MAX FREQ

The maximum frequency of operation is  2  Megahertz  for  both  Target  and ECL-3211 memory.

DEC INTERNAL

The 6502 Pod cannot operate using the bank of memory termed in  the  User's Guide as DEC Internal.

### PHANTOMS

The 6502 Pod performs Phantom Jumps.  Naturally, provision must be made to return to the original code path if that is desired by the user.

There are two important qualifications to their use:

1) The instruction immediately preceding the Phantom Jump must perform a Prefetch.  This means that a Phantom Jump cannot be inserted after a 2 or 3 byte intruction.

2) The address desired as a Breakpoint condition must be defined as an address value (ADDR) rather than a Program Counter value (PC).

To illustrate, consider the following examples of defining Breakpoint 4 as a Phantom Jump to address 5050:

| | ADDR | INSTR | DATA |
|---|---|---|---|
Given this code segment-- | **** | ***** | **** |
| | • | • | • |
| | • | • | • |
| | A500 | DEX | CA |
| | A501 | LDX   OFF | A2 |
| | A502 | | FF |
| | A503 | INX | E8 |
| | • | • | • |
| | • | • | • |

a) Typing "BR 4 PH=5050/ADDR=A501" will be successful. The Phantom Jump is being inserted by the Prefetch of a single byte instruction at a location defined as ADDR rather than PC (Program Counter).

b) Typing "BR 4 PH=5050/PC=A501" will fail. The address where the Phantom Jump is intended to be inserted is defined as PC, a Program Counter value.

c) Typing "BR 4 PH=5050/ADDR=A503" will fail. The preceding instruction, LDX, is a 2 byte instruction and does not Prefetch.

## TRACE DATA CAPTURE

If the Trace has been turned on, it takes a "snapshot" of conditions during each Machine Cycle when the conditions are valid. For example, the Data bus is sampled when it contains valid Data. Address information is sampled when there is a valid Address on the bus. Control signals are sampled at the same time as the Data unless they must be sampled at a different point in the Machine Cycle. (The Trace is turned on by defining a Breakpoint with conditions that will be met and an Action statement including Set Trace, as described in the User's Guide and HELP file.)

Instructions are disassembled in the Trace as they appeared on the Data bus when they were fetched.

Note that the External Inputs are not sampled simultaneously in a Machine Cycle. External Inputs 0-3 are sampled during the valid address time of a Machine Cycle and External Inputs 4-7 are sampled during valid data time.

## BREAKPOINT ACTION

Defined Breakpoint conditions are tested and resolved prior to the end of the Machine Cycle. Any Breakpoint Actions for a Breakpoint with conditions that have been met in a Machine Cycle commence at the completion of that Machine Cycle.

## CLOCK

The Emulator provides two sources of Clock signals for the 6502 Pod, the ECL-3211 and the Target circuit. Internal Clock has a guarantee of 100 Kilohertz resolution.

### --- External ---

External Clock is the mode in which the Target Circuit provides the clock. Since it is buffered in the Pod with TTL logic, the clock signal must be TTL driven or equivalent. Do not clock the Pod with a Crystal/RC Network circuit.

Type "FREQ EXT" to select this mode.

### --- Internal ---

Internal Clock is the mode in which the 6502 Pod is clocked by the Emulator. The clocking signal taken from the Target is not used. $\emptyset 1$ (pin 3) and $\emptyset 2$ (pin 39) are still active.

Type "FREQ xxxx" to select the Internal Clock mode. "xxxx" is the value of the frequency in units of Kilohertz. There is no need to specify "Internal" at any point.

### NOT EMULATING

When the ECL-3211 is not in Emulation mode, the signals from the 6502 Pod to the Target have the following status:

| | |
|---|---|
| A0-A15 | Active |
| D0-D7 | Tri-state |
| SYNC | Active |
| SO | Active |
| $\phi$2 | Active |
| $\phi$1 | Active |
| $\phi$0 | Active; ignored if Clock Internal selected |
| IRQ-L | High; ignored by Pod |
| NMI-L | High; ignored by Pod |
| RES-L | High; ignored by Pod |
| RDY | High; ignored by Pod |
| R/W-L | High; ignored by Pod |

*** ELECTRICAL (DC) CHARACTERISTICS ***

| Signal | Buffer Type | Output Drive | | Input Load | | Delay, additional | Termination, pull-up R |
|--------|-------------|--------------|-----------|------------|---------|-------------------|------------------------|
|        | 74xxx       | High mA      | Low mA    | High mA    | Low mA  | nSec typical      | ohms                   |
| A0-A15 | LS245       | -15.0        | 24.0      | --         | --      | 12                | --                     |
| D0-D7  | LS245       | -15.0        | 24.0      | 0.02       | 0.2     | 8                 | --                     |
| SYNC   | LS04        | -0.4         | 8.0       | --         | --      | 13                | --                     |
| R/W-L  | F04         | -1.0         | 2.0       | --         | --      | 7                 | --                     |
| ∅2     | LS04        | -0.4         | 8.0       | --         | --      | 13                | --                     |
| ∅1     | LS04        | -0.4         | 8.0       | --         | --      | 20                | --                     |
| SO     | LS04        | --           | --        | 0.02       | -0.4    | 20                | --                     |
| ∅0     | LS00        | --           | --        | 0.02       | -0.4    | 20                | --                     |
| IRQ-L  | LS32        | --           | --        | 0.02       | -0.4    | 14                | --                     |
| NMI-L  | LS32        | --           | --        | 0.02       | -0.4    | 14                | --                     |
| RES-L  | LS32        | --           | --        | 0.02       | -0.4    | 24                | --                     |
| RDY    | LS32        | --           | --        | 0.02       | -0.4    | 14                | --                     |
| HALT-L | LS32        | --           | --        | 0.02       | -0.4    | 14                | --                     |