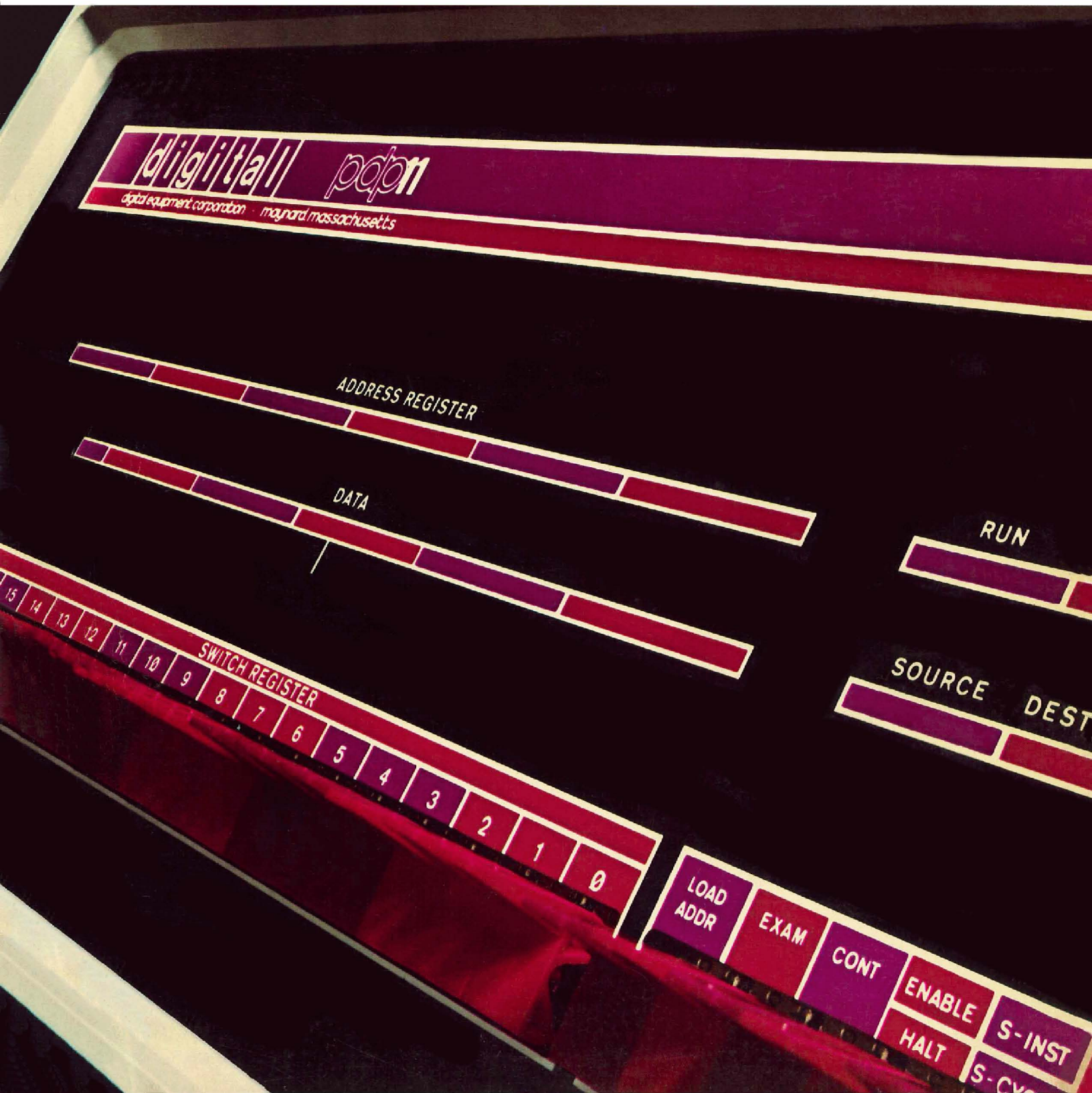
digital

DM11-BB
modem control
option manual



DM11-BB
modem control
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DEC-11-HDMBA-A-D

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FOREWORD

This manual provides the user with information and theory of operation necessary to understand and maintain the DM11-BB Modem Control Option. The level of discussion assumes that the user is familiar with basic digital computer theory and basic PDP-11 operation.

The DM11-BB is used in conjunction with a data multiplexer similar to the DM11-AA which is described in the *DM11 Asynchronous 16-Line Single-Speed Multiplexer Manual,* DEC-11-HDMA-D. The DM11-BB provides multiplexed modem control for 16 asynchronous modem interfaces. The unit provides the required control signals and levels to interface with Bell 103A/E/F/G/H, 202C/D, and 811B Modems or their equivalents. However, this manual does *not* describe the operation of these units. A detailed description of the operation of the modems is contained in their respective Bell System Communications Technical Reference Manual. Other modems and terminals interfaced by the DM11-BB have their respective documentation supplied with them.

This manual is supplied with each DM11-BB. Throughout this manual various engineering drawings are referenced. A set of engineering drawings, entitled *DM11-BB Modem Control Option Engineering Drawings,* is supplied with the DM11-BB. This set of drawings reflects the latest drawings for the DM11-BB at the time the equipment is shipped and is to be used in conjunction with this manual.

This manual is divided into 5 chapters:

a. General Description
b. Installation
c. Operational Programming
d. Detailed Description
e. Maintenance

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The DM11-BB Modem Control unit is used with the DM11-AA for modem control in dedicated and switched networks. The DM11-BB is used to interface the modem control signals between the modem and the processor. Data is handled by the DM11-AA asynchronous 16-line single-speed multiplexer. Also with the DM11-BB System, up to four DM11-DCs are used to line condition up to 16 modems. The DM11-BB is used when modem control is required by the DM11 System.

1.2 GENERAL DESCRIPTION

The DM11-BB is a multiplexed modem control for 16 asynchronous modem interfaces. The unit provides necessary control signals and levels to interface with Bell 103A/E/F/G/H, 202C/D, and 811B Modems or their equivalents. The interface levels are EIA/CCITT compatible for data set operation. The DM11-BB is ideally suited for applications where data is collected at remote locations and forwarded to a controlling processor. Typical applications include numerical control, data acquisition, physics, and biomedical and time-sharing systems.

1.3 FUNCTIONAL DESCRIPTION

The modem control signals for up to 16 modems are connected to the DM11-BB through the DM11-AA distribution panel, which provides level conversion for all DM11 lines interfaced (Figure 1-1). Line adaption is achieved at the distribution panel through the DM11-DC option. The DM11-DC unit is required for modem control interfacing. Each DM11-DC implements four EIA/CCITT lines including cabling for modem interfacing. Four DM11-DCs are necessary to handle the maximum 16 modems. Each of the modem types that can be interfaced may be mixed over the 16 lines available.

The DM11-BB scans the SEC RX, CLEAR TO SEND, CARRIER, and RING lines for each modem line sequenced by a line counter in the logic. When a transition is detected on a line, for the modem line designated by the line counter, an interrupt condition is generated. Providing interrupt enable and line enable are programmed, the interrupt requests bus control through the interrupt control logic. Likewise, through the address selector logic, the processor sends SEC TX, REQUEST TO SEND, and TERMINAL READY to the modem designated by the line counter. The line counter enables the particular transmit signal to be asserted on the line designated. The line counter is sequenced through the ring counter, which is clocked internally (scan logic) and enabled by the program-controlled Scan Enable and Step conditions.

The DM11-BB utilizes two basic types of modem control: transmit (to the modem) and receive (from the modem); The transmit control functions are: Terminal Ready, Request to Send, and Secondary Transmit. The receive control functions are: Clear to Send, Carrier, Secondary Receive, and Ring. The sequential usage of these control

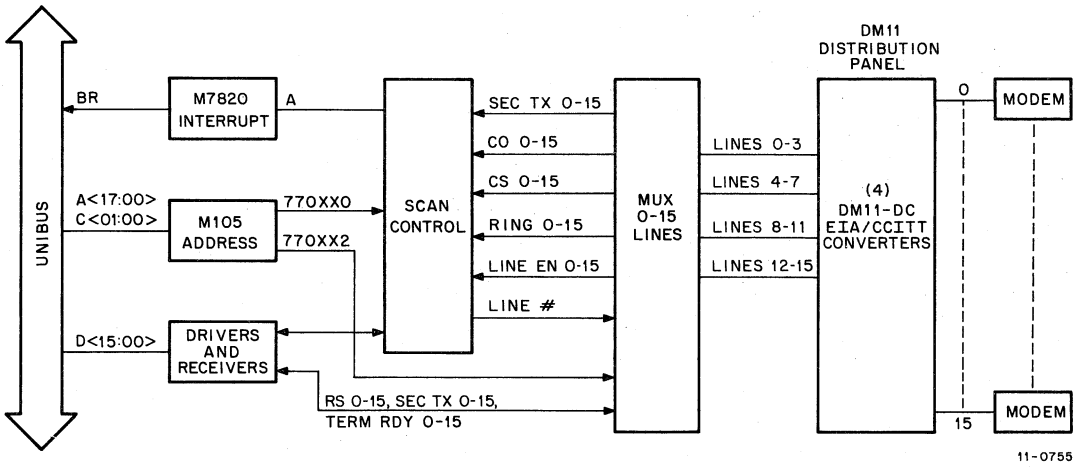


Figure 1-1 DM11-BB Block Diagram

functions (or leads) for the various modems, can be determined by using the modem timing diagrams shown in Appendix C. For example, a typical channel establishment sequence for the 103A Modem would be as follows:

a. 103A ORIGINATE MODE channel establishment (Figure C-1)

1. Setting the Data Terminal Ready lead to 1, followed by dialing via the DN11 Automatic Dialing Unit (DEC-11-HDNA-D) or by manual means initiates a call to the remote modem.

2. When the data link is established by the remote modem answering the call, CARRIER and CLEAR TO SEND make a simultaneous transition to the ON state.

3. If the DM11-BBs line enable for the line is set and Interrupt Enable and Scan Enable are set, the transitions (CARRIER and CLEAR TO SEND) are detected and an interrupt is generated to the Unibus.

4. At this time, the DM11-AA may transmit and/or receive data over the established data communications link.

b. 103A ANSWER MODE channel establishment (Figure C-1) (assume Line Enable, Scan Enable, and Interrupt Enable conditions are present).

1. A RING signal is forwarded, from the modem, to the DM11-BB. This OFF to ON transition is detected by the scanner and forwarded, as an Interrupt condition, to the Unibus.

2. The data link may then be established with the calling modem or line in question, by setting DATA TERMINAL READY.

3. When the simultaneous transitions of CARRIER and CLEAR TO SEND occur (OFF to ON), causing an interrupt condition to the Unibus, the communications data link is established.

4. The DM11-AA may now transmit and/or receive data with the modem.

1.4 SPECIFICATIONS

The DM11-BB specifications are grouped into four categories:

a. physical description
b. environmental limits
c. performance specifications
d. interface specifications

1.4.1 Physical Description

The DM11-BB occupies the remainder of the two system unit DM11-AA module slots (1/2 system units). The DM11-BB, a scan-operated modem control for 16 asynchronous modems, uses the following parts:

Quantity	Part	Description
1	M7246	Scan Module
2	M7247	Data MUX (8 Lines)
1	M105	Address Selector
1	M7820	Interrupt Control
4	BC08R-12	Mylar Cable (4 Lines)
4	M971	Cable Module (BC08R)
1	H861	Test Connector (16 Lines)
1	7408925	DC11 Test Connector (1 Line)

These parts are used according to the system drawing of Figure 1-2. The modem level converters and the modem cabling are not part of the DM11-BB. They are included in the DM11-DC option discussed in the DM11 manual. In relation to the DM11-BB, the DM11-DC provides EIA/CCITT conversion and cabling for four modems each. Thus, four DM11-DCs are utilized for 16 modems or lines. Figure 1-3 shows the interfacing of the DM11-BB to the modems' lines through the DM11-DCs.

1.4.2 Environmental Limits and Performance and Interface Specifications

The environmental limits, performance specifications, and interface specifications for the DM11-BB are listed in Table 1-1.

Table 1-1
DM11-BB Specifications

Environmental Limits	
Power requirements	At +5V, 2.4A
Temperature	10°C to 50°C
Humidity (relative)	Up to 90% (non-condensing)
Performance Specifications	
Interrupts	CARRIER, SEC RX, CLEAR TO SEND, and RING transitions cause interrupts.
Modem status maximum rate change	10,000 Hz for both receive and transmit circuits.
Scan rate	The DM11-BB tests line conditions for interrupts at a rate of 1 mHz ± 10% or one line per 1.2 μs, approximately.
Scan control	Programmable to allow scan to run free (SCAN EN) or to sequentially step through Scan line by line (STEP).
LINE counter	Line numbers (LINE #) may be accessed by program, sequentially or randomly, without concern for internal synchronization.

(continued on next page)

Table 1-1 (Cont)
DM11-BB Specifications

Performance Specifications (Cont)	
Scan limitations	The Scan cannot be halted and the line number changed with one instruction due to the Read/Write cycles of the Scan's memory. Also, the program must wait for CLR SCAN (programmable) to ripple through the DM11-BB memory logic.
Interrupt bus request	Hard-wired to level 4 (BR4).
Interface Specifications	
Unibus	The DM11-BB presents one unit load to the bus and meets all Unibus electrical specifications.
Modem interface	The DM11-BB provides modem control leads compatible to modem types 103A, 103F, 103E (G and H), 202C/D, and 811B. (Types may be mixed over the 16 lines available.) These lines are EIA RS-232-C and CCITT compatible.
Condensed EIA RS-232-C Electrical Specifications	
Driver output logic levels with 3K to 7K load	$15V > _{oh} > 5V$ $-5V > _{ol} > -15V$
Driver output voltage with open circuit	$/V_o/ < 25V$
Driver output impedance with power off	$20 >$ 300 ohms
Output short circuit current	$/I_o/ <$ 0.5A
Driver slew rate	$\frac{dv}{dt} < 30\ V\mu s$
Receiver input impedance	$7k\Omega > R_{in} > 3k\Omega$
Receiver output voltage	±15V compatible with driver
Receiver output with open circuit input	Mark
Receiver output with +3V input	Space
Receiver output with –3V input	Mark
+15 +5	LOGIC "0" = SPACE – CONTROL ON
	Noise margin
+3 0 -3	Transition region
	Noise margin
-5 -15	LOGIC "1" = MARK = CONTROL OFF

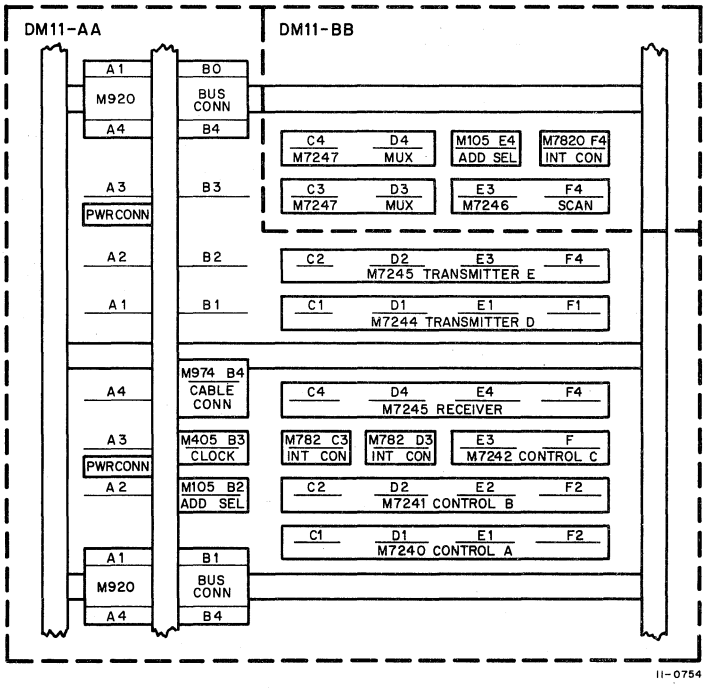


Figure 1-2 DM11 System Unit Layout with DM11-BB Option

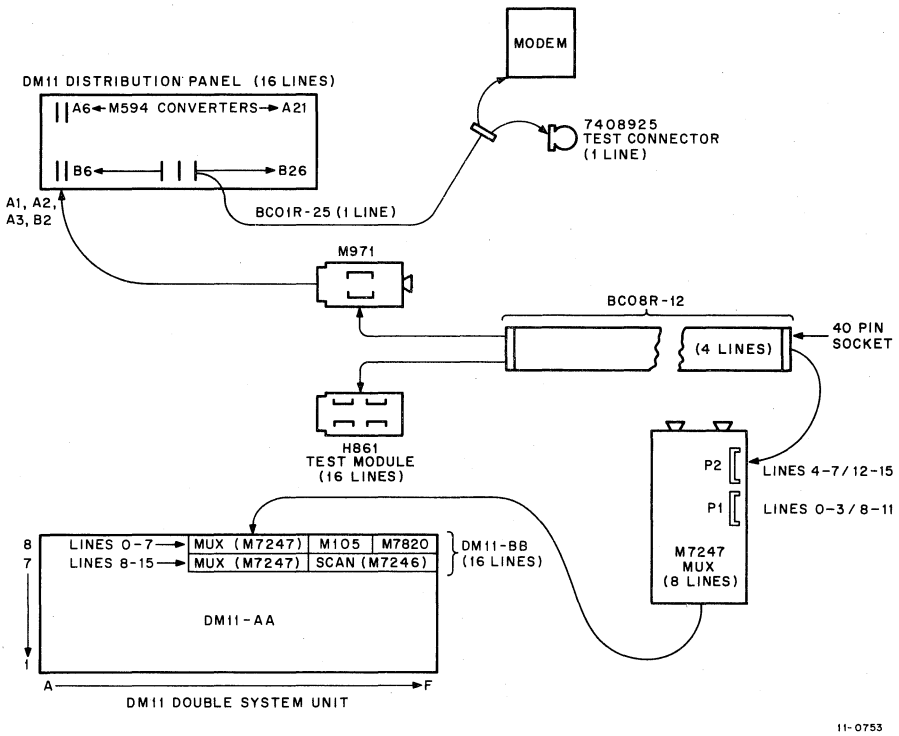


Figure 1-3 DM11-BB Hardware Configuration

CHAPTER 2
INSTALLATION

2.1 INSTALLATION OPTIONS

The DM11-BB options consist of communication and customer options.

The communication options regard the interface to the modems from the DM11-BB. The DM11-DC unit provides connections for the DM11-BB (M971), modem cables (BC01R-25) and EIA converters (M594) to implement four lines. Optional to this is the utilization of a Null Modem Jumper Box (synchronous/asynchronous), H312A. The null modem has two EIA type 25-pin sockets.

The customer options consist of inhibiting initialization from the bus and inhibiting interrupts. INITIALIZE from the bus is inhibited from clearing the DM11-BB by disconnecting the single back panel wire in the system unit from FD8D2 to ground. Interrupts may be inhibited for CARRIER, RING, SEC RX, or CLEAR TO SEND for all lines by removing the back panel wire in the system unit that connects the MUX (M7247) to the Scan Module (M7246). These connections are listed in Table 2-1.

Table 2-1
Interrupt Inhibit Connections

Status	Remove
CARRIER	E08A1 to D08B1
RING	E08C1 to D08F2
SEC RX	E08B1 to D08C1
CLEAR TO SEND	E0801 to D08C1

These functions may also be inhibited, for single lines, at the DM11-AA distribution panel.

2.2 INSTALLATION CABLING AND TERMINATIONS

The cabling and terminations for the DM11-BB provide the interface to the DM11-AA distribution panel. Figure 2-1 shows the block diagram for the DM11-BB cabling, including the distribution cabling and terminations to the modems. Table 2-2 lists the modem control signals for all lines per DM11-DC and the pin connections for each stage from the M7247 to the modem cable, including the DM11-AA distribution panel. Table 2-3 lists the modem signals with respect to their EIA RS-232-C circuit designations, pin numbers, and CCITT equivalent interface. Table 2-4 lists the signal designations and pin numbers for each of the modems.

As an example of how Table 2-2 and Figure 2-1 can be used to trace the electrical path of a control line, the following procedure traces the electrical path for the CLEAR TO SEND (CS) line number 0 from the M7247 Module to the modem connector.

a. In the "Line Number" column of Table 2-2, locate the group of line numbers that contains line 0. To the right of this group, locate CS in the "Signal Name" column. All of the electrical connections for this control line can be found on this line of the table by reading across to the right.

b. In the "M7247 P1/P2" column pin S is designated as the connection pin in the 40-pin connector for the M7247 Module. Checking Figure 2-1 shows that P1 of the M7247 Module is used for lines 0 through 3. Therefore, it has been determined that the control line leaves the M7247 Module on pin S of P1.

c. In the next column to the right entitled "M971 40-Pin Conn.", pin DD is designated as the BC08R-12 cable and module connection.

NOTE

This same connection is used for the H861 16-Line Test Connector. To trace out the circuits for the H861, the H861 circuit schematic and Table 2-2 can be used.

d. In the column of Table 2-2 entitled "Input (M971 Pins) A1, A2, A3, B2", pin H1 is listed in the input pin for the DM11-AA distribution panel. Figure 2-1 shows that line 0 comes into the DM11-AA distribution panel in location A1, so that pin H1 of location A1 is where the control line enters the distribution panel.

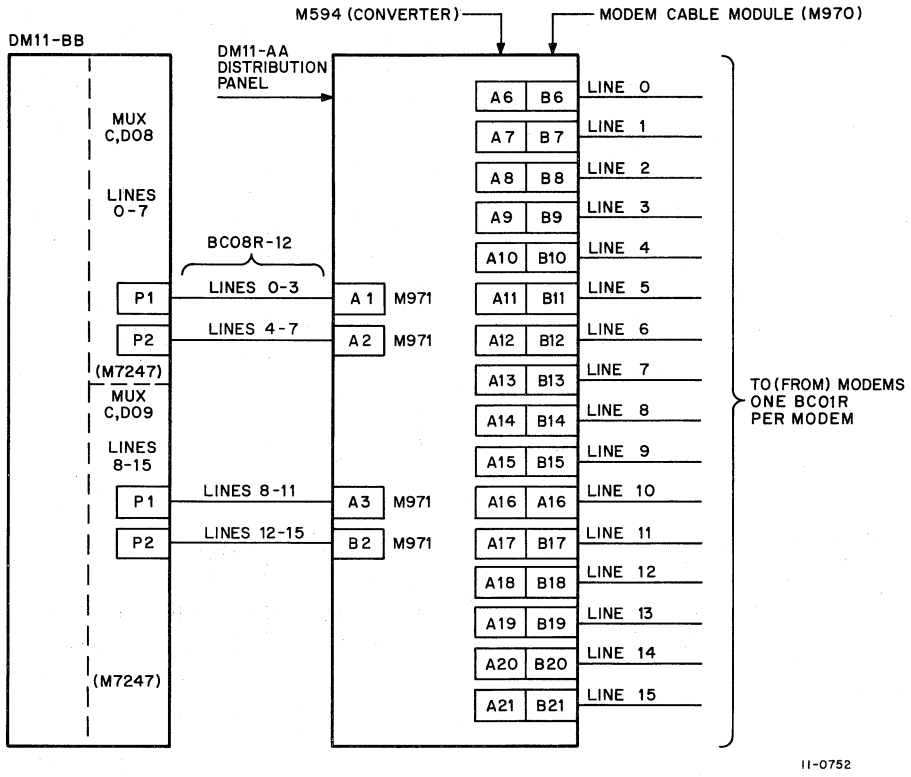


Figure 2-1 DM11-BB Cable/Converter Locator Diagram

e. In the column entitled "Converter (M594) A6–A21" pin F2 is listed as the TTL input/output to the M594 Converter. Figure 2-1 shows that line 0 comes out of A6–B6, so that it is pin F2 of the M594 in location A6.

f. Pin M2 is listed as the EIA input/output to the M594 Converter in location A6.

g. In the column entitled "Output (M970 Pins) B6–B21" pin K2 is listed as the cable connector pin at location B6. Connector B6 is the receptacle for the BC01R modem cable.

h. In the column entitled "25 Pin Conn.", pin 5 is designated as the electrical connection at the end of the modem cable for the CS line number 0.

Table 2-2
DM11-BB/Modem Wire Locator

Line Number	Signal Name	M7247 P1/P2	Distribution Panel				Output (M970 Pins) B6 – B21	25 Pin Conn.
			M971 40 Pin Conn.	Input (M971 Pins) A1,A2,A3,B2	Converter (M594) A6 – A21 TTL	Converter (M594) A6 – A21 EIA		
	Ground	A,C	VV,TT	A1	–	–	–	1,7
	–	E	RR	B1	–	–	–	–
	Ground	H	NN	C1	–	–	–	1,7
	Ring	K	LL	D1	C1	K2	M2	22
	TERM RDY	M	JJ	E1	P2	R2	R2	20
0,4,8,12	RS (Busy)	P	FF	F1	S2	T2	L2 (S1)	4,(25)
	CS	S	DD	H1	F2	M2	K2	5
	CO	U	BB	J1	B1	H2	P2	8
	SEC TX	W	Z	K1	U2	U1	E1	11
	SEC RX	Y	X	L1	E1	L2	F1 (J2)	12 (17)
	(Restraint)							
	RING	AA	V	M1	C1	K2	M2	22
	TERM RDY	CC	T	N1	P2	R2	R2	20
	RS (Busy)	EE	R	P1	S2	T2	L2 (S1)	4,(25)
	CS	HH	N	R1	F2	M2	K2	5
	CO	KK	L	S1	B1	H2	P2	8
	Ground	MM,PP	J,F	T1	–	–	–	1,7
1,5,9,13	SEC TX	UU	B	U1	U2	U1	E1	11
	SEC RX	SS	D	V1	E1	L2	F1 (J2)	12 (17)
	(Restraint)							
	–	B,D	UU,SS	A2	–	–	–	–
	–	F	PP	B2	–	–	–	–
	Ground	J	MM	C2	–	–	–	1,7
	RING	L	KK	D2	C1	K2	M2	22
	TERM RDY	N	HH	E2	P2	R2	R2	20
	RS (Busy)	R	EE	F2	S2	T2	L2 (S1)	4 (25)
2,6,10,14	CS	T	CC	H2	F2	M2	K2	5
	CO	V	AA	J2	B1	H2	P2	8
	SEC TX	X	Y	K2	U2	U1	E1	11
	SEC RX	Z	W	L2	E1	L2	F1 (J2)	12 (17)
	(Restraint)							
	RING	BB	U	M2	C1	K2	M2	22
	TERM RDY	DD	S	N2	P2	R2	R2	20
	RS (Busy)	FF	P	P2	S2	T2	L2 (S1)	4 (25)
3,7,11,15	CS	JJ	M	R2	F2	M2	K2	5
	CO	LL	K	S2	B1	H2	P2	8
	Ground	NN,RR	E,H	T2	–	–	–	1,7
	SEC TX	TT	C	U2	U2	U1	E1	11
	SEC RX	VV	A	V2	E1	L2	F1 (J2)	12 (17)
	(Restraint)							

Table 2-3
RS-232-C Interface Connections

RS-232-C	CCITT	Description	Pin
CA	105	Request to Send	4
CB	106	Clear to Send	5
CF	109	Received Line Signal Detector	8
SBA*	118	Secondary Transmitted Data	14 (11*)
SSB*	119	Secondary Received Data	16 (12*)
—	—	Restraint	17
CD	108.2	Data Terminal Ready	20
CE	125	Ring Indicator	22
—	—	Force Busy	25

*SBA and SSB are shipped wired for a Bell 202 modem. EIA pinning can be selected at the M970 cable module.

Table 2-4
Modem Interface Connections

Pin	Function	103A	103E/G/H	103F	202C/D	811B
1	Protective Ground	X	X	X	X	X
2	Transmitted Data	X	X	X	X	X
3	Received Data	X	X	X	X	X
4	Request To Send			X	X	
5	Clear To Send	X	X	X	X	X
6	Data Set Ready	X	X	X	X	X
7	Signal Ground	X	X	X	X	X
8	Carrier Detector	X	X	X	X	X
9						
10						
11	Originate Mode			X		
11	Secondary Transmitted Data				X	
12	Local Mode*			X		
12	Secondary Received Data				X	
13						
14						
15						
16						
17	Restraint					X
18						
19						
20	Data Terminal Ready	X	X		X	X
21						
22	Ringing Indicator	X	X		X	X
23						
24	EOT*					X
25	Busy		X			X

*The DM11-BB does not provide for these lines.

2.3 POWER CONNECTIONS

Power connections to the DM11-BB are provided by the PDP-11 System (Figure 1-2). When power is applied to the PDP-11 System, the DM11-BB, as well as the DM11-AA, receives power. These power connections are discussed in detail in the *PDP-11 Unibus Interface Manual* (DEC-11-HIAB-D).

2.4 INSTALLATION TESTING

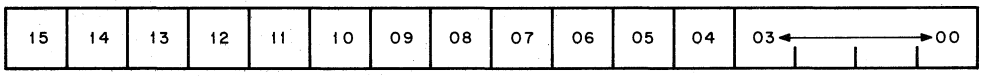
Installation testing is performed to ensure that the DM11-BB has been installed properly and is operational. This is accomplished by running the DM11-BB diagnostic, MainDEC-11-D9KA, supplied with the DM11-BB unit.

CHAPTER 3
OPERATIONAL PROGRAMMING

3.1 PROGRAMMABLE DEVICE REGISTERS

The two programmable DM11-BB device registers and their specific bit assignments are listed in the following paragraphs.

3.1.1 Control Status Register (CSR) (Address: 770XX0)



Bit	Status	Description
03:00	LINE #	The LINE # bits are the binary addresses for the DM11-BB's 16 lines (0–15) as follows:

Bit 3 2 1 0	Line #
0 0 0 0	0
0 0 0 1	1
⋮	⋮
1 1 1 1	15

If the Scan is cleared by INITIALIZE or CLR SCAN, the Line # Register will settle in 16 μs ±10%. When settled, the Line # Register will be set to Line # 0 (0000).

NOTE

When the Scan is enabled (or STEP) the next line to be tested will always be Line # +1. These bits are Read/Write and are cleared by INITIALIZE and by CLR SCAN.

04	BUSY	BUSY provides a program indicator that is set to 1 when the Scan is cycling. This bit is particularly useful to determine when a CLR SCAN (bit 11) has completed the task of cycling 0s into the Scanner's memory elements.

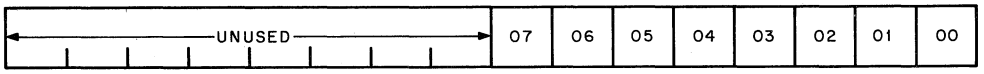
In addition, this bit *must* be tested for 0 if SCAN ENABLE was turned off preparatory to changing the Line #.

In Interrupt Mode, this procedure guarantees that detected transitions are serviced before the Line # is changed. (If functioning with interrupts OFF, then DONE should be tested after BUSY is found to be 0.)

Bit	Status	Description
05	SCAN EN	The SCAN ENABLE flip-flop allows the scan to "free run" – testing all lines sequentially if the DONE flip-flop is cleared. When the SCAN EN flip-flop is set to 1 and DONE is 0, a ring counter is allowed to cycle in the following order (from Rest): *a.* Increment line counter. *b.* Store contents of memory (Line # Address) in the HOLD flip-flop. *c.* Write current modem status into memory. *d.* Compare HOLD and contents of memory for Interrupt conditions. The ring counter continues to cycle (*a* to *d*) if DONE remains 0 and SCAN EN is set. If the SCAN EN flip-flop is negated while the ring counter is cycling (i.e., DONE not set) the ring counter will come to rest in 1.2 μs ± 10% (MAX). The line # Register must not be changed until BUSY (bit 04) is found to be 0. This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
06	INTR EN	If set to 1, Interrupt Enable allows DONE to cause an interrupt on priority four (4). This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
07	DONE	The DONE flag, when set to 1, indicates that the hardware Scan has detected a transition on CARRIER, SEC RX, CS, or the RING Modem Status leads. Additionally, DONE freezes the Scan which makes available to the programmer: *a.* The Line # that caused the interrupt *b.* The state of the flags (4 bits) *c.* Modem status (8 bits) This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
08	STEP	STEP, when set to 1, causes the Scan to increment the Line # and test that line for interrupts causing transitions. STEP can be used in place of SCAN EN, but care should be exercised that the Scan rate is great enough (milliseconds) so that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires 1.2 μs ± 10% to execute. This bit is Write 1s only.
09	MAINT MODE	When the MAINT MODE flip-flop is set to 1, it conditions the Scan Input (RING, CLEAR TO SEND, CARRIER, and SEC RX) to a 1 or ON state. Utilizing STEP or SCAN EN with MAINT MODE exercises 100 percent of the scan logic (not the data multiplexers). This includes the interrupt circuits (M7820) and the address selector (M105). This mode provides a diagnostic feature, as well as an on-line test facility for the DM11-BB's interaction with the Unibus. This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
10	CLEAR MUX	CLEAR MUX clears the REQUEST TO SEND, TERMINAL READY, SEC TX, and LINE EN flip-flops for all lines, when this bit is set to 1. This bit is Write 1s only.

Bit	Status	Description
11	CLR SCAN	CLEAR SCAN clears all active functions (Line #, SCAN EN, etc.) and the memory logic, when this bit is set to 1. The memory logic requires 18.8 μs ±10% to cycle a CLEAR through the memory locations. This function is especially useful if the programmer requires knowledge of the ON states of CARRIER, CLEAR TO SEND, RING and SEC TX. When the Scan is enabled (or STEP) following a CLR SCAN, an interrupt will occur for all ON states as they will appear (to the logic) as OFF to ON transitions.
12	SEC RX	The SECONDARY RECEIVE flag is 1 if an ON to OFF or an OFF to ON transition has occurred on this modem lead. This bit is redefined as RESTRAINT when the 811B Modem is used. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED or CLR SCAN.
13	CS	The CLEAR TO SEND flag is 1 if an ON to OFF or OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED or CLR SCAN.
14	CO	The CARRIER flag is 1 if an ON to OFF or OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED and CLR SCAN.
15	RING	The RING flag is 1 if an OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED and CLR SCAN.

3.1.2 Line Status Register (LSR) (Address: 770XX2)



11-0750

Bit	Status	Description
00	LINE EN	The LINE ENABLE flip-flop, when asserted, enables RING, CO, CS, and SEC RX to be sampled (line status) by the program, and to be tested for transitions. This bit is Read/Write and cleared by INITIALIZE and CLEAR MUX.

Bit	Status	Description
01	TERM RDY	Controls switching of the data communications equipment to the communication channel (via modem). Auto-Dial and Manual Call origination: Maintains the established call. Auto-Answer: Allows "handshaking" in response to a RING signal. This bit is Read/Write and is cleared by INITIALIZE and CLEAR MUX.
02	RS	When REQUEST TO SEND is set to 1, it conditions the modem for transmit if the communications channel has been established (switched network). When the DM11-BB is used to interface with 103E (or equivalent) Modems, this lead is redefined as FORCE BUSY. (RS = 1 = FORCE BUSY "ON"). This bit is Read/Write and is cleared by INITIALIZE and CLEAR MUX.
03	SEC TX	The SECONDARY TRANSMIT (202) flip-flop, when 1, presents a MARK to the modem's secondary transmit lead. This bit is Read/Write and is cleared by INITIALIZE or CLEAR MUX.
04	SEC RX	The state of the modem's Secondary Receive lead, when 1, is a MARK state. The SEC RX bit is inhibited when the LINE EN flip-flop is 0. When the DM11-BB is used to interface with the 811B Modem, this lead is redefined as RESTRAINT. This bit is Read Only.
05	CS	This bit reflects the current state of the modem CLEAR TO SEND lead. An ON indicates that the modem is ready to transmit data. This lead is most often the result of the REQUEST TO SEND lead. The CS bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.
06	CO	This bit reflects the current state of the modem carrier control lead. An OFF indicates that no signal is unsuitable for demodulation. The CO bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.
07	RING	This bit reflects the current state of the modem's ring lead. The RING bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

NOTE
The Line Status Register bits 07:04 are inhibited when LINE EN is 0.

3.2 SYSTEM ADDRESSES

Addresses are assigned for sixteen (16) DM11-BBs per system and are assigned upward as follows:

1st DM11-BB	Address	770500 770502
2nd DM11-BB	Address	770510 770512
.		.
.		.
.		.
16th DM11-BB	Address	770670 770672

3.3 INTERRUPT VECTORS

Each DM11-BB requires one interrupt vector. The vector addresses are assigned upward from 300 to 777. The DM11-BB falls in behind the DN11 in contiguous assignments from 300. The sequential list leading to the DM11-BB is:

DC11
KL11
DP11
DM11-AA
DN11
DM11-BB

3.4 TIMING CONSIDERATIONS

The DM11-BB timing considerations consist of scan control and CLR SCAN operations. Scan control through the CSR allows the scan to either run free (SCAN EN) or to be sequentially stepped through the line counter line by line (STEP bit of CSR). The Read/Write cycles of the DM11-BB scan logic (Paragraph 4.4) force the program to wait, after issuing CLR SCAN, until it has cycled through the memories. Also, the scan's Read/Write cycles prevent halting the scan and changing the line number with one machine cycle.

CHAPTER 4
DETAILED DESCRIPTION

4.1 INTRODUCTION

The DM11-BB consists of four basic logic units. They are the Address Selector Logic, Interrupt Control Logic, Scan Logic, and the Data Multiplexer Logic (MUX). These units are discussed in detail in the following paragraphs. Refer to Figure 4-1 for the DM11 functional scan block diagram. Also, the maintenance mode of operation is discussed.

4.2 ADDRESS SELECTOR LOGIC

The address selector logic (M105) is jumper-prepared to recognize the two register addresses assigned to the DM11-BB. When the bus designates either of these addresses, they are recognized by the M105 and, according to the bus operation (DATO, DATI, DATIP, or DATOB), the M105 generates SELECT and IN, OUT signals. DATI or DATIP bus operations designate the IN selection signal for gating to the bus; DATO or DATOB designate the OUT selection signal for gating from the bus. SELECT 0 and OUT LOW load the CSR, while SELECT 0 and IN gate the CSR to the bus. SELECT 2 and IN gate the MUX TERM RDY, MUX LINE EN, MUX RQ TO SEND, and MUX SEC TX to the bus along with MUX SEC RX, MUX CLEAR TO SEND, MUX CARRIER, and MUX RING. SELECT 2 and OUT LOW enable the generation of the clock for MUX transmitting to the modem lines. For a detailed description of the M105 Module refer to the *PDP-11 Unibus Interface Manual.*

4.3 INTERRUPT CONTROL LOGIC

The M7820 Interrupt Control Module enables the DM11-BB unit to gain control of the bus (become bus master) and perform an interrupt operation. This is accomplished through a bus request (BR) at BR level 4. Detection of a transition in CARRIER, SEC RX, CLEAR TO SEND, or RING signal lines from any modem, designated by the modem line counter, generates an interrupt request through the M7280, as long as INTR EN has been set by the program. Any of these conditions causes the interrupt control to generate the BR to the processor requesting bus control. For detailed description of the M7820 Module refer to the *PDP-11 Unibus Interface Manual.*

4.4 SCAN LOGIC

The scan logic (engineering drawing D-CS-M7246-0-1, sheets 2 and 3) includes the control logic for the DM11-BB and the Unibus receivers and drivers. The Unibus receivers and drivers are standard for the PDP-11 and meet all requirements for connection to the Unibus. The control logic performs the programmable functional conditions of the CSR. The principal logic units of the scan logic are the ring counter, line counter, scan memory logic, and the interrupt logic.

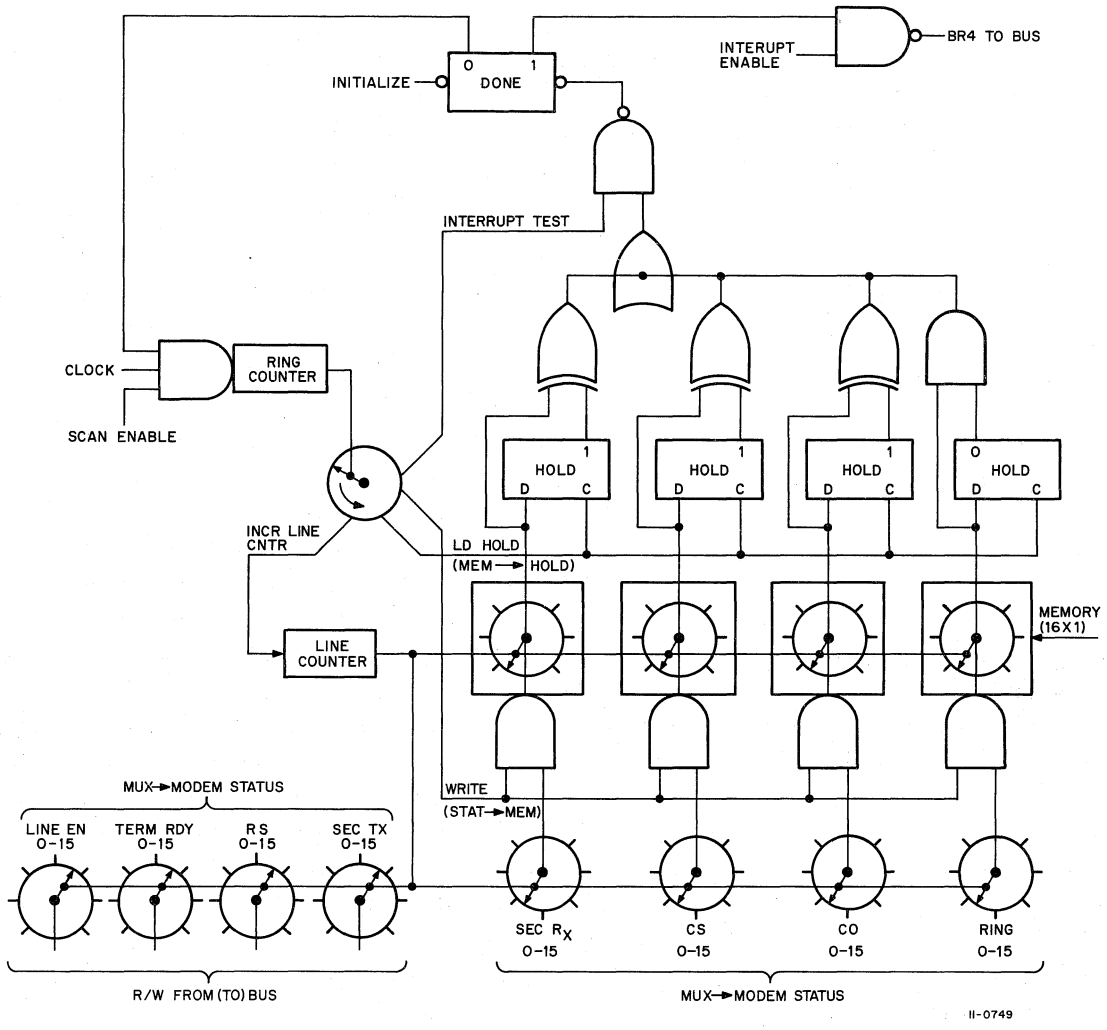


Figure 4-1 Scan Functional Block Diagram

Initiation of the DM11-BB is achieved through the program-controlled device registers. Initialization is achieved through the CLR SCAN signal from the program and BUS INITIALIZE. These signals combine to clear the logic flip-flops and counters, while setting CLEAR CYCLE. CLEAR CYCLE puts a low to the direct clear inputs of the HOLD flip-flops (SEC RX HOLD, CS HOLD, CO HOLD, and RING HOLD) and inhibits inputs from the MUX to scan memory while the memory is being cycled through all lines. The CLEAR CYCLE flip-flop is then cleared when all scan memory locations have been written with 0s. The DM11-BB is now initiated by setting the SCAN EN bit. SCAN EN with DONE clear (no interrupt conditions present) inputs the 8271 Ring Counter. The CLOCK cycles the ring counter through four states; that is, the ring counter increments the LINE CNTR (LINE INCR), loads the HOLD flip-flops with the last known contents of memory (at LINE #) (LD HOLD), transfers the current status of the LINE # to the memory section (IN WRITE), and tests the contents of the HOLD flip-flops and the memory section (at LINE #) for interrupt-causing conditions (INTR TEST). This four-state ring counter sequence is repeated for each line (LINE #), sequentially, as long as the SCAN EN condition with DONE clear is present to the ring counter. The programmable flip-flop STEP can also enable the ring counter, but for only one count; STEP enables one clock of the ring counter to increment the LINE CNTR (LINE INCR) which feeds back to clear STEP. The ring counter sequences the other three steps (LD HOLD, IN WRITE, and INTR TEST) before coming to rest.

The LINE CNTR is programmable for loading with a desired line count from the bus (BUS DATA 00 through BUS DATA 03). The LINE CNTR outputs provide line selection for testing, sensing, and modifying the line status on a per line basis. The LINE CNTR output also inputs the memory section at the 4007 X- and Y-decoders. The 4007s select the memory locations in the 7481s for each line's SEC RX, CS, CO, and RING status. When the ring counter sequences the WRITE IN signal, the status of each of the RING, CARRIER, SEC RX, and CLEAR TO SEND lines for the particular modem (LINE #) is loaded into the memory location of the 7481s designated by the LINE CNTR X- and Y-decoder inputs.

During INITIALIZE, when the X- and Y-decoders are loaded from LINE 0000, the decoder's LSB (least significant bit) output combines with the ring counter WRITE IN sequence signal to clear the CLEAR CYCLE flip-flop. The HOLD flip-flops can now be input from the 7481 memories. For each line selected through the X- and Y-decoders, the states of the MUX SEC RX, MUX CLEAR TO SEND, MUX CARRIER, and MUX RING are loaded into the respective memory locations, by the WRITE IN signal from the ring counter. When WRITE IN is unasserted these memories present their state for the respective LINE # to HOLD flip-flops. Each time the ring counter sequences LD HOLD for each line, the HOLD flip-flops are loaded with the contents of the respective memory locations. The memory contents are the last known state or status designated by the LINE CNTR. When the ring counter sequences WRITE IN, the new status is loaded into memory for the particular line. This new status (SEC RX, CLEAR TO SEND, CARRIER, and RING) is then compared with the contents of the respective HOLD flip-flops in the Exclusive OR gates for SEC RX, CLEAR TO SEND, and CARRIER and the AND gate for RING. This gating operation detects transitions in the line status each time the LINE # is sequenced. A (low to high) transition of any of the conditions for a particular line generates an interrupt condition. This is tested when the ring counter sequences INTR TEST. The presence of an interrupt condition at INTR TEST with the MUX LINE EN present (see MUX description), sets DONE. DONE set, with INTR EN set by the program, generates an interrupt condition to the interrupt control logic, which generates a bus request to the processor. An interrupt will not occur if the program has modified the LINE CNTR and the ring counter has not cycled. For example, if the Scan last tested LINE #5, followed by the program's modification of the LINE CNTR to LINE #8, for example, the HOLD flip-flops now contain the line status of LINE #5, while the memory is at LINE #8 and inputting the transition gates for LINE #8. Therefore, any transitions detected are a function of LINE #5 and LINE #8 and are not valid interrupt conditions.

4.5 MODEM CONTROL (MUX) LOGIC

The modem control (MUX) logic contains the status selector logic for each line interfaced (engineering drawing D-CS-7247-0-1, sheets 2 and 3). The status to the modem is Read/Write and the status from the modem is Read Only. Read/Write status control signals are LINE EN, TERM RDY, RQ TO SEND, and SEC TX. The Read Only status control signals are RING, CARRIER, CLEAR TO SEND, and SEC RX. For any Read Only status to be read the respective LINE EN must be on. If this is not the case, RING, CARRIER, CLEAR TO SEND, and SEC RX are blinded to the line status from the scan control logic.

The MUX Read/Write is clocked by the LINE DCDR. The LINE DCDR is input with the LINE CNTR output and WRITE SEL. WRITE SEL is initiated by the selection logic through OUT LOW and SELECT 2, and thus program-controlled. Also, WRITE SEL reflects the LINE CTR GROUP 0–7 or GROUP 8–15 signals that enable the respective LINE DCDR of each MUX module. The LINE DCDR provides a CLOCK signal for each line's status signal selector. Each CLOCK for each line inputs a respective 8271 for clocking in LINE EN and either SEC TX, TERM RDY, or RQ TO SEND to be transmitted on the respective modem line. The data bits for LINE EN, SEC TX, TERM RDY, and RQ TO SEND input the 8271s from the bus receivers (D00 to D03). CLOCK enables the 8271s to output to the respective modem lines.

Three of the LINE CNTR outputs provide enabling signals for the 74151 selectors in the MUX. The states of these inputs according to the LINE # select the proper line to be enabled at the selectors from the respective modem lines. For the signals coming from the modems, the RING SELECTOR, CARRIER SELECTOR, CLEAR TO SEND SELECTOR, and SEC RX SELECTOR are enabled at the current LINE # by INTR STATUS. INTR STATUS is asserted to enable the receiver selectors when CLEAR CYCLE is not set and MUX LINE EN is present. The receiver selectors output MUX RING, MUX CARRIER, MUX CLEAR TO SEND, and MUX SEC RX to the memory section of the scan logic to test for interrupts. MUX LINE EN is generated in the transmit selector when the programmable LINE EN is set for the respective LINE #, enabling the selector from the LINE CNTR. These transmit selectors are enabled by R/W STATUS, which asserts to the respective MUX module for either Lines 0–7 (GROUP 0–7, from LINE CNTR) or Lines 8–15 (GROUP 8–15 from the LINE CNTR). The control signal status conditions are available to the program, with the receive conditions handled by the scan logic for interrupt conditions, and the transmit conditions for each line sent to the respective modems.

4.6 MAINTENANCE MODE

The maintenance mode of operation in the DM11-BB is achieved by the programmed setting of the MAINT MODE flip-flop of the CSR. Setting MAINT MODE forces MUX SEC RX, MUX CLEAR TO SEND, MUX CARRIER, and MUX RING low, thus asserting a transition for the line designated by the line counter. These conditions can then be checked by the program through the CSR and allowed to cause interrupt conditions.

CHAPTER 5
MAINTENANCE

5.1 INTRODUCTION

DM11-BB maintenance consists of running two diagnostic software tests: the ON LINE and OFF LINE tests. The ON LINE diagnostic tests 100 percent of the scan logic, interrupts, and the Unibus interface. Additionally, 70 percent of the data multiplexer (MUX, M7247) may be tested. The OFF LINE test uses a test connector to test 100 percent of the DM11-BB, up to the point of demarcation at the modem interface. This chapter provides instructions for running the tests, as well as the hardware configurations for the respective tests.

5.2 TESTING CONFIGURATIONS

The DM11-BB test/diagnostic procedures provide for four test configurations. Two are for the OFF LINE and two are for the ON LINE tests as listed:

- OFF LINE (used for production test and acceptance)
  - *a.* DM11-BB terminated with H861 (Figure 5-1).
  - *b.* DM11-BB terminated by test connector (Figure 5-2).
- ON LINE (limited data flow)
  - *a.* Modem loop back configuration (used for production test and acceptance procedures during first six months of production shipments) (Figure 5-3).
  - *b.* Remote or local terminal via modem (Figure 5-4).

5.2.1 OFF LINE

The OFF LINE test/diagnostic procedures exercise 100 percent of the DM11-BB/DM11-DC hardware, up to the point of demarcation at the modem interface. The OFF LINE test requires two configurations (Figures 5-1 and 5-2) to achieve 100 percent testing.

Hardware requirements are as follows:

1 PDP-11 with > 4K core
1 DM11-AA System Unit (modules not required)
1 DM11-BB Module Set
1 H861 Test Connector (16 lines)
1 7408925 Test Connector (1 line)
4 BC08R Cables
4 M971 Cable Modules
A/R DM11-DC EIA/CCITT Level Converters with BC01R-25 Modem Cables
1 Jumper
1 MainDEC-11-D9KA

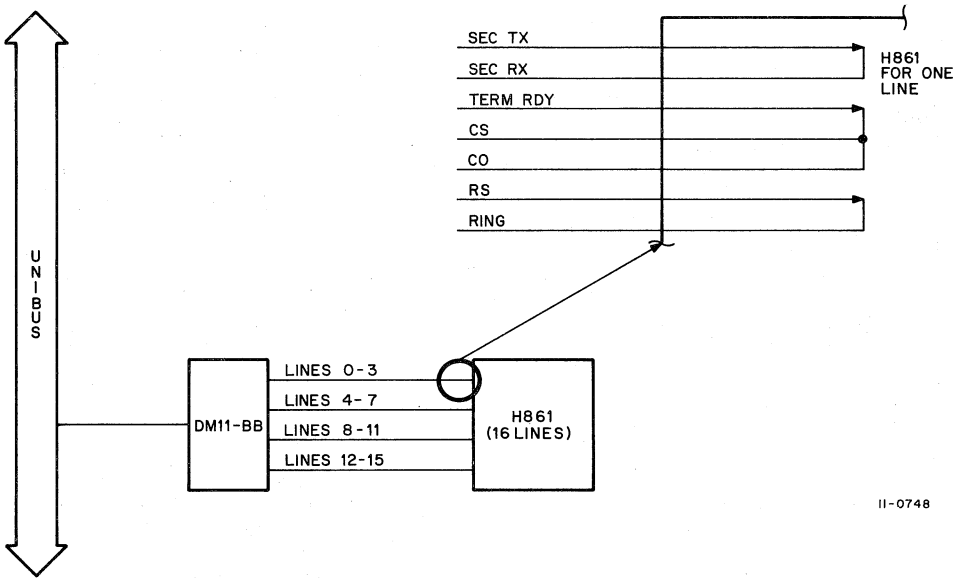


Figure 5-1 Test Configuration (DM11-BB with H861)

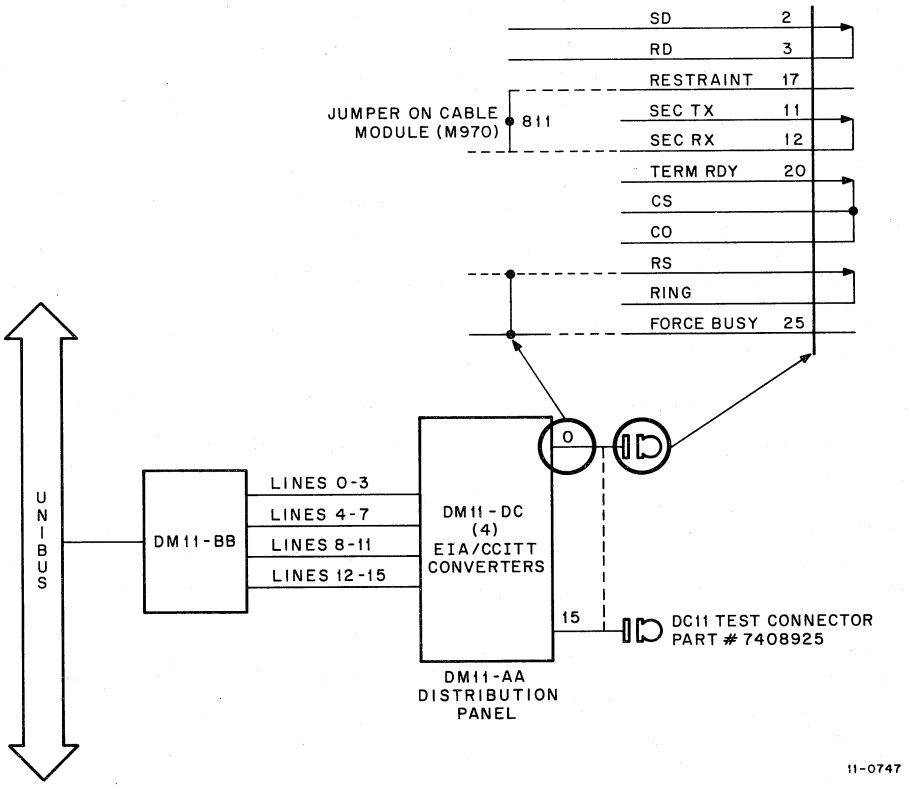


Figure 5-2 Test Configuration
(DM11-BB, Distribution Panel and Test Connector)

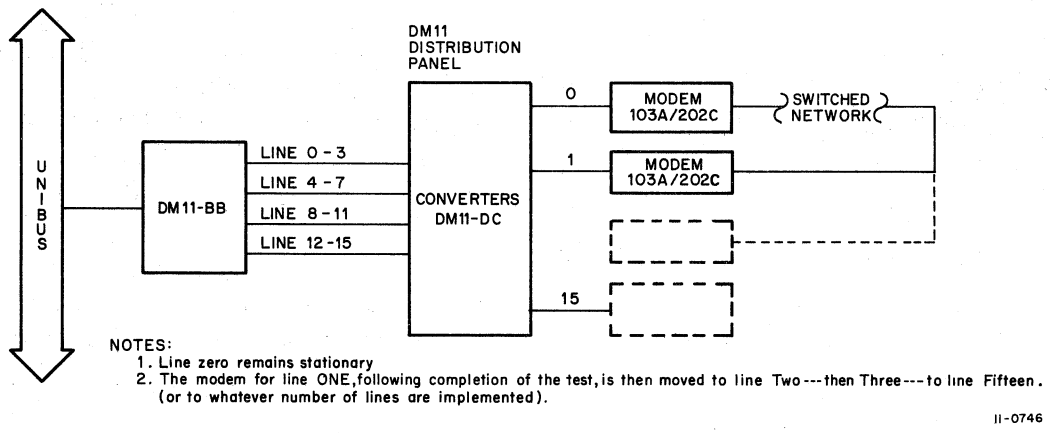


Figure 5-3 Test Configuration (ON LINE Modem Loop Back)

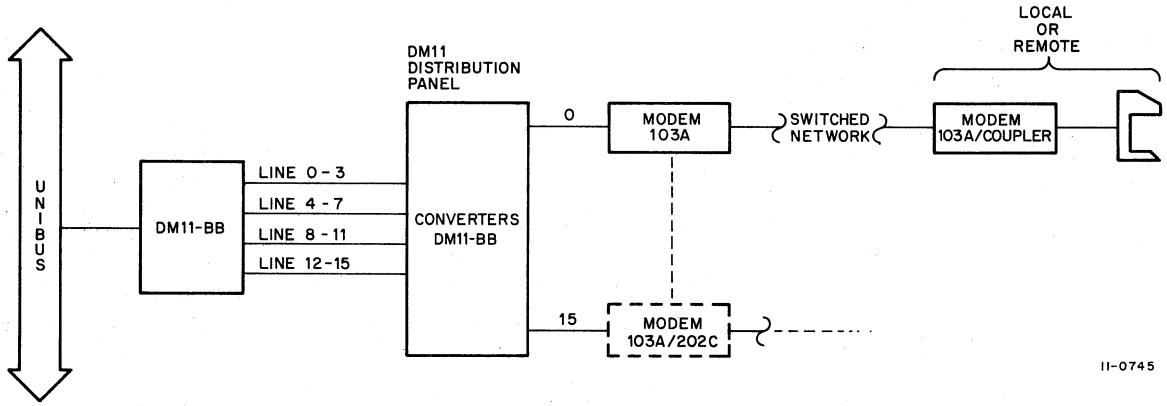


Figure 5-4 Test Configuration (ON LINE Modem to Terminal)

OFF LINE – Terminated with H861

Step	Procedure
1	Assemble hardware per Figure 5-1.
2	Operate MainDEC-11-D9KA per MainDEC procedures.
3	5 or more passes is considered a valid test.
4	Install jumper (labeled 811) on the BC01R Cable Module, Type M970.
	NOTE **The 811 jumper will cause malfunction if used on a synchronous interface.**
5	Assemble hardware per Figure 5-2.
6	Operate MainDEC-11-D9KA per MainDEC procedures.
7	5 or more passes are considered a valid test.

5.2.2 ON LINE

The ON LINE Test/Diagnostic will function with limited configurations and is intended to perform a confidence test, in that the DM11-BB will adapt to 103, 202, and 811B (or equivalent) type modems. The 811B configuration is left out as the 202 satisfactorily exercises all of the active elements used with the 811B Interface.

The ON LINE test utilizes two configurations as illustrated in Figures 5-3 and 5-4. Figure 5-3 utilizes two modems; they may be either two 103As or two 202Cs.

Figure 5-4 provides an ON LINE test for up to 16 lines to a local or remote terminal. In this configuration, the DM11-BB is operated in the Auto-Answer mode. The modems connected to the DM11-BB are 103As, while those connected to the terminal may be 103As or acoustic couplers.

The hardware required is:

1 PDP-11 with > 4K Core
1 DM11-AA
1 DM11-BB Module Set
4 BC08R Cables
4 M971 Cable Modules
A/R DM11-DC Converters
A/R Modems (103A or 202C)

ON LINE – Modem Loop

Step	Procedure
1	Assemble hardware per Figure 5-3.
2	Connect a modem (originate) to Line 0.
3	A second modem (answer) should be connected to any line that requires a test (Lines 1 through 15).
4	Operate MainDEC-11-D9KA per MainDEC procedures.
5	5 or more passes are considered a valid test.

ON LINE – Modem to Terminal

Step	Procedure
1	Assemble hardware per Figure 5-4.
2	Connect modem (103A) as required to lines 0 through 15. These modems should be connected for Auto-Answer mode of operation. **NOTE** **The terminal should originate all communications channels.**
3	Operate MainDEC-11-D9KA per MainDEC Instructions.
4	Satisfactory transfers to (from) the terminal(s) is considered a valid test.

APPENDIX A
GLOSSARY

DM11-BB Terms	Definitions
TP	Test Point
Sec Rx	Secondary Received Data (202)
Carrier or CO	Received Line Signal Detector (CF)
CS	Clear to Send (CB)
RING	Ring Indicator (CE)
LINE CNT	Line Count
CNTR	Counter
LSB	Least Significant Bit
MSB	Most Significant Bit
EN	Enable
INI	Initialize
INTR	Interrupt
HOLD (Ring, CO, CS, Sec Rx)	Holding register for last known status (not current)
Request to Send or RS	Request to Send (CA)
Sec Tx	Secondary Transmitted Data (202)
TERM RDY	Data Terminal Ready (CD)
LINE EN	Line Enable
X DCDR	X Decoder for Memory
Y DCDR	Y Decoder for Memory
BUSY	Force Busy (103E)

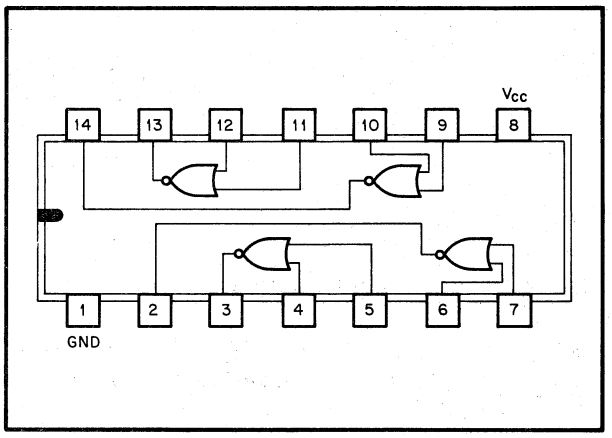
APPENDIX B
IC DESCRIPTIONS

B.1 DM11-BB INTEGRATED CIRCUIT (IC) DESCRIPTIONS

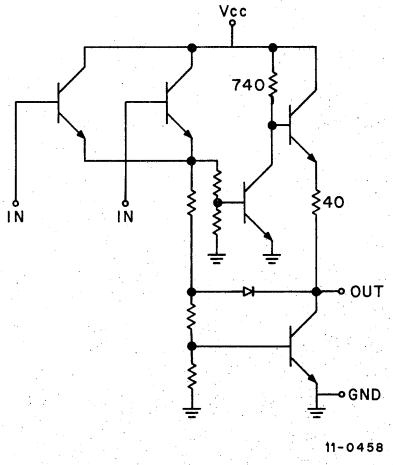
This section provides diagrams, truth tables, pin assignments, and some descriptions of the integrated circuit units used in the DM11-BB logic. The ICs covered in this section are listed as follows:

380 NOR Gates
1488 Quad Line Drivers
1489 Quad Line Receivers
4007 Dual-Binary-To-One-of-Four-Line Decoder
4015 Quad Type D Flip-Flop
7400 Quad 2-Input Positive NAND Gates
7404 Hex Inverters
7408 Quad 2-Input Positive AND Gates
7410 Triple 3-Input Positive NAND Gates
7416 Hex Inverter Buffers/Drivers
7417 Hex Buffers/Drivers
7442 4-Line-To-10-Line Decoders
7474 Dual D-Type Edge-Triggered Flip-Flops
7481 16-Bit Active-Element Memories
7486 Quad 2-Input Exclusive-OR Gates
74151 Data Selector/Multiplexer
74197 50-MHz Presettable Decode and Binary Counters/Latches
8271 4-Bit Shift Register
8815 Dual 4-Input NOR Gates
8881 Quad 2-Input NAND Gates

380 NOR GATES

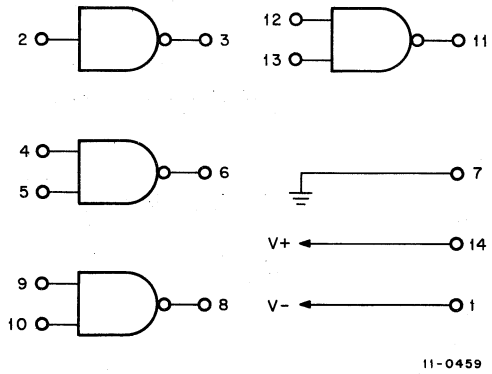


11-0759

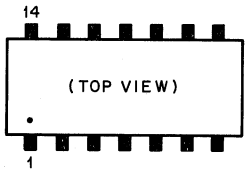


11-0458

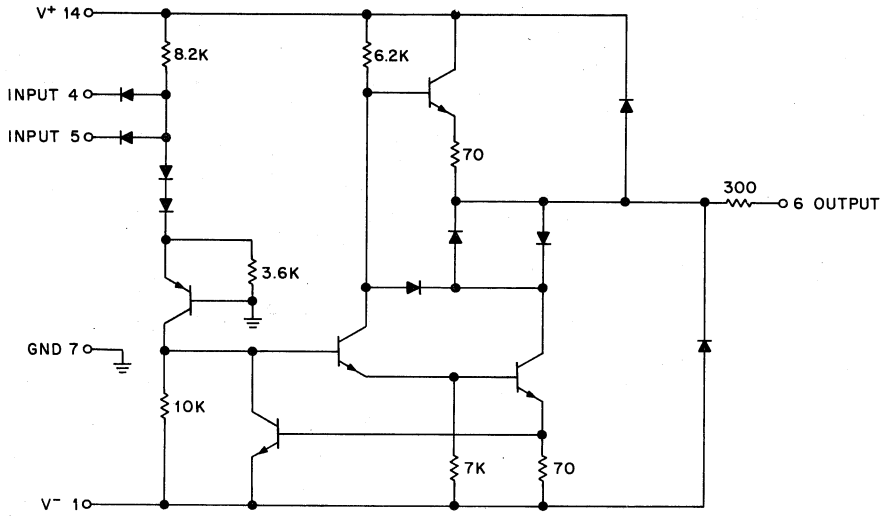
MC1488L QUAD LINE DRIVER



11-0459



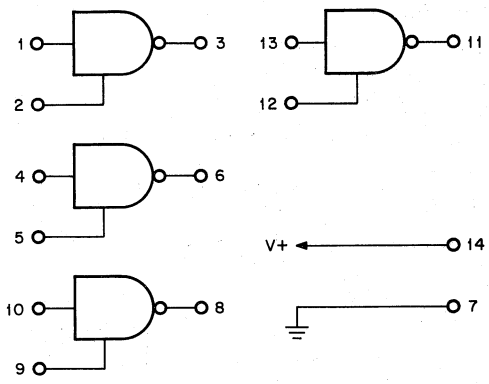
11-0486



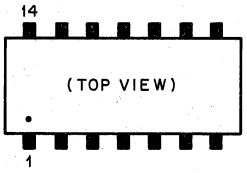
NOTE:
1/4 of circuit shown.

11-0760

MC1489 QUAD LINE RECEIVERS



11-0460



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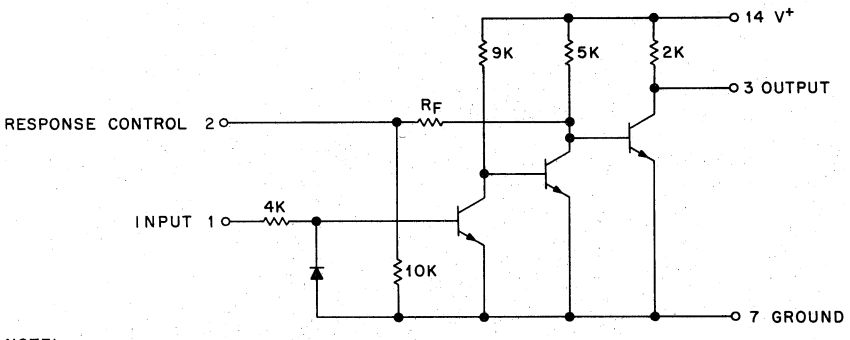
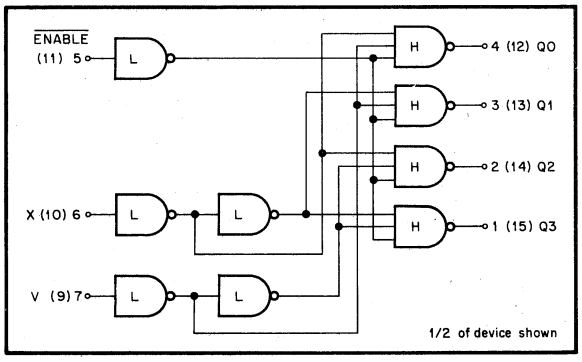


NOTE:
1/4 of circuit shown.

11-0761

4007 DUAL-BINARY-TO-ONE-OF-FOUR LINE DECODER



11-0742

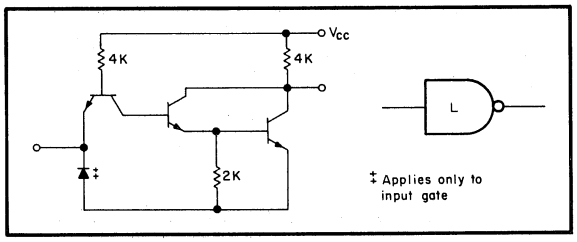
E = 0

TRUTH TABLE

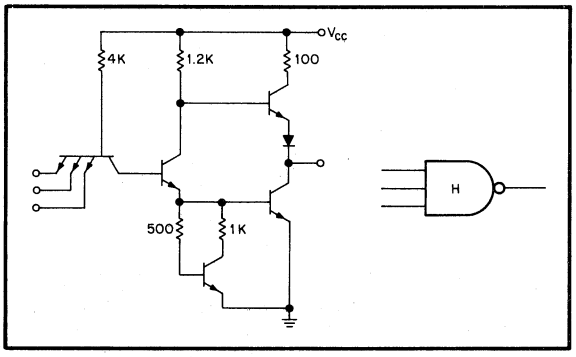
X	Y	Q0	Q1	Q2	Q3
0	0	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
1	1	1	1	1	0

1 = High State
0 = Low State

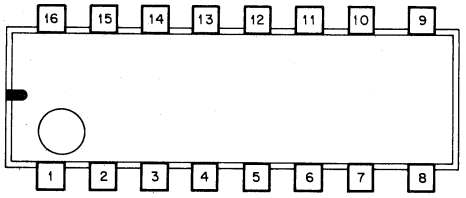
LOW-LEVEL GATE



HIGH-LEVEL GATE

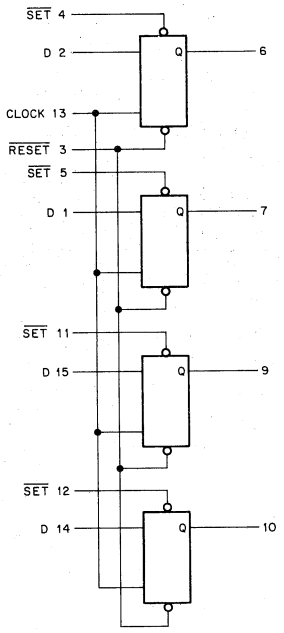


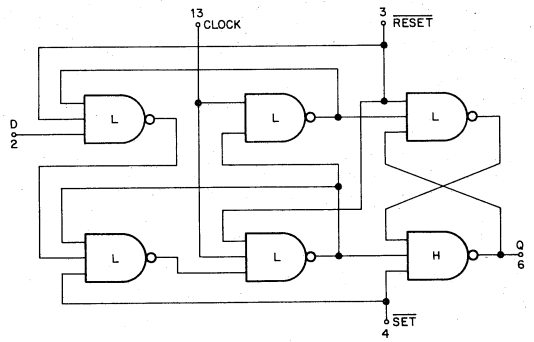
11-0743



11-0744

4015 QUAD TYPE D FLIP-FLOP

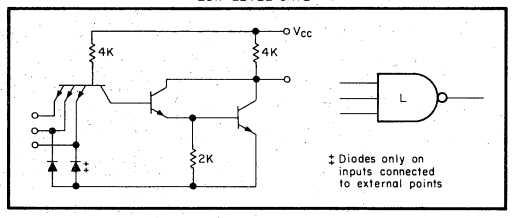




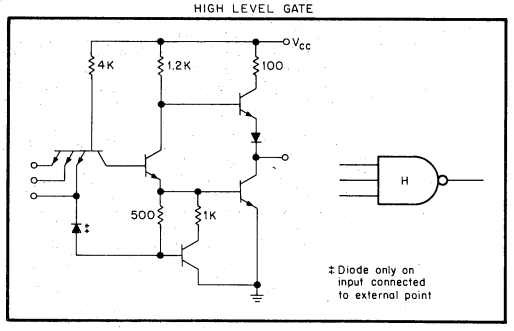
1/4 OF DEVICE SHOWN
CLOCK AND $\overline{\text{RESET}}$ COMMON TO ALL FOUR FLIP-FLOPS
V_{cc} = PIN 16
GND = PIN 8

11-0739

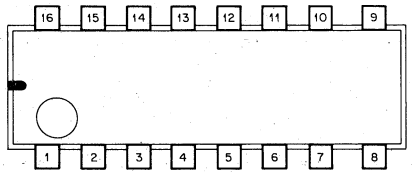
LOW LEVEL GATE



HIGH LEVEL GATE



11-0740



11-0741

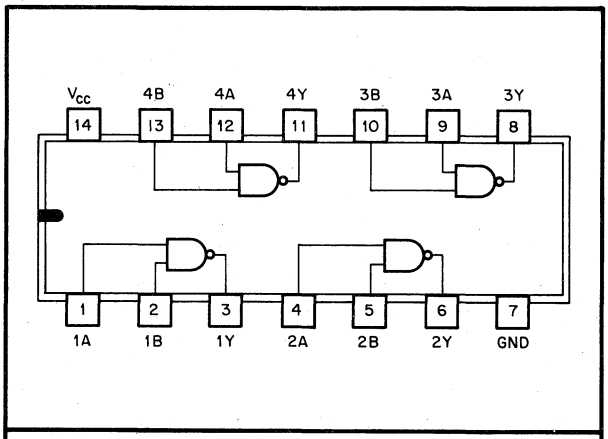
TRUTH TABLE

D	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = time period prior to clock pulse

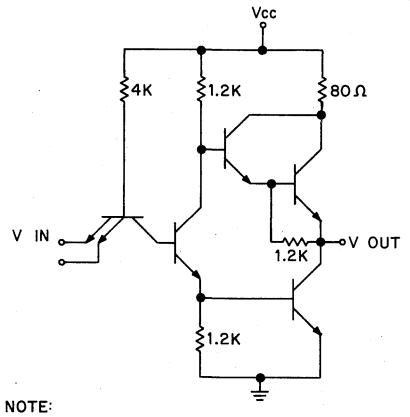
Q_n = time period following clock pulse

7400 QUAD 2-INPUT POSITIVE NAND GATES



POSITIVE LOGIC: $Y = \overline{AB}$

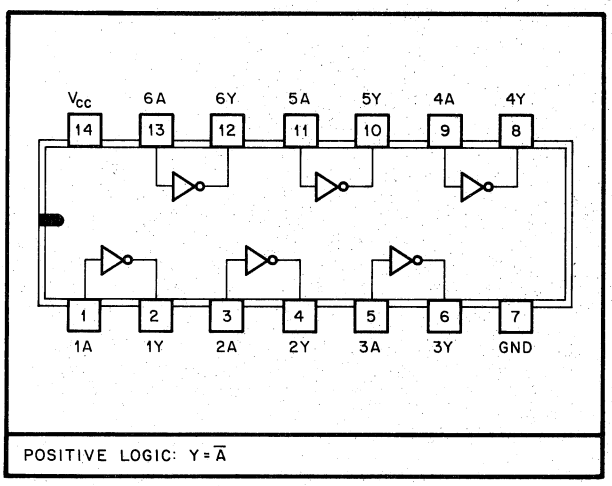
11-0762



NOTE:
Component values are typical.

11-0461

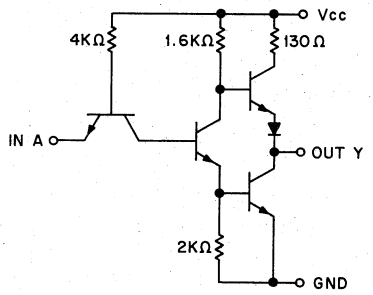
7404 HEX INVERTERS



POSITIVE LOGIC: $Y = \overline{A}$

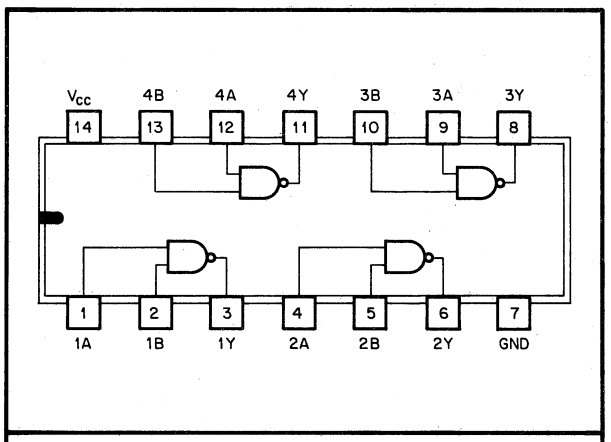
11-0763

Schematic (each inverter)



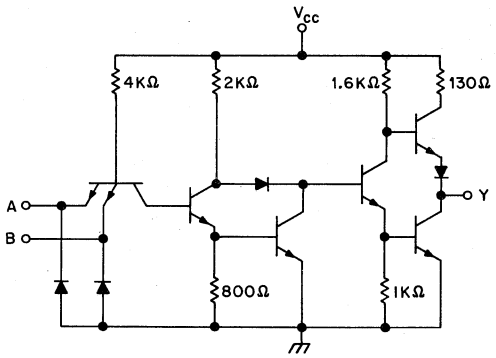
NOTE:
Component values shown are nominal.

7408 QUAD 2-INPUT POSITIVE AND GATES



POSITIVE LOGIC: Y = AB

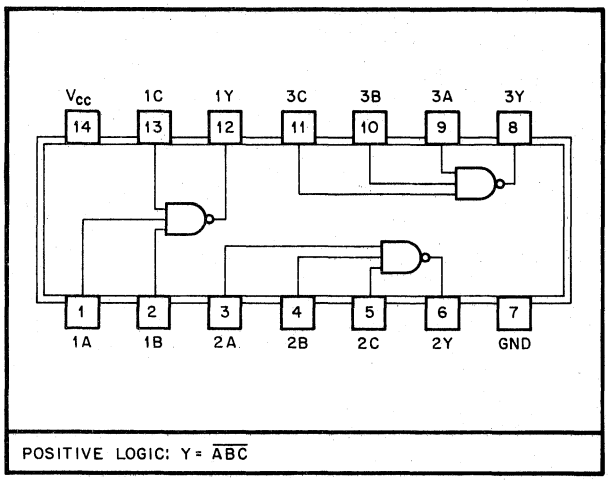
11-0738



Component values shown are nominal.

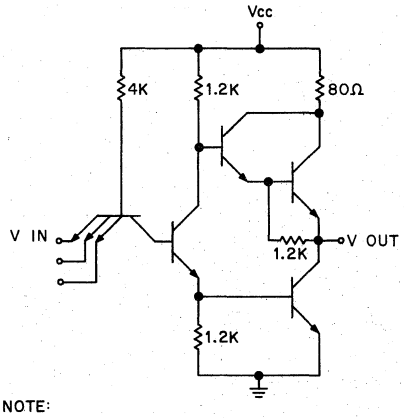
11-0737

7410 3-INPUT POSITIVE NAND GATES



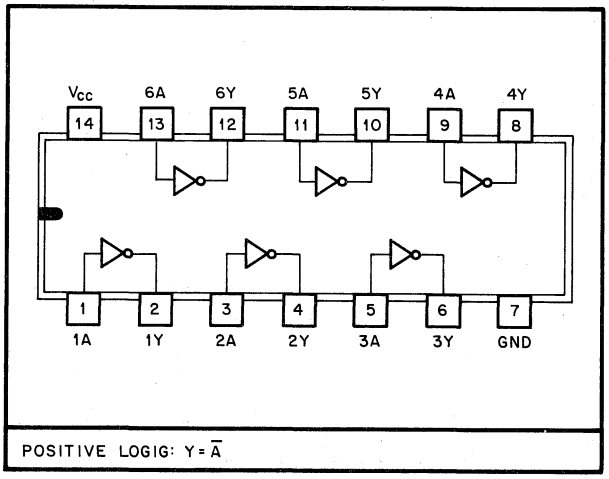
POSITIVE LOGIC: $Y = \overline{ABC}$

11-0764



NOTE:
Component values are typical.

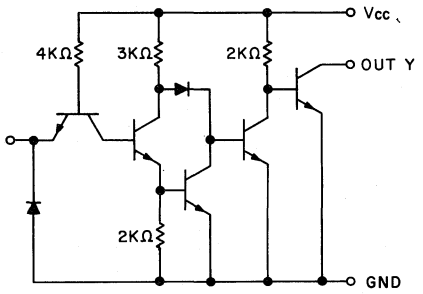
7416 HEX INVERTER BUFFERS/DRIVERS



POSITIVE LOGIG: $Y = \overline{A}$

11-0765

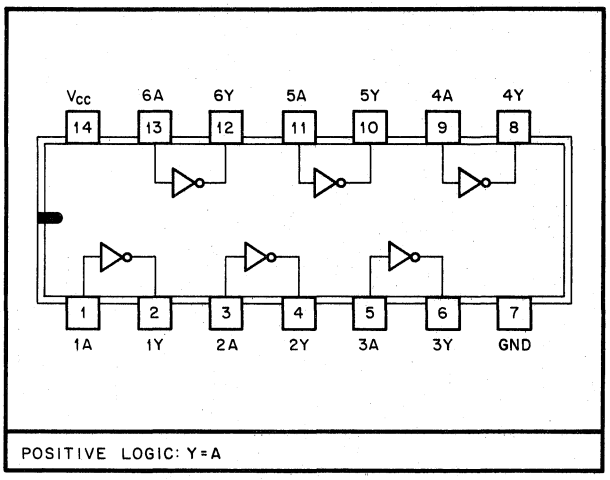
Schematic (each inverter)



NOTE:
Component values shown are nominal.

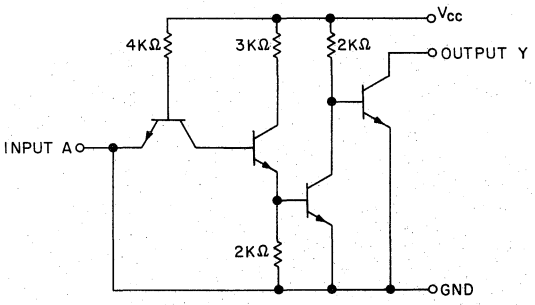
11-0465

7417 HEX BUFFERS/DRIVERS



POSITIVE LOGIC: Y=A

11-0736

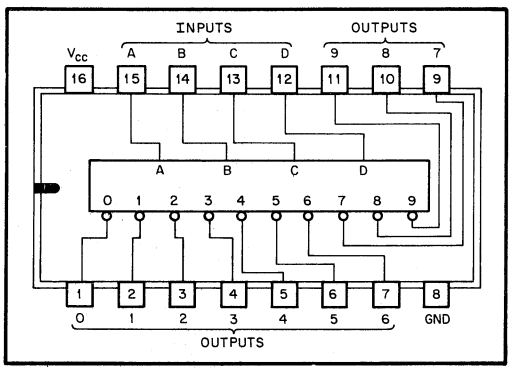


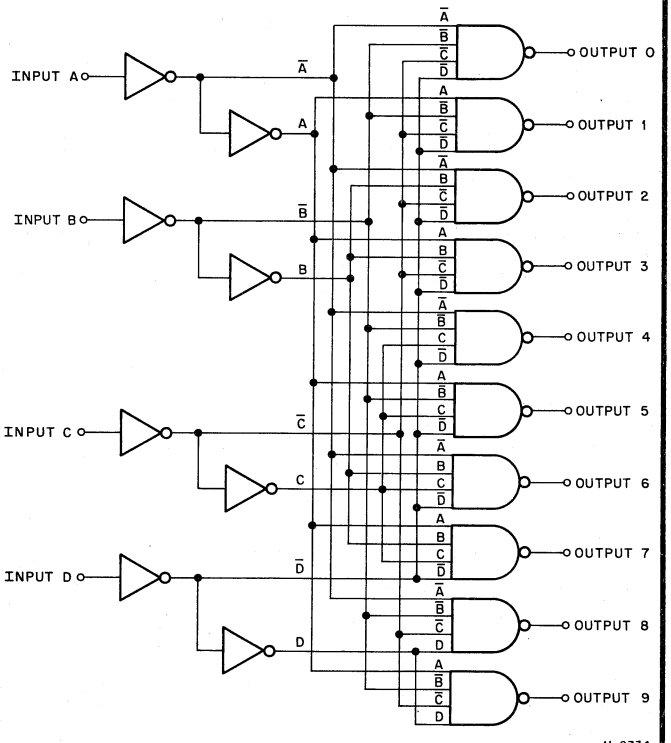
Component values shown are nominal.

11-0735

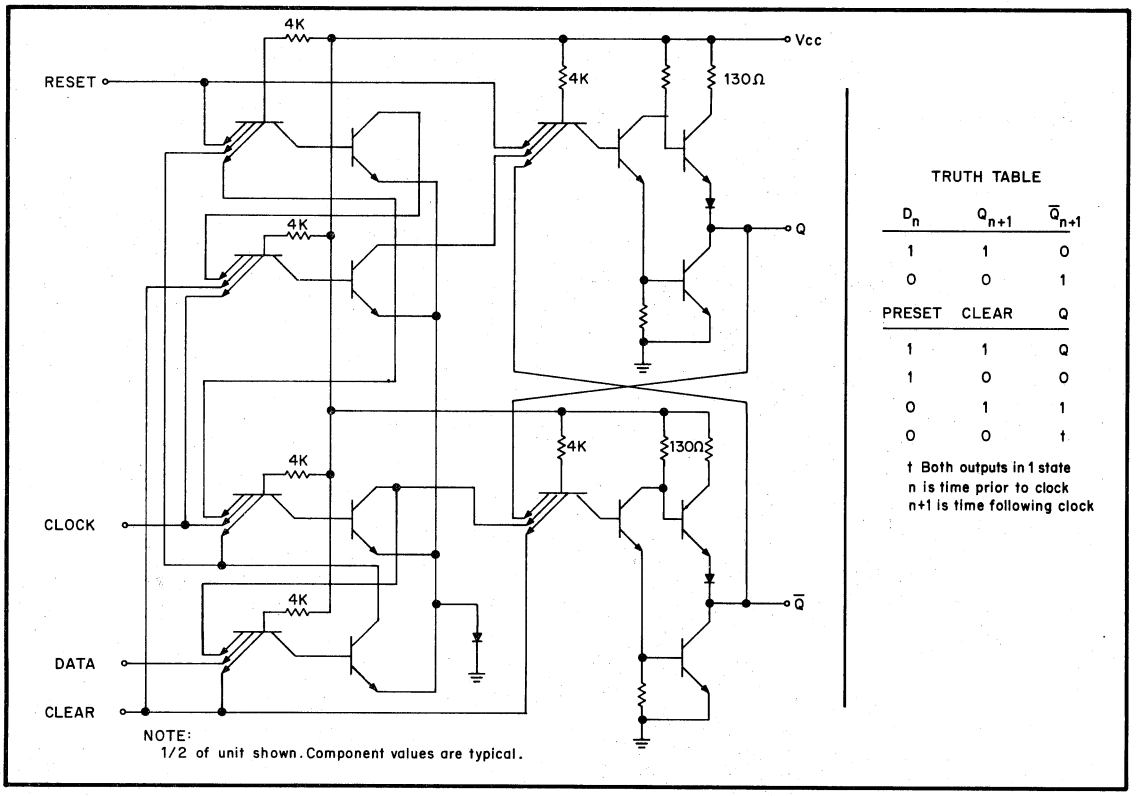
TRUTH TABLES

BCD Input				Decimal Output									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1





SN7474 DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS



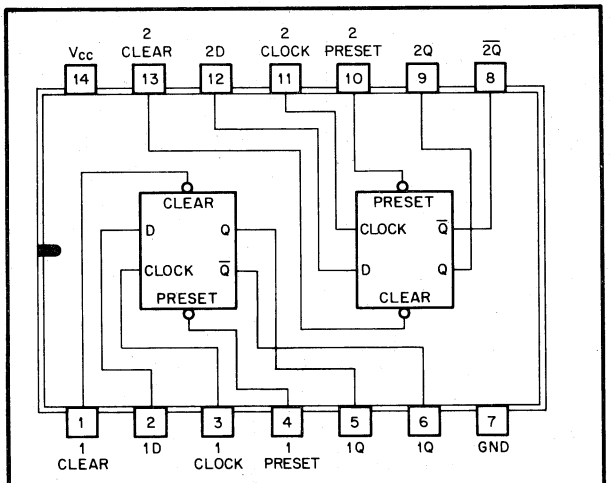
TRUTH TABLE

D_n	Q_{n+1}	$\overline{Q}_{n+1}$
1	1	0
0	0	1

PRESET	CLEAR	Q
1	1	Q
1	0	0
0	1	1
0	0	†

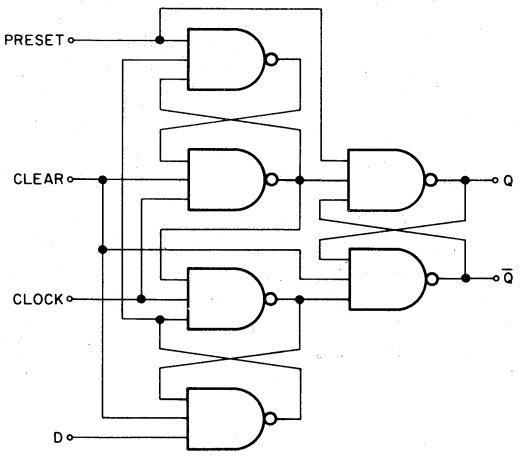
† Both outputs in 1 state
n is time prior to clock
n+1 is time following clock

11-0469

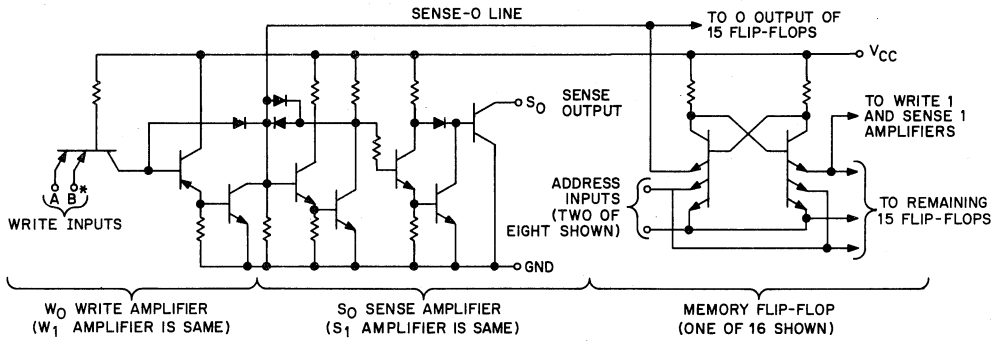


POSITIVE LOGIC: LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
PRESET AND CLEAR ARE INDEPENDENT OF CLOCK

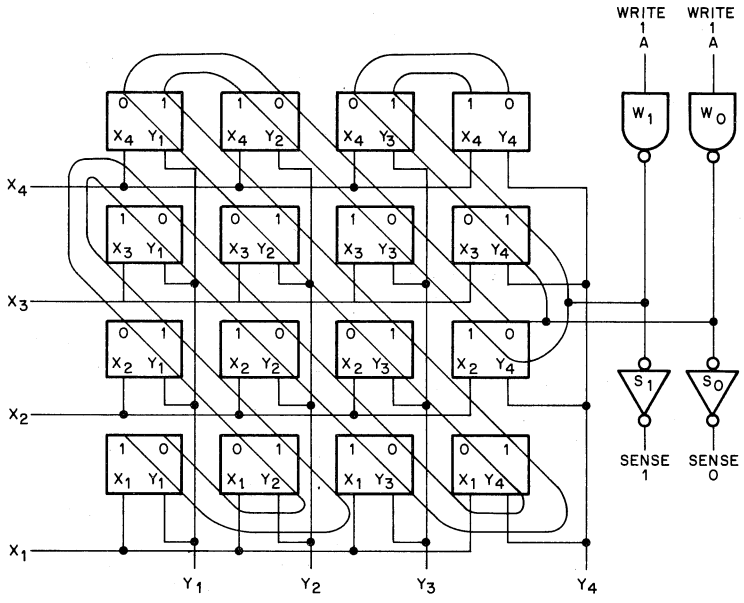
11-0766



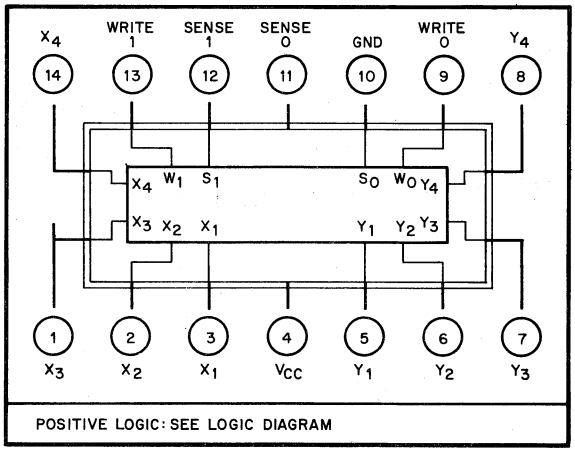
11-0767



II-0729

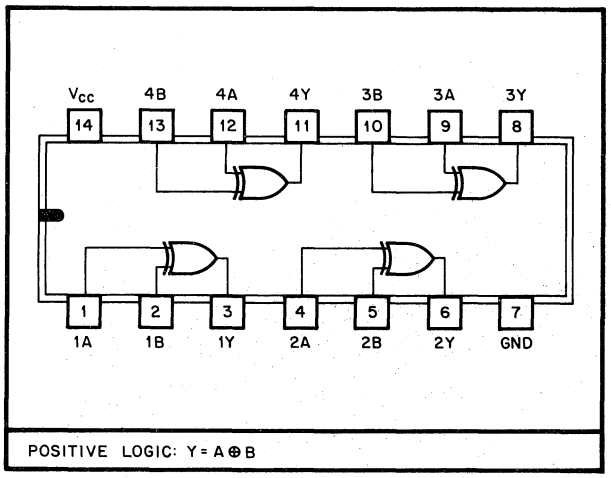


II-0731



II-0730

SN7486 QUAD 2-INPUT EXCLUSIVE-OR GATES



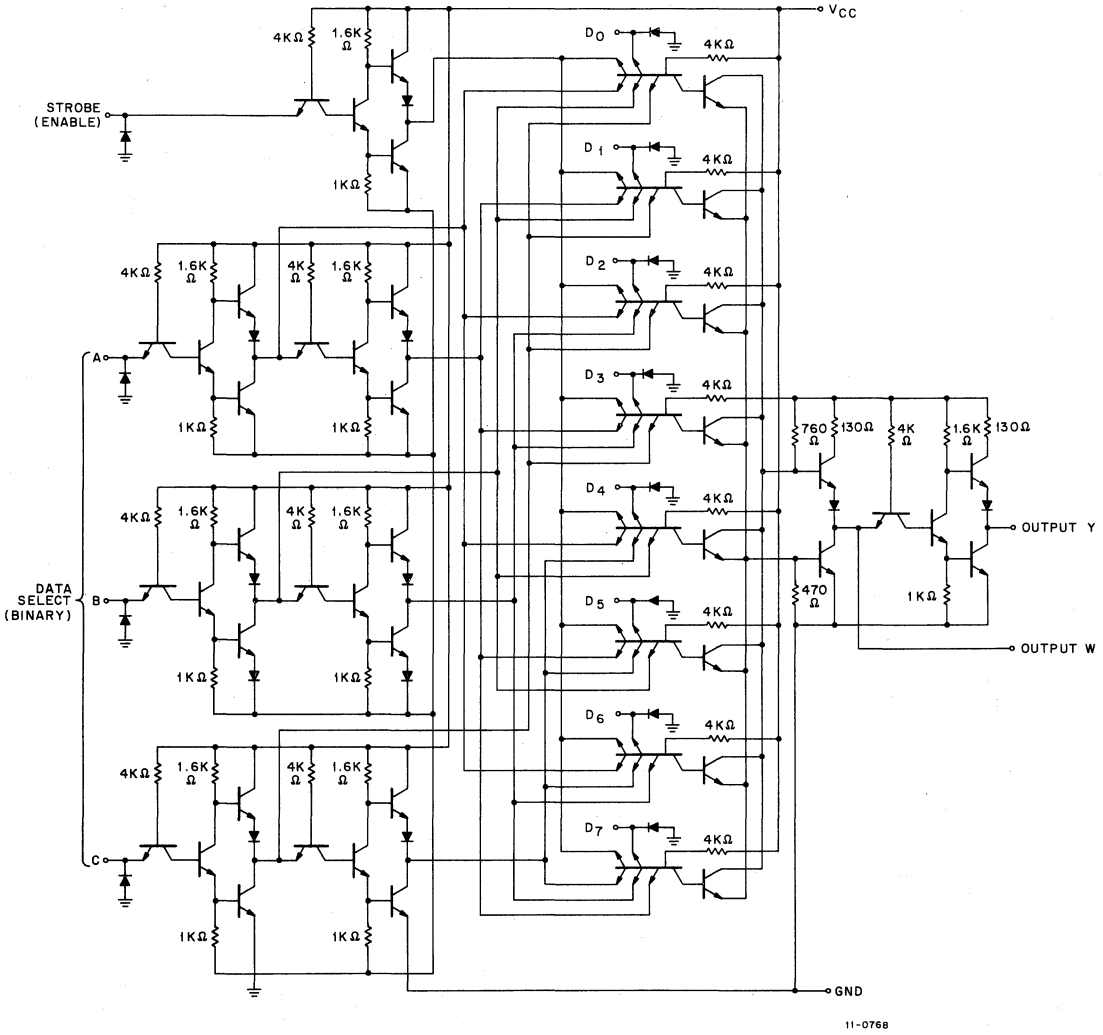
POSITIVE LOGIC: $Y = A \oplus B$

11-0732

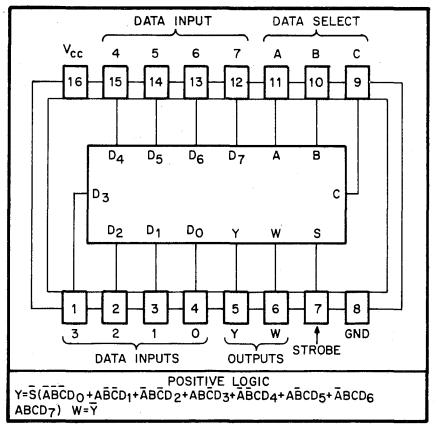
TRUTH TABLE

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

74151 DATA SELECTOR/MULTIPLEXER



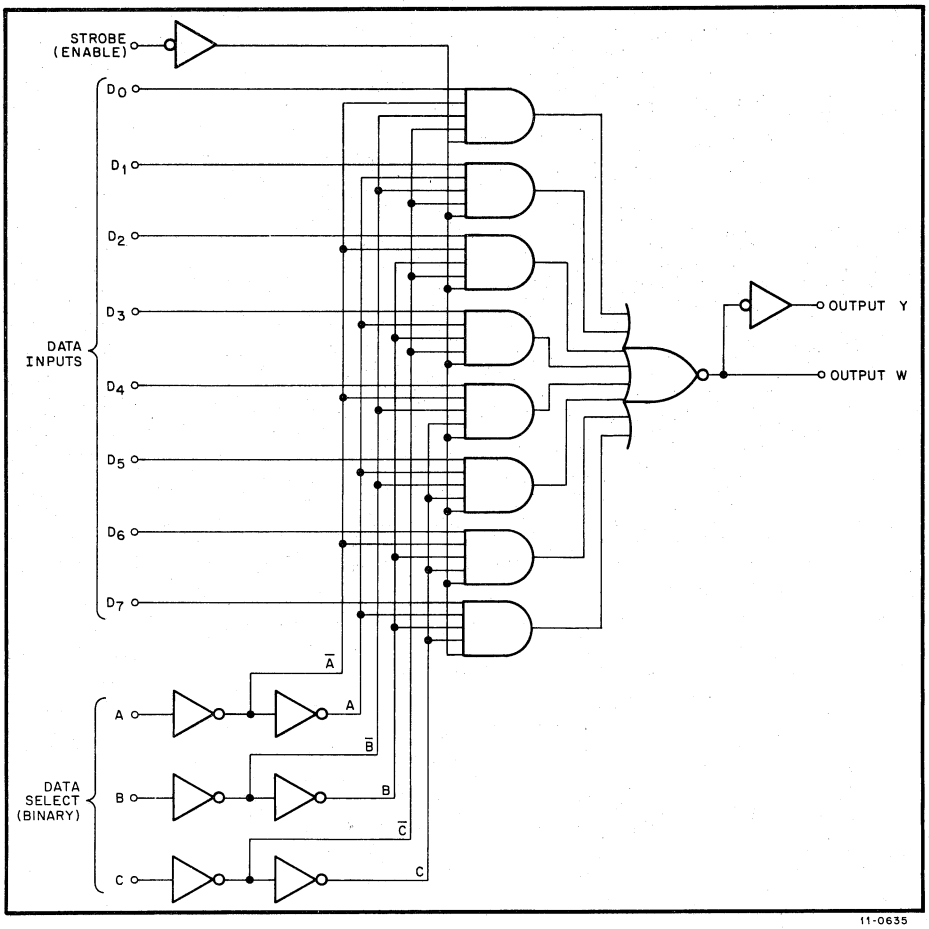
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



POSITIVE LOGIC

$Y=\bar{S}(\bar{A}\bar{B}\bar{C}D_0+A\bar{B}\bar{C}D_1+\bar{A}B\bar{C}D_2+AB\bar{C}D_3+\bar{A}\bar{B}CD_4+A\bar{B}CD_5+\bar{A}BCD_6+ABCD_7)$ $W=\bar{Y}$

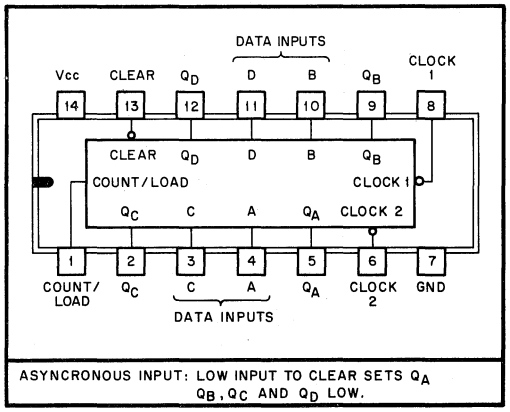
11-0634



TRUTH TABLE SN74151

Inputs												Outputs	
C	B	A	Strobe(1)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y(1)	W
x	x	x	1	x	x	x	x	x	x	x	x	0	1
0	0	0	0	0	x	x	x	x	x	x	x	0	1
0	0	0	0	1	x	x	x	x	x	x	x	1	0
0	0	1	0	x	0	x	x	x	x	x	x	0	1
0	0	1	0	x	1	x	x	x	x	x	x	1	0
0	1	0	0	x	x	0	x	x	x	x	x	0	1
0	1	0	0	x	x	1	x	x	x	x	x	1	0
0	1	1	0	x	x	x	0	x	x	x	x	0	1
0	1	1	0	x	x	x	1	x	x	x	x	1	0
1	0	0	0	x	x	x	x	0	x	x	x	0	1
1	0	0	0	x	x	x	x	1	x	x	x	1	0
1	0	1	0	x	x	x	x	x	0	x	x	0	1
1	0	1	0	x	x	x	x	x	1	x	x	1	0
1	1	0	0	x	x	x	x	x	x	0	x	0	1
1	1	0	0	x	x	x	x	x	x	1	x	1	0
1	1	1	0	x	x	x	x	x	x	x	0	0	1
1	1	1	0	x	x	x	x	x	x	x	1	1	0

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE
(TOP VIEW)*



ASYNCRONOUS INPUT: LOW INPUT TO CLEAR SETS Q_A Q_B, Q_C AND Q_D LOW.

*Pin assignments for these circuits are the same for all packages.

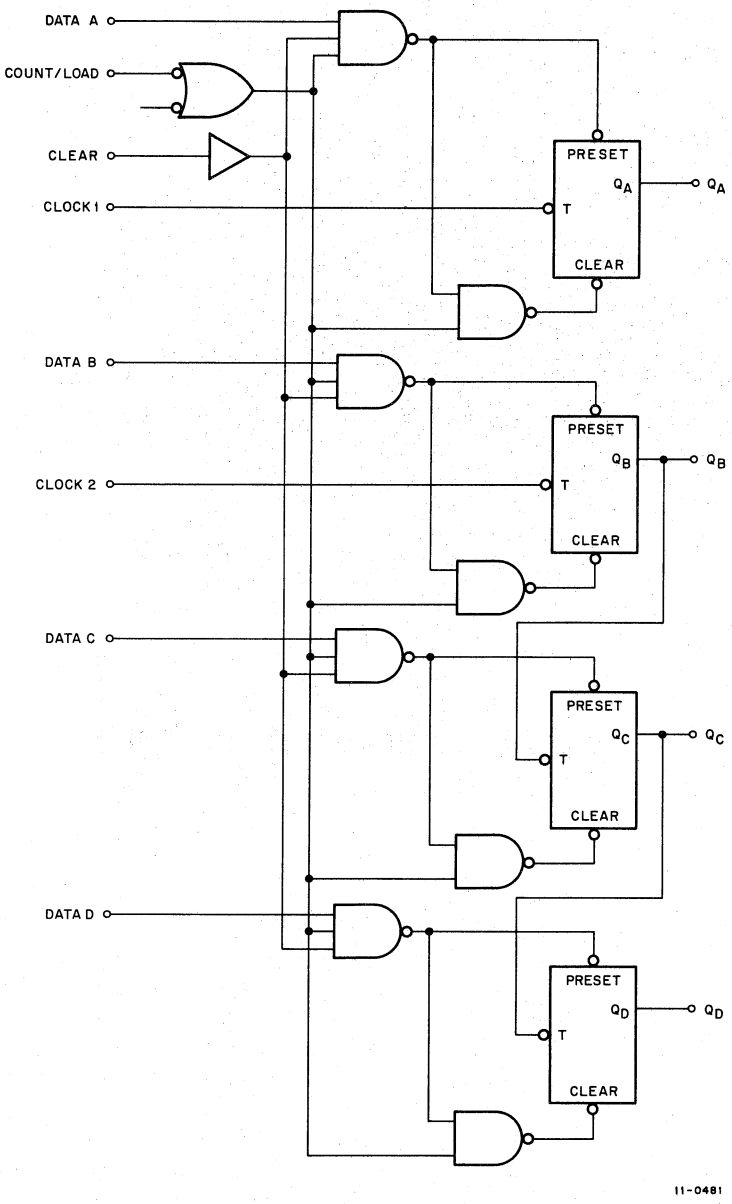
11-0482

SN74197 TRUTH TABLE
(See Note A)

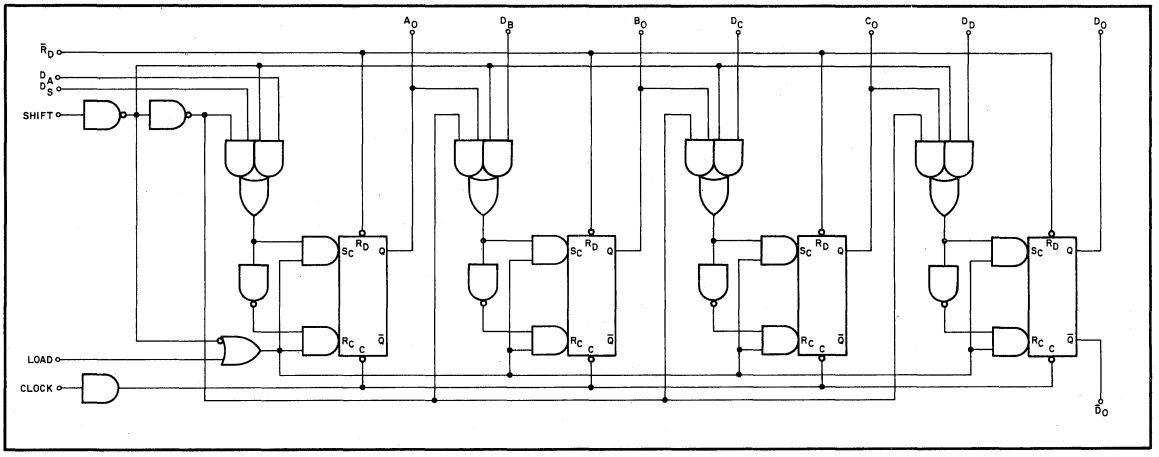
Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE A: Output Q_A connected to clock-2 input.

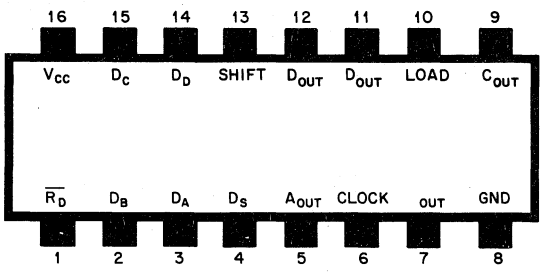
74197 50-MHz PRESETTABLE DECODE AND BINARY COUNTERS/LATCHES (Cont)



8271 4-BIT SHIFT REGISTER



12-0327

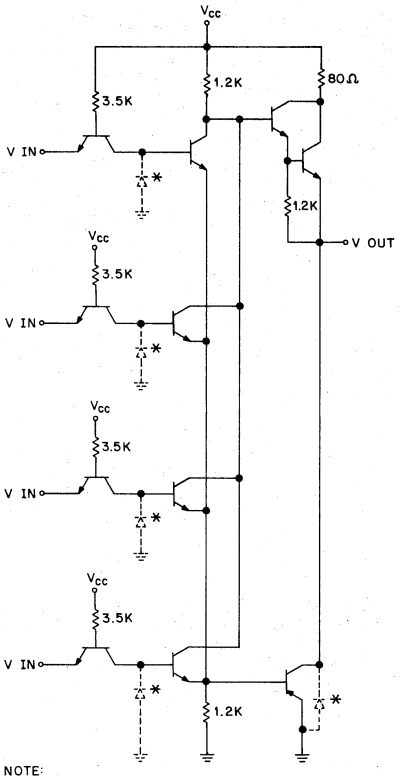


11-0756

TRUTH TABLE

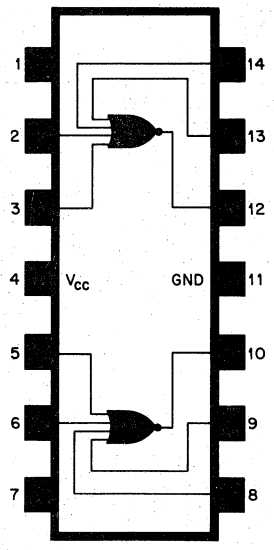
Control State	Load	Shift
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

8815 DUAL 4-INPUT NOR GATES



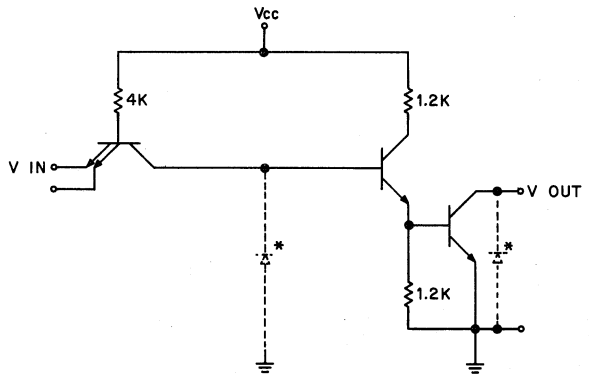
NOTE:
Component values are typical
* Isolation Diode

11-0901



11-0757

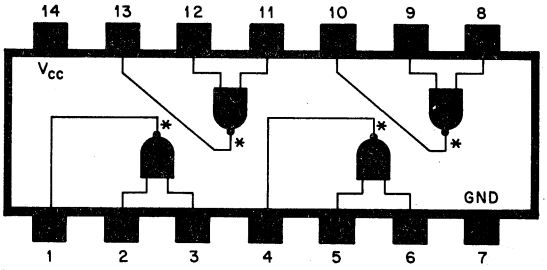
8881 QUAD 2-INPUT NAND GATES



NOTE:
1/4 of unit shown. Component values are typical.
*ISOLATION DIODE

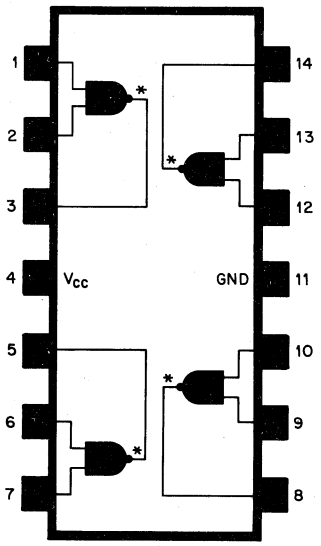
11-0480

A, F PACKAGE



*No pull-up provided

J PACKAGE



11-0758

APPENDIX C
MODEM TIMING AND FLOW DIAGRAMS

This appendix provides the timing and flow diagrams for some modems utilized with the DM11-BB. These diagrams are for reference information and are as follows:

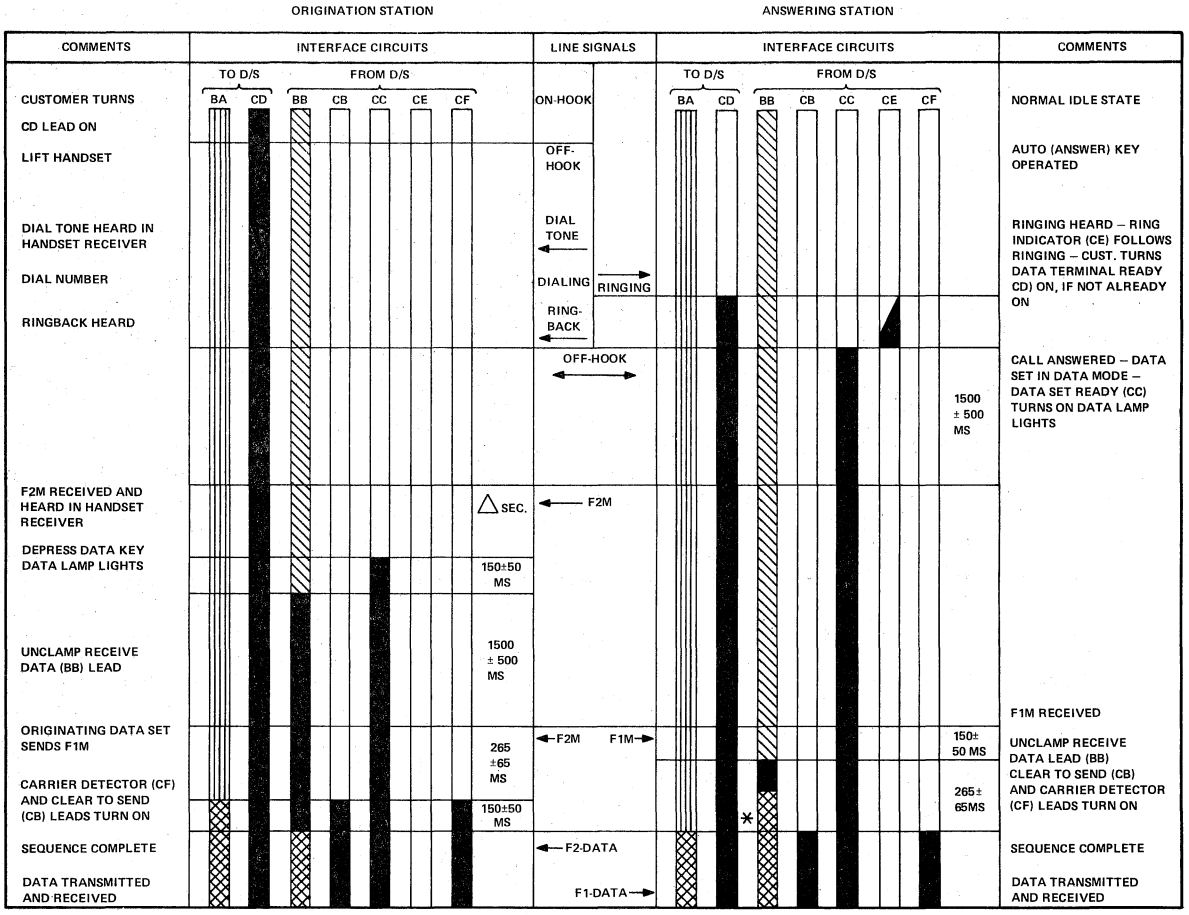


Figure C-1 Data Set 103A Channel Establishment Sequence

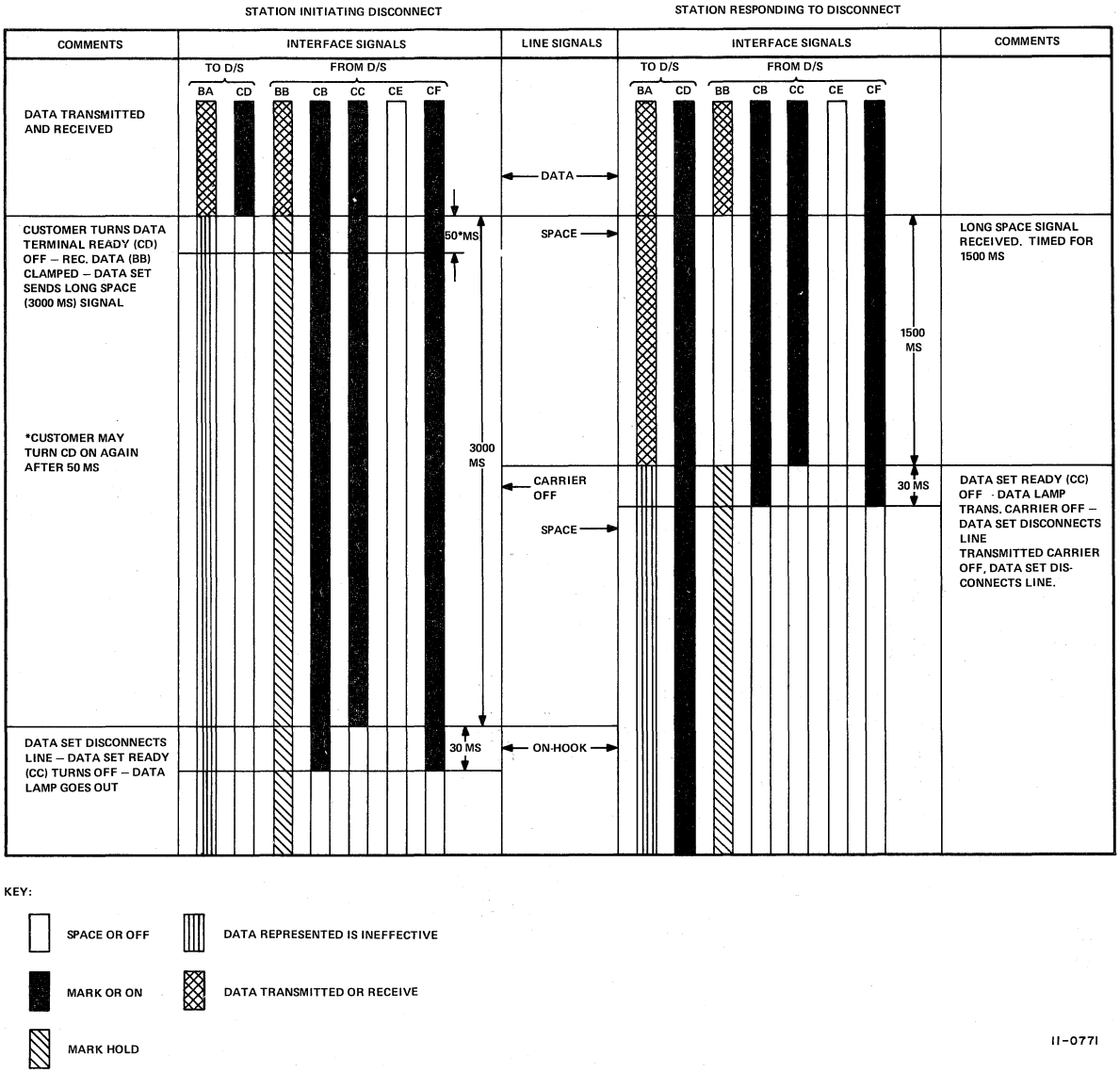


Figure C-2 Data Set 103A Space Disconnect Sequence

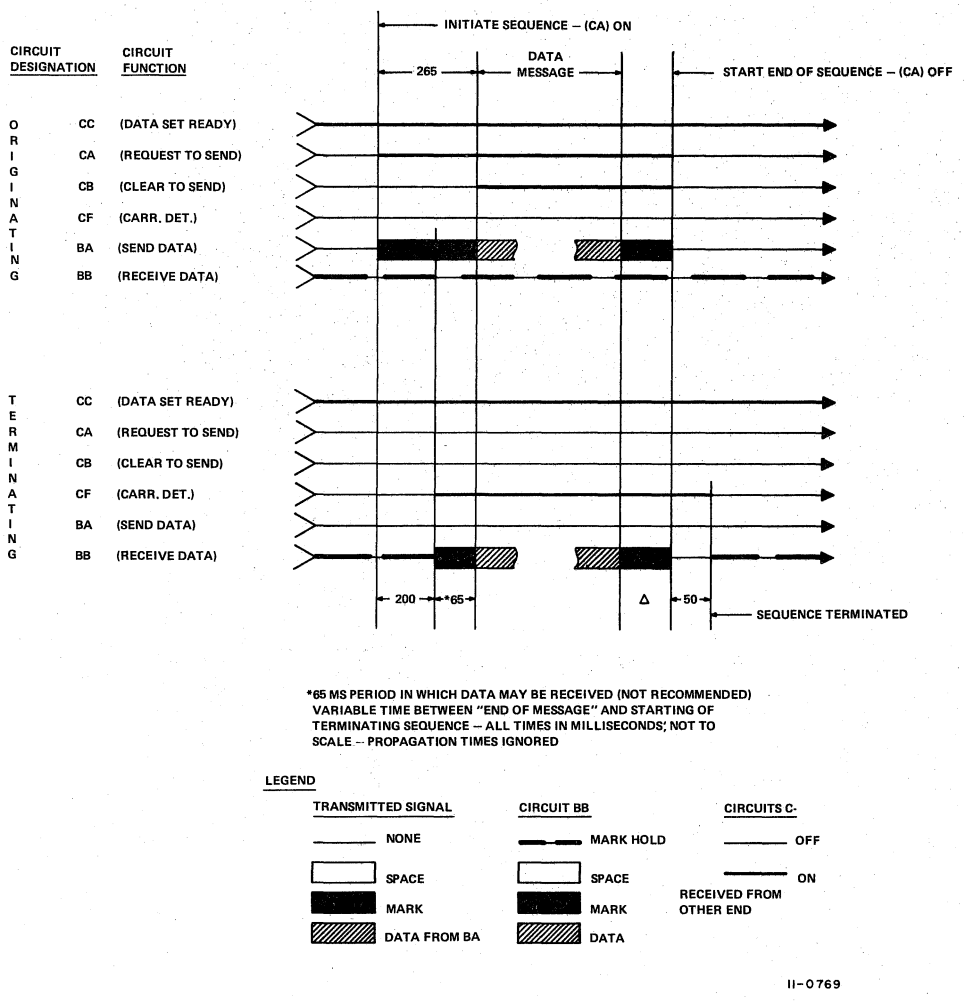


Figure C-3 Data Set 103F Timing Sequence

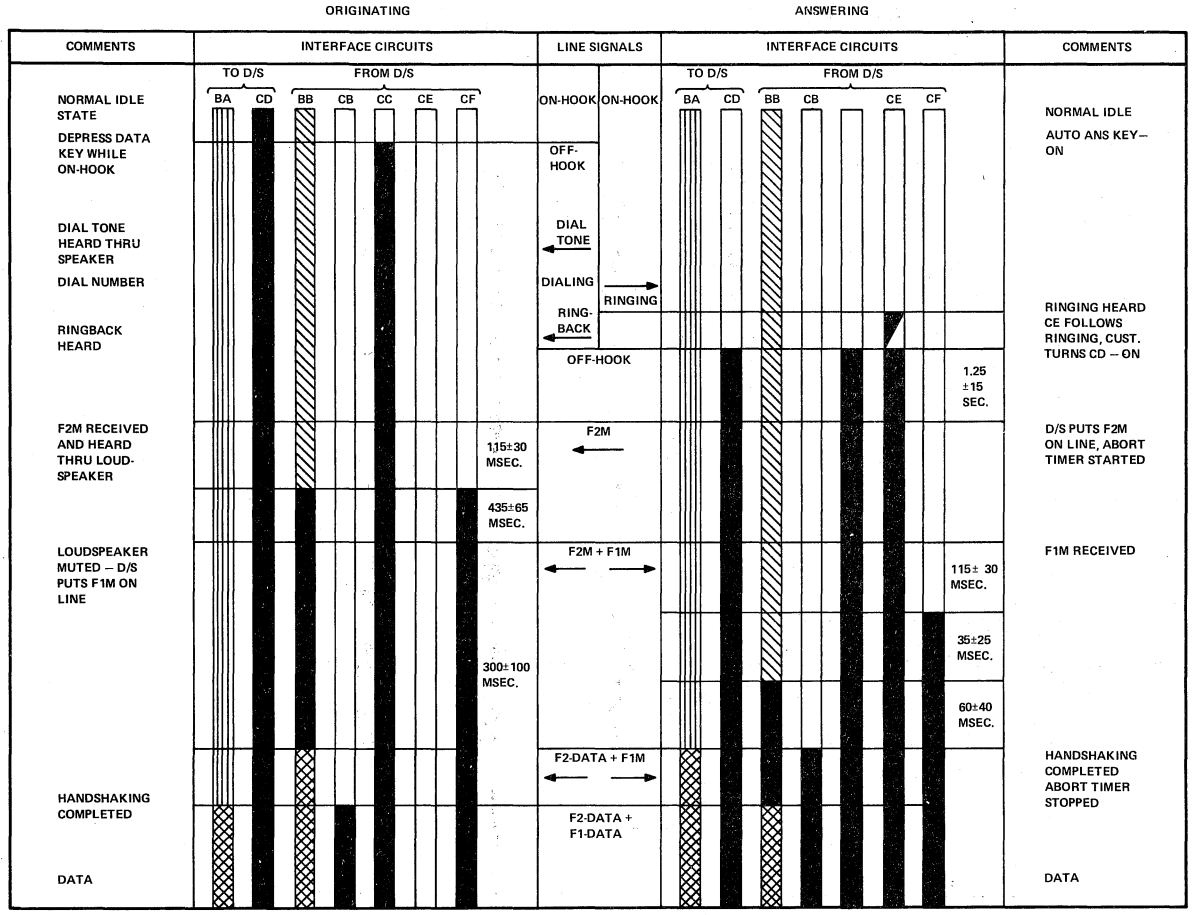
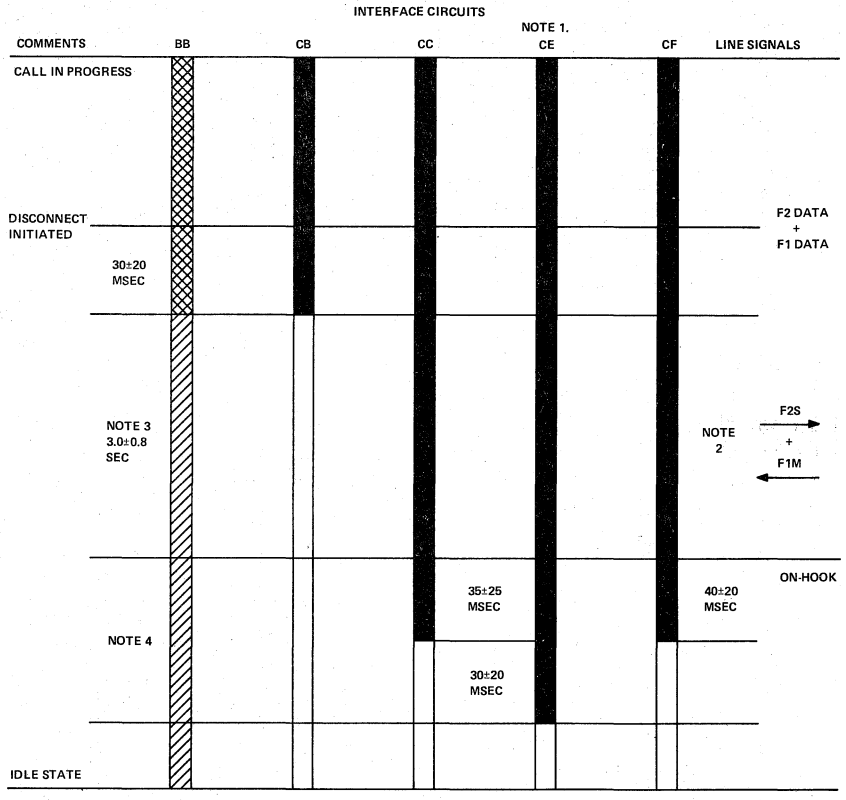


Figure C-4 Data Set 103E Type Sequence Chart for a Call Originated in the Semiautomatic Manner and Answered Automatically

1 DISCONNECT INITIATED BY EITHER
A) BUSINESS MACHINE TURNING CKT. CD OFF
B) ATTENDANT DEPRESSING CLEAR KEY, OR
C) AUTOMATIC CALLING UNIT SIGNALING DATA SET TO DISCONNECT



NOTES:
1. FOR ANS MODE STATION WITH "CE-ON" OPTION.
2. IF THE OTHER STATION IS WIRED TO DISCONNECT ON SPACE, CF WILL GO OFF DURING THIS INTERVAL.
3. TIME SHOWN IS FOR "SEND DISCONNECT-YES" OPTION. TIME FOR "SEND DISCONNECT-NO" OPTION IS 30±20 MSEC, IF DISCONNECT IS INITIATED BY CD OFF. OTHERWISE TIME IS AS SHOWN.
4. SEQUENCING OF TURN-OFFS MAY BE EITHER CF, CC, CE, OR CC, CR, CE, OR CC, CE, CF.
5. TIME SHOWN IS FOR "CB-CF INDICATIONS SEPARATE" OPTION. FOR "CB-CF INDICATIONS COMMON" OPTION, CF TURNS OFF WITH CB.

11-0773

Figure C-5 Data Set 103E Type Detailed Disconnect Sequences

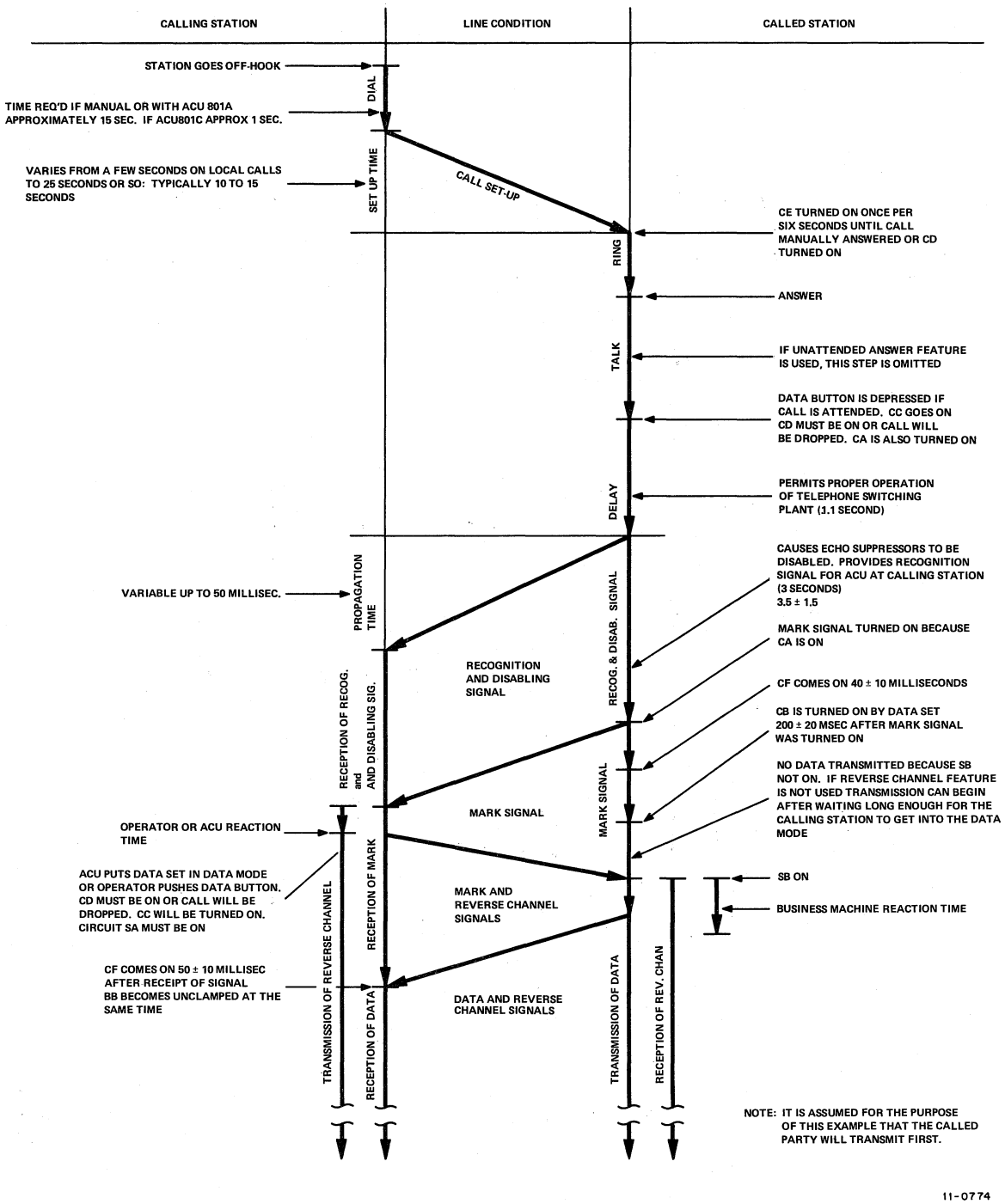


Figure C-6 Establishment of a 202C Call

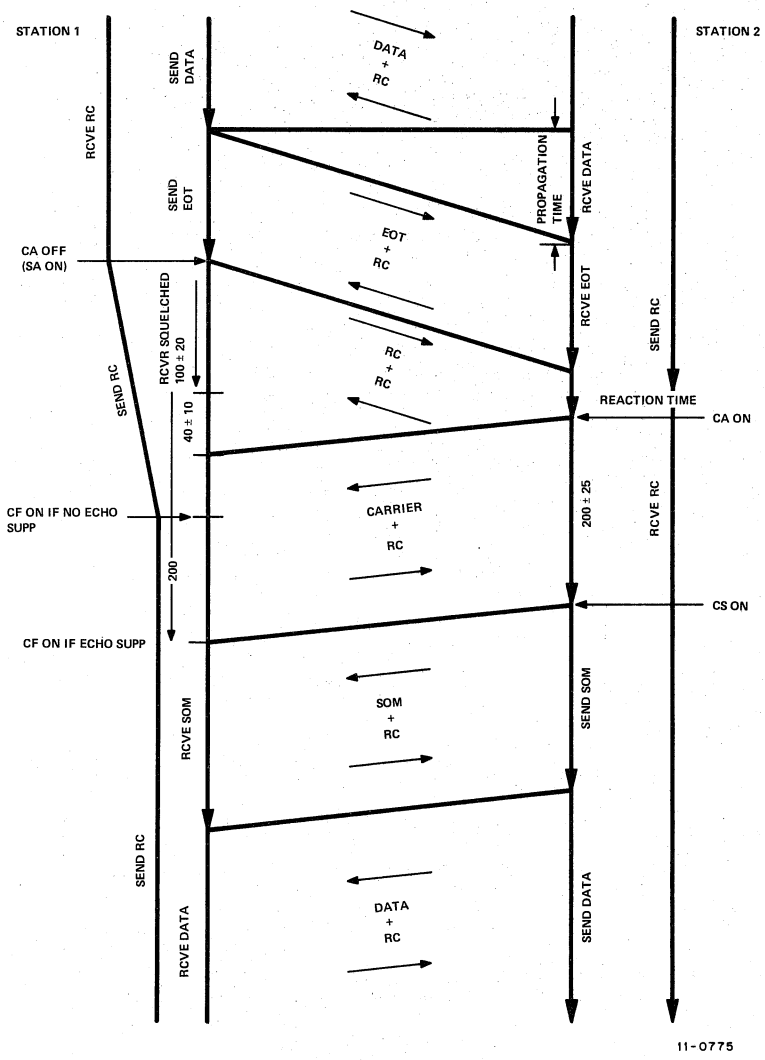


Figure C-7 Turn Around In Data-Phone Service 202C

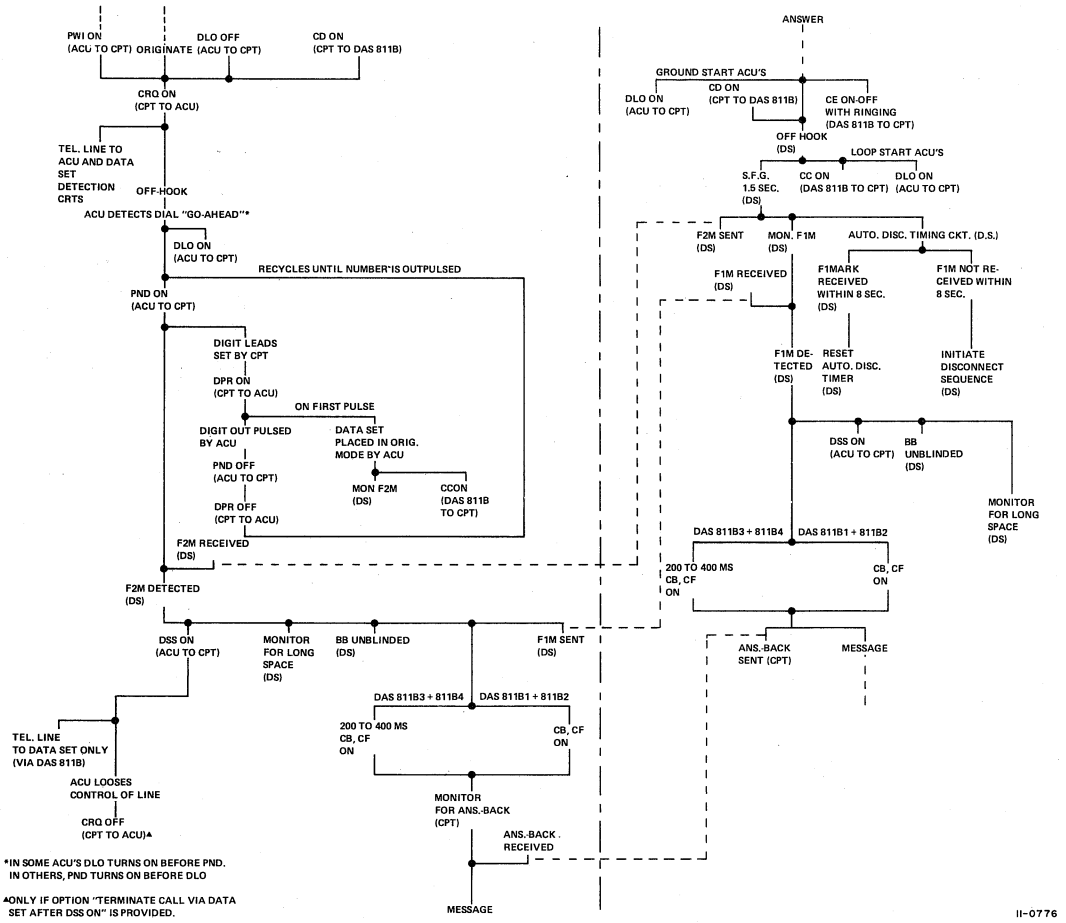


Figure C-8 811B Originating and Answering Flow Chart
for CPT for 3 or 4 Row TWX Service Data Set Tone Detection without EON

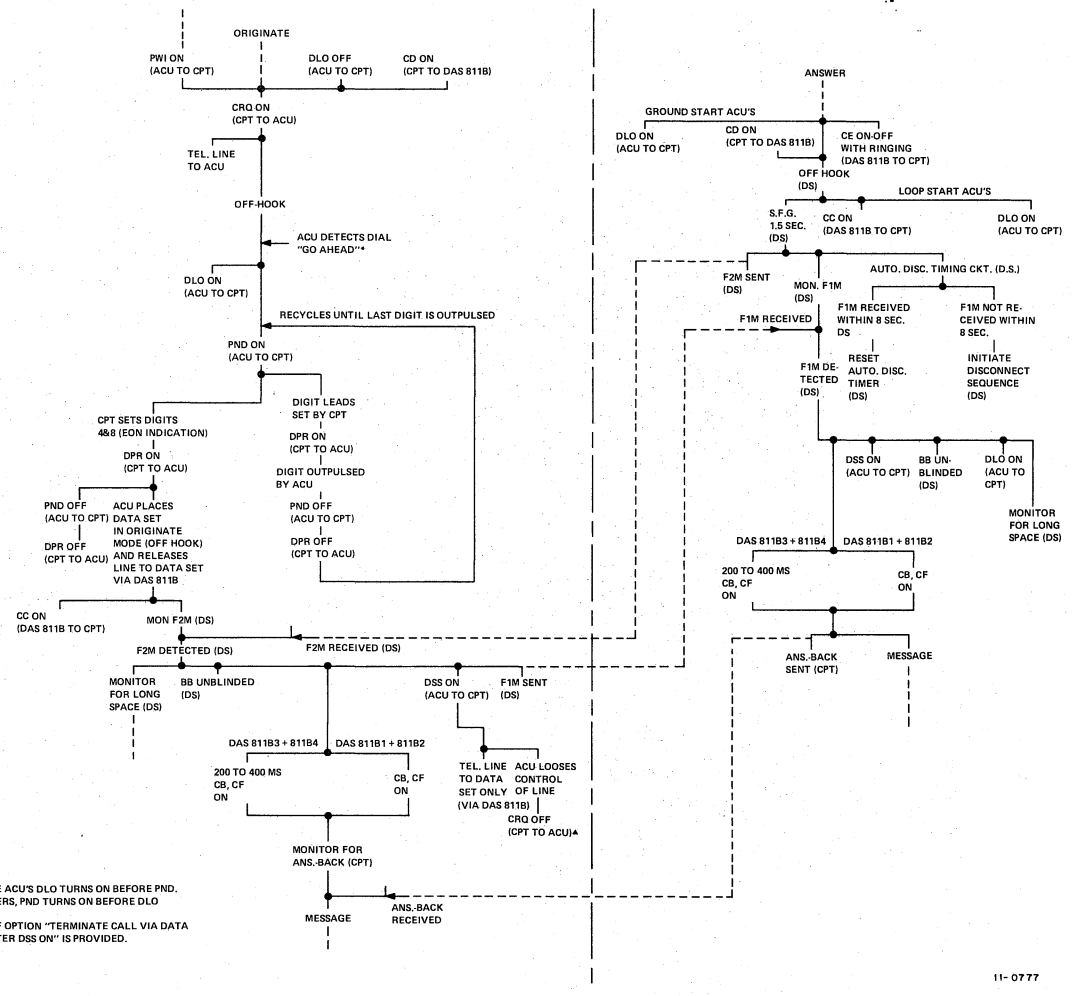


Figure C-9 811B Originating and Answering Flow Chart
for CPT for 3 or 4 Row TWX Service Data Set Tone Detection with EON

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City _____ State _____ Zip or Country _____

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