pdp11

DL11
asynchronous
line interface
engineering drawings

digital

DL11
asynchronous
line interface
engineering drawings

digital equipment corporation · maynard, massachusetts

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET ☐☐☐☐

PRINT SET #1

SEQUENCE		
DRAWING DIRECTORY		B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE		C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	(PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE		E-CS-M78ØØ-YA-1
CABLE ASSEMBLY (KL8/E)		D-IA-7008360-Ø-Ø
SOFTWARE LIST		A-SL-DL11-Ø-4
ACCESSORY LIST		A-AL-DL11-Ø-5
INSTALLATION PROCEDURE		A-SP-DL11-Ø-2

PRINT SET #2

SEQUENCE		
DRAWING DIRECTORY		B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE		C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	(PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE		E-CS-M78ØØ-Ø-1
CABLE, MODEM BCØ5C		D-UA-BCØ5C-Ø-Ø
FILTER NETWORK		B-CS-G8ØØØ-Ø-1
MODEM TEST CONN		D-CS-H315-Ø-1
SOFTWARE LIST		A-SL-DL11-Ø-4
ACCESSORY LIST		A-AL-DL11-Ø-5
INSTALLATION PROCEDURE		A-SP-DL11-Ø-2

PRINT SET #3

SEQUENCE		
DRAWING DIRECTORY		B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE		C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	(PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE		E-CS-M78ØØ-Ø-1
CABLE, MODEM BCØ5C		D-UA-BCØ5C-Ø-Ø
CABLE ASSEMBLY (KL81E)		D-IA-7008360-Ø-Ø
MODEM TEST CONN.		D-CS-H315-Ø-1
INSTALLATION PROCEDURE		A-SP-DL11-Ø-2

UNIT VARIATIONS

VAR	TITLE	PRINT SET DL11-1	PRINT SET DL11-2
DL11-A	ASYNC LINE INTERFACE, CURRENT LOOP	1	0
DL11-B	ASYNC LINE INTERFACE, EIA	0	1
DL11-C	ASYNC LINE INTERFACE, CURRENT LOOP	1	0
DL11-D	ASYNC LINE INTERFACE, EIA	0	1
DL11 E	ASYNC LINE INTERFACE, DATA SET	0	1

REVISIONS			
REV	CHG. NO.	DATE	
K	REDRAWN DL11-00009	2-76	

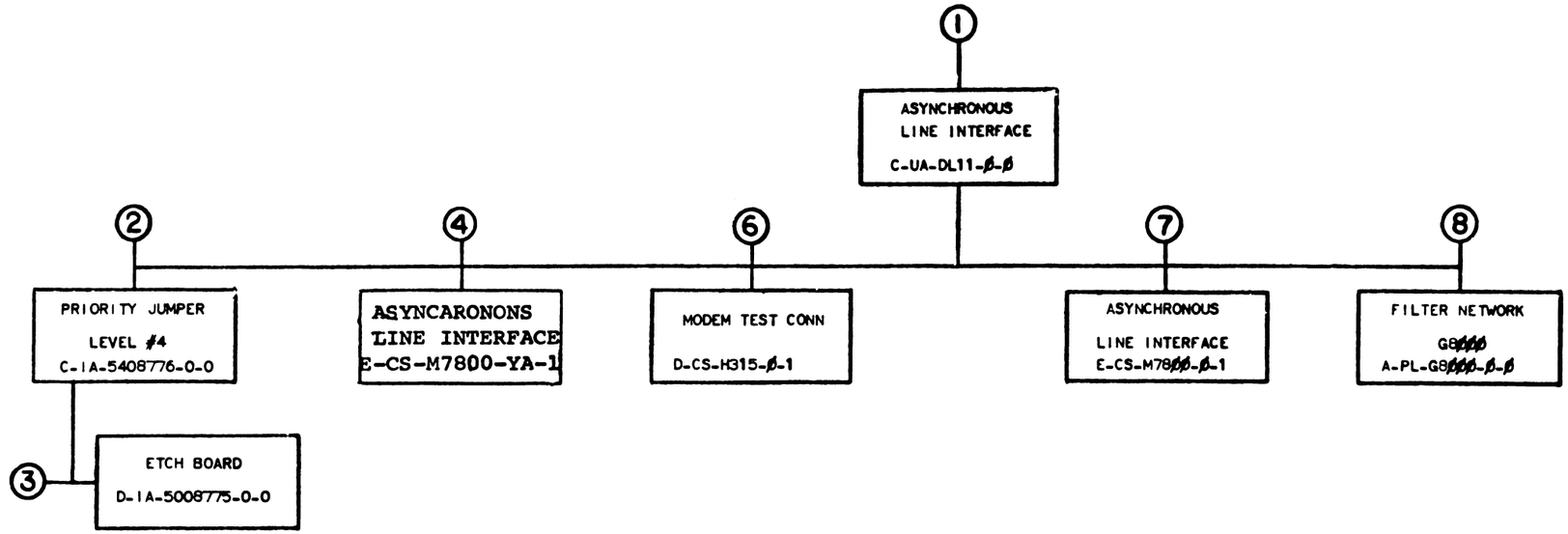
USED ON OPTION/MODEL

SHEET 1 OF 3

DRN. M. Pierce	DATE 4-28-72	TITLE: ASYNCHRONOUS LINE INTERFACE
CHK'D. R. Cook	DATE 5-9-72	
PROJ ENG. P.E.Janson	DATE 5-11-72	
PROD. J.McIntyre	DATE 5-15-72	SIZE B · CODE DD · NUMBER DL11-Ø · REV K
FIELD SERV. R. Evans	DATE 5-15-72	DIST

EN-01062-1A-1-R972-(325)

DEB 106



TITLE	SHEET	SIZE	CODE	NUMBER	REV
ASYNCHRONOUS LINE INTERFACE	2 OF 3	B	DD	DL11 - Ø	K

ELECTRICAL

CUSTOMER PRINT SET DL11-1	DL11-2	DL11-3	DEPOT SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
X	X	X		1.	C-UA-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE	
X	X	X			A-PL-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE (PL)	
	X	X			D-UA-BCØ5C-Ø-Ø	*	1	CABEE, MODEM, BCØ5C	
X		X			D-IA-7008360-0-0	#	1	CABLE, ASSEMBLY (KL8/E)	
					A-SP-DL11-Ø-1	*	11	ENGINEERING SPECIFICATION	
X	X	X			A-SP-DL11-Ø-2	F	9	INSTALLATION PROCEDURE	
					A-SP-DL11-Ø-3	B	8	TEST PRODEDURE (TEST & ACCEPTANCE)	
X	X				A-SL-DL11-Ø-4	*	1	SOFTWARE LIST	
X	X				A-AL-DL11-Ø-5	C	1	ACCESSORY LIST	
				2.	C-IA-5408776-0-0		1	PRIORITY JUMPER LEVEL #4	
					B-CS-5408776-0-1		1	CIRCUIT SCHEMATIC	
					K-CO-5408776-0-4		1	X-Y COORDINATE HOLE LOC	
					B-MH-5408776-0-6		1	MODULE ECO HISTORY	
				3.	C-AH-5408776-0-5		1	ASSY/DRILLING HOLE LAYOUT	
X				4	E-CS-M7800-YA-1	#	6	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M7800-YA-4		1	X-Y COORDINATE HOLE LOCATION	
					D-AH-M7800-YA-5		1	ASSY DRILLING HOLE LAYOUT	
					B-MH-M7800-YA-6		1	MODULE ECO HISTORY	
	X	X		6.	D-CS-H315-Ø-1	#	1	MODEM TEST CONN	
					K-CO-H315-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-H315-Ø-5		1	ASSY DRILLING HOLE LAYOUT	
					B-MH-H315-Ø-6		1	MODULE ECO HISTORY	
X	X	X		7.	E-CS-M7800-Ø-1	#	7	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M7800-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-M7800-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-M7800-Ø-6		1	MODULE ECO HISTORY	
	X			8.	A-PL-G8000-Ø-Ø		1	FILTER NETWORK	
					B-CS-G8000-Ø-1	#	1	CIRCUIT SCHEMATIC	
					K-CO-G8000-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-G8000-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-G8000-Ø-6		1	MODULE ECO HISTORY	

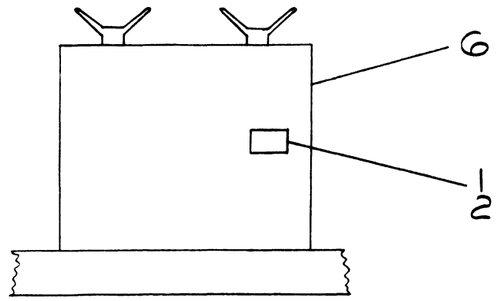
MECHANICAL

CUSTOMER PRINT SET DL11-1	DL11-2	DL11-3	DEPOT SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
				1.	C-UA-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE	
					A-PL-DL11-Ø-Ø	F	1	ASYNCHRONOUS LINE INTERFACE (PL)	
					D-UA-BCØ5C-Ø-Ø		1	CABLE, MODEM BCØ5C	
					D-IA-7008360-0-0		1	CABLE ASSEMBLY (KL8/E)	
				2.	C-IA-5408776-0-0		1	PRIORITY JUMPER LEVEL #4	
					K-CO-5408776-0-4		1	X-Y COORDINATE HOLE LOC	
					B-MH-5408776-0-6		1	ASSY/DRILLING HOLE LAYOUT	
				3.	D-IA-5008775-0-0		1	ETCH BOARD	
					C-AH-5408776-0-5		1	ASSY/DRILLING HOLE LAYOUT	
				6.	D-CS-H315-Ø-1		1	MODEM TEST CONN	
					K-CO-H315-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-H315-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-H315-Ø-6		1	MODULE ECO HISTORY	
				7.	E-CS-M7800-Ø-1		7	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M7800-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-M7800-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-M7800-Ø-6		1	MODULE ECO HISTORY	
				8.	A-PL-G8000-Ø-Ø		1	FILTER NETWORK	
					K-CO-G8000-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-G8000-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-G8000-Ø-6		1	MODULE ECO HISTORY	

TITLE	SHEET	SIZE	CODE	NUMBER	REV
ASYNCHRONOUS LINE INTERFACE	3 OF 3	B	DD	DL11-Ø	K

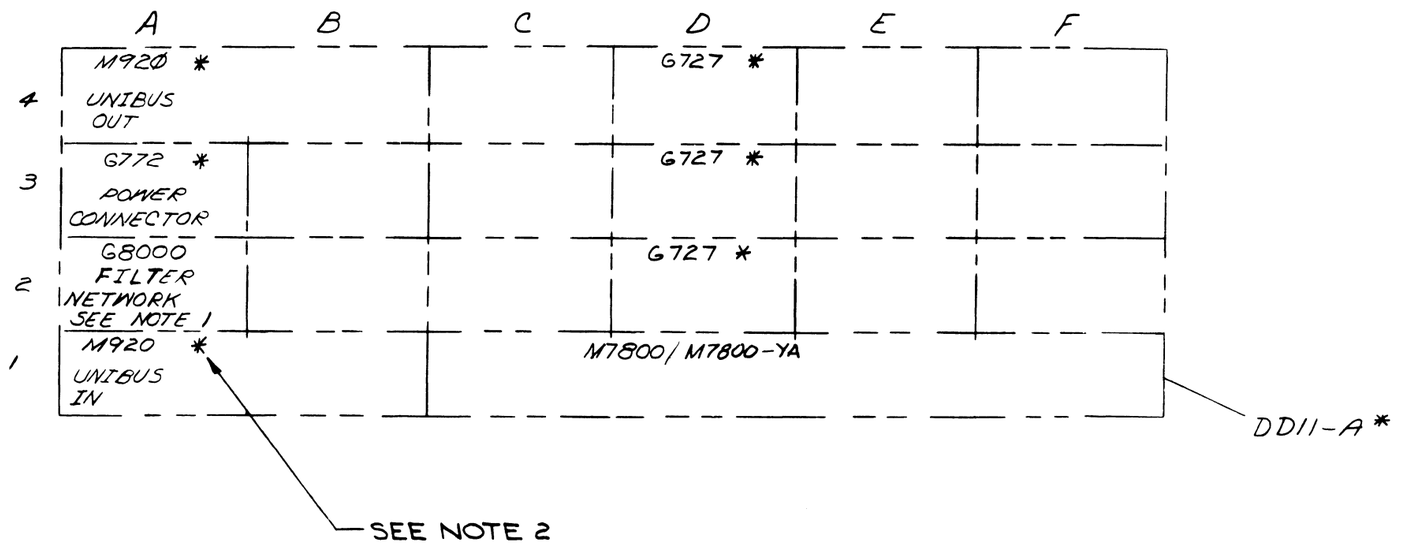
DRB 108

DEC 16-(325)-1062-2-N871



NOTES:

1. G 8000 IS REQUIRED ONLY IN PDP 11 SYSTEMS WHERE +15V IS NOT AVAILABLE. THE INSTALATION REQUIRES 2 WIRES TO BE ADDED.
   A03V2 - A02V2
   A02N2 - CXXU1
   WHERE (XX) IS THE SLOT NUMBER CONTAINING THE DL 11.
2. ITEMS INDICATED WITH ASTERICK (*) ARE SHOWN FOR REFERENCE ONLY AND ARE NOT PART OF THIS UNIT.



REVISIONS																								
CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.
	DL11-00001	A		DL11-00002	B		DL11-00003	C		DL11-00005	C		DL11-00006	D		DL11-00008	E		DL11-00009	F					
	R JANSON 2-18-72			R JANSON 7-17-72			JANSON 12-5-72			P.E. Jansen 12-5-72			L. CONDON 7-31-73			L. CONDON 9-21-73			L. CONDON 11-2-73			J. MCINTYRE 12-FEB 76		

FIRST USED ON OPTION/MODEL: PDP-11	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —

FINISH —

DRN. M Price	DATE 7/18/72	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D. J Fenerson	DATE 9-29-72	
ENG. P E Jansen	DATE 5-11-72	TITLE: ASYNCHRONOUS LINE INTERFACE
PROJ ENG. P E Jansen	DATE 5-11-72	
PROD. J McIntyre	DATE 5-15-72	
NEXT HIGHER ASSY. B-DD-DL11-0		SIZE C · CODE UA · NUMBER DLH-[redacted] · REV. F
SCALE NONE		
SHEET 1 OF 1		DIST. G

NUMBER DL11-0-0 · REV. E · SIZE C · CODE UA

DEC FORM NO. DRC 100-A

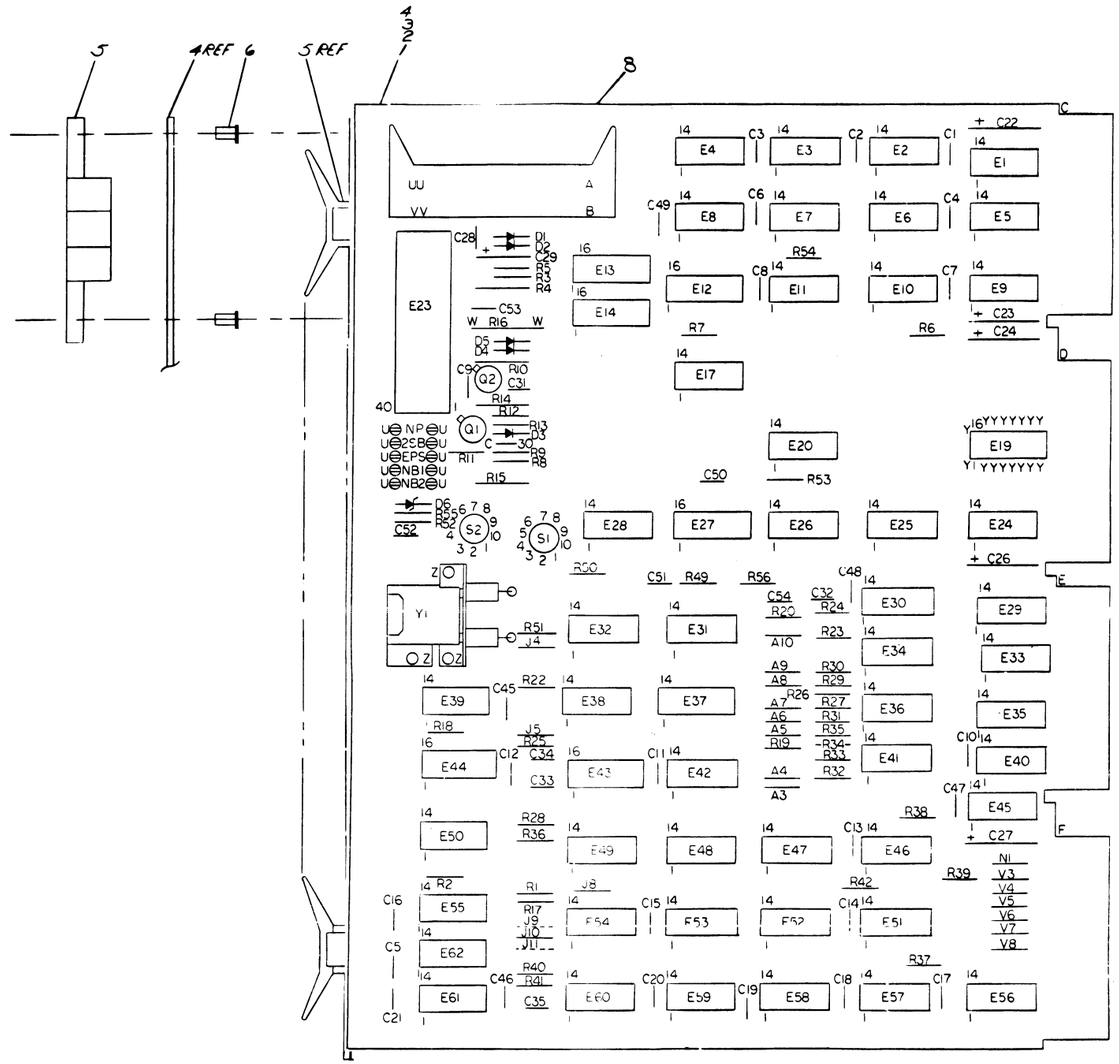
DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

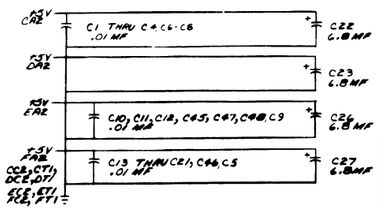
PARTS LIST

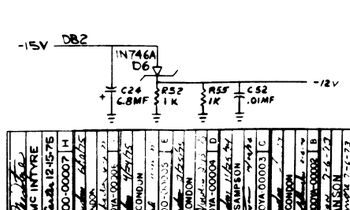
MADE BY M. PIERCE DATE 4/27/72	CHECKED J. FERGUSON DATE 4/27/72	SECTION 1
ENG P. E. JANSON DATE 5/11/72	PROD J. McIntyre DATE 5/15/72	ISSUED SECT. 1

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION DL11-A	DL11-B	DL11-C	DL11-D	DL11-E
1	C-IA-5408776-0-0	PRIORITY JUMPER LEVEL #4	1	1	1	1	1
3	D-UA-BCØ5C-25	CABLE MODEM BCØ5C	-	1	-	1	1
4	D-IA-7008360-0-0	CABLE ASSEMBLY (KL8E)	1	-	1	-	-
5	D-CS-H315-Ø-1	MODEM TEST CONNECTOR	-	-	-	-	A/R See Note 2
6	E-CS-M7800-Ø-1	ASYNCHRONOUS LINE INTERFACE	-	1	-	1	1
7	~~A-PL-G8000-Ø-Ø~~	~~FILTER NETWORK~~	~~-~~	~~A/R~~	~~-~~	~~A/R~~	~~A/R See Note 1~~
8		CRYSTAL	A/R	A/R	A/R	A/R	A/R See Note 3
9	E-CS-M7800-YA-1	ASYNCHRONOUS LINE INTERFACE	1	-	1	-	-
10	9008269	TRANSPARENT VINYL TAPE	A/R				
	NOTES:						
	1. G8000 IS REQUIRED	ONLY IN PDP11 SYSTEMS WHERE +15V IS NOT					
	AVAILABLE. ONE PER DD11-A						
	2. ONE H315 PER PDP11	SYSTEM					
	3. CRYSTAL FREQUENCY	DEFINED BY CUSTOMER SPECIFIED BAUD RATE					
	OR BY THE DOCUMENTATION OF AN OPTION WHICH USES THE DL11.						
	4. APPLY TAPE TO TOP	SURFACES OF CRYSTAL AND MOUNTING					
	BRACKETS TO INSULATE FROM ADJACENT MODULES.						
	5. PRIORIY LEVELS 5.6, or 7 MAY BE SPECIFIED BY THE CUSTOMER						
	OR THE DOCUMENTATION OF AN OPTION WHICH USES THE DL11.						

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø	A	PL	DL11-Ø-Ø	F	DL11-00009
	SHEET 1 OF 1	DIST.				







NOTES:

1.) PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.

2.) JUMPERS TO BE USED AT CONNECTIONS A3-A10, J4-J6, J8-J10, V3-V8, AND N1.

3.) LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (Z).

4.) DEC 8640S WERE PHASED IN AS 380 REPLACEMENTS ANY 380 FAILURES SHOULD BE REPLACED BY 8640S, EXCEPT E28. E28 MUST BE REPLACED WITH A 7380 CHIP.

PIN NOMENCLATURE

MODULE	SYSTEM UNIT
A	C
B	D
C	E
D	F

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	E28	IC DEC 7380	1910390	69
A/R		INSULATION TUBING	91 7256-11	68
1	R3	RES 750Ω 1/4W 5%	1301401	67
1	R38	RES 390 Ω 1/4 W, 5%	1300309	66
1	D6	DIODE 1N746A	1104860	65
2	Q1, Q2	TRANSISTOR 6534D	1503409-00	64
1	C53	CAP 100PF 100V 5% DIPPED MICA	1000016	63
1	C54	CAP 560PF 100V 5% DIPPED MICA	1000025	62
2	C50, C51	CAP .047MF CERAMIC	1009678	61
1	E27	IC DEC 74161	1910650	60
2	C34, C35	CAP 330PF 100V 5% DIPPED MICA	1000023	59
1	C32	CAP 470PF 100V 5% DIPPED MICA	1000024	58
1	C31	CAP 1000PF 100V 5% DIPPED MICA	1000042	57
29	C1-C21, C29, C30, C45-C49, C52	CAP .01UF 100V 20% CERAMIC DISC	1001610	56
1	C29	CAP .47UF 35V 10% TANT	1005965	55
5	C22-C24, C26, C27	CAP 6.8 UF 35V 20% TANT	1000067	54
1	C33	CAP 150PF 100V 5% DIPPED MICA	1000019	53
2	R14, R15	RES 1.5K 1/2W 5%	1300394	52
5	R23, R26, R40, R52, R55	RES 1K 1/4W 5%	1300365	51
1	R41	RES 47Ω 1/4W 5%	1300202	50
1	R10	RES 68 Ω 1/2W 10%	1300220	49
1	R5	RES 82 Ω 1/4W 5%	1301477	48
1	R24	RES 100Ω 1/4W 5%	1300229	47
1	R11	RES 150Ω 1/4W 5%	1300230	46
2	R42, R57	RES 180Ω 1/4W 5%	1301322	45
1	R53	RES 220Ω 1/4W 5%	1300271	44
5	D1-D5	DIODE D664 20V 100mA	1100114	43
3	R9, R13, R51	RES 470Ω 1/4W 5%	1300316	42
1	R4	RES 560Ω 1/2W 5%	1300338	41
3		NUT HEX #2-56	9006555	40
1	R16	RES 750Ω 1W 5%	1302385	39
26	R1, R2, R6, R7, R17-R21, R25, R27-R37, R39, R47, R50, R52, R54, R56	RES 10K 1/4W 5%	1300479	38
2	R8, R12	RES 1.5K 1/4W 5%	1300391	37
1	E23	IC DEC UART	1910459	36
4	E32, E55, E61, E62	IC DEC 7474	1905547	35
2	E36, E41	IC DEC 8242	1909712	34
3	E31, E49, E59	IC DEC 7408	1910155	33
3		SCR PHIL HD PAN #2-56 × 25/16	9006001-1	32
2	E20, E26	IC DEC 7490	1909037	31
11	E1, E2, E5, E7-E9, E11, E30, E47, E54, E56	IC DEC 8881	1909705	30
2		AUGAT 8000 PG-1	1202812	29
1	E43	IC DEC 74123	1910436	28
3	E48, E57, E52	IC DEC 74H74	1909667	27
3	E42, E54, E58	IC DEC 7400	1903575	26
1	E10	IC DEC 7413	1909989	25
2	E50, E53	IC DEC 7402	1909004	24
7	E3, E4, E33, E35, E40, E45, E46	IC DEC	19.1469	23
1	E12	IC DEC 74153	1909937	22
1	E60	IC DEC 74H04	1909931	21
1	E25	IC DEC 7492	1909053	20
4	E6, E17, E38, E39	IC DEC 7404	1909686	19
1	E24	IC DEC 7493	1909054	18
1	E34	IC DEC 7410	1903576	17
1	E29	IC DEC 314	1909704	16
1	E37	IC DEC 7442	1910046	15
1	E44	IC DEC 8271	1909615	14
2	E13, E14	IC DEC 74175	1910651	13
1		BRACKET, CRYSTAL HOLDER	5302825	12
1		BRACKET, CRYSTAL HOLDER	5302154	11
1	E19	IC SOCKET	1209938	10
2	S1, S2	SWITCH, SINGLE POLE, 10 POS	1210012-1	9
1		40 PIN CONNECTOR BERG	1209941	8
10		SPLIT LUGS	9006735	7
8		EYELET #554-7 E.B. STIMPSON	9006732	6
4		HANDLE, FLIP-CHIP, MAGENTA	9008337-06	5
1		ETCHED CIRCUIT BOARD	5009778	4
REF		MODULE ECO HISTORY	[illegible]	3
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7800-YA-5	2
REF		X-Y COORDINATE HOLE	K-CO-M7800-YA-5	1

PARTS LIST

ETCH BOARD REV H

IC TYPE	GND	+5V	+V	-12V
DEC 74161	8	16	—	—
DEC UART	3	1	—	2
DEC 74175	8	16	—	—
DEC 8271	8	16	—	—
DEC 7442	8	16	—	—
DEC 314	1	8	—	—
DEC 7493	10	5	—	—
DEC 7492	10	5	—	—
DEC 74153	8	16	—	—
DEC 8640	1	8	—	—
DEC 7490	10	5	—	—
DEC 74123	8	16	—	—

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

DEC FORM NO. DRE 104

DEC NO.	EIA NO.
6534D	MPS6534
1N746A	1N4M3.3AZ
D664	1N3606

SEMICONDUCTOR CONVERSION CHART

REV	CHANGE NO.	CHK		
H	M7800-00007		JOHN MC INTYRE	12-15-75
	M7800YA-00006		L. CONDON	
E	M7800-00005		L. CONDON	
D	M7800YA-00004		B. SAMPSON	
C	M7800YA-00003		L. CONDON	
B	M7800YA-00002		P. JANSON	7-6-73
A	M7800-00001 ORIGINATED			

EQUIPMENT CORPORATION

TITLE
ASYNCHRONOUS
LINE INTERFACE

NEXT HIGHER ASSY
SCALE
SHEET 1 OF 6

E CS M7800-YA-1 REV. H

CS M7800-YA-1

DL-2 BINIT H
BUS INIT L
DL-2 BINIT L

E45 74S64 E59

E03 DL-2 BD07 H → DL-4 RD7 H → 8881 E07 → BUS D07 L
E02 DL-2 BD06 H → DL-4 RD6 H → 8881 E07 → BUS D06 L
E04 DL-2 BD05 H → DL-4 RD5 H → 8881 E08 → BUS D05 L
E04 DL-2 BD04 H → DL-4 RD4 H → 8881 E08 → BUS D04 L
E03 DL-2 BD03 H → DL-4 RD3 H → 8881 E08 → BUS D03 L
E03 DL-2 BD02 H → DL-4 RD2 H → 8881 E08 → BUS D02 L
E04 DL-2 BD01 H → DL-4 RD1 H → 8881 E07 → BUS D01 L
E04 DL-2 BD00 H → DL-4 RD0 H → 8881 E07 → BUS D00 L
DL-5 RBUF TO BUS H → 8881 E07

DL-4 XMIT READY H → 8881 E11 → CM2 → BUS D07 L
DL-4 XMIT INT ENB (1)H → 8881 E11 → CV2 → BUS D06 L
DL-4 MAINT (1)H → 8881 E11 → CP2 → BUS D05 L
DL-4 BREAK (1)H → 8881 E11 → CN2 → BUS D04 L
DL-5 XCSR TO BUS H → 8881 E11

DL-4 RCVR DONE H → 8881 E09 → CM2 → BUS D07 L
DL-4 RCVR INT ENB (1)H → 8881 E09 → CV2 → BUS D06 L
DL-4 DATASET INT ENB (1)H → 8881 E09 → CP2 → BUS D05 L
DL-4 SEC XMIT (1)H (N) → 8881 E09 → CT2 → BUS D03 L
DL-4 REQ TO SEND (1)H (M) → 8881 E09 → CV2 → BUS D02 L
DL-4 DATA TERMINAL READY (1)H (F) → 8881 E09 → CR2 → BUS D01 L
CS2 → BUS D00 L

+5V R1 10K J8 DL-5 RBUF TO BUS L → 74S03 E53

DL 4 OR ERR H → 74S04 E06 → 74S13 E10 → 8881 E02 → ERROR H
DL 4 FR ERR H → 74S04 E06 → 74S04 E06 → 8881 E02
DL 4 P ERR H → 74S04 E06 → 74S04 E06 → 8881 E02

+5V R2 10K J7 DL-5 RCSR TO BUS L → 74S02 E58

DL-5 RCSR TO BUS H
DL-4 RCVR BUSY (1)H

8881 E01 → CD2 → BUS D15 L
8881 E01 → CE2 → BUS D14 L
8881 E01 → CF2 → BUS D13 L
8881 E05 → CH2 → BUS D12 L
8881 E01 → CH1 → BUS D11 L
8881 E05 → CJ2 → BUS D10 L

REVISIONS		
CHK.	ECO NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DL11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: XXX = .005, XX = .02, X = .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRAN. — DATE 10/72
CHK'D. — DATE
ENG. — DATE 11/72
PROGRAM. — DATE 11/6/72
PROD. — DATE 11/6/72
NEXT HIGHER ASSY. —
SCALE —
SHEET 2 OF 6

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE ASYNCHRONOUS LINE INTERFACE (BUS RECEIVERS & DRIVERS) DL-2

SIZE	CODE	NUMBER	REV.
D	CS	M7800-YA-1	H

DIST.

SEE NOTE 3

Y1		844.8 KHZ		1.0368 MHZ		1.152 MHZ		4.608 MHZ	
		BAUD	USEC	BAUD	USEC	BAUD	USEC	BAUD	USEC
SWITCH POS.	1	36.7	1700	44.8	1342	50	1250	200	312
	2	55	1135	67.3	928	75	833	300	208
	3	110	567	134.5	464	150	417	600	104
	4	220	284	269	232	300	208	1200	52
	5	440	142	538	116	600	104	2400	26
	6	880	71	1076	58	1200	52	4800	13
	7	1320	47.4	1614	38.7	1800	34.6	7200	8.7
	8	1760	35.5	2152	29	2400	26	9600	6.5
	9	BERG CLOCK INPUT - COMMON TO RCVR AND XMIT							
	10	EXTERNAL CLOCK INPUT - RCVR: DSI; XMIT: DRI							

PRIORITY PLUG E19

DL-3 BG IN H	DJ2	#1 / #2	18	DD2 BUS BR7 L
DL-6 BG OUT H	DV2	#3	15	DC2 BUS BR6 L
BUS BG4 OUT H	DT2	#4	14	DF2 BUS BR5 L
BUS BG4 IN H	DS2	#5	13	DH2 BUS BR4 L
BUS BG5 OUT H	DR2	#6	12	DJ2 DL-6 REQUEST L
BUS BG5 IN H	DP2	#7	11	DK2 BUS BR7 IN H
BUS BG6 OUT H	DN2	#8	10	DL2 BUS BR7 OUT H
			09	DM2 BUS BR6 IN H

R49 10K; R50 10K; C50 .047 UFD; C51 .047 UFD; Y1; R51 470; E28; E26

20 MA RECEIVE (K) (S); R3 750; R5 82; C28 .01 UFD; C29 .01 UFD; C45 .01 UFD; R4 *60 -15V; D1 D664; D2 D664; (H) TO HDFR/ INTERLOCK

74153 E12; BERG CLOCK INPUT (CC); BERG SERIAL IN L (F); TTL SERIAL IN L; R1 10K; R2 10K; 7413 E10; DL-4 MAINT (TH); BERG CLK ENB L (HH); R44 10K; DL-4 SERIAL OUT H; F1 09 FRI DL-3 RCLK H; 10 07 FSI DL-3 SI H

7490 E26; 7493 E25; 7493 E24; 74161 E27; 7380 E28; R56 10K

DR1 EXT XMIT INPUT; DL-3 XMIT CLK H; (CC) BERG CLOCK INPUT; DSI EXT RCVR INPUT; DL-3 RCVR CLK H; S1 T; S2 R

DB1 TTL RDR ENB L; DL-4 RDR ENB (I) H; 7404 E17; R8 1.5K; R9 470; R11 150; Q1 6534D; D3 D664; C38 .01 UFD; READER RELAY; (PP); R10 68Ω; -15V; (EE)

(BB); DC1 TTL SERIAL OUT L; R12 1.5K; R13 470; C31 1000 pF; C53 100 pF; Q2 6534D; D4 D664; D5 D664; R14 1.5K; R15 1.5K; 20 MA TRANSMIT; R16 750; (AA); (KK); -15V

(TT); (VV); (UU)

NOTES:
1. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X)
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE 7008360 CABLE. THIS CABLE ALSO CONNECTS BERG PINS H TO E.
4. WITH HIGH THE ABOVE TABLE INDICATES NOT THE STANDARD SETTING. THE OTHER VALUES MAY BE SPECIFIED BY THE CUSTOMER BY OTHER DOCUMENTATION IF THE CUSTOMER WANTS THE SETTING.

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL: DLII	QTY.	DESCRIPTION	PART NO.
		PARTS LIST	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES: DECIMALS XXX ± .005, .XX ± .02, X ± 1; ANGLES ± 0° 30'	DRN.	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
	CHK'D.	DATE	TITLE: ASYNCHRONOUS LINE INTERFACE (CLOCK & CURRENT LOOPS) DL-3
	ENG.	DATE	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	PROJ. ENG.	DATE	
	PROG.	DATE	
MATERIAL	NEXT HIGHER ASSY.		SIZE: D; CODE: CS; NUMBER: M7800-YA-1; REV.: H
FINISH	SCALE		
	SHEET 3 OF 6		DIST.

DL-2 BINIT L

DL-5 SEL 2 L — 7408 E31

UART E20
CLR R DONE, STB STATUS, STB RD, R CLK, SERIAL IN
DL-2 BDØ7 H, DL-2 BDØ6 H, DL-2 BDØ5 H, DL-2 BDØ4 H, DL-2 BDØ3 H, DL-2 BDØ2 H, DL-2 BDØ1 H, DL-2 BDØØ H
DL-5 LD XD L, X CLK H
R DONE, OR ERR, FR ERR, P ERR, RD7, RD6, RD5, RD4, RD3, RD2, RD1, RDØ
DL-4 OR ERR H, DL-4 FR ERR H, DL-4 P ERR H, DL-4 RD7 H, DL-4 RD6 H, DL-4 RD5 H, DL-4 RD4 H, DL-4 RD3 H, DL-4 RD2 H, DL-4 RD1 H, DL-4 RDØ H
SERIAL OUT, XRDY, EOC
CLR LDC NB2 NB1 NP EPS 288

7474 E62 — DL-4 RCVR DONE H

7474 E53 — DL-4 RCVR BUSY (1)H

7402 E50 — DL-2 BINIT H

8271 E44 — CLR LD CLK DS — FSI DL-3 SI H

7474 E53 — DL-3 RCLK H FRI

7474 E61 — DL-4 SERIAL OUT H

7474 E17 — R53 220Ø — C54 560PF

7474 E20 — SET 9, CLR, CLKBC CLKØ — DL 3 XMIT CLK H

DL-2 BDØ2 H, DL-2 BDØØ H, DL-2 BDØ8 H — 74175 E14 — DL-4 MAINT (1)H, DL-4 BREAK (Ø)H, DL-4 XMIT INT ENB (1)H — CLR CLK — DL-5 BUS TO XCSR H

DL-4 BREAK (1)H — +5V R18 10K — J5

DL-4 XMIT READY H — 7408 E31 — DL-4 XMIT INT H

DL-4 RCVR DONE H — 7408 E42 — +5V R19 10K — J6 — DL-4 RCVR INT H

DL-2 BDØ5 H, DL-2 BDØ2 H, DL-2 BDØ6 H, DL-2 BDØ3 H — 74175 E13 — DL-4 DATASET INT ENB (1)H, DL-4 REQ TO SEND (Ø)H, DL-4 RCVR INT ENB (1)H, DL-4 SEC XMIT (Ø)H — CLR CLK — DL-4 REQ TO SEND (1)H — J3 — CMI — +5V 220 10K — CK1 DL-4 SEC XMIT (1)H

DL-4 DATA LEADS ONLY L — J4

DL-2 BDØ1 H — DTA 7474 E32 — DL-4 DATA TERMINAL READY (1)H, DL-4 DATA TERMINAL READY (Ø)H — CFI — +5V R22 10K

DL-2 BDØØ H — RDR ENB 7474 E32 — DL-4 RDR ENB (1)H — DL-5 BUS TO RCSR H

J9, J11, J10

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL: DL11	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL — FINISH

DRN — DATE — CHK'D — DATE — ENG. — DATE — MFG. — DATE — MGR — DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: ASYNCHRONOUS LINE INTERFACE (UART & STATUS) DL-4

NEXT HIGHER ASSY. — SCALE — SHEET 4 OF 6

SIZE: D — CODE: CS — NUMBER: M7800-YA-1 — REV: H — ENGT.

BUS A11 L EL1 #4
BUS A13 L EK2 #5
BUS A14 L EK1 #9
BUS A15 L ED2 #9
BUS A16 L EC2 10
BUS A17 L ED1 11
BUS A12 L EC1 12
314 E29 #3

BUS MSYN L EE1 12 — E33 13

7418 E34 #9, 10, 11 — 8

#5 — 7404 E39 — #4 — +5V R23 1K — R24 680 — #2 — #3 — C32 470 pf — #1 — EJ1 BUS MSYN L

#9 — 7404 E39 — #8 — EL2 REG SEL H

+5V R26 1K

A10 — R27 10K — #5, #6 — 8242 E36 — #4
A9 — R29 10K — #1, #2 — 8242 E36 — #3
A8 — R30 10K — #9, #8 — 8242 E36 — 10
A7 — R31 10K — 12, 13 — 8242 E36 — 11
A6 — R32 10K — #5, #6 — 8242 E41 — #4
A5 — R33 10K — #1, #2 — 8242 E41 — #0
A4 — R34 10K — 12, 13 — 8242 E41 — 11
A3 — R35 10K — #8, #9 — 8242 E41 — 10

BUS A10 L EP1 — E40 — 13
BUS A09 L ER1 — 10 — E40 — 14
BUS A08 L EN2 — #7 — E35 — #2
BUS A07 L EP2 — #4 — E35 — #3
BUS A06 L EU1 — E45 — 13
BUS A05 L EV1 — 10 — E45 — 14
BUS A04 L EU2 — #7 — E48 — #2
BUS A03 L EV2 — #4 — E48 — #3
BUS A01 L EH1 — #4 — E33 — #3
BUS A02 L EF1 — 10 — E33 — 14
BUS A00 L EH2 — 11 — E35 — 13
BUS C1 L EF2 — #7 — E33 — #2
BUS C0 L EJ2 — 10 — E35 — 14

#0 — 7418 E34 — #6
#1, #2 — 7418 E34 — 12 — 12
13 — D3
14 — D2
15 — D1
D0

7442 E37: f9 11, f8 10, f7 #9, f6 #7, f5 #6, f4 #5, f3 #4, f2 #3, f1 #2, f0 #1

#9 — 7404 E39 — #4 — DL-5 BUS TO XCSR H
#5 — 7404 E39 — #6 — DL-5 BUS TO RCSR H
#1 — 7404 E38 — #2 — DL-5 XCSR TO BUS H
#3 — 7404 E38 — #4 — DL-5 RBUF TO BUS H
#5 — 7404 E38 — #6 — DL-5 RCSR TO BUS H

#9 — 10 — +5V R25 10K — C33 150 pf — 5000 ns — #7, #8 — 74123 E43 — 1, 12, 13, #5, #0, 12 — EBL DL 5 LD XD L
+5V R28 10K

DL-5 BUS TO XBUF L

NOTE 1: THE 'A LINES ARE TO BE JUMPERED FOR A 0.

DL 5 RBUF TO BUS L

#1 — #2 — 74123 E43 — 13, #4, 14, 15, 13, #4, #0 — DL 5 SEL 2 L
C34 330 pf — 1000 ns — +5V R36 10K

DL 5 BUS TO RBUF L
DL-5 RCSR TO BUS L

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	FIND NO.
DL11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS/ SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRAW — DATE
CHKD — DATE
ENG — DATE
PROJ. ENG. — DATE
PROD. — DATE
NEXT HIGHER ASSY. —
SCALE —
SHEET 5 OF 6

[redacted] EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (ADDRESS SELECTION) DL-5

CODE	NUMBER	REV.
DICS	M7800-YA-1	H

DIST.

DL-4 RCVR INT H FV1

DL-4 XMIT INT H FV1

DL-3 BG IN H FB1

BUS NPR L FJ1

BUS BBSY L FD1

BUS SSYN L FC1

FP1 DL-6 REQUEST L

FR1 DL-6 BR OUT H

FT2 BUS BACK L

FC2 BUS D@2 L

FL1 BUS D@3 L

FN2 BUS D@4 L

FF1 BUS D@5 L

FM1 BUS INTR L

FF2 BUS D@6 L

FM1 BUS D@7 L

FK1 BUS D@8 L

NOTE: THE 'V' LINES ARE TO BE JUMPERED FOR A 1.

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	FIND NO.
DL11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005	±0° 30'
.XX = .02	
.X = .1	

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL

FINISH

	NAME	DATE
DRAWN		
CHECKED		
ENGR		
PROJ. ENGR		
PROD.		

NEXT HIGHER ASSY.

SCALE

SHEET 6 OF 6

EQUIPMENT CORPORATION

TITLE: ASYNCHRONOUS LINE INTERFACE (INTERRUPT CONTROL) DL-6

SIZE	CODE	NUMBER	REV.
D	CS	M7800-YA-1	H

DIST.

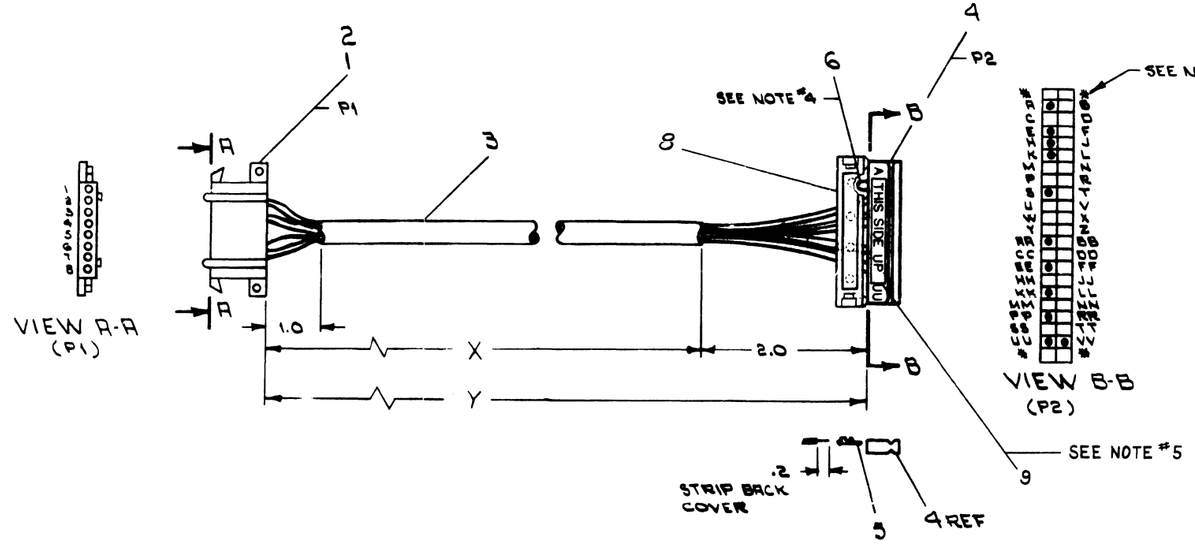
WIRE TABLE

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	PAIR NO.	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH
3	22	BLK	1	P1-2	2	P2-KK	5
3		RED		P1-3	2	P2-S	
3,7		SHIELD		SEE NOTE #2	—	P2-A(NOTE #3)	
3		BLK	2	P1-4	2	P2-EE	
3		WHT		P1-5	2	P2-RR	
3,7		SHIELD		SEE NOTE #2	—	P2-UU(NOTE #3)	
3		BLK	3	P1-6	2	P2-PP	
3		GRN		P1-7	2	P2-K	
3,7		SHIELD		SEE NOTE #2	—	P2-VV(NOTE #3)	
6	22	BLK	—	P2-E	5	P2-H	5

LEGEND

VARIATION	LENGTH X	LENGTH Y
7008360-0	25IN±1.0	27IN±1.0
7008360-1	46IN±1.0	48IN±1.0

NOTES:
1. * ASTERISKS INDICATE CAVITIES NOT USED OR DESIGNATED BY LETTERS.
2. DRAIN WIRES TO BE CUT BACK TO OUTER INSULATION ON P1 END OF CABLE ONLY. SHIELDS TO BE CUT BACK TO OUTER INSULATION ON BOTH ENDS OF CABLES.
3. DRAIN WIRES ON P2 END OF CABLE TO BE EACH ENCLOSED WITH ITEM #7 (TUBING) FROM END OF CABLE JACKET TO POINT WHERE THEY ENTER P2 CONNECTOR.
4. ITEM #6 (WIRE) TO BE APPROXIMATELY ONE(1) INCH LONG.
5. PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #4 (BERG HOUSING) AS SHOWN.



QTY	DESCRIPTION	PART NO.	ITEM NO.
	LABEL, THIS SIDE UP	3611567	9
	TRAIN WIRE	12 1106	8
A/R	TUB. #18 TEF. THINWALL WHT	9107278-11	7
A/R	WIRE #22 AWG STRD TEF BLK	9107350-00	6
11	SOCKET, CRIMP # 7216	12100889-07	5
1	HOUSING, BERG #3043-115	1210919-15	4
A/R	CABLE, BELDEN #8777-3PR SHLD	9107725-0	3
6	CONTACT MATE-N-LOCK (FEMALE)	12099879-03	2
1	CONN. MATE-N-LOCK (FEMALE)	12098340-00	1

PARTS LIST

REVISIONS REV.	CHANGE NO.	
A	00008	7/16/71
B	00008	7/16/71
C	00008	7/16/71
D	7008360-00002	3-17-72
E	7008360-00003	3/21/74
F	BG95M-00001	10/2/74

DRAWN R. REGAN 10-28-71
TRACED R. REGAN 9-30-74
CHECKED R. REGAN 10/2/74
ENG APPROVED M.E. LEWANDOWSKI 10/2/74
PROJ ENG APPROVED M.E. LEWANDOWSKI 10/2/74
PROD APPROVED M.E. LEWANDOWSKI 10/2/74

FIRST USED ON OPTION / MODEL: PDP-8E

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES .XX ±.02 .XXX ±.010 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL: SEE PARTS LIST
FINISH

DRN. [illegible] DATE 7/16/71
CHK'D [illegible] DATE 7-8-71
ENG [illegible] DATE 7-9-71
PROJ ENG [illegible] DATE 7-12-71
PROD [illegible] DATE 7/14/71
NEXT HIGHER ASSY: A ML-KL8-E-0
SCALE: NONE
SHEET OF

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: CABLE ASSEMBLY (KL8E)

SIZE D | CODE DIA | NUMBER 7008360-0-0 | REV F
DIST.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

SOFTWARE LIST

MADE BY EMPellegrini	CHECKED P. Janson	SECTION
DATE 8/29/72	DATE 8-30-72	
ENG P. Janson	PROD J. Kelly	ISSUED SECT.
DATE 8/29/72	DATE 8-31-72	

LEGEND

D DOCUMENT
DN DOCUMENT CHANGE NOTICE
PA PAPER TAPE ASCII
PB PAPER TAPE BINARY
PM PAPER TAPE READ-IN-MODE

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION							KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
			DL11-A	DL11-B	DL11-C	DL11-D	DL11-E				
1	LIBKIT-11-KL11-04	KL11 MAINDEC	1	1	0	0	0				
2	LIBKIT-11-DL11C-A-K	DL11 MAINDEC	0	0	1	1	0				
3	LIBKIT-11-DL11E-A-K	DL11 MAINDEC	0	0	0	0	1				

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV.	ECO NO
DL11 SOFTWARE LIST	SHEET 1 OF 1	A	SL	DL11-0-4		
		DIST.				

DEC FORM NO. DEC 16-(327)-1049 N471
DRA 120

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ACCESSORY LIST

MADE BY	E. Pellegrini	CHECKED	C. Janson
DATE	June 26, 1972	DATE	8-8-72
ENG	Paul Janson	PROD	J. Thurston
DATE	June 26, 1972	DATE	8-8-72

SECTION

ISSUED SECT.

LEGEND

D	DOCUMENT
DN	DOCUMENT CHANGE NOTICE
PA	PAPER TAPE ASCII
PB	PAPER TAPE BINARY
PM	PAPER TAPE READ-IN-MODE

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION DL11-A	DL11-B	DL11-C	DL11-D	DL11-E			KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
1	M7800	ASYNCHRONOUS LINE INTERFACE (EIA)	-	1	-	1	1				
2	G8000	FILTER NETWORK	0	A/R	0	A/R	A/R				
3	M7800-YA	ASYNCHRONOUS LINE INTERFACE (CURRENT LOOP)	1	0	1	0	0				
4	5408776	PRIORITY JUMPER LEVEL #4	1	1	1	1	1				
5	BC05-C-25	MODEM CABLE	0	1	0	1	1				
6	7008360	TTY CABLE	1	0	1	0	0				
7	-	CRYSTAL	1	1	1	1	1				
8	-	DL11 ENGINEERING DRAWINGS	1	1	1	1	1				
9	DEC-11-HDLAA-A-D	DL11 ASYNCHRONOUS LINE INTERFACE MANUAL	1	1	1	1	1				
10	LIBKIT-11-KL11-04	KL11 MAINDEC	1	1	0	0	0				
11	LIBKIT-11-DL11C-A-K	DL11 MAINDEC	0	0	1	1	0				
12	LIBKIT-11-DL11E-A-K	DL11 MAINDEC	0	0	0	0	1				
13	H315	MODEM TEST CONNECTOR	0	0	0	0	A/R				

NOTES: 1. G8000 IS REQUIRED ONLY IN PDP-11 SYSTEMS WHERE +15V IS NOT AVAILABLE. ONE PER DD11-A.

2. CRYSTAL FREQUENCY DEFINED BY CUSTOMER SPECIFIED BAUD RATE.

3. ONE H315 PER PDP11 SYSTEM

4. INSURE THAT TRANSPARENT VINYL TAPE HAS BEEN APPLIED TO THE TOP SURFACE OF THE CRYSTAL AND MOUNTING BRACKET.

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV.	ECO NO
DL11 CHECK LIST	SHEET 1 OF 1	A	AL	DL11-0-5	C	DL11-00005
		DIST.				

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

DATE 6-21-72

TITLE DL11 INSTALLATION PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	CHANGE PER ECO	DL11-4	JANSON	3/73	P. Janson	4-6-73
D	CHANGE PER ECO	DL11-5	CONDON	7/73	L. Condon	8/27/73
E	CHANGE PER ECO	DL11-7	CONDON	8/74	L. Condon	9/1/74
F	CHANGE PER ECO	DL11-8	CONDON	4-75	L. Condon	4/8/75

ENG	APPD	SIZE	CODE	NUMBER	REV
Paul E. Janson	Paul E. Janson	A	SP	DL11-0-2	F

DEC FORM NO DRA 107A

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

DL11 INSTALLATION PROCEDURE:

Installation of the M7800 module or its variation as a DL11-A through DL11-E option consists of the following preparations:

1. Jumper insertion/deletion for selection of operation mode (A, B, C, D, or E).
2. Register address assignment.
3. Vector address assignment.
4. Priority assignment.
5. Special NPR jumper insertion/deletion.
6. Selection of data format (data bits, stop bits, parity).
7. Selection of crystal for baud rate.
8. Installation of G8000 in systems where +15v is not available.
9. Filter capacitor selection for high baud rate current-loop.

A. OPERATION MODE:

The following describes the jumpers associated with controlling the mode of operation (A,B,C,D, or E):

J1. Ties EIA driver to REQUEST-TO-SEND lead (pin 4) of dataset cable. IN for DL11-B,D, and E; does not affect DL11-A and C. Drawing DL-7.

J2. Ties EIA driver, normally used for the REQUEST-TO-SEND lead, to FORCE BUSY lead (pin 25) for use with Bell 103E. This is a customer option. If not specified, jumper is OUT for all DL11's. Drawing DL-7.

J3. When inserted, allows REQUEST-TO-SEND lead (pin 4) to be controlled by bit 2 of the receiver status register. OUT for DL11-B and D; IN for DL11-E; does not affect DL11-A and C. Drawing DL-4.

J4. When inserted, forces "DATA LEADS ONLY" mode of EIA operation. Turns DATA TERMINAL READY (pin 20) and REQUEST-TO-SEND (pin 4) on. IN for DL11-B and D; OUT for DL11-E; does not affect DL11-A and C. Drawing DL-4.

J5. When inserted, allows the BREAK bit to function. OUT for DL11-A and B; IN for DL11-C,D, and E. Drawing DL-4.

J6. When inserted, allows DSET INT to cause interrupts. OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-4.

J7. When inserted, allows dataset control bits to be read as part of the receiver status register.

	SIZE	CODE	NUMBER	REV
	A	SP	DL11-0-2	F

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

J7. (con't)

OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-2.

J8. When inserted, allows error bits to be read as part of the receiver data register. OUT for DL11-A and B; IN for DL11-C,D and E. Drawing DL-2.

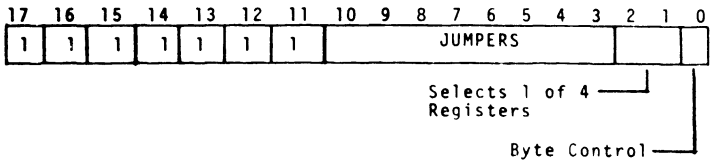
Summary of mode control jumpers:

JUMPER	A	B	C	D	E	DRAWING
J1	*	IN	*	IN	IN	DL-7
J2	OUT	OUT	OUT	OUT	OUT	DL-7
J3	*	OUT	*	OUT	IN	DL-4
J4	*	IN	*	IN	OUT	DL-4
J5	OUT	OUT	IN	IN	IN	DL-4
J6	OUT	OUT	OUT	OUT	IN	DL-4
J7	OUT	OUT	OUT	OUT	IN	DL-2
J8	OUT	OUT	IN	IN	IN	DL-2

*= don't care

B. REGISTER ADDRESS ASSIGNMENTS:

The DL11 can respond to addresses with the following format:



Bits 10 through 3 are controlled by jumpers A10 to A3. A jumper inserted indicates a zero.

For the DL11-A and B used as the console device, address 777560 is assigned. For additional units, assign 776XX0, where XX=50 for the first additional unit and XX=67 for the 16th unit.

For the DL11-C,D and E assign address 77XXX0, where XXX=561 for the first line, and XXX=617 for the 31st line. Assign all C's first, then D's, and then E's.

	SIZE	CODE	NUMBER	REV
	A	SP	DL11-0-2	F

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

C. VECTOR ADDRESS ASSIGNMENT:

Jumpers V8 through V3 control the interrupt vector. A jumper inserted provides a vector bit of one. Vectors can be produced in the form XXØ and XX4 where XX ranges from ØØ to 77.

For the DL11-A and B used as a console device the vector address is 060/064. For additional units vectors are floating.

For the DL11-C,D, and E vector addresses are floating. Assign all C's first, then D's then E's.

D. PRIORITY ASSIGNMENT:

Interrupt priority is established by inserting a "priority plug" in the socket at IC location E19. For DL11-A B,C,D and E use level 4, for the standard assignment or level 5-7 as specified by the customer or the documentation of an option which uses the DL11.

SUMMARY OF REGISTER, VECTOR AND PRIORITY ASSIGNMENTS:

	ADDRESS	VECTOR	PRIORITY
DL11-A,B CONSOLE	777560 777562 777564 777566	60/64	BR4
DL11-A,B ADDITIONAL UNITS	776XXØ 776XX2 776XX4 776XX6	FLOATING	BR4

Where XX= 50 for line #1
and XX= 67 for line #16

	ADDRESS	VECTOR	PRIORITY
DL11-C,D,E	77XXXØ 77XXX2 77XXX4 77XXX6	Floating	4

Where XXX= 561 for line #1
and XXX= 617 for line #31

	SIZE	CODE	NUMBER	REV
	A	SP	DL11-0-2	F

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

E. SPECIAL NPR JUMPER:

Jumper N1, shown on drawing DL-6, controls the response of the interrupt circuit to an NPR request. The jumper should normally be IN, except for 11/20 and 11/15 systems without the KH11 option.

F. SELECTION OF DATA FORMAT:

1. Data Bits

Split lug pairs NB2 and NB1 control the number of data bits in the serial character as follows:

NB2	NB1	# OF DATA BITS
OUT	OUT	8
OUT	IN	7
IN	OUT	6
IN	IN	5

2. Parity

Parity is controlled by split lug pairs NP and EPS as follows:

NP	EPS	PARITY
OUT	OUT	OFF
OUT	IN	OFF
IN	OUT	EVEN
IN	IN	ODD

3. Stop Bits

Split lug pair 2SB and jumpers J9, J10 and J11 control the number of stop bits in the serial character as follows:

2SB	J9	J10	J11	# OF STOP BITS
OUT	OUT	IN	OUT	2
IN	OUT	IN	OUT	1
IN	OUT	OUT	IN	1.5 for TI, GI, and SCM UARTS
IN	IN	OUT	OUT	1.5 for WD UARTS

G. CRYSTAL SELECTION:

The clocking scheme of the DL11 consists of a single crystal oscillator feeding a divider network, with two 10-position switches tapping various points to feed into the UART's

G. Con't

transmitter and receiver sections. Thus, for a given crystal frequency, 8 baud rates are independently selectable for transmit and receive. The two addition switch positions select external clocks.

SPEED GROUP		1	2	3	4
		CRYSTAL (HZ)			
POSITION	FACTOR	844.8K	1.03296M	1.152M	4.608M
1*	23040	36.7	44.8	50	200
2	15360	55	67.3	75	300
3	7680	110	134.5	150	600
4	3840	220	269	300	1200
5	1920	440	538	600	2400
6	960	880	1076	1200	4800
7	640	1320	1614	1800	7200
8	480	1760	2152	2400	9600

*Most counter-clock wise position.

To determine a crystal frequency for a non-standard baud rate, pick the position of the closest baud rate in the 1.152MHz column, and then multiply the non-standard baud rate by the factor for that position. For example, if the customer specifies 1050 baud, this is closest to 1200 baud, position 6.

1050 X 960 = 10080000 = 1.008MHz.

The crystal frequency should not fall outside the range of the standard crystals. Although the above table included only the standard DL11 crystals other values may be specified by the customer or by other documentation of an option which uses the DL11.

DEC part number for the standard crystals are as follows:

844.8 KHz	18-10245-1*
1.03296 MHz	18-05501-6
1.152 MHz	18-05501-5
4.608 MHz	18-05501-7

*Use A or C cut crystals only Do not use crystals marked NE-6D.

When ordering a special crystal, refer to purchase specification 18-05501 for crystal specification.

Insure that transparent vinyl tape (9008269) is applied to the top surfaces of the crystal and mounting brackets to insulate from adjacent modules.

H. G8000 INSTALLATION:

For DL11-B, D, and E a positive voltage is required between 9 and 15 volts to operate the EIA drivers. For PDP-11/20 and PDP-11/15 systems with the H720 power supply, a G8000 module must be installed to provide this voltage. Using a filter network, this module converts the full-wave rectified "+8V" signal to a positive DC voltage.

1. Install G8000 into slot AØ2 of DD11-A.
2. Wire AØ3V2 to AØ2Y2.
3. Wire AØ2N2 to CXXU1 where XX is the slot location of the M7800.

Refer to diagram 1.

I. FILTER CAPACITOR SELECTION:

For DL11-A's and DL11-C's, which operate with 20ma current loops, capacitors are used to filter the receive line and slow the switching time of the transmit line. To avoid excessive distortion above 150 baud, the capacitance in each of these two circuits must be reduced. This is accomplished by clipping C29 (.47 mfd) and C31 (1000 pf), both shown on drawing DL-3.

J. DL11-B,D,E in Systems with +15V available using DD11-A
There is a special situation of using a DD11-A to mount a DL11-B, D, Or E in systems with +15V available. These systems have +15V available and it appears at pin AØ3V2 of the DD11-A when using power harness such as 7009177, 7008855, or 7008909. In this situation, no G8000 is necessary, and +15V can be wired directly from AØ3V2 to CXXU1, where XX is the slot number of the DL11. NOTE: this does not apply to DL11-A or C or DD11-B.

K. When using the DL11-B,D,E in an 11/05 processor pin CXXU1 has +15V available on it so no G8000 or no jumpers are required.

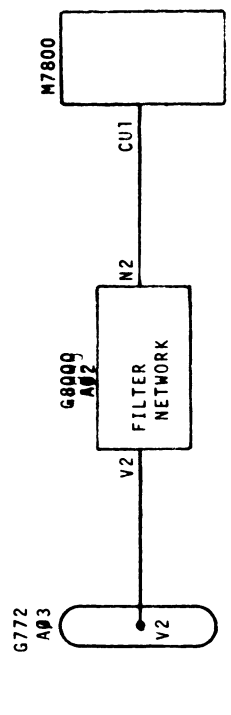
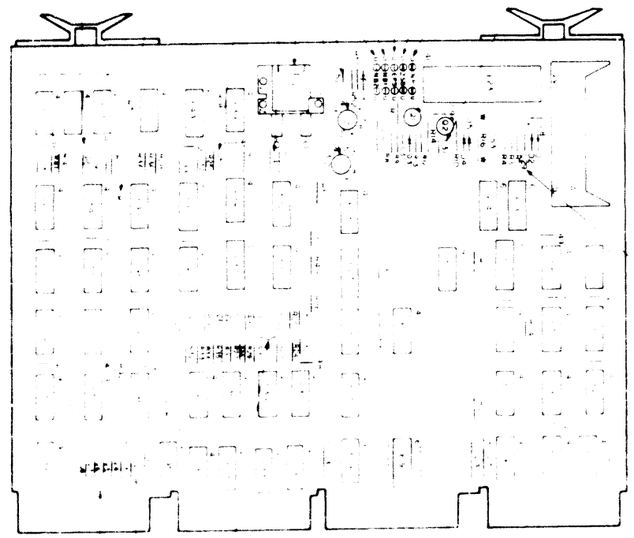


DIAGRAM 1. G8000 INSTALLATION



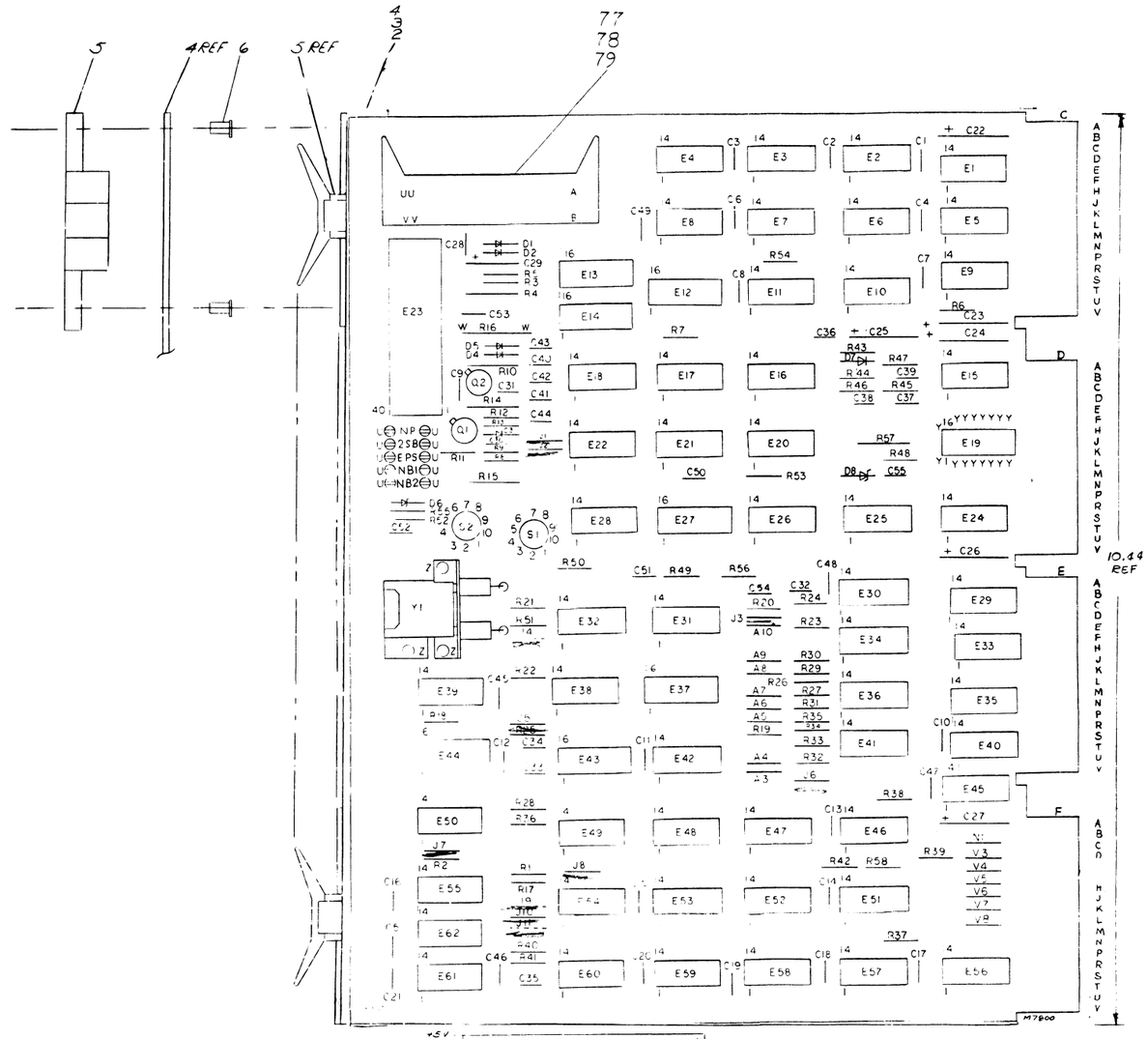
NOTES:

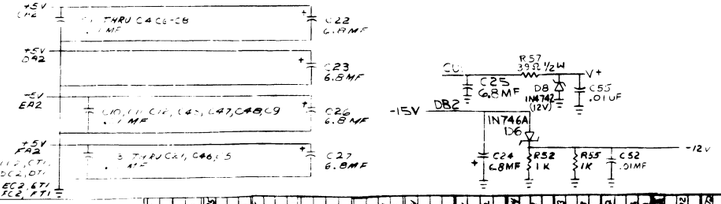
1. PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.
2. JUMPERS TO BE USED AT CONNECTIONS A3-A10, J1-J10, V3-V8, AND N1.
3. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X).

PIN NOMENCLATURE

MODULE	SYSTEM UNIT
A	C
B	L
C	F

4. DEC 8642's WERE PHASED IN AS DEC 38Ø REPLACEMENTS ANY 38Ø FAILURES SHOULD BE REPLACED BY 8642's EXCEPT E28. E28 MUST BE REPLACED WITH A 7380.
5. FOR YC VERSION, C36 VALUE IS 1200PF.





DEC 74161	8	16	—	—
DEC 1488	7	—	4	1
DEC UART	3	1	—	2
DEC 74175	8	16	—	—
DEC 8271	8	16	—	—
DEC 7442	8	16	—	—
DEC 314	1	8	—	—
DEC 7493	10	5	—	—
DEC 7492	10	5	—	—
DEC 74153	8	16	—	—
DEC 8640	1	8	—	—
DEC 7490	10	5	—	—
DEC 74123	8	16	—	—
IC TYPE	GND	+5V	+V	-12V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

ITEM NO.	QTY	REF DESIGNATION	DESCRIPTION	PART NO.
80	1	U28	DEC 1480	1910390
79	1		LATCH RIGHT	1209941-04
78	1		LATCH LEFT	1209941-03
77	1		CONNECTOR BERG	1209941-02
76	1		INSULATED JUMPER	9009185
75			[illegible]	1002[illegible]
74	[illegible]		WIRE [illegible]	9107[illegible]-01
73	1	R57	RES 39Ω 1/2W 5%	1302336
72	1	D8	DIODE 4742 12V 10% 1W ZENER	1109302
71	3		INT. WASHER #2	9006631
70	1	E22	IC DEC 1480	1910650
69	1		NUT HEX #2	9006555
68	1		SCR PHIL PAN HD 2-56 X 1/4 LG	9006301-1
67	1		ALIGAT PCB RG-1	1202512
66	1	DIODES D7	DIODE 1664 REV 100MA	1109114
65	1	D[illegible]	DIODE 1N4860	1104860
64	1	[illegible]	TRANSISTOR 2N34D	1503409-00
63	1	[illegible]	CAP 100PF 100V 5% DIPPED MICA	1000016
62	1	[illegible]	CAP .5UF 100V 5% DIPPED MICA	1000025
61	1	C55 [illegible]	CAP .47MF CERAMIC	1003978
60	1	C36	CAP 1200PF 100V 5% DIPPED MICA	1000121
59	2	C34, C35	CAP 330PF 100V 5% DIPPED MICA	1000123
58	2	C30, C37 [illegible]	CAP 47PF 100V 5% DIPPED MICA	1000124
57	1	C31	CAP 150PF 100V 5% DIPPED MICA	1000122
56	30	C1-28 [illegible]	CAP .01UF 100V 20% CERAMIC DISC	1001402-01
55	1	C29	CAP 1.0UF 35V 10% TANT	1003962
54	6	C22-C27	CAP 6.8 UF 35V 10% TANT	1003306
53	1	C33	CAP 150PF 100V 5% DIPPED MICA	1000119
52	2	R14, R15	RES 1.5K 1/2W 5%	1303915
51	1	R[illegible]	RES 1K 1/4W 5%	1303165
50	1	R4	RES 47.1K 1/4W 5%	1302052
49	1	R10	RES 68.1K 1/2W 5%	1303405
48	1	R5	RES 8.[illegible] 1/4W 2%	1301477
47	4	R24, R25, R26, R27	RES 100K 1/4W 5%	1302239
46	1	R11	RES 150K 1/4W 5%	1302630
45	2	R23	RES 2[illegible] 1/4W 5%	1302322
44	2	R44 [illegible]	RES [illegible] 1/4W 5%	1302271
43	1	R45	RES [illegible] 1/4W 5%	1302309
42	2	R9, R13, R43 [illegible]	RES [illegible] 1/4W 5%	1302316
41	1	R8	RES [illegible] 1/2W 5%	1302338
40	1	R3	RES [illegible] 1/4W	1302401
39	1	R16	RES [illegible] 1/4W 5%	1302385
38	7	R1, R2, R6, R7, R17, R22, R40, R41, R42, R58, R59 x4	RES 1K 1/4W 5%	1302479
37	2	R[illegible], R[illegible]	RES [illegible] 1/4W 5%	1302391
36	[illegible]	[illegible]	RES [illegible] 1/4W 5%	1302394
35	4	C32, C36, C41, C42	CAP [illegible] 100V 10% CERAMIC DISC	1001402-01
34	3	C38, C39, C40	IC DEC 8642	1909712
33	3	C31, C49, C50	IC DEC 7404	1910155
32	6	C18, C21	IC DEC 8659	1910323
31	2	C1, C14	IC DEC 1489	1909037
30	11	E1, E2, E3, E4, E5, E6, E7, E8, E9, E10, E11	IC DEC 8641	1909705
29	[illegible]	[illegible]	IC DEC 1488	1910326
28	1	E41	IC DEC 74123	1909439
27	3	E48, E57, E58	IC DEC 74174	1909267
26	3	E49, E50, E51	IC DEC 7400	1903775
25	1	E10	IC DEC 7413	1909989
24	6	E52, E53, E54, E55, E56, E[illegible]	IC DEC 7402	1909004
23	[illegible]	E[illegible]	IC DEC 8640	1911469
22	1	E18	IC DEC 74153	1909927
21	1	E60	IC DEC 74LS[illegible]	1909933
20	1	E35	IC DEC 7492	1909059
19	5	E6, E16, E17, E35, E37	IC DEC 7404	1909606
18	1	E24	IC DEC 7493	1909054
17	1	E34	IC DEC 7410	1903776
16	1	E39	IC DEC 314	1909706
15	1	E37	IC DEC 7442	1909046
14	1	E42	IC DEC 8271	1909613
13	2	E13, E14	IC DEC 74175	1906471
12	1		DELAY LINE CRYSTAL HOLDER	1302283
11	1		BRACKET, CRYSTAL HOLDER	1301176
10	1	E19	IC SOCKET	1209930
9	2	S1, S2	SWITCH, SINGLE POLE, 10 POS	1200972-1
8	[illegible]	[illegible]	NO PIN CONNECTOR [illegible]	[illegible]
7	10		SPLIT LUGS	9002135
6	8		SOCKET #554-7 E.F. SITTMAN	9006552
5	1		HANDLE, FLIP-CHIP, WIRE WRAP	9008337-06
4	1		ETCHED CIRCUIT BOARD	3009776
REF	REF		MODULE ECO HISTORY	A-M-M7800-0-1
REF	REF		ASSY DRILLING HOLE LAYOUT	D-M-M7800-0-1
REF	REF		XY COORDINATE HOLE	X-00-M7800-0-1

PARTS LIST

ETCH BOARD REV H

DEC NO.	EIA NO.	DEC NO.	EIA NO.
		G534D	MPS6534
		IN746A	1N4736A
		D66	1N3606

SEMICONDUCTOR CONVERSION CHART

REV	DESCRIPTION	CHANGE NO.	DATE	APPROVED
A	M7800-0001		3/11/74	
B	M7800-0002		6-23-72	
C	M7800-0003		8-30-72	
D	M7800-0004		9-22-72	
E	M7800-0005		11-3-72	
F	M7800-0006		3/11/74	
G	M7800-0007		5/21/74	
H	M7800-0008		6-23-74	
J	M7800-0009		8-30-74	
K	M7800-0010		11-15-74	
L	M7800-0011		3/11/75	
M	M7800-0012		6-23-75	
N	M7800-0013		8-30-75	
P	M7800-0014		11-15-75	

REVISIONS

DRN	M. Pena	DATE	2/6/74
CHK		DATE	3/11/74
ENG		DATE	3/11/74
MFG		DATE	3/11/74
NEXT HIGHER ASSY			
SCALE		SHEET	1 OF 2

EQUIPMENT CORPORATION

TITLE: ASYNCHRONOUS LINE INTERFACE

SIZE E | CS M7800-0-1 | REV P

DIST

DEC FORM NO. 2SE 301

DL-2 BINIT H
BUS INIT L
DL-2 BINIT L

DL-2 BD07 H
DL-2 BD06 H
DL-2 BD05 H
DL-2 BD04 H
DL-2 BD03 H
DL-2 BD02 H
DL-2 BD01 H
DL-2 BD00 H

DL-4 RD7 H
DL-4 RD6 H
DL-4 RD5 H
DL-4 RD4 H
DL-4 RD3 H
DL-4 RD2 H
DL-4 RD1 H
DL-4 RD0 H
DL-5 RBUF TO BUS H

DL-4 XMIT READY H
DL-4 XMIT INT ENB (1)H
DL-4 MAINT (1)H
DL-4 BREAK (1)H
DL-5 XCSR TO BUS H

DL-4 RCVR DONE H
DL-4 RCVR INT ENB (1)H
DL-4 DATASET INT ENB (1)H
DL-4 SEC XMIT (1)H (LKI)
DL-4 REQ TO SEND (1)H (CMI)
DL-4 DATA TERMINAL READY (1)H (CFI)

CM2 BUS D07 L
CV2 BUS D06 L
CP2 BUS D05 L
CN2 BUS D04 L
CT2 BUS D03 L
CU2 BUS D02 L
CR2 BUS D01 L
CS2 BUS D00 L

DL-5 RCSR TO BUS L
J7
R2 10K

J8
R1 10K
DL-5 RBUF TO BUS L

DL-4 OR ERR H
DL 4 FR ERR H
DL-4 P ERR H

ERROR H

DL-7 DATASET INT (1)H
DL-7 RING H
DL-7 CLEAR TO SEND H
DL-7 CARRIER H
DL-5 RCSR TO BUS H
DL-4 RCVR BUSY (1)H
DL-7 SEC REC DATA H

CD2 BUS D15 L
CE2 BUS D14 L
CF2 BUS D13 L
CH2 BUS D12 L
CH1 BUS D11 L
CJ2 BUS D10 L

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL: DL11	QTY.	DESCRIPTION	PART NO.
PARTS LIST			

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRAWN B. Peck DATE 3-20-72
CHK'D DATE 4-3-72
ENG DATE 4-3-72
MFG DATE 4-3-72
PROJ. DATE 4-3-72
NEXT HIGHER ASSY.
SCALE
SHEET OF

[redacted] EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (BUS RECEIVERS & DRIVERS) DL-2

SIZE	NUMBER	REV.
D	CS M7800-0-1	P

DWG.

SEE NOTE 3

YI		844.8 KHZ		1.03296 MHZ		1.152 MHZ		4.608 MHZ	
		BAUD	μSEC	BAUD	μSEC	BAUD	μSEC	BAUD	μSEC
SWITCH POS.	1	36.7	1700	44.8	1342	50	1250	200	312
	2	55	1135	67.3	928	75	833	300	208
	3	110	567	134.5	464	150	417	600	104
	4	220	284	269	232	300	208	1200	52
	5	440	142	538	116	600	104	2400	26
	6	880	71	1076	58	1200	52	4800	13
	7	1320	47.4	1614	38.7	1800	34.6	7200	8.7
	8	1760	35.5	2152	29	2400	26	9600	6.5
	9	BERG CLOCK INPUT - COMMON TO RCVR AND XMIT							
	10	EXTERNAL CLOCK INPUT - RCVR: DSI ; XMIT: DRI							

DL-3 BB IN H — DV2 — PRIORITY PLUG E19 — DDB BUS BR7 L
DL-6 BB OUT H — DV2
BUS BG4 OUT H — DT2 — DT2 BUS BR5 L
BUS BG4 IN H — DR2 — DR2 BUS BR4 L
BUS BG5 OUT H — DR2 — DL-6 REQUEST L
BUS BG5 IN H — DF2 — DR2 BUS BR7 IN H
BUS BG6 OUT H — DM2 — DL2 BUS BR7 OUT H
DM2 BUS BR6 IN H

R49 10K, R50 10K, 7380 E28, C50 .047UFD, C51 .047UFD, Y1, R51 47Ø

20 MA RECEIVE (K) (S) — +5V R3 75Ø, R4 56Ø -15V, C28 .01UFD, C29 .47UFD, C45 .01UFD, D1 D664, D2 D664, (H) TO MFPS INTERLOCK

7490 E26 — SET9, CLR, CLKB0 CLKB — R3(1) R2(1) R1(1) R8(1)
7492 E25 — CLR, CLKBC CLKB — R3(1) R2(1) R1(1) R8(1)
7493 E24 — CLR, CLKBC CLKB — R3(1) R2(1) R1(1) R8(1)

DR1 EXT XMIT INPUT
DL-3 XMIT CLK H — T S1
(CC) BERG CLOCK INPUT
DSI EXT RCVR INPUT
DL-3 RCVR CLK H — R S2

74153 E12 — F1 — Ø9 FR1 DL-3 RCLK H
BERG CLOCK INPUT(CC)
BERG SERIAL IN L (E) — +5V R7 10K — 7413 E10
TTL SERIAL IN L (AA) — +5V R6 10K — 7413 E10
Ø7 FSI DL-3 SI H
DL-4 MAINT (I)H
BERG CLK ENB L (HH) — +5V R54 10K
DL-4 SERIAL OUT H

T 74161 E27 — +5V R56 10K — CLR, D3 D2 D1 D0, R3(1) R2(1) R1(1) R8(1), CARRY, LD, CLK — Ø9 Ø2
7380 E28

DL-4 RDR ENB (I)H — 7404 E17 — DB1 TTL RDR ENB L — +5V R11 150, R9 478, R8 1.5K, Q1 6534D, D3 D664, C30 .01UFD — (PP) 6 — READER RELAY

-15V — R10 68Ω — (EE) 4

DC1 TTL SERIAL OUT L — 7404 E17 — +5V R12 1.5K, R13 470, C31 1000 pf, Q2 6534D, D4 D664, D5 D664, R14 1.5K, R15 1.5K, R16 75Ø — (SS) — (AA) 5 — 20 MA TRANSMIT — (KK) 2

+5 — (TT) — (A) — (B) — (VV) — (UU)

NOTES:
1. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X)
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE 7008360 CABLE. THIS CABLE ALSO CONNECTS BERG PINS H TO E.
3. ALTHOUGH THE ABOVE TABLE INCLUDES ONLY THE STANDARD DL11 CRYSTALS OTHER VALUES MAY BE SPECIFIED BY THE CUSTOMER OR BY OTHER DOCUMENTATION OF AN OPTION WHICH USES THE DL11.

REVISIONS

CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.
DL11		PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓
MATERIAL
FINISH

DRAWN B Pirdi 8-20-72 — CHK'D J Feigar 8-25-72 — ENGR Tom Cardon 8-27-72 — MFG Joe Jason 8-27-72 — QA 8-27-72 — NEXT HIGHER ASSY. — SCALE — SHEET 3 OF 9

EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (CLOCK & CURRENT LOOPS) DL-3

SIZE D — CODE CS — M78ØØ-Ø-1 — REV. P

DL-2 BINIT L

DL-5 SEL 2 L

DL-2 BINIT H

DL-4 RCVR BUSY (1)H

DL-5 SI H

DL-5 RCLK H FRI

DL-4 SERIAL OUT H

DL-3 XMIT CLK H

DL-5 LD XD L

X CLK H

DL-2 BD07 H
DL-2 BD06 H
DL-2 BD05 H
DL-2 BD04 H
DL-2 BD03 H
DL-2 BD02 H
DL-2 BD01 H
DL-2 BD00 H

CLR R DONE
STB STATUS
STB RD
R CLK
SERIAL IN
R DONE
OR ERR
FR ERR
P ERR
RD7
RD6
RD5
RD4
RD3
RD2
RD1
RD0
SERIAL OUT
XRDY
EOC
CLR LDC NB2 NB1 NP EP 2SB

DL-4 OR ERR H
DL-4 FR ERR H
DL-4 P ERR H
DL-4 RD7 H
DL-4 RD6 H
DL-4 RD5 H
DL-4 RD4 H
DL-4 RD3 H
DL-4 RD2 H
DL-4 RDI H
DL-4 RD0 H

DL-2 BD02 H
DL-2 BD00 H
DL-2 BD06 H
DL-4 MA INT (1)H
DL-4 BREAK (1)H
DL-4 BREAK (0)H
DL-4 XMIT INT ENB (1)H
DL-5 BUS TO XCSR H

DL-4 XMIT READY H
DL-4 XMIT INT H
DL-4 RCVR DONE H
DL-7 DATASET INT (1)H
DL-4 RCVR INT H

DL-2 BD05 H
DL-2 BD02 H
DL-2 BD06 H
DL-2 BD03 H
DL-4 DATASET INT ENB (1)H
DL-4 REQ TO SEND (1)H
DL-4 REQ TO SEND (0)H
DL-4 RCVR INT ENB (1)H
DL-4 SEC XMIT (1)H
DL-4 SEC XMIT (0)H

DL-4 DATA LEADS ONLY L
DL-2 BD01 H
DL-4 DATA TERMINAL READY (1)H
DL-4 DATA TERMINAL READY (0)H
DL-2 BD00 H
DL-4 RDR ENB (1) H
DL-5 BUS TO RCSR H

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL: DL11	QTY.	DESCRIPTION: PARTS LIST	PART NO.

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES: DECIMALS .XXX ± .005, .XX ± .02, .X ± .1; ANGLES ±0° 30'. REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

DWN. B Pinder	DATE 3-26-72	EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS
CHK'D. W. Gagnon	DATE 4-11-72	
ENGR. Dan London	DATE 4/11/72	
PROJ. ENG. [illegible]	DATE 4-27-72	
APPD. [illegible]	DATE 4 D-72	

MATERIAL: —
FINISH: —
NEXT HIGHER ASSY.:
SCALE:
SHEET 1 OF 1

TITLE: ASYNCHRONOUS LINE INTERFACE (UART & STATUS) DL-4

SYSTEM	NUMBER	REV.
DCS	M7800-0-1	P

SIZE: D

BUS A11 L
BUS A13 L
BUS A14 L
BUS A15 L
BUS A16 L
BUS A17 L
BUS A12 L
316 E29
BUS MSYN L
8640 E33
7410 E34
+5V
R27 10K
R29 10K
R30 10K
R31 10K
R32 10K
R33 10K
R34 10K
R35 10K
R26 1K
A10
A9
A8
A7
A6
A5
A4
A3
8242 E36
8242 E37
8242 E38
8242 E41
8242 E42
8242 E43
8242 E44
8242 E47
BUS A10 L
BUS A09 L
BUS A08 L
BUS A07 L
BUS A06 L
BUS A05 L
BUS A04 L
BUS A03 L
BUS A01 L
BUS A02 L
BUS A00 L
BUS C1 L
BUS C0 L
8640 E40
8640 E45
8640 E46
8640 E48
8640 E49
8640 E50
8640 E51
8640 E52
8640 E53
8640 E54
8640 E55
8640 E56
EP1
EP2
EU1
EV1
EU2
EV2
EH1
EF1
EH2
EF2
EJ2
7418 E34
7404 E39
8881 E30
R23 1K
R24 180
C32 470 pf
EL1 BUS MSYN H
EL2 REG SEL H
7404 E39
R28 10K
R25 10K
C33 150pf
500ms
74123 E43
EBL DL 5 LD XD L
DL-5 BUS TO XBUF L
7404 E39
DL-5 BUS TO XCSR H
7404 E39
DL-5 BUS TO RCSR H
7404 E38
DL-5 XCSR TO BUS H
DL 5 RBUF TO BUS L
7404 E38
DL-5 RBUF TO BUS H
7404 E38
DL-5 RCSR TO BUS H
R36 10K
C34 330pf
1000ms
DL 5 SEL 2 L
DL 5 BUS TO RBUF L
DL-5 RCSR TO BUS L
7442 E37
D3
D2
D1
D0
NOTE: THE A LINES ARE TO BE JUMPERED FOR A 0

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL: DL11	QTY.	DESCRIPTION	PART NO.
		PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: XXX = .005, XX = .02, X = .1
ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRN. — DATE 4-27-73
CHKD. — DATE 4-27-73
ENG. — DATE 4-27-73
PROJ ENG. — DATE 4-27-73
MFG. — DATE 4-27-73
NEXT HIGHER ASSY.
SCALE
SHEET 5 OF 7

EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE: ASYNCHRONOUS LINE INTERFACE (ADDRESS SELECTION) DL-5

SIZE	CODE	NUMBER	REV.
D	CS	M7800-0-1	P

SHT.