

DR11-A

General Device Interface

DR11-A General Device Interface

The DR11-A General Device Interface is a set of three logic modules which form a self-contained interface between the PDP-11 UNIBUS and a user's peripheral. The DR11-A performs all of the necessary tasks to communicate with the PDP-11, so that the user may easily interface his device. The simplicity and low cost of the DR11-A demonstrates the utility and power of the PDP-11 UNIBUS concept.

The DR11-A permits bidirectional transfer of 16-bits of information between a user's device and PDP-11 UNIBUS. The three functional sections of the DR11-A are: the M786 16-bit I/O Buffer, the M7820 Bus and Interrupt Control Unit, and the M105 Address Selector Unit.

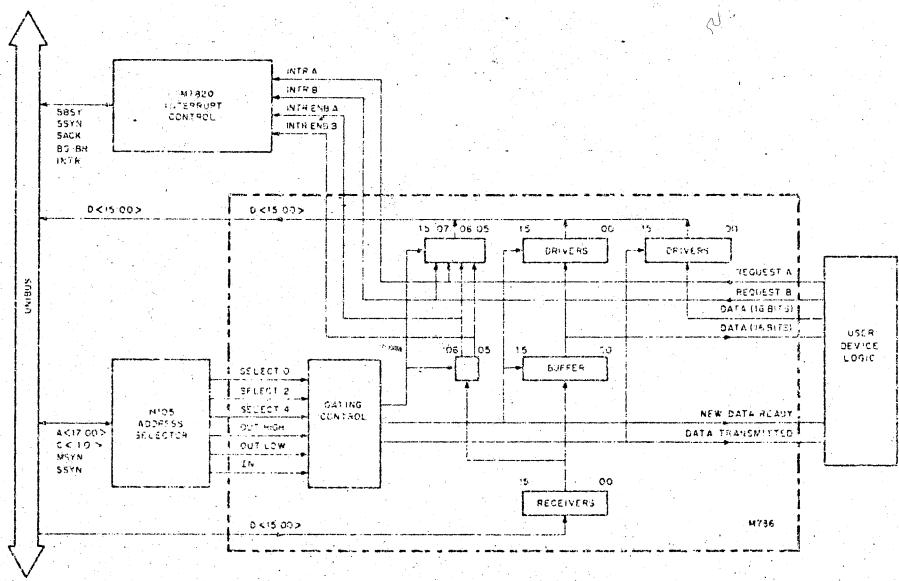
OUTPUT: Information from the UNIBUS is stored in a 16-bit buffer register. Once this register has been set under program control, the outputs are available to the device until the register is loaded with new data from the UNIBUS. The register can also be read onto the UNIBUS.

INPUT: The DR11-A also provides 16 lines of input to UNIBUS transmitter. This allows data from user devices to be read onto the UNIBUS. These signals are not held in the flip-flop register of the DR11-A.

CONTROL: Upon data transfer to the buffer register, a control signal, NEW DATA READY, indicates to the device that data has been loaded into the register. For input onto the UNIBUS, a control signal, DATA TRANSMITTED, indicates to the device that the input lines have been read.

Two interrupt request lines provide the ability to make vectored interrupt requests to the PDP-11 processor through two sets of unique vector addresses. Interrupt enable/disable circuits are controlled by bits 6 and 5 of the addressable DR11-A control register.

Complete information for designing with the DR11-A is supplied in the PDP-11 UNIBUS Interface Manual, available upon request.

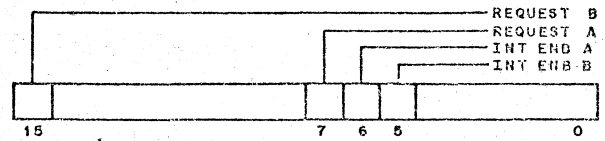


DR11-A General Device Interface Block Diagram

Registers

Control Register

INT ENB A



Enables Interrupt requests from request line A.

INT ENB B

Enables Interrupt requests from request line B.

Both may be set or cleared from Unibus.

Both are cleared by START or RESET.

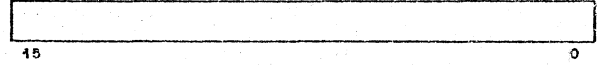
REQUEST A

Indicates status of REQUEST A line; +3V = 1, 0V = 0.

REQUEST B

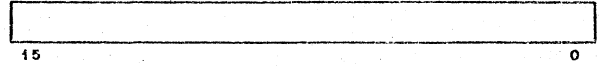
Indicates status of REQUEST B line; +3V = 1, 0V = 0.

Buffer Register



All bits may be cleared or set from Unibus. Register cleared by START or RESET. Outputs available to user.

Input Register



All bits may be read from UNIBUS. Bit status determined by user input lines.

Register Addresses

Control 177520

Standard factory setting.

Buffer 177522

May be changed by jumpers on M105.

Input 177524

Vector Address A 110

Standard factory setting.

Vector Address B 114

May be changed by jumpers on M7820.

Priority Level

5 normal

May be changed by priority jumper plug on M786.

Input Levels

+3V = 1, 0V = 0

1 TTL unit load

Output Levels

+3V = 1, 0V = 0

capable of driving 8 TTL loads

Signal Connections

Input, output, control and ground signals are available on two H807 connectors mounted on the M786. Connections are normally made to the H807's via M925 (flexprint connector card) or M927 (cable connector cards with solder lugs for ribbon cable or twisted pairs). Two M927 Connector Cards are supplied.

Environmental

Temperature 10° - 50°C

Humidity 20% - 90% noncondensating

Physical

Mounts in one small peripheral slot in KA11 or DD11-A.

Power derived from H-720 in BA11.

Features:

Low-cost

Completely self-contained interface

16-bits input and output

Supplies all needed control signals

Operates in PDP-11 interrupt environment

DR11-A General Device Interface

The DR11-A General Device Interface is a 3-module set that plugs into either a small peripheral slot in the processor or into one of four slots in a DD11 Small Peripheral Mounting Panel. The DR11-A provides the logic and buffer register necessary for transfers of 16-bit input and output data between the PDP-11 System and an external device.

The DR11-A contains three functional sections: a 16-bit buffer register, a 16-bit data input circuit, and a 2-channel flag and interrupt control. Address and bit assignments are shown in Figure 1. The DR11-A contains three physical modules: an M105 Address Selector, an M7820 Interrupt Control and an M786 General Device Interface with two M927 cable connectors.

The 16-bit buffer register is an addressable register that may be read or loaded by instructions transmitted through the Unibus (see Figure 1). The register outputs, together with a control signal pulse (NEW DATA READY) used to indicate that the register has been loaded from the Unibus, are available on a printed circuit edge connector #1 which is mounted on the M786 Module. All bits in the buffer register are cleared to 0s by the occurrence of an INIT signal on the Unibus. These signals are logic levels of either +3V (true) or 0V (false). The NEW DATA READY signal is a pulse which has a leading edge coincident with the loading of the buffer flip-flops. The connector accepts an M927 Cable Connector, which contains solder lugs and can be used with ribbon cable, twisted pair cable, or open wire. The M927 is electrically identical to the M904 Module described in the Logic Handbook.

The interface input circuits consist of 16 bus drivers gated to the bus when the input register is read by a DATI bus sequence (see Figure 1). The 16 input lines are +3V if true or 0V if false. These signals are also applied to the M786 Module through an M927 Cable Connector and a second printed circuit connector #2. When a DATI sequence occurs, a pulse signal (DATA TRANSMITTED) is applied to the external device.

Two additional request lines are furnished and may be asserted (+3V) by the external device to initiate an interrupt or to generate a flag that may be tested by the program. Whether these two request lines cause an interrupt is determined by two interrupt enable flip-flops which form part of the control and status register in the option (see Figure 1). The request lines form two more bits of the status register, independent of the status of the enable flip-flops; thus, they may be tested by the program.

The priority level of both interrupts must be the same, with interrupt A on a higher sublevel than interrupt B. The M786 contains a priority jumper plug which is normally set at BR5. The interrupt enable flip-flops are cleared to 0 (inhibit interrupt) by the occurrence of an INIT signal on the Unibus, or may be set or cleared by the program. Priority may be changed by the jumper plug.

The DR11-A pin assignments are listed in Table 1. All inputs are one standard TTL unit load. Inputs have diode protection clamps to ground and +5V. All signals are +3V if true. All outputs are TTL levels capable of eight unit loads. The new data ready and data transmitted signals are positive pulses, approximately 2 μ s in duration

Table 1
DR11-A Pin Assignments

Inputs			Outputs		
Signal	Connector	Pin	Signal	Connector	Pin
IN00	2	S1	OUT00	1	P2
IN01	2	S2	OUT01	1	M2
IN02	2	P1	OUT02	1	S1
IN03	2	L1	OUT03	1	P1
IN04	2	P2	OUT04	1	K2
IN05	2	K2	OUT05	1	M1
IN06	2	M1	OUT06	1	S2
IN07	2	T2	OUT07	1	L1
IN08	2	M2	OUT08	1	J1
IN09	2	D2	OUT09	1	H2
IN10	2	E1	OUT10	1	E2

(continued on next page)

Table 1 (Cont)
DR11-A Pin Assignments

Inputs			Outputs		
Signal	Connector	Pin	Signal	Connector	Pin
IN11	2	D1	OUT11	1	H1
IN12	2	H1	OUT12	1	D2
IN13	2	E2	OUT13	1	E1
IN14	2	B1	OUT14	1	D1
IN15	2	J1	OUT15	1	B1
REQUEST A	1	T2	NEW DATA RDY	1	V2*
REQUEST B	2	H2	DATA TRANSMITTED	2	V2*

*Pulse signals, approximately 2 μ s wide.

Figure 2 shows the physical layout of the M786 and M927 modules.

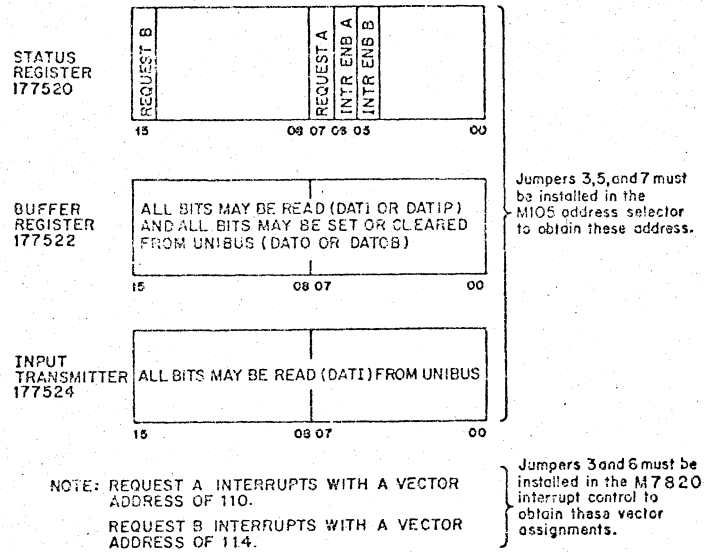


Figure 1 DR11-A Address and Bit Assignments

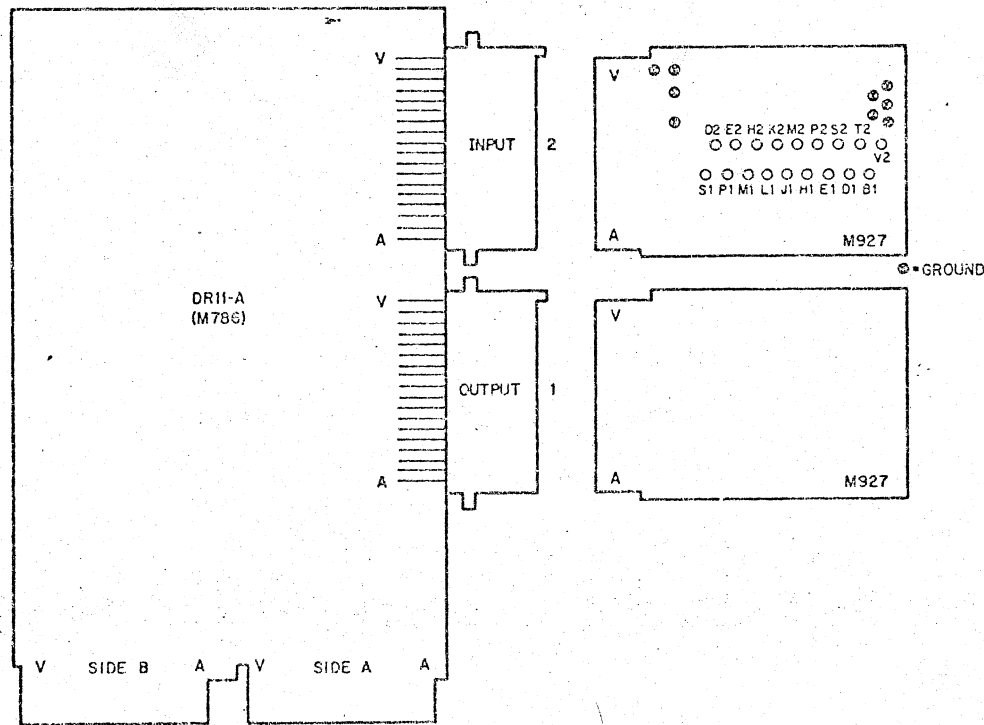
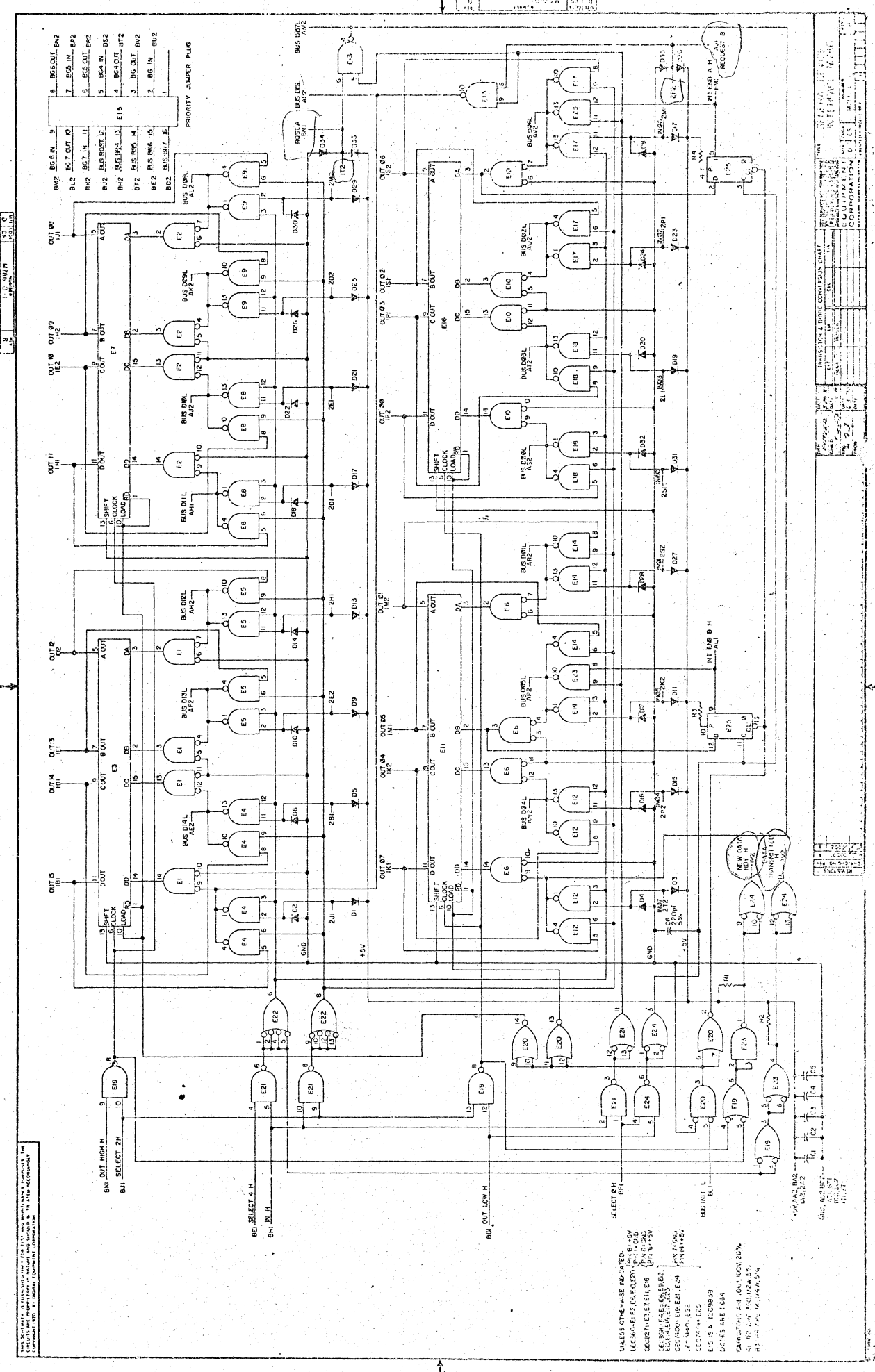


Figure 2 DR11-A Physical Layout



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UNLESS OTHERWISE INDICATED:
 RESISTORS: ALL VALUES UNLESS OTHERWISE SPECIFIED.
 CAPACITORS: ALL VALUES UNLESS OTHERWISE SPECIFIED.
 DECODERS: ALL VALUES UNLESS OTHERWISE SPECIFIED.
 LOGIC: ALL VALUES UNLESS OTHERWISE SPECIFIED.
 CONNECTIONS: ALL VALUES UNLESS OTHERWISE SPECIFIED.
 DIMENSIONS: ALL VALUES UNLESS OTHERWISE SPECIFIED.

DATE: 10/18/78
 TIME: 14:21
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 CHECKED: [illegible]
 APPROVED: [illegible]
 TITLE: [illegible]

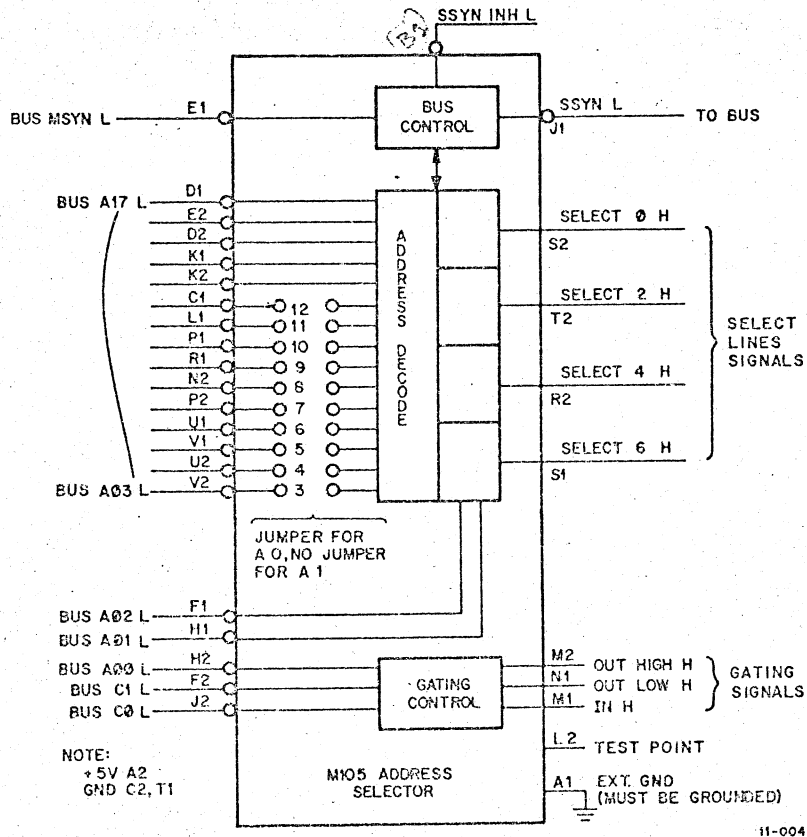
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3.3.4 M105 Address Selector Module

The M105 Address Selector Module provides gating signals for up to 4 full 16-bit device registers. A block diagram of this module is shown in Figure 3-11. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the M105 is used in a peripheral device, an OUT transfer is a transfer of data out of the master (such as the processor) and into the device. Likewise, an IN transfer is the operation of the peripheral furnishing data to the processor. The M105 Module is described more fully in following paragraphs.

3.3.4.1 Inputs -- The M105 Module input signals consist of 18 address lines, A(17:00); 2 bus control lines, (1:0); and a master synchronization (MSYN) line. The address selector decodes the 18-bit address on lines A(17:00) as described below. This address format, used for selecting a device register, is shown in Figure 3-12. Note that all inputs are standard bus receivers.

- a. Line A00 is used for byte control.
- b. Lines A01 and A02 are decoded to select one of the four addressable device registers.
- c. Decoding of lines A(12:03) is determined by jumpers on the module. When a given line contains a jumper, the address selector searches for a zero on that line. If there is no jumper, the address selector searches for a one.
- d. Address lines A(17:13) must be all ones. This specifies an address within the top 8K byte address bounds for device registers.



11-0046

Figure 3-11 M105 Address Selector

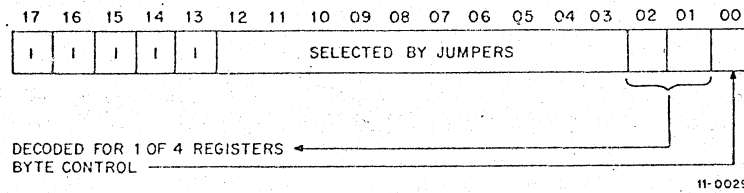


Figure 3-12 Device Register Select Address Format

3.3.4.2 Slave Sync (SSYN) – When SSYN INH is grounded, it inhibits the acknowledgment signal (SSYN) normally generated by the M105. In this case, the SSYN must be generated by another source. When SSYN INH is not grounded, SSYN is returned to the master 100 ns after register select becomes true. This time may be extended to a maximum of 400 ns by adding an external capacitor between SSYN INH and ground.

3.3.4.3 Outputs – The M105 Output Signals permit selection of four 16-bit registers and provide three signals used for gating information to and out of the master device. The M105 may be used instead to select up to eight 8-bit registers, or any appropriate combination of byte and word registers.

The input signals select the M105 control output line states as shown in Tables 3-2 and 3-3.

Table 3-2
M105 Select Lines

Input Lines A<02:01>	Select Lines True (+3V)
00	0
01	2
10	4
11	6

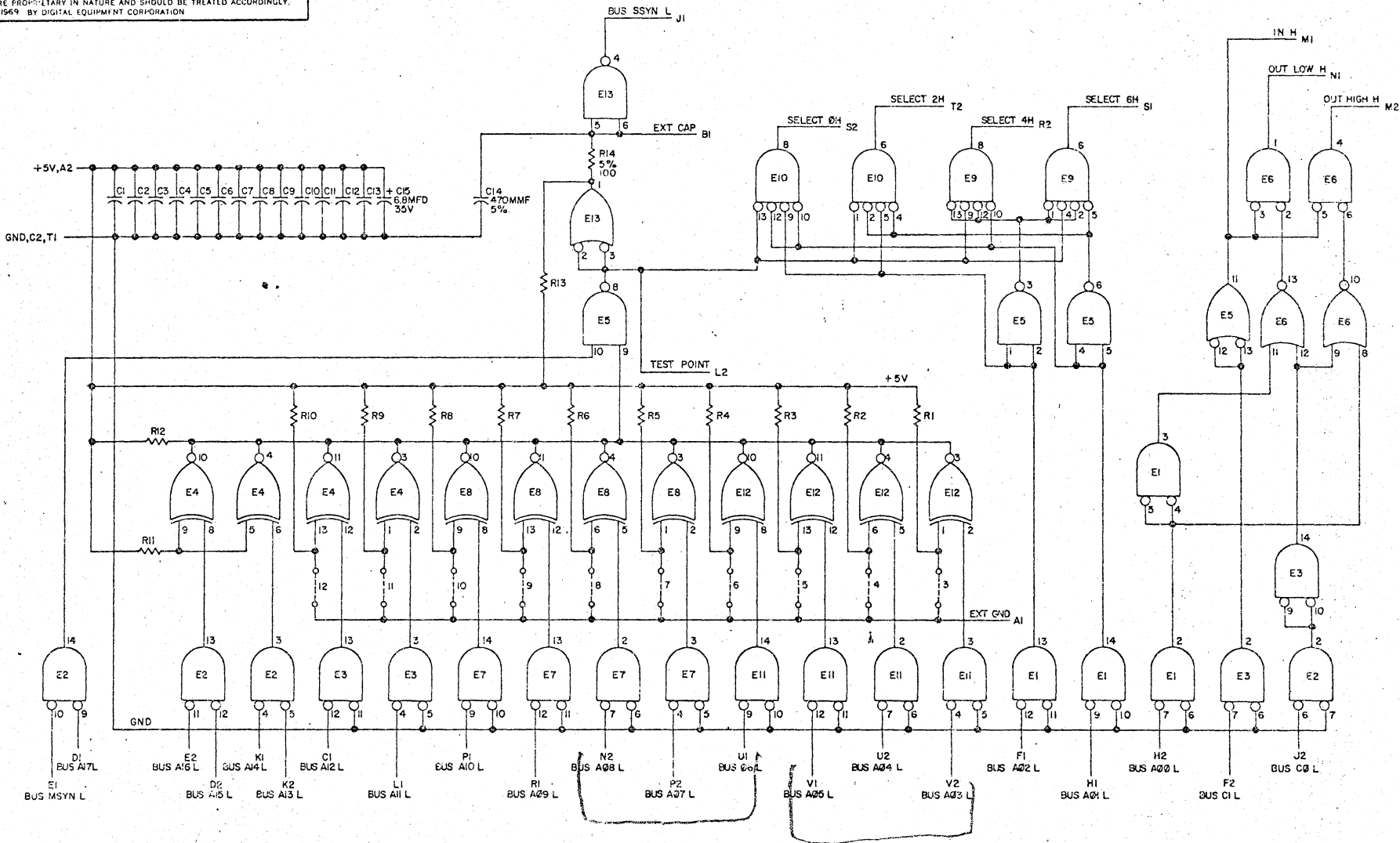
NOTE

1. Lines A<17:13> must be all 1s (0V on Unibus).
2. Lines A<12:03> are selected by jumpers.

Table 3-3
Gating Control Signals

Mode Control C<1:0>	Byte Control A00	Gating Control Signals True (+3V)	Bus Sequence
00	0	IN	DATI
00	1	IN	DATI
01	0	IN	DATIP
01	1	IN	DATIP
10	0	OUT LOW	DATO
		OUT HIGH	

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UNLESS OTHERWISE INDICATED:
 ○---○ INDICATES JUMPERS
 RESISTORS ARE 1K, 1/4W, 5%
 CAPACITORS ARE .01MFD, 100V, 20%
 E1, E2, E3, E7, E11 ARE DEC380
 E4, E5, E12 ARE DEC8242
 E9, E10 ARE DEC8815
 E5 IS DEC7400
 E6 IS DEC7402
 E13 IS DEC8881
 PIN 1 ON E1, E2, E3, E7, E11 = GND
 PIN 8 ON E1, E2, E3, E7, E11 = +5V
 PIN 7 ON E4, E5, E6, E8, E9, E10, E12, E13 = GND
 PIN 14 ON E4, E5, E6, E8, E9, E10, E12, E13 = +5V

REVISIONS A B C	DATE 11-26-69 1-9-70 3-21-70 11/17/70	TRANSISTOR & DIODE CONVERSION CHART DEC EIA DEC EIA				TITLE ADDRESS SELECTOR M105
		EQUIPMENT CORPORATION NATHAN, MASSACHUSETTS				
PRINTED CIRCUIT REV					NUMBER M105-0-1	REV. B

Table 3-3 (Cont)
Gating Control Signals

Mode Control C(1:0)	Byte Control A00	Gating Control Signals True (+3V)	Bus Sequence
10	1	OUT LOW OUT HIGH	DATO
11	0	OUT LOW	DATOB
11	1	OUT HIGH	DATOB

NOTE
Gating control signals may become true although select lines are not.

3.3.4.4 Specifications – The M105 output fanout is ten standard TTL loads for register select lines and eight standard TTL loads for gating control lines. The module is a single-height, 8.5-inch-long Flip-Chip. A circuit schematic for this module is shown in Figure 3-13. Note that pin A1 (EXT GND) must be grounded by the user.

3.3.5 M782 Interrupt Control Module

The M782 Interrupt Control Module provides the circuits and logic required to make bus requests and to gain control of the bus (become bus master). The module also includes circuits needed to generate an interrupt, if desired. The module contains two completely independent request and grant acknowledge circuits (channels A and B) for establishing bus control. The interrupt control circuit can be used with either, or both, of the request channels and provides a unique vector address for each channel. Figure 3-14 is a block diagram of the M782 Module, which is a single-height, 8.5-inch-wide Flip-Chip.

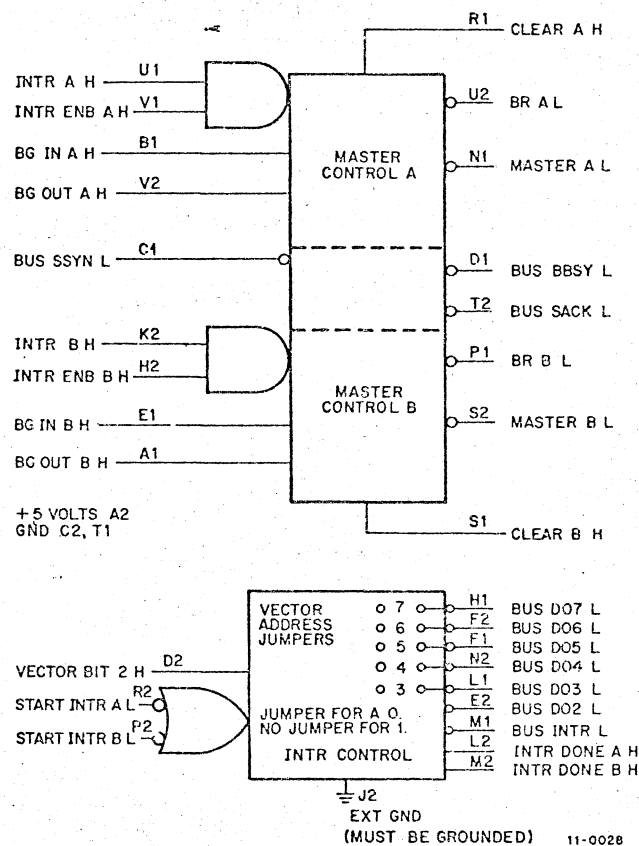


Figure 3-14 M782 Interrupt Control (block diagram)

The master control section (either channel A or B) is used to gain control of the bus. When the INTR and INTR ENB requesting inputs are asserted, a bus request is made on the BR level corresponding to the level of the BR line wired to the BR pin of the module. When the priority arbitration logic in the system recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the device has fulfilled all requirements to become bus master, the master control circuit asserts BBSY and then asserts a MASTER signal. (Refer to Section 2.4.1.)

Once the device has gained bus control by means of a BR request, an interrupt can be generated. If an interrupt is desired, the module is interconnected as shown in Figure 3-15. This figure illustrates the use of the two channels to first generate requests for bus control and then initiate interrupts. The request from channel A is a slightly higher priority than the channel B request because the bus grant signal first enters A, then enters B.

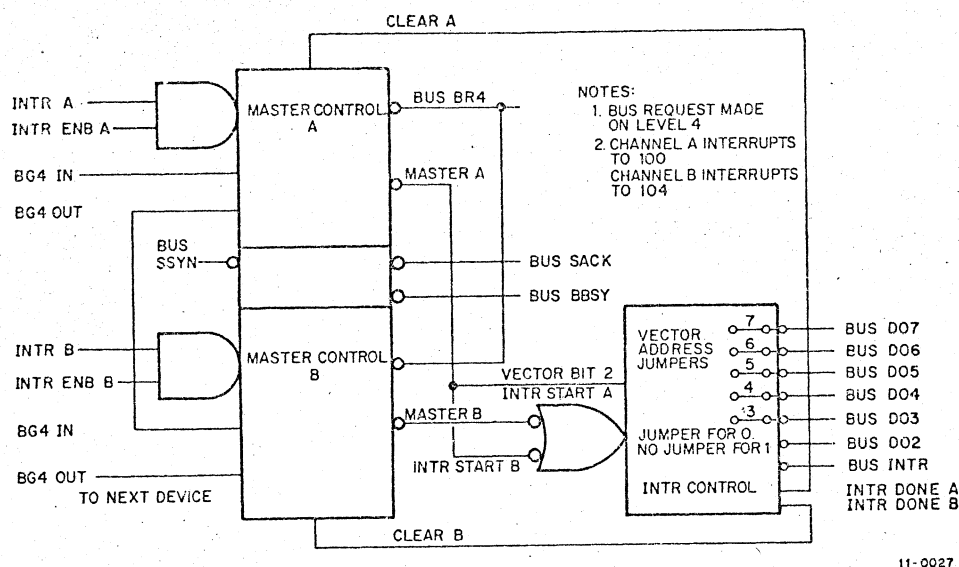


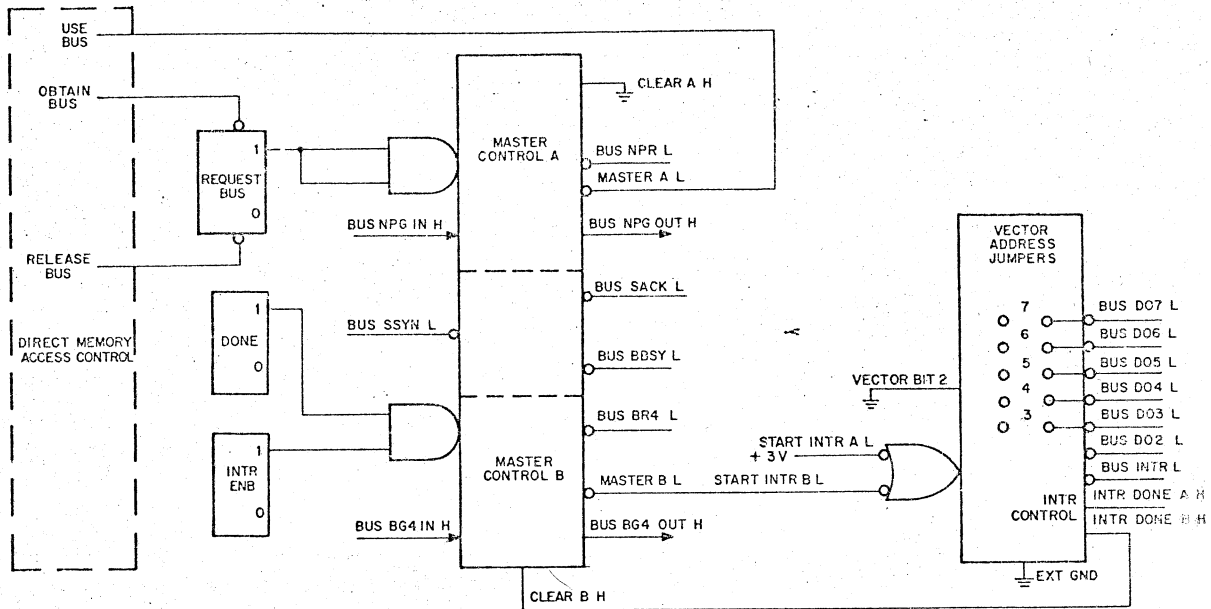
Figure 3-15 M782 Interconnection for 2-Channel Interrupt

The vector address is selected by jumpers on the M782 Module. Since the vector is a two-word (four-byte) block, it is not necessary to determine the state of bits 0 and 1. The six selectable lines determine the vector address. The least significant line is controlled by the VECTOR BIT 2 input signal. If this input is asserted, then bus line D02 is asserted. Thus, the interrupt on channel A uses a vector at location 100 and channel B uses a vector at location 104.

Figure 3-16 illustrates an M782 Module used for bus control in a device that directly transfers data to memory and then causes an interrupt when the transfer is completed. Channel A is connected to the NPR and NPG lines and is used to gain bus control for direct to memory, or device-to-device, transfers. Channel B is used to gain bus control for an interrupt.

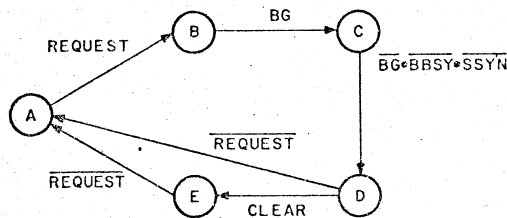
Each M782 Module master control section contains two flip-flops that sequence through four states, thereby controlling the request for bus control. Figure 3-17 is a state diagram of this sequence and Figure 3-18 shows a circuit schematic of the M782. The BG IN signal is allowed to pass through the module to BG OUT when the device is not issuing a request (state A), is master (state D), or has had the request honored (state E). To request bus use, the AND condition of INTR and INTR ENB must be satisfied. These levels must be true at least until the request is granted. Once bus control has been attained, it can be released by either asserting CLEAR or by negating either INTR or INTR ENB. The first method leaves the master control in state E, thereby inhibiting further bus requests

even if INTR and INTR ENB remain asserted. In order to make another bus request, INTR or INTR ENB must be dropped and then reasserted to cause the module to advance from state E through state A to state B where it asserts the request line. This prevents multiple interrupts when the master control is used to generate interrupts. The second method is used to release the bus after NPR use. Note that pin J2 (EXT GND) must be grounded by the user. A summary of all M782 signals is listed in Table 3-4.



11-0026

Figure 3-16 M782 Interconnection for Direct Memory Access



11-0026

Figure 3-17 State Diagram of Master Control

Table 3-4
Summary of M782 Signals

Signal	Assertion Level	Input Loading	Output Drive
INTR A, B	H	1 TTL (each)	
INTR ENB A, B	H	1 TTL	
CLEAR A, B	H	1 TTL	
MASTER A, B	L		10 TTL
START INTR A, B	L	2 TTL	
INTR DONE A, B	H		10 TTL
BG IN A, B	H	1 R*	
BG OUT A, B	H		2 D**
BR A, B	L		1 D
VECTOR BIT 2	H	1 TTL	
BUS SSYN	L	1 R	
BUS BBSY	L	1 R	2 D
BUS SACK	L		2 D
BUS INTR	L		1 D
BUS D(07:02)	L		1 D

*R = Standard Unibus receiver load.
**D = Standard Unibus transmitter (driver) output.

M7820 Interrupt Control

The M7820 is used in PDP-11 device interfaces. It consists of logic circuits that can be divided into three functional sections: Master Control A, Master Control B, and INTR Control.

The Master Control circuits are used to gain control of the UNIBUS for satisfying the need to either Gain direct memory access (DMA), or to perform the INTR bus operation which alters program flow.

To become master of the bus involves a question of priority. Briefly, this priority question is split into three phases:
 1) bus request lines, 2) processor's priority level, and 3) physical placement of a device on the UNIBUS.

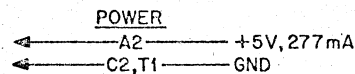
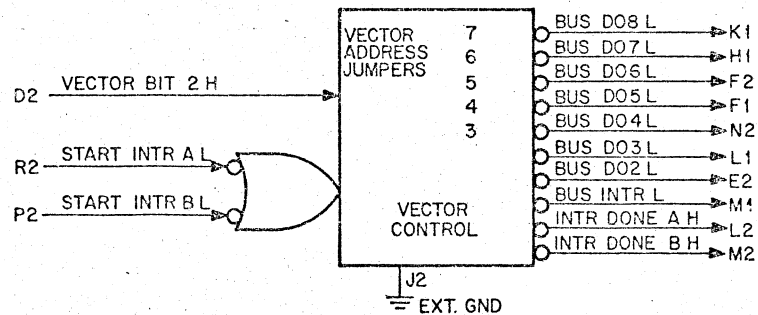
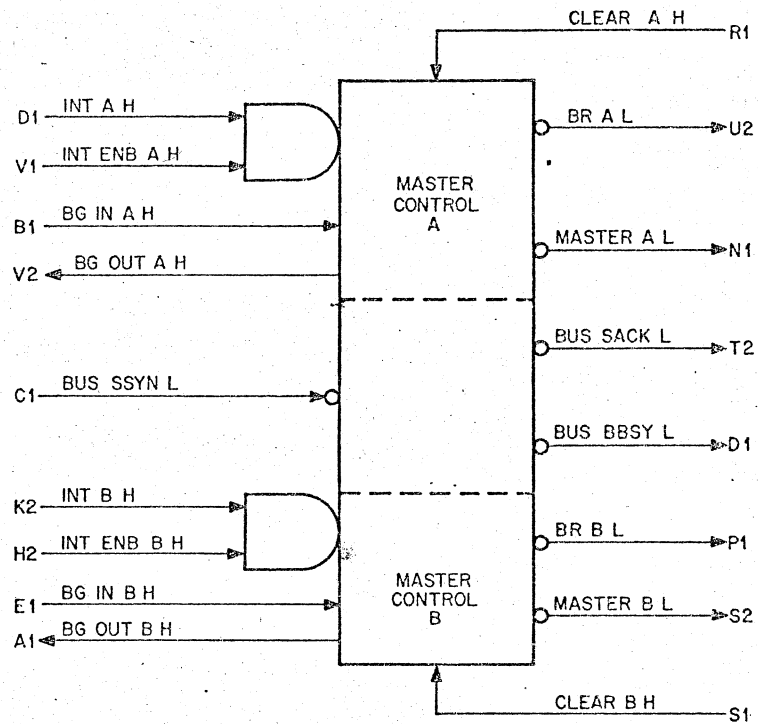
- 1) NPR (highest)
 BR7
 BR6 (except for trap instructions)
 BR5
 BR4 (lowest)

- 2) The processor acknowledges BR's of level $> N$:

where N is an Octal number in processor's status register. (NPR's are not affected.)

- 3) Highest priority goes to the device closest to the processor on the unique bus grant chain.

M7820 Interrupt Control

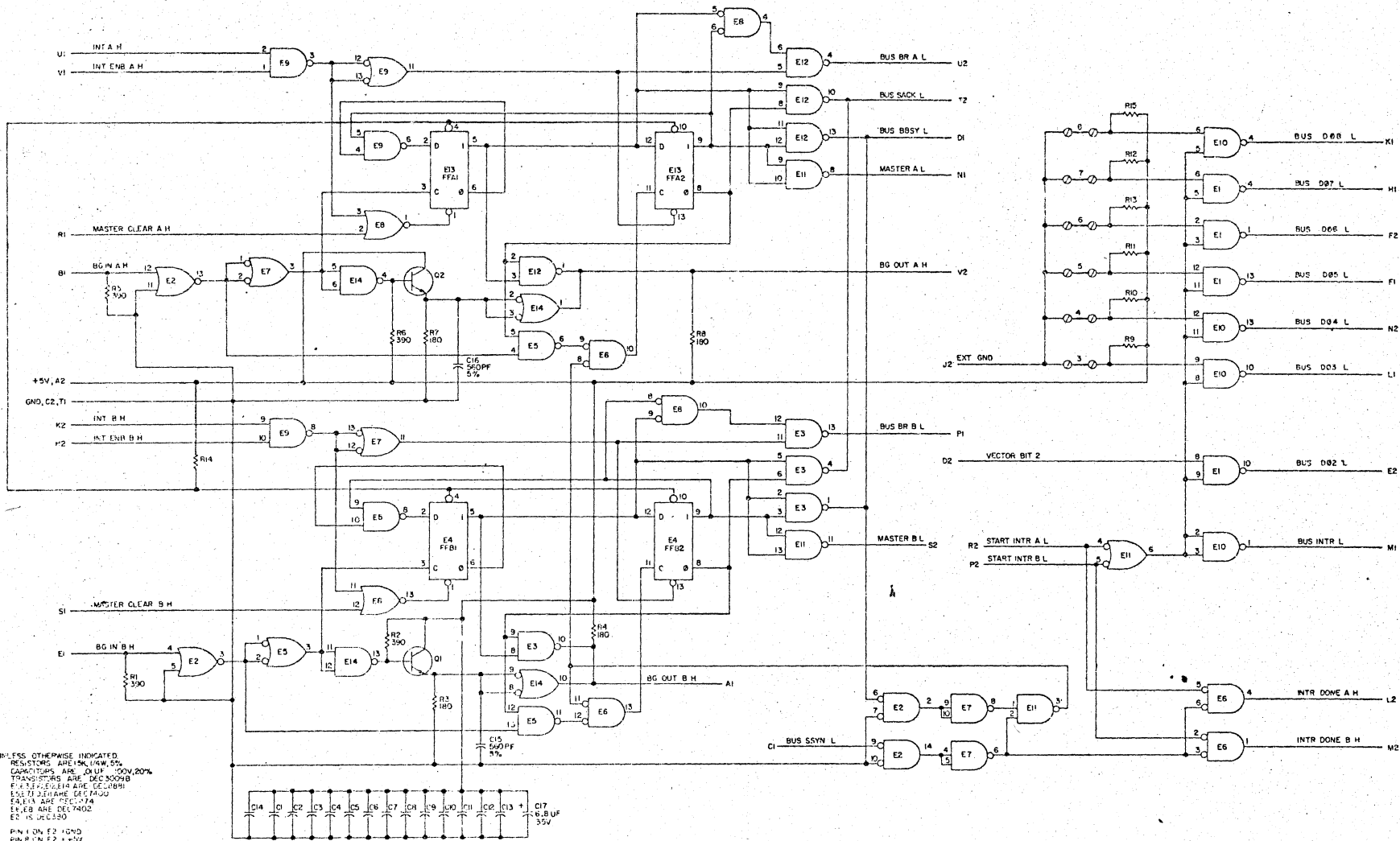


Theory of Operation

If a device wants control of the bus, it asserts both INT A and INT ENB A. Then a request is made on a BR. This then leads to priority determination and a BG results. Now the Master Control A responds with BUS SACK. The processor sees this acknowledgement and removes BG.

Printed Ckt. Rev.: C
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ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED. THE DIMENSIONS ARE APPROXIMATE. THE DIMENSIONS ARE APPROXIMATE. THE DIMENSIONS ARE APPROXIMATE.



UNLESS OTHERWISE INDICATED
 RESISTORS ARE 1/4W, 5%
 CAPACITORS ARE 50V, 20%
 TRANSISTORS ARE 2N3904
 E3, E4 ARE 7413
 E1, E2, E3, E4 ARE 7401
 E5, E6, E7, E8 ARE 7402
 E9, E10, E11, E12, E13, E14 ARE 7403
 E15 IS 7404
 PIN 1 ON E2, E4, E6
 PIN 1 ON E3, E5, E7, E9
 PIN 1 ON E1, E13, E14 - GND
 PIN 1 ON E11, E13, E14 - +5V
 ⊕ = SPLIT LEADS
 --- = JUMPERS

REV. 1
M7820-0-1

REV.	DATE	BY	CHKD.
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12	1/22/72	J. M. G.	J. M. G.
13	1/22/72	J. M. G.	J. M. G.
14	1/22/72	J. M. G.	J. M. G.
15	1/22/72	J. M. G.	J. M. G.
16	1/22/72	J. M. G.	J. M. G.
17	1/22/72	J. M. G.	J. M. G.
18	1/22/72	J. M. G.	J. M. G.
19	1/22/72	J. M. G.	J. M. G.
20	1/22/72	J. M. G.	J. M. G.

TRANSISTOR & DIODE CONVERSION CHART				
74xxx	DC	EMA	DC	EMA
7401	9013	9013	9013	9013
7402	9013	9013	9013	9013
7403	9013	9013	9013	9013
7404	9013	9013	9013	9013
7405	9013	9013	9013	9013
7406	9013	9013	9013	9013
7407	9013	9013	9013	9013
7408	9013	9013	9013	9013
7409	9013	9013	9013	9013
7410	9013	9013	9013	9013
7411	9013	9013	9013	9013
7412	9013	9013	9013	9013
7413	9013	9013	9013	9013
7414	9013	9013	9013	9013
7415	9013	9013	9013	9013
7416	9013	9013	9013	9013
7417	9013	9013	9013	9013
7418	9013	9013	9013	9013
7419	9013	9013	9013	9013
7420	9013	9013	9013	9013
7421	9013	9013	9013	9013
7422	9013	9013	9013	9013
7423	9013	9013	9013	9013
7424	9013	9013	9013	9013
7425	9013	9013	9013	9013
7426	9013	9013	9013	9013
7427	9013	9013	9013	9013
7428	9013	9013	9013	9013
7429	9013	9013	9013	9013
7430	9013	9013	9013	9013
7431	9013	9013	9013	9013
7432	9013	9013	9013	9013
7433	9013	9013	9013	9013
7434	9013	9013	9013	9013
7435	9013	9013	9013	9013
7436	9013	9013	9013	9013
7437	9013	9013	9013	9013
7438	9013	9013	9013	9013
7439	9013	9013	9013	9013
7440	9013	9013	9013	9013

TITLE: INTERRUPT CONTROL M7820
 DATE: 1/22/72
 DRAWN: J. M. G.
 CHECKED: J. M. G.
 APPROVED: J. M. G.
 CORPORATION: M7820-0-1
 PRINTED CIRCUIT BOARD

When BUS BBSY and BUS SSYN are negated, the Master Control A removes its BR and asserts BUS BBSY itself. It also asserts Master A when it is in control of the bus. Now the device can use the bus. To release control of bus, the device can assert CLEAR A or negate: INT A or INT ENB A. Master Control B is identical to A.

The INTR operation transfers a "vector address" to the processor. At this address is stored two consecutive words: 1) the starting address of the interrupt service routine, and 2) a status word. When the processor detects this, a trap sequence is initiated (current value of PC and current status of PS are stored and new ones are fetched). Now the interrupt service routine is executed.

To start the process: START INTR A or START INTR B is asserted. Then BUS INTR is asserted along with a 6-bit address. This is transferred onto the data lines: BUS D (08:02) providing a range of 000 to 774 (OCTAL) in increments of 4. D (08:03) are controlled by jumpers, which when "in", forces the bit to zero. The processor seeing BUS INTR asserts BUS SSYN. When this is detected, an INTR DONE A is asserted which negates the START INTR signal. This in turn negates BUS INTR, which negates BUS SSYN. As a result, a trap sequence is initiated. Vector bit-2 controls D02. When it is asserted D02 is asserted. It does not control any other bits.

LOGIC LEVEL 1 (high) > +3V at 40 μ A

LOGIC LEVEL 0 (low) < .4V at -1.6 mA

Input Loading: One TTL load (each)

INT A,B
INT ENB A,B
MASTER CLEAR A,B
VECTOR BIT 2

Two TTL loads (each)

START INTR A,B

One UNIBUS receiver
load* (each)

BG IN A,B
BUS BBSY
BUS SSYN

-25 mA (max.)

EXT. GND

*A UNIBUS receiver load is characterized at:

< 1.4V at 25 μ A (max.) Low level

> 2.5V at 160 μ A (max.) High level

Output Drive: Ten TTL loads (each)

One UNIBUS driver
load* (each)

Two UNIBUS driver
loads* (each)

MASTER A,B
INTR DONE A,B

BR A,B
BUS INTR
BUS D (08:02)

BUS SACK
BUS BBSY

BG OUT A,B

Power: +5 Volts at 277 mA (max.)

The grant chain to tie in the Master Control as follows:

BG IN has 390Ω to GND and BG has 180Ω
+5 Volts

EXT GND is used for testing purposes and should be tied to ground in normal operations.

Size: Extended length, single height, single width FLIP CHIP module.

*A UNIBUS driver load is characterized at:

< 0.8V at 50 mA (max.)
25 μ A (max.)

LOW LEVEL
Open collector leakage

Inputs			Outputs		
Signal	Connector	Pin	Signal	Connector	Pin
IN11	2	D1	OUT11	1	H1 ✓
IN12	2	H1	OUT12	1	D2 ✓
IN13	2	E2	OUT13	1	E1 ✓
IN14	2	B1	OUT14	1	D1 ✓
IN15	2	J1 & H2	OUT15	1	B1 ✓
REQUEST A	1	T2	NEW DATA RDY	1	V2*
REQUEST B	2	H2	DATA TRANSMITTED	2	V2*

OUT 7
OUT 15

*Pulse signals, approximately 2 μs wide.

Figure 2 shows the physical layout of the M786 and M927 modules.

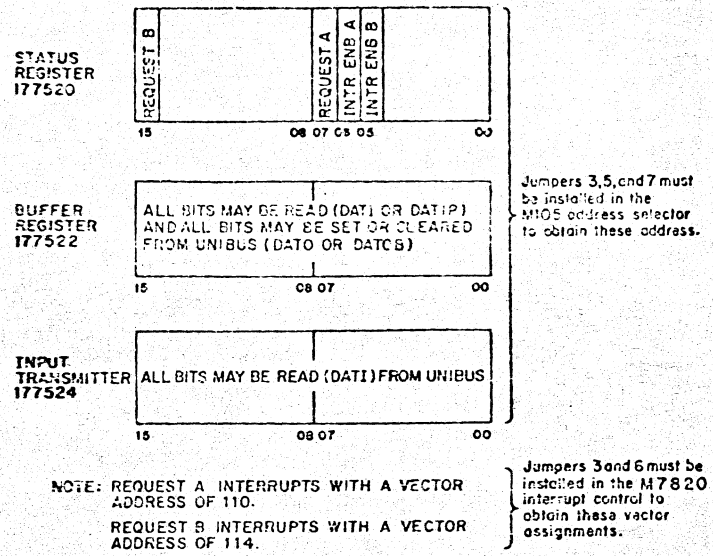


Figure 1 DR11-A Address and Bit Assignments

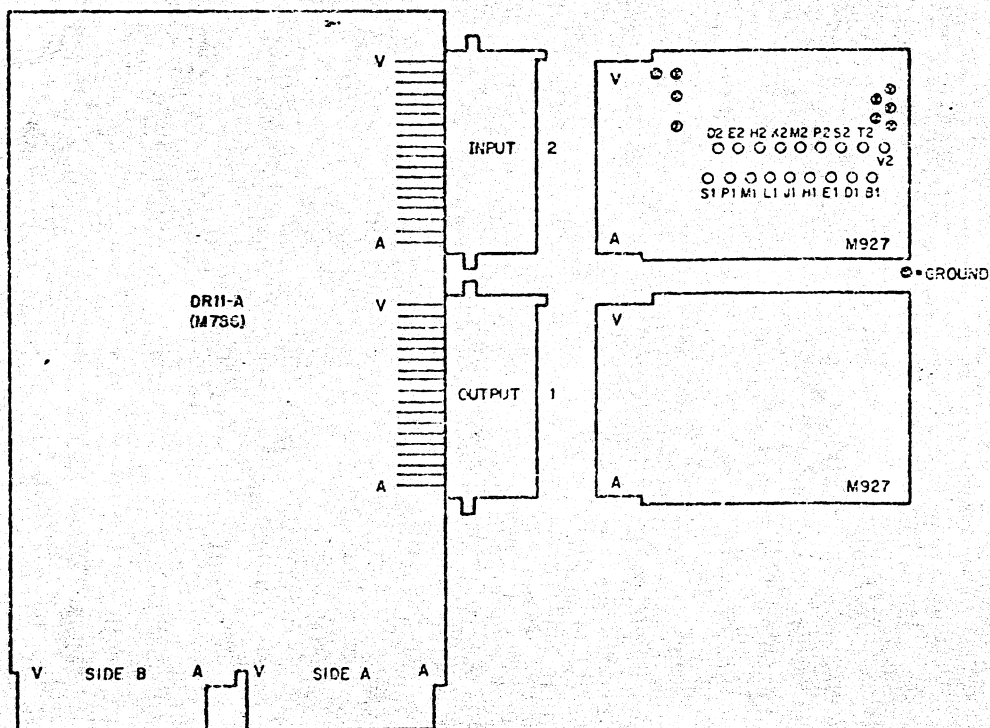


Figure 2 DR11-A Physical Layout

DR11-A General Device Interface

The DR11-A General Device Interface is a 3-module set that plugs into either a small peripheral slot in the processor or into one of four slots in a DD11 Small Peripheral Mounting Panel. The DR11-A provides the logic and buffer register necessary for transfers of 16-bit input and output data between the PDP-11 System and an external device.

The DR11-A contains three functional sections: a 16-bit buffer register, a 16-bit data input circuit, and a 2-channel flag and interrupt control. Address and bit assignments are shown in Figure 1. The DR11-A contains three physical modules: an M105 Address Selector, an M7820 Interrupt Control and an M786 General Device Interface with two M927 cable connectors.

The 16-bit buffer register is an addressable register that may be read or loaded by instructions transmitted through the Unibus (see Figure 1). The register outputs, together with a control signal pulse (NEW DATA READY) used to indicate that the register has been loaded from the Unibus, are available on a printed circuit edge connector #1 which is mounted on the M786 Module. All bits in the buffer register are cleared to 0s by the occurrence of an INIT signal on the Unibus. These signals are logic levels of either +3V (true) or 0V (false). The NEW DATA READY signal is a pulse which has a leading edge coincident with the loading of the buffer flip-flops. The connector accepts an M927 Cable Connector, which contains solder lugs and can be used with ribbon cable, twisted pair cable, or open wire. The M927 is electrically identical to the M904 Module described in the Logic Handbook.

The interface input circuits consist of 16 bus drivers gated to the bus when the input register is read by a DATI bus sequence (see Figure 1). The 16 input lines are +3V if true or 0V if false. These signals are also applied to the M786 Module through an M927 Cable Connector and a second printed circuit connector #2. When a DATI sequence occurs, a pulse signal (DATA TRANSMITTED) is applied to the external device.

Two additional request lines are furnished and may be asserted (+3V) by the external device to initiate an interrupt or to generate a flag that may be tested by the program. Whether these two request lines cause an interrupt is determined by two interrupt enable flip-flops which form part of the control and status register in the option (see Figure 1). The request lines form two more bits of the status register, independent of the status of the enable flip-flops; thus, they may be tested by the program.

The priority level of both interrupts must be the same, with interrupt A on a higher sublevel than interrupt B. The M786 contains a priority jumper plug which is normally set at BR5. The interrupt enable flip-flops are cleared to 0 (inhibit interrupt) by the occurrence of an INIT signal on the Unibus, or may be set or cleared by the program. Priority may be changed by the jumper plug.

The DR11-A pin assignments are listed in Table 1. All inputs are one standard TTL unit load. Inputs have diode protection clamps to ground and +5V. All signals are +3V if true. All outputs are TTL levels capable of eight unit loads. The new data ready and data transmitted signals are positive pulses, approximately 2 μ s in duration

Table 1
DR11-A Pin Assignments

Inputs			Outputs		
Signal	Connector	Pin	Signal	Connector	Pin
IN00	2	S1	OUT00	1	P2
IN01	2	S2	OUT01	1	M2
IN02	2	P1	OUT02	1	S1
IN03	2	L1	OUT03	1	P1
IN04	2	P2	OUT04	1	K2
IN05	2	K2	OUT05	1	M1
IN06	2	M1	OUT06	1	S2
IN07	2	T2	OUT07	1	L1
IN08	2	M2	OUT08	1	J1
IN09	2	D2	OUT09	1	H2
IN10	2	E1	OUT10	1	E2

(continued on next page)

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