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Technical Reference Guide

Compaq Armada 1700 Family of Personal Computers

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Compaq Computer Corporation

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Introduction

About This Guide

This guide provides technical information on the Compaq Armada 7800 Family of Personal Computers.

Additional Information Sources

Additional information on the products covered in this guide is available from manufacturer's data sheets, application notes, and published industry standards. Please refer to the sources listed below for additional information.

Publications

For more information on components used in products covered in this guide, refer to the following publications:

- Compaq Computer Corp. and others, *Serialized IRQ on the PCI Way*, version 5.4.
- Compaq Computer Corp., *Compaq BIOS Technical Reference Guide*, PN 074A/0693, Third Edition, Copy Date: June 1995.
- Hogan, Thomas, *The Programmers PC Sourcebook*, Microsoft Press, © 1991.
- IEEE, *IEEE 1284 Parallel Port Specification.*
- Intel Corp., *Mobile Pentium II Processor Data Sheets*.
- Intel Corp., *Mobile Pentium Processor with MMX Technology Data Sheets*, Copy Date: January 1997, Order No. 243292-001.
- Intel Corp., *Pentium Family User's Manual*, Document No. 241563-003.
- Intel Corp., *Pentium Processor Specification Update*, Copy Date: May 17, 1995.
- Intel Corporation, *Pentium Pro Family Developer's Manual*, Intel Corporation, 1996.
- Phillips Semiconductor, *I^2C Peripherals for Microcontrollers Data Book*, I^2C Protocol Reference.
- S3 Inc., *S3 Virge\MX™ Data Book*, Copy Date: July 1996, Document No. DB022-A.
- SMC Corporation, *Infrared Communications Controller Specification*, revision 1.30, November 1, 1995.
- SMC Corporation, *SMC37C957FR Data Sheet.*

Online Information

The following web sites may furnish additional information on products covered in this guide:

- www.compaq.com/support/techpubs/
- www.fapo.com/ieee1284.htm
- www.modems.com/general/mcglossary.html
- www.pc-card.org
- www.picmg.com
- www.s3.com
- www.smc.com
- www.ti.com

Notational Conventions

Values

I/O addresses and other values are in hexadecimal notation when shown with the letter "h" after them. Memory addresses are in hexadecimal notation when expressed as SSSS:OOOO (SSSS is a 16-bit segment and OOOO is a 16-bit offset). Other references are in binary notation when expressed as ones and zeroes with a trailing letter "b" after the value. All other numbers are in decimal notation.

Ranges

Ranges or limits for a parameter are shown as a pair of values separated by two dots. For example, 4. .0 includes numbers 4, 0 and every number in between (3, 2, and 1).

Signal Labels

Signal values are labeled A0, A1, A15, etc. Signal names are in uppercase letters. Signals that are negative true, or active low, are indicated in the text by an underscore (_) suffix.

Register Notation and Usage

The standard Intel naming conventions are used for the Pentium registers. EAX, EBX, ECX, EDX, EBP, ESP, ESI, and EDI are the names of the general registers used as double word-length registers (32-bit). AH, BH, CH, and DH are the names for the general registers used as high byte-length registers (8-bit); AL, BL, CL, and DL are the names for the general registers used as low byte-length registers (8-bit). SI, DI, and BP denote the source index, destination index, and base pointer registers, respectively.

CS, SS, DS, ES, FS, and GS denote the four segment registers: code segment, stack segment, and four data segments respectively. CS is used with the EIP (instruction pointer) register, and SS is used with the SP (stack pointer) register. EFLAGS is the 32-bit Flag register used to return the status of some operations. Status is given as the state of one of the flags within the register: CF for Carry Flag, IF for Interrupt Flag, etc.

System Overview

The Compaq Armada 1700 Family models are designed to operate using a 32-bit PCI architecture low-voltage technology, and a 233- or 266-MHz Pentium II processor. Standard features for all models include a keyboard with integrated pointing device and user-programmable keys, a Soundblaster compatible audio board, a modular MultiBay, optical disc bay, battery bay, and plug and play–supported dual 16-/32-bit PC Card slots. Model dependent standard features include a 13.3- or 12.1-inch color TFT XGA or 12.1-inch dual STN display, 32-MB Synchronous Dynamic Access Ram (SDRAM), and a 4.0-GB hard drive. Options include an integrated K56flex modem, a 24X max CD-ROM, and a DVD-ROM drive.

Desktop functionality is provided through the Convenience Base II.

All computer models may be set to operate under DOS, Windows, or other standard operating systems, and are Energy Star compliant. Not all operating systems or operating system versions support all hardware features of this computer

Figure 2-1. *Compaq Armada 1700 Personal Computer*

System Architecture

The Computer's system architecture is shown in Figure 2-2.

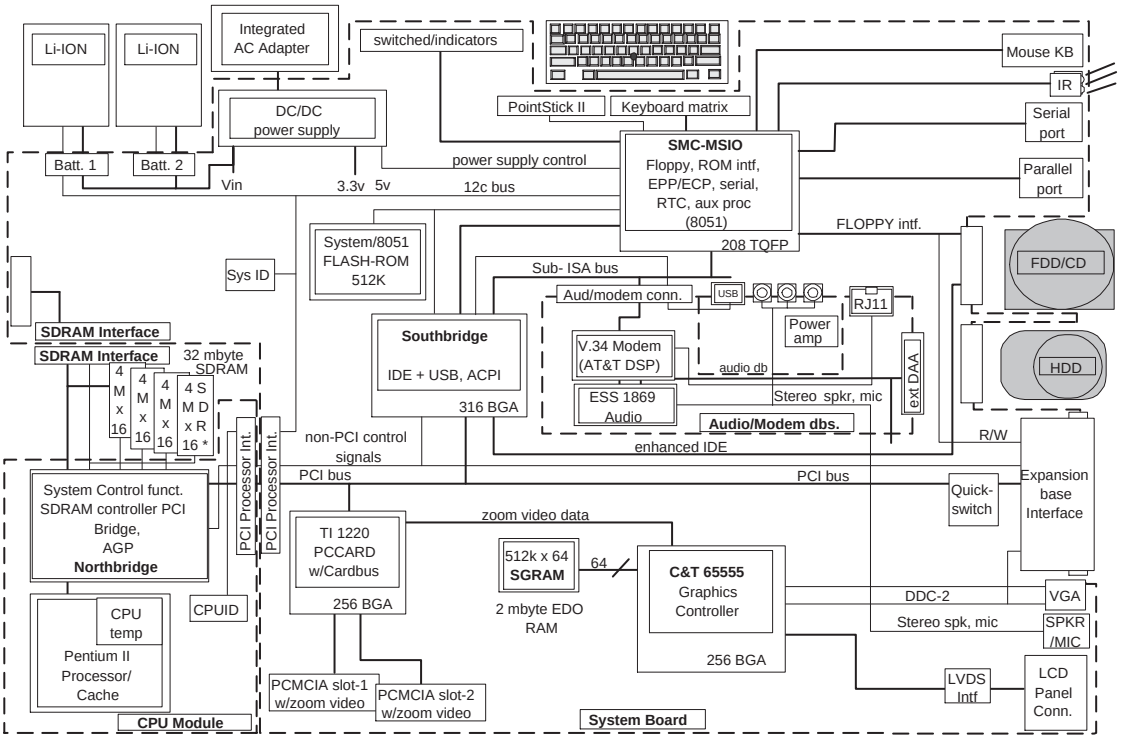


Figure 2-2. *Block Diagram*

Architecture

The computer architecture is composed of a 64-bit host bus, a 32-bit PCI local bus, and an 8-bit ISA bus. Host, memory, and PCI bus control is accomplished by the Intel 440BX Northbridge and Intel PIIX4E Southbridge. The processor board contains the microprocessor, the L2 cache, 32-MB system memory, and the Intel 440BX Northbridge.

System Memory

The first 32-MB of system memory resides on the system board. The expansion system memory is located on a single SODIMM. The memory is 3.3-VDC, SDRAM operating at host bus speed of 66-MHz.

Secondary L2 Cache

A secondary L2 cache memory system is integrated into the Pentium II processor sub-assembly. This memory consists of two burst-static-cache RAMS mounted in the processor cartridge.

Shared Flash ROM

The system flash ROM is capable of being written to, or "flashed," in order to be easily updated by using special BIOS update utility software (ROMPaq). The flash ROM containing the system BIOS code also provides non-volatile storage for the code used by the 8051 controller located in the super I/O device.

System Control

The Intel PIIX4E Southbridge contains the PCI to ISA bridge, two 82C59 Interrupt Controllers, the 82C54 timer, the IDE support logic, power management logic, and the USB controller with one USB port.

Peripheral Control

The SMC37C95xFR MSIO provides the remaining AT compatible 765A Floppy Disk Controller, two 16550A UARTS (one with IrDA encoding/decoding), printer port with extended capabilities including bidirectional high speed, EPP 1.7 and 1.9 modes, ECP mode, PC/AT mode, and PS/2 mode.

The MSIO contains an integrated 8051 microcontroller which provides PS/2 type serial interface ports for the internal pointing device and the external mouse/keyboard connectors. The 8051 also provides key scan circuits to scan the internal keyboard, and provides the system power management functions.

Mass Storage

The computer is equipped with one factory-installed 4.0-GB hard drive. The hard drive is designed for easy removal and upgrading. The drive type is automatically detected and configured by the system.

The diskette drive controller supports 3.5-inch,1.44-MB diskette drives. The diskette drive is provided as a standard MultiBay module. The MultiBay will also accept optional LS-120 diskette drive, Zip drive, a second battery pack or second hard drive. The optical disc bay is a dedicated bay that accepts a 5.25-inch, 24X max CD-ROM or DVD drive.

Video Graphics Subsystem

The video graphics subsystem consists of the C&T 65555 video graphics controller interfaced to the processor via the 33- MHz PCI bus, 2-MB of memory, and a 13.3-or 12.1-inch color TFT or 12.1 inch dual STN LCD. In addition to the integrated LCD panel, the graphics controller can also support either the Energy Star Monitor, Reduced Emissions Video Graphics Color Monitor, Video Graphics Color Monitor, or the Video Graphics Monochrome Monitor. Multimedia capabilities are provided by the C&T 65555™ video controller through a 16-bit Zoomed Video port.

PC Card Interface Control

Models provide two slots for installing either two Type I or Type II PC Cards, or one Type III PC Card. A single device controls the operation of two 32-bit, multiplexed, synchronous PC Card slots. The PC Card interface supports 3-v and/or 5-v PC Cards in a keyed socket that conforms to the PC Card Standard version 5.0. Both CardBus PC Card (32-bit mode) and 16-bit PC Card modes are supported to allow for bus mastering (32-bit mode) and Compaq PC Card DMA support (16-bit PC Card legacy mode) for peripheral devices such as memory or communications devices. The plug and play feature allows 16-bit PC Card(s) or CardBus PC Card(s) to be plugged into the system without powering down, reconfiguring, or rebooting the system.

I/O Interface

The I/O interface used in the includes a serial interface, a serial infrared interface, a parallel interface, and a Universal Serial Bus (USB) interface. These ports are configurable as COM1, COM2, COM3, or COM4, and LPT1, LPT2, and LPT3.

Audio Subsystem

The audio is derived from an ESS1869 audio controller, a TPA-0102 amplifier, and equalization circuitry. The audio subsystem is fully compatible with industry standard sound cards and the Microsoft Windows Sound System.

Modem Subsystem

The internal data/fax modem also provides RJ-11 and international DAA connectivity. The modem is a controllerless design capable of 56kbps.

Thermal Management

Thermal Management is implemented by a CPU temperature-control system that regulates the processor temperature through a temperature-controlled fan, a heat dissipating heat sink, processor clock modulation, and power management.

Power Subsystem

The power subsystem for the computer is made up of the following components:

- Internal AC/DC converter
- DC/DC converter providing outputs of:

  +3.3 V (4.0 A), +5 V (5.0 A), +12 V (0.075 A)

- Display inverter to generate high voltage for CCFL backlight.
- Power management controller

Power Sources

The computer derives power from the following power sources:

- Smart Li-Ion battery pack(s)
- AC from standard AC power lines
- Automobile/Aircraft adapter charger

Power Management

The power management feature allows the system to enter several levels of reduced power consumption initiated by the user through the keyboard or automatically during periods of reduced activity. Power Management is provided in both AC and DC power modes. Both Advanced Power Management (APM) and Advanced Configuration and Power Management (ACPI) are supported.

Security

The computer is protected against unauthorized access through user-selected password entry requirements and disabling techniques. Cable Lock and other hardware-locking provisions are available to prevent unauthorized removal of the computer, expansion/convenience bases, and/or devices.

Security is enhanced through additional password requirements for access to the computer or network and through device disabling for hard drives and I/O ports.

Intelligent Manageability

Insight Management Agents Version 3.51 is preinstalled. This version does include notification of battery charge faults and failures and external monitor fault alerts. This version is not Desktop Management Interface (DMI) 2.0 compliant.

Compaq will release an updated version of the Insight Management Agents that includes these new features. When available, this updated version will be available on the *Compaq Support Software CD*, or may be downloaded from the Compaq Web site at www.compaq.com/support/files.

NOTE: The installed version of the Insight Management Agents is DMI 2.0 compliant.

The version of Insight Management Agents installed on the Computer provides fault management capabilities that issue alert messages to notify the user of any impending hardware failures. Local and network alert notifications are displayed for SMART hard drive failures, memory changes, and system overheating. The Insight Management Agents also work with Compaq Insight Manager and other management applications used to remotely manage computers connected to a network.

For additional information on Intelligent Manageability please check out the following sources:

- Online information:
  - compaq.com: http://www.compaq.com/im/index.html
- Agent availability:
  - Downloads: http://www.compaq.com/support/files
  - *Support Software CD*

Expansion Support

The main system unit of the computer can be connected to the Convenience Base II for desktop functionality and expandability. The system unit can be used as a network-ready desktop system when connected to the convenience base . The convenience base provides a permanent desktop base for the system unit and eliminates device connection/disconnection problems. Connection to an external CRT and full-size keyboard and mouse are also provided, along with MIDI/joystick, stereo speakers, and port replication.

Specifications

Table 2-1
Computer Specifications

	U.S.	Metric
Dimensions		
Height	2.3 in	5.84 cm
Depth	9.6 in	24.5 cm
Width	12.5 in	31.75 cm
Weight		
With battery and optional CD-ROM	8.3 lbs	3.55 kg
Standalone (Battery) Power Requirements		
Nominal Operating Voltage (Li-Ion)	14.2	14.2
Nominal Operating Voltage (NiMh)	9.6	9.6
Maximum Operating Power	45 W	45 W
Peak Operating Power	50 W	50 W
Integrated AC Power Power Requirements		
Operating Voltage	100 to 240 VAC RMS	100 to 240 VAC RMS
Operating Current	1.1 A RNS	1.1 A RMS
Operating Frequency Range	47 to 63 Hz AC	47 to 63 Hz AC
Maximum Transient	4/50 kV	4/50 kV
Temperature		
Operating	5 to 95°F	10 to 35°C
Nonoperating	-4 to 140°F	-30 to 60°C
Relative Humidity (noncondensing)		
Operating	10 to 90%	10 to 90%
Nonoperating (t_W = 38.7°C max)	5 to 90%	5 to 90%
Altitude		
Operating	0 to 10,000 ft	0 to 3.15 km
Nonoperating	0 to 30,000 ft	0 to 10.14 km
Shock		
Operating	10 G, 11 ms, half sine	
Non operating	240 G, 2 ms, half sine	
Vibration		
Operating	0.55 G, 0.25 Oct/Min sweep rate	
Nonoperating	1.5 G, 0.5 Oct/Min sweep rate	

NOTE: Applicable product safety standards specify thermal limits for plastic surfaces. The Compaq Armada operates well within this range of temperatures.

Processor/Cache and System Support

Introduction

This chapter briefly describes the Mobile Pentium II processor (MP2) and two ASICs used on the Compaq Armada 7800 Family of Personal Computers. The ASICs include the Compaq Northbridge and Compaq Southbridge.

The computer system supports interchangeable CPU modules that plug into the CPU interposer board. The core logic on the CPU interposer board translates the processor bus interface into a PCI interface, an Accelerated Graphics Processor (AGP) interface, and a 64-bit DRAM interface to the system board.

This chapter describes the system processor, bus architecture, and system support consisting of the following devices:

- Processor/cache subsystem
- AGP bus overview
- PCI bus overview
- ISA bus overview
- Direct memory access
- Interrupts
- Interval timer
- RTC and configuration memory
- BIOS ROM
- System I/O map

Processor/Cache Subsystem

The computer is built with an MP2 and two Compaq ASICs—the Northbridge and Southbridge—that integrate a number of bus control and memory functions on the processor board. Refer to Figure 3-1 for a block diagram of the processor board.

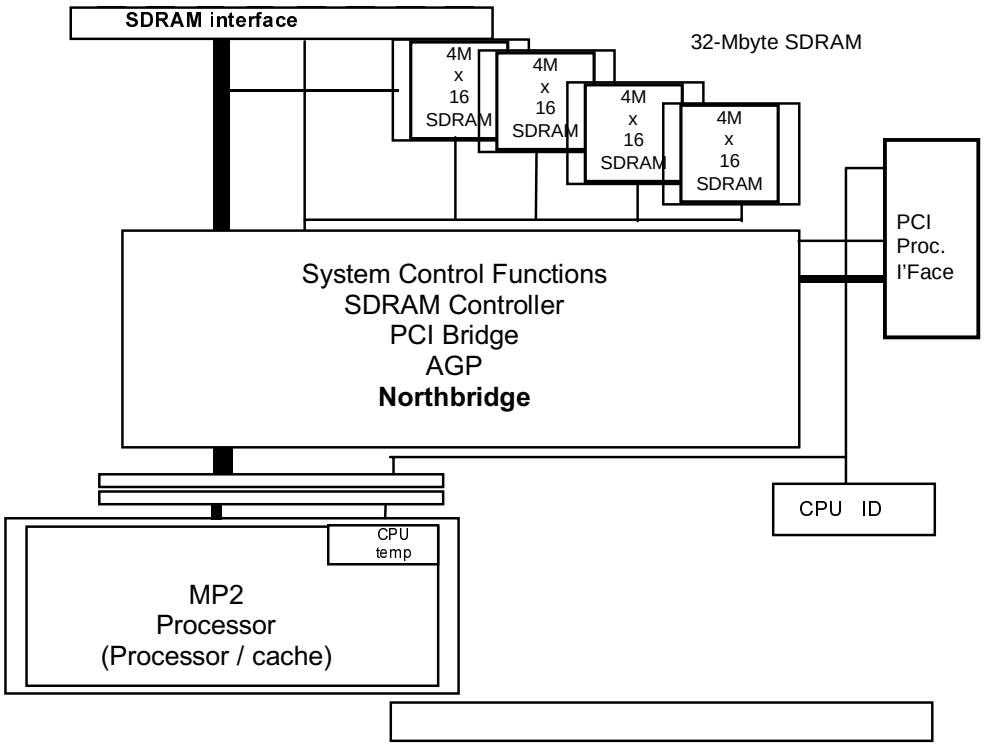


Figure 3-1. *Processor/Cache Subsystem Board, Block Diagram*

The mobile Pentium II processor is supplied as an integrated subassembly containing the processor, 512-KB L2 cache, and an integral processor temperature sensor. The module is supplied in a shielded cartridge with integral 240-pin Berg connector, providing a high-speed data bus interface to the system.

Mobile Pentium II Processor

The Mobile Pentium II (MP2) processor is object code compatible with software written for Intel 8086/88, 80286, 80386/486 DX/SX, 486 DX2, Pentium, and Pentium II processors. The MP2 processor has all the features of the Pentium II processor, plus voltage reduction technology and improvements in architectural design and other enhancements to provide substantially greater performance for graphics, video, and audio. The MP2 adds an integral L2 cache to the processor module for higher performance. A temperature monitor permits better thermal management in demanding environments.

Features provided by the mobile Pentium II processor include:

- Enhanced Pipelined Floating-Point Unit
- MMX technology
- Write-back MESI protocol for cache data
- Internal parity checking
- Execution checking
- Performance monitoring
- System Management mode
- Virtual mode extensions
- Fully compatible with MS-DOS, Windows, OS/2, and UNIX operating systems

New features provided by the mobile Pentium II processor include:

- Multiple Branch Prediction
  - Past history
  - Typical usage
- Reduced voltage technology
  - 1.8-, 2.0-, and 2.5-volt core voltage
  - 3.3-volt Vcc
- Separate internal 16-KB data and 16-KB instruction caches
- Superscalar architecture with:
  - Enhanced 12-stage pipeline
  - Two pipelined integer units capable of four instructions/clock
  - Pipelined MMX unit
  - Pipelined floating-point unit
- Advanced design features:
  - Pool of four write buffers used by both pipelines
  - Enhanced branch prediction
  - Virtual mode extensions
- On-chip module power-down capabilities for extended battery life
- Core frequency of 266-MHz at 66-MHz bus frequency
- Dual Independent Bus architecture
  - Processor to main memory bus
  - Processor to L2 cache bus
- Integral L2 cache
- Integral CPU Temperature monitor

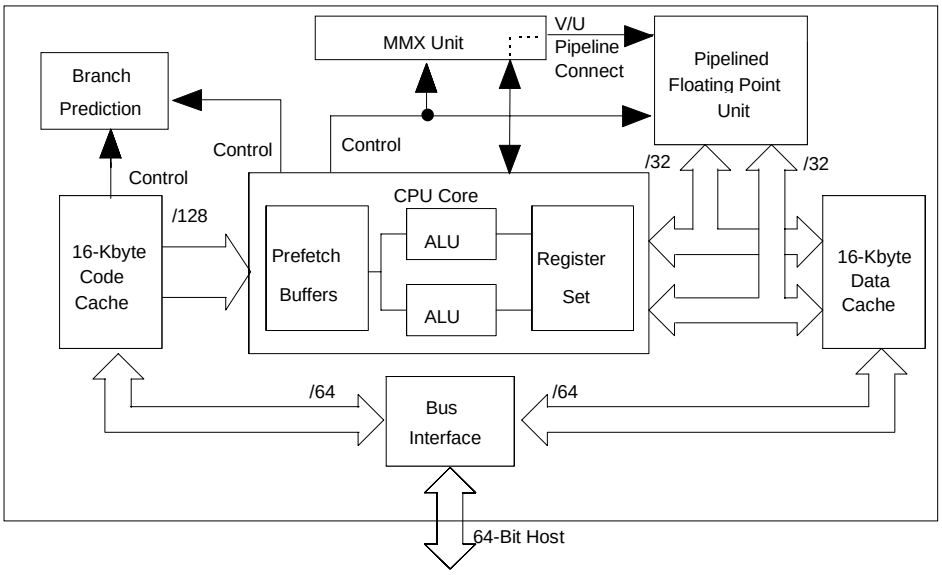


Figure *3-2.* *Mobile Pentium II Processor, Block Diagram*

The mobile Pentium II processor provides a 64-bit external data bus with the ability to pipeline all reads and a number of writes. The system memory interface architecture complements the microprocessor by reducing the number of wait states by the number of clocks pipelined for a given cycle.

The mobile Pentium II processor contains a 32-KB Level 1 (L1) cache. This cache is divided into 16-KB for code and 16-KB for data. The data cache is designed as a write-back cache, which means that data written from the CPU can be retained in the primary cache without being immediately passed on to the secondary cache or system memory, thus providing the CPU with a quicker turnaround in processing. The secondary cache and/or system memory is updated later when it is more convenient for the bus to handle the transfer.

Dual 12-staged pipelined architecture using dual-ALU operation provides 4 instructions-per-cycle performance. The prefetch buffer can hold more than 1 instruction and partially decodes 2 instructions at a time to determine if they can be processed in parallel.

If the two instructions are not reliant upon each other and meet other criteria, they are each routed simultaneously to a processing pipeline. Final decoding is completed, and the instructions are executed in the ALUs. The data cache is arranged as a two-way set-associative cache, so each way can service an ALU simultaneously if the two requested data are in different ways. Once an instruction completes a stage in the pipeline, that stage is free to accept another instruction.

CPU Modes

The Pentium II processor uses a CPU core that is compatible with software written for x86/88 microprocessors. The CPU core can operate in real, protected, or virtual mode. The microprocessors used in this system also support clock control and system management mode (SMM), during which power conservation operations are performed. The SM mode is discussed in the CPU Power Management Support subsection.

Cache Memory

The system uses a two-level (L1 and L2) cache system. The Pentium II processor includes 32-KBs of first-level (L1) cache memory that is divided into 16-KB halves. One half is designated as a code (instruction) cache, and the other half is designated for data. Each half operates as a two-way set-associative cache based on the modified/exclusive/shared/invalid (MESI) cache consistency protocol.

- Modified state: Indicates that the cache content of the indicated address is valid and has been written to more than once by the CPU. For a write-back cache, this means the cache contains the only valid data for this location, and the system memory contains obsolete data for that location.
- Exclusive state: Indicates that the CPU (L1) cache contains an exclusive copy of a location in system memory.
- Shared state: Indicates that both L1 and L2 caches contain copies of a location in system memory.
- Invalid state: Indicates that the current cache location contains obsolete data and should not be used.

If one cache has a modified or exclusive line, all matching lines in the other cache will be marked as invalid.

The code cache portion of the L1 cache is write-protected to prevent code from being inadvertently corrupted and supports the shared and invalid states of MESI. The data cache portion of the L1 cache supports all four MESI states.

The second-level (L2) cache memory includes 512 KB of two-way set-associative synchronous SRAM that works independently of the L1 cache and supports write-back operation. The L2 cache is located in the processor module.

Power Management Support

Mobile Pentium II processors support a system management mode (SMM) that is utilized by power management firmware to conserve power consumption and extend battery life. The SMM support package includes the following elements:

- System management interrupt (SMI), which is non-maskable and has the highest priority (even over the NMI). The SMI is delivered through the SMI pin only; APIC operation is not supported on this system.
- System management memory (SMRAM), which holds the SMI handler code and CPU state data. A status signal, SMIACT_, is provided to facilitate access to the SMRAM.
- Resume (RSM) instruction for exiting the SMM.
- I/O Restart and Auto Halt Restart features.

The SMM is initiated by an action that generates the SMI interrupt, which results in the following sequence:

1. The CPU asserts the SMIACT_ signal while in SMM to enable the SMRAM.
2. The CPU saves its state to SMRAM starting at base address 3FFFFh and works down as in a stack.
3. The CPU switches to SMM, which equates to real mode in the following areas:
   a. Address calculation
   b. GB limit checking
   c. Clearing of IF, TF, and DR7
   d. NMI disabling
   e. RSM instruction opcode becomes valid
4. The CPU jumps to the absolute address of 38000h in SMRAM to execute the SMI handler code and perform system management activities.
5. At its completion, the SMI handler executes the RSM instruction, which restores the CPU state from SMRAM, deasserts the SMIACT_ signal, and returns control to the previously interrupted program.

The chipset supports power management features similar to the Intel SL chip set. The most important features are the six programmable I/O break and activity timers that allow idle peripherals to be shut down. The controller uses the SMI interrupt to signal the microprocessor that the timeout has occurred. The ability to reduce the speed of the microprocessor when maximum power is not required is provided by the controller. The speed reduction is accomplished by generating a stop clock event. The duration of the event is programmable. The SMI handler is in a protected region of the ROM and operates independently of the operating system.

For further information concerning the mobile Pentium II processor, refer to *Mobile Pentium II Processor Data Sheets*, Intel Corp.

AGP BUS Overview

The Accelerated Graphics Port (AGP) bus provides a very high speed bus interface between system logic and the high performance S3 Virge/ MX graphics accelerator in the Armada 7800 Family of Personal Computers. AGP provides a dedicated, point-to-point 66-MHz bus interface between the CPU Northbridge logic chip and the graphics accelerator. The AGP bus definition was developed as a superset to the 66-MHz PCI revision 2.1 specification, but was redefined to allow for only one device, the system graphics accelerator.

The AGP graphics implementation in the Compaq Armada 7800 Family of Personal Computers enables improved performance in 2D and 3D graphics applications as well as host-based video applications such as software-based MPEG and DVD playback. By moving the data transfers for these applications from the shared, 133-MB/s PCI bus to a dedicated, 266-MB/s AGP bus, the Armada 7800 architecture eliminates a significant bottleneck of previous portable system designs and enables new performance levels to be achieved.

PCI Bus Overview

NOTE: This section describes the PCI bus in general and highlights bus implementation in this particular system. For detailed information regarding PCI bus operation, refer to the *PCI Local Bus Specification Revision 2.1*.

The standard PCI device configuration of the computer system has the processor/memory complex (via the CPU/PCI bridge) and the ISA bus (via the ISA/PCI bridge) connected to the PCI bus. PCI transactions occur synchronously with the host bus. The PCI bus operates at up to 33 MHz, providing 132-MB/s transfer performance. All I/O transactions involve the PCI bus. All ISA bus transactions with the microprocessor, cache memory, and/or system memory also involve the PCI bus. Memory transactions may or may not involve the PCI bus, depending on the source and destination.

PCI Bus Addressing

Four types of address cycles can take place on the PCI bus: I/O, memory, configuration, and special. Address decoding is distributed (left up to each device on the PCI bus).

Two types of address decoding are allowed on the PCI bus: positive and subtractive. Positive decoding provides higher performance because PCI devices respond immediately to an address within a certain range. For this system, most components on the PCI bus use positive decoding. Subtractive decoding is performed by the PCI/ISA bridge. A PCI device responds to its address by asserting the DEVSEL_ signal. The PCI/ISA bridge decodes subtractively and asserts the DEVSEL_ signal when no other PCI device responds to a cycle.

I/O And Memory Cycles

For I/O addressing, a standard 32-bit address decode (AD31..0) for byte-level addressing is handled by the appropriate PCI device. For memory addressing, PCI devices decode the AD31..2 lines for DWORD-level addressing and check the AD1,0 lines for burst (linear incrementing) mode. In burst mode, subsequent data phases are conducted a DWORD at a time with addressing assumed to increment accordingly (4 bytes at a time).

Conf*igur*at*i*on Cycl*e*s

Devices on the PCI bus must comply with PCI protocol that allows configuration of that device by configuration software. In this system, Configuration Mechanism No.1 (as described in the *PCI Local Bus Specification Revision 2.1*) is employed. This method uses two 32-bit registers for initiating a configuration cycle for accessing the configuration space of a PCI device. The configuration address (CONFIG_ADDRESS) register at IO address 0CF8h holds a value that specifies the PCI bus, PCI device, and specific register to be accessed. The configuration data (CONFIG_DATA) register at IO address 0CFCh contains the configuration data.

Conf*igur*at*i*on Add*r*ess R*egis*t*er*
I/O Po*r*t 0C*F*8h, R/W

BIT	FUNCTION
31	Configuration Enable 0 = Disabled 1 = Enabled
30..24	Reserved: read/write 0s.
23..16	Bus Number. Selects PCI bus to be used: Read/Write 0's.
15..11	PCI Device Number. Selects PCI device to be accessed (refer to Table 3-1).
10..8	Function Number. Selects function of the PCI device.
7..2	Register Index. Specifies configuration register to be accessed.
1,0	Config. Cycle Type ID: 00 = Type 0 (single PCI bus) 01 = Type 1 (multiple PCI buses)

Conf*igur*at*i*on Data R*egis*t*er*
I/O Po*r*t 0C*F*Ch, R/W

BIT	FUNCTION
31..0	Configuration Data

The PCI device number determines which one of the AD31..11 lines is to be asserted high for the IDSEL function. These address lines act as a chip select for the PCI device to be configured. Table 3-1 lists the device numbers.

Table 3-1
PCI Device Numbers

PCI Device	PCI Device Number	IDSEL Wired To:
CPU/PCI Bridge (MPC)	0 (00h)	AD16
ISA/PCI Bridge (MISC_L)	14 (0Fh)	AD30
Graphics Controller	13 (0Dh)	AD29
PC Card Controller	12 (0Ch)	AD28

The computer system in the standard system configuration contains only one PCI bus, so that the configuration cycle type bits (<1,0>) of CF8h will be "00" to initiate a Type 0 configuration cycle.

The function number is used to select a particular function within a multifunction PCI device.

The register index identifies the 32-bit location within the configuration space of the PCI device to be accessed. All PCI devices can contain up to 256 bytes of configuration data of which the first 64 bytes (00h-3Fh) comprises a predefined configuration space header. The remaining 192 bytes (40h - FFh) are optional and device specific.

The PCI components are typically configured during POST. Each PCI device is identified with a vendor ID (allocated by the PCI Special Interest Group) and a device ID (allocated by the vendor).

Special Cycles

Special cycles are similar to configuration cycles and are initiated by writing to CONFIG_ADDRESS (CF8h, Bus No. all 0s, Device = all 1s, Function = all 1s, and Register = all 0s) and CONFIG_DATA (CFCh) to generate a Type 0 configuration cycle (Figure 3-6). This Type 0 cycle, however, does not assert any of the IDSEL lines and therefore results in a master abort with FFFFh returned to the microprocessor.

Option ROM Mapping

During POST, the PCI bus is scanned for devices that contain option ROM. The scan procedure follows the standard PC BIOS scan procedure. Beginning at C000h, memory is probed at intervals of 2-KB for the signature 0x55h at offset 0, and 0xAAh in location offset 1. This search terminates at E800h (F000h - 2KB).

Option ROMs have the following header format:

Offset	Value	Description
00h	55h	First signature byte
01h	AAh	Second signature byte
02h	Size	Size of ROM modulo 512 (must round up to next 2K boundary)
03h	Entry	Start of installation subroutine (routine must have a far return)

The size of the ROM in bytes is divided modulo 512 and rounded up to the next 2K boundary. For example, a 47K video ROM would have to be rounded up to 48K and divided modulo 512 to produce a value of 96 (60h).

When the BIOS finds the ROM signature, it will add the bytes modulo 256 starting at offset 00h, and will produce an error message if the sum isn't zero. Otherwise it will make a far call to the entry point at offset 3, then continue searching for ROMs on the next 2K boundary.

Option ROM data, if detected, is loaded into system memory's DOS compatibility area (C8000h-DFFFFh). In the standard configuration, only the video subsystem is detected as having option ROM (32K) and is loaded into RAM starting at C0000h.

ISA Bus Overview

The ISA bus provides an 8-bit path for standard I/O peripherals as well as for optional devices that can be attached to the MultiBay Connector. Figure 3-3 shows the key functions and devices that reside on the ISA bus.

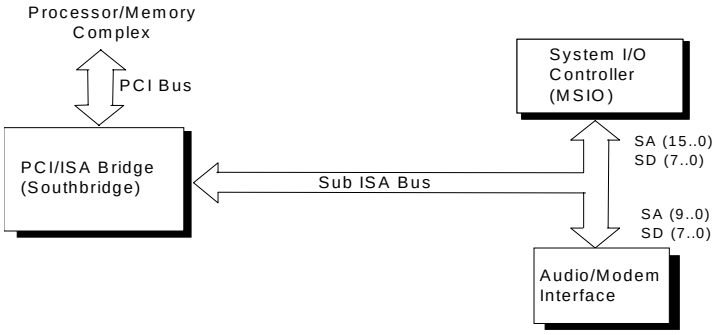


Figure *3-3.* *ISA Bus Block Diagram*

Devices limited to 8-bit transfers use data lines SD<7..0> and the following control lines:

- MRDC_ (memory read cycle low)
- MWTC_ (memory write cycle low)
- SBHE_ (byte high enable, accesses high byte)
- SA0_ (accesses low byte)
- IORC_ input/output read cycle low)
- IOWC_ (input/output write cycle low, to enable or latch data on the data bus)

Direct Memory Access

Direct memory access (DMA) is a method by which an ISA device accesses memory without involving the microprocessor. DMA reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks. DMA is normally used to transfer blocks of data to or from an ISA I/O device, but by implementation of Distributed DMA (DDMA) architecture, DMA devices are also allowed to exist on the PCI bus. The distributed DMA architecture is discussed later in the subsection "Distributed DMA."

The PCI/ISA bridge component includes the equivalent of two 8237 DMA controllers. The DMA circuitry is register-compatible with software written for AT-type systems.

Table 3-2 lists the default configuration of the DMA channels.

Table 3-2
Default DMA Channel Assignments

DMA Channel	Function
Cntlr 1 - Byte Transfers:	
0	Audio Controller
1 (Default)	Audio Controller
2	Diskette Drive
3	EPP Parallel Port
Cntlr 2 - Word Transfers:	
4 (0)	Cascade from Controller 1
5 (1)	Fast Infrared (8-bit Mode) EISA Ext.
6 (2)	Spare
7 (3)	Spare

NOTE: 1. Speakerphone uses one audio channel for Tx and the other for Rx.
2. Channel numbers in parentheses are channels in MISC.

All channels in Controller 1 (channels 0, 1, 2, and 3) operate at a higher priority than those in Controller 2 (channels 5, 6, and 7). Channel 4 of Controller 2 is not available for normal DMA. Unlike the CPU, DMA Controller 2 can transfer words only on an even address boundary. The DMA controller and page register define a 24-bit address that allows data transfers within the address space of the CPU. The DMA controllers operate at 8 MHz.

DMA Memory Page Register

The DMA memory page register contains the 8 most-significant bits of the 24-bit address. It works in conjunction with the DMA controllers to define the complete (24-bit) address for the DMA channels. Table 3-3 gives the port address assigned to each page register.

Table 3-3
DMA Port Addresses

DMA Channel	Page Register I/O Port Address
0	087h
1	083h
2	081h
3	082h
4	None
5	08Bh
6	089h
7	08Ah
Refresh	08Fh (See Note)

NOTE: The DMA memory page register for the refresh channel must be programmed with 00h for proper system operation.

The memory address is derived as follows:

24-Bit Address - Controller 1 (Byte Transfers)

8-bit Page Register	8-Bit DMA Controller
A23..A16	A15..A0

24-Bit Address - Controller 2 (Word Transfers)

7-bit Page Register	16-Bit DMA Controller
A23..A17	A16..A1, A0 always 0

A16 from the DMA Memory Page register is disabled when DMA Controller 2 is selected. A0 is not connected to DMA Controller 2 and is always 0 when word-length transfers are selected. Not connecting A0 means that the size of the block of data that can be moved or addressed is measured in 16-bit words, rather than 8-bit bytes, and the words must always be on an even boundary.

DMA Controller 1 can move as much as 64 KBs of data per DMA transfer. DMA Controller 2 can move as much as 64K words, or 128 KB of data per DMA transfer. Word DMA operations are only possible between 16-bit memory and 16-bit peripherals.

Distributed DMA

The distributed DMA architecture provided by the PCI/ISA bus bridge device allows the individual DMA controller channels to be distributed between all PCI devices as well as ISA bus devices. The I/O address space for each channel is separated into a consecutive 16-byte block, which is then mapped, relative to a base address, into the 64-KB I/O address space. A new distributed master DMA interface ties the old and new I/O registers together and will control all reads and writes to any legacy DMA I/O register.

The DDMA registers are defaulted to I/O memory space 0800h - 087Fh. The base address for these registers are programmed in the system unit PCI/ISA bridge device and are programmable to be any contiguous 128-byte block on even boundaries, i.e., 0, 80, 100, 180. The DDMA registers are distributed throughout the system according to the DMA channel used by the individual PCI device.

The PCI/ISA bus bridge device can be configured to be a master DMA by setting bit 31 in the PCI distributed DMA configuration register. When the PCI/ISA bus bridge device is enabled as a master DMA controller it will monitor all PCI I/O reads and writes to all Legacy DMA registers. Both the system PCI/ISA bus bridge device and the expansion base PCI/ISA bus bridge device use all seven DMA channels. It is up to the software to ensure that the same DMA channels are not enabled in both PCI/ISA bus bridge devices.

The monitored cycles are controlled as shown in the following list:

1. A PCI I/O cycle is initiated on the PCI bus with a legacy DMA when a read/write to a Legacy DMA register is attempted by the CPU bridge device. The master DMA uses the “Retry Engine” and takes control of the cycle by driving DEVSEL_ to request the PCI bus and issues a “retry” to terminate the cycle after IRDY is activated.
2. The request by the CPU bridge device is then immediately masked by the PCI arbiter.
3. The master DMA runs up to seven PCI I/O byte reads/writes after being granted the PCI bus. PCI bus multibyte access is serviced to completion one byte at a time.

4. The master DMA will set an internal completion flag at the end of the first read/write cycle, the request CPU pin is unmasked, and the master DMA interface relinquishes control of the PCI bus. The master DMA waits for the retried PCI I/O read/write from the CPU bridge device.
5. Access to Legacy DMA Registers from sources other than the host bridge device will be serviced normally by the master DMA. The PCI I/O read/write cycle is reinitiated and the data is returned by the master DMA for a read. For a write that is initiated after IRDY is activated, the cycle is terminated and will reset the internal flag.

The DMA Master Configuration Register is described as follows:

Address: 08Ch-08Fh, R/W, Reset Value: 00000000h

BIT	FUNCTION
31	Master DMA enabled 0 = Disabled 1 = Enabled
30..8	Reserved - read/write 0s.
7..5	Identifies active DMA channel in PCI/ISA bridge device. One bit per channel. 0 = Distributed Legacy DMA Channel 1 = Local Legacy DMA Channel
4	Reserved - read/write 0s.
3-0	Identifies active DMA channel in PCI/ISA bridge device . One bit per channel. 0 = Distributed Legacy DMA Channel 1 = Local Legacy DMA Channel

NOTE: Bits 0-3 and 5-7 are tied to their corresponding DMA Slave Configuration Register. Therefore, a write or read from either location will automatically be reflected in the other register on read.

Refresh Operations

The RAM refresh is designed to perform a memory read cycle on each of the 512 row addresses in the DRAM memory space. Refresh operations are used to refresh memory on the 64-bit memory bus. The remaining address lines are in an undefined state during the refresh cycle. Hidden refresh of the DRAM is performed in the system while refresh timing on the ISA bus of the expansion base is set by the Refresh Count Value Register in the PCI configuration space of the MISC-E device.

Int*erru*pts

The Interrupts used in the Armada 7800 Family of Personal Computers are serialized as shown in Figure 3-4. The PCI and ISA interrupts are routed to the PCI/ISA bridge device on the expansion base, where they are serialized onto a single wire bus to the PCI/ISA bridge device in the system unit. They are then MUXed with the system unit IRQs and fed to the interrupt controller.

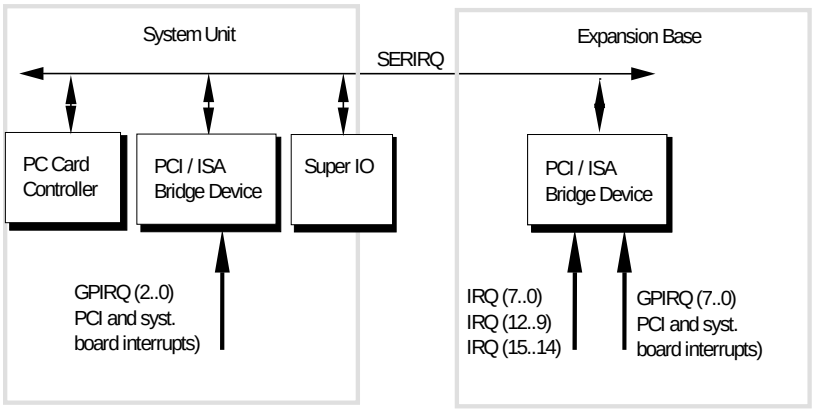


Figure *3-4.* *SER IRQ Serial Interrupt Bus Architecture, Block Diagram*

The GPIRQ pins are mapped by the same mapping logic in both the system unit and expansion base PCI/ISA bridge devices to any ISA IRQ with the exception of IRQ0, IRQ1, IRQ2, IRQ8, and IRQ13. The mapped IRQs, standard IRQ pins, and internal interrupts are ANDed by both PCI/ISA bridge devices. The data is then serialized and placed on the serial bus. The output of the serial bus is sent by the system unit PCI/ISA bridge device to the Edge/Level Control registers and then to the 8259 interrupt controllers.

For further information concerning Serialized Interrupts, refer to the joint publication by Compaq and other companies titled *Serialized IRQ on the "PCI Way"* Version 5.4.

The Interrupt Index Register and Mapping Registers are described as follows:

Interrupt Index Register
Address: AEh, R/W, Reset Value: 0000h

BIT	FUNCTION
7..3	Reserved - read/write 0s.
2..0	GP_IRQ Index. Specifies GPIRQ pins for mapping in the Interrupt Mapping Register. GPIRQ 3 & 4 are IDE interrupts. Only index values 0-5 are valid. 000 = GPIRQ 0 011 = GPIRQ 5 (Expansion PCI/ISA bridge device only) 001 = GPIRQ 1 100 = GPIRQ 6 (Expansion PCI/ISA bridge device only 010 = GPIRQ 2 101 = GPIRQ 7 (Expansion PCI/ISA bridge device only)

Interrupt Mapping Register
Address: AFh, R/W, Reset Value: 01h

BIT	FUNCTION
7..4	Interrupt Map Value represents which IREQ controller is mapped by the GP_IRQ in the Interrupt Index Register. Interrupts 0.1, 2, 8, and 13 are reserved.
3..1	Reserved - read/write 0s.
0	Interrupt Disable 1 - The selected interrupt is disabled 0 - The selected interrupt is enabled

The Interrupt Edge Level Control Register is described as follows:

Edge Level Control Register
Address:04D0h, R/W, Reset Value: 0000h

BIT	FUNCTION
15..14	INT 15/INT 14 Level Mode 0 = Edge Mode 1 = Level Mode
13	Reserved - read/write 0s.
12..9	INT 12/INT 9 Level Mode 0 = Edge Mode 1 = Level Mode
8	Reserved - read/write 0s.
7..3	INT 7/INT 3 Level Mode 0 = Edge Mode 1 = Level Mode
2..0	Reserved - read/write 0s.

Nonmaskable Interrupts

The microprocessor uses two basic types of interrupts: maskable and nonmaskable. A nonmaskable interrupt cannot be masked off within the processor, but may be masked under software control using additional logic on the system board. A maskable interrupt can be enabled or disabled by the microprocessor using the STI and CLI instructions.

There are two interrupt signals that are nonmaskable by the microprocessor: the SMI_ and NMI signals. The SMI_ signal is used for power management and is discussed in Appendix B, "Power Conservation." This section describes the NMI signal. An NMI signal is caused by:

- Parity errors on any expansion boards that pull the IOCHK_ line low
- Parity errors detected on the PCI bus including Special Cycles
- Parity errors detected on the PCI bus (except Special Cycles)

When an NMI is caused by hardware, register 61h indicates the source of the interrupt. Bits set to 1 in port 61h show which device requested an NMI. After the NMI routine processes the interrupt, the NMI status bits [7, 6] are reset.

If bit [6] is set, the interrupt comes from the hardware IOCHK_ line. To reset the hardware IOCHK_ latch, pulse bit [3] of port 61h high.

If bit [7] is set, the interrupt comes from a processor board parity error. To reset the parity error latch bit, pulse bit [2] of port 61h high.

The registers that affect NMI generation are described in the following paragraphs.

NMI Status Register

This register provides various functions including those related to the NMI. Note that bits 7..4 are meant as read-only bits.

NMI Status Register Address: 061h

BIT	FUNCTION
7	SERR_ NMI Source Status: RO 0 = No NMI from system board parity error 1 = NMI requested
6	IOCHK_ NMI Source Status: RO 0 = No NMI from IOCHK_ 1 = IOCHK_ is low (active), NMI requested, read only
5	Timer Counter 2 OUT Status: RO State of the interval timer 1, counter 2 output signal (speaker), read only
4	Refresh Cycle Toggle: RO This bit toggles with every refresh.
3	IOCHK_ NMI Enable: RO 0 = IOCHK_ NMI enabled 1 = IOCHK_ NMI disabled and cleared, read and write
2	System Board PCI SERR#NMI Enable: RW 0 = Parity error NMI enabled 1 = Parity error NMI disabled and cleared, read and write
1	Speaker Data Enable: RW 0 = SPKR output is 0 1 = SPKR output is the value of Counter 2 OUT
0	Timer Counter 2 Enable: RW Gate signal for interval timer, counter 2 (speaker) 0 = Counter 2 disabled 1 = Counter 2 enabled

NMI Enable Register

The Mask register for the NMI interrupt is at I/O address 70h shown below. Writing 80h to this port masks the NMI from all sources. Note that if the NMI is masked, the non-maskable interrupt from the NMI port, the Bus Master Timeout, and the Fail-Safe Timer will not be generated and the appropriate bits in register 061h will not be set. Even if NMI is masked, the proper bits for the IOCHK_ and parity error bits in register 061h will be set. If NMI is not masked and these bits are set, then NMI will be generated at that time.

This port is shared with the real-time clock and configuration memory device (the lower 7 bits). Do not modify the contents of this register without considering the effects on the state of the other bits. Refer to the "Real-Time Clock and Configuration Memory" subsection on the usage of I/O address 70h for time and system information.

NMI Enable Register Address: 070h

BIT	FUNCTION
7	0 = NMI enabled 1 = NMI disabled
6..0	Real-time clock

Maskable Interrupts

All maskable (hardware) interrupts generated by PCI and ISA peripherals are channeled through 8259-type interrupt control logic that is integrated into the PCI/ISA bridge device. PCI interrupts are applied to the PCI interrupt redirect logic. The redirect logic maps the PCI interrupts to selected ISA (IRQ) interrupts. The IRQn interrupts are then processed as in standard AT-type systems, with the microprocessor responding to the active INTR signal.

The maskable interrupt logic is register-compatible with software written for standard AT-type systems.

Table 3-4 lists the 15 possible sources for maskable interrupts and their priorities. The highest-priority interrupt is processed first.

Table 3-4
Maskable Interrupt Priorities and Sources

Priority	Label	Controller	Typical Interrupt Source
1	IRQ0	1	Interval timer 1, counter 0 output (System Timer)**
2	IRQ1	1	Keyboard Controller
3	IRQ8	2	Real-time clock (RTC)
4	IRQ9	2	Expansion Bus pin B04*
5	IRQ10	2	Expansion Bus pin B03*
6	IRQ11	2	Expansion Bus pin D04*
7	IRQ12	2	Mouse Controller/Expansion Bus pin D05*
8	IRQ13	2	Coprocessor error**
9	IRQ14	2	IDE Controller /Expansion Bus pin D07*
10	IRQ15	2	Expansion Bus pin D06* Secondary IDE Controller
11	IRQ3	1	Serial (infrared) port 1(COM2)/ Expansion Bus pin B25* (Modem Only)
12	IRQ4	1	Shared Serial (RS-232) port 2 (COM3) (COM1)/Expansion Bus pin B24*
13	IRQ5	1	Parallel Port 2/Expansion Bus pin B23* (Audio)
14	IRQ6	1	Diskette drive controller/Expansion Bus pin B22*
15	IRQ7	1	Parallel Port 1/Expansion Bus pin B21*
--	IRQ2	1	Interrupt from Controller 2 (cascaded)

* Expansion Base PCI/ICS bridge device pin.
**System Unit PCI/ICS bridge device (internal).

The Numeric Coprocessor Interrupt is created by synchronizing FERR with PCICLK to generate IRQ13.

Interval Timer

The purpose of a programmable interval timer is to generate pulses at software controllable intervals. This system uses one 8254-compatible timer in the PCI/ISA bridge device that provides three counters. Table 3-5 lists the interval timer functions.

Table 3-5
Interval Timer Functions

Counter	Function	Gate	Clock In	Clock Out
0	System Clock	Always On	1,193 MHz	IRQ0
1	Not Used	N/A	N/A	N/A
2	Speaker Tone	Port 61, bit [0]	1,193 MHz	Speaker Input

Counter 0 provides a system interrupt for the time of day, diskette timeout, and other system functions. Counter 2 generates the tone for the "beep" speaker. The output to the speaker is enabled by ANDing it (SPKCLK) with Port 61h bit [1]. The output of the counter can be read at Port 61h bit [5] (regardless of enable bit [0] status). See the Port 61h bit descriptions under "Nonmaskable Interrupts" in this chapter for more information. To minimize power dissipation in the speaker, the speaker output should be left high (port 61h, bit [1] set to 1) when not in use.

The facilities available for programming the timers include:

- Control Word specifies:
  - which counter to read or write.
  - the operating mode.
  - the count format (binary or BCD).
- Counter Latch latches the current count so that it can be read by the system; the countdown process continues.
- Read Back reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 3-6
Interval Timer Port Functions

Port	Function
40h	Read or Write count for counter 0 (system clock)
41h	Read or Write count for counter 1 (refresh request)
42h	Read or Write count for counter 2 (speaker tone)
43h	Control Word Register

Real-Time Clock and Configuration Memory

The real-time clock (RTC) is compatible with the MC146818 device. The auxiliary battery is used to provide power to the RTC and the configuration data stored in EEPROM. When fully charged and all other power sources are disconnected, the date and time are held for at least one month.

The first 14 memory locations of configuration memory are used for the RTC. The remaining memory locations are used for system configuration.

All registers are read/write except:

- Status registers C and D, which are read only.
- Bit[7] of status register A, which is read only.
- The high-order bit of the seconds byte, which is read only.

Figure 3-5 shows the memory map for the real-time clock.

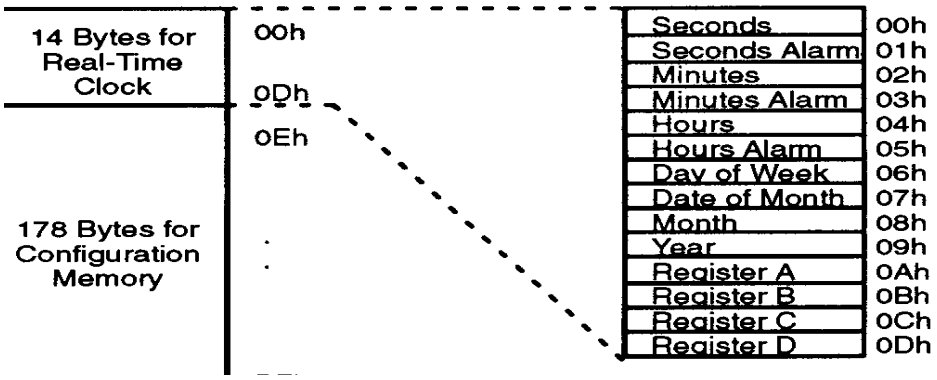


Figure *3-5.* *RTC/Configuration Memory Map*

To reset the time or system configuration, run the Compaq SETUP Utility or use the appropriate INT 1Ah (BIOS) command. The TIME and DATE commands of DOS 3.31 or the date/time properties window of Windows 95 also update the RTC.

The RTC is an I/O-mapped device using indirection (see below).

To write a value into configuration memory:

1. Use OUT 70h, AL to specify the memory location to change. 70h is the port number; AL is the memory location.
2. Use OUT 71h, AL to specify the data for the memory location. 71h is the port number; AL is the data.

To read the contents of a memory location:

1. Use OUT 70h, AL to specify the memory location to read. 70h is the port number; AL is the memory location.
2. Use IN AL, 71h to read the data stored in that location. The returned data is placed in the AL register of the processor.

The port 70h is shared between the NMI Mask register and the Configuration Memory Address register. To leave the NMI Mask enabled, write a “0” to bit [7] of the RTC address

Table 3-7 summarizes the types of information stored in the RTC and Configuration memory locations.

Table 3-7
Real-Time Clock and Configuration Memory Locations

Register	Function	Register	Function
00h	Seconds	14h	Equipment installed
01h	Seconds Alarm	15h, 16h	Base memory size
02h	Minutes	17h, 18h	Extended memory installed
03h	Minutes Alarm	19h	Drive C type if extended drive type
04h	Hour	1Ah	Reserved
05h	Hour Alarm	1Bh..23h	Reserved
06h	Day of Week	24h, 25h	System identification
07h	Date of Month	26h	Disk configuration and bus parameters
08h	Month	27h	CPU boot speed
09h	Year	28h	Base memory size and IRQ12 select
0Ah	Status register A	29h	Peripheral configuration
0Bh	Status register B	2Ah..2Ch	Reserved
0Ch	Status register C	2Dh	Additional flags
0Dh	Status register D	2Eh, 2Fh	Checksum value
0Eh	Diagnostic byte	30h, 31h	Memory more than 1 megabyte
0Fh	Reset code byte	32h	Century, part of time and date function
10h	Diskette drive type	33h	System information
11h	Reserved	34h..36h	Reserved
12h	Fixed disk drive type	37h..3Fh	System password
13h	Keyboard and boot options		

BIOS ROM

NOTE: This section discusses aspects of BIOS and other ROM-based firmware unique to this product. For a detailed description and listing of the BIOS calls and functions contained in ROM, refer to the *Compaq BIOS Technical Reference Guide*, P/N 074A/0693 and the *PCI Local Bus Specification Revision. 2.1*.

The BIOS ROM of the computer system includes the following functions:

- Chipset POST and power management firmware
- ROM-based Setup
- Keyboard controller firmware
- PCI bus functions (revision level 2.1)
- Video controller firmware (video BIOS)
- Plug and play functions (revision level 1.0a)
- PC Card firmware
- APM functions (revision level 1.1)

The firmware contained in the BIOS ROM supports the following operating systems:

- DOS 6.2
- Windows 3.1
- Windows for Workgroups 3.11
- Windows 95
- Windows NT 3.5
- Windows NT 4.0
- OS/2 v 2.1
- OS/2 Warp

The system firmware is contained in a flash ROM device, which can be rewritten with updated data if necessary. During POST, the integrity of the BIOS ROM is checked. If a fatal error is detected, a system beep will result. Crash recovery and BIOS ROM updates are supported through the ROMPaq diskette program. Additional ROM recovery is provided by a parallel port Flash Disaster recovery mechanism.

System Identification

System Identification ROM Locations

The ROM memory locations containing system identification data are listed in Table 3-8.

Table 3-8
System Identification BIOS ROM Locations

Address	Function	Value
F000:FFE4	Product family code	"V" (ASCII)
F000:FFE5	BIOS point release number	20h
F000:FFE6	BIOS revision code	(incr. ea. release)
F000:FFE7	BIOS family code	20h
F000:FFE8	BIOS type code	3033h
F000:FFEA	Machine ID	"COMPAQ" (ASCII)
F000:FFF5	BIOS date of release	mm/dd/yy
F000:FFFE	Machine type code	FCh

Computer Setup

The disk-based Computer Setup utility displays the system's current configuration and allows the user to set the system parameters. The configuration parameters are stored in nonvolatile configuration memory commonly referred to as CMOS. A backup copy is also saved in the boot block Flash EPROM. The user activates Computer Setup by pressing F10 at boot time.

Some changes made in Computer Setup may take effect immediately upon exiting Computer Setup, while other changes will require the system to be rebooted to take effect. The following parameter changes will take effect immediately upon exiting Computer Setup:

- Date/time
- Power conservation (when/how much)
- Hibernation (on/off, settings)
- Warning beep
- Computer Setup password
- Port disables (diskette, serial/IrDA, parallel, PC Cards)
- Monitor energy saving
- Resume password

The following parameter changes will not take effect until after a system boot:

- POST memory test
- Keyboard num lock
- Boot sequence/display
- Port settings (serial, IrDA, parallel)
- Power-on password
- Diskette boot disable
- Language selection
- MPEG video format
- Network settings

Plug and Play (PnP) Support

The BIOS includes plug and play (PnP) support, including support for the Windows 95 operating system. The following PnP functions are supported:

Function	Description
00h	Get Number of System Device Nodes
01h	Get System Device Node
02h	Set System Device Node
03h	Get Event
04h	Send Message
05h	Get Docking Station Info

The BIOS will detect if a PnP OS is present. If a PnP OS is detected, the following devices that can be configured by the OS will be inaccessible for configuration by the user and will be grayed out in Setup:

- Serial and infrared ports
- Parallel port
- Network setup
- PC Card slots

PC Card Support

The BIOS ROM includes PC Card firmware support for DOS and Windows. The PC Card interface is discussed in Chapter 5, “PC Card Interface.”

APM Support

In addition to ACPI, the BIOS ROM includes support for APM Version 1.2. This system also supports the following Compaq-specific APM functions:

INT 15h, AX = 5307h, - Set IR Device Power State

This function is called by the device driver to turn on/off the infrared device.

INPUT:

- AH = 53h
- AL = 07h
- BX = E400h, IR device
- CX = 0040h to turn on
  = 0003h to turn off

OUTPUT:

Successful

- CF = 0

Unsuccessful

- AH = Error Code:
  = 01h, Power management functionality disabled
  = 03h, Interface not connected
  = 09h, Unrecognized device ID
  = 0Ah, Parameter value out of range
  = 0Bh, Interface not engaged
  = 60h, Unable to enter requested state
  = All other values OEM-specified
- CF = 1

INT 15h, AX = 530Bh, - Get PM Event (Monitor Switching)

The BIOS will post this event when the hotkey is pressed and after the monitor switching has occurred. The video driver will receive this event and process it in its message handling loop to accommodate the resolution change.

INPUT:

- AH = 53h
- AL = 0Bh

OUTPUT :

(Successful):

- BX = 0200h, Display device switched event notice
- CF = 0

(Unsuccessful):

- AH = Error Code:
  = 03h, Interface not connected
  = 0Bh, Interface not engaged
  = 80h, No power management events pending
- CF = 1

System Memory

This chapter describes the system memory. Standard memory for all models is 32-MB. The memory subsystem consists of 32-MB of 66-MHz Synchronous Dynamic Access RAM (SDRAM) located on the processor board. Memory is expandable to 160-MB.

Memory Control

The Northbridge ASIC provides address control, data control, and communication for the memory subsystem. This device is a 3.3VDC device and support 3.3VDC memory components. The Northbridge ASIC provides the following memory related features:

- 64-bit wide DRAM memory system
- Programmable RAS and CAS timing
- Refresh mode support for RAS only, CAS only, CAS before RAS, and Self refresh
- Programmable refresh rate
- Burst Read Supported
- Shadow RAM in the 640-KB to 1-MB area
- Support for 16-, 32-, 64-, and 128-MB 144-pin SODIMM modules
- 32-MB of main system SDRAM standard
- SDRAM expandable to 160-MB using 128-MB SODIMM module
- Memory Configuration

The computer comes equipped with 32 MB of 66-MHz synchronous dynamic random access memory (SDRAM). Memory is expandable to a maximum of 160 MB by using 16-, 32-, 64-, or 128-MB SODIMM memory expansion modules.

Memory Timing

SDRAM signals are quite similar to conventional DRAM, but the manner in which the setup and transfer occurs is different. DRAM uses the RAS and CAS signals to start the read, write, or refresh cycle. SDRAM uses its clock line to synchronously latch in all of the required I/O signals into the SDRAM's pipeline to start the cycle. After a programmed number of cycles (typically 5 or 6), new data is available on each clock cycle.

Upon power-up, the Mode Register is undefined and must be initialized for correct operation. This requires a Mode Register Set command, performed by driving the address lines with configuration data during a Mode Register Set command. The desired operating conditions of the device are specified. The device is now available for transfer operations. This programming operation takes place during system boot, and is controlled by the system BIOS.

The system clock input synchronizes all signals during operation. All signals are referenced to this positive edge of the clock. Unlike conventional DRAM, however, data is cached, so that at each clock edge, new data is available at the output.

Memory Map

System memory is configured with 640-KB of base memory. Video RAM is mapped into the next 128-K block, and Video BIOS ROM is mapped into the 48-K immediately above that. System BIOS ROM is mapped at the top 64 K of the first 1-M address space.

Memory Refresh

Refreshing the device is similar to the DRAM refresh, but is initiated in two different ways. Instead of actually asserting the CAS and RAS signals, the Auto Refresh command may be given to the device when both banks are in the idle mode. Upon receiving this command, the device will then perform a CBR refresh cycle automatically. Both banks will be refreshed alternately before the internal refresh counter is incremented.

The Self Refresh mode is entered by issuing the Self Refresh Entry command. This command will perform refresh cycles until the device receives a Self Refresh Exit command. During a refresh cycle, all I/O buffers are disabled.

Memory Configuration

Table 4-1 describes the possible memory configurations for the computer.

Table 4-1
Memory Configuration

SODIMM Module Present	Total system memory
No SODIMM present	32-MB
16-MB	48-MB
32-MB	64-MB
64-MB	96-MB
128-MB	160-MB
Any EDO in Pentium II	32-MB (EDO not usable)

If an EDO memory module is placed into a Pentium II system, a POST error message will be printed to the screen. The new message will read “This expansion memory type (EDO) is not supported.”

PC Card Interface

This chapter describes the PC Card interface as defined by the Personal Computer Memory Card International Association (PCMCIA) 1997 PC Card Standard. The PC Card interface provides system expansion that is transparent to the user through two PC Card slot connectors. Peripherals (in the form of PC Cards) can be added to the system, which automatically interrogates the PC card and determines its function and requirements. This can be accomplished without the need of powering down, reconfiguring, and rebooting the system.

The PC Card controller is a PCI bus bridge device providing 16-bit PC Card and CardBus PC Card (32-bit) support as defined in the PCMCIA 1997 PC Card Standard. The PC Card subsystem provides support for 8-, 16-, and 32-bit operation and can physically accommodate up to two Type I or Type II PC Cards or one Type III PC card.

This section contains basic information about the functions provided by the TI-PCI1220 PCI/CardBus controller. For a detailed description of this PC Card implementation, consult the *PCI1220 PC Card Controller* specification sheets by Texas Instruments dated May 8, 1997.

Functional Description

The PC Card interface facilitates mass storage, audio/video and/or communications capabilities of the computer through easily installable PC Cards. Video and audio features are supported through a dedicated Zoomed Video bus in slot A (bottom slot) that provides a direct, uninterrupted video signal path to video memory frame buffers. A functional PC Card interface involves the use of following hardware components

- Hardware: The PC Card and the PC Card controller
- Software: A set of special BIOS calls, routines, and device drivers that mediate between the hardware, operating system, and application software. Compaq products are provided with a multilayered software support for PC Card operation. PC cards may also require and come with device drivers to facilitate interface support.

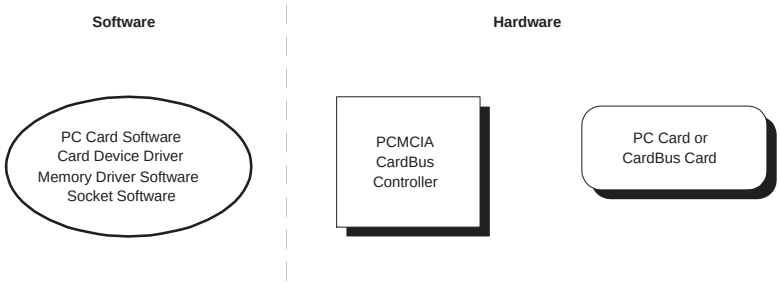


Figure 5-1. PC Card Interface Components

Hardware

The hardware components of the PC Card interface include: a PC Card interface/controller and the PC Card itself. The PC Card is not described in detail in this section but is discussed later in this chapter in the “Operational Overview” subsection. The TI-PCI1220 PC Card controller provides for features such as:

- Power-on (hot) plugging and unplugging of two 5.0-volt or 3.3-volt PC Cards
- PCI Power Management and PCI 2.1 compliance
- Serial vendor and subsystem ID interface EEPROMs and LED activity pins
- Support for Zoomed Video mode (slot A)
- Pipelined architecture provides increased throughput (>130 MB/sec)
- Parallel PCI interrupts, parallel ISA IRQs, serialized ISA IRQs and PCI interrupts
- Separate configuration spaces for each multifunction PCI device socket
- Support for 16-bit distributed DMA and PC/PCI DMA on both PC Card sockets

The Texas Instruments TI-PCI1220 PC Card Controller supports two PC Card sockets (see Figure 5-2). A 68-pin connector provides the electrical interface between the PC Card controller and the PC Card, as specified in the March 1997 PC Card Standard. This connector and the associated PC Card interface signals are described in detail in the section titled "Connector Information."

When in the legacy mode (16-bit PC Card mode), the controller uses a 16-bit data bus that can function as a memory bus or as an I/O bus. The 26-line address bus allows the direct addressing of up to 64 Mbytes of memory for 16-bit memory cards. The same address lines are used as port selection lines for I/O peripherals.

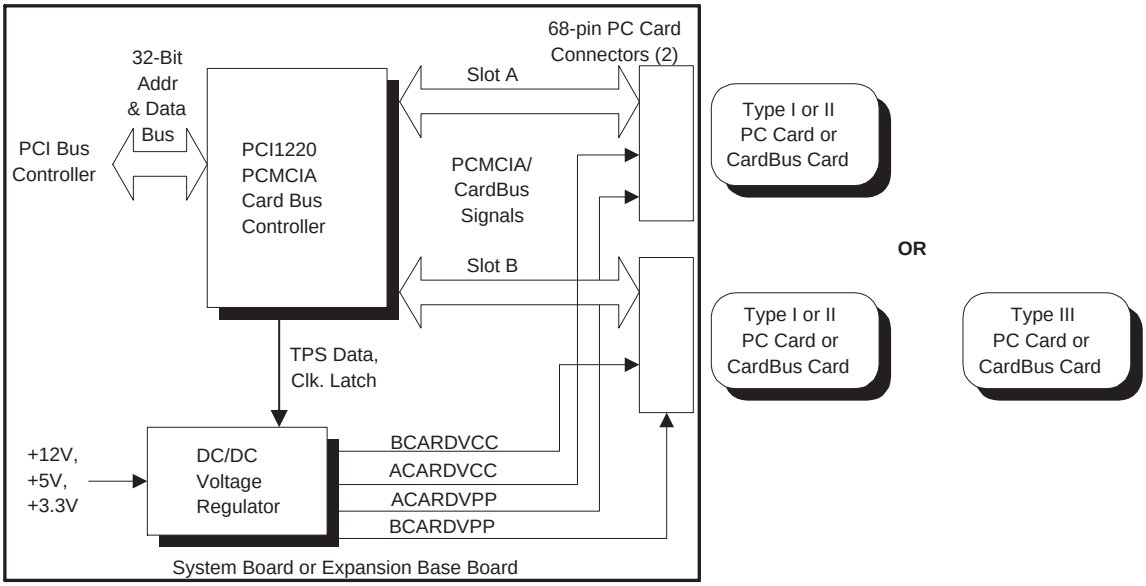


Figure 5-2. PC Card Interface, Hardware Components

For details concerning the PC Card interface, consult the *PCI1220 CardBus Controller* specification by Texas Instruments dated May 8, 1997.

PC Card Slots

This system supports two Type II PC Card format expansion sockets stacked to allow the support of a single Type III PC Card as well. The expansion card can be easily removed by an eject button.

Both sockets offer CardBus PC Card compatibility as specified by the March 1997 PC Card Standard. CardBus PC Card offers a 32-bit multiplexed synchronous interface very similar to the PCI bus. The CardBus PC Card specification has increased the maximum frequency for the interface to 33 MHz, which requires a different connector with improved card grounding characteristics on the 68-pin interface, for 32-bit support. This improved connector is also backward compatible with previous PC Cards.

For maximum compatibility, the PC Card sockets support bus mastering (in the CardBus mode), and distributed DMA compatibility (in the 16-bit PC Card compatibility mode). DMA channels are mappable to available channels, rather than the dedicated system used previously.

Socket keying for 3v/5v card support is per the March 1997 PC Card Standard. This keying and voltage sense pin convention allows 3v-only cards, 5v-only cards, and milti-voltage or dual-voltage (3-/5-volt) cards. The power rails and buffer levels for each socket are independently controllable to support use of any combination of the 3-volt, 5-volt, or 3-/5-volt cards.

Software

The flexibility of the PC Card interface is supported by a layered software support scheme to ensure that PC Card usage is transparent not only to the user, but also to application and the majority of operating system software. The computer uses a software package to support PC Card hardware that contains three layers of software to provide socket level access, card compatibility, and special device/memory drivers.

Socket level software is a collection of standard software calls that provide access functions to and from the PC Card, and is the first (lowest) level of software support of the PC Card interface. Socket level software provides basic control of PC Card interface accessibility. These routines are tailored specifically to the type of PC Card controller used, and are hardware-dependent.

Card compatibility software is operating system dependent and provides the compatibility link between the application software and socket level software. Card-level software contains a table of system resources available to PC Cards and allocates those resources. Card-level software is also responsible for controlling the process of determining the type and function of an installed PC Card through the socket-level software.

While card- and socket-level software provide access to all PC Card functions, some PC Cards require special consideration regarding read/write/erase cycles. Such operating specifications are controlled with routines contained in device drivers and memory technology drivers. PC Card device driver software includes basic device driver support for memory and ATA/IDE devices that meet the 1997 PC Card Standard criteria. PC Cards that require special considerations should be supplied with their own device drivers, which need to be loaded onto the system so that they can be accessed by the PC Card software. Figure 5-3 shows the software layer relationship.

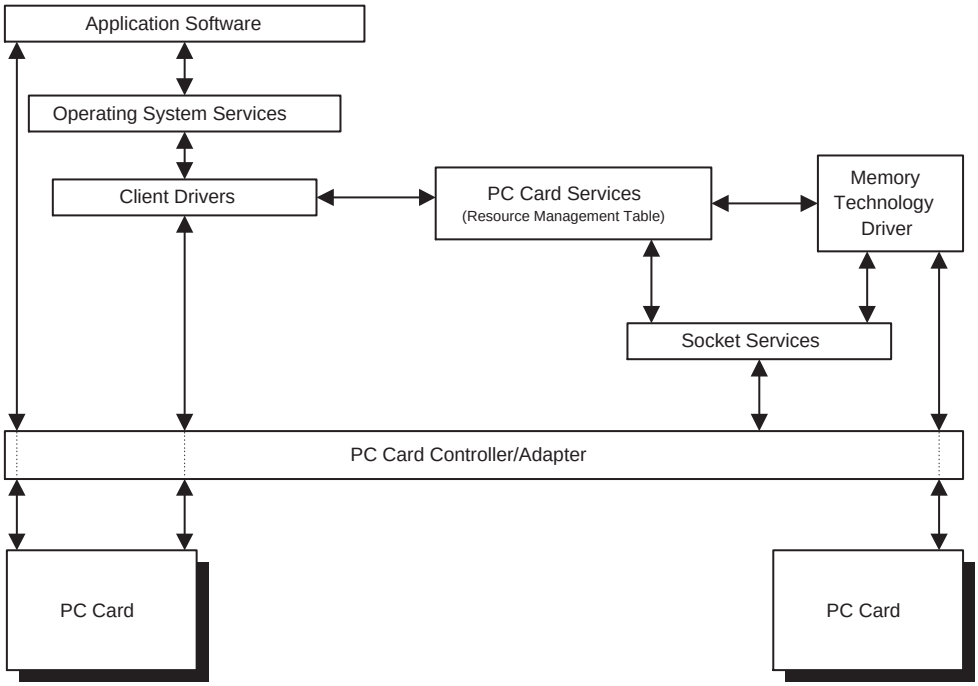


Figure 5-3. PC Card Interface, Software Architecture Diagram

BIOS Initialization

In order to support the legacy mode (16-bit operation), the PC Card controller is initialized by BIOS into the Intel 82365-compatible mode as device PNP0E03. The following steps are necessary for BIOS POST time for PC Card controller configuration space initialization.

- Command register (offset 0x04) set to 0x07
- Register base address (offset 0x10) set to 0
- All memory and I/O windows set to 0 (offset 0x1C - 0x38)
- Interrupt line register (offset 0x3C) set to 0xff (no IRQ assigned)
- Legacy base address (offset 0x44) set to legacy mode I/O base address (e.g., 0x3E0)

- Any other controller-specific initialization requirements

This procedure puts the PC Card controller into the legacy mode for access as a PCIC compatible controller by the Microsoft Windows socket services driver.

Microsoft Windows puts the PC Card controller into the CardBus PC Card mode (32-bit operation) when the BIOS enumerator detects PNP0E03 and the compatible ID of PnP0E00. Microsoft Windows then hides the device and calls the BIOS to disable it. When BIOS receives the call, it performs the following procedure:

- Command register (offset 0x04) set to 0
- Register base address(offset 0x10) set to 0
- Interrupt line register (offset 0x3C) set to 0xFF
- Legacy base address (offset 0x44) set to 0
- Any other controller-specific initialization requirements

The system is made compatible with both Windows (PCIC mode) and future versions of Windows after completion of this procedure.

IMPORTANT: Do not share writable PCI configuration space bits in a multifunctional PCI device. The interface legacy mode base address register at offset 44h in the Type 2 PCI header is the only exception due to the shared functions for compatibility with the ExCA programming model.

The BIOS is PCI 2.1 compliant and supports the Microsoft specified Interrupt Routing Table format (SPIR). The SPIR table returns all PCI IRQ routing information, including those for the CardBus controller. Because the PCI interrupts are sharable and only IRQ 11 is available in the computer, both PCI1220 CardBus socket PCI interrupts (INTA and INTB) are routed to the same IRQ 11. In this case, IRQ 11 is programmed as level-triggered.

Operational Overview

Automatic PC Card Detection/Initialization

The PC Card controller is used in either the ISA-based16-bit PC Card legacy mode, memory mapped PCI/ISA access mode (default mode), or the PCI-based 32-bit CardBus PC Card mode. The PCI1220 controller interface recognizes and identifies the installed PC Card type at power-up, or run time, and switches modes (including power) automatically to accommodate16-bit or 32-bit PC Cards.

The operation of the PC Card interface begins with the insertion of a PC Card into a PC Card socket. When a PC Card is inserted, an interrupt is generated, informing the system of the new device in the PC Card socket. Since 3.3-volt and 5.0-volt PC Cards are used, the socket can no longer power to 5.0 volts automatically. Cards are inserted into a cold socket and are then interrogated to determine the type of voltage required before being powered. The PC Card is then powered up and initialized. The actual power-up and initialization sequence can be tailored through the PC Card control registers. The PC Card contains information that defines the purpose, capabilities, and features of the PC Card. This information, called the card information structure (CIS), is read by card-level software, which configures the PC Card interface accordingly.

PC Card Interface Operation

A PC Card interface is configured, based on the CIS of the installed PC Card, for either memory-mapped or I/O-mapped operation, or both. When a PC Card is first installed, however, the PC Card controller assumes that the PC Card is a memory device. This assumption allows the system to access an area called attribute memory, which all PC Cards have, that contains the CIS. Two different device functions are available in the PC Card controller and are referred to as either Function 0 for PC Card socket A functions, and Function 1 for PC Card socket B operations. Function 0 and Function 1 are separately addressable PC configuration headers.

Addressing

All PC Cards are addressed using a windowing scheme where each PC Card is mapped into the address space of the microprocessor of the system unit. Memory-mapped 16-bit PC Cards are accessible through four address windows of common memory and one window of attribute memory. Both attribute and common memory are accessed with 26-bit addressing resulting in up to 64-megabytes of memory for 16-bit PC cards that can be directly addressed, either through one large common memory window or paged through several common memory windows.The I/O PC Cards are accessed through two I/O address windows. All PC Cards include a window of attribute memory where the CIS is contained. The attribute memory window allows up to 64 Mbytes of address space for ISA-based 16-bit PC Cards and up to 4-GB for PCI-based CardBus cards.

When a CardBus card is installed, access is made through the PCI1220 32-bit memory and I/O windows mapped directly to the CardBus memory. This direct mapping makes the use of page registers and offset registers unnecessary for CardBus operations.

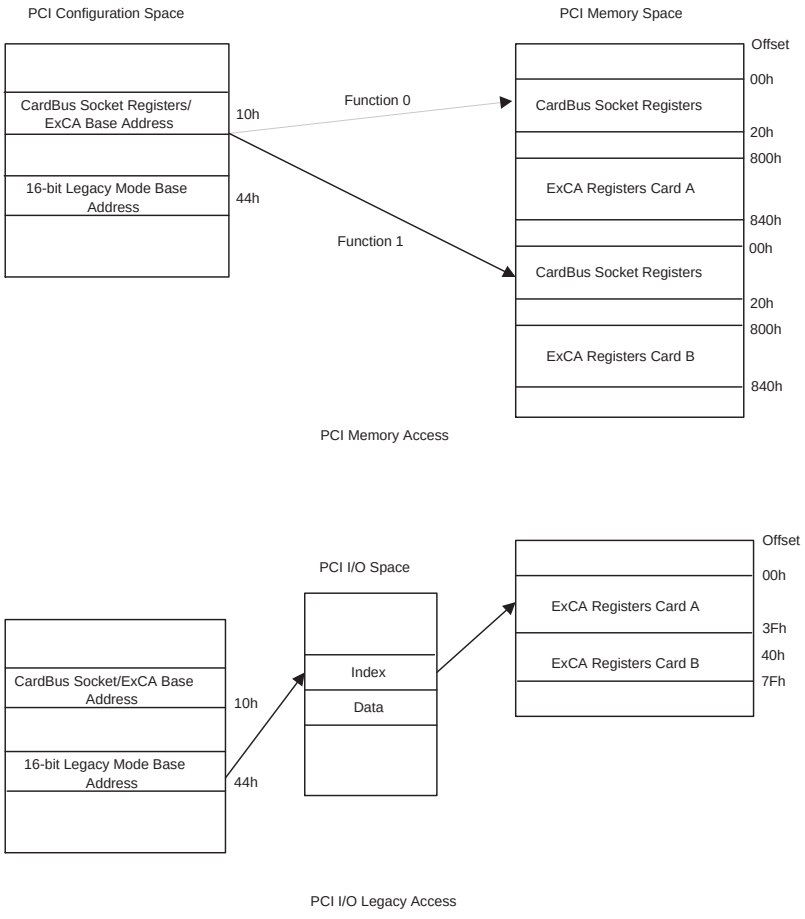


Figure 5-4. PCI Memory Access and PCI I/O Legacy Access Diagram

Interrupts

The PC Card interface can be configured to support several different interrupt-signaling schemes. The two basic types of interrupts used for PC Card devices are the Card Status Change (CSC) interrupts generated during card insertion, card removal, card ready, card battery condition, etc., and functional interrupts that are communicated over a dedicated signal by the PC Card application to request explicit service. Both CSC and functional-type interrupts are used for 16-bit I/O cards and CardBus card functions such as battery/wait states, card status changes, and power cycles status.

The PC Card controller also provides a serialized interrupt protocol that uses a single IRQ line to indicate all interrupt status information to the host controller in the form of packets that have a start, a stop, and several intermediate interrupt cycles. The host software must configure the PCI1220 controller to use serialized IRQs by setting bits <2> and <1> of the PCI configuration register to10b at offset 92h.

IDE Support

A PC Card interface can also be configured for AT attachment (ATA) mode, which operates as an IDE-compatible interface for mass storage devices such as hard drives. When configured for ATA mode, a number of PC Card interface pins change functions to provide IDE compatibility. These pins are discussed in “Connector Information.”

Power Management

The PC Card controller includes features to extend system unit battery life. These features include automatic low power mode, Suspend mode, and control of PC Card socket power.

Both legacy APM and advanced OS directed power management features are used by the PC Card interface through the implementation of ACPI power management.

In automatic low power mode, the PC Card controller inhibits the clock to most logic while address and data lines are tristated. Any activity on the PC Card interface will restore the controller to full operation. The automatic low power mode (recommended setting) is programmable through System Control registers.

The suspend mode uses the least amount of power. In the suspend mode, practically all circuitry of the controller is turned off.

The PC Card controller provides programmable control of power to the PC Card sockets. This allows PC Cards not being used to be turned completely off, thus reducing system unit battery drain.

Under ACPI compliant operating system, the PCI1220 can be programmed to 4 different device states (D0-D3). PCI1220 consumes progressively less power from D0 through to D3 state:

- D0: Device is on and running (full power consumption + full functionality)
- D1: Controller context is preserved but memory & I/O windows are not accessible. PCI configuration registers are still accessible. Card status change and functional interrupts are disabled. Power condition to cards retains.
- D2: Functionally the same as D1, except less power is consumed.
- D3: Controller context is lost. Memory & I/O windows are inaccessible. Card status change and functional interrupts are disabled. Power to cards is turned off.

To detect card status change events under D1, D2 and D3 states, the traditional interrupts cannot be used. Instead, the PME (Power Management Event) signal is used to wake up the controller to D0 state so that it can access the memory and I/O windows to configure the cards successfully. The power management driver will program the appropriate Interrupt Mask and Flags registers before putting the controller into the low power states. This will determine what events can wakeup the controller. The power management of PCI1220 can be controlled through PCI Power Management Control/Status register (offset A4h).

Refer to *PCI Bus Power Management Interface v1.0* (March 18 1997) specification and Microsoft released *Device Class Power Management for PC Card Controller Device Class* specification v1.0 for more PC Card power management information.

Thermal Management

The computer attaches a thermistor (LM75) to the CardBus cage and monitors temperature. Physically, the sensor is connected to a “leg” of the CardCage, and is operates whether a card is installed or not.

The Intelligent Manageability application will call the INT15 function to read the CardCage temperature periodically. The INT15 call will perform a read to the MSIO thermistor, and calculate the offset needed to translate the raw LM75 reading into the INT15 return data. If the thermistor measures over 65°C, the Intelligent Manageability application will either give the user a warning, or shut down the card itself.

The following describes the sequence used for cooling down the system.

1. The fan turned on or powered to HIGH speed.
2. The CPU will clock throttle to 50 percent.
3. The battery charger will be disabled.
4. An Intelligent manageability alert will be issued to the user.

Connector Information

A 68-pin connector provides the electrical interface between the PC Card adapter and the PC Card. Table 5-1 describes the signals used in the 68-pin PC Card connector and lists the signals in pin number order but grouped according to function. The I/O designation is with respect to the host system; that is, an "I" indicates an input signal that is coming into the host system from the PC Card. Note that a number of signal lines change functions according to the type of PC Card installed. PC cards such as Zoomed Video, CardBus, and speakerphone cards are sensed by the system, and the connector pins are configured for the correct signal and power requirements.

When a PC Card interface is configured in the ATA mode, some signals change in function. Unless otherwise noted in Table 5-1, signals either retain the same function or are not used in ATA mode.

For pin and signal information regarding Zoomed Video and CardBus PC Cards, refer to the zoomed video section in Chapter 8, and Figure B-6 in Appendix B of this guide. Refer to the PCI1220 Data sheets for signal descriptions in other modes.

Table 5-1
PC Card Connector Interface Signals

Pin	Signal	I/O	Functional Description
I	GND	-	Ground.
34	"	-	
35	"	-	
68	"	-	
2	D3	I/O	These bidirectional lines are for transferring data.
3	D4	"	
4	D5	"	
5	D6	"	
6	D7	"	
30	D0	"	
31	D1	"	
32	D2	"	
37	D11	"	
38	D12	"	
39	D13	"	
40	D14	"	
41	D15	"	
7	CE1–	O	Card Enable. When active (low), enables bytes at even (CE1 –)
42	CE2–	"	and odd (CE2–) addresses.
8	A10	O	Address lines. For memory functions, allow up to 64 megabytes
10	A11	"	to be directly addressed. For I/O functions, determine port
11	A9	"	selection.
12	A8	"	
13	A13	"	In ATA mode, only lines A2..A0 retain the same function. The
14	A14	"	following signals change function:
19	A16	"	A25 becomes CSEL
20	A15	"	A24 becomes M/S–
21	A12	"	A23 becomes VU
22	A7	"	A9 becomes CD1–
23	A6	"	All others are tri-stated.
24	A5	"	
25	A4	"	
26	A3	"	
27	A2	"	
28	A1	"	
29	A0	"	

Continued

Table 5-1, PC Card Connector Interface Signals *Continued*

Pin	Signal	I/O	Functional Description
46	A17	"	
47	A18	"	
48	A19	"	
49	A20	"	
50	A21	"	
53	A22	"	
54	A23	"	
55	A24	"	
56	A25	"	
9	OE	O	Output Enable. When active low, enables read access of a PC Card (memory) by the host system.
15	WE–/PGM	O	Write Enable/Program. For normal operation, enables write access to PC Card (memory) by host. Supports programming of EPROM on PC Card.
16	RDY/BSY–/IREQ–	I	Ready/Busy/Interrupt Request. When high, indicates to host system that PC Card is ready to service an access request. When low, indicates to host system that PC Card is either servicing a request or initiating a request.
17	Vcc	O	DC power to the PC Card.
51	"	"	
18	Vpp1	O	Programming power to the PC Card.
52	Vpp2	"	
33	WP/IOIS16–	I	Write Protect/Port is 16-bit. On some memory PC Cards, indicates (when high) status of write-protect tab. For I/O PC Cards, indicates (when low) to host system that PC Card has 16-bit functionality.
36	CD1	I	Card Detect. When active high, indicate to host of PC Card installation.
67	CD2	"	
43	RFSH	O	Refresh signal for memory PC Cards.
44	RSVD/IORD–	O	Reserved/Port read. For I/O peripherals is active low during a host system read of an I/O port.
45	RSVD/IOWR–	O	Reserved/Port read. For I/O peripherals is active low during a host system write of an I/O port.
57	RSVD	-	Reserved.
58	RESET	O	Reset.
59	WAIT-	I	Wait. When high, instructs host system to extend bus cycle. In ATA mode, this signal becomes IOCHRDY.
60	RSVD/ INPACK–	I	Reserved/Port Acknowledge. Used by I/O peripherals to acknowledge interrupt request. In ATA mode, this signal becomes DREQ.
61	REG–	O	Register Select. When active low, address selects attribute memory location. When high, address selects normal memory location. ATA mode = DACK.
62	BVD2/SPKR–	I	Battery Voltage Detect/Speaker Output. Can be used (by host system) to monitor PC Card's internal battery condition. Also used by the PC Card for audio output to host system. In ATA mode, becomes LED–.
63	BVD1/ STSCHG–	I	Battery Voltage Detect/Card Status Changed. Used (by the host system) to monitor PC Card's internal battery condition. Also by PC Card to indicate a change in status. In ATA mode, signal becomes PDIAG.

Serial, IR Serial, and Parallel Interfaces

Serial Interface

The serial interface in the SMC FDC37C95x FR Ultra I/O (MSIO) is equipped with two UART controllers functionally equivalent to the 16550A. UART 1 may be I/O-mapped to addresses 3F8h..3FFh (COM1), 2F8h..2FFh (COM2), 3E8h..3EFh (COM3), or 2E8h..2EFh (COM4) through the setup utilities. The UART input, output, and handshake pins are connected to the serial connector through a MAX213 RS232 transceiver. A detailed description of the device registers follows.

Device Registers

The following is a detailed description of the serial interface device registers. Note that the first two I/O addresses have different registers and bit definitions depending on state of the line control register (base address + 3). The scratch pad register is a general purpose register used to store temporary data at the programmers discretion.

Receiver Buffer/Transmitter Holding Register (Base Address)

This register contains the byte just received or the next byte to be transmitted by the serial controller.

Baud Rate Divisor Latch (Base Address)

This register is enabled when bit <7> of the line control register = 1. The serial controller contains a built-in baud rate generator that divides the input clock (1.8432 MHz) by a divisor to create a desired baud rate or serial transmission frequency.

The divisor is found according to the formula:

Divisor = 1843200 / (desired baud rate × 16)

Interrupt Enable (Base Address + 1)

The bits of this register enable up to four interrupt sources. The register format is described in the following chart.

Addr. Offset = 1h, DLAB = 0, R/W

BIT	FUNCTION
7..4	Reserved
3	1 = Modem Status interrupt enabled
2	1 = Receiver Line Status interrupt enabled
1	1 = Transmitter Holding register empty, interrupt enabled
0	1 = Baud Rate Divisor interrupt enabled

Interrupt ID (Base Address + 2)

This register contains one bit that flags the serial controller as the source of the interrupt and three bits that specify the reason for the interrupt. The serial controller interrupts are prioritized and are listed below with the lowest-priority interrupt first. To clear the interrupt, read the contents of the register.

Addr. Offset = 2h, DLAB = 0, RO

BIT	FUNCTION
7,6	00 = FIFO disabled 11 = FIFO enabled
5,4	Reserved
3..1	000 = Modem Status (Clear to Send, Data Set Ready, Ring Indicator, or Carrier Detect) 001 = Transmitter Holding register empty 010 = Received Data Available 011 = Receiver Line Status register (Overrun Error, Parity Error Framing Error, or Break) 100 = Reserved 101 = Reserved 110 = Character timeout 111 = Reserved
0	0 = Interrupt is pending (this device sent interrupt)

FIFO Control Register (Base Address + 2)

This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level, and select DMA mode.

Addr. Offset = 2h, DLAB = x, WO

BIT	FUNCTION
7, 6	Sets the RCVR trigger level 00 = 1 byte 01 = 4 bytes 10 = 8 bytes 11 = 14 bytes
5, 4	Reserved
3	Reserved
2	0 = XMIT FIFO not reset 1 = Clears and resets the XMIT FIFO
1	0 = RCVR FIFO not reset 1 = Clears and resets the RCVR FIFO
0	0 = Disables and clears the FIFOs 1 = Enables both the XMIT and RCVR FIFOs

Line Control (Base Address + 3)

This register specifies the serial data transmission format.

Addr. Offset = 3h, DLAB = 0, R/W

BIT	FUNCTION
7	0 = Enable Receiver Buffer/Transmitter Holding registers and Interrupt Enable register Access 1 = Enable Divisor Latch Access to write Baud Rate Divisor
6	1 = Break control bit # forces SOUT signal low
5	1 = Stick Parity # with even parity enabled, the parity bit becomes logic 0; with odd parity enabled, the parity bit becomes logic 1.
4	0 = Odd Parity 1 = Even parity
3	1 = Parity bit enabled
2	0 = 1 Stop bit 1 = 2 Stop bits (1.5 for 5-bit words)
1, 0	00 = 5-bit word 01 = 6-bit word 10 = 7-bit word 11 = 8-bit word

Modem Control (Base Address + 4)

This register controls the modem interface lines.

Addr. Offset = 4h, DLAB = x, R/W

BIT	FUNCTION
7..5	Reserved
4	1 = Enable Internal Loopback (processor verification of Tx/Rx)
3	1 = Enable Serial Port Interrupts (Out2)
2	1 = Output 1 (Out1) control. R/W by CPU only
1	1 = RTS_ signal active
0	1 = DTR_ signal active

Line Status (Base Address + 5)

This register contains the status of the current data transfer. Bits <2..0> are cleared on a read of this port.

Addr. Offset = 5h, DLAB = x, R/W

BIT	FUNCTION
7	1 = At least one parity error, framing error, or break indication in the RCVR FIFO
6	1 = Transmitter Holding register and Transmitter Shift register are empty
5	1 = Transmitter Holding register is empty, ready for character
4	1 = When a Break Interrupt has occurred
3	1 = Framing Error
2	1 = Parity Error
1	1 = Overrun Error - data lost
0	1 = A character is in the Data register to be read

Modem Status (Base Address + 6)

This register contains the status of the interface lines.

Addr. Offset = 6h, DLAB = x, R/W

BIT	FUNCTION
7	1 = DCD_ signal active
6	1 = RI_ signal active
5	1 = DSR_ signal active
4	1 = CTS_ signal active
3	1 = DCD_ has changed state since last read by the system
2	1 = RI_ has changed from a low to a high state since last read
1	1 = DSR_ has changed state since last read by the system
0	1 = CTS_ has changed state since last read by the system

Infrared Serial Interface

The infrared serial interface of the computer is composed of two parts. The first part is the IrDA compliant transceiver module. This module meets the Infrared Data Association (IrDA) specifications[1] for Fast IR (4-MB) communication with IR driven devices. The transceiver is designed to operate from a distance of from 1 cm to 1 meter between the computer and the external IR device. The IR communication data rate can be as high as 4 Mbps at viewing angles up to 15 degrees.

The transceiver module consists of a high-speed IR photo diode receiver and an IR LED transmitter. The input and output of this module is connected directly to the output and input pins of the MSIO Super I/O device. The choice of input and output pins may be selected through the SCE Configuration Register A, bit <7>.

The second part of the IR interface is the second UART in the MSIO Super I/O device. This section of the device is fully compliant to the IrDA Version 1.1 specification. IrDA-SIRA, IrDA-SIRB, IrDA-HDLC and IrDA-FIR modes at up to 4 Mbps are supported. The Infrared Communications Controller (IrCC) also provides support for ASK-IR, Consumer (TV remote) IR, and RAW-IR.

The host controller has direct access to the IR bit stream from/to the transceiver in RAW mode. The IrCC block is a superset of UART2, comprising a UART2 Asynchronous Communications Engine (ACE) and a separate Synchronous Communications Engine to provide the full set of IR modes, as well as the standard UART COM mode. This device is more fully described in the IrCC Specification referenced on page 1-1 of this document. This document is available from the SMC Web site, http:\\www.smc.com.

Figure 6-1 is a block diagram of the infrared serial interface.

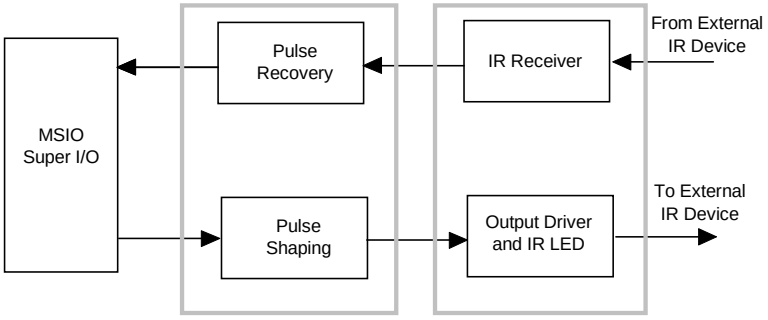


Figure 6-1. *Infrared Serial Interface, Block Diagram*

[1]IrDA 4MB compliant. IR performance may vary depending on performance of IR peripherals, distance between IR devices, and applications used.

IR Registers

Configuration Registers Overview

In order to support the IrCC, four configuration registers are added to UART2. These registers consist of the Fast IR Base I/O address registers (0x62h and 0x63h), an IrCC DMA channel select register (0x74h), and an IR Half Duplex timeout register (0xF2h).

Base I/O Addresses

Asynchronous Communications Engine (UART) Registers

Register Index	Base I/O Range	Fixed Base Offsets
0x60h, 0x61h	0x100h : 0xFF8h	+0 : RR/TB I LSB divisor
		+1 : IER I MSB divisor
(0x60h = MSB	On 8 byte boundaries	+2 : IIR/FCR
0x61h = LSB		+3 : LCR
of UART 16 bit Base address)		+4 : MCR
		+5 : LSR
		+6 : MSR
		+7 : SCR

Fast IR/USRT

In this computer, the FIR hardware is enabled, and the Windows 95 drivers work with the hardware to support FIR modes. If a user moves to Windows 98, new drivers are used that do NOT work with the older BIOS/FIR hardware combination.

Synchronous Communications (SCE) Registers

Register Index	Base I/O Range	Fixed Register Base Offset
0x62h, 0x63h	0x100h : 0xFF8h	+0 : Register Block N, Address 0
		+1 : Register Block N, Address 0
(0x62h = MSB	On 8 byte boundaries	+2 : Register Block N, Address 0
0x63h = LSB		+3 : Register Block N, Address 0
of UART 16 bit Base address)		+4 : Register Block N, Address 0
		+5 : Register Block N, Address 0
		+6 : Register Block N, Address 0
		+7 : USRT Master Control Register

IR DMA Channels

DMA channel 0, 1, 2, or 3 may be selected for use with the IR logic through the configuration registers of logical device 5. The DMA channel for IR is routed from channel 2 on the MSIO to the General Purpose DRQ (GPDRQ) #4 on the Southbridge. BIOS maps this register during POST to DMA channel 5, as seen in Device Manager.

IR IRQ

The interrupt IRQ for the IR logic is selectable through the configuration registers for logical device 5. Refer to the SMC publications referenced on page 1-2 of this document.

Parallel Interface

The parallel port interface is integrated in the MSIO Super I/O device. The parallel port supports three standard modes of operation: standard parallel port (SPP), enhanced parallel port (EPP), and extended capabilities port (ECP). The parallel port pins are accessible by the 8051, which allows the 8051 to perform flash recovery through this port.

Printer functions are controlled by writing to, or reading from I/O ports. The printer access I/O ports are given in Table 6-1.

Table 6-1
Parallel Port I/O Addresses

Primary Port	Secondary Port	Read/Write	Function
378h	278h	R/W	Printer data register
379h	279h	R	Printer status register
37Ah	27Ah	R/W	Printer control register
37Bh	27Bh	Reserved	

Standard Parallel Port (SPP)

The SPP is fully compatible with ISA, EISA, and Micro Channel parallel ports. The parallel port uses a software based protocol and can transfer data up to 150 Kbps.

A write operation causes data to be sent to pins PD [0:7]. With the extended SPP mode, a write operation to the data register causes data to be latched in the data register. If the data port direction bit CTR [5] is 0, the latched data is also sent to pins PD [0:7]. Otherwise, the data is only latched.

In a read operation of the data register, the register contains the last data written to it by the CPU. With the extended SPP mode, when the CTR [5] is 0, a read operation from the data register allows the CPU to read the last data it wrote to the port. When CTR [5] is 1, a read operation to the data register causes the port to present the latched data on pins PD [0:7].

Enhanced Parallel Port (EPP)

The EPP mode provides better parallel port throughput and allows the CPU to address the peripheral device registers directly. Faster data transfers are achieved by automatically generating the address and data strobes. The EPP mode uses 8 single byte registers with a base address of 278h or 378h.

The four EPP transfer operations are address write, address read, data write, and data read. An EPP transfer operation consists of a CPU read or write cycle (from or to an EPP register) and an EPP read or write cycle (from a peripheral device to an EPP register or from an EPP register to a peripheral device).

Extended Capabilities Port (ECP)

The ECP mode is a hardware protocol that provides data transfer rates up to 2 MB/s. The ECP has DMA support and FIFO buffers for receive/transmit capability to reduce the load on the CPU. The FIFO buffers are 16 bytes each and can be configured for either transmit or receive. In addition, the FIFO buffers provide threshold interrupt for both directions.

The ECP is enabled when printer control register PCR [2] is 1. Once enabled, its mode is controlled via ECR[5:7]. The ECP has a total of 10 registers.

Registers

The parallel ports are controlled by several mapped registers: data, control, status, and configuration. The following paragraphs and charts describe the important registers in detail.

Data Register (378h, or 278h)

Each byte written to the data register (read or write) is latched into a loopback register and is output to the printer. The register contents can be read back (for test purposes). When the parallel port is in input mode, data is read from this register.

Status Register (379h, or 279h Read Only)

This register contains the current printer status. Reading this register clears the interrupt condition from the parallel port.

BIT	FUNCTION
7	0 = Printer busy
6	0 = Printer acknowledges correct receipt of data byte
5	1 = Out of paper
4	1 = Printer selected (on line)
3	0 = Printer error
2	Reserved
1	Reserved
0	1 = In EPP mode, time-out occurred in EPP cycle

Control Register (37Ah or 27Ah)

This register provides the printer control functions described below.

BIT	FUNCTION
7,6	Reserved
5	Direction control in PS/2 and ECP modes 1 = Tristates drivers on data lines and data is read from peripheral. 0 = Drivers enabled, Port writes to peripheral (Default)
4	Acknowledge Interrupt Enable 1 = Enables an interrupt on the rising edge of nACK 0 = Disables the nACK interrupt (Default)
3	0 = Printer select
2	1 = Initialize
1	0 = Auto line feed
0	0 = Strobe

[2]The checksum algorithm adds the contents of bytes 10h through 5Dh into a word. The word is written into 5Eh (MSB) and 5Fh (LSB).

Audio Subsystem

Functional Description

The entertainment audio subsystem provides 16-bit stereo audio support for CD-Audio, Zoomed Video, MPEG/TV, and entertainment software compatible with industry standards. The ES1869 AudioDrive component possesses an embedded microcontroller, OPL3™ superset ESFM™ music synthesizer, 16-bit stereo wave ADC and DAC, 16-bit stereo music DAC, MPU-401 UART serial port, dual game port, full Plug and Play support, hardware master volume control, FS Zoom Video interface, DMA control logic with FIFO, and ISA bus interface logic. The audio subsystem can capture and play back. WAV files.

All audio, including CPU-generated tones, keyboard beeps, audio from PC Card and MPEG/Zoomed Video options, and audio from sound files, is played through the internal speakers, or, if connected, headphones or external speakers. A programmable volume control sets the audio output from the ES1869 to a selected value. A 1.5-watt stereo amplifier and equalizer circuit provides the power necessary to drive the line devices, speakers, or earphones.

A block diagram of the audio subsystem is shown in Figure 7-1.

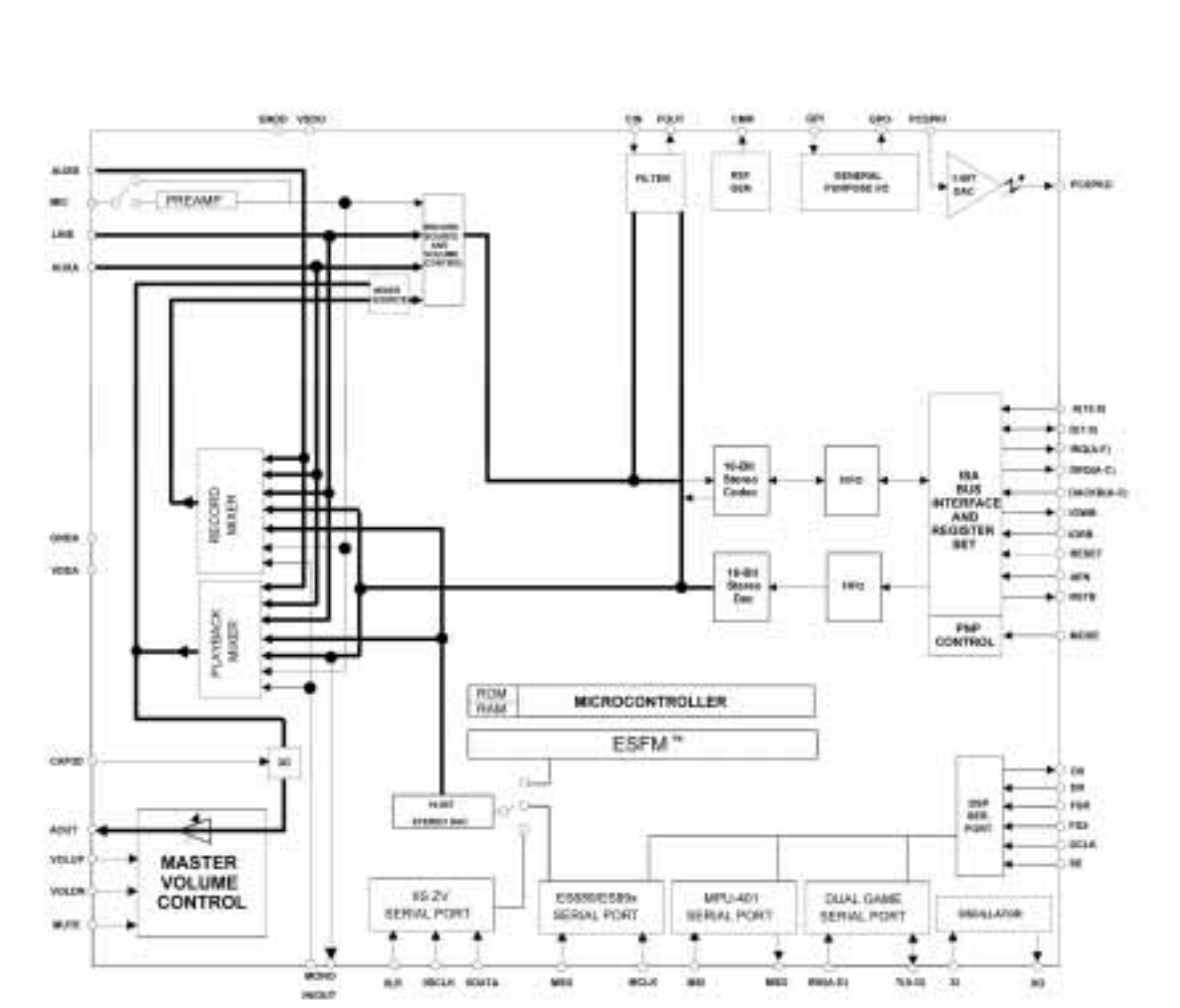


Figure 7-1. *Audio Subsystem, Block Diagram*

Features provided by the ES1869 audio controller are as follows:

- Plug and play support using internal ROM
- Stereo full duplex through two DMA channels
- Self-timed joystick port
- I^2S serial bus to Zoom Video Port
- General interrupt mapping and shared interrupts

The TPA0102 audio interface and equalization circuitry are physically located on the audio daughter card along with some supporting logic. The ES1869 audio controller on the system board through the sub-ISA connector. Audio information from the CD-ROM and PC Card subsystems is sent to the audio controller through the ISA connector.

Standard Audio I/O

The following paragraphs describe the external audio input and output connections of the audio subsystem.

Mic In (Input): The mic-in connector is a two-conductor mini-jack (3.5 mm) designed to work only with a mono electret microphone. Plugging into the mic-in jack disconnects the internal microphone from the audio subsystem.

Headphone Out/Line Out (Output): The headphone-out connector is a three-conductor (stereo) mini-jack primarily designed to allow connection of a pair of headphones. This port can also be used to connect a pair of "powered" speakers (i.e., the type meant to be used with portable radio/cassette players). Plugging into the headphone-out jack disconnects the internal speakers from the audio subsystem.

Audio I/O

The convenience base duplicates the following audio interfaces for external components:

- **Line Out (Output):** This three-conductor mini-jack allows connection to a pair of powered speakers.
- **Line In (Input):** This three-connector mini-jack accepts line-level outputs.
- **Joystick/MIDI Port:** This interface is used for connecting either a joystick or MIDI component.

PCM Operation

The ES1869 includes analog-to-digital converters (ADC) and digital-to-analog converters (DAC) that use pulse code modulation (PCM) to capture and play back waveform (.WAV) data files. The .WAV files produced through PCM contain numerical values that represent waveform amplitudes that, measured by timed sampling, determine the frequencies. This section describes ADC and DAC operation as well as how the digital audio data is transferred over the peripheral bus.

ADC Operation

The ADC receives an analog signal and quantizes it into a digital code that specifies the voltage level of the analog signal at that particular time. Depending on the mode of operation, up to eight formats are available from the following options:

- Mono or stereo
- 8- or 16-bit
- Signed or unsigned

DAC Operation (PCM)

The digital-to-analog (DAC) conversion simply reverses the procedure of the ADC. The digital audio data stream is received by the DAC, and the quantized values are decoded at the sampling frequency rate. A filter provides the final shaping of the wave before it is applied to the analog output circuitry.

DAC/ADC Configuration

The DAC/ADC used for PCM operation can be configured for compatible (common sound board functionality) mode or set up for extended mode, which has performance advantages over compatible mode. Table 7-1 lists the differences between compatible and extended modes.

Table 7-1
Mode Differences

Function	Compatibility Mode	Extended Mode
FIFO Size Available	64 bytes (SW Cntl)	256 bytes (HW Cntl)
Mono 8-bit ADC, DAC	44 KHz Max Samp.	48 KHz Max Samp.
Mono 16-bit ADC, DAC	22 KHz Max Samp.	48 KHz Max Samp.
Stereo 8-bit ADC, DAC	22 KHz Max Samp.	48 KHz Max Samp.
Stereo 16-bit ADC	11 KHz Max Samp.	48 KHz Max Samp.
Stereo 16-bit DAC	11 KHz Max Samp.	48 KHz Max Samp.
Signed/Unsigned Control	No	Yes
AGC During Capture	Mono Only (22 KHz)	No
Programmed I/O Block Trnsf.	No	Yes
FIFO Status Flags	No	Yes
Auto Reload DMA	Yes	Yes
Time Base for Progrbl. Timer	1 MHz or 1.5 MHz	800 KHz or 400 KHz
ADC/DAC Jitter	+/- 2 usec	None

The quality of audio is largely determined by two factors: resolution and sampling rate. A 16-bit resolution provides more levels of amplitude for definition as opposed to 8 bits. A higher sampling rate provides more accurate digital representation of the audio signal. The rule of thumb (based on the Nyquist theorem) dictates that the sampling rate should be at least twice the highest frequency to be processed (i.e., if 20 KHz is anticipated, then the sampling rate should be set to 40K per second or greater.)

Depending on the mode used, the sampling rate can be constrained by the resolution selected as indicated in the table above. Additionally, higher resolutions and sampling rates require more storage space for a given period of audio recording. Recording audio using 16-bit stereo resolution at a 44-KHz sampling rate takes up approximately 175 KB of hard drive space per second.

PCM Bus Cycles

The I/O and DMA cycles used by PCM (pulse code modulation) operations to process .WAV data follow standard ISA bus conventions. All bus transfers occur at the byte level. Programmed I/O cycles are always used for programming the control registers and may also be used for transferring audio data to and from the ES1869 as well. The use of DMA cycles allows the use of discrete transfers for each byte of audio data to and from the ES1869.

The audio subsystem can be configured for either single DMA channel mode or dual DMA channel mode. Single DMA channel mode means that capture and playback operations share the same (playback) DMA channel and only one operation, capture or playback, is possible at a time. Dual DMA channel mode allows simultaneous capture/playback operation to occur if desired, but requires two dedicated DMA channels. It is the programmer's responsibility to ensure that the capture and playback data have the same sample rate and format.

For transferring audio data over the bus, the ES1869 builds the quantized audio data using the “little endian” format. This format is defined as having the least significant byte of a multibyte word occupying the lowest memory address. Stereo capture and playback alternates between the left and right channels, starting with the left channel first. Mono capture samples only the left channel input, while mono playback routes the left channel through both left and right output circuitry.

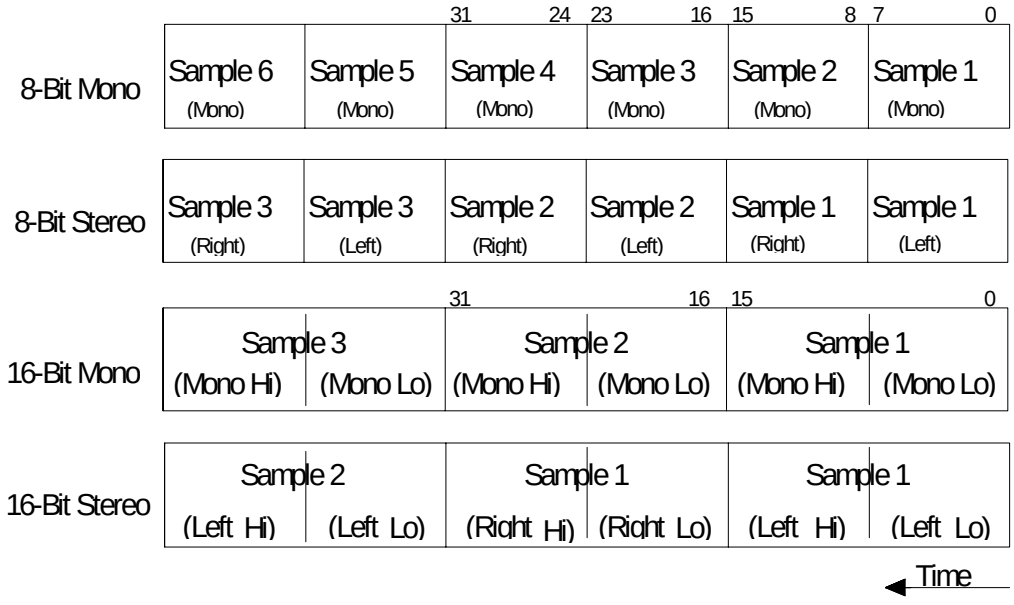


***Figure 7-2. ES1869**-to-ISA Bus Audio Data Formats and Byte Ordering*

FM Synthesis

The ES1869 component includes FM synthesis logic that supports the playback of MIDI (.MID) data files. The FM synthesizer function is register-controlled and uses frequency modulation to generate harmonics that will simulate the tone of musical instruments.

MIDI (.MID) files do not contain audio information in the same way that .WAV files do. In .MID files, audio data consists of note on/note off, tone type, and amplitude information. Audio stored in the .MID file format has the benefit of taking up far less storage space than audio stored as .WAV files[1].

A number of parameters affecting the generated sound are selectable or programmable. These parameters including the following:

- Waveform shape
- Waveform envelope characteristics (attack rate, decay rate, sustain level, release level)
- Key scale rate
- Rhythm percussion sounds

FM Synthesis Cycles

The **ES1869** component provides full FM synthesis support for playback of .MID data files. Processing .MID files is handled primarily with write cycles to the **ES1869**. A read cycle is used only for reading status. Note that if the succeeding data byte is meant for the same location as the previous data byte, then the address does not need to be rewritten.

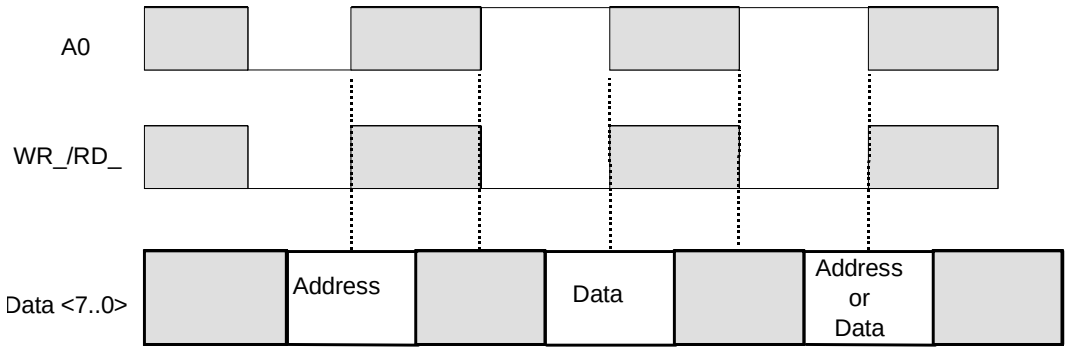


Figure 7-3. FM Synthesis Cycle

[1]The Joystick/MIDI interface of the optional expansion unit allows the connection of MIDI equipment to the system, enabling the transfer of digital MIDI data between the system and MIDI equipment.

Table 7-2 describes the available MIDI instrument sounds available.

Table 7-2
General MIDI Melodic Instrument Map

Patch #Instrument	Patch #Instrument	Patch #Instrument	Patch #Instrument
1 Acoustic Grand Piano	33 Acoustic Bass	65 Soprano Sax	97 Rain
2 Brt Acoustic Grand Piano	34 E. Bass - Finger	66 Alto Sax	98 Sound track
3 Electric Piano	35 E. Bass - Pick	67 Tenor Sax	99 Crystal
4 Honky-Tonk Piano	36 Fretless Bass	68 Baritone Sax	100 Atmosphere
5 Electric Piano 1	37 Slap Bass 1	69 Oboe	101 Brightness
6 Electric Piano 2	38 Slap Bass 2	70 English Horn	102 Goblins
7 Harpsichord	39 Synth Bass 1	71 Bassoon	103 Echoes
8 Clarinet	40 Synth Bass 2	72 Clarinet	104 Sci Fi
9 Celestra	41 Violin	73 Piccolo	105 Sitar
10 Glockenspiel	42 Viola	74 Flute	106 Banjo
11 Music Box	43 Cello	75 Recorder	107 Shamisen
12 Vibraphone	44 Contrabass	76 Pan Flute	108 Koto
13 Marimba	45 Tremelo Strings	77 Blown Bottle	109 Kalimba
14 Xylophone	46 Pizzicato Strings	78 Shakuhachi	110 Bag Pipe
15 Tubular Bells	47 Orchestral Harp	79 Whistle	111 Fiddle
16 Dulcimer	48 Timpani	80 Ocarina	112 Shanai
17 Drawbar Organ	49 String Ensemble 1	81 Lead 1 - Square	113 Tinker Bell
18 Percussive Organ	50 String Ensemble 2	82 Lead 2 - Sawtooth	114 Agogo
19 Rock Organ	51 Synth Strings 1	83 Lead 3 - Calliope	115 Steel Drums
20 Church Organ	52 Synth Strings 2	84 Lead 4 - Chiff	116 Woodblock
21 Reed Organ	53 Choir Aahs	85 Lead 5 - Charang	117 Taiko Drum
22 Accordion	54 Voice Oohs	86 Lead 6 - Voice	118 Melodic Tom
23 Harmonica	55 Synth Voice	87 Lead 7 - Fifth	119 Synth Drum
24 Tango Accordion	56 Orchestra Hit	88 Bass + Lead	120 Reverse Cymbal
25 Acoustic Guitar Nylon	57 Trumpet	89 Pad 1 - New Age	121 Guitar Fret Noise
26 Acoustic Guitar - Steel	58 Trombone	90 Pad 2 - Warm	122 Breath Noise
27 Electric Guitar Jazz	59 Tuba	91 Pad 3 - Polysynth	123 Seashore
28 Electric Guitar - Clean	60 Muted Trumpet	92 Pad 4 - Choir	124 Bird Tweet
29 Electric Guitar Muted	61 French Horn	93 Pad 5 - Bowed	125 Telephone Ring
30 Overdriven Guitar	62 Brass Section	94 Pad 6 - Metallic	126 Helicopter
31 Distortion Guitar	63 Synth Bass 1	95 Pad 7 - Halo	127 Applause
32 Guitar Harmonics	64 Synth Bass 2	96 Pad 8 - Sweep	128 Gunshot

Table 7-3 lists the percussive options available.

Table 7-3
General MIDI Percussion Instrument Map

Note #Instrument	Patch #Instrument	Patch #Instrument	Patch #Instrument
35 Acoustic Bass Drum	47 Low Mid Tom	59 High Timbale	71 Short Whistle
36 Bass Drum 1	48 High Mid Tom	60 Low Timbale	72 Long Whistle
37 Side Stick	49 Crash Cymbal 1	61 Low Bongo	73 Short Guiro
38 Acoustic Snare	50 High Tom	62 Mute Hi Conga	74 Long Guiro
39 Hand Clap	51 Ride Cymbal	63 Open Hi Conga	75 Claves
40 Electric Snare	52 Chinese Cymbal	64 Low Conga	76 High Wood Block
41 Low Floor Tom	53 Ride Bell	65 High Timbale	77 Low Wood Block
42 Closed Hi Hat	54 Tambourine	66 Low Timbale	78 Mute Cuica
43 High Floor Tom	55 Splash Cymbal	67 High Agogo	79 Open Cuica
44 Pedal Hi Hat	56 Cowbell	68 Low Agogo	80 Mute Triangle
45 Low Tom	57 Crash Cymbal 2	69 Cabasa	81 Open Triangle
46 Open Hi Hat	58 Vibraslap	70 Maracas	

MIDI Keyboard Control

When the computer is docked in the convenience base , a MIDI keyboard can be attached to the joystick/MIDI connector on the convenience base and used to control wavetable synthesis. For this configuration, the MPU-401 interface of the ES1869 should be configured in the Smart mode (instead of the UART mode).

NOTE: A MIDI keyboard left connected to the system may cause problems if FM synthesis is used simultaneously.

Register Programming

The audio subsystem can be made inactive using various methods, depending on whether the intent is toward power management or freeing up system resources. The system ROM includes firmware support for the audio subsystem.

The audio subsystem is controlled through I/O mapped registers. These registers are classified as either for joystick/PCM control or for FM synthesis control.

Table 7-4
ES1869 Registers

Address [1]	Register	R/W
0201h	Joystick Control	R/W
02*n*0h-02*n*Fh	PCM Processor	R/W
0388h-038Bh	FM Synthesizer	R/W

NOTES: [1] *n* = 2 for primary address (default), = 4 for secondary.

PCM Registers

The joystick/PCM functions are controlled through the I/O locations listed in Table 7-5.

The system allows reconfiguration to a secondary, tertiary, or quaternary base address as follows:

- Unlock address configuration register with a write (any value) to port FBh.
- Write 00h to port E0h.
- Write desired value of base address to bits <1,0> of port E1h.
- Lock the configuration with a write (any value) to port F9h.

Address Configuration Register, E1h

BIT	FUNCTION
7..3	Reserved - read/write 0s.
2	Chip Enable: 0 = Audio disabled 1 = Audio enabled
1,0	PCM Ops Base Address Select 00 = 220h 01 = 230h 10 = 240h 11 = 250h

Table 7-5
Joystick/PCM Registers

Address [1]	Register	R/W
0201h	Joystick Control	R/W
02*n*0h-02*n*3h	FM Synthesizer	R/W
02*n*4h	Mixer Address	R/W
02*n*5h	Mixer Data	R/W
02*n*6h	Reset Control (Write), Activity/Power Status (Read)	R/W
02*n*7h	Power Management	R/W
02*n*8h-02*n*9h	Reserved	R/W
02*n*Ah	Read Buffer Input Data	RO
02*n*Bh	Reserved	R/W
02*n*Ch	Command/Data (Write), Status (Read)	R/W
02*n*Dh	Reserved	R/W
02*n*Eh	Data Available Status	RO
02*n*Fh	FIFO I/O Address (Extended Mode)	R/W

NOTE: [1] *n* = 2 for primary address (default), = 4 for secondary.

The following pages include descriptions of joystick/PCM registers. For detailed programming information on the ES1869, refer to the *ES1869 AudioDrive Design Guide* by ESS Technology, Inc.

Joystick I/O Register (0201h, Read/Write)

This 8-bit register is used for reading data from or writing data to the joystick interface. An access generates the appropriate (read or write) control signal from the ES1869.

FM Synthesis Control Registers (02n0h-02n3h, Read/Write)

The ES1869 decodes addresses in this range only to generate a chip enable signal to the YMF262. Register descriptions for these locations are described later in the “FM Synthesizer” section.

Mixer Registers (02n4h, 02n5h, Read/Write)

The mixer registers allow level control of the audio inputs to the ES1869. Recording source and stereo/mono mode are also selected through these registers. Two sets of indexed registers are available: one set (00h-2Eh) is compatible with common sound cards, while the other set (00h-3Eh) provides extended capabilities. Both sets are accessed through two locations, 02n4h and 02n5h. The index is written to 02n4h and the data is written to or read from 02n5h.

02n4h, Mixer Index

BIT	FUNCTION
7,6	Reserved.
5..1	Index Address (refer to Table 7-4).
0	MXD - Mixer Flag. When set, indicates mixer register has been written to but not processed.

02n5h, Mixer Data

BIT	FUNCTION
7..0	Data

Table 7-6
Mixer Functions

Compatible Index	Extended Index	Function	Reset Value
00h	00h	Mixer Reset	—
04h	14h	Voice Volume	88h
0Ah	1Ah	Microphone Volume	00h
0Ch	1Ch	ADC (Recording) Source	00h
0Eh	1Eh	Stereo/Mono Switch	00h
22h	32h	Master Volume	88h
26h	36h	FM Volume	88h
28h	38h	CD Volume	00h
2Eh	3Eh	Line Volume	00h

As indicated in Table 7-6, the mixer functions have the same mapping for compatible and extended modes. In compatible mode, level control is confined to a 3-bit resolution per channel (Mic mix has 2 bits). In extended mode, a 4-bit resolution is used.

Mixer Reset Register (Index 00h, Write Only)

This register is used to reset the mixer values (a software reset does not affect the mixer registers). A write of any value to this register resets the mixer registers to their initial values.

Voice Level Register (Index 04h or 14h, Read/Write)

This register sets the level of volume for the voice audio.

Index 04h, Compatible, R/W

BIT	FUNCTION
7..5	Voice Volume Left
4	Reserved
3..1	Voice Volume Right
0	Reserved

Index 14h, Extended, R/W

BIT	FUNCTION
7..4	Voice Volume Left
3..0	Voice Volume Right

Microphone Level Register (Index 0Ah or 1Ah, Read/Write)

This register sets the level of volume for the microphone audio.

Index 0Ah, Compatible, R/W

BIT	FUNCTION
7..3	Reserved
2,1	Mic Volume
0	Reserved

Index 1Ah, Extended, R/W

BIT	FUNCTION
7..4	Mic Volume Left
3..0	Mic Volume Right

ADC (Recording Source) Register (Index 0Ch or 1Ch, Read/Write)

This register selects the input sound source for processing by the ADC.

Index 0Ch, Compatible, R/W

BIT	FUNCTION
7..3	Reserved
2,1	ADC Source: 00 = Microphone (default) 01 = CD 10 = Microphone 11 = Line
0	Reserved

Index 1Ch, Extended, R/W

BIT	FUNCTION
7..3	Reserved.
2..0	ADC Source : 000 = Mic 001 = L - mic R - master vol l & R 010 = CD 011 = Aout 100 = Mic 101 = Record mixer 110 = Line input 111 = Master vol input
0	Reserved.

NOTE: Some sound adapters use bit <5..3> of this register for filter control. On the ES1869, this bit has no effect.

Stereo/Mono Switch Register (Index 0Eh or 1Eh, Read/Write)

Bit <1> of this register, when set, selects the stereo mode for the DAC. This function is valid only for DMA transfers in compatible mode. The default/reset state of bit <1> is zero.

NOTE: Some sound adapters use bit <5> of this register for filter control. On the ES1869, this bit has no effect.

Master Level Register (Index 22h or 32h, Read/Write)

This register sets the master volume level.

Index 22h, Compatible, R/W

BIT	FUNCTION
7..5	Master Volume Left
4	Reserved
3..1	Master Volume Right
0	Reserved

Index 32h, Extended, R/W

BIT	FUNCTION
7..4	Master Volume Left
3..0	Master Volume Right

FM Level Register (Index 26h or 36h, Read/Write)

This register sets the volume level of the FM synthesis input.

Index 26h, Compatible, R/W

BIT	FUNCTION
7..5	FM Volume Left
4	Reserved
3..1	FM Volume Right
0	Reserved

Index 36h, Extended, R/W

BIT	FUNCTION
7..4	FM Volume Left
3..0	FM Volume Right

CD Level Register (Index 28h or 38h, Read/Write)

This register sets the volume level of the CD-ROM input.

Index 28h, Compatible, R/W

BIT	FUNCTION
7..5	CD Volume Left
4	Reserved
3..1	CD Volume Right
0	Reserved

Index 38h, Extended, R/W

BIT	FUNCTION
7..4	CD Volume Left
3..0	CD Volume Right

Line Level Register (Index 2Eh or 3Eh, Read/Write)

This register sets the volume level of the line audio input.

Index 2Eh, Compatible, R/W

BIT	FUNCTION
7..5	Line Volume Left
4	Reserved
3..1	Line Volume Right
0	Reserved

Index 3Eh, Extended, R/W

BIT	FUNCTION
7..4	Line Volume Left
3..0	Line Volume Right

Reset/Power Management Register (02n6h, Read/Write)

This register, on a write, controls the reset state of the ES1869 and, on a read, reports activity flags and power management status.

02n6h, Read/Write

BIT	FUNCTION
7	Activity Flag 2 (RO). When read as 0, indicates read or write has occurred to an FM port (02x0h-02x3h, 02x8h, 02x9h, 0388h-03Bh)
6	Activity Flag 1 (RO). When read as 0, indicates a read has occurred to ports 02xCh and/or 02xEh.
5	Activity Flag 0 (RO). When read as 0, indicates one or more of the following actions has occurred: DMA read/write to 02n4h, 02n5h DMA write to 02n6h DMA read of 02nAh DMA write to 02nCh DMA read/write to 02nFh
4	Reserved.
3	Power Down Status (RO). When read as 0, the digital section of the **ES1869** is powered down.
2	MIDI Mode (RO). When read as 0, a MIDI command (30h, 34h, or 35h) is being processed.
1	FIFO Reset (R/W) Compatibility Mode: Don't care Extended Mode: 0 = Release FIFO from reset. 1 = Hold FIFO in reset.
0	Software Reset (R/W): 0 = Release **ES1869** from reset. 1 = Hold **ES1869** in reset.

Power Management Register (02n7h Read/Write)

This register controls power management functions of the ES1869.

02n7h, Read/Write

BIT	FUNCTION
7,6	Reserved - read 0s
5	FM Reset. When cleared (0), forces reset to the FM logic.
4	FM Wakeup Control. 0 = Wakeup on FM activity is disabled 1 = Wakeup on FM activity is enabled
3,2	Power Down Control. 00 = **ES1869** full on 01 = Complete power down (analog and digital) 11 = Partial power down (digital down, analog up)
1	GPO1 - Not used
0	GPO0 - Used to control the power amp of the system unit internal speakers. 0 = Amp power ON 1 = Amp power OFF

Read Buffer Register (02nAh, Read Only)

This 8-bit register holds the input data from the read buffer. Bit <7> of 02nEh can be checked to determine if contents are valid.

ES1869 Status Register (02nCh, Read)

This 8-bit register is read to determine the overall status of the ES1869. This register should be checked (read) before sending (writing) a command or data to 02nCh.

02xCh, Read

BIT	FUNCTION
7	Write Buffer Status: 0 = Buffer available (not busy) 1 = Buffer not available (busy)
6	Read Buffer Status: 0 = Data not available 1 = Data available
5	FIFO Full: When set, indicates 256 bytes loaded.
4	FIFO Empty: When set, indicates 0 bytes loaded.
3	FIFO Half Empty: Set during extended mode.
2	Processor IRQ Flag. when set, **ES1869** internal processor generated an IRQ.
1	FIFO IRQ Flag. When set, indicates change in bit <3>, resulting in an IRQ. Used by programmed I/O with FIFO in extended mode.
0	DMA Counter Overflow IRQ Flag. When set, indicates DMA counter overflow resulting in an IRQ.

Command/Data Register (02nCh, Write)

This 8-bit register is used for writing commands or data to the ES1869. Before a write, this location should be read first to determine buffer/FIFO status (refer to the read bit definitions previously described). Table 7-7 lists and describes the commands available.

Table 7-7
ES1869 Commands

Command	Function	Mode
10h	Direct write 8-bit DAC in 8-bit signed format.	Comp.
10h	Direct write 8-bit DAC in 8-bit signed format.	Comp.
11h	Direct write 16-bit DAC in 16-bit unsigned format.	Ext.
14h	Start 8-bit DAC transfer in normal mode DMA.	Comp.
15h	Start 16-bit DAC transfer in normal mode DMA.	Ext.
1Ch	Start 8-bit DAC transfer in auto-init. mode DMA.	Comp.
1Dh	Start 16-bit DAC transfer in auto-init. mode DMA.	Ext.
20h	Direct mode 8-bit ADC in 8-bit unsigned format.	Comp.
21h	Direct mode 16-bit ADC in 16-bit unsigned format.	Ext.
24h	Start 8-bit ADC transfer in normal mode DMA.	Comp.
25h	Start 16-bit ADC transfer in normal mode DMA.	Ext.
2Ch	Start 8-bit ADC transfer in auto-init. mode DMA.	Comp.
2Dh	Start 16-bit ADC transfer in auto-init mode DMA.	Ext.
30h, 31h	MIDI input mode. Value 31h will cause IRQ for each MIDI byte.	Comp.
34h, 35h	MIDI output mode. Value 35h will cause IRQ for each MIDI byte.	Comp.
38h	MIDI output single byte.	Comp.
40h	Set time constant for timer used for DMA with DAC/ADC.	Comp.
41h	Alternate time constant.	Ext.
42h	Independent setting of filter clock.	Ext.
48h	Block size.	Comp.
64h	Start DMA to DAC in ESPCM low compression format.	Ext.
65h	Same as above but with reference byte flag.	Ext.
66h	Start DMA to DAC in ESPCM medium compression format.	Ext.
67h	Same as above but with reference byte flag.	Ext.
6Ah	Start DMA to DAC in ESPCM high compression format.	Ext.
6Bh	Same as above but with reference byte flag.	Ext.
6Eh	Start DMA to ADC in ESPCM low compression format.	Ext.
6Fh	Same as above but with reference byte flag.	Ext.
74h	Start DMA to DAC in ADPCM 4-bit format.	Comp.
75h	Same as above but with reference flag.	Comp.
76h	Start DMA to DAC in ADPCM 2.6-bit format.	Comp.
77h	Same as above but with reference flag.	Comp.

Continued

Table 7-7, ES1869 Commands *Continued*

Command	Function	Mode
7Ah	Start DMA to DAC in ADPCM 2.6-bit format.	Comp.
7Bh	Same as above but with reference flag.	Comp.
80h	Insert Silence period.	Comp.
90h	Start DMA to DAC in auto-init. format.	Comp.
91h	Start DMA 8-bit transfer to DAC.	Comp.
98h	Start high-speed 8-bit DMA from ADC in auto-init mode.	Comp.
99h	Start high-speed 8-bit DMA from ADC.	Comp.
Axh, Bxh, Cxh	ES1869 Extension Commands.	Ext.
C0h	Enables Reads of ES1869 registers used for Extended Mode: Axh, Bxh.	Ext.
C1h	Resume after Suspend.	Ext.
C6h	Extension command enable (for Axh, Bxh).	Ext.
C7h	Extension command disable (for Axh, Bxh).	Ext.
D0h	DMA pause.	Comp.
D1h	Voice DAC mixer input enable.	Comp.
D3h	Voice DAC mixer input disable.	Comp.
D4h	Continue DMA after D0h command.	Comp.
D5h	ES488 compatibility command - returns 1.	Ext.
D6h, D7h	ES488 compatibility commands-no effect.	Ext.
D8h	Voice DAC status return - 0 = disabled, FFh = enabled.	Comp.

ES1869 Extension Commands (Axh, Bxh, Cxh, Read/Write)

The ES1869 component supports a group of commands that provide additional functions not supported in by industry standard sound adapter compatible mode. Each of these commands has an associated register that is written when a command write occurs. A write process consists of first writing the command to 02nCh followed by the data.

Writing example:

```
Out 02nCh, Reg Nr      ; Register number to write to
Out 02nCh, Data        ;Desired register contents in hex
```

A read of an extension command register is accomplished with the C0h command.

Reading Example:

```
Out 02nCh, C0h         ;enable 1869 read
Out 02nCh, Reg Nr      ;Register number to read from
In, 02nAh              ;get the register contents
```

The read data available bit should be polled before reading the register contents.

Sample Rate Generator Register (A1h, Read/Write)

This 8-bit register holds the 2's compliment sample rate divider value that should be programmed for all ADC and DAC operations in extended mode. The sample rate is determined using the following formulas:

Bit <7> = 0, then 397.7 KHz / (128-X) = Sample Rate

Bit <7> = 1, then 795.5 KHz / (256-X) = Sample Rate where X = value of bits <6..0>.

Aih

BIT	FUNCTION
7	Sample Rate Clock Source Select: 0 = 397.7 KHz (sample rate <= 22 KHz) 1 = 795.5 KHz (sample rate > 22 KHz)
6..0	Sample Rate Divider Value

Filter Divider Register (A2h, Read/Write)

This 8-bit register determines the low pass frequency of the switched capacitor filters inside the ES1869. The filter clock frequency will be the roll-off frequency (80% of the sample rate divided by 2) multiplied by 82. The following formula is used by the register to determine the filter clock frequency:

7.16 MHz / (256-X) = Filter Clock Frequency where X = value of bits <7..0>.

DMA Transfer Counter Reload Registers (A4h, A5h Read/Write)

These registers hold the 16-bit 2's complement value that is copied into the FIFO transfer control counter after each overflow (and at the beginning of the initial DMA transfer). Register A4h is the low byte counter value, and A5h is the high byte counter value. The counter is incremented after each successful byte is transferred by DMA.

Program Type Register (A8h Read/Write)

This register selects either mono or stereo mode for DMA recording or playback.

A8h

BIT	FUNCTION
7..4,2	Reserved.
3	DMA Playback - Reserved. DMA Record Monitor: 0 = Record Monitor disable 1 = Record Monitor enable
1,0	Program Type: 10 = Mono 01 = Stereo

Interrupt Control Register (B1h, Read/Write)

This register determines IRQ generation by the **ES1869** component during audio operations.

B1h, Read/Write

BIT	FUNCTION
7	Processor IRQ: 0 = IRQ generation is disabled (extended mode) 1 = IRQ generation is enabled (compatibility mode)
6	DMA Counter Overflow IRQ: 0 = IRQ not generated 1 = IRQ generated for DMA counter overflow
5	FIFO Half-Empty IRQ: 0 = IRQ not generated 1 = IRQ generated for FIFO transitions (ext. mode)
4	IRQ Enable: 0 = All IRQs disabled 1 = IRQ generation is enabled
3..0	Interrupt Select: 0000= IRQ2, 9, all others 0101 = IRQ5 (default) 1010 = IRQ7 1111 = IRQ10

DMA Control Register (B2h, Read/Write)

This register determines DRQ generation by the ES1869 component during audio operations.

B2h, Read/Write

BIT	FUNCTION
7	Reserved for Game Compatible DRQ: (left at zero for Extended Mode)
6	Extended DMA DRQ: 0 = DRQ not generated (block I/O w/FIFO in ext. mode) 1 = DRQ generated for DMA in extended mode
5	Enable Game Compatibility DMA DRQ: 0 = DRQ not generated 1 = DRQ generated for DMA in game compatibility mode
4	Don't Care.
3..0	DMA Channel Select (Read Only): 0000 = All others selected 0101 = Ch 0 1010= Ch 1 1111 = Ch 3

Input Volume Control Register (B4h, Read/Write)

This register controls the stereo input volume. Each channel has 4 bits of resolution control, with a range of 0 dB to +22.5 dB in 1.5 dB steps. The low nibble (bits 3..0) controls the left volume, and the high nibble (bits 7..4) controls the right volume.

DAC/ADC Initialize and Configuration Registers (B6h, B7h Read/Write)

These registers are used to configure the DAC and ADC for a specific data format for playback (DAC) or record (ADC). Between the six format parameters (mono/stereo, 8-/16bit, and signed/unsigned), eight formats are available. The table below shows how registers B6h and B7h are set for the desired format. Note that B7h receives two bytes.

Table 7-8
DAC/ADC Configuration Register Loading

Format	Register B6h*	Register B7h
Mono, 8-Bit, Unsigned	80h	51h, D0h
Mono, 8-Bit, Signed	00h	71h, F0h
Mono, 16-Bit, Unsigned	80h	51h, D4h
Mono, 16-Bit, Signed	00h	71h, F4h
Stereo, 8-Bit, Unsigned	80h	51h, 98h
Stereo, 8-Bit, Signed	00h	71h, B8h
Stereo, 16-Bit, Unsigned	80h	51h, 9Ch
Stereo, 16-Bit, Signed	00h	71h, BCh

*Register B6h is used only when configuring the DAC (playback).

FM Synthesis Control Registers

The FM synthesis logic is typically mapped at 0388h-038Bh. A total of 243 control registers divided into two banks are available. The FM synthesis control registers are accessed by first writing the address of the control register to 0388h (for bank 0) or 038Ah (for bank 1) followed by writing the data to either 0389h or 038Bh. If a succeeding data byte is destined for the same control register, that control register's address need not be rewritten. Basically, FM synthesis is a write-only operation, as only one read, for status, is permitted. Table 7-9 lists the mapping of the FM synthesis logic.

Table 7-9
FM Synthesis Mapping

Address	Register	R/W
0388h	FM Synthesizer Register Address Write (Bank 0)	WO
0388h	FM Synthesizer Status Register	RO
0389h	FM Synthesizer Register Data Write	WO
038Ah	FM Synthesizer Register Address Write (Bank 1)	WO
038Bh	FM Synthesizer Register Data Write	WO

Table 7-10 lists the control registers for FM synthesis. Refer to the data sheet for the ES1869 for detailed register information.

Table 7-10
FM Synthesis Control Registers

Address	Bank 0 Function	Bank 1 Function
01h	Test - all 0s	Test - all 0s
02h	Timer 1	Not Used
03h	Timer 2	Not Used
04h	Timer Mask/Timer Start	4-Operator Configuration.
05h	Not Used	4-Operator Enable
08h	Key Scale (KSR) # Determiner	Not Used
20h-35h	AM, Vib., EG Type, KSR, Mult.	Same as bank 0
40h-55h	Key Scale Level, Tone Level	Same as bank 0
60h-75h	Attack Rate, Decay Rate	Same as bank 0
80h-95h	Sustain Level, Release Rate	Same as bank 0
A0h-A8h	Freq. Number	Same as bank 0
B0h-B8h	Key On, Block Octave, Freq. No.	Same as bank 0
BDh	Depth. of AM/Vib., Rhythm Mode	Not Used
C0h-C8h	Stereo Left/Right, Feedback, Conn.	Same as bank 0
E0h-F5h	Wave Select	Same as bank 0
Abbreviations	AM - Amplitude Modulation (tremolo) Vib - Vibrato Conn - Connection (oscillator configuration)	

Audio Subsystem Specifications

Table 7-11 lists the specifications for the audio subsystem.

Table 7-11
Audio Subsystem Specifications

Parameter	Minimum	Nominal	Maximum
Input Level:			
Microphone	10 mV	—	125 mV
Line	0.5 V	—	3.00 V
Input Impedance:			
Microphone	—	4 k ohms	—
Line	—	20 k ohms	—
Internal Microphone Sensitivity	—	-50db	—
Output Power (both channels)	—	0.45 watts rms @ 8 ohms	—
Headphone Output Impedance	8 ohms	32 ohms (recommended)	—

Graphics/Video Subsystem

The standard graphics subsystem consists of a graphics controller, frame buffer memory, and a Liquid Crystal Display (LCD). The graphics/video subsystem can alternately drive an external Compaq VGA monitor by switching between the internal display and the external VGA monitor. To utilize the full capabilities of the integrated VGA controller, a monitor that supports a horizontal refresh rate of 41.25 kHz and a vertical refresh rate of 62.8 Hz for 800 x 600 modes is required.

MultiMedia capabilities are provided by Motion Video Acceleration (MVA) for playback of video data. The Zoomed Video port provides video capabilities through optional PC Card MultiMedia hardware decoder cards (MPEG or Video Capture) for full-screen, full-motion viewing of TV/VCR video files stored in hard disk or CD-ROM drives. Stored video clips can also be displayed without hardware decoders through the preinstalled Mediamatics MPEG decoder software.

NOTE: This chapter describes general subsystem architecture, focusing largely on aspects unique to this system's graphics and video subsystem. For detailed information regarding BIOS and register programming for standard VGA modes, refer to the *Compaq QVision Video Graphics System Technical Reference Guide* p/n 073A/0693.

For detailed information regarding components used in this subsystem refer to the particular component's data sheet.

Subsystem **Ov*er*v*ie*w**

A general block diagram of the graphics/video subsystem is shown in Figure 8-1 and described in the following paragraphs.

Master Clock—Provides dot clock source at a frequency specified by the Miscellaneous Output Register. An external clock may be substituted through the video feature connector. In QVision modes a separate clock is generated for memory for optimum performance.

Graphics/Video ASIC—The Chips 65555 graphics/video component provides most of the graphics/video subsystem's functionality. The video BIOS code is contained within the 48-KB system BIOS ROM, video drivers are supplied with the system.

Frame Buffer—The graphics/video subsystem includes 2 MB of memory for frame buffer usage. Four, 50ns, 256K x 16 EDO DRAM components are accessed using a 64-bit interface. The EDO memory allows the MCLK to be set to 49 MHz.

Zoomed Video (ZV) Port—Provides direct connection between the VGA controller and external PC Card host adapter. The ZV port allows the PC Cards that are plugged into the host adapter to write video data directly into the video frame buffer.

CRT Monitor I. D. (DDC-2) —Provides a standard for the CPU to determine the type of VGA monitor that is connected to the system. DDC-2 is unidirectional and only allows reading of monitor information.

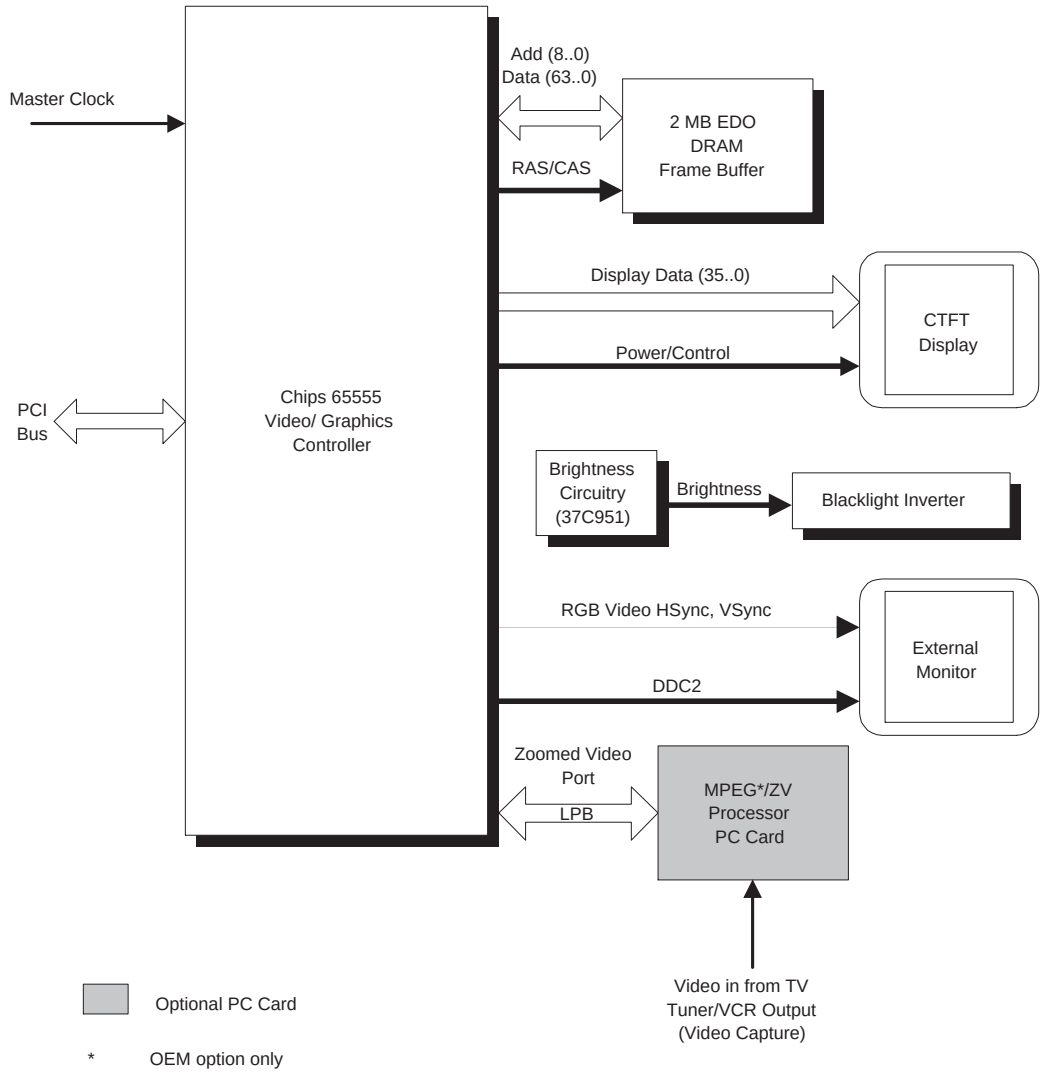


Figure 8-1. *Graphics/Video Subsystem, Block Diagram*

Graphics ASIC

The Chips 65555 graphics ASIC contains most of the functionality the graphics/video subsystem. The CHIPS 65555 graphics ASIC features a Motion Video Accelerator (MVA) that provides hardware support of video decompression and a Zoomed Video port. Other features include EDO DRAM support, multi-format frame buffering, YCrCb-to-RGB color space conversion, enhanced frame-rate buffering, and comprehensive resolution-compensation. The following paragraphs describe key functions of the 65555.

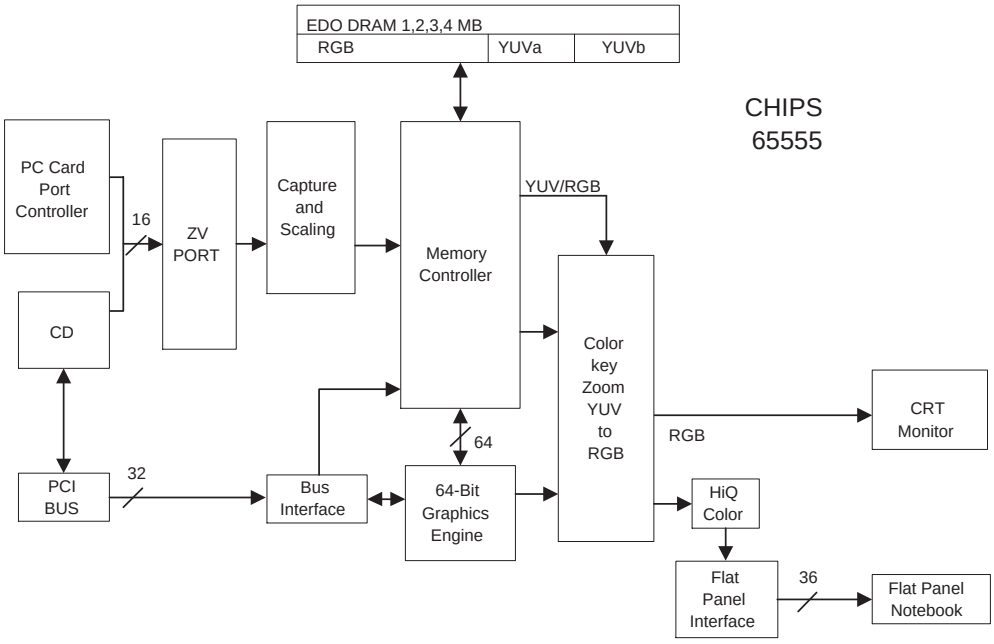


Figure 8-2. 65555 Graphics/Video ASIC, Block Diagram

Local Bus Interface

The 65555 is configured for PCI local bus operation. Memory and I/O accesses utilize a 64-bit bandwidth at up to 33 MHz, including burst cycle support. The 65555 is register-level compatible with software applications written for standard VGA, EGA, and CGA operation. Extended VGA modes and special features are supported through the video BIOS and supplied drivers.

Table 8-1 lists the I/O addresses used in the graphics subsection.

Table **8-***1*
65555 V*ideo/***G***raphics Controller Registers*

Address	**F***unction*
03B4h-03B5h	CRT Controller (monochrome)
03BAh	EGA Compatibility
03C0h-03C1h	Attribute Controller
03C2h	Miscellaneous Control (Write)/Input Status (Read)
03C3h	Controller Enable
03C4h-03C5h	Sequencer
03C6h-03C9h	VGA Color Palette
03CAh	Feature Control (Read)
03CCh	Miscellaneous Control Read)
03CEh-03CFh	Graphics Controller/Extended Mode Functions *
03D0h- 03D1h	Flat Panel Control
03D2h-3D3h	Multimedia Controller
03D4h-03D5h	CRT Controller (color)/Extended Mode Functions
03D6h-03D7h	Extended Mode Functions*
03D8h-03DBh	Compatibility
0E2.92h-0E2.93h	Contrast and Brightness (data R/W @ 0E3h)

* Extended Mode Functions use indexed addressing to access extended (super) VGA functions such as the BltBLT engine as well as LCD control and Motion Video Accelerator control functions. For detailed register descriptions refer to the data sheet for the Chipps 65555 video/graphics controller.

Memory Interface

The memory interface to the frame buffer handles the data transfers to and from the frame buffer in both text and graphics modes. This function provides formatting and manipulation operations that may be required of display data. The memory interface is also responsible for taking the output of the master clock and generating timing and control signals used by all other graphics subsystem functions.

Attribute Controller

The attribute controller processes the data from the frame buffer and provide text blinking, highlighting, underlining, and reverse. A 16-of-64 color palette is included for EGA compatibility.

BitBLT Engine

The Bit Block Transfer (BitBLT) engine is activated in S and/or extended VGA modes and provides hardware support for moving blocks of data from one area of the frame buffer to another with minimum CPU intervention. The BitBLT engine can also provide pattern fills, raster ops, and color expansion or transparency. These operations enhance the performance of graphics user interface (GUI) such as Windows that typically call for high-resolution packed-pixel graphics modes.

Screen-to-Screen BitBLT

This function copies a rectangular bitmap from one section of the frame buffer to another. The memory addresses are generated by the BitBLT engine without CPU intervention. The graphics subsystem is programmed with the bitmap width, height, source address, destination offset address, an increment/decrement selection for the copy direction, and the pitch between scanlines. The registers allow the flexibility to move non-byte aligned and overlapping blocks.

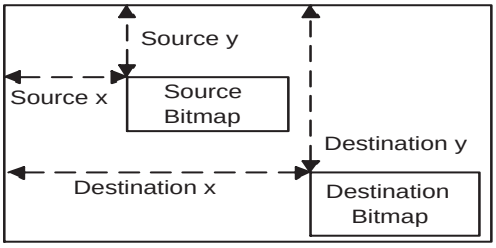


Figure 8-3. Screen-to-Screen BitBLT

CPU-To Screen BitBLT

This function facilitates the transfer of data from the microprocessor to the screen. Both planar (color-expand) and packed pixel views are supported. In planar modes, the data is transferred from the microprocessor as bytes, words, or dwords.

Pattern-to-Screen BitBLT

Pattern-to-Screen BitBLTs are useful for filling portions of the frame buffer with a repetitive pattern that may be as complex as a multi-color bitmap or as simple as a solid color. Simple patterns can be transferred to the screen in a single packed-pixel or color-expand BitBLT. More complex patterns may require multiple BitBLTs.

Color Expansion

Color expansion is the automatic conversion of a monochrome bitmap (which typically defines a character, icon, or pattern) into foreground and background values. These values are written to memory and also held in registers. Write performance of the CPU is improved by optimizing Host bus bandwidth since single bits are expanded across the bus into 8- or 16-bit pixels.

Cursor Engine

The cursor engine provides hardware support of the cursor indicator and replaces the need for software to continually save and restore cursor draw data as the pointing device position is changed. Once the software has initiated the cursor engine, only x-y data needs to be updated, allowing much smoother cursor operation. The cursor is overlaid on top of graphics and/or video information and can be either a 64 x 64 bit pattern (8 pattern choices) or a 32 x 32 bit pattern (with up to 32 pattern choices). Each pixel in the pattern can be transparent or one of two colors from the extended palette.

Video Playback

Full-screen video playback of software-decompressed DCI-compatible video clips (MPEG files) from a HDD/CD-ROM. Decoding and playback of MPEG video from files stored in the HDD or CD-ROM is provided through the CPU under Mediamatics software control without additional hardware decoders. Optional MPEG and Video Capture PC Card multimedia cards are also available to provide hardware decoding of video input signals.

RAMDAC

The RAMDAC contains the color palette (also known as the color look up table (CLUT)) that is used for color processing of the graphics data for some modes. An extended palette is also provided for color support for the cursor engine and border functions. The DAC portion provides the digital-to-analog conversion for an external color monitor. Color-processed data is also distributed to the LCD controller. The RAMDAC also provides the overlaying of motion video data.

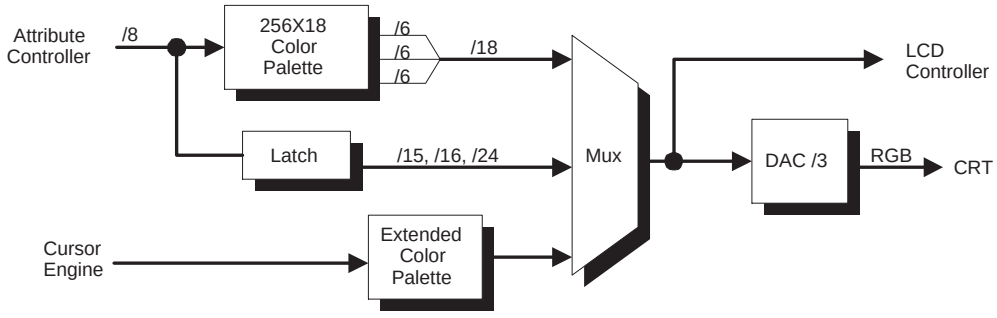


Figure 8-4. RAMDAC Block Diagram.

Color Processing With Palette

The color palette consists of a 256 x 18-bit color lookup table (CLUT) that provides three 6-bit values (an 18-bit word) to determine the hue from the primary colors of red, green, and blue. Using an 8-bit color code input, the CLUT can support a simultaneous display of up to 256 out of 262,144 ("256K") colors. For VGA modes using up to 256 colors at a time, the color palette provides very fast color processing.

Direct-/True-Color Processing

The color palette (CLUT) is bypassed in direct- and true-color VGA modes, which allow 32K, 64K, and 16 million colors to be displayed simultaneously. In these modes, pixel color data is received from the attribute controller, selected by the mux and applied to the DAC. More data is required from the frame buffer but of course more colors are available. Performance is maintained by using a higher video clock frequency in these modes.

Digital-To-Analog Converter (DAC)

The DAC converts digital video data to three analog signals (Red, Green, and Blue) for routing to a CRT monitor. The output voltage is based on the .7 volt standard for a white pixel.

Dithering Engine

The dithering engine intermingles pixels of available colors together to produce a perceived color that is otherwise unavailable. This technique increases the number of colors in a given display mode relative to what the display is capable of without dithering. A pattern is used to add as many as six bits of resolution per primary color. Dithering can be applied to both the main graphics display as well as the motion video window. The amount of dithering can be set for automatic or can be programmed.

CRT Controller

The CRT controller generates horizontal and vertical blanking and synchronization signals required by an external CRT monitor. Simultaneous LCD/CRT display capability is possible depending on the display mode, the LCD panel type, and CRT type used.

LCD Controller

The LCD controller processes the video data for display on the LCD and provides power sequencer and screen save functions. A dithering engine uses a pattern and frame rate modulation to produce grey shades with a minimum of flicker on the LCD screen.

Power Management

The 65555 includes controls and features that support the system's power management functions to maximize battery life. The following subsections describe the Local Standby and Global Standby (Suspend) modes of the 65555 during the system unit's power conservation states.

Local Standby Mode

In Local Standby, the unit's applications are active (microprocessor is still processing data) and the 65555 continues to process display data. The Local Standby mode is entered through software control after a predetermined period of subsystem inactivity time has elapsed.

For software initialization of Standby, the 65555 power management register CR20 (3D5.20h) bit <4> is set. Standby is entered upon timeout if no hardware activity has occurred.

The following states occur in the 65555 during Standby:

- LCD and LCD controller are powered down.
- CRT controller is powered down.
- VCLK is stopped.
- RAMDAC is in low power mode.
- Frame buffer memory is refreshed at a slower rate.
- Microprocessor can still access the graphics subsystem for memory/palette updates.

Suspend Mode

The 65555 enters its Suspend mode when system unit enters Global Standby, which occurs either as a software- or hardware-initiated function. When Suspend mode is initiated, the 65555 Software Configuration register SR23 (3C5.23h) bit <5> is cleared and the SUSPI pin (87) is pulled active, resulting in the additional situations:

- MCLK is stopped
- CPU cannot access 65555 registers or frame buffer
- Frame buffer contents are preserved

CRT Monitor Control

The 65555 supports Display Power Management Signaling (DPMS) criteria specified by the EPA Energy Star Computer Program and by VESA for controlling an external CRT monitor that is DPMS-compatible.

Table 8-2 describes the CRT monitor control register settings and the resulting sync and CRT monitor status.

Table **8-2**
DPMS-Compliant CRT Monitor Control

G*RE Reg.* *Bits* **<2**,*1***>**	**V***SYNC*	**H***SYNC*	*CRT Monitor Status*
00	active	active	On. Full power consumption
01	active	inactive	Standby. Nominal power, short recovery time to On.
10	inactive	active	Suspend. Significant power reduction, long recovery to On.
11	inactive	inactive	Off. Minimum power consumption, long recovery to On.

For more information on power management refer to “Power Conservation” in *Appendix B* of this manual.

Zoomed Video Port

The Zoomed Video (ZV) port is a point to point, uni-directional, video bus that allows video data from a PC Card device to be transferred directly into the VGA frame buffer over a dedicated bus in real time without extra data buffering or bus arbitration logic. Either a composite or S-video signal can be received with automatic input signal detection provided. The PC Card hardware performs decoding/digitizing and routes the video signal in YUV 4:2:2 format to the Zoomed Video port. The zoom video interface performs video processing, and routes the 16-/32-bit video data (along with the 3-bit audio data) to the 65555 over the zoom video bus for on-screen viewing.

Video capturing to disk is done by the CPU through the zoomed video port. The CPU takes the video data out of the display frame buffer and sends it to the mass storage device directly, thus allowing the stored data to be viewed as it is being stored.

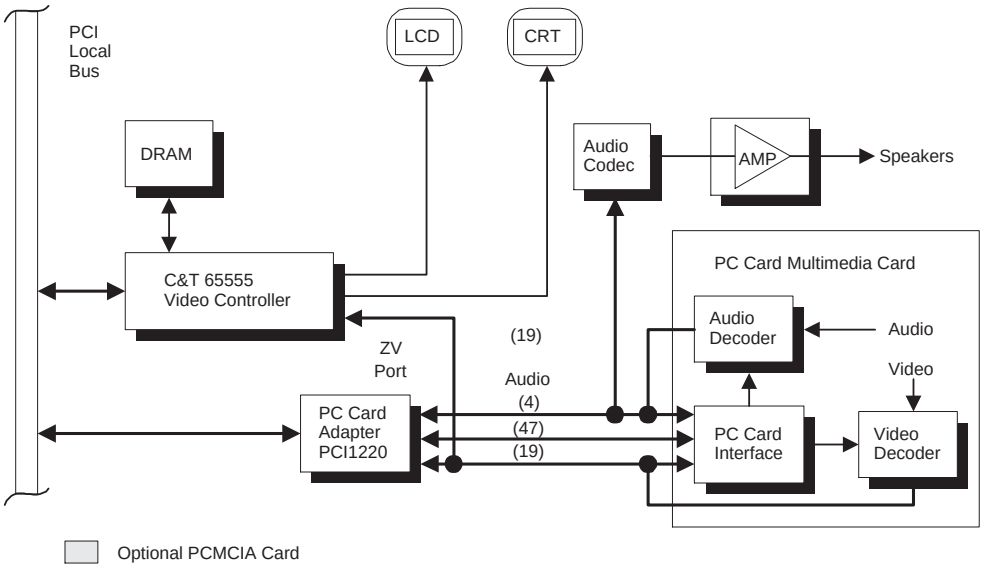


Figure 8-5. Zoomed Video Multimedia Port Block Diagram

When the optional video PC Card is installed, and the PC Card host adapter is switched to the ZV multimedia mode, the bussing is as shown in Figure 8-5. In this special mode the CPU control and data will follow the same data path to the card as it would for any standard PC Card device, but the addressing range is restricted to 32, sixteen-bit I/O ports. The unused address range is used to define the 19-pin ZV data bus and as control for a four-channel digital audio. The multimedia PC Card does not support memory mapped addressing.

Zoomed Video/LPB Signals

The PC Card, ZV, and LPB signals and their functions are given in Table 8-3.

Table 8-3
PC Card Port

PC Card Signal Name	*PC Card Pin Number*	*Zoomed Video*	*LPB Signals*	*Function*
-IOIS16	33	PCLK	LCLK	Pixel Clock to ZV Port
A10	8	HREF	~VREQ/HS	Horz. Sync to ZV Port
A11	10	VS	~CREQ/VS	Vert. Sync to ZV Port
A9	11	Y0	LD0	Video Data to ZV Port (YUV:4:2:2)
A17	46	Y1	LD1	Video Data to ZV Port (YUV:4:2:2)
A8	12	Y2	LD2	Video Data to ZV Port (YUV:4:2:2)
A18	47	Y3	LD3	Video Data to ZV Port (YUV:4:2:2)
A13	13	Y4	LD4	Video Data to ZV Port (YUV:4:2:2)
A19	48	Y5	LD5	Video Data to ZV Port (YUV:4:2:2)
A14	14	Y6	LD6	Video Data to ZV Port (YUV:4:2:2)
A20	49	Y7	LD7	Video Data to ZV Port (YUV:4:2:2)
A21	50	UV0	LD8	Video Data to ZV Port (YUV:4:2:2)
A22	53	UV1	LD9	Video Data to ZV Port (YUV:4:2:2)
A16	19	UV2	LD10	Video Data to ZV Port (YUV:4:2:2)
A23	54	UV3	LD11	Video Data to ZV Port (YUV:4:2:2)
A15	20	UV4	LD12	Video Data to ZV Port (YUV:4:2:2)
A24	55	UV5	LD13	Video Data to ZV Port (YUV:4:2:2)
A12	21	UV6	LD14	Video Data to ZV Port (YUV:4:2:2)
A25	56	UV7	LD15	Video Data to ZV Port (YUV:4:2:2)
INPACK-	60	I^2S _LRCLK	I^2S _LRCLK	I^2S Audio L/R Select PCM
BVD2/SPKR-	62	I^2S _DATA	I^2S _DATA	I^2S Audio PCM Data
A7	22	I^2S _SCLK	I^2S _SCLK	I^2S Data Clock
A6	23	I^2S _MCLK	I^2S _MCLK	I^2S Master Clock
A5	24	RESERVED	RESERVED	N/C in PC Card. (3 state)
A4	25	RESERVED	RESERVED	N/C in PC Card. (3 state)
A[3:0]	26:29	ADD[3:0]	ADD[3:0]	Used for accessing PC Card

MPEG-1

The MPEG software decoder decompresses MPEG-1 stream data, which includes video and audio information. The decompressed video data is distributed in 4:2:2 YUV format back to the 64V+ controller, which transfers the video data to the video memory. The MPEG audio data stream, which contains left and right channel information, is converted into separate left and right digital I^2S signals that are routed to the audio subsystem.

MPEG-1 Video Data Structure

Video information is contained in a portion of the stream called a video sequence. A video sequence (Figure 8-6) starts with a sequence header, followed by one or more picture groups, and ending with a sequence end code.

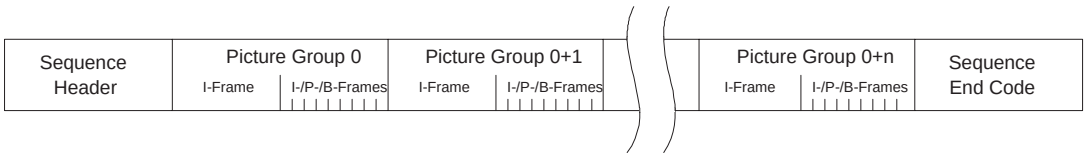


Figure 8-6. MPEG-1 Video Sequence

Each picture group contains a set of frames. Video data compression is based on the fact that there is a large amount of redundancy (little change) from moment to moment on a video display. In a given video sequence and within picture groups, video information can be more efficiently coded based on differences (changes in the picture) from frame to frame than on the picture itself. Three types of frames are used:

- Intra (I-) Frames: I-Frames are coded using Joint Photographic Experts Group (JPEG) compression and contain only picture data. These frames provide the basis for P- and B-Frame production and are also used as reference points for MPEG file scanning. I-Frames offer the least amount of data compression, but are used at a much lower rate than P- or B-Frames, typically no more than twice a second. A picture group always starts with an I-Frame.
- Predicted (P-) Frames: P-Frames are coded by predicting image redundancy with respect to the preceding I- or P-Frame. Motion compensation is utilized in coding to allow more data compression.
- Bidirectional Interpolated (B-) Frames: B-Frames are coded using predicted redundancy data from both preceding and succeeding I- and P-Frames, providing a higher degree of both accuracy and data compression. This third frame type distinguishes the MPEG system from the .AVI type of coding, which uses two frame types for video data compression.

Each frame can be further broken down into sub-units identified as slices, macroblocks, and, finally, blocks (Figure 8-7).

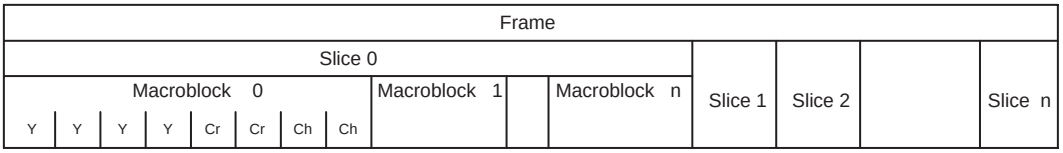


Figure 8-7. *Video Frame Format*

The block holds the values based on the CCIR 601 standard for color subsampling. Each block represents an 8-pixel × 8-line set of values for a luminance (Y) or chrominance (Cr or Cb) component. Upon decoding, the video data is output in a 4:2:2 format, meaning that for every 4 luminance (Y) samples there are 2 chrominance samples for CR (red minus Y) and 2 chrominance samples for Cb (blue minus Y).

MPEG-1 Audio Data Structure

The MPEG-1 includes audio information that is decoded into a serial bit stream. This stream is routed along with a clock signal and a signal that identifies the left and right channel information (Figure 8-8) to the MPEG audio DAC. The sampling rates are programmable for 32, 44.1, or 48 KHz.

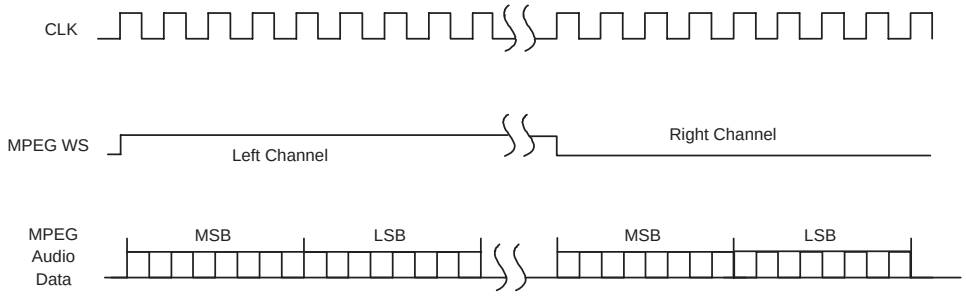


Figure 8-8. *Decoded MPEG-1 Audio Stream*

The MPEG DAC provides digital-to-analog conversion of the audio data and provides two signals (left/right) to the audio subsystem.

Liquid Crystal Display (LCD)

Tables 8-4 and 8-5 list the key parameters of the active (TFT) matrix display.

Table **8-4**
12.1-Inch CTFT, SVGA Display

	U.S.	Metric
Dimensions		
Height	7.24 in	18.4 cm
Width	9.7 in	24.6 cm
Number of Colors	64K	
Contrast Ratio	100:1 minimum	
Pixel Resolution		
Pitch	0.30 × 0.30 mm	
Format	800 × 600	
Configuration	RGB Stripe	
Backlight	Edge Lit	
Character Display	80 × 25	

Table **8-5**
13.3-Inch CTFT, XGA Display

	U.S.	Metric
Dimensions		
Height	7.9 in	20.1 cm
Width	10.6 in	26.9 cm
Number of Colors	64K	
Contrast Ratio	100: 1 minimum	
Pixel Resolution		
Pitch	0.29 x 0.29 mm	
Format	1024 x 768	
Configuration	RGB Stripe	
Backlight	Edge Lit	
Character Display	80 × 25	

Brightness Control

The brightness of the TFT LCD display is controlled by a hot key **(F10)** that affects a signal applied to the backlight inverter board. Keyboard inputs used to adjust the brightness are handled by system management (SM) firmware.

A 2-MHz pulse width modulator (PWM) timer is used to establish the brightness signal output duty cycle from 0% (min. brightness) to 100% (max. brightness). Brightness duty cycles are adjusted at a resolution of 1/128 (00h) for 0% duty cycle up to a value of 127/128 (FFh) at 100% duty cycle. The brightness control register (PWM0) used to configure the PWM clocking and output polarity is located in the 37C951 at address E2h (E3h data) index 92h.

Display Modes

The graphics subsystem provides one of two types of displays: text or graphics.

Text Modes

The text display uses a multiplane configuration where a character, its attributes, and fonts are stored in the separate memory planes. Table 8-6 lists the text configurations provided by the video system. Note that the text configurations for CGA/MDA, EGA, and VGA share common video BIOS modes that result in the same format but provide different pixel resolutions.

Table **8-6**
Text Display Modes

Software Interface				*Video BIOS Mode*	*Format*	*Pixel Resolution*	*Number of Colors*	*Display*
				0	40 x 25 Text	320 x 200	16	LCD/CRT
			CGA	1	40 x 25 Text	320 x 200	16	LCD/CRT
				2	80 x 25 Text	640 x 200	16	LCD/CRT
				3	80 x 25 Text	640 x 200	16	LCD/CRT
		EGA	MDA	7	80 x 25 Text	720 x 350	Mono	LCD/CRT
				0 *	40 x 25 Text	320 x 350	16	LCD/CRT
	VGA			1 *	40 x 25 Text	320 x 350	16	LCD/CRT
				2 *	80 x 25 Text	640 x 350	16	LCD/CRT
SVGA				3 *	80 x 25 Text	640 x 350	16	LCD/CRT
				0+	40 x 25 Text	360 x 400	16	LCD/CRT
				1+	40 x 25 Text	360 x 400	16	LCD/CRT
				2+	80 x 25 Text	720 x 400	16	LCD/CRT
				3+	80 x 25 Text	720 x 400	16	LCD/CRT
				7+	80 x 25 Text	720 x 400	Mono	LCD/CRT
				14	132 x 25	1056 x 400	16	CRT
				54	132 x 43	1056 x 350	16	CRT
				55	132 x 25	1056 x 350	16	CRT

Graphics Modes

The graphics subsystem can operate in either of two fundamental graphics modes: multiplane or packed pixel. The multiplane (MP) mode provides four graphics planes in memory, each plane simultaneously supplying one bit of the 4-bit code that defines a particular color. The packed-pixel (pp) mode allows software to use as many as 16 bits to determine a particular color. The graphics modes are listed in Table 8-7.

Table **8-7**
G*raphics Display Modes*

*Soft***w***are Interface*	**V***ideo BI***O***S Mode*	*Pi***x***el Resolution*	**N***umber of Colors*	*Display Compatibility*	
				L*CD Panel*	*E***x***t. CRT Monitor* *
	4	320 x 200 @ 2 bpp	4	VGA, SVGA	VGA, SVGA
CGA	5	320 x 200 @ 2 bpp	4	VGA, SVGA	VGA, SVGA
	6	640 x 200 @ 1 bpp	2	VGA, SVGA	VGA, SVGA
	D	320 x 200 (MP)	16	VGA, SVGA	VGA, SVGA
EGA	E	640 x 200 (MP)	16	VGA, SVGA	VGA, SVGA
	F	640 x 350 (MP)	Mono	VGA, SVGA	VGA, SVGA
	10	640 x 350 (MP)	16	VGA, SVGA	VGA, SVGA
	11	640 x 480 (MP)	2	VGA, SVGA	VGA, SVGA
VGA	12	640 x 480 (MP)	16	VGA, SVGA	VGA, SVGA
	13	320 x 200 @ 8 bpp	256	VGA, SVGA	VGA, SVGA
	16	640 x 480 (MP)	16	VGA, SVGA	VGA, SVGA
	17	800 x 600 (MP)	16	SVGA	SVGA
	18	1024 x 768 @ 4 bpp	16	---	SVGA
	58,6A	800 x 600 @ 4 bpp	16	SVGA	SVGA
	5C	800 x 600 @ 8 bpp	256	SVGA	SVGA
	5D	1024 x 768 @ 4 bpp	16	---	SVGA
SVGA	5E	640 x 400 @ 8 bpp	256	VGA, SVGA	VGA, SVGA
	5F	640 x 480 @ 8 bpp	256	VGA, SVGA	VGA, SVGA
	60	1024 x 768 @ 8 bpp	256	---	SVGA
	64	640 x 480 @ 16 bpp	64K	VGA, SVGA	VGA, SVGA
	65	800 x 600 @ 16 bpp	64K	SVGA	SVGA
	66	640 x 480 @ 15 bpp	32K	VGA, SVGA	VGA, SVGA
	67	800 x 600 @ 15 bpp	32K	SVGA	SVGA
SXGA		1024 x 768 @ 16 bpp	256	---	VGA, SVGA, XGA
		1280 x 1024 @ 8 bpp	256	---	VGA, SVGA, XGA

* Optional

The 65555 provides resolution compensation for display modes that have a lower than maximum resolution than LCD panel is capable of. This compensation provides a full LCD screen display for lower resolution display modes.

Status Indication

The LCD pop-up status indicators provide system status that is displayed on the LCD display panel after any one of the hot keys on the internal keyboard are depressed.

The displayed system status information includes the following:

- Popup Icon Location (F1)
- Firmware Version (F2)
- Speaker audio volume (F5)
- QuickLock (F6)
- Power Management Mode (F7)
- Display brightness (F10)

Keyboard/Pointing Device Subsystem

The internal keyboard consists of a keyboard matrix with keyboard controller on the system board, an integrated touchpad pointing device, and select buttons. The computer and optional Convenience Bases have a connector for an external full-sized keyboard and mouse.

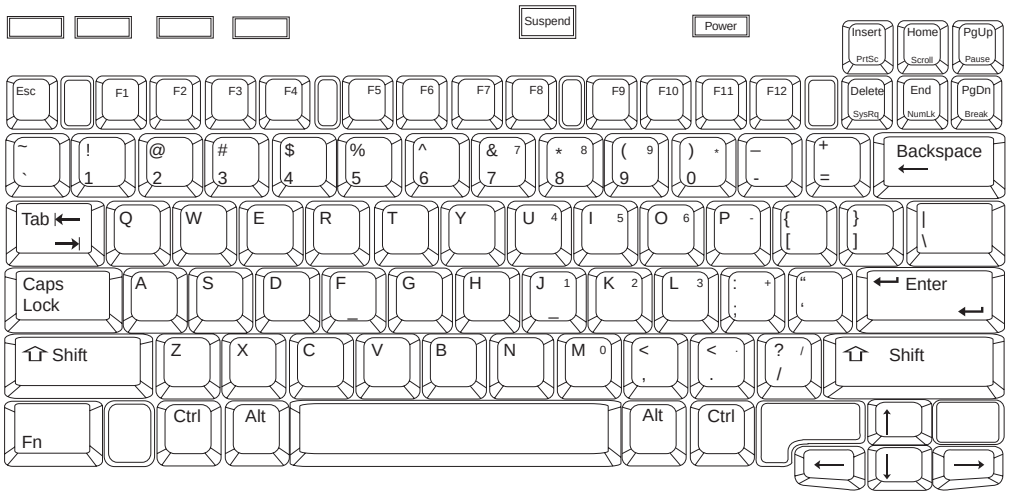
Internal Keyboard

The internal keyboard provides all the functionality of the full-sized keyboard with 12 function keys. The keyboard membrane is automatically identified by the system through the keyboard controller KSO (KSO0 - KSO3) and GPIO18 (KSIN15) scan lines.

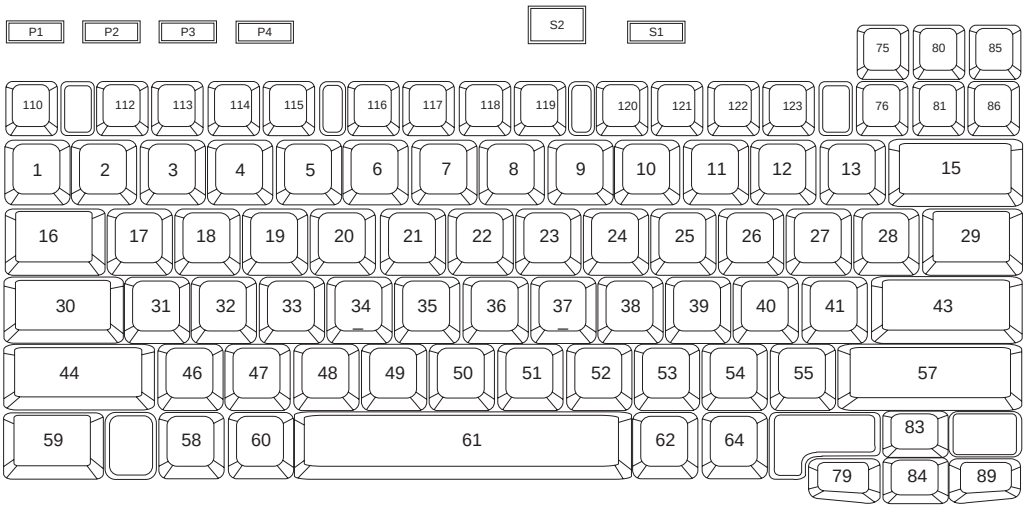
The keyboard assembly has four additional keys located above the standard keys that are used as Windows and application logo keys, and as user programmable keys to enable programs and custom or frequently used functions to be activated with a single keystroke. Located on the left side of the computer (if it is facing you) is the audio volume control buttons. Also located above the standard keys is the Suspend mode button, and the power on/off slide switch.

Five LEDs located above the Suspend mode button indicate MultiBay, Hard drive Bay, Scroll Lock, Num Lock, and Caps Lock status. Two other indicator LEDs located below the touch pad indicate Power/Suspend and battery charger status. The two pick buttons for the pointing device are positioned below the pointing device.

System status information is provided through a popup screen display when any of the hotkeys (F4-F10, and T) are depressed along with the Fn key. The different character sets are selected through Setup.



F**igure **9-1. U.S. Enhanced Internal Keyboard Layout



F**igure **9-2. Internal Keyboard Assigned Key Location Numbers.

K*eyboard Control*

Keyboard control is provided by the 8051 keyboard controller in the SMC FDC37C95x FR Ultra I/O (MSIO) on the system board. Keyboard scanning is accomplished by the keyboard controller scan logic which provides 14 scan out (KSO) lines and 8 scan input (KSI) lines forming a 96-key (12 × 8) scan matrix. When all KSO lines are driven active, the scan logic can then generate an interrupt when any KSI line is activated. This type of scanning allows the keyboard controller to wait for a key depression rather than repeatedly polling the entire matrix.

Modifier keys (Shift, Ctrl, Alt, and Fn) are positioned in the matrix by diodes to allow three-key combinations and to prevent aliasing.

Functional Description

After power-on occurs, the default (initial state) conditions of the keyboard are:

- Embedded keyboard is enabled if the optional external keyboard is not present.
- Scroll Lock and Caps Lock LEDs are off. The Num Lock LED is defined in the system setup.
- Typematic rate = 10 characters/sec (+/- 20%)
- Typematic delay = 500 milliseconds (+/- 20%)

The keyboard controller has both a first-in, first-out (FIFO) buffer and a repeating key function. Both make and break codes are generated when keys are used. Make codes are transmitted when a key is pressed, break codes when it is released. This combination of codes is referred to collectively as the "scan codes" of a key.

Scan codes for up 8 characters (24 bytes) are stored in the FIFO buffer if the system cannot immediately accept them when they are generated. If two or more keys are pressed simultaneously, the keyboard processes the first scan code detected and stores the others in the buffer in the order in which they are detected. If a key is pressed when the buffer is full, no scan code is generated. An overrun code is stored in the last buffer location, which is reserved for overrun conditions.

Modes of Operation

The default mode at power-up is the Normal mode. Enhanced operation is available in the Normal mode. QWERTY, numeric pad, and separate cursor key functions are available.

Normal Mode

The Normal mode is compatible with a standard 11-bit serial keyboard interface. Each key has a unique make and break code. The make code is transmitted when the key is pressed, and the break code is transmitted after the key is released. The non-standard keyboard scan codes for this mode are shown in Tables 9-1 and 9-2.

Num Lock Key

The **Num Lock** key provides access to the embedded numeric keys. The operation of the embedded keypad depends on the state of the **Num Lock** key.

Function (Fn) Key

The operation of the **Fn** (function) key is unique; its only purpose is to flag the system keyboard controller.

The following tables and paragraphs describe the combined effects of the keypad, **Fn** key, and **Num Lock** key on the keyboard controls.

Embedded **N***umeric* **K***eypad*

The embedded numeric keypad (Figure 9-3) is a set of 16 keys and is enabled and disabled by the **Num Lock** key. If **Num Lock** is on, the embedded numeric keypad is enabled; if **Num Lock** is off, the keypad is disabled. When enabled, the embedded keypad transmits the scan codes of the enhanced numeric keypad. In this mode, the **Shift** key enables the cursor-control functions instead of the numeric functions as it would on an enhanced keyboard.

If **Num Lock** is off, the embedded keypad may also be enabled if the **Fn** key is pressed. When the **Fn** key is released, the keyboard returns to the QWERTY mode. If the **Fn** key and the **Shift** keys are pressed simultaneously, the embedded keypad functions as cursor-control keys.

If **Num Lock** is on, regular (QWERTY) keyboard activity can be enabled temporarily by holding down the **Fn** key. When the **Fn** key is released, the embedded keypad is enabled.

The embedded keypad is disabled if an external keyboard or keypad is present. The keyboard remains enabled.

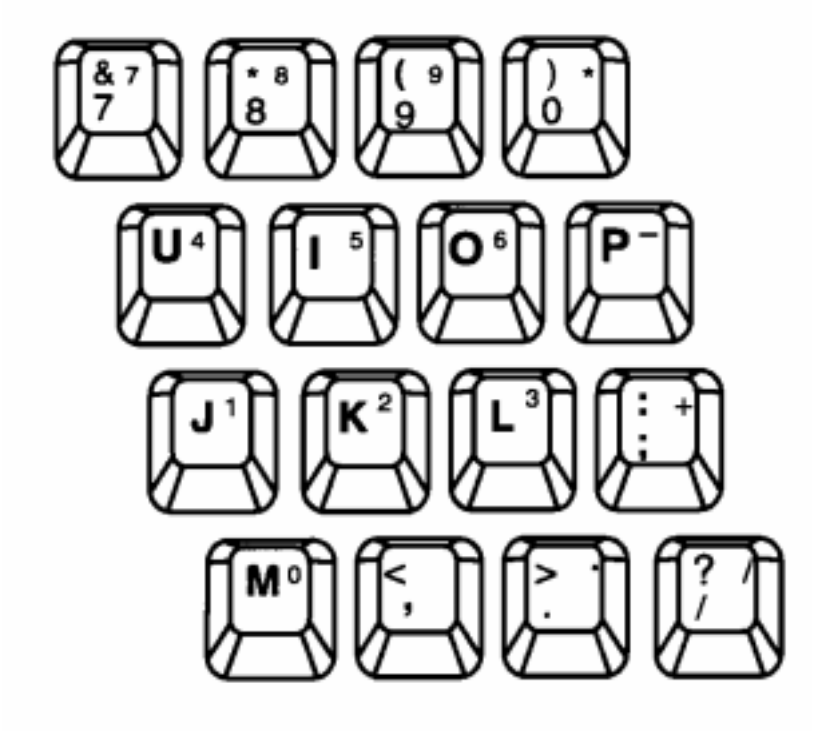


Figure 9-3. Internal Keyboard Embedded Numeric Keypad Layout

Cursor- and Screen-Control **F***unctions*

The embedded numeric keypad also provides cursor- and screen-control functions. During regular (QWERTY) keyboard activity, these functions can be accessed by pressing the **Fn** and **Shift** keys. Releasing the **Fn** key returns the keypad to normal keyboard operations.

If **Num Lock** is on (embedded numeric keypad enabled), pressing the **Shift** key enables these functions. Releasing the **Shift** key returns the keypad to numeric keypad operations.

When cursor- and screen-control functions are active, the *, +, -, and / arithmetic functions are also active. Some applications require the use of the cursor- and screen-control functions in the embedded numeric keypad rather than in the cursor control cluster.

Typematic **F***unction*

When a key is held down, it will have a repeating rate of 10 (+/- 1) Hz after a delay of 500 (+/- 100) milliseconds. If multiple keys are depressed, the last depressed key is valid for typematic action. Autorepeating will stop when the last depressed key is released.

Break codes of keys released are sent during the typematic transmission. The typematic action consists of multiple transmissions of the make code.

Typematic transmission of multibyte make codes require a one millisecond delay between each make code byte. This delay is measured from the falling edge of the stop bit of the first make code to the falling edge of the start bit of the next make code. After a one millisecond delay, the keyboard will check the status of the KBDCLK line and respond with the proper protocol procedure (i.e., RTS). If the computer system has clamped the KBDCLK low, the keyboard will restart the one millisecond delay again. This operation will repeat until the next make code byte is sent.

K*eyboard Scan Modes*

Normal mode with Scan Set 2 non-standard scan codes for the keyboard subsystem are given in Tables 9-1 and 9-2. Scan codes not listed are industry standard scan codes. The keyboard translates the Scan Set 2 scan code to produce the Scan Set 1 system codes.

N*ormal Mode Scan Codes* **(***Scan Set* **2)**

Normal mode is the default mode of the enhanced keyboard. In this mode, the keyboard controller translates the make codes generated by the keyboard and converts them to the AT 101/102 keyboard Scan Set 1 system codes required by the system BIOS.

In the Normal mode, the keyboard generates the break code, a 2-byte sequence that consists of a make code immediately preceded by F0h.

Table 9-1 lists the non-standard scan codes for the keyboard operating in the Normal mode. Refer to the keyboard key assignments in Figures 9-1 and 9-2 for keyboard key locations.

Table **9-***1*
N*on-Standard Scan Codes* **(H***ex)* *for the* **N***ormal Mode*

K*ey* **L***ocation*	*Scan Set* **2** *Make Code*	*Scan Set* **2** *Break Code*	*Scan Set 1 System Code*
14 ****	6*A*	*F0* 6*A*	7*D*
29 *	5*D*	*F0* 5*D*	***2****B*
42 **	5*D*	*F0* 5*D*	***2****B*
45 ***	6***1***	*F0* 6***1***	56
56 ****	5***1***	*F0* 5***1***	—
70 ****	67	*F0* 67	—
7***1*** ****	6***4***	*F0* 6***4***	—
7***2*** ****	***13***	*F0* ***13***	—
*P****1***^	***1***0	*F0* ***1***0	65
*P****2***^	***2***0	*F0* ***2***0	67
*P****3***^	***3***0	*F0* ***3***0	69
*P****4***^	***4***0	*F0* ***4***0	6*B*

NO*TE*: * U*.S. keyboard only*
** I*nternational and Japanese keyboard*
*** I*nternational keyboard only*
**** J*apanese keyboard only*
^ U*ser programmable keys*

Table **9-2**
F*unction* **K***ey Scan Code for the* **N***ormal Mode*

F*n key* **(59) +** **K***ey* **N***umber*	*Make Code*	*Break Code*
Fn+5***8***	*E0* ***14***	*E0 F0* ***14***
Fn+75*	*E0* ***12*** *E0 7C*	*E0 F0 7C E0 F0* ***12***
Fn+76*	***84***	*F0* ***84***
Fn+*80**	7*E*	*F0* 7*E*
Fn+***81****	77	*F0* 77
Fn+*85**	*E1* ***14*** 77	*E1 F0* ***14*** *F0* 77
Fn+*86**	***14*** *E0* 7*E*	*E0 F0* 7*E F0* ***14***
Fn+***112****	7***8***	*F0* 7***8***
Fn+***113****	07	*F0* 07

NO*TE*: *U*.S. keyboard only*

Hotkeys

Hotkeys and buttons are used to provide the user with easy access to various functions by using Fn keys or pushbuttons. The hotkeys and system responses are listed in Table 9-3 along with the indices to locations in memory for these and other system operations.

Table 9-3
Hotkey and SMI Switch/Key Parameters

Key Combination or Switch	Function	System Response
Fn + Esc	BIOS version	BIOS version information
Fn + F1	Popup Icon	Adjust location of popup icon
Fn + F3	Unused	
Fn + F4	CRT/LCD switch	Cycles between CRT and /LCD and both
Fn + F5	Warning Beep Control	on/off
Fn + F6	QuickLock/QuickBlank	Locks keyboard and turns off display
Fn + F7	Power Mgt.	Allows Power Drain level to be set
Fn + F8	Fuel Gauge	Displays battery charge condition
Fn + F9	Unused	
Fn + F10	Brightness	Display Brightness setting
Fn + F11	Reset ESCD	See note
Fn + F12	Unused	
Fn + T	Stretch Video	Toggles the stretch video functions
Arrow Keys	Cursor Movement	Left, Right, Down, Up cursor (respectively)
Esc	Escape key	Escape functions
Lock Icon	Request Lock Icon	Keyboard/mouse activity while locked
Unlock Icon	Request Unlock Icon	Valid password entered while locked
Suspend Button	Suspend SMI	Enters/Exits Suspend Mode
Fn + Suspend Button	Hibernate SMI	Enters/Exits Hibernation Mode
Off Button	Power Off SMI	System power off

Note: Fn + F11 clears the ESCD configuration information. If the Fn + F11 sequence is pressed very early after powering the machine on (after you see the keyboard LEDs blink, but before the video is initialized), CMOS memory will be invalidated. The ESCD is cleared, the machine is reset and boots with the "162 - System Options Not Set" message. This is a way to clear out configuration information, such as Windows 95's knowledge about a docking station. It may help clear up problems if the configuration information had been corrupted. Timing of this keystroke sequence is critical, as there is a very narrow window during which the keys will be recognized.

Pointing Device Interface

The Touchpad pointing device is a PS/2 compatible internal pointing device. If an external PS/2 pointing device is connected, the internal pointing device will work in parallel.[1]

Data and clock outputs from the pointing device controller(s) are routed to the keyboard controller data port and onto the controller internal data bus for processing. The external keyboard and pointing devices from the expansion/convenience base are connected through separate keyboard and mouse PS/2 connectors. The computer has a single PS/2 connector that will accept an external mouse and/or keyboard through a Y-connector. As many as three PS/2 devices are able to communicate with the system at the same time as shown in Figure 9-4.

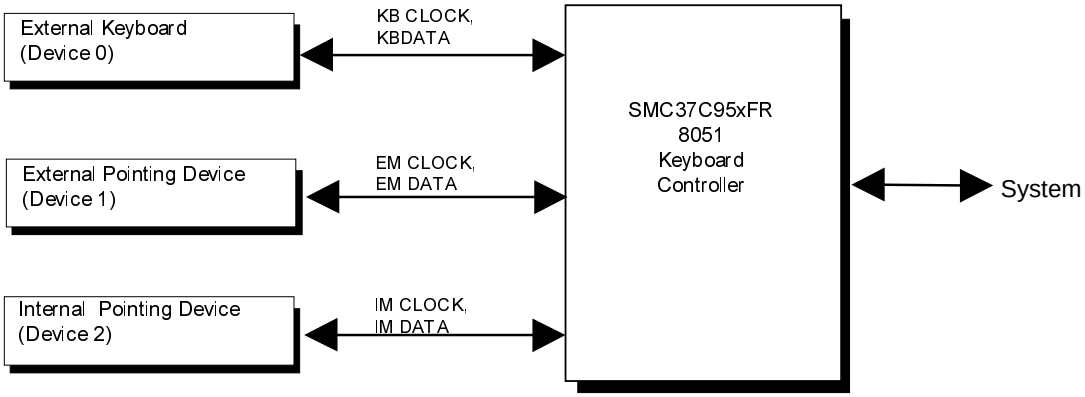


Figure 9-4. Pointing Device Interface, Block Diagram

[1] An external USB keyboard and mouse are also supported in BIOS firmware. Refer to chapter 6 for details.

Pointing Device Initialization

When the PS/2 mouse is powered on, it sends 0xAAh, then 0x00h.

Data Format

The data transmitted by the pointing device to the system consists of the X/Y coordinates of the pointer and status of the buttons. This data is transmitted in a three-byte serial PS/2 data packet that is compatible with the Microsoft PS/2 mouse.

Serial PS2 data, illustrated in Figure 9-5, is transmitted to the system using the following parameters:

- Data Bits 8 bits
- Start Bits 1 bit
- Stop Bits 1 bit
- Parity 1 bit, odd

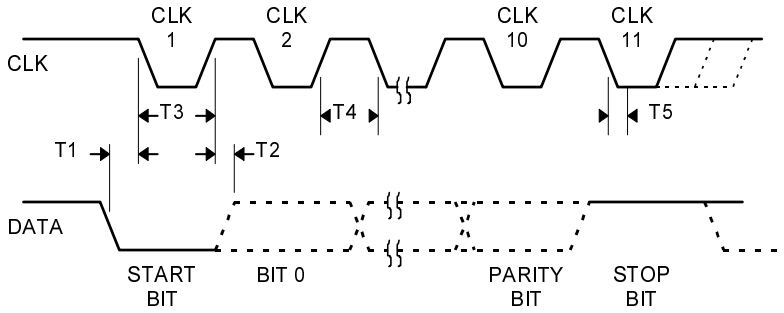


Figure 9-5. PS/2 Data Transmission Sequence

External Keyboard/Mouse Communications

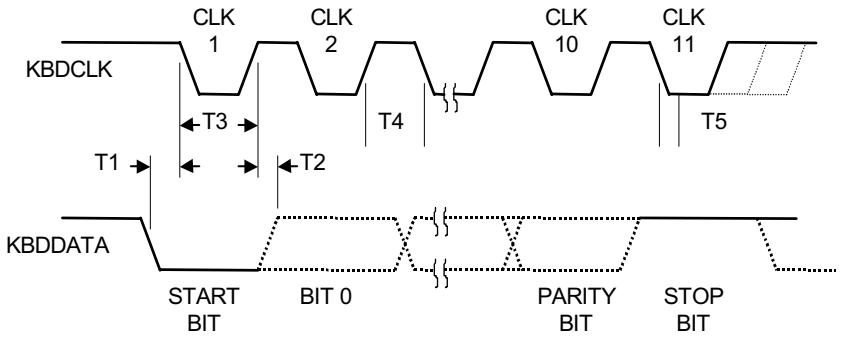
Communication between the computer system and the external keyboard or mouse is bidirectional. The keyboard controller of the computer system controls both KBDDATA and KBDCLK for status signaling. When the keyboard is idle or between scan code transmissions, both KBDCLK and KBDDATA are set high.

Keyboard/Mouse-to-System Transmissions

PS/2 keyboards and PS/2 mice use the same data protocol. The following discussion applies to both devices. Prior to the beginning of a transmission, the keyboard must check the status of KBDDATA and KBDCLK. A low KBDCLK indicates keyboard inhibition and all keystrokes are loaded into the keyboard buffer. A low KBDDATA indicates the computer system is issuing a request-to-send (RTS) command. When the computer system issues an RTS, the keyboard will load all keystrokes into the buffer and prepare to receive data.

The keyboard will begin transmission when both KBDDATA and KBDCLK are high. Data transmissions consist of a start bit, eight data bits, an odd parity bit, and a stop bit. The keyboard will first set the correct level on KBDDATA, and then pulse KBDCLK low. After the transmission, the system will make KBDCLK low until the transmitted data is processed.

During a keyboard transmission, the computer system can request a transmission interrupt by lowering KBDCLK. The keyboard will check the state of KBDCLK every 100 microseconds during a transmission. If the line is detected low and the parity bit has been clocked out, the keyboard will finish the transmission. If KBDCLK is detected low before the rising edge of the parity bit is clocked out, the keyboard will abort the transmission. All data aborted during a transmission will be sent later.



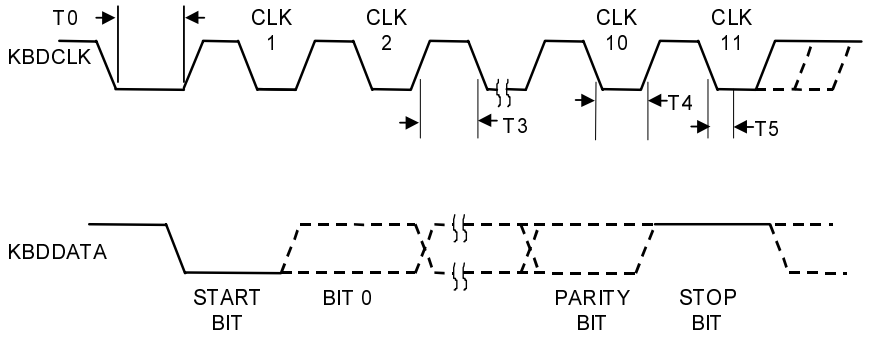
	Timing Parameter	Min	Max
T1	KBDDATA transition to falling edge of KBDCLK	5 μsec	25 μsec
T2	KBDCLK rising edge to DATA transition	5 μsec	T4 - 5 μsec
T3	KBDCLK inactive time	30 μsec	50 μsec
T4	KBDCLK active time	30 μsec	50 μsec
T5	Auxiliary device inhibit after CLK 11	>0 μsec	50 μsec

Figure 9-6. Timing Diagram for Keyboard-to-System Transmissions

*System-to-**K**eyboard/Mouse Transmissions*

The computer system has several commands that it may issue to the keyboard or mouse at any time. When the keyboard or mouse is transmitting to the computer system, the system first clamps the KBDCLK signal line to request a keyboard or mouse transmission halt. To ensure that the keyboard or mouse recognizes the interface request, the KBDCLK line must remain low (0) for at least 100 μs. If the keyboard or mouse transmission is past the rising edge of the parity bit clock pulse, the keyboard or mouse completes its transmission; if not, the keyboard or mouse will load the data into the character buffer and receive the data from the computer system.

Figure 9-7 shows the timing diagram for system-to-keyboard or mouse transmissions.



	Timing Parameter	Min	Max
T0	KBDCLK low device inhibit	100 μsec	
T3	KBDCLK inactive time	30 μsec	50 μsec
T4	KBDCLK active time	30 μsec	50 μsec
T5	Auxiliary device inhibit after CLK 11	>0 μsec	50 μsec

Figure 9-7. Timing Diagram for System-to-Keyboard or Mouse Transmissions

When the system is ready to transmit a command to the keyboard or mouse, it sets the DATA line low (0). This action serves as both a request-to-send and a start bit. Upon detecting the KBDDATA line low, the keyboard or mouse sets the KBDCLK line low, causing the start bit to be clocked out of the system. The interface then places the least-significant bit (LSB, data bit <0>) on the KBDDATA line, and the keyboard or mouse clocks out the LSB on the next negative going clock pulse. This process continues until all eight data bits are clocked out of the interface.

After all data bits are clocked out of the interface, the system places an odd parity bit on the KBDDATA line. The keyboard or mouse repeats its clocking of the parity bit as before. The keyboard or mouse then sets the KBDDATA line low and clocks this line to the system for a stop bit. When the keyboard or mouse receives the stop bit, the interface sets the KBDCLK line low, to inhibit the keyboard or mouse, while it is processing the received data.

After the external device receives a controller command, the external device returns an ACK code (0xFAh) to the controller. If a parity error or timeout occurs, a resend command (0xFEh) is sent to the keyboard controller.

Power Supply

The power supply is designed to operate from multiple power sources and has advanced power management features. This power subsystem consists of an internal 44 peak watt AC adapter, DC/DC converter, and a rechargeable lithium-ion battery pack.

Functional Description

The internal AC adapter assembly converts 110/220 volts AC into low voltage DC to drive the DC-DC converter and to recharge the battery pack. The output of this auto-configuring AC/DC supply is the battery voltage, approximately 10V - 19V.

The internal DC/DC power supply accepts this voltage and generates the required system voltages. A firmware controlled fan is used in the system for cooling the supply and the rest of the system components.

The internal DC-DC converter also takes the input DC voltage from the battery pack and converts it to the voltages required by the computer and display circuitry. The power supply provides +3.3 VDC, +5 VDC, +12 VDC.

The computer is powered from 14.4-volt (nominal) rechargeable lithium-ion (Li-Ion) battery pack. The Li-Ion battery pack is composed of battery cells and control circuitry that reports battery fuel gauge information and protects the battery from overheating or overcharging. A coin cell is provided to maintain power to the real-time clock (RTC) when all other power is removed from the system.

Figure 10-1 shows a block diagram of the power supply subsystem.

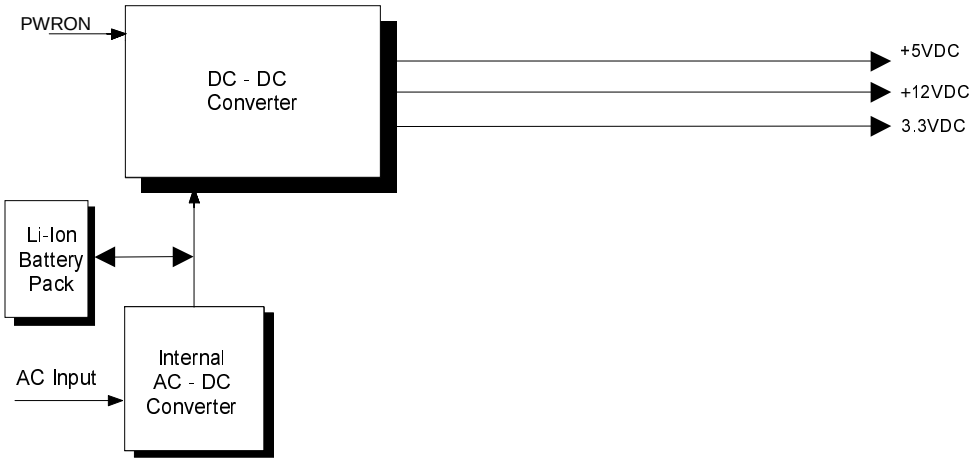


Figure 10-1. *Power Supply, Block Diagram*

AC/DC Converter

The AC input to the power supply is through a three-wire (hot, neutral, ground) power cord that uses small gauge, high flexibility wire. This power cord connects to the internal AC/DC converter through an IEC 320 type C6 three-pin power connector on the rear panel of the computer.

The internal AC adapter converts high voltage AC into low voltage DC that is used to drive the DC/DC converter and to recharge the battery pack. The AC adapter provides two output signals, VBATT+ and AC DETECT.

When charging a battery, the DC output voltage is limited to the same voltage as the battery pack, but never below 10 VDC. In the absence of a battery pack, or if the battery is not charging, the adapter output can rise to a maximum of 18.5 VDC +/- 5%.

Table 10-1 shows operating specifications for the AC/DC converter.

Table 1*0*-1
AC/DC Converter Specifications

AC Input:	
Voltage	90 - 240 Volts AC
Frequency	47 - 63 Hz
Current	1.10 amps
DC Output:	
Voltage	18.5 VDC maximum
Current	4.5 amps maximum
Power	43 watts typical

The AC/DC power supply returns an AC DETECT signal to indicate to the system that AC is present and can run the system. This line is used to drive an input to the 8051 and is connected to the MASTERBAT line as part of the power arbitration scheme. When converted AC voltage is applied, the AC DETECT signal will be low.

DC-DC Converter

The internal DC-DC converter is built on the system board. Total output power is rated at 38W continuous and 48W peak. Power supply input current is limited by a fuse. DC input from the AC adapter or battery is converted to three DC outputs:

- +3.3 V @4.0A
- +5 V @ 5.0A
- +12 V @0.075A

Specifications for the DC-DC converter are shown in Table 10-2.

Table 10-2
DC-DC Converter Specifications

Parameter	Value
Input DC Voltage Range	9.0 to 20.0 VDC
Input Current (max)	3.7 A , 4.65 A (peak), 500 mA (max. ripple)
Power Output:	
Steady State	38 W
Peak	40 W
Output Voltage/Wattage	
Voltage	Watts
3.3 VDC	13.2
5.0 VDC	25
12.0 VDC	0.9
Voltage Regulation:	
Output Voltage	Variance
3.3 VDC	±5%
5.0 VDC	±5%
12.0 VDC	±5%
1.3-2.0 VDC	±40 m V.

Fan Control

The fan control circuitry is located in the DC/DC power supply section of the system board. Fan speed is controlled by MSIO-driven I^2C interfaced potentiometers to control the two fans in the system. This allows the fan speed to be changed based on the CPU temperature, battery status, and other parameters.

Fault-Detection Circuits

The fault-detection circuits shut down the power supply until all faults are removed and the power switch is turned off, then on. Power supply faults[1] that trigger the protection circuitry include:

- Thermal overload: The protection circuit triggers if the power supply becomes too hot as a result of fan failure or a restriction of the air flow.
- Overvoltage: All supplies activate the overvoltage crowbar circuit that triggers the protection circuit when the output exceeds the maximum voltage level.
- Short circuit: The protection circuit triggers if any power supply output is shorted to ground or to another output. This function prevents any shock or fire hazard.

[1]Minimum load conditions must be met at all times to ensure normal operation and meet specifications.

Battery Pack

The lithium-ion (Li-Ion) battery pack provides for long battery run time in a light-weight package. The battery pack delivers a total capacity of 38.4 W-Hr each. The Li-Ion battery pack consists of eight 3.6-volt cells connected in such a way as to provide from 10 to 16 volts (14 volts nom.) output and the monitoring circuitry for the battery fuel gauge. In addition, a temperature sensor and other circuit protection devices are housed in the battery pack.

The specifications of the Li-Ion battery pack are shown in Table 10-3.

Table 10-3
Lithium-Ion (Li-Ion) Battery Pack Electrical Specifications

Parameter	Value	Notes
Open circuit voltage:	14.4 V	Nominal
Capacity:	38.4 W-hours	
Temperature:		
Charge	10°C to 40°C (50°F to 104°F)	
Storage	0°C to 50°C (32°F to 122°F)	

The battery pack has an onboard microcontroller that monitors the battery history and charge state of the battery cells. This microcontroller communicates with the 8051 in the system by I^2C internal bus. The 8051 is the master, and the battery pack is the slave on the bus. The battery can signal the system that attention is required through a Compaq implemented technique that does not violate the I^2C protocols. The Li-Ion battery pack has six contacts as described in Table 10-4.

Table 10-4
Lithium-ion (Li-Ion) Battery Pack Contacts

Contact	Function
BAT+	Battery (+) connection (high current)
LOCRES	Analog position indicator
SCL	Serial clock line referenced to BAT–
SDA	Serial data line referenced to BAT–
MASTERBAT	Master battery line, bidirectional
BAT–	Battery (–) connection

All Li-Ion battery packs used in the full system (computer battery bay and second battery in MultiBay) are connected in parallel (+ BAT connected to + BAT, – BAT connected to – BAT). Each battery has a location ID line (LOCRES) that has a resistor to ground on the system board (or on a logic board in the docking station) to provide geographic location information to each battery pack. By reading this resistance value, the battery pack decides what location information to use when communicating with the 8051 in the system.

The battery uses the location information to set its I^2C bus address. The battery only responds to the I^2C address for the location that it is presently occupying. This location information determines the batteries position in the charge and discharge hierarchy of the system. The charge and discharge hierarchy is described in a following section. The I^2C bus connections are implemented on the SCL and SDA lines from the battery pack.

The Li-Ion battery location resistor values are given in Table 10-5.

Table 1*0-5*
Lithium-Ion (Li-Ion) Battery Location Identification

LOCRES Resistor Value	Battery Location
0	RESERVED, indicates possible error condition
511 Ω	Main computer battery
2 K Ω	Computer MultiBay
3920 Ω	RESERVED (used in charger)
5110 Ω	RESERVED (used in charger)
6810 Ω	RESERVED
9090 Ω	RESERVED
∞	Battery pack not installed in system

Charge Status Monitoring

The battery pack has internal circuitry that monitors the charge state and charge history. This internal battery controller monitors the charge state and communicates battery status and charge level to the system for use by the system fuel gauge. This information is available to the user on request. This information also determines which battery should be charged when more than one battery is installed in the system.

The battery pack has intelligence that communicates with the system via the system I^2C bus. The battery pack behaves like a pseudo master on the I^2C bus. The battery pack microcontroller is not able to initiate a complete transaction on the I^2C bus. It is only able to generate a start condition followed by a stop condition on the bus. This short bus transaction generates an interrupt to the system 8051 in the MSIO ASIC. In response to this interrupt, the 8051 queries each of the possible pack locations to find out which pack is in need of service.

The battery pack contains two FETs—one to control charging of the pack and one to allow discharge of the pack. The microcontroller inside the pack controls each of these FETs according to commands from the 8051.

Master Battery Arbitration

The MASTERBAT line is pulled down when the battery is installed in the system to allow the battery to provide power to the system and cause an interrupt to the battery microcrontroller. The battery microcontroller then decides if the battery is powering the system and relays the information to the 8051 through the I^2C bus. The 8051 checks the MASTERBAT line for status changes and determines if the battery is to power the system. If the battery is determined to be the highest priority for discharge in the system, the MASTERBAT line is driven high by the battery supplying power to the system.

The MASTERBAT signal is also generated from the AC DETECT signal output by the AC adapter to indicate AC line power is available. If AC is present, the power supply drives the MASTERBAT line high. This keeps the Li-Ion battery pack turned off, letting the AC power supply provide all of the current to run the system. If AC power is removed while the system is running, the MASTERBAT line goes low, causing the battery pack in the computer battery bay to start supplying power to the system.

Li-Ion Battery Charging/Discharging Order

The Li-Ion battery packs can only be charged one at a time. The battery packs are charged in a predetermined order which allows the user to better determine which battery pack is being charged at any given time. The battery pack installed in the battery bay of the computer is the first to be charged and last to be discharged. The battery in the MultiBay charged next.

Fuel Gauges

System Fuel Gauges

Through a hotkey sequence(**Fn**+**F8**),the Li-Ion battery pack charge state can be displayed on a popup window on the screen. The popup is capable of displaying the fuel gauge information for each of the batteries installed in the system. A total system fuel gauge is also displayed when the system is running off of one of these batteries. If the system is powered by AC power, the battery that is currently being charged is indicated by highlighting.

RTC Power Supply

The real time clock in the 37C95xFR has its own power pins (VCC0). The 8051 and associated interface circuitry in the 37C951FR also has a separate power pin (VCC1). These two sources are provided power whenever any power source is available in the system. The available power sources include: the AC supply or the main Li-Ion battery. All of these sources drive the VBAT+ line in the system. A coin cell provides power to the RTC when all other power sources are removed.

Mass Storage

This chapter describes the mass storage devices. The computer is equipped with one easily removable 4.0-GB hard drive. The MultiBay supports an optional IDE hard drive, 3.5-inch high-density diskette drive, zipdrive or 120-MB LS-120 drive. Also available are either a CD-ROM or DVD-ROM module for the computer optical disc bay.

The preinstalled hard drive contains software that supports PC Cards, IrDA, multimedia, and other system features.

Hard Drive Subsystem

The computer supports one removable 2.5-inch IDE hard disk drive in a fixed disk module that consists of the drive, and a bracket assembly. The hard drive automatically retracts the heads and locks them in a non-data parking zone at power-down.

The internal hard drive connects directly to the system board for data buffering and I/O address decoding. All I/O operations are 16-bit. The PCI IDE interface can run extremely short ISA-type cycles, because it uses dedicated control signals rather than the ISA control signals.

All timing aspects of the cycle are directly programmable to meet the capabilities of the drive being used. There is support for two separate IDE drives on the same bus with independent timing requirements. This feature allows the hard drive and an optional CD-ROM drive to occupy the same bus, with optimal access to both devices.

Hard Drive Programming

The hard drive subsystem supports the ATA-3 specification for hard drive interfacing, programming and control. A working draft of this specification is available from the ATA Anonymous FTP Site, fission.dt.wdc.com. The ATA directory is: /pub/standards/ata/ata3. Additional information is available from the following WEB sites:

- www.computercraft.com/docs/evsterms.html
- www.lib.ox.ac.uk/internet/news/faq/archive/pc-hardware-faq (there are two parts to this collection of USENET FAQs.

Registers

Table 11-1 lists the standard and alternate I/O addresses for the hard drive controller. Addresses in the first (1) column are the computer addresses, and addresses in the second (2) column are for the expansion base. These settings can be changed by the user in the configuration mode or by OS drivers.

Table 11-1
Hard Drive Controller I/O Addresses

I/O Address 1	I/O Address 2	Read/Write	Register
1F0h	170h	R/W	Data
1F1h	171h	R	Error
1F1h	171h	W	Features
1F2h	172h	R/W	Sector Count
1F3h	173h	R/W	Sector Number
1F4h	174h	R/W	Cylinder Low
1F5h	175h	R/W	Cylinder High
1F6h	176h	R/W	Drive/Head
1F7h	177h	R	Status
1F7h	177h	W	Command
3F6h	376h	R	Alternate Status
3F6h	376h	W	Drive Control
3F7h	377h	R	Drive Address (see note)
3F7h	377h	W	Not used for hard drive

NOTE: Only bits <6..0> are resident on the hard drive controller. Bit <7> of this I/O address is resident on the system board.

Hard Drive Connector

Table 11-2 lists the hard drive connector signals.

Table 11-2
Hard Drive Connector Signals

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	26		
2	HDRST_	Reset signal	27	GND	Ground
3	DATA7	IDE Data bus Bit 7	28	DATA8	IDE Data bus Bit 8
4	DATA6	IDE Data bus Bit 6	29	DATA9	IDE Data bus Bit 9
5	DATA5	IDE Data bus Bit 5	30	DATA10	IDE Data bus Bit 10
6	DATA4	IDE Data bus Bit 4	31	DATA11	IDE Data bus Bit 11
7	GND	Ground	32	GND	Ground
8	DATA3	IDE Data bus Bit 3	33	DATA12	IDE Data bus Bit 12
9	DATA2	IDE Data bus Bit 2	34	DATA13	IDE Data bus Bit 13
10	DATA1	IDE Data bus Bit 1	35	DATA14	IDE Data bus Bit 14
11	DATA0	IDE Data bus Bit 0	36	DATA15	IDE Data bus Bit 15
12	GND	Ground	37		
13			38	GND	Ground
14	HDWR_	IDE Bus write signal	39	GND	Ground
15	HDRD_	IDE Bus read signal	40	GND	Ground
16	HDCHRDY	I/O channel ready	41	GND	Ground
17			42	GND	Ground
18	IRQ		43	IO16_	IDE bus I/OCS16_ signal
19	A1	IDE bus address bit 1	44	PDIAG_	Slave drive finished power-up
20	A0	IDE bus address bit 0	45	A2	IDE bus address bit 2
21	GND	Ground	46	GND	Ground
22	CS1_	Chip select for 1F0-1F7h (170-177)	47	CS3_	Chip select for 3F6h (176)
23	DASP_	Drive access/slave present	48	GND	Ground
24	+5V	+ 5V power	49	+5V	+ 5V power
25	GND	Ground	50		

Hard Drive Specifications

Table 11-3 describes the specifications for the hard drive.

Table 11-*3*
Hard Drive Specifications

Standard Model Configurations	***4.0*-GB**
Formatted Capacity per Drive (MB)	
Physical	
Logical	4,099,866,624
Drive Type	
Drive Height	
With drive frame (mm)	12.7
Drive Size	
Inches	2.5 x 0.5
Millimeters	102 x 75
Transfer Rate	
Media (Mb/s)	51.4-83.4 MB/sec
Interface (Mb/s)	16.6 MB/sec
Sector Interleave	1:1
Typical Seek Time (Including setting)	
Single Track (ms)	4 ms
Average (ms)	13 ms (read)
Full Stroke (ms)	32 ms (read)
Disk Rotational Speed (RPM)	4009
Physical Configuration	
Cylinders	6975
Data Heads	6
Sectors/Track	144-240
Bytes/Sector	512
Logical Configuration	
Cylinders	7944
Heads	16
Sectors per Track	63
Bytes per Sector	512
Buffer Size	512-KB

Note: For hard drives, GB = billion bytes

Diskette Drive Subsystem

There are no permanently installed diskette drives in the computer MultiBay. One full-height diskette drive MultiBay module can be installed in the MultiBay of the computer.

Figure 11-1 is a functional block diagram of a diskette drive.

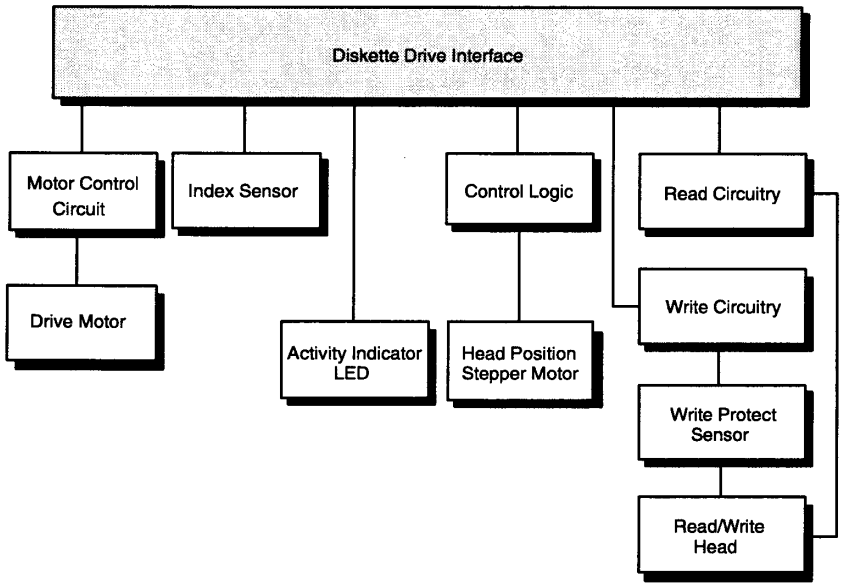


Figure 11-1. *Diskette Drive, Functional Block Diagram*

1.*44*-Megabyte Diskette Drive

The 1.44-megabyte diskette drive is a high-capacity diskette drive with the following features:

- 0.6-inch high, 3.5-inch diskette drive
- Two transfer rates: 250 Kb/s (low density) or 500 Kb/s (high density)
- Data storage on 80 tracks (135 tpi)
- Write- and read-compatible with low density (720-Kbyte) 3.5-inch media

Diskette Drive Controller

The diskette drive controller circuitry is contained in the SMC37C95xFR MSIO device. Through dedicated I/O port addresses, this circuitry transmits data to and from a diskette drive and controls drive functions and reads the current drive status. Table 11-4 lists the port addresses of the diskette drive controller.

Table 11-*4*
Port Addresses for the Diskette Drive Controller Circuits

Port 1	Port 2	Read/Write	Register Function
3F1h	371h	R	Media ID
3F2h	372h	R/W	Drive Control
3F4h	374h	R	Main Status
3F5h	375h	R/W	Data
3F7h	377h	R	Diskette Change Status/Fixed Disk Drive Status
3F7h	377h	W	Date Transfer Rate Control

Diskette Drive Controller Registers

The diskette drive controller registers are described in the following paragraphs.

Media ID (*3*F1h, Read Only)

The media ID register can be used to identify a 3.5-inch diskette drive and the media installed in the drive. The format for this register is:

BIT	FUNCTION
7	Media ID bit
6..0	Reserved

To identify media type:

1. Select drive, turn motor on using 3F2h.
2. Clear the DISKETTE CHANGE_ signal if it is active.
3. Read bit <7> at location 3F1. If the bit is low, 720-Kbyte media is installed. If the bit is high, then 1.44-megabyte media is installed.

Main Status (*3F4*h, Read Only)

The main status register of the diskette drive controller is used as the diskette drive status register. The format for this register is:

BIT	FUNCTION
7	Request for Master
6	Data I/O Direction
5	Non DMA Execution
4	Command in Process
3	Drive 3 busy
2	Drive 2 busy
1	Drive 1 busy
0	Drive 0 busy

Data (*3F5*h)

Commands and data are written to this port. Data and status bytes are read from this port.

Data Transfer Rate Control (*3F7*h, Write Only)

This register contains the current data transfer rate in kilobits per second (Kb/s). The format for this register is:

BIT	FUNCTION
7..2	Reserved
1,0	Data Transfer Rate (Kb/s) 00 = 500 01 = 300 10 = 250 11 = 1000

Diskette Drive and Hard Drive Status (*3F7*h, Read Only)

This register provides both diskette drive status information (bit <7>) and hard drive status information (bits <6..0>). The format for this register is as follows:

BIT	FUNCTION
7	Diskette change
6..0	Reserved for Hard Drive

Drive Controller

The drive controller accepts commands from the computer that control most drive functions and transfers of data to the drives.

The drive controller operates in the ISA-compatible DMA mode for data transfers to and from the system. It issues a DMA request (DRQ2) signal and receives a DMA acknowledge (DACK2_) signal for each byte transferred.

All drive controller commands have three operating phases:

- The command phase, in which the drive controller receives the command from the system
- The execution phase, in which the drive controller carries out the command
- The results phase, in which the status and results are read back from the drive controller to the system

Diskette Data Transfer Rate

The system can transfer data at various rates depending on the drive and the type of media being used. The data transfer rate control register (3F7h) contains the bits that specify the transfer rate.

Table 11-5 lists the media dependent transfer rates of the diskette drive subsystem.

Table 11-*5*
Programmable Data Transfer Rate

Data Transfer Rate (in KB/s)	When Using:
500	1.44-MB diskette drive with 1.44-MB media
250	1.44-MB diskette drive with 720-KB media

Write Precompensation

Write precompensation is a process of time shifting write data bits to help cancel out an opposite shift induced during magnetic recording. This process increases data integrity at high data densities. The data density increases as the diskette drive head approaches the center tracks. Write precompensation is always on and is always 125 ns for all data-transfer rates (500, 300, and 250 Kb/s).

LS-12*0* Drive Subsystem

The LS-120 drive is supported through the MultiBay module. This drive is supported as a bootable device.

If the drive is present during POST, BIOS attempts to read the boot record from the drive. If a bootable diskette is inserted in the drive, BIOS will use the drive when INT 19h is called.

The drive utilizes an imbedded ATAPI (IDE) controller for the host interface. The drive is capable of reading and writing to standard SuperDisk LS-120 diskettes, industry standard 1.44-MB and 720-KB 3.5-inch diskettes, 1.7-MB Distribution Media Formatted diskettes (read only), and 1.2-MB diskettes.

Table 11-*6*
LS-12*0* Drive Specifications

	12*0* MB	**1.*7* MB DMF**	**1.*44* MB**	**1.2 MB**	**1.2 MB**	***720* KB**	***640* KB**
Formatted Capacity (Bytes)	125,958,144	1,720,320	1,474,560	1,261,568	1,228,800	737,280	655,360
Sector Size (bytes)	512	512	512	1024	512	512	512
Sectors	246,527	3360	2880	1,232	2400	1,440	1,280
Magnetic Tracks/ Surface	1736	80	80	77	80	80	80
Optical Servo Tracks/Surface	900	N/A	N/A	N/A	N/A	N/A	N/A
Sectors/track	51-92	21	18	8	15	9	8
Sector Interleave	1:1	2:1	1:1	1:1	1:1	1:1	1:1
Spare sectors	170	0	0	0	0	0	0
Zones (each side)	55	1	1	1	1	1	1
Average random seek	70 ms	70 ms	70 ms	70 ms	70 ms	70 ms	70 ms
Track-to-Track seek	20 ms	25 ms	25 ms	25 ms	25 ms	25 ms	25 ms
Max single seek	120 ms	170 ms	170 ms	170 ms	170 ms	170 ms	170 ms
Average Latency	41.67 ms	41.67 ms	41.67 ms	41.67 ms	41.67 ms	41.67 ms	41.67 ms
Motor rpm	720 ±0.5%	720 ±0.5%	720 ±0.5%	720 ±0.5%	720 ±0.5%	720 ±0.5%	720 ±0.5%
Motor Start Time,	800 ms	800 ms	800 ms	800 ms	800 ms	800 ms	800 ms
Track Density	2,490 TPI	135 TPI	135 TPI	135 TPI	135 TPI	135 TPI	135 TPI
Track Width	8 μm	125 μm	125 μm	125 μm	125 μm	125 μm	125 μm
Encoding Method	(1,7)RLL	MFM	MFM	MFM	MFM	MFM	MFM

Continued

Table 11-*6*, LS-12*0* Drive Specifications *Continued*

	12*0* MB	**1.*7* MB DMF**	**1.*44* MB**	**1.2 MB**	**1.2 MB**	***720* KB**	***640* KB**
Max Flux Density	33,660 FCI	17,334 FCI	17,334 FCI	17,334 FCI	17,334 FCI	8,717 FCI	8,717 FCI
Recording Density	44,880 BPI	17,334 BPI	17,334 BPI	17,334 BPI	17,334 BPI	8,717 BPI	8,717 BPI
Nominal Transfer Rate	375-680 KB/sec	150 KB/sec	150 KB/sec	125 KB/sec	125 KB/sec	75 KB/sec	75 KB/sec
Nominal Sustained Transfer Rate across interface	313-565 KB/sec	65 KB/sec Read, 32 KB/sec Write	55 KB/sec Read, 28 KB/sec Write	49 KB/sec Read, 25 KB/sec Write	46 KB/sec Read, 23 KB/sec Write	28 KB/sec Read, 14 KB/sec Write	28 KB/sec Read, 14 KB/sec Write
Buffer Transfer rate	4.0 MB/sec	4.0 MB/sec	4.0 MB/sec	4.0 MB/sec	4.0 MB/sec	4.0 MB/sec	4.0 MB/sec

CD-ROM Drive

The computer supports a modular 24X max CD-ROM drive in the optical disc bay. These CD-ROM drives support the following modes:

- CD-ROM Mode 1
- CD-ROM Mode 2
- CD-Digital Audio
- CD-XA (Form 1, Form 2)
- CD-I Mode 2 (Form 1, Form 2)
- CD-I Ready
- CD Bridge
- CD-WO (fixed/variable packets)
- Photo CD (Multisession)
- CD-R
- Video CD
- CD-Extra (CD+)
- CD-G
- CD-RW

Table 11-7 describes the specifications for the CD-ROM drive.

Table 11-7
CD-ROM Specifications

Applicable Disc	CD-ROM mode 1, mode 2 CD-Digital Audio CD-XA mode 2 (Form 1, Form 2) CD-I mode 2 (Form1, Form 2) CD-I Ready CD-Bridge CD-WO (fixed/variable packets) Photo CD (singlemultisession)
Center Hole Diameter	15 mm
Disc Diameter	12 cm, 8 cm
Disc Thickness	1.2 mm
Track Pitch	1.6 μm
Laser	
Beam Divergence	53.5 ± 1.5 degrees
Output Power	0.24 ± 0.1 mw
Type	Semiconductor Laser GaA1As
Wave Length	780 nm ± 25 nm
Access time	
Random	<350 ms
Full Stroke	<750 ms
Audio output level	
Line Out	0.7 Vrms
Headphone	None
Cache buffer	128 KB
Data transfer rate	
Sustained, 10x	1500 KB/sec
Sustained, single	150 KB/sec
Burst	8.3 MB/sec
Startup Time	<8 seconds typical
Capacity	
Mode 1, 12 cm	550 MB
Mode 2, 12 cm	640 MB
8 cm	180 MB

DVD-ROM Drive

Table 11-8 lists the DVD-ROM specifications.

Table 11-*8*
DVD-ROM Specifications

Disc Formats Supported	DVD-5, DVD-9, DVD-10, DVD-18 CD-ROM mode 1, mode 2 CD-Digital Audio CD-XA mode 2 (Form 1, Form 2) CD-I mode 2 (Form1, Form 2) CD-I Ready CD-Bridge CD-R Photo CD (singlemultisession)
Center Hole Diameter	15 mm
Disc Diameter	12 cm, 8 cm
Disc Thickness	1.2 mm
Track Pitch	1.6 μm
Capacity	4.7-GB - DVD-5 8.5-GB - DVD-9 9.4-GB - DVD-10 550-Mbytes (Mode 1, 12) 640 Mbytes (Mode 2, 12 cm) 180 Mbytes (8 cm) 17.1 - DVD -18
Laser	
Output Power	5mw
Type	Semiconductor Laser GaA1As
Wave Length	650 nm ± 25 nm (DVD Mode) 795 nm ± 25 nm (CD-ROM mode)
Access time	
Random	<200 ms
Full Stroke	<250 ms
Audio output level	
Line Out	0.7 Vrms
Headphone	None
Cache buffer	128 KB
Data transfer rate	
Sustained, 1x (CD-ROM mode)	150 KB/sec
Sustained, 20x CD-ROM CAV mode	1200-3000 KB/sec
Sustained, DVD mode	2760 Kbytes/s sustained, DVD mode
Burst	16.6 MB/sec
Startup Time	<15 seconds typical

MultiBay *60*-Pin Connector

Table 11-9 presents the MultiBay connector signals.

Table 11-*9*
MultiBay Connector Signals

Pin	Signal	Description	Pin	Signal	Description
1	Vcc	+5v	31	SD12	Data bit 12 of the IDE data
2	Vcc	+5v	32	SD3	Data bit 3 of the IDE data
3	Ground		33	SD11	Data bit 11 of the IDE data
4	DASP_	Drive Access/Slave Present	34	SD4	Data bit 4 of the IDE data
5	3FXCS_	Chip select 3F6 (176) drive register	35	SD10	Data bit 10 of the IDE data
6	1FXCS_	Chip select 1F0-1F7 (170-177) regs.	36	SD7	Data bit 7 of the IDE data
7	SA2	IDE address bit <2>	37	SD9	Data bit 9 of the IDE data
8	SA0	IDE address bit <0>	38	SD6	Data bit 6 of the IDE data
9	MBID1	Multibay device ID	39	SD8	Data bit 8 of the IDE data
10	SA1	IDE address bit <1>	40	SD7	Data bit 7 of the IDE data
11	Pdiag*		41	Ground	
12	IRQ*	IDE Irq active	42	HDRST*	IDE Reset*
13	MBID0	Multibay device ID	43	Ground	
14	DMACK*	DMA active*	44	Nc	
15	Nc		45	Nc	
16	IORDY*	IDE Ready signal	46	Nc	
17	Ground		47	Nc	
18	IOR*	Read from IDE active	48	HDSEL	Floppy head select
19	Ground		49	RDATA	Floppy Read data
20	IOW*	Write active to IDE device	50	WRTPRT*	Floppy is Write protected
21	DRQ	IDE DMA request line (IDE interface)	51	TRK0*	Track Zero Indicator*
22	SDDAQ*	IDE DMA request active	52	WGATE_	Floppy Write Gate*
23	MPBDET*	Multibay device is present	53	WDATA_	Floppy Write Data*
24	Ground		54	STEP*	Causes floppy heads to step*
25	SD15	Data bit 15 of the IDE data	55	1.6MODE	Determines floppy density*
26	SD0	Data bit 0 of the IDE data	56	DIR_	Direction of Head Movement*
27	SD14	Data bit 14 of the IDE data	57	MTR0_	Motor On*
28	SD1	Data bit 1 of the IDE data	58	DSKCHG_	Diskette Change*
29	SD13	Data bit 13 of the IDE data	59	DSO*	Drive select
30	SD2	Data bit 2 of the IDE data	60	INDEX_	Index Detection*

*****Diskette drive controller interface signal

Zip Drive

Table 11-10 lists the specifications of the Zip Drive.

Table 11-1*0*
ZIP Drive Specifications

Total Formatted Capacity (bytes)	100,663,296
Sector Size (bytes)	512
Total Number of Sectors	196,608
Number of Reassignable Spare Sectors	252
Sector Interleave	1:1
Number of Zones (each side)	4
Sectors per Track, Zone 0	72
Sectors per Track, Zone 1	60
Sectors per Track, Zone 2	48
Sectors per Track, Zone 3	40
Magnetic Track/Surface	908
Compaq Part Number for Diskette	270928-001
Seek Times (including settling)	
Average Seek	29 ms
Track-to-Track	5 ms
Maximum	55 ms
Average Latency	10 ms
Motor Speed (rpm)	2941 ±5%
Motor Start Time (ms)	3000
Track Density (TPI)	2118
Track Width (μm)	12
Encoding Method	(1,8) RLL
Max Flux Density (FCI)	34,560
Max Recording Density (BPI)	46,000
Transfer Rate From Diskette (kb/sec.)	790-1400
Buffer Transfer Rate (maximum, MB/sec)	3.3

Boot Order

The following describes the boot order used by the mass storage devices of the computer.

The LS-120 is bootable. It will become the "A:" floppy device. ZIP drives are NOT bootable at this time. The CD-ROM is bootable, per the El-Torito specification, an industry standard. If Multiboot is NOT enabled (leaving the machine in its default boot mode), the machine will attempt to boot in the following order:

1. CD-ROM
2. 1.44 Floppy
3. LS-120 in the MultiBay (treated as a floppy)
4. Internal HDD

If Multiboot is enabled, then the boot order will depend on the way Multiboot has been defined.

If an internal hard disk is present, then the user can not boot from a second hard disk in the MultiBay. This is an operating system limitation. Specifically, DOS (and all DOS-based derivatives such as Win31, Win9x, etc), DEMAND that they be booted from "the first primary partition on the first HDD". For all practical purposes, this means the internal hard disk.

The internal hard disk used in the computer is always the IDE Master device on the first IDE channel. While the BIOS could attempt to bootstrap from the second hard disk, as soon as the operating system figures out where it was, it would stop booting due to an internal failure. The operating system assumes that it is on the first hard disk, and thus won’t be able to continue finding/loading its own files.

Chapter 12

Internal Modem

This chapter describes the K56flex modem. Information contained in this chapter may be used as a programming reference in developing software and in determining correct configurations and settings.

Modem Description

The internal modem supports data rates up to 56 kbps and fax at up to 14.4 kbps. The features and functions of the modem are described in the following lists.

Features

The features provided by the internal Compaq high-speed fax/communications modem are as follows:

- Data Mode: TIA/EIA 602 standard AT command set modulation protocols:
  - ITU-T V.90 (56 Kbps)
  - ITU-T V.34 Annex 12 (33.6 Kbps)
  - ITU-T V.34 (28.8 Kbps)
  - ITU-T V.32 terbo (19.2 Kbps)
  - ITU-T V.32bis (14.4 Kbps)
  - ITU-T V.22bis (2400 bps)
  - TU-T V.22 (1200 bps)
  - ITU-T V.23 (1200/75 bps)
  - Bell 212a (1200 bps)
  - Bell 103 (300 bps)
- Data error correction protocols:
  - MNP2-4, ITU-T V.42,
- Data compression protocols:
  - ITU-T V.42bis and MNP5
- Fax Mode:
  - ITU-T V.17 (14.4 Kbps)
  - ITU-T V.27ter (4.8/2.4 Kbps)
  - ITU-T V.29 (9.6/7.2 Kbps)
  - ITU-T V21 Channel 2 (300 bps)
  - EIA 578
- Digital Line Guard
- Global modem with universal DAA

Functional Overview

The internal modem is controlled by several software application layers that are accessed by the user through a Windows application. This application acts as a remote control for the data and fax software applications. The application alerts the user to incoming calls, identifies the caller, and provides options that allow the user to choose the desired action regarding the call. The application also launches the fax and data software when the user is initiating a call. The modem only operates using one of the following operating systems: Windows 95, Windows 98 or Windows NT 4.0.

The modem operates in either the "command mode" or "online mode" and can be controlled by the preinstalled communication software or by use of the Attention (AT) command set. The modem enters the command mode upon power-up and is configured by the default conditions that have been set in modem memory by the factory for normal operation. If necessary, these settings may be altered by changing the AT command settings, dial modifiers, and S register settings while in the command mode. After a command has been executed and a connection is established with another modem or fax machine, the modem enters the online mode (unless otherwise specified by changes in the AT dial modifiers).

The modem has two basic modes of operation while in the online state: data and fax. The settings established by the user or the software will determine the operation mode of the modem. If data mode is selected, the modem will modulate and demodulate the signals from another computer using a protocol established by setup or negotiation. When facsimile is selected, the modem provides a Class 1 interface that will transmit and receive faxed information at the established rate.

Hardware Functional Description

The modem hardware is a hybrid configuration consisting of a standard modem. The modem provides a software UART interface for normal data and fax operations.

The modem interfaces the telephone analog information with the system board ISA bus. The data access arrangement (DAA) circuitry and speaker/microphone I/O devices transfer the analog information into and out of the modem. The information is translated by the line codec during the data and fax modes. The codec uses a sigma-delta technique to provide 15-bit resolution with 12-bit linearity and sends and receives in 16-bit, two's complement, binary format.

Line and acoustic information are processed by the digital signal processor (DSP) and interfaced to the modem's internal DA bus by the data interface. The Lucent Technologies DSP16415 controller is a 16-bit, fixed-point DSP with 24-K words of program ROM and contains the data/fax algorithms.

The modem operation is separated into the following six areas:

- ISA interface
- 16550 Software UART emulation
- 256 × 8-bit SRAM module
- Configuration and control registers
- General purpose input/output ports

AT Commands

The TIA/EIA-602 standard for AT commands and TIA/EIA-578 FAX specification are fully supported by the Compaq High-Speed Fax/Voice Modem. These commands and settings are available on the Compaq support Web site. The URL for the modem commands is www.compaq.com/support/techpubs/.

Supported Countries

The following lists the countries the modem supports

- USA
- Canada
- Mexico
- Brazil
- United Kingdom
- France
- Germany
- Netherlands
- UAE
- Czechoslovakia
- Belgium
- Switzerland
- Sweden
- Norway
- Denmark
- Finland
- Portugal
- Italy
- Spain
- Austria
- Australia
- New Zealand
- Singpore
- Malaysia
- Taiwan
- China
- Japan

Error Messages and Codes

Error Messages

The following pages list warning messages, error codes and system error beep codes not documented elsewhere, with a brief description of the probable cause. The computer will generate only those codes applicable to the actual system configuration and installed options.

Common Power-On Messages

Table A-1 lists the error messages that may occur when the system is powered-on or reset.

Table A-1
Power-On Messages

Message	Beeps	Probable Cause
163 - Time and date not set	*2S*	*Invalid time or date*
(Two very short beeps)	*2VS*	*Power-on successful*
RESUME = "F1" key	*None*	*Any failure*

Initialization Diagnostic Messages

Table A-2 lists error messages that may occur as part of the Power-On Self-Test (POST).

Table A-2
Power-On Self-Test (POST) Messages

Message	Beeps	Probable Cause
No visible message	*3L*	*Processor Self-test*
No visible message	*2L*	*Memory map failure*
101 - I/O ROM error	*1L, 1S*	*Option ROM checksum*
101 - ROM error	*1L, 1S*	*System ROM checksum*
102 - System Board Failure	*None*	*DMA or timers*
102 - System or Memory Board Failure	*None*	*High-order addresses*
162 - System Options Error	*2S*	*No diskette drives or mismatch in drive types*
162 - System Options Not Set (Run SETUP)	*2S*	*System SETUP*

NOTES: *1.* L = *long beep, S = short beep*

2. XX000Y ZZ = *Address* (XX), *byte* (Y), *data bit* (ZZ) *of failed memory test*

Continued

Table A-2-Power-On Self-Test (POST) Messages *Continued*

Message	Beeps	Probable Cause
163 *- Time and Date Not Set*	***2S***	*Invalid time or date in configuration memory*
164 *- Memory Size Error*	***2S***	*Memory size discrepancy*
170 *- Expansion Device not Responding* (Run *SETUP*)	None	*Expansion device not responding*
176 *- Slot with No Readable ID* (Run *SETUP*)	None	*Slot with no readable ID*
177 *- SETUP Not Complete* (Run *SETUP*)	None	*SETUP not complete*
178 *- Processor SETUP Invalid* (Run *SETUP*)	None	*Processor SETUP invalid*
XX000Y ZZ ***201*** *- Memory Error*	None	*RAM failure*
XX000Y ZZ ***203*** *- Memory Error*	None	*RAM failure*
205 *- Cache Memory Failure*	None	*System board*
Z ***2***05 *- Memory Failure*	None	*Memory board failure*
206 *- Secondary Cache Controller Failure*	None	*Cache Memory Controller Failure*
207 *- Invalid Memory Configuration*	None	*System memory board*
Z ***2***09 *- NCA RAM Error*	None	*NCA Failure*
211 *- Memory Failure*	None	*RAM Failure*
301 *- Keyboard Error*	None	*Keyboard failure*
301 *- Keyboard Error or Test Fixture Installed*	None	*Keyboard test fixture*
302 *- System Unit Security Lock is Locked - Unlock System Unit Security Lock*	***2S***	*System locked*
303 *- Keyboard Controller Error*	None	*Keyboard controller*
304 *- Keyboard or System Unit Error*	None	*Keyboard interface*
401 *- Printer Error*	None	*Printer controller*
401 *- Port **1** Address Assignment Conflict*	***2S***	*External and Internal Port assignments to Port **1***
402 *- Monochrome Adapter Failure*	***1***L, ***2S***	*Monochrome display controller*
403 *- Port **3** Address Assignment Conflict*	***2S***	*External and Internal Port Assignments to Port **1***
50***1*** *- Display Adapter Failure*	***1***L, ***2S***	*Graphics display controller*
60***1*** *- Diskette Drive Controller Error*	None	*Diskette drive controller*
60***2*** *- Diskette Drive Boot Record Error*	None	*Diskette drive does not have a valid boot record*
605 *- Diskette Drive Type Error*	***2S***	*Wrong drive type used in the computer setup utility*

NOTES: ***1***. L = *long beep, S = short beep*

2. XX000Y ZZ = *Address* (XX), *byte* (Y), *data bit* (ZZ) of *failed memory test*

Continued

Table A-2-Power-On Self-Test (POST) Messages *Continued*

Message	Beeps	Probable Cause
607 - *Diskette Drive Controller Error*	*2S*	*Configuration error*
6*11* - *Primary Diskette Drive Assignment Conflict*	*2S*	*Configuration error*
6*12* - *Secondary Diskette Drive Assignment Conflict*	*2S*	*Configuration error*
70*2* - *A-Coprocessor Detection Error*	*2S*	*Add coprocessor or configuration error*
70*3* - *Coprocessor Detection Error*	*2S*	*Add coprocessor or configuration error*
*112*5 - *Internal Serial Port Failure*	*2S*	*Defective internal serial port*
*11*50 - xx *Comm Port Setup Error*	*2S*	*Setup not correct (run SETUP)*
*11*5*1* - *COM1 Address Assignment Conflict*	*2S*	*External and internal port assignments to COM1*
*11*5*2* - *COM2 Address Assignment Conflict*	*2S*	*External and internal port assignments to COM2*
*11*5*3* - *COM3 Address Assignment Conflict*	*2S*	*External and internal port assignments to COM3*
*11*5*3* - *COM4 Address Assignment Conflict*	*2S*	*External and internal port assignments to COM4*
*1*600 - *32-Bit System Manager Board Failure*	*2S*	*Configuration mismatch*
*173*0 - *Hard Drive 0 Does Not Support DMA Mode*	*2S*	*Configuration mismatch*
1731 - *Hard Drive 1 Does Not Support DMA Mode*	*2S*	*Configuration mismatch*
*174*0 - *Hard Drive 0 Failed Set Block Mode Command*	*2S*	*Configuration mismatch*
1741 - *Hard Drive 1 Failed Set Block Mode Command*	None	*Wrong drive type*
*1*750 - *Hard Drive 0 Failed Identify Command*	None	*Wrong drive type*
*1*751 - *Hard Drive 0 Failed Identify Command*	None	*Wrong drive type*
*1*760 - *Hard Drive 0 Does Not Support Block Mode*	*2S*	*Configuration mismatch*
*1*761 - *Hard Drive 1 Does Not Support Block Mode*	*2S*	*Configuration mismatch*
*1*771 - *Primary Drive Port Address Assignment Conflict*	*2S*	*Internal and external hard drive controllers assigned to primary address*
*1*772 - *Secondary Disk Port Address Assignment Conflict*		*Internal and external hard drive controllers assigned to secondary address*

NOTES: *1*. L = *long beep, S = short beep*

2. XX000Y ZZ = *Address* (XX), *byte* (Y), *data bit* (ZZ) of *failed memory test*

Continued

Table A-2-Power-On Self-Test (POST) Messages *Continued*

Message	Beeps	Probable Cause
1780 - Hard Drive 0 Failure	None	*Hard drive 0 not ready*
1781 - Hard Drive 1 Failure	*2S*	*Hard drive 1 not ready*
1782 - Hard Drive Controller Failure	None	*Hard drive controller*
1790 - Hard Drive 0 Error	None	*Wrong drive type used in SETUP*
1791 - Hard Drive 1 Error	None	*Wrong drive type used in SETUP*
1792 - Secondary Drive Controller Error	None	*hard drive error or wrong drive type*
1793 - Secondary Controller or Drive Failure	None	*hard drive error or wrong drive type*
XX000Y ZZ *Parity Check 2*	None	*RAM parity failure*
Hard Drive Parameter Table or BIOS Error	*3L*	*Configuration or hardware failure*
IO*CHECK Active, Slot* X	None	*Defective board in slot* x
Bus Master Time-Out Slot X	None	*Defective board in slot* x
Audible	*1S*	*Power-On successful*
Audible	*2S*	*Power-On successful*
(R*ESUME* = "*F1*" KEY)	None	*As indicated to continue*

NOTES: *1*. L = *long beep, S = short beep*

2. XX000Y ZZ = *Address* (XX), *byte* (Y), *data bit* (ZZ) of *failed memory test*

Advanced Diagnostics Error Messages

The following tables list error messages that may occur during Advanced Diagnostics testing. Depending on installed options, all messages may not apply to all systems.

Processor

Table A-3 lists error messages that relate to the system processor or to other system board devices.

Table A-3
Processor Error Messages

Message	Probable Cause
101 - 01	CPU test failed
101 - 02	32-Bit CPU test failed
101 - 91	Multiplication test failed
101 - 92	Multiplication test failed
101 - 93	Multiplication test failed
101 - 94	Multiplication test failed
102 - 01	Numeric coprocessor initial status word incorrect
102 - 02	Numeric coprocessor initial control word incorrect
102 - 03	Numeric coprocessor tag word not all ones
102 - 04	Numeric coprocessor tag word not all zeros
102 - 05	Numeric coprocessor exchange command failed
102 - 06	Numeric coprocessor masked exception incorrectly handled
102 - 07	Numeric coprocessor unmasked exception incorrectly handled
102 - 08	Numeric coprocessor wrong mask bit set in Status register
102 - 09	Numeric coprocessor unable to store real number
102 - 10	Numeric coprocessor real number calculation test failed
102 - 11	Numeric coprocessor speed test failed
102 - 12	Numeric coprocessor pattern test failed
102 - 15	Numeric coprocessor is inoperative or socket is unoccupied
102 - 16	Weitek coprocessor not responding
102 - 17	Weitek coprocessor failed register transfer test
102 - 18	Weitek coprocessor failed arithmetic operations test
102 - 19	Weitek coprocessor failed data conversion test
102 - 20	Weitek coprocessor failed interrupt test
102 - 21	Weitek coprocessor failed speed test
103 - 01	DMA page registers test failed
103 - 02	DMA byte controller test failed
103 - 03	DMA word controller test failed

Continued

Table A-3-Processor Error Messages *Continued*

Message	Probable Cause
104 - 01	Interrupt controller master test failed
104 - 02	Interrupt controller slave test failed
104 - 03	Interrupt controller software RTC is inoperative
105 - 01	Port 61 bit <6> not at zero
105 - 02	Port 61 bit <5> not at zero
105 - 03	Port 61 bit <**3**> not at zero
105 - 04	Port 61 bit <**1**> not at zero
105 - 05	Port 61 bit <0> not at zero
105 - 06	Port 61 bit <5> not at one
105 - 07	Port 61 bit <**3**> not at one
105 - 08	Port 61 bit <**1**> not at one
105 - 09	Port 61 bit <0> not at one
105 - 10	Port 61 I/O test failed
105 - 11	Port 61 bit <7> not at zero
105 - 12	Port 61 bit <**2**> not at zero
105 - 13	No interrupt generated by failsafe timer
105 - 14	NMI not triggered by failsafe timer
106 - 01	Keyboard controller self-test failed
107 - 01	CMOS RAM test failed
108 - 02	CMOS interrupt test failed
108 - 03	CMOS interrupt test, CMOS not properly initialized
109 - 01	CMOS clock load data test failed
109 - 02	CMOS clock rollover test failed
109 - 03	CMOS clock test, CMOS not properly initialized
110 - 01	Programmable timer load data test failed
110 - 02	Programmable timer dynamic test failed
110 - 03	Program timer **2** load data test failed
111 - 01	Refresh detect test failed
112 - 01	Speed test Slow mode out of range
112 - 02	Speed test Mixed mode out of range
112 - 03	Speed test Fast mode out of range
112 - 04	Speed test unable to enter Slow mode
112 - 05	Speed test unable to enter Mixed mode
112 - 06	Speed test unable to enter Fast mode
112 - 07	Speed test system error
112 - 08	Unable to enter Auto mode in speed test
112 - 09	Unable to enter High mode in speed test

Continued

Table A-3-Processor Error Messages *Continued*

Message	Probable Cause
112 - 10	*Speed test* High *mode out of range*
112 - 11	*Speed test Auto mode out of range*
112 - 12	*Speed test Variable Speed mode inoperative*
113 - 01	*Protected mode test failed*
114 - 01	*Speaker test failed*
116 - xx	Way 0 *read/write test failed*
199 - 00	In*stalled devices test failed*

Memory

Table A-4 lists error messages for memory-related errors.

Table A-*4*
Memory Error Messages

Message	Probable Cause
200 - 04	Real memory size changed
200 - 05	Extended memory size changed
200 - 06	Invalid memory configuration
200 - 07	Extended memory size changed
200 - 08	CLIM memory size changed
201 - 01	Memory machine ID test failed
202 - 01	Memory system ROM checksum failed
202 - 02	Failed RAM/ROM map test
202 - 03	Failed RAM/ROM protect test
203 - 01	Memory read/write test failed
203 - 02	Error while saving block under test in read/write test
203 - 03	Error while restoring block under test in read/write test
204 - 01	Memory address test failed
204 - 02	Error while saving block under test in address test
204 - 03	Error while restoring block under test in address test
204 - 04	A20 address test failed
204 - 05	Page hit address test failed
205 - 01	Walking I/O test failed
205 - 02	Error while saving block under test in walking I/O test
205 - 03	Error while restoring block under test in walking I/O test
206 - xx	Increment pattern test failed
210 - 01	Memory increment pattern test
210 - 02	Error while saving memory in increment pattern test
210 - 03	Error while restoring memory in increment pattern test
211 - 01	Memory random pattern test
211 - 02	Error while saving memory in random memory pattern test
211 - 03	Error while restoring memory in random memory pattern test

Keyboard

Table A-5 lists error messages for keyboard-related errors.

Table A-5
Keyboard Error Messages

Message	Probable Cause
301 - 01	Keyboard short test, 8042 self-test failed
301 - 02	Keyboard short test, interface test failed
301 - 03	Keyboard short test, echo test failed
301 - 04	Keyboard short test, keyboard reset failed
301 - 05	Keyboard short test, keyboard reset failed
302 - 01	Keyboard long test, failed
303 - 01	Keyboard LED test, 8042 self-test failed
303 - 02	Keyboard LED test, reset test failed
303 - 03	Keyboard LED test, reset failed
303 - 04	Keyboard LED test, LED command test failed
303 - 05	Keyboard LED test, LED command test failed
303 - 06	Keyboard LED test, LED command test failed
303 - 07	Keyboard LED test, LED command test failed
303 - 08	Keyboard LED test, command byte restore test failed
303 - 09	Keyboard LED test, LEDs failed to light
304 - 01	Keyboard repeat key test failed
304 - 02	Unable to enter mode 3
304 - 03	Incorrect scan code from keyboard
304 - 04	No Make code observed
304 - 05	Cannot disable repeat key feature
304 - 06	Unable to return to Normal mode

Printer

Table A-6 lists error messages for printer-related errors.

Table A-*6*
Printer Error Messages

Message	Probable Cause
401 - 01	*Printer failed or not connected*
402 - 01	*Printer Data register failed*
402 - 02	*Printer Control register failed*
402 - 03	*Printer Data register and Control register failed*
402 - 04	*Printer loopback test failed*
402 - 05	*Printer loopback test and Data register failed*
402 - 06	*Printer loopback test and Control register failed*
402 - 07	*Loopback test, Data register, and Control register failed*
402 - 08	*Printer interrupt test failed*
402 - 09	*Printer interrupt test and Data register failed*
402 - 10	*Printer interrupt test and Control register failed*
402 - 11	*Printer interrupt, Data register, and Control register failed*
402 - 12	*Printer interrupt test and loopback test failed*
402 - 13	*Interrupt test, loopback test, and Data register failed*
402 - 14	*Interrupt test, loopback test, and Control register failed*
402 - 15	*Interrupt test, loopback test, Data/Control registers failed*
402 - 16	*Unexpected interrupt received*
403 - 01	*Printer pattern test failed*
498 - 00	*Printer failed or not connected*

Video

Table A-7 lists video error messages.

Table A-7
Video Error Messages

Message	Probable Cause
501 - 01	Video controller test failed
502 - 01	Video memory test failed
503 - 01	Video attribute test failed
504 - 01	Video character set test failed
505 - 01	Video 80 x 25 mode 9 x 14 character cell test failed
506 - 01	Video 80 x 25 mode 8 x 8 character cell test failed
507 - 01	Video 40 x 25 mode test failed
508 - 01	Video 320 x 200 mode color set 0 test failed
509 - 01	Video 320 x 200 mode color set 1 test failed
510 - 01	Video 640 x 200 mode test failed
511 - 01	Video screen memory page test failed
512 - 01	Video gray scale test failed
514 - 01	Video white screen test failed
516 - 01	Video noise pattern test failed

Diskette Drive

Table A-8 lists error messages for diskette drive-related errors.

Table A-*8*
Diskette Drive Error Messages

Message	Probable Cause
600 - xx	*Diskette drive ID test*
600 - 05	*Failed to reset controller*
600 - 20	*Failed to get drive type*
601 - xx	*Diskette drive format*
601 - 05	*Failed to reset controller*
601 - 09	*Failed to format a track*
601 - 23	*Failed to set drive type in ID media*
602 - xx	*Diskette read test*
602 - 01	*Exceeded maximum soft error limit*
602 - 02	*Exceeded maximum hard error limit*
602 - 03	*Previously exceeded maximum soft error limit*
602 - 04	*Previously exceeded maximum hard error limit*
602 - 05	*Failed to reset controller*
602 - 06	*Fatal error while reading*
603 - xx	*Diskette drive read/write compare test*
603 - 01	*Exceeded maximum soft error limit*
603 - 02	*Exceeded maximum hard error limit*
603 - 03	*Previously exceeded maximum soft error limit*
603 - 04	*Previously exceeded maximum hard error limit*
603 - 05	*Failed to reset controller*
603 - 06	*Fatal error while reading*
603 - 07	*Fatal error while writing*
603 - 08	*Failed compare of read/write buffers*
604 - xx	*Diskette drive random seek test*
604 - 01	*Exceeded maximum soft error limit*
604 - 02	*Exceeded maximum hard error limit*
604 - 03	*Previously exceeded maximum soft error limit*
604 - 04	*Previously exceeded maximum hard error limit*
604 - 05	*Failed to reset controller*
604 - 06	*Fatal error while reading*
605 - xx	*Diskette drive ID media test*
605 - 20	*Failed to get drive type*

Continued

Table A-8-Power-On Messages *Continued*

Message	Probable Cause
605 - 24	Failed to read diskette media
605 - 25	Failed to verify diskette media
606 - xx	Diskette drive speed test
606 - 26	Failed to read media in speed test
606 - 27	Failed speed limits
607 - xx	Diskette wrap test
607 - 10	Failed sector wrap test
608 - xx	Diskette drive write-protect test
608 - 28	Failed write-protect test
609 - xx	Diskette drive reset controller test
609 - 05	Failed to reset controller
610 - xx	Diskette drive change line test
610 - 21	Failed to get change line status
610 - 22	Failed to clear change line status
694 - 00	Pin 34 not cut on 360 KB Diskette drive
697 - 00	Diskette type error
6xx - 01	Exceeded maximum soft error limit
6xx - 02	Exceeded maximum hard error limit
6xx - 03	Previously exceeded maximum soft error limit
6xx - 04	Previously exceeded maximum hard error limit
6xx - 05	Failed to reset controller
6xx - 06	Fatal error while reading
6xx - 07	Fatal error while writing
6xx - 08	Failed compare of read/write buffers
6xx - 09	Failed to format a track
6xx - 10	Failed sector wrap test
6xx - 20	Failed to get drive type
6xx - 22	Failed to clear change line status
6xx - 23	Failed to set drive type in ID media
6xx - 24	Failed to read diskette media
6xx - 25	Failed to verify diskette media
6xx - 26	Failed to read media in speed test
6xx - 27	Failed speed limits
6xx - 28	Failed write-protect test
698 - 00	Diskette drive speed not within limits
699 - 00	Drive/media ID error – rerun SETUP

Serial Communications

Table A-9 lists error messages for serial communications-related errors.

Table A-*9*
Serial Communications Error Messages

Message	Probable Cause
11*01 - 0*1	*Serial port test,* UART *DLAB bit failure*
11*01 - 0*2	*Serial port test, line input or* UART *fault*
11*01 - 0*3	*Serial port test, address line fault*
11*01 - 0*4	*Serial port test, data line fault*
***11*01 -** 05	*Serial port test,* UART *control signal failure*
***11*01 -** 06	*Serial port test,* UART THR*E bit failure*
***11*01 -** 07	*Serial port test,* UART *DATA READY bit failure*
11*01 - 0*8	*Serial port test,* UART TX/RX *buffer failure*
***11*01 -** 09	*Serial port test,* INTERRU*PT circuit failure*
***11*01 - *1*0**	*Serial port test, COM**1** set to invalid interrupt*
11*01 - *11	*Serial port test, COM**2** set to invalid interrupt*
11*01 - *12	*Serial port test, DRIVER/RECEIVER control signal failure*
11*01 - *13	*Serial port test,* UART *control signal interrupt failure*
11*01 - *14	*Serial port test, DRIVER/RECEIVER data failure*
11*09 - 0*1	*Clock register initialization failure*
11*09 - 0*2	*Clock register rollover failure*
11*09 - 0*3	*Clock reset failure*
11*09 - 0*4	I*nput line or clock failure*
***11*09 -** 05	*Address line fault*
***11*09 -** 06	*Data line fault*
***11*50 -** xx	*Comm port setup error (run SETUP)*

Modem Communications

Table A-10 lists error messages for modem communications.

Table A-10
Modem Communications Error Messages

Message	Probable Cause
1201 - xx	Modem internal loopback test
1201 - 01	UART DLAB bit failure
1201 - 02	Line input or UART failure
1201 - 03	Address line fault
1201 - 04	Data line fault
1201 - 05	UART control signal failure
1201 - 06	UART THRE bit failure
1201 - 07	UART DATA READY bit failure
1201 - 08	UART TX/RX buffer failure
1201 - 09	Interrupt circuit failure
1201 - 10	COM1 set to invalid interrupt
1201 - 11	COM2 set to invalid interrupt
1201 - 12	DRIVER/RECEIVER control signal failure
1201 - 13	UART control signal interrupt failure
1201 - 14	DRIVER/RECEIVER data failure
1201 - 15	Modem detection failure
1201 - 16	Modem ROM, checksum failure
1201 - 17	Tone detection failure
1202 - xx	Modem internal test
1202 - 01	Modem time-out waiting for SYNC (local loopback mode)
1202 - 02	Modem time-out waiting for response (local loopback mode)
1202 - 03	Modem exceeded data block retry limit (local loopback mode)
1202 - 11	Time-out waiting for SYNC (analog loopback originate mode)
1202 - 12	Time-out waiting for modem response (analog loopback originate mode)
1202 - 13	Exceeded data block retry limit (analog loopback originate mode)
1202 - 21	Time-out waiting for SYNC (analog loopback answer mode)
1202 - 22	Time-out waiting for modem response (analog loopback answer mode)
1202 - 23	Exceeded data block retry limit (analog loopback answer mode)
1203 - xx	Modem external termination test
1203 - 01	Modem external TIP/RING failure
1203 - 02	Modem external DATA TIP/RING failure
1203 - 03	Modem line termination failure
1204 - xx	Modem auto originate test

Continued

Table A-10-Modem Communications Error Messages *Continued*

Message	Probable Cause
1204 - 01	Modem time-out waiting for SYNC
1204 - 02	Modem time-out waiting for response
1204 - 03	Modem exceeded data block retry limit
1204 - 04	RCV exceeded carrier lost limit
1204 - 05	XMIT exceeded carrier lost limit
1204 - 06	Time-out waiting for dial tone
1204 - 07	Dial number string too long
1204 - 08	Modem time-out waiting for remote response
1204 - 09	Modem exceeded maximum redial limit
1204 - 10	Line quality prevented remote connection
1204 - 11	Modem time-out waiting for remote connection
1205 - xx	Modem auto answer test
1205 - 01	Modem time-out waiting for SYNC
1205 - 02	Modem time-out waiting for response
1205 - 03	Modem exceeded data block retry limit
1205 - 04	RCV exceeded carrier lost limit
1205 - 05	XMIT exceeded carrier lost limit
1205 - 06	Time-out waiting for dial tone
1205 - 07	Dial number string too long
1205 - 08	Modem time-out waiting for remote response
1205 - 09	Modem exceeded maximum redial limit
1205 - 10	Line quality prevented remote connection
1205 - 11	Modem time-out waiting for remote connection
1206 - xx	Dial multi-frequency tone test
1206 - 17	Tone detection failure
1210 - xx	Modem direct connect test
1210 - 01	Modem time-out waiting for SYNC
1210 - 02	Modem time-out waiting for response
1210 - 03	Modem exceeded data block retry limit
1210 - 04	RCV exceeded carrier lost limit
1210 - 05	XMIT exceeded carrier lost limit
1210 - 06	Time-out waiting for dial tone
1210 - 07	Dial number string too long
1210 - 08	Modem time-out waiting for remote response
1210 - 09	Modem exceeded maximum redial limit
1210 - 10	Line quality prevented remote connection
1210 - 11	Modem time-out waiting for remote connection

Hard Drive

Table A-11 lists error messages for hard drive-related errors.

Table A-11
Hard Drive Error Messages

Message	Probable Cause
1700 - xx	Hard Drive drive ID test
1700 - 05	Failed to reset controller
1700 - 09	Failed to format a track
1700 - 41	Failed to ID hard (drive not ready)
1700 - 42	Failed to recalibrate drive
1700 - 45	Failed to get drive parameters from ROM
1700 - 46	Invalid drive parameters found in ROM
1700 - 66	Failed to initialize drive parameter
1700 - 69	Failed to read drive size from controller
1700 - 70	Failed translate mode
1700 - 71	Failed non-translate mode
1701 - xx	Hard drive format
1701 - 05	Failed to reset controller
1701 - 09	Failed to format a cylinder
1701 - 42	Failed to recalibrate drive
1701 - 58	Failed to write sector buffer
1701 - 59	Failed to read sector buffer
1701 - 66	Failed to initialize drive parameter
1702 - xx	Hard drive read test
1702 - 01	Exceeded maximum soft error limit
1702 - 02	Exceeded maximum hard error limit
1702 - 03	Previously exceeded maximum soft error limit
1702 - 04	Previously exceeded maximum hard error limit
1702 - 05	Failed to reset controller
1702 - 06	Fatal error while reading
1702 - 40	Failed cylinder 0
1702 - 65	Exceeded maximum bad sectors per track
1702 - 68	Failed to read long
1702 - 70	Failed translate mode
1702 - 71	Failed non-translate mode
1702 - 72	Bad track limit exceeded
1702 - 73	Previously exceeded bad track limit
1703 - xx	Hard drive read/write compare test

Continued

Table A-11-Hard Drive Error Messages *Continued*

Message	Probable Cause
1703 - 01	Exceeded maximum soft error limit
1703 - 02	Exceeded maximum hard error limit
1703 - 03	Previously exceeded maximum soft error limit
1703 - 04	Previously exceeded maximum hard error limit
1703 - 05	Failed to reset controller
1703 - 06	Fatal error while reading
1703 - 07	Fatal error while writing
1703 - 08	Failed compare of read/write buffers
1703 - 40	Cylinder 0 error
1703 - 55	Cylinder 1 error
1703 - 63	Failed soft error rate
1703 - 65	Exceeded maximum bad sectors per track
1703 - 67	Failed to write long
1703 - 68	Failed to read long
1703 - 70	Failed translate mode
1703 - 71	Failed non-translate mode
1703 - 72	Bad track limit exceeded
1703 - 73	Previously exceeded bad track limit
1704 - xx	Hard drive random seek test
1704 - 01	Exceeded maximum soft error limit
1704 - 02	Exceeded maximum hard error limit
1704 - 03	Previously exceeded maximum soft error limit
1704 - 04	Previously exceeded maximum hard error limit
1704 - 05	Failed to reset controller
1704 - 06	Fatal error while reading
1704 - 40	Cylinder 0 error
1704 - 55	Cylinder 1 error
1704 - 65	Exceeded maximum bad sectors per track
1704 - 70	Failed translate mode
1704 - 71	Failed non-translate mode
1704 - 72	Bad track limit exceeded
1704 - 73	Previously exceeded bad track limit
1705 - xx	Hard drive controller test
1705 - 05	Failed to reset controller
1705 - 44	Failed controller diagnostics
1705 - 56	Failed controller RAM diagnostics
1705 - 57	Failed controller to drive diagnostics

Continued

Table A-11-Hard Drive Error Messages *Continued*

Message	Probable Cause
1706 - xx	Hard drive ready test
1706 - 41	Drive not ready
1707 - xx	Hard drive recalibrate test
1707 - 42	Failed to recalibrate drive
1708 - xx	Hard drive format bad track test
1708 - 02	Exceeded maximum hard error limit
1708 - 05	Failed to reset controller
1708 - 09	Format bad track failed
1708 - 42	Recalibrate drive failed
1708 - 58	Failed to write sector buffer
1708 - 59	Failed to read sector buffer
1709 - xx	Hard drive reset controller test
1709 - 05	Failed to reset controller
1710 - xx	Hard drive park head test
1710 - 45	Failed to get drive parameters from ROM
1710 - 47	Failed to park heads
1714 - xx	Hard drive file write test
1714 - 01	Exceeded maximum soft error limit
1714 - 02	Exceeded maximum hard error limit
1714 - 03	Previously exceeded maximum soft error limit
1714 - 04	Previously exceeded maximum hard error limit
1714 - 05	Failed to reset controller
1714 - 06	Fatal error while reading
1714 - 07	Fatal error while writing
1714 - 08	Failed compare of read/write buffers
1714 - 10	Failed diskette sector wrap during read
1714 - 48	Failed to move disk table to RAM
1714 - 49	Failed to read diskette media in file write test
1714 - 50	Failed file I/O write test
1714 - 51	Failed file I/O read test
1714 - 52	Failed file I/O compare test
1714 - 55	Failed cylinder 1
1714 - 65	Exceeded maximum bad sectors per track
1714 - 70	Failed translate mode
1714 - 71	Failed non-translate mode
1714 - 72	Bad track limit exceeded
1714 - 73	Previously exceeded bad track limit

Continued

Table A-11-Hard Drive Error Messages *Continued*

Message	Probable Cause
1715 - xx	Hard drive head select test
1715 - 45	Failed to get drive parameters from ROM
1715 - 53	Failed drive head register test
1715 - 54	Failed digital input register test
1716 - xx	Hard drive conditional format test
1716 - 01	Exceeded maximum soft error limit
1716 - 02	Exceeded maximum hard error limit
1716 - 05	Failed to reset controller
1716 - 06	Fatal error while reading
1716 - 07	Fatal error while writing
1716 - 08	Failed compare of read/write buffers
1716 - 40	Cylinder 0 error
1716 - 42	Failed to recalibrate
1716 - 55	Cylinder 1 error
1716 - 58	Failed to write sector buffer
1716 - 59	Failed to read sector buffer
1716 - 60	Failed to compare sector buffer
1716 - 65	Exceeded maximum bad sectors per track
1716 - 66	Failed to initialize drive
1716 - 70	Failed translate mode
1716 - 71	Failed non-translate mode
1716 - 72	Bad track limit exceeded
1716 - 73	Previously exceeded bad track limit
1717 - xx	Hard drive ECC test
1717 - 01	Exceeded maximum soft error limit
1717 - 02	Exceeded maximum hard error limit
1717 - 03	Previously exceeded maximum soft error limit
1717 - 04	Previously exceeded maximum hard error limit
1717 - 05	Reset controller failed
1717 - 06	Fatal error while reading (BIOS status > or = 0 x 20)
1717 - 07	Fatal error while writing
1717 - 08	Compare data failed
1717 - 40	Cylinder 0 failed
1717 - 55	Cylinder 1 failed
1717 - 61	Failed uncorrectable error
1717 - 62	Failed correctable error
1717 - 65	Exceeded maximum bad sectors per track

Continued

Table A-11-Hard Drive Error Messages *Continued*

Message	Probable Cause
1717 - 67	Failed to write long
1717 - 68	Failed to read long
1717 - 70	Failed translate mode
1717 - 71	Failed non-translate mode
1717 - 73	Previously exceeded bad track limit
1719 - xx	Hard drive power mode test failed
1799 - 00	Invalid hard disk drive type
17xx - 01	Exceeded maximum soft error limit
17xx - 02	Exceeded maximum hard error limit
17xx - 03	Previously exceeded maximum soft error limit
17xx - 04	Previously exceeded maximum hard error limit
17xx - 05	Failed to reset controller
17xx - 06	Fatal error while reading
17xx - 07	Fatal error while writing
17xx - 08	Failed compare of read/write/compare
17xx - 09	Failed to format a track
17xx - 10	Failed sector wrap test
17xx - 19	Controller failed to deallocate bad sectors
17xx - 40	Failed cylinder 0
17xx - 41	Drive not ready
17xx - 42	Recalibrate failed
17xx - 43	Failed to format bad track
17xx - 44	Failed controller diagnostics
17xx - 45	Failed to get drive parameters from ROM
17xx - 46	Invalid drive parameters found in ROM
17xx - 47	Failed to park heads
17xx - 48	Failed to move hard drive table to RAM
17xx - 49	Failed to read media in file write test
17xx - 50	Failed file I/O write test
17xx - 51	Failed file I/O read test
17xx - 52	Failed file I/O compare test
17xx - 53	Failed drive/head register test
17xx - 54	Failed digital input register test
17xx - 55	Failed cylinder 1
17xx - 56	Hard drive controller RAM diagnostics failed
17xx - 57	Hard drive controller to drive test failed
17xx - 58	Failed to write sector buffer

Continued

Table A-11-Hard Drive Error Messages *Continued*

Message	Probable Cause
*1*7xx - 59	*Failed to read sector buffer*
*1*7xx - 60	*Failed uncorrectable ECC error*
*1*7xx - 6*2*	*Failed correctable ECC error*
*1*7xx - 6*3*	*Failed soft error rate*
*1*7xx - 65	*Exceeded maximum bad sectors per track*
*1*7xx - 66	*Failed initial drive parameter*
*1*7xx - 67	*Failed to write long*
*1*7xx - 6*8*	*Failed to read long*
*1*7xx - 69	*Failed to read drive size from controller*
*1*7xx - 70	*Failed translate mode*
*1*7xx - 7*1*	*Failed non-translate mode*
*1*7xx - 7*2*	*Bad track limit exceeded*
*1*7xx - 7*3*	*Previously exceeded bad track limit*

Pointing Device Interface

Table A-12 lists the error messages pointing devices interface-related errors.

Table A-12
Pointing Device Interface Error Messages

Message	Probable Cause
8601 - xx	*Pointing device interface*
8601 - 0*1*	*Mouse ID fails*
8601 - 0*2*	*Left button is inoperative*
8601 - 0*3*	*Left button is stuck closed*
8601 - 0*4*	*Right button is inoperative*
8601 - 05	*Right button is stuck closed*
8601 - 06	*Left block not selected*
8601 - 07	*Right block not selected*
8601 - 0*8*	*Time-out occurred*
8601 - 09	*Mouse loopback test failed*
8601 - *1*0	*Pointing device is inoperative*

Appendix B

Power Conservation

The power conservation features that are designed to extend operating time while running in either the normal operating “ON” mode or the reduced power “Suspend” (also referred to as “Global Standby” or “System Standby”) mode under either AC power or internal battery power. These features are all user-controllable through the SETUP utility during boot, by using the **F10** key or through the Windows/Windows NT power properties icon. Power conservation involves the control and interaction of three main elements: battery condition, power conservation level setting, and reduced power settings (Local standby, Suspend, or Hibernation modes). The hibernation feature provides data loss security, protection from battery rundown, and a "bookmark" function that returns the user to their original location prior to the interruption.

Battery Conditions

The CPU monitors the system battery conditions and reports the results to the user in the form of an icon in the popup status display window. Individual four-segment "fuel gauge" battery cell icons indicate the percent of charge remaining in the battery. The total system capacity fuel gauge is also displayed in the popup window. Only one battery is allowed to provide power at a time. The system power is switched to the next battery when the battery in use is depleted.

The battery condition is indicated by the battery charge LED. When on, this LED indicates the battery is being charged; when blinking, the battery is low; and when off, the battery is fully charged. A warning beep is also sounded when the battery is low or when being switched.

When connected to AC power the battery state icon is replaced with an AC plug icon to indicate that the unit is no longer powered by batteries. While in AC power mode, the fuel gauge continues to indicate the charge remaining in the battery. A water spigot icon is displayed, indicating the level of conservation selected.

Operating Mode

The computer recognizes two battery conditions while in either the operating or suspend mode: low battery 1 and low battery 2.

Low battery 1 - In this condition, the battery pack has approximately thirteen percent of its charge remaining. The computer indicates this condition by flashing the battery icon on the status panel and beeping the speaker once every 15 seconds.

Low battery 2 - When this condition is reached, the battery pack has only eight percent of its charge remaining. When this condition is reached, while in the suspend mode, the battery pack has less than ten percent of its charge remaining. This condition is indicated by the system entering into Hibernation (if enabled) or Suspend mode (if Hibernation is not enabled).

If the battery is allowed to completely discharge, (without enabling Hibernation) the state of the computer will be lost and the subsequent boot will load the system configuration from the non-volatile EEPROM. If the system is still in the Low Bat 2 state, it will remain in the low power state even when the Suspend switch is pushed. See Chapter 10 for more information on the battery and AC supplies.

Power Conservation Levels

The computer features user-selectable power conservation levels that are used in the Suspend mode. The power conservation level determines parameters such as subsystem timeouts and processor speed, both of which affect the amount of drain the system places on the battery pack. The power conservation levels are selected from the integrated keyboard only.

The user-selectable power conservation level settings that determine the conservation time-outs are shown in Table B-1.

Table B-1
Power Conservation Settings

Parameter	*Drain*	*High*	*Medium*	*Custom*
Suspend Timeout	Off	3 min	5 min	Off, 1, 2…17
Hard drive Timeout	Off	1 min	3 min	Off, 1..17 min
ScreenSave Timeout	Off	1 min	3 min	Off, 1..31 min
Processor Speed	100%	100%	100%	100%, 50%
Brightness	100%	50%	75%	Off, 1..100%

NOTES: Hibernation settings are set up (independent of the power conservation levels) as low battery or Suspend mode timeout settings from 0.5 to 15.0 minutes in 0.5 min increments.

All settings apply to both the computer and the expansion/convenience bases.

The computer also reduces power consumption when in Local Standby. The local standby mode is entered automatically after a user-selected value for hard drive Idle or Screen Save timeouts has elapsed and the screen and/or hard drive subsystems are powered down by the system. The Hibernation routine, as discussed later, may also be set to begin after the user-selected time out (0 to 15) hours has occurred.

The processor speed is automatically decreased through clock throttling during the local standby mode. If APM is enabled, APM idle calls put the CPU in the Stop Grant state to slow the CPU clock rate automatically which reduces processor speed according to usage.

Figure B-1 and Table B-2 show the transitions between the various reduced power stages along with the causes and results of each transition.

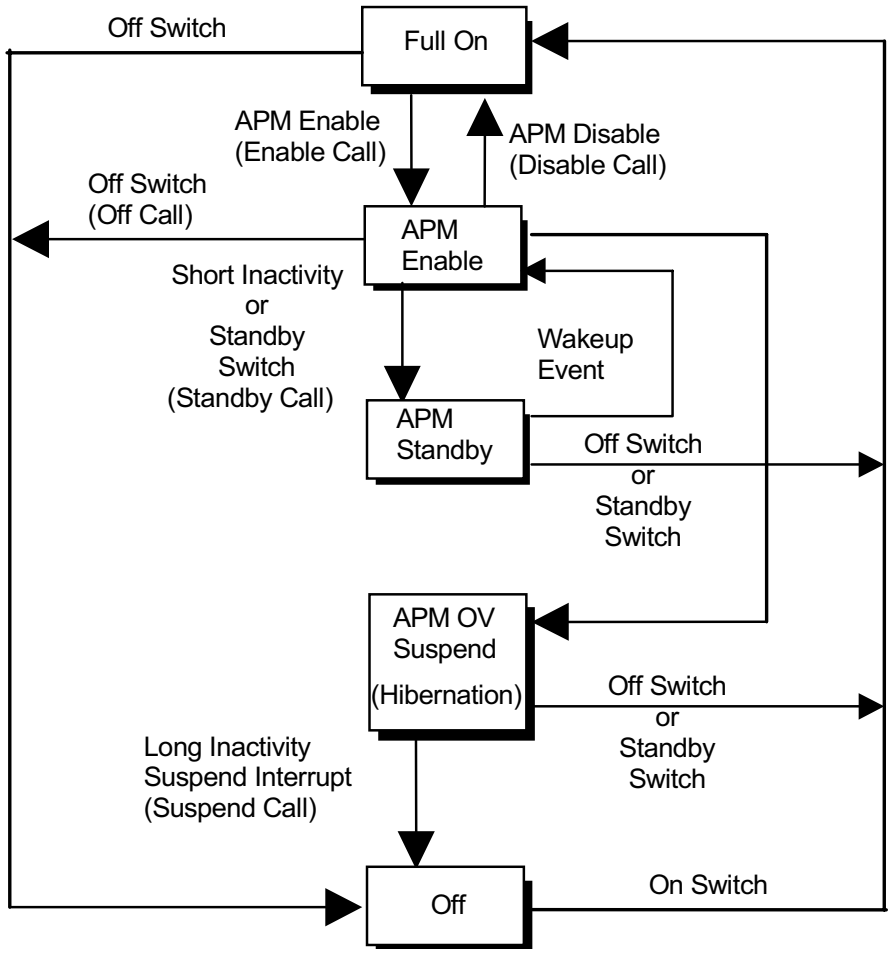


***Figure B-1*. APM Power Conservation State Diagram**

Table B-2
Management Mode Transitions

Current State	*Trigger Events*	***Hardware Actions***	***Firmware Actions***	***Next State***
OFF	Power Button	1. Turn on system power. 2. All devices at "best performance". 3. All chipsets at AT-Compatible.	1. Handle reset and POST functions. 2. Boot the Operating System.	ON
ON	Power Button	1. Generate firmware SMI. 2. Shut down system power (or On).	1. Confirms and ask hardware to shut down or system left On.	OFF
ON	Suspend	1.Generate firmware SMI. 2. Power down devices.	1. Save hardware states into DRAM. 2. Power down non-essential devices	Suspend
ON	Suspend Button	1. Generate an firmware SMI 2. Power down devices	1. Save hardware states into DRAM. 2. Power down non-essential devices	Suspend
ON	Hibernation Button	1. Generate firmware SMI 2. Turn off system after firmware has saved all hardware states.	1. Save hardware states to hard disk 2. Request system power shut down	Hibernation
ON	OS Idle	Stop CPU clock as requested by os.	Program hardware to stop CPU clock.	Syst. Idle
ON	Hibernation Timer	1. Generate firmware SMI. 2. Turn off system after firmware has saved all hardware states.	1. Save hardware states to hard disk. 2. Request system power shut down.	Hibernation
ON	Low Battery Critical	1. Generate firmware SMI. 2. Hibernate or Suspend as requested by firmware.	If Hibernation file exists, enter Hibernation state, or Suspend state.	Hibernation/ Suspend
System Idle	Interrupts or SMIs	Resume CPU clock and start executing sw/fw code.	No actions.	ON
Suspend	Suspend Button	1. Power up or resume CPU clock 2. Power up other devices	Ask hardware to power up devices and restore their states.	ON
Suspend	Hibernation Timer	1. Power up /resume CPU clock 2. Remain in Suspend mode or enter Hibernation.	If no Hibernation file, suspend, otherwise save hardware states to hard disk and enter Hibernation.	Suspend/ Hibernation
Suspend	RING or Alarm	1. Power up or resume CPU clock 2. Power up other devices	Ask hardware to power up devices and restore their states.	ON
Suspend	Low Battery Critical	1. Power up or resume CPU clock. 2. Remain in Suspend or enter Hibernation.	If no Hibernation file - suspend, otherwise save to hard disk enter Hibernation.	Hibernation/ Suspend
Suspend	Battery Exhausted	At 1% level the system is turned off to protect the battery.		OFF
Hiber-nation	Power Button	1. Turn on System power. 2. Power on all devices.	Check system configuration. If changed, resume aborted or reboot. Otherwise, restore hardware states from hard disk.	ON/ Hibernation

Reduced Power Conditions

The computer can be switched manually into one of two reduced battery power conditions: Suspend or Hibernation while being powered by converted AC or battery power. While in the battery powered mode, the unit can be placed into the suspend mode automatically by software from a Low battery 2 condition, by an inactivity timeout, or by pressing the Suspend button. Excessive CPU temperatures will also cause the system to enter the Suspend or Hibernation modes.

Local Standby

The computer enters the local standby condition automatically when various subsystems are placed in a reduced power mode after a period of inactivity. A power management firmware routine executes to clear timer registers and slow the CPU clock speed.

The subsystems that determine the status of suspend condition are monitored during local standby for I/O port or IRQ activity. If activity is detected, a System Management Interrupt (SMI) is generated which immediately brings that subsystem out of the suspend condition.

Table B-3 lists the ports and IRQs that are monitored for activity during Local Standby.

Table B-3
Subsystems Monitored for Activity During Local Standby

Subsystem	*Ports or IRQs*	*IRQ*
Keyboard	60h/64h (IRQ1)	1
Mouse	64h/64h (IRQ12)	12
Hard Drive (primary)	1F0h-1F7h	
Hard Drive (secondary)	170h-177h and 376h	
Serial Ports (Comm Port 1 & 2)	3F8h-3FFh 2F8-2FFh	
Parallel Port (LPT1 - LPT3)	378h-37Ah 278h-27Ah 3BCh-3BEh	

LCD Panel Blanking

The Screen Save timeout is used to place the graphics controller into Local Standby or Suspend mode, and then blank the LCD screen. If Enable Energy Savings Monitor is selected in setup, the VGA controller will be placed into Suspend mode. If this function is not enabled, the VGA controller will be placed into the local standby mode.

External Monitor Blanking

If an external "Energy Star" monitor is attached to the computer, it may be placed in a low power mode automatically after the "AC ENERGY SAVER" option is selected and the "ENERGY SAVE MONITOR" box is checked in the Windows setup utility. The monitor may be placed into either a "Quick Monitor Response" or "Maximum Energy Savings" (deep sleep) mode of power conservation (depending upon the mode selected during Setup) after a pre-set time of system inactivity has expired.

The Quick Energy Saver option allows the monitor to enter a "suspend" mode only, with power to the monitor reduced. When the Maximum Energy Savings mode is chosen, the monitor will first enter a suspend mode and then into a deep sleep mode after 40 minutes. The monitor will respond immediately when system activity is detected while in the Quick Energy Saver mode, but a 10 to 20 second warm-up time is required for the monitor when returning from the Maximum Savings mode.

Processor During Local Standby

During Local Standby, the CPU is idled during periods of inactivity by the stop clock signal. When activity occurs and interrupts are generated, the hardware clears this signal and the system returns to full speed operation.

Hard Drive During Local Standby

The operating mode of the hard drive is independent of the Local Standby condition of the computer except when a drive access occurs. A hard drive access by the computer will bring the computer out of the Local Standby condition. The time periods are programmed directly into the registers in the integrated drive electronics through IDE commands.

The hard drive has two Local Standby operating modes:

- Spin Down
- Sleep

Hard Drive Spin Down Mode

The hard drive Spin Down mode is determined by the hard drive timeout parameter set by the user. After a predefined period of drive inactivity, the drive motors and a large portion of the drive circuitry are turned off. A drive access request will bring the hard drive out of the Spin Down mode, but requires approximately 10 seconds for the drive platters to spin up to speed before the request is serviced. The hard drive can exit the Spin Down mode by entering the Sleep mode or being activated by a read/write request.

Hard Drive Sleep Mode

The hard drive enters the Sleep mode from the Spin Down mode. Additional drive circuitry is turned off for more power savings during Sleep Mode. The drive is powered up after any access from the host. The drive returns to normal operation after approximately 10 seconds.

Suspend (**G***lobal Standby*)

In Suspend, processing is stopped (suspended) and a large portion of the system is either powered off or placed in a low power mode. In this condition, the LCD is completely turned off and the system memory is held active so that data in memory is not lost. The suspend condition uses the least amount of battery power and is entered either from the Local Standby condition or by pressing the Suspend button. The computer may remain in the suspend condition for up to 100 hours depending on the condition of the battery at the time suspend is entered.

*Table B-**4***
Subsystem Status During Suspend

Subsystem	*Status*
Processor	Low Power (Halt)
Clock Generator	Low Power (outputs disabled)
Memory	Refresh Slowed to 32KHz
BIOS Flash ROM	Low Power
Ext. Keyboard/Pointing Device	Powered Off
Int. Pointing Device	Powered Off
Hard Drive	Powered Off
Diskette Drive	Powered Off
Diskette Drive Controller	Low Power
PCMCIA Controller	Powered Off (if selected)
Video Graphics Controller (RAM)	Low Power (32KHz Refresh)
LCD	Powered Off
Serial Port (IR)	Low Power
Serial Port (RS232)	Low Power
Parallel Port	Low Power
8051 Clock	8051 in deep sleep mode

Entering Suspend

The computer can be placed in the suspend condition by one of the following methods:

- By pressing the Suspend button
- Automatically due to peripheral inactivity or low battery condition
- Automatically due to over temperature conditions
- With special application software

Regardless of how the "entry into suspend" procedure is initiated, the system activity is the same.

The system monitors the same subsystems for Suspend as it does for Local Standby. If all peripheral timers expire (indicating no peripheral activity), then the system firmware initiates the suspend procedure. If the system detects activity in a monitored peripheral, an SMI for that activity will not be generated and the system will remain in the normal operating mode until that SMI is generated.

During the course of entering Suspend, the operating state of some subsystems must be saved prior to being powered down. The internal register data of the hard drive and the state of the numeric (math) coprocessor must be preserved. The pre-suspend status of these subsystems are saved in a portion of memory called system management (SM) RAM. The SMRAM is enabled only during the processing of an SMI, and is disabled when the SMI service is complete.

The video controller status is not saved to SMRAM because data is preserved by the video controller during suspend. The video RAM data is preserved. The video controller enters its low power mode and turns off the LCD. If an external monitor is being used, the display will be blanked in the suspend condition due to the video (RAM) DAC being placed in a low power mode by the video controller.

Entering Suspend With The Suspend Button

When the Suspend button on the keyboard is pressed, the keyboard processor generates an SMI and the SMI handler routine is invoked. The system firmware monitors floppy and hard drive activity. Once all monitored subsystems have been detected as inactive for four seconds, the firmware continues to place the computer into the suspend condition with the procedure described earlier. The system unit can be placed into the suspend condition while on battery or AC power.

Entering Suspend By Peripheral Inactivity

The suspend condition may be entered due to peripheral inactivity. The inactivity requirements for Suspend are basically the same as those for Local Standby. In most cases, this method of entering suspend will be the result of the computer having been in the Local Standby condition. However, if the user configures the suspend timeout parameter to be shorter than the Local Standby timeout value, then the computer will, after a period of inactivity, simply enter the suspend condition directly.

When the inactivity timers monitoring peripherals all timeout, the system firmware performs the same monitor functions as with the Suspend switch.

Entering Suspend Due To Low Battery Condition

The condition of the battery pack is monitored at regular intervals. This monitoring function is handled by a controller within the battery pack itself and the peripheral controller. A serial data link is used between the battery controller and the keyboard controller to transfer the battery status byte, which is placed in a register of the keyboard controller. The battery status byte value is compared to a low battery 1 set point value.

When the battery status byte equals or is less than the low battery 1 set point value, the system firmware sounds warning beeps and a warning message is posted by Windows or Windows NT.

Entering Suspend With Software

The computer will allow application software to initiate the suspend condition. Software-initiated suspend may be useful in an application where unattended processing such as a data transfer over modem is to take place. At the end of the data transfer (or if the transfer cannot be accomplished) the application software can force the computer into the suspend condition instead of waiting for the computer to go through the timeout procedures that use more battery power.

Software-initiated suspend is effected through an INT15 call. When the system receives a suspend condition request with the INT15 call, the firmware loads a suspend warning timer with a timeout value and sets the software request bit of the of the SMC37C95XFR I/O Controller.

The suspend warning timer is loaded and the timeout is started automatically. When the suspend timer times out, an SMI is generated. The firmware determines the cause of the SMI from the SM status request register and, if the cause is the software application, places the computer into the suspend condition.

Exiting Suspend

Recovery from suspend can be initiated in the following ways:

- Pressing the Suspend button or the power switch
- Automatically due to ring indication from PC Card modem or RTC alarm
- Automatically due to Hibernation (on battery power only)

While in the suspend condition, a portion of the SMC37C95XFR controller is kept active to maintain vigilance over the system.

After exiting Suspend, the SM firmware checks the system for configuration changes that may have occurred during Suspend such as removal or installation into the convenience base or removal or installation of a PC Card.

Exiting Suspend With the Suspend Button

When the Suspend button is pressed, the SMC37C95XFR I/O Controller restarts the CPU clock and allows the CPU to begin operating by removing the STPCL signal.

The firmware then clears the suspend status bit and restores the system to the condition it was in prior to entering the suspend condition. This involves powering up devices and subsystems that were shut off, and re-enabling components that were in a low power mode. Device configurations are then restored to the pre-suspend state.

NOTE: If the computer is in the low battery 2 condition while in the suspend condition, the Suspend button cannot be used to bring the computer out of suspend. This is due to the masking of a "suspend button push" bit when the low battery 2 condition is detected.

Exiting Suspend With Hibernation

You can configure the computer to enter the Hibernation condition after being in suspend for a certain period time. The Hibernation routine is discussed in the following section.

Hibernation

The Hibernation feature is a special implementation of Suspend that helps in preventing data loss due to automatic shut down due to low battery conditions. When fully hibernated, the system is actually in the "off" state. A manual entry, or bookmark function, is also provided that initiates Hibernation through a key sequence.

Hibernation, when initiated, saves all information in memory to disk, including the exact location of the user in any open applications, then powers down the computer. Upon exiting Hibernation, the computer is returned to the exact state it was in when Hibernation was initiated. Open applications are restored and the user is returned to the exact location as when Hibernation was initiated.

Hibernation must be enabled (through the Setup utility) before it can be initiated. Once enabled, Hibernation can be initiated one of three ways:

- Upon reaching condition Low Battery 2
- With the Fn key and Suspend button (valid under battery or external power, but NOT while using the system unit docked in the expansion base)

When Hibernation is enabled, the HIBERN8.EXE utility generates a hidden system file called HIBRN8.DAT in the root directory (C:\). A pointer is written to configuration (CMOS) memory that points to the directory sector of that file. The BIOS ROM can use this file independently of the operating system. When Hibernation is initiated, the entire state of the system is written to HIBRN8.DAT and a CMOS flag is set. Upon the next power up cycle, the CMOS flag tells the system to read HIBRN8.DAT and restore the system accordingly.

System Thermal Management

The system has two primary areas of thermal management. The first is the internal AC Adapter power supply, especially when charging the Li-Ion battery. The second area is the system component temperatures, especially the main CPU. The 8051 microcontroller inside the SMC37C95xFR controller controls the batteries charge time and is the controlling device on the system I^2C bus. The fan speed control device and the CPU module temperature measurement device are interfaced to the I^2C bus and are controlled by the 8051.

The charging of the Li-Ion battery has the potential to draw the full power capacity of the power supply, and under extreme environmental conditions, cause the supply to run beyond its specified temperature limit. The 8051 microcontroller is able to monitor the battery charging status to provide the appropriate power supply cooling by turning on the fan.

A temperature sensor is included in the CPU module to monitor CPU module internal temperature. The 8051 communicates temperature information to the host system. From a table of temperature zones and corresponding fan speeds, the host system passes the appropriate fan speed to the 8051. The system is designed so that most of the air movement generated by the fan is drawn across the CPU module heat sink.

Under extreme conditions, the CPU clock speed may be reduced (throttled). Reduced clock speeds decrease CPU power consumption and resulting heat. Clocks are throttled only after the fan is running at full speed and the temperature is still determined to be too high. The fan provides sufficient cooling for the CPU for most operating conditions. It is necessary to have both forms of thermal management active to keep control of the main CPU under extreme conditions.

In summary, thermal management is achieved by the following means:

- Turning on the fan when charging a battery
- Turning on the fan when CPU temperature sensor indicates cooling is needed for the processor
- Throttling the CPU clock if temperature exceeds certain limits after the fan has been turned on at high speed

The following table summarizes the thermal management process.

Table B-5
Thermal Management

Zone	Low Threshold °C	High Threshold °C	CPU Percent	Fan Percent	Approx. Fan Voltage
0	-128	60	100	Off	0V
1	55	65	100	40	4.9V
2	61	69	100	50	5.6V
3	66	73	100	60	6.3V
4	70	79	100	70	7.0V
5	77	86	75	90	8.5V
6	84	88	50	100	11.2V
7	86	95	Standby	100	11.2V
8	86	127	Hibernation*	Off	0V

* The final zone (8) is hibernation, or Off is hibernation is not enabled.

Appendix C

Security Features

This appendix provides information to aid system administrators and program developers in the use of the security features of the computer.

Feature Descriptions

The computer provides the following security features:

- Power-On Password
- Administrative/Setup Password
- Input Lockout
- QuickLock/QuickBlank
- DriveLock
- Keyboard Lock
- Diskette Drive Control
- Hardware Locks

Power-On Password

A user can set a power-on password using POST Setup. This password will then be stored in an 8051 protected NV RAM device. Each time the system is powered on the user will be prompted for the power-on password. This password can be removed by entering the password followed by a slash.

The power-on password integrates the power-on (boot), return from Hibernation, and QuickLock password functions. The POST routine checks the non-volatile configuration memory to determine if password protection is being used and, if so, allows the user to enter the password in the security menu. The user is limited to three power-on password entry attempts.

Administrative/Setup Password

The user can set up an administrator password using POST Setup. This password is stored in an 8051 protected NV RAM device. Each time the user attempts to run Setup, the system prompts the user for the administrator password. This password can be removed by entering the password followed by a slash. To enter Setup for the intent of making changes to the system, the user must correctly enter the setup password. The system allows a limit of three attempts to enter the correct password. Once the correct password is entered, the user is able to make configuration changes.

If the administrator password is lost or forgotten, the following procedure is recommended to regain access to Setup.

1. Remove AC power.
2. Remove the keyboard, audio daughter board, audio/modem board and the audio board bracket.
3. Remove all batteries from the system including unplugging the auxiliary battery and the RTC coin cell battery.
4. Allow the computer to set for at least 5 minutes.
5. Reinstall the auxiliary battery and RTC coin cell.
6. Re-apply AC power to the unit through the AC power adapter with no batteries in the unit.

When the system restarts with the Error 162-System options not set, re-enter Setup and make the proper entries.

QuickLock/QuickBlank

The QuickLock feature allows a user to lock the keyboard while within an application by invoking a hotkey combination (see “Hotkeys” section of Chapter 9). This action guards against tampering with a system while the user is away from the workstation. When enabling the QuickLock feature, the user has the additional option of enabling/disabling the QuickBlank feature. When in QuickBlank, both internal and external screens are blanked and the lock icon will not appear when the mouse is moved or a key is pressed. After the correct power-on password has been entered, the system will exit the QuickLock/QuickBlank mode and return to full power operation. There is no limit on the number of password entry attempts.

QuickLock on Suspend

The QuickLock feature can be enabled so that it is actvated when the user places the system in Suspend. In this mode, the system power-on password protects against unauthorized access to the system while in Suspend. When the user exits Suspend, the password is presented for power-on password entry before exiting Suspend. There is no limit to the number of password entry attempts.

DriveLock

The DriveLock feature allows a user to lock a hard drive to prevent unauthorized access to the applications and data on the drive. The password may be set on each removable drive in the computer.

The drive may be unlocked only when in the system MultiBay, or in the hard drive bay of the computer. DriveLock cannot be used on drives in the desktop or convenience expansion bases. DriveLock protected drives cannot be unlocked when placed in either of the expansion bases.

Passwords

Two passwords are associated with the DriveLock feature:

- User password—used by the daily user of the drive to prevent unauthorized use of the drive.
- Master password—used by the system administrator to remove DriveLock protection. The master password can also be used to reset the user password.

The Compaq power-on password may be used to simplify DriveLock password prompting. If a power-on password is set, and a DriveLock user or master password on that drive is set to the same password, the user will see only the power-on password prompt. The power-on password will be applied as a DriveLock password, thereby gaining access to the drive.

BIOS Support for DriveLock

The BIOS provides support for DriveLock through F10 based setup. Once enabled, the user is prompted for the password on startup or cold-boot. The user is not prompted for the password on warm-boot.

Blocking DriveLock

If a system administrator wishes to restrict the use of the DriveLock feature, there are two methods available:

- Set a Compaq setup password so the user cannot access F10 Setup, where DriveLock protection can be changed
- Enable DriveLock protection, and give the user the DriveLock user password only.

Recovery

If the DriveLock user password is lost but the master password is known, the drive can be recovered by using F10 Setup and the DriveLock master password to remove the protection. If the DriveLock master password is lost and the user password is known, the drive is technically recoverable.

***CAUTION:** Losing both the master password and user password will render the hard drive permanently inaccessible.*

Keyboard Lock

The Keyboard Lock function, when invoked, allows the system to completely boot up but will not allow user input until the power-up password has been entered. There is no limit on the number of password entry attempts.

Diskette Drive Protection

The diskette drive is protected in three different ways:

Drive Disable	*The diskette drive can be disabled by setting bit <1> at location 2065h, index 99. Clearing bit <1> enables the diskette drive to be accessed (default condition). Note that if bit <2> of port 99h is set (1), then bit <1> of 2065.99h cannot be changed, thus providing more security from inadvertently enabling/disabling the diskette drive.*
Drive Write Protect	*Writes to the diskette drive can be inhibited by clearing bit <3> of 2065.99h. This condition protects against unauthorized copying of system software. Setting bit <3> to a one (1) enables writes to the diskette drive (default condition).*
Drive Boot Disable	*Booting from the diskette drive is prevented when the Diskette Boot Disable feature is select during setup. This feature prevents the system from being booted up by an undesirable DOS or boot-type configuration disk. The normal diskette read function is preserved.*

Hardware Locks

Several physical locks are provided to prevent unauthorized removal of the computer and the modular subassemblies. The locking devices are described in the following topics.

Hard Drive

The user is able to “lock” the hard drive in the dedicated drive bay using a security screw.

Cable Lock

The computer base can be secured to an immovable object using an optional cable lock.

MultiBay Devices

The user is able to “lock” devices in the MultiBay by using a security screw.

Programming Information

During the boot sequence, the BIOS ROM reads the parameters stored in the NVRAM (non-volatile RAM) by the Setup utility. Additionally, software programs may access the configuration memory and certain I/O ports to read the status of the security features.

Status Read Of Security Features

The CMOS configuration byte at location 13h contains the status of the security features as shown below:

RTC Configuration Memory Location 13h

BIT	**FUNCTION**
7	*Reserved - DO NOT CHANGE**
6	*Enable Quickblank after standby* *(Quicklock/Quickblank is also enabled)* 0 = *Disabled* ***1*** = *Enabled*
5	*Administrator Password* 0 = *Not present* ***1*** = *Present*
4	*Reserved - DO NOT CHANGE**
3	*Diskette Boot Enable* 0 = *Enabled* ***1*** = *Disabled*
2	*QuickLock* 0 = *Disabled (default)* ***1*** = *Enabled*
1	*Network Server / Security Lock Override* 0 = *Disable* ***1*** = *Enable*
0	*Password State (Set by ROM at power up)* 0 = *Not set* ***1*** = *Set*

Status Read Of Security Features Involving Peripherals

The configuration bytes located at RTC memory address 26h and 29h contains the control bits for the serial and parallel interfaces as well as the fixed disk and diskette drive controllers as shown below:

RTC Configuration Byte **26***h*

BIT	**FUN***CTI***ON**
7..**1**	R*eserved* **-** *D*O NOT *CHANGE**
0	*Diskette controller* 0 = *Disabled* ***1*** = *Enabled*

RTC Configuration Byte **29***h,*
*I/***O** *Port Address* **0***C***65***h*

BIT	**FUN***CTI***ON**
7	R*eserved* **-** *D*O NOT *CHANGE**
6,5	*Parallel interface* 00 = *Primary* 0***1*** = *Secondary* ***1***0 = T*ertiary* ***11*** = *Disabled*
4	*Fixed disk drive controller* 0 = *Disabled* ***1*** = *Enabled*
3	R*eserved* **-** *D*O NOT *CHANGE**
2	R*eserved* **-** *D*O NOT *CHANGE**
1	*Serial interface* 0 = *Disabled* ***1*** = *Enabled*
0	R*eserved* **-** *D*O NOT *CHANGE**

* R*efer to Chapter* ***3*** **-** *Processor/System Support under* R*eal T*ime *Clock and Configuration Memory*

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