COMPAQ

Professional Workstation

Technical Reference Guide

The hardcopy of this document is designed to be placed into a standard 3-ring binder. Provided below is a title block that can be copied and cut out and placed into the slip or taped onto the edge of the binder.

COMPAQ *Professional Workstation TRG*

NOTICE

The information in this document is subject to change without notice.

COMPAQ COMPUTER CORPORATION SHALL NOT BE LIABLE FOR TECHNICAL OR EDITORIAL ERRORS OR OMISSIONS HEREIN; NOR FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES RESULTING FROM THE FURNISHING, PERFORMANCE, OR USE OF THIS MATERIAL. IT IS THE RESPONSIBILITY OF MANUFACTURERS TO ENSURE THAT DEVICES DESIGNED TO BE USED WITH COMPAQ PRODUCTS COIMPLY WITH FCC CLASS B EMISSIONS REQUIREMENTS.

For more information regarding specifications and Compaq-specific parts please contact Compaq Computer Corporation, Industry Relations Department.

Compaq Professional Workstation Technical Reference Guide
First Edition - November 1996
Document Number 213A/1196

First Edition - November 1996

TABLE OF CONTENTS

First Edition - November 1996

LIST OF FIGURES

LIST OF TABLES

Chapter 1
INTRODUCTION

1.1 ABOUT THIS GUIDE

This guide provides technical information about the Compaq Professional Workstation. This document includes information regarding system design, function, and features that can be used by programmers, engineers, technicians, and system administrators.

1.1.1 USING THIS GUIDE

This guide consists of chapters and appendices. The chapters primarily describe the hardware and firmware elements contained within the chassis and specifically deal with the system board and the power supply assembly. The appendices contain general information about standard peripheral devices such as the keyboard as well as separate graphics or other interface cards, as well as other general information in tabular format.

1.1.2 ADDITIONAL INFORMATION SOURCES

This guide does not describe in detail other manufacturer's components used in the product covered. For more information on individual commercial-off-the-shelf (COTS) components refer to the indicated manufacturers' documentation. The product covered by this guide uses architecture based on industry-standard specifications. For a detailed description on industry-standard designs and architecture referred to in this guide refer to the following publications:

- The Lotus/Intel/Microsoft Expanded Memory Specification, Ver. 4.0
- PCI Local Bus Specification Revision 2.1
- Extended Industry Standard Architecture Expansion Bus Technical Reference Guide, p/n 130584, Second Edition, Compaq Computer Corporation
- Compaq Basic Input/Out System (BIOS) Technical Reference Guide
  Doc.# 074A/0693, Fourth Edition, Compaq Computer Corporation

1.2 NOTATIONAL CONVENTIONS

1.2.1 VALUES

Hexadecimal values are indicated by the letter “h” following an alpha-numerical value. Binary values are indicated by the letter “b” following a value of ones and zeros. Memory addresses expressed as “SSSS:OOOO” (SSSS = 16-bit segment, OOOO = 16-bit offset) can be assumed as a hexadecimal value. Values that have no succeeding letter can be assumed to be decimal.

1.2.2 RANGES

Ranges or limits for a parameter are shown as a pair of values separated by two dots:

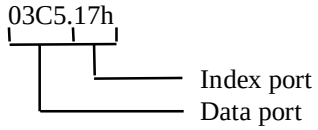
Example: Bits <7..4> = bits 7, 6, 5, and 4.

1.2.3 SIGNAL LABELS

Signal names are indicated using abbreviations, acronyms, or, if possible, the full signal name in all capital letters. Signals that are meant to be active low are indicated with a dash immediately following the name.

1.2.4 REGISTER NOTATION AND USAGE

This guide uses standard Intel naming conventions in discussing the microprocessor’s (CPU) internal registers. Registers that are accessed through programmable I/O using an indexing scheme are indicated using the following format:



In the example above, register 03C5.17h is accessed by writing the index port value 17h to the index address (03C4h), followed by a write to or a read from port 03C5h.

1.2.5 BIT NOTATION

Bit values are labeled with bit <0> representing the least-significant bit (LSb) and bit <7> representing the most-significant bit (MSb) of a byte. Bytes, words, double words, and quad words are typically shown with most-significant portions on the left or top and the least-significant portions on the right or bottom respectively.

1.3 COMMON ACRONYMS AND ABBREVIATIONS

Table 1-1 lists the acronyms and abbreviations used in this guide.

Table 1-1.
Acronyms and Abbreviations

Acronym/Abbreviation	Description
A	ampere
AC	alternating current
ACK	acknowledge
A/D	analog-to-digital
API	application programming interface
APM	advanced power management
ASIC	application-specific integrated circuit
AT	1. attention (commands) 2. 286-based PC architecture
ATA	AT attachment (mode)
AVI	audio-video interleaved
AVGA	Advanced VGA
BCD	binary-coded decimal
BIOS	basic input/output system
bis	second/new revision
BitBLT	bit block transfer
BNC	Bayonet Neill-Concelman (connector)
bps or b/s	bits per second
BSP	Bootstrap processor
CAS	column address strobe
CD	compact disk
CD-ROM	compact disk read-only memory
CDS	compct disk system
CEMM	Compaq expanded memory manager
CF	carry flag
CGA	color graphics adapter
Ch	channel
CLUT	color look-up table (pallete)
cm	centimeter
CMC	cache/memory controller
CMOS	complimentary metal-oxide semiconductor (configuration memory)
Cntlr	controller
codec	compressor/decompressor
CPQ	Compaq
CPU	central processing unit
CRT	cathode ray tube
CSM	Compaq system management / Compaq server management
DAA	direct access arrangement
DAC	digital-to-analog converter
db	decibel
dbm	decibel referenced to one milliwatt
DC	direct current
DCH	DOS compatibility hole
DDC	Display Data Channel
DF	direction flag
DIN	Deutche IndustriNorm (connector standard)
DIP	dual inline package
DMA	direct memory access
dpi	dots per inch
DRAM	dynamic random access memory
DRQ	data request
DOS	disk operating system
DSP	digital signal processor

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
DTE	data terminal equipment
DTMF	dual-tone multi-frequency
ECC	error correction code
ECP	extended capabilities port
EDID	extended display identification data
EDO	extended data out (RAM type)
EEPROM	electrically eraseable PROM
EGA	enhanced graphics adapter
EIA	Electronic Industry Association
EISA	extended ISA
EPP	enhanced parallel port
EIDE	enhanced IDE
ExCA	Exchangeable Card Architecture
FIFO	first in / first out
FL	flag (register)
FM	frequency modulation
FPM	fast page mode (RAM type)
FPU	Floating point unit (numeric or math coprocessor)
ft	foot
GB	gigabyte
GND	ground
GPIO	general purpose I/O
GUI	graphics user interface
h	hexadecimal
HW	hardware
hex	hexadecimal
Hz	hertz
IDE	integrated drive element
IEEE	Institute of Electrical and Electronic Engineers
IF	interrupt flag
I/F	interface
in	inch
INT	interrupt
I/O	input/output
IrDA	InfraRed Data Association
IRQ	interrupt request
ISA	industry standard architecture
Kb / KB	kilobits / kilobytes (x 1024 bits / x 1024 bytes)
Kb/s	kilobits per second
kg	kilogram
KHz	kilohertz
kv	kilovolt
lb	pound
LCD	liquid crystal display
LED	light-emitting diode
LIF	low insertion force (socket)
Li-ion	lithium-ion
LPB	local peripheral bus
LSI	large scale integration
LSb / LSB	least significant bit / least significant byte
LUN	logical unit (SCSI)
m	meter
mA	milliampere
Mb / MB	megabit / megabyte (1 x 2^{20} for memory, 1 x 10^{6} for mass storage)
MDA	monochrome display adapter

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
MIDI	musical instrument digital interface
ML	multiplexed local bus
MPEG	Motion Picture Experts Group
ms	millisecond
MSb / MSB	most significant bit / most significant byte
mux	multiplex
MVA	motion video acceleration
MVW	motion video window
n	variable parameter/value
NIC	network interface card/controller
NiCad	nickel cadmium
NiMH	nickel-metal hydride
NMI	non-maskable interrupt
ns	nanosecond
NT	nested task flag
NTSC	National Television Standards Committee
NVRAM	non-volatile random access memory
OS	operating system
PAL	1. programmable array logic 2. phase altering line
PC	personal computer
PCI	peripheral component interconnect
PCM	pulse code modulation
PCMCIA	Personal Computer Memory Card International Association
PF	parity flag
PIN	personal identification number
POST	power-on self test
PROM	programmable read-only memory
PTR	pointer
RAM	random access memory
RAS	row address strobe
rcvr	receiver
RF	resume flag
RGB	red/green/blue
RH	Relative humidity
RMS	root mean square
ROM	read-only memory
RPM	revolutions per minute
RTC	real time clock
R/W	read/write
SCSI	small computer system interface
SECAM	sequential colour avec memoire (sequential color with memory)
SF	sign flag
SIMM	single in-line memory module
SIT	system information table
SMI	system management interrupt
SMM	system management mode
SMRAM	system management RAM
SPP	standard parallel port
SRAM	static RAM
STN	super twist pneumatic
SVGA	super VGA
SW	software
TAD	telephone answering device

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
TAM	telephone answering machine
TCP	tape carrier package
TF	trap flag
TFT	thin-film transistor
TIA	Telecommunications Information Administration
TPE	twisted pair ethernet
TPI	track per inch
TTI	transistor-transistor logic
TV	television
TX	transmit
UART	universal asynchronous receiver/transmitter
us / µs	microsecond
USB	Universal Serial Bus
V	volt
VESA	Video Electronic Standards Association
VGA	video graphics adapter
vib	vibrato
VLSI	very large scale integration
VRAM	Video RAM
W	watt
WRAM	Windows RAM
ZF	zero flag
ZIF	zero insertion force (socket)

Chapter 2
SYSTEM OVERVIEW

2.1 INTRODUCTION

The Compaq Professional Workstation (Figure 2-1) is designed with an emphasis on speed, storage capacity, and multimedia compatibility to meet the requirements of intensive CAD/CAM applications and software development. The Professional Workstation features an architecture based on Pentium Pro microprocessors incorporating the PCI and ISA busses and running the Windows NT 4.0 operating system. All models are easily upgradeable and expandable to keep pace with the needs of the office.

Figure 2–1. Compaq Professional Workstation with Monitor

2.2 FEATURES

This section describes the standard and distinguishing features.

2.2.1 STANDARD FEATURES

The following standard features are included on all models:

- One or two Pentium Pro microprocessors
- 3.5 inch, 1.44-MB diskette drive
- IDE 8X CD-ROM drive
- Integrated audio controller
- Enhanced IDE controller support for up to four IDE drives
- Integrated Ultra SCSI adapter
- Hard drive fault prediction
- PCI-based graphics
- Two serial interfaces
- Parallel interface
- 32-bit 10Base-T/100Base-TX Autosensing network interface controller
- Three dedicated PCI slots
- One dedicated ISA slot
- One combination PCI/ISA slot
- 240-watt power supply
- Easy serviceability features
- Compaq Space Saver keyboard with Windows support
- Compaq PS/2-type mouse
- APM 1.2 power management support
- Plug ’n Play compatible (with ESCD support)
- Client management support (Intelligent Manageability)
- Security features including:
    - Flash ROM write-protect
    - Diskette drive disable, boot disable, write protect
    - Power-on password
    - Administrator password
    - QuickLock/QuickBlank
    - Serial port disable
    - Parallel port disable
    - Hood removal sensor/indicator

2.2.2 OPTIONS

Options that are specific to the Compaq Professional Workstation include:

- Memory:
  - 16-MB Memory Module
  - 32-MB Memory Module
  - 64-MB Memory Module
  - 128-MB memory Module

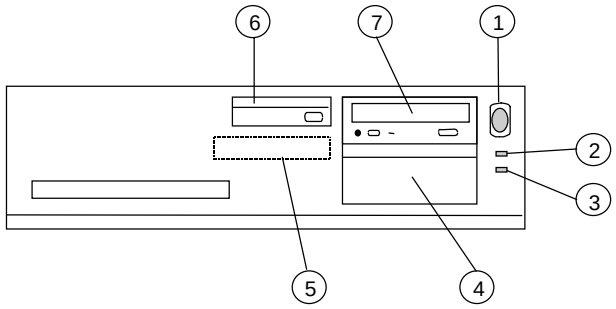
- Graphics:
  - 2-/6-MB WRAM Upgrade Modules (Matrox Millennium Card)
  - 8-MB DRAM Upgrade Module (ELSA GLoria-L Graphics Card)

The Compaq Professional Workstation is easily upgraded and enhanced with peripheral devices designed to meet PCI and ISA standards. The Compaq Professional Workstation is compatible with peripherals design for Plug ’n Play operation.

2.3 MECHANICAL DESIGN

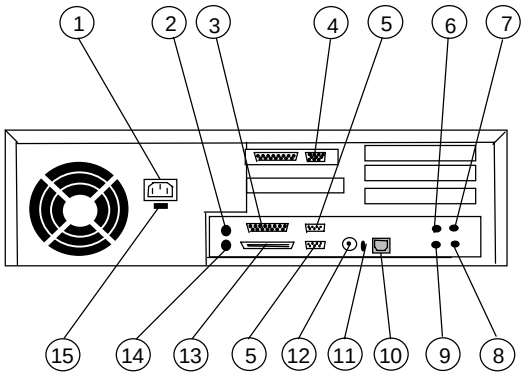
This section illustrates the mechanical design of the Professional Workstation. In addition, this section includes the layouts of the system boards.

2.3.1 CABINET LAYOUT



Item	Function
1	Power Switch
2	Power-On Light
3	Hard Drive Activity Light
4	½ Height Drive Bay (3.5” or 5.25” Drive)
5	1/3 Height Internal Drive Bay (3.5” Drive)
6	1.44 MB Diskette Drive (3.5” Drive)
7	CD-ROM drive

Figure 2–2. Cabinet Layout, Front View



Item	Function
1	AC Line In Connector
2	Mouse Interface Connector
3	Parallel Interface Connector
4	Monitor Interface Connector
5	Serial Interface Connector
6	Microphone Input Connector
7	Audio Line In Connector
8	Audio Line Out Connector
9	Headphone Out Connector
10	Network Interface (RJ-45) Connector
11	Network activity LED Connector
12	Network Interface (BNC) Connector
13	Ultra SCSI Interface Connector
14	Keyboard Interface Connector
15	Line Voltage Select Switch

Figure 2–3. Cabinet Layout, Rear View

2.3.2 CHASSIS LAYOUT

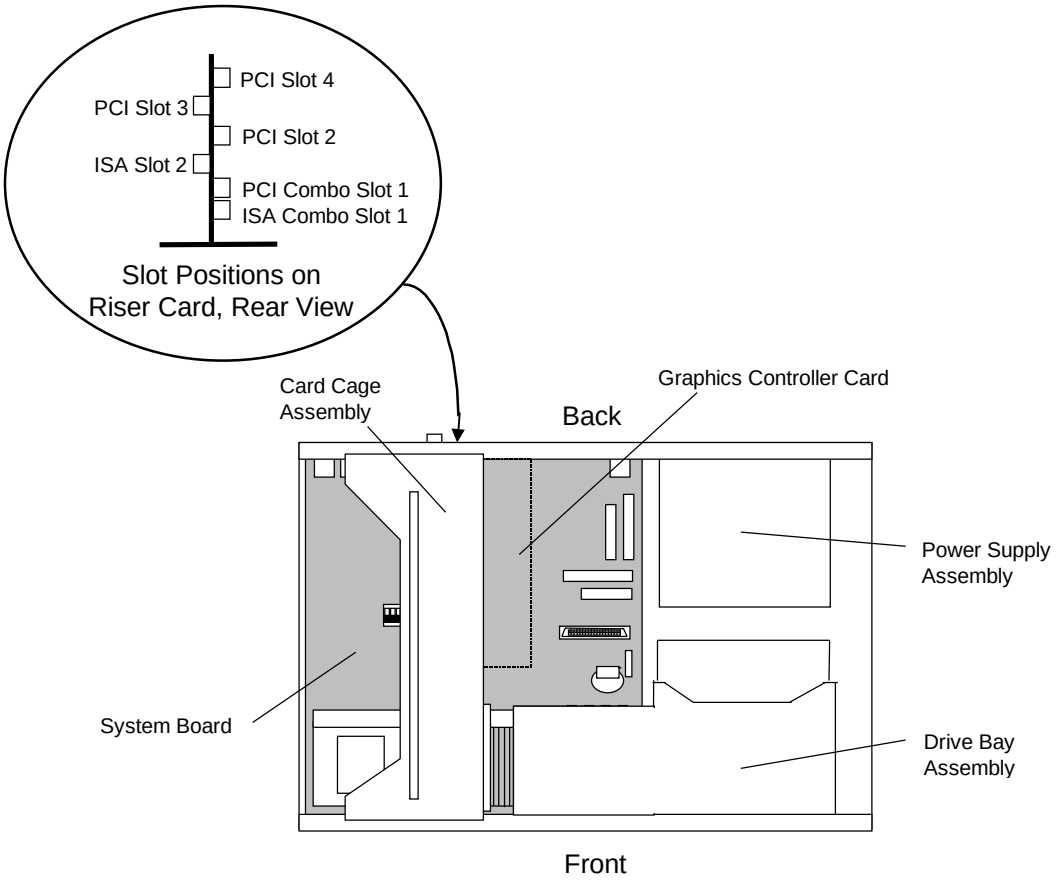
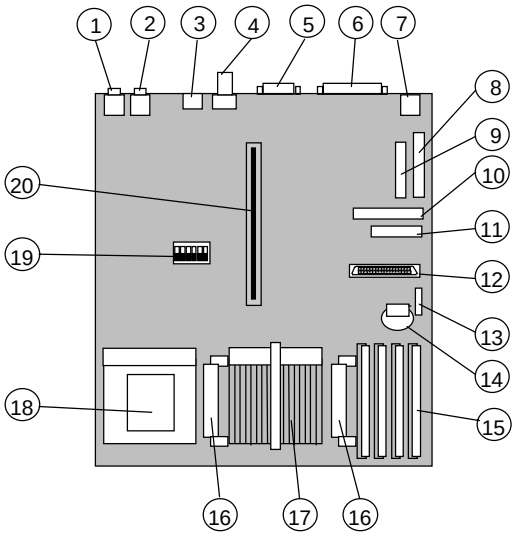


Figure 2–4. Chassis Layout, Top View

The chassis is designed for easy access to expansion cards and mass storage (drive) units. With the chassis cover removed, the card cage assembly can be removed from the chassis as a unit complete with expansion cards and riser card. With the front bezel also removed from the chassis, the drive bay assembly can also be removed as a unit complete with drives.

2.3.3 SYSTEM BOARD LAYOUT



Item	Function
1 (Top)	Line In (audio) connector
1 (Bottom)	Line Out (audio) connector
2 (Top)	Mic (audio) connector
2 (Bottom)	Headphones (audio) connector
3	Network I/F connector (RJ-45)
4	Network I/F connector (BNC)
5	Serial I/F connectors (2)
6 (Top)	Parallel I/F connector
6 (Bottom)	Ultra SCSI connector
7 (Top)	Mouse connector
7 (Bottom)	Keyboard connector
8	Power supply connector
9	Power supply connector
10	IDE connector
11	Diskette drive connector
12	Wide-Ultra SCSI connector
13	Battery replacement header
14	RTC/CMOS battery
15	DIMM sockets
16	Voltage Regulator
17	Microprocessor (P1) in socket
18	P2 microprocessor socket (populated on some models)
19	DIP Switch (SW1)
20	Riser Card connector

Figure 2–5. System Board Layout, Component Side

2.4 SYSTEM ARCHITECTURE

The Compaq Professional Workstation is based on the Pentium Pro microprocessor matched with a support chipset that is complimentary in design. The system architecture (Figure 2-6) utilizes three main buses: the Host bus, the Peripheral Component Interconnect (PCI) bus, and the Industry Standard Architecture (ISA) bus.

The Host bus provides high performance support for CPU, cache and system memory accesses, and operates at 50 to 75 % of the processing speed of the microprocessor, depending on processor speed configuration. The PCI bus provides support for the graphics subsystem, the EIDE controllers, and expansion devices designed for high performance. The PCI bus operates at typically 50 % of the Host bus speed. The ISA bus provides a standard 8-MHz interface for the input/output (I/O) devices such as the keyboard, diskette drive, serial and parallel interfaces, as well as the addition of 16- or 8-bit expansion devices.

The Host/PCI bridge function is handled by Intel 82441 and 82442 components. These components provide memory controller and data buffering/accelerator functions as well as bus control and arbitration functions.

The PCI/ISA bridge function is provided by the Compaq OSB ASIC, which also includes IDE interfaces for mass storage peripherals.

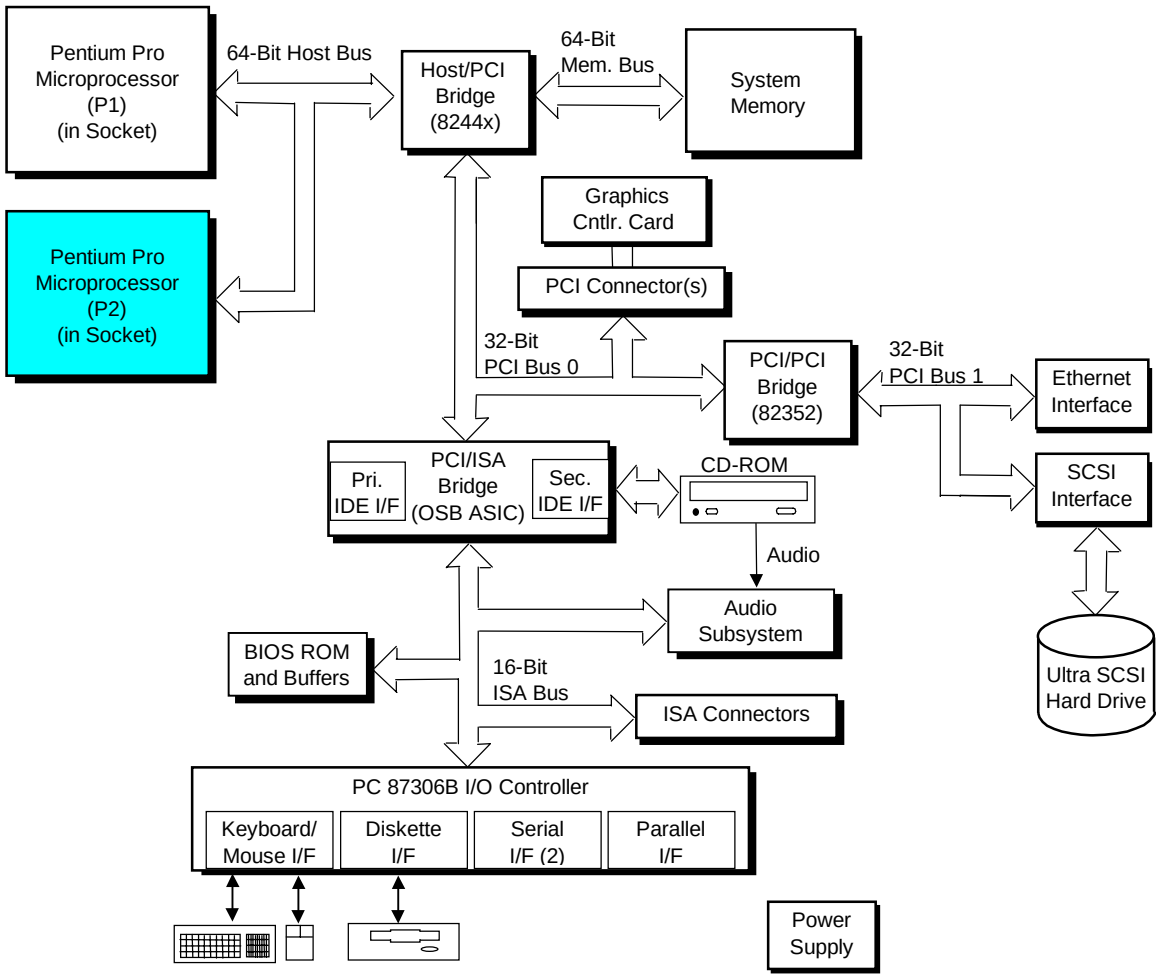
The I/O port functions and diskette drive controller are integrated into the PC87306 I/O Controller. This component also includes the real time clock and battery-backed configuration memory (CMOS).

The Compaq Professional Workstation is shipped in several standard configurations as shown in Table 2-1.

Table 2-1.
System Configurations

	2691120-002	**269120-003**	**269120-004**	**269120-006**	**269130-002**
Pentium Pros Installed:	1	1	1	1	2
Hard Drive Size:	2.1 GB	2.1 GB	4.3 GB	4.3 GB	4.3 GB
System Memory Installed:	32 MB	64 MB	64 MB	64 MB	128 MB
Graphics Subsystem:	Millennium PCI Card	Millennium PCI Card	GLoria-L PCI Card	GLoria-L PCI Card	GLoria-L PCI Card

The following subsections provide a description of the key functions and subsystems.



Second processor (P2) standard on some models, optional on others. See Table 2-1.

Figure 2–6. Compaq Professional Workstation System Architecture, Block diagram

2.4.1 MICROPROCESSOR

The Compaq Professional Workstation features the Pentium Pro microprocessor. This microprocessor is backward-compatible with software written for x86-type microprocessors, but provide a dramatic increase in performance over earlier x86-type and Pentium components. The Pentium Pro microprocessor includes a dual-ALU central processing unit (CPU) with branch prediction support and an integrated 16-KB cache along with a math coprocessor. In addition, the Pentium Pro microprocessor integrates a 256-KB secondary cache and supports out-of-order instruction processing. Zero-insertion-force (ZIF) type-8 sockets are employed for easy upgrading. The type 8 socket used on the Pentium Pro-based system boards supports the P6S series of microprocessors.

2.4.2 MEMORY SUBSYSTEM

The memory subsystem consists of the memory controller, data buffers, and system memory (DRAM) installed in one to four Dual Inline Memory Module (DIMM) sockets. Standard configurations include 32, 64, or 128 megabytes of 60 ns, unbuffered EDO DRAM. Memory can be expanded to a maximum of 512 megabytes.

2.4.3 GRAPHICS CARD

The Compaq Professional Workstation comes with a graphics card installed in a PCI slot. One of two types of cards (Table 2-2) may be installed, depending on model.

Table 2-2.
Graphics Card Comparison

	Matrox Millennium PCI Graphics Card	**GLoria-L PCI Graphics Card**
Graphics Controller	MGA2064W	GLINT 500TX 3D Processor
Graphics Memory:		
Standard installed:	2 MB WRAM	8 MB VRAM / 8 MB DRAM
Expandable to:	8 MB WRAM	na / 16 MB DRAM
Maximum Resolution		
w/ standard mem.	1600x1200 @ 256 colors	1600x1280 @ 32K colors
w/ max. mem.	1600x1200 @ 16.7M	1600x1200 @ 16M colors

2.4.4 MASS STORAGE

All models include a 3.5 inch 1.44-MB diskette drive, a CD-ROM drive, and a Fast-Wide SCSI hard drive installed. Support is provided for additional Fast-Wide SCSI and/or IDE hard drives.

2.4.5 SERIAL AND PARALLEL INTERFACES

All models include two serial and one parallel port available at the rear of the unit. The serial and parallel ports are integrated into a PC87306 I/O Controller component. Each serial port is RS-232-C/16550-compatible and operates at baud rates up to 19,000. The parallel interface is Enhanced Parallel Port (EPP) and Enhanced Capability Port (ECP) compatible, and supports bi-directional data transfers.

2.5 SPECIFICATIONS

This section includes the environmental, electrical, and physical specifications for the Compaq Professional Workstation.

Table 2-3.
Environmental Specifications

Parameter	Operating	Nonoperating
Air Temperature	50° to 95° F (10° to 35° C)	-40° to 158° F (-40° to 70° C)
Shock	2.0 g for 11 ms half-sine pulse	30.0 g for 11 ms half-sine pulse
Vibration	1 G for 5-200 Hz sinusoidal	N/A
Humidity	90% RH @ 36° C (no hard drive)	95% RH @ 36° C
Maximum Altitude	10,000 ft (3048 m)	30,000 ft (9,144 m)

Table 2-4.
Electrical Specifications

Parameter	Domestic	International
Input Line Voltage:		
Nominal:	100 - 120 VAC	200 - 240 VAC
Maximum:	90 - 135 VAC	180 - 265 VAC
Input Line Frequency Range:		
Nominal:	50 - 60 Hz	50 - 60 Hz
Maximum:	47 - 63 Hz	47 - 63 Hz
Power Supply:		
Maximum Continuous Power:	240 watts	240 watts
Maximum Line Current Drain:	6.0 A	3.0 A

Table 2-5.
Physical Specifications

Paramemter	Dimensions
Height	5.25 in (13.34 cm)
Width	19.25 in (48.90 cm)
Depth	15.69 in (39.85 cm)
Weight	35.65 lb (12.85 kg)

NOTE:
Metric measurements shown in parenthesis.

Table 2-6.
Diskette Drive Specifications

Paramemter	Measurement
Media Type	3.5 in 1.44 MB/720 KB diskette
Height	1/3
Bytes per Sector	512
Sectors per Track:	
High Density	18
Low Density	9
Tracks per Side:	
High Density	80
Low Density	80
Read/Write Heads	2
Average Access Time:	
Track-to-Track (high/low)	3 ms/3 ms
Average (high/low)	94 ms/94ms
Settling Time	15 ms
Latency Average	100 ms

Table 2-7.
8x CD-ROM Drive Specifications

Paramemter	Measurement
Media Type	Mode 1,2, Mixed Mode, CD-DA, Photo CD, Cdi, CD-XA
Center Hole Diameter	15 mm
Disc Diameter	8/12 cm
Disc Thickness	1.2 mm
Track Pitch	1.6 um
Laser	
Beam Divergence	53.5 +/- 1.5 °
Output Power	53.6 0.14 mW
Typr	GaAs
Wave Length	790 +/- 25 nm
Average Access Time:	
Random	150 ms
Full Stroke	350 ms
Audio Output Level	0.7 Vrms
Cache Buffer	128 KB (min)
Data Transfer Time	
Sustained	1200 KB/s
Startup Time	7 secs (nom)

Table 2-8.
PD-CD Drive Specifications

Paramemter	Measurement
Media Type	Mode 1,2, Mixed Mode, CD-DA, Photo CD, Cdi, CD-XA, CD-WO
Center Hole Diameter	15 mm
Disc Diameter	8/12 cm
Disc Thickness	1.2 mm
Track Pitch:	
CD	1.6 mm
PD	1.2 mm
Laser	
Beam Divergence	53.5 +/- 1.5 °
Output Power	13.5 mW +/- 2.0 mW
Type	GaAs
Wave Length	790 nm +/- 25 nm
Average Access Time:	
Random:	
Quad-Speed CD-ROM Mode	< 240 ms
PD Mode	<200 ms
Full Stroke:	
Quad Speed CD-ROM Mode	<350 ms
PD Mode	<275 ms
Audio Output Level	0.7 Vrms
Cache Buffer	256 KB
Startup Time (nom)	<7 seconds
Stop Time (nom)	<3 seconds
SCSI Bus Rate	
Asynchronous	3.0 MB/s
Synchronous	5.0 MB/s
Data Transfer Time (sustained):	
Single-Speed CD-ROM Mode	150 KB/s
Dual-Speed CD-ROM Mode	300 KB/s
Quad-Speed CD-ROM Mode	600 KB/s
PD Mode	500-1100 KB/s

Table 2-9.
Hard Drive Specifications

	2.1 GB	4.3 GB
Interface	SCSI	SCSI
Physical Capacity (Formatted)	2140 MB	4510 MB
Drive Size	5.25 in	5.25 in
Buffer Size	954 KB	512 KB
Transfer Rate (Interface)	20.0 MB/s	20.0 MB/s
Seek Time (w/settling)		
Single Track	1.9 ms	2.5 ms
Average	10.0ms	9.5 ms
Full Stroke	22.0 ms	18.0 ms
Disk RPM	7200	7200
Cylinders (logical)	3511	4390
Data Heads (logical)	11 Data, 1 Servo	16 (Emb. Servo)
Sectors per Track (logical)	86-125	100-135

This page is intentionally blank.

Chapter 3
PROCESSOR/ MEMORY SUBSYSTEM

3.1 INTRODUCTION

This chapter describes the processor/cache memory subsystem of the Compaq Professional Workstation. This chapter includes the following topics:

The processor/memory subsystem uses an 82442 data buffer/accelerator, an 82441 system controller, and comes standard with 32, 64, or 128 megabytes of 60 ns DRAM for system memory (Figure 3-1).

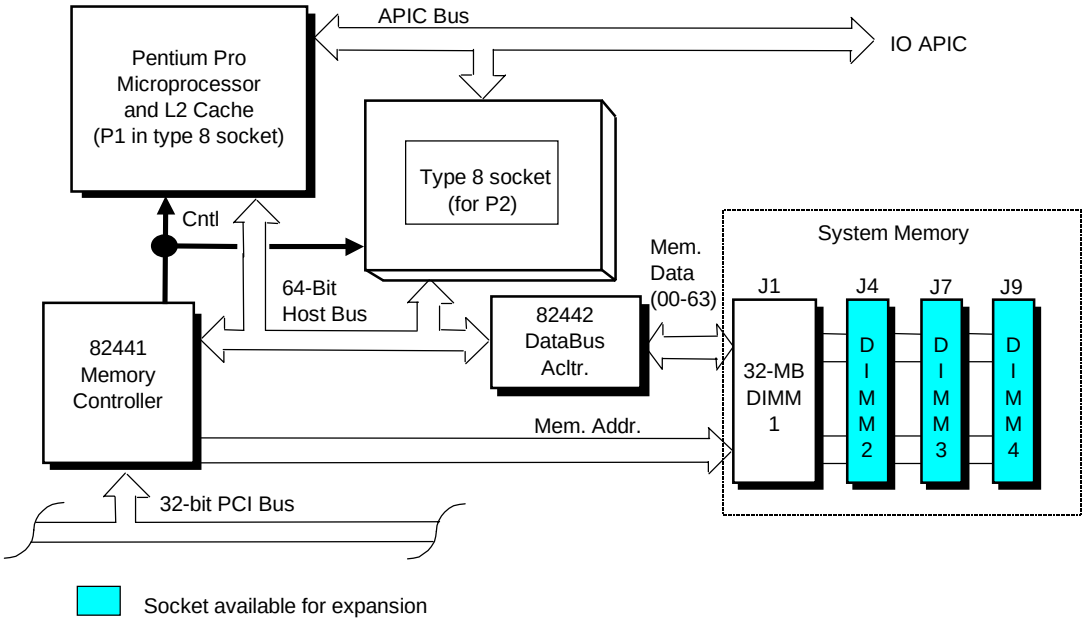


Figure 3–1. Processor/Memory Subsystem Architecture

The system comes standard with a Pentium Pro microprocessor mounted in a type-8 ZIF socket that facilitates easy changing/upgrading. An additional type 8 socket is provided for adding a second (P2) microprocessor. The type-8 socket supports P6.0, P6S, and P6T microprocessors. Replacing the microprocessor may require reconfiguring a DIP switch to select the correct bus frequency/core frequency combination, and is described in detail later in this section. The 82441system controller provides the Host/PCI bridge functions and drives the memory address lines. The 82441 handles transfers with the 64-bit memory data bus. The system provides four DIMM (dual-72-pin) sockets. Memory can be expanded up to 512 megabytes.

3.2 PENTIUM PRO MICROPROCESSOR

The Pentium Pro microprocessor is the successor to the Pentium microprocessor and integrates such features as dual ALUs, branch prediction logic, 16-KB L1 cache, a 256-KB L2 cache, and pipelined math coprocessor (Figure 3-2).

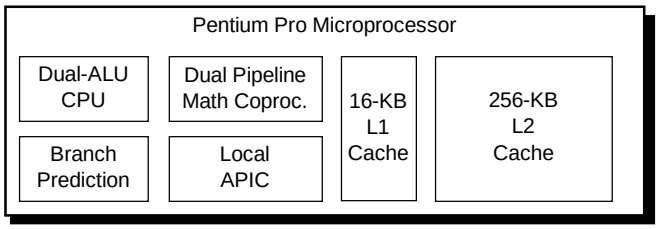


Figure 3–2. Pentium Pro Microprocessor

The Pentium Pro microprocessor is software-compatible with earlier x86-type microprocessors but provides significantly enhanced performance due to a number of enhancements such as:

- Integrated L1 cache with separate sections for code and data
- Integrated 256-KB second-level cache
- Super-scalar architecture
- Internal error checking (Machine Check Architecture)
- Model-specific register programming
- Out-of-order instruction processing support

The type, stepping, and L2 cache size of the Pentium Pro microprocessor can be obtained with the CPUID instruction. When the CPUID instruction is executed with EAX = 1, the type and stepping is returned in the EAX register (i.e., a P6S processor of B0 stepping would be identified with 0616h in EAX). When the CPUID instruction is executed with EAX = 2, the cache size is returned in the EDX register (i.e., if 256 KB cache then EDX = 42h; if 512 KB cache then EDX = 43h). For detailed information on the Pentium Pro microprocessor refer to the manufacturer's documentation.

3.2.1 DUAL PROCESSOR OPERATION

The system includes an IO APIC component that facilitates multi-processor operation. The Local APIC of the microprocessors intercommunicate through the APIC bus to determine such aspects as to which processor is to be the Bootstrap processor (BSP) and which processor is to handle interrupts. Interrupt processing in dual-processor configurations is handled using APIC mode, which is discussed in more detail in chapter 4.

This system provides a Hot Spare Boot function, where should one of the microprocessors fail due to an internal error the condition is logged into NVRAM and detected by BIOS during a reset. The failed microprocessor is tri-stated and the remaining processor assumes all duties. The Hot Spare Boot function is discussed in more detail in chapter 8.

3.2.2 BUS/PROCESSING SPEED CONFIGURATION

The system board includes a six-position DIP switch (SW1) that is used to select the Host bus frequency and the processing frequency of the system. Switch SW1-2 selects the host bus frequency while positions 3 through 6 determine the bus-to-core frequency ratio, i.e., the processing speed. Table 3-1 shows the possible switch configurations and their respective results.

Table 3-1.
Bus/Core Speed Switch (SW1) Settings

DIP SW1 Settings [1]					Bus/Core	Bus/Core
2	3	4	5	6	Ratio	Speed (in MHz)
Off	On	On	On	On	2/4 (1/2)	60/120
Off	On	On	On	Off	2/5	60/150
Off	On	On	Off	On	2/6 (1/3)	60/180
Off	On	On	Off	Off	2/7	60/210
Off	On	Off	On	On	2/8 (1/4)	60/240
Off	On	Off	On	Off	2/9	60/270
Off	On	Off	Off	On	2/10 (1/5)	60/300
Off	On	Off	Off	Off	2/11	60/330
On	On	On	On	On	2/4 (1/2)	66/133
On	On	On	On	Off	2/5	66/167
On	On	On	Off	On	2/6 (1/3)	66/200 [2]
On	On	On	Off	Off	2/7	66/233
On	On	Off	On	On	2/8 (1/4)	66/266
On	On	Off	On	Off	2/9	66/300
On	On	Off	Off	On	2/10 (1/5)	66/333
On	On	Off	Off	Off	2/11	66/366

NOTES:
[1] Off = open or logic “1” signal, On = closed or logic “0” signal
[2] Default setting

The status of switch positions 3 through 6 is software-readable through the GPIO port 79h using the serial scan chain read procedure (refer to chapter 8). Table 3-2 shows the switch position-to-serial scan chain (SSC) data format.

Table 3-2.
Bus/Core Speed Switch (SW1) SSC Data Format

Switch Position	Signal Name	SSC Byte 2
S3	CFG NMI	bit <4>
S4	CFG A20M	bit <5>
S5	CFG IGNNE	bit <6>
S6	CFG INTR	bit <7>

3.3 SYSTEM MEMORY

This system uses the 82441 for controlling eight banks of system memory. The 82441 drives the address lines while the data transfers are handled by the 82442 data bus buffer.

The DIMM sockets can be populated with 16-, 32-, 64-, or 128-MB modules in any combination. The standard configuration uses 60-ns modules. This system **does not** support dynamic bank timing.

Typical Host memory read performance for the Pentium-based system is shown in Table 3-3.

Table 3-3.
Host Memory Performance
w/60 ns EDO DIMMs @ 60-/66-MHz

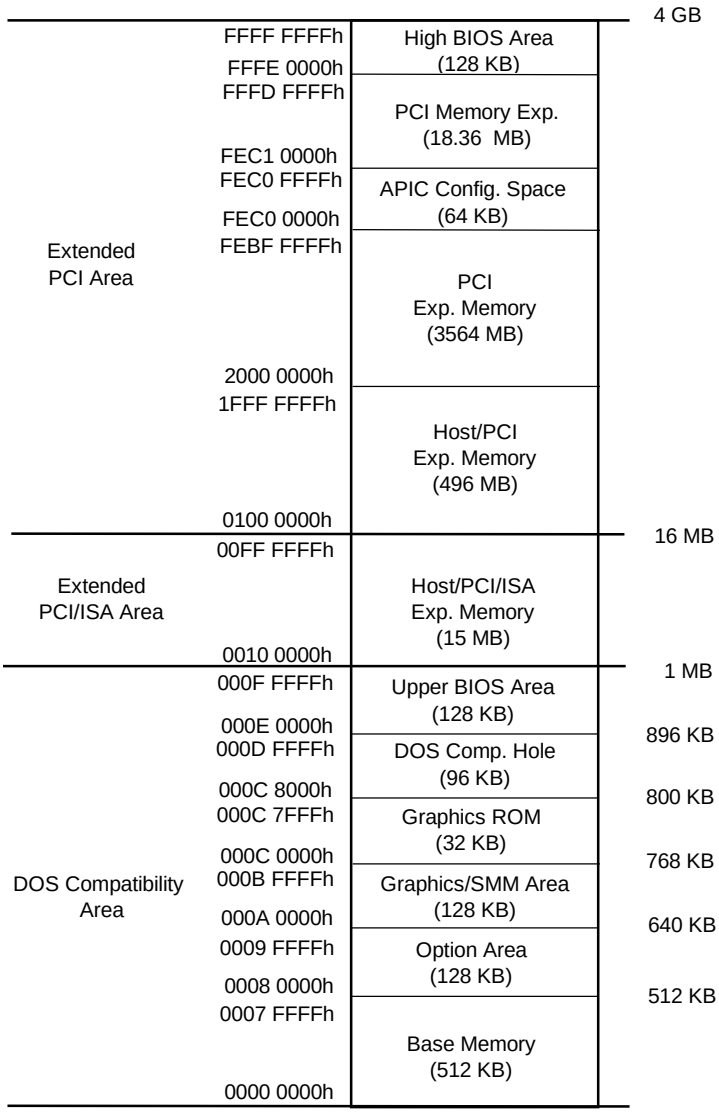
Action	<= 2 Banks/Rows	> 2 Banks/Rows
Read/Write Initial	11-2-2-2	12-3-3-3
Read/Write Row Miss	12-2-2-2	13-3-3-3
Read/Write Page Miss	14-2-2-2	14-3-3-3
Read/Write Page Hit	8-2-2-2	9-3-3-3

NOTE:
Each DIMM socket supports two banks, two rows.

Either EDO or burst EDO (BEDO) DRAM modules can be used. During POST, the BIOS checks the memory module type and speed using the Serial Presence Detect (SPD) method and configures the appropriate register (55h-58h) in the PMC's PCI Configuration Space.

> **NOTE:** This system uses unbuffered ECC DIMMs. The RAS and CAS signals drive the DIMMs directly. The MWE and remaining address signals are buffered **on the system board**. The required unbuffered DIMMs use different mechanical keying than buffered DIMMs.

The memory map for the system is shown in Figure 3-3 and includes areas of variable usage. The 128-KB Option Area can be mapped as a DOS region or for PCI purposes. The 128-KB graphics/SMM area is mapped as PCI space in normal operation and is also used when the system is in system management mode (SMM). The next twelve 16-KB blocks and the BIOS areas can have four possible attributes: read only (from DRAM for reads, to PCI for writes), write only (to DRAM for writes, from PCI for reads), read/write (all DRAM accesses), and disabled (all PCI accesses). ROM shadowing is accomplished by first setting the appropriate area to write-only. A read access will then obtain the data from the ROM. Next, a write to the same address will result in the data being written into DRAM. After the copy function is complete, the attributes of the appropriate area can be set to read-only or read-write. The ROM can be un-shadowed by resetting the attributes to write-only.



NOTE: Non-cacheable memory includes PCI memory and all memory above the first 2 GB.

Figure 3–3. System Memory Map

3.3.1 SUBSYSTEM CONFIGURATION

A number of parameters involving the L2 cache and system memory are configurable through PCI configuration registers of the 82441 (PMC). The PCI configuration registers listed in Table 3-4 are typically setup by BIOS at power-up but re-configurable by software.

Table 3-4.
82441 PCI Configuration Registers

PCI Config. Addr.	Register	Resert Value	PCI Config. Addr.	Register	
00, 01h	Vender ID	8086h	54h	Auxiliary Control	00h
02, 03h	Device ID	1237h	55, 56h	DRAM Row Type	0000h
04, 05h	PCI Command	0006h	57h	DRAM Control	01h
06, 07h	PCI Status	0280h	58h	DRAM Timing	10h
08h	Revision ID	00h	59-5Fh	Programmable Attr. Map	00h
0Ah	Sub-class Code	00h	60-67h	DRAM Row Bpoundary	01h
0Bh	Base Class Code	06h	68h	Fixed DRAM Hole Cntrl.	00h
0Dh	Latency Timer	00h	70h	Multi-Transaction Timer	00h
0Eh	Header	00h	71h	CPU Latency Timer	0Fh
0Fh	BIST Register	00h	72h	SMRAM Control	02h
50, 51h	PMC Configuration	4x00h	90h	Error-Command	00h
52h	Deturbo Counter Control	00h	91, 92h	Error-Status	0000h
53h	DBX Buffer Control	80h	93h	Turbo Reset Control	00h

NOTE:
Assume unmarked locations are reserved.

For more information on PCI configuration register access refer to Chapter 4, “System Support.”

Chapter 4
SYSTEM SUPPORT

4.1 INTRODUCTION

This chapter covers subjects dealing with basic system architecture and covers the following topics:

This chapter covers functions provided by off-the-shelf chipsets and therefore describes only basic aspects of these functions as well as information unique to the Compaq Professional Workstation. For detailed information on specific components, refer to the applicable manufacturer's documentation.

4.2 PCI BUS OVERVIEW

NOTE: This section describes the PCI bus in general and highlights bus implementation in this particular system. For detailed information regarding PCI bus operation, refer to the *PCI Local Bus Specification Revision 2.1*.

The 32-bit PCI bus uses a shared address/data bus design. On the first clock cycle of a PCI bus transaction the bus carries address information. On subsequent cycles, the bus carries data. PCI transactions occur synchronously with the Host bus at a rate of up to 33 MHz, depending on the speed of the microprocessor used. All I/O transactions involve the PCI bus. All ISA transactions involving the microprocessor, cache, and memory also involve the PCI bus. Memory cycles will involve the PCI if the access is initiated by a device or subsystem other than the microprocessor.

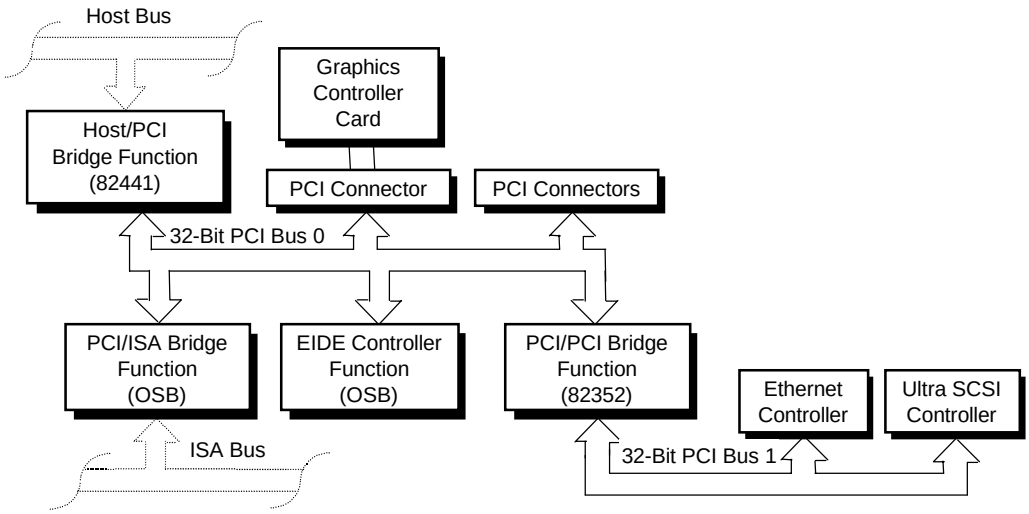


Figure 4–1. PCI Bus Devices and Functions

4.2.1 PCI SLOT DESCRIPTIONS

Slot 1 Standard PCI 5-volt 32-bit connector with all common PCI signals and slot-specific signals including REQ0- and GNT0-. Configured as PCI Device # 2.

Slot 2 Standard PCI 5-volt 32-bit connector with all common PCI signals and slot-specific signals including REQ1- and GNT1-. Configured as PCI Device # 3.

Slot 3 Standard PCI 5-volt 32-bit connector with all common PCI signals and slot-specific signals including REQ2- and GNT2-. Configured as PCI Device # 4.

4.2.2 PCI CONNECTOR

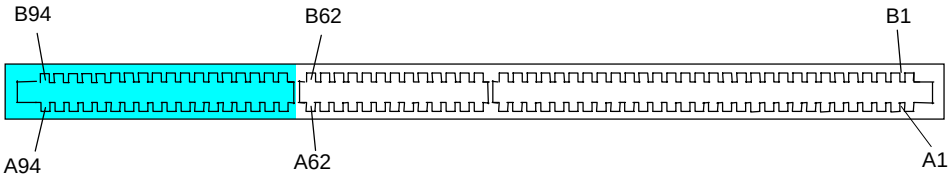


Figure 4–2. PCI Bus Connector (5V Type)

Table 4-1.
PCI Bus Connector Pinout

Pin	B Signal	A Signal	Pin	B Signal	A Signal	Pin	B Signal	A Signal
01	-12 VDC	TRST-	32	AD17	AD16	63	Reserved	GND
02	TCK	+12 VDC	33	C/BE2-	+3.3 VDC	64	GND	C/BE7-
03	GND	TMS	34	GND	FRAME-	65	C/BE6-	C/BE5-
04	TDO	TDI	35	IRDY-	GND	66	C/BE4-	+5 VDC
05	+5 VDC	+5 VDC	36	+3.3 VDC	TRDY-	67	GND	PAR64
06	+5 VDC	INTA-	37	DEVSEL-	GND	68	AD63	AD62
07	INTB-	INTC-	38	GND	STOP-	69	AD61	GND
08	INTD-	+5 VDC	39	LOCK-	+3.3 VDC	70	+5 VDC	AD60
09	PRSNT1-	Reserved	40	PERR-	SDONE	71	AD59	AD58
10	RSVD	+5 VDC	41	+3.3 VDC	SBO-	72	AD57	GND
11	PRSNT2-	Reserved	42	SERR-	GND	73	GND	AD56
12	GND	GND	43	+3.3 VDC	PAR	74	AD55	AD54
13	GND	GND	44	C/BE1-	AD15	75	AD53	+5 VDC
14	RSVD	Reserved	45	AD14	+3.3 VDC	76	GND	AD52
15	GND	RST-	46	GND	AD13	77	AD51	AD50
16	CLK	+5 VDC	47	AD12	AD11	78	AD49	GND
17	GND	GNT-	48	AD10	GND	79	+5 VDC	AD48
18	REQ-	GND	49	GND	AD09	80	AD47	AD46
19	+5 VDC	Reserved	50	Key	Key	81	AD45	GND
20	AD31	AD30	51	Key	Key	82	GND	AD44
21	AD29	+3.3 VDC	52	AD08	C/BE0-	83	AD43	AD42
22	GND	AD28	53	AD07	+3.3 VDC	84	AD41	+5 VDC
23	AD27	AD26	54	+3.3 VDC	AD06	85	GND	AD40
24	AD25	GND	55	AD05	AD04	86	AD39	AD38
25	+3.3 VDC	AD24	56	AD03	GND	87	AD37	GND
26	C/BE3-	IDSEL	57	GND	AD02	88	+5 VDC	AD36
27	AD23	+3.3 VDC	58	AD01	AD00	89	AD35	AD34
28	GND	AD22	59	+5 VDC	+5 VDC	90	AD33	GND
29	AD21	AD20	60	ACK64-	REQ64-	91	GND	AD32
30	AD19	GND	61	+5 VDC	+5 VDC	92	Reserved	Reserved
31	+3.3 VDC	AD18	62	+5 VDC	+5 VDC	93	Reserved	GND
--	--	--	--	--	--	94	GND	Reserved

64-bit extension not present in this system.

4.2.3 PCI BUS MASTER ARBITRATION

The PCI bus uses a bus master/target arbitration scheme. A bus master is a device that has been granted control of the bus for the purpose of initiating a transaction. A target is a device that is the recipient of a transaction. Request (REQ), Grant (GNT), and FRAME signals are used by PCI bus masters for gaining access to the PCI bus. When a PCI device needs access to the PCI bus (and does not already own it), the PCI device asserts it's REQ*n* signal to the PCI bus arbiter (a function of the system controller component). If the bus is available, the arbiter asserts the GNT*n* signal to the requesting device, which then asserts FRAME and conducts the address phase of the transaction with a target. If the PCI device already owns the bus, a request is not needed and the device can simply assert FRAME and conduct the transaction. Table 4-1 shows the grant and request signals assignments for the devices on the PCI bus.

Table 4-2.
PCI Bus Mastering Devices

PCI Device	PCI Bus #	REQ/GNT Line
PCI/ISA Bridge (OSB)	0	PHOLD-/PHLDA-
PCI/PCI Bridge (82352)	0	P2PREQ-/P2PGNT-
PCI Connector Slot 1	0	REQ0-/GNT0-
PCI Connector Slot 2	0	REQ1-/GNT1-
PCI Connector Slot 3	0	REQ2-/GNT2-
Network Interface Controller	1	REQ4-/GNT4-
SCSI Controller	1	REQ5-/GNT5-

PCI bus control is granted according to a Least Recently Used (LRU) algorithm. During times that the bus is not used or requested, bus control is given to the Host/PCI bridge. After a device has given up control of the bus or has not executed a transaction for 16 PCI clock cycles (PCICLKs) after gaining bus control, it loses access and is placed on the bottom of the priority list.

The PCI/ISA bridge is given special consideration. If the PCI/ISA bridge gains control of the PCI bus but does not execute a transaction after 16 PCICLKs, the PCI/ISA bridge retains ownership of the PCI bus until the current ISA bus master relinquishes the ISA bus. The PCI/ISA bridge is then placed on the bottom of the priority list.

PCI bus priority can be altered in two ways: by a master needing to perform a retry of a data cycle, or by the master locking the bus. When a master is retried, it releases the bus and negates its REQ*n*- line for a minimum of two PCICLKs and then requests the bus again. If the master is granted the bus before the condition that caused the retry is resolved, the master is retried again, which may result in bus "thrashing." Bus thrashing is minimized by masking the REQ*n*- line of a particular device that has had a transaction retried.

If a master locks the PCI bus, it retains top priority, allowing it to quickly finish a lock sequence. The PCI/ISA bridge cannot become master until the locking device unlocks the bus. Consequently, a master should not lock the bus for long periods of time or latency problems could occur.

4.2.4 PCI BUS TRANSACTIONS

The PCI bus consists of a 32-bit path (AD31-00 lines) that uses a multiplexed scheme for handling both address and data transfers. A bus transaction consists of an address cycle and one or more data cycles, with each cycle requiring a clock (PCICLK) cycle. High performance is realized during burst modes in which a transaction with contiguous memory locations requires that only one address cycle be conducted and subsequent data cycles are completed using auto-incremented addressing. Four types of address cycles can take place on the PCI bus; I/O, memory, configuration, and special. Address decoding is distributed (left up to each device on the PCI bus).

Two types of address decoding are allowed on the PCI bus; positive and subtractive. Positive decoding provides higher performance because PCI devices respond immediately to an address within a certain range. For this system, the Host/PCI bridge and any devices installed in the PCI expansion slots use positive decoding. The PCI/ISA bridge uses positive decoding for all functions except accesses to DMA register space and memory accesses below 16-MB that are claimed by a PCI device.

4.2.4.1 I/O and Memory Cycles

For I/O and memory cycles, a standard 32-bit address decode (AD31..0) for byte-level addressing is handled by the appropriate PCI device. For memory addressing, PCI devices decode the AD31..2 lines for dword-level addressing and check the AD1,0 lines for burst (linear-incrementing) mode. In burst mode, subsequent data phases are conducted a dword at a time with addressing assumed to increment accordingly (four bytes at a time).

4.2.4.2 Configuration Cycles

Devices on the PCI bus must comply with PCI protocol that allows configuration of that device by software. In this system, configuration mechanism #1 (as described in the PCI Local Bus specification Rev. 2.1) is employed. This method uses two 32-bit registers for initiating a configuration cycle for accessing the configuration space of a PCI device. The configuration address register (CONFIG_ADDRESS) at 0CF8h holds a value that specifies the PCI bus, PCI device, and specific register to be accessed. The configuration data register (CONFIG_DATA) at 0CFCh contains the configuration data.

PCI Configuration Address Register
I/O Port 0CF8h, R/W access (32-bit only)

Bit	Function
31	Configuration Enable 0 = Disabled 1 = Enable
30..24	Reserved - read/write 0s
23..16	Bus Number. Selects PCI bus
15..11	PCI Device Number. Selects PCI device for access
10..8	Function Number. Selects function of selected PCI device.
7..2	Register Index. Specifies config. reg.
1,0	Configuration Cycle Type ID. 00 = Type 0 01 = Type 1

PCI Configuration Data Register
I/O Port 0CFCh, R/W access (8-, 16-, 32-bit)

Bit	Function
31..0	Configuration Data.

Figure 4-3 shows how the loading of 0CF8h results in a Type 0 configuration cycle on the PCI bus. The Device Number (bits <15..11> determines which one of the AD31..11 lines is to be asserted high for the IDSEL signal, which acts as a "chip select" function for the PCI device to be configured.

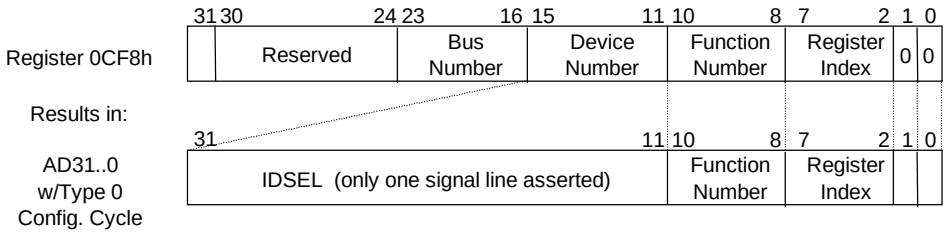


Figure 4–3. Type 0 Configuration Cycle

Type 0 configuration cycles are used for configuring devices on PCI bus # 0. Type 1 configuration cycles (reg. 0CF8h bits <1,0> = 01b) are passed on to PCI bus # 1. Table 4-3 shows the device numbers and IDSEL connections for the PCI devices.

Table 4-3.
PCI Device Configuration Access

PCI Device	PCI Bus #	Device No. (CF8h <15..11>)	IDSEL Wired to:
Support Chipset:			
PMC (82441)	0	0	AD11
OSB	0	20	AD31
PCI Connector (slot 1)	0	11	AD22
PCI Connector (slot 2)	0	10	AD21
PCI Connector (slot 3)	0	9	AD20
PCI Connector (slot 4)	0	8	AD19
PCI/PCI Bridge (82352)	0	6	AD17
Firewire I/F	1	9	AD25
USB I/F	1	10	AD26
Ethernet Controller	1	11	AD27
SCSI Controller	1	12	AD28

The function number (CF8h, bits <10..8>) is used to select a particular function within a multifunction PCI device as shown in Table 4-4.

Table 4-4.
PCI Function Configuration Access

PCI Function	Device No.	Function No.
Host/PCI Bridge (82411)	0	0
PCI/ISA Bridge (OSB)	20	0
EIDE Interface (OSB)	20	1

The register index identifies the 32-bit location within the configuration space of the PCI device to be accessed. All PCI devices can contain up to 256 bytes of configuration data (see Figure 4-4), of which the first 64 bytes comprise the configuration space header.

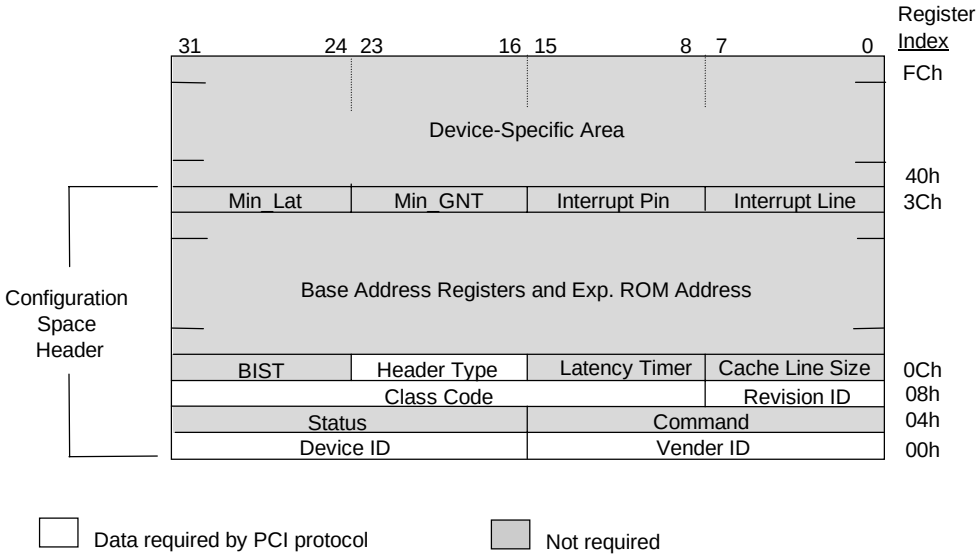


Figure 4–4. PCI Configuration Space Map

Each PCI device is identified with a vender ID (assigned to the vender by the PCI Special Interest Group) and a device ID (assigned by the vender). The device and vender IDs for the devices used in these systems are listed in Table 4-5.

Table 4-5.
PCI Device Identification

PCI Device	Vender ID	Device ID
Support Chipset:		
PMC	8086h	1237h
OSB	0E11h	AE33h
PCI/PCI Bridge (82352)	8086h	na
Ethernet Controller	0E11h [1]	AE35h [1]
SCSI Controller	na	na

NOTE:
[1] Texas Instruments component, but uses Compaq ID numbers.

4.2.4.3 Special Cycles

There are two types of special cycles that may occur on the PCI bus. The first type iS initiated by the host and is used to perform the following functions: Shutdown, Flush, Halt, Write Back, Flush Acknowledge, Branch Trace Message, and Stop/Grant. These cycles start like all other PCI cycles and terminate with a master abort.

The second type of special cycle is initiated by writing to 0CF8h, Bus # = all 0s, Device = all 1s, Function # all 1s, and Register = all 0s) and 0CFCh to generate a Type 0 configuration cycle. This type 0 cycle, however, does not assert any of the IDSEL lines and therefore results in a master abort with FFFFh returned to the microprocessor.

4.2.5 OPTION ROM MAPPING

During POST, the PCI bus is scanned for devices that contain their own specific firmware in ROM. Such option ROM data, if detected, is loaded into system memory's DOS compatibility area (refer to the system memory map shown in chapter 3).

4.2.6 PCI CONFIGURATION

PCI bus operations, especially those that involve ISA bus interaction, require the configuration of certain parameters such as PCI IRQ routing, top of memory accessable by ISA, SMI generation, and clock throttling characteristics. These parameters are handled by the PCI/ISA bridge function (PCI function #0) of the OSB ASIC and configured through the PCI configuration space registers listed in Table 4-6. Configuration is provided by BIOS at power-up but re-configurable by software .

Table 4-6.
PCI/ISA Bridge Configuration Registers (OSB ASIC)

PCI Config. Addr.	Register	PCI Config. Addr.	Register
00, 01h	Vender ID	4C, 4Dh	PCI/ISA Hole #3
02, 03h	Device ID	4E, 4Fh	PCI/ISA Hole #4
04, 05h	Command	52, 53h	Top of Main Memory
06, 07h	Status	54, 55h	Cut MEMCS- Attri. Reg.
08h	Revision ID	58-5Bh	PERR- Address Register
09-0Bh	Class Code	5Ch	PERR- Command Register
0Eh	Header Type	60, 61h	PCI/ISA Hole Top #1
40h	PCI Control	62, 63h	PCI/ISA Hole Top #2
41h	PCI Misc. Function	64, 65h	PCI/ISA Hole Top #3
42h	Cut MEMCS- Cntrl.	66, 67h	PCI/ISA Hole Top #4
44, 45h	PCI/ISA Hole #1 (PCI/ISA map)	68h	Refresh Count Value
46, 47h	PCI/ISA Hole #2	69h	Min. Grant #2 and 3 (PCI slots 2, 3)
48h	ISA Addr. Dec. #1 (DMA map)	6Ah	Min. Grant #4 (PCI slot 4)
49h	ISA Addr. Dec. #2 (DCH map)	6Bh	AMD NICFIX gnt_[3..0] proc
4A, 4Bh	Min. Grant (CPU, EDMA, slot 1)	6C-6Fh	Test Mode Enable

NOTE: Assume unmarked locations/gaps as reserved.

4.3 ISA BUS OVERVIEW

NOTE: This section describes the ISA bus in general and highlights bus implementation in this particular system. For detailed information regarding ISA bus operation, refer to the *Compaq Extended Industry Standard Architecture (EISA) Technical Reference Guide.*

The industry standard architecture (ISA) bus provides an 8-/16-bit path for standard I/O peripherals as well as for optional devices that can be installed in the ISA expansion slots. Figure 4-5 shows the key functions and devices that reside on the ISA bus.

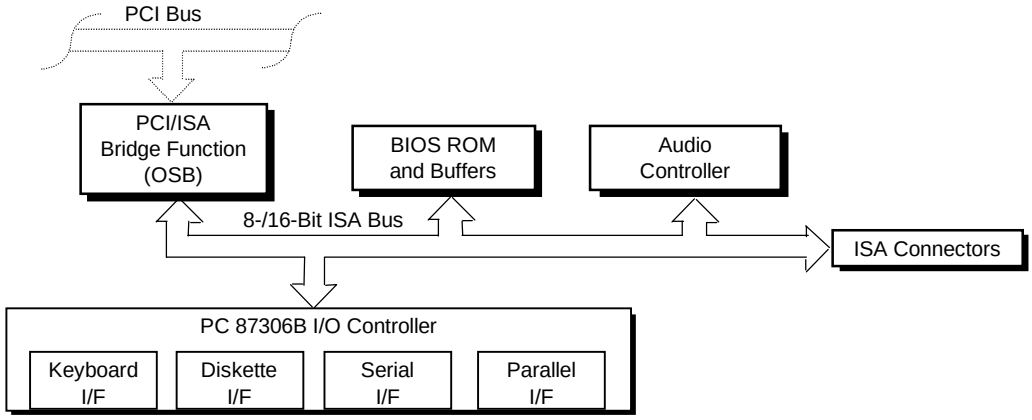


Figure 4–5. Compaq Deskpro 4000/6000 Series ISA Bus Devices and Functions

4.3.1 ISA SLOT DESCRIPTIONS

Slot 1 Standard 16-bit ISA connector with all common ISA signals.

Slot 2 Standard 16-bit ISA connector with all common ISA signals.

Slot 3 Standard 16-bit ISA connector with all common ISA signals.

4.3.2 ISA CONNECTOR

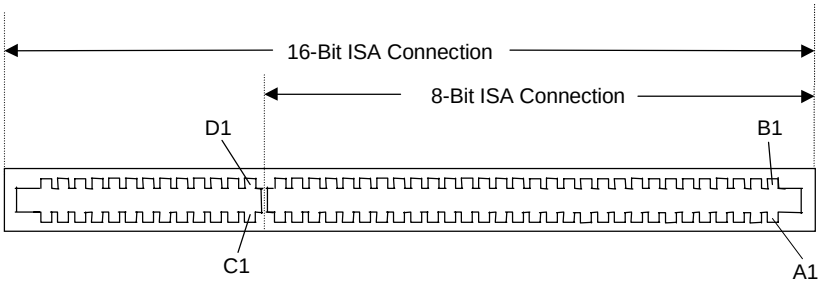


Figure 4–6. ISA Expansion Connector

Table 4-7.
ISA Expansion Connector Pinout

8-Bit ISA Interface				16-Bit ISA Interface			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
B01	GND	A01	I/O CHK-	D01	M16-	C01	SBHE-
B02	RESDRV	A02	SD7	D02	I/O16-	C02	LA23
B03	+5 VDC	A03	SD6	D03	IRQ10	C03	LA22
B04	IRQ9	A04	SD5	D04	IRQ11	C04	LA21
B05	-5 VDC	A05	SD4	D05	IRQ12	C05	LA20
B06	DRQ2	A06	SD3	D06	IRQ15	C06	LA19
B07	-12 VDC	A07	SD2	D07	IRQ14	C07	LA18
B08	NOWS-	A08	SD1	D08	DAK0-	C08	LA17
B09	+12 VDC	A09	SD0	D09	DRQ0	C09	MRDC-
B10	GND	A10	BUSRDY	D10	DAK5-	C10	MWTC-
B11	SMWTC-	A11	DMA	D11	DRQ5	C11	SD8
B12	SMRDC-	A12	SA19	D12	DAK6-	C12	SD9
B13	IOWC-	A13	SA18	D13	DRQ6	C13	SD10
B14	IORC-	A14	SA17	D14	DAK7-	C14	SD11
B15	DAK3-	A15	SA16	D15	DRQ7	C15	SD12
B16	DRQ3	A16	SA15	D16	+5 VDC	C16	SD13
B17	DAK1	A17	SA14	D17	GRAB-	C17	SD14
B18	DRQ1	A18	SA13	D18	GND	C18	SD15
B19	REFRESH-	A19	SA12				
B20	BCLK	A20	SA11				
B21	IRQ7	A21	SA10				
B22	IRQ6	A22	SA9				
B23	IRQ5	A23	SA8				
B24	IRQ4	A24	SA7				
B25	IRQ3	A25	SA6				
B26	DAK2-	A26	SA5				
B27	T-C	A27	SA4				
B28	BALE	A28	SA3				
B29	+5 VDC	A29	SA2				
B30	OSC	A30	SA1				
B31	GND	A31	SA0				

4.3.3 ISA BUS OPERATION

The ISA bus supports 8- and 16-bit transfers at an 8-MHz rate. Devices limited to 8-bit transfers use the lower byte portion (data lines 7..0) while 16-bit transfers use the full bandwidth (data lines 15..0). Addressing is handled by two classifications of address signals: latched and latchable. Latched address signals (SA19..0) select the specific byte within the 1-MB section of memory defined by address lines LA23..17. Latchable address lines (LA23..17) provide a longer setup time for pre-chip selection or for pre-address decoding for high-speed memory and allow access to up to 16-MB of physical memory on the ISA bus. The SA19..17 signals have the same values as the LA19..17 signals for all memory cycles. The I/O cycles use only the SA15..0 signals.

The key control signals are described as follows:

- MRDC- (Memory Read Cycle): MRDC- is active on all ISA memory reads accessing memory from 000000h to FFFFFFh.
- SMEMR- (System Memory Read): SMEMR- is asserted by the PCI/ISA bridge to request an ISA memory device to drive data onto the data lines for accesses below one megabyte. SMEMR- is a delayed version of MRDC-.
- MWTC- (Memory Write Cycle): MWTC- is active on all ISA memory write cycles accessing memory from 000000h to FFFFFFh.
- SMEMW- (System Memory Write): SMEMW- is asserted by the PCI/ISA bridge to request an ISA memory device to accept data from the data lines for access below one megabyte. SMEMW- is a delayed version of MWTC-.
- IORC- (Input/Output Read Cycle): IORC- commands an ISA I/O device to drive data onto the data lines.
- IOWC- (Input/Output Write Cycle): IOWC- commands an ISA I/O device to accept data from the data lines.
- SBHE- (System Byte High Enable): SBHE- indicates that a byte is being transferred on the upper half (D15..8) of the data lines.
- SA0- (System Address Bit <0>): This bit is the complement of SBHE- and indicates that a byte is being transferred on the lower half (D7..0) of the data lines.
- M16- (16-bit Memory Cycle): M16- is asserted by 16-bit ISA devices to indicate 16-bit memory cycle capability.
- IO16- (16-bit I/O Cycle): IO16- is asserted by 16-bit ISA devices to indicate 16-bit I/O cycle transfer capability.

If the address on the SA lines is above one megabyte, SMRDC- and SMWTC- will not be active. The MRDC- and MWTC- signals are active for memory accesses up to 16 megabytes and can be used by any device that uses the full 16-bit ISA bus. To request a 16-bit transfer, a device asserts either the M16- (memory) or IO16- (I/O) signal when the device is addressed.

When another device (such as a DMA device or another bus master) takes control of the ISA, the Bus Address Latch Enable (BALE) signal is held active for the duration of the operation. As a result , signals LA23..17 are always enabled and must be held stable for the duration of each bus cycle.

When the address changes, devices on the bus may decode the latchable address (LA23..17) lines and then latch them. This arrangement allows devices to decode chip selects and M16- before the next cycle actually begins.

The following guidelines apply to optional ISA devices installed in the system:

- On bus lines that can be driven by a controller board, the driver should be able to sink a minimum of 20 ma at 0.5 VDC and source 2 ma at 3.75 VDC.
- On bus lines that are driven in the low direction only (open collector), the driver should be able to sink 20 ma at 0.5 VDC.
- The load on any logic line from a single bus slot should not exceed 2.0 ma in the low state (at 0.5 VDC) or 0.1 ma in the high state (at 3.75 VDC).
- The logic-high voltage at the bus ranges from 3.75 VDC to 5.5 VDC. The logic low voltage ranges from 0 VDC to 0.8 VDC.

4.3.4 ISA CONFIGURATION

The working relationship between the PCI and ISA buses requires that certain parameters be configured. The PC/ISA bridge function of the OSB or 82371 includes configuration registers to set parameters such as PCI IRQ routing and top-of-memory available to ISA/DMA devices. These parameters are programmed by BIOS during power-up, using registers listed previously in Table 4-6.

4.4 DIRECT MEMORY ACCESS

Direct Memory Access (DMA) is a method by which an ISA device accesses system memory without involving the microprocessor. DMA is normally used to transfer blocks of data to or from an ISA I/O device. DMA reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks.

> **NOTE:** This section describes DMA in general. For detailed information regarding DMA operation, refer to the *Compaq Extended Industry Standard Architecture (EISA) Technical Reference Guide.* Note, however, that EISA enhancements as described in the referenced document are not supported in this (ISA only) system.

The OSB and 82371 components include the equivalent of two 8237 DMA controllers cascaded together to provide eight DMA channels. Table 4-8 lists the default configuration of the DMA channels.

Table 4-8.
Default DMA Channel Assignments

DMA Channel	Device ID
Controller 1 (byte transfers)	
0	Spare & ISA conn. pins D8, D9
1	Audio subsystem & ISA conn. pins B17, B18
2	Diskette drive & ISA conn. pins B6, B26
3	ECP LPT1 & ISA conn. pins B15, B16
Controller 2 (word transfers)	
4	Cascade for controller 1
5	Spare & ISA conn. pins D10, D11
6	Spare & ISA conn. pins D12, D13
7	Spare & ISA conn. pins. D14, D15

All channels in DMA controller 1 operate at a higher priority than those in controller 2. Note that channel 4 is not available for use other than its cascading function for controller 1. The DMA controller 2 can transfer words only on an even address boundary. The DMA controller and page register define a 24-bit address that allows data transfers within the address space of the CPU. The DMA controllers operate at 8 MHz.

4.4.1 DMA CONTROLLER ACCESS

The DMA logic is accessed through two types of I/O mapped registers; page registers and controller registers. The mapping is the same regardless of the support chipset used.

4.4.1.1 Page Registers

The DMA page register contains the eight most significant bits of the 24-bit address and works in conjunction with the DMA controllers to define the complete (24-bit)address for the DMA channels. Table 4-9 lists the page register port addresses.

Table 4-9.
DMA Page Register Addresses

DMA Channel	Page Register I/O Port
Controller 1 (byte transfers)	
Ch 0	087h
Ch 1	083h
Ch 2	081h
Ch 3	082h
Controller 2 (word transfers)	
Ch 4	n/a
Ch 5	08Bh
Ch 6	089h
Ch 7	08Ah
Refresh	08Fh [see note]

NOTE:
The DMA memory page register for the refresh channel must be programmed with 00h for proper operation.

The memory address is derived as follows:

24-Bit Address - Controller 1 (Byte Transfers)

8-Bit Page Register	8-Bit DMA Controller
A23..A16	A15..A00

24-Bit Address - Controller 2 (Word Transfers)

8-Bit Page Register	16-Bit DMA Controller
A23..A17	A16..A01, (A00 = 0)

Note that address line A16 from the DMA memory page register is disabled when DMA controller 2 is selected. Address line A00 is not connected to DMA controller 2 and is always 0 when word-length transfers are selected.

By not connecting A00, the following applies:

- The size of the the block of data that can be moved or addressed is measured in 16-bits (words) rather than 8-bits (bytes).
- The words must always be addressed on an even boundary.

DMA controller 1 can move up to 64 Kbytes of data per DMA transfer. DMA controller 2 can move up to 64 Kwords (128 Kbytes) of data per DMA transfer. Word DMA operations are only possible between 16-bit memory and 16-bit peripherals.

The RAM refresh is designed to perform a memory read cycle on each of the 512 row addresses in the DRAM memory space. Refresh operations are used to refresh memory on the 32-bit memory bus and the ISA bus. The refresh address is provided on lines SA00 through SA08. Address lines LA23..17, SA18,19 are driven low.

The remaining address lines are in an undefined state during the refresh cycle. The refresh operations are driven by a 69.799-KHz clock generated by Interval Timer 1, Counter 1. The refresh rate is 128 refresh cycles in 2.038 ms.

4.4.1.2 DMA Controller Registers

Table 4-10 lists the DMA Controller Registers and their I/O port addresses. Note that there is a set of registers for each DMA controller.

Table 4-10.
DMA Controller Registers

Register	Controller 1	Controller 2	R/W
Status	008h	0D0h	R
Command	008h	0D0h	W
Mode	00Bh	0D6h	W
Write Single Mask Bit	00Ah	0D4h	W
Write All Mask Bits	00Fh	0DEh	W
Software DRQx Request	009h	0D2h	W
Base and Current Address - Ch 0	000h	0C0h	W
Current Address - Ch 0	000h	0C0h	R
Base and Current Word Count - Ch 0	001h	0C2h	W
Current Word Count - Ch 0	001h	0C2h	R
Base and Current Address - Ch 1	002h	0C4h	W
Current Address - Ch 1	002h	0C4h	R
Base and Current Word Count - Ch 1	003h	0C6h	W
Current Word Count - Ch 1	003h	0C6h	R
Base and Current Address - Ch 2	004h	0C8h	W
Current Address - Ch 2	004h	0C8h	R
Base and Current Word Count - Ch 2	005h	0CAh	W
Current Word Count - Ch 2	005h	0CAh	R
Base and Current Address - Ch 3	006h	0CCh	W
Current Address - Ch 3	006h	0CCh	R
Base and Current Word Count - Ch 3	007h	0CEh	W
Current Word Count - Ch 3	007h	0CEh	R
Temporary (Command)	00Dh	0DAh	R
Reset Pointer Flip-Flop (Command)	00Ch	0D8h	W
Master Reset (Command)	00Dh	0DAh	W
Reset Mask Register (Command)	00Eh	0DCh	W

NOTE:
For a detailed description of the DMA registers, refer to the *Compaq EISA Technical Reference Guide*.

4.5 INTERRUPTS

The microprocessor uses two types of interrupts; maskable and nonmaskable. A maskable interrupt can be enabled or disabled within the microprocessor by the use of the STI and CLI instructions. A nonmaskable interrupt cannot be masked off within the microprocessor but may be inhibited by hardware or software means external to the microprocessor.

4.5.1 MASKABLE INTERRUPTS

The maskable interrupt is a hardware-generated signal used by peripheral functions within the system to get the attention of the microprocessor. Peripheral functions produce a unique INTA-D (PCI) or IRQ0-15 (ISA) signal that is routed to interrupt processing logic that asserts the interrupt (INTR) input to the microprocessor. The microprocessor halts execution to determine the source of the interrupt and then services the peripheral as appropriate.

This system supports two modes of maskable interrupt processing:

- 8259-compatible mode (power-up default)
- APIC mode

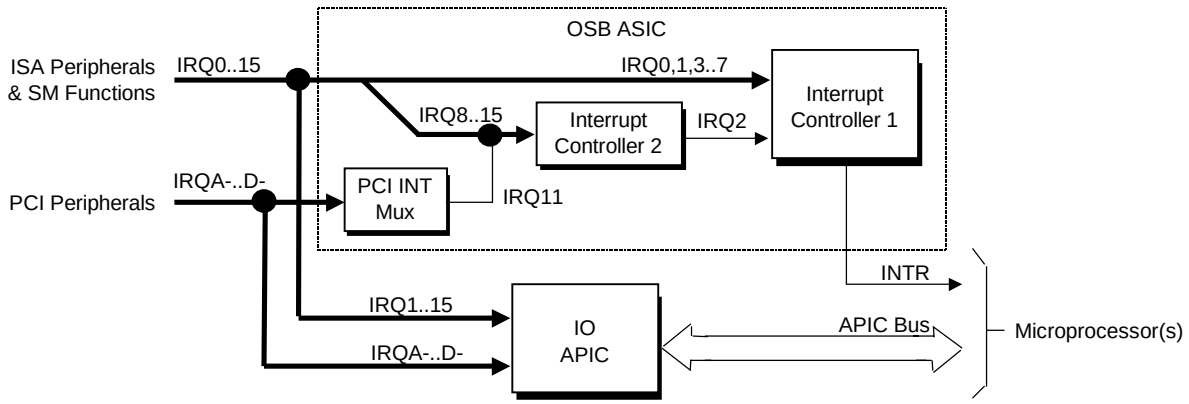


Figure 4–7. Interrupt Processing, Block Diagram

4.5.1.1 8259-Compatible Mode

During POST, the system enters the 8259-compatible mode where the OSB, which includes the equivalent of two 8259 interrupt controllers cascaded together, handles the standard AT-type (ISA) interrupt signals (IRQ0-15). The OSB also receives the PCI interrupt signals (IRQA- thru IRQD-) from PCI devices, and handles several system management interrupt sources as well. Table 4-11 lists the standard source configuration for maskable interrupts and their priorities. If more than one interrupt is pending, the highest priority (lowest number) is processed first.

Table 4-11.
Maskable Interrupt Priorities and Assignments

Priority	Signal Label	Source (Typical)	Notes
1	IRQ0	Interval timer 1, counter 0	
2	IRQ1	Keyboard	
3	IRQ8-	Real-time clock	
4	IRQ9	Spare and ISA connector pin B04	
5	IRQ10	Spare and ISA connector pin D03	
6	IRQ11	PCI interrupts and ISA connector pin D04	[1]
7	IRQ12	Mouse and ISA connector pin D05	
8	IRQ13	System management and Coprocessor (math)	[2]
9	IRQ14	IDE primary I/F and ISA connector pin D07	
10	IRQ15	IDE secondary I/F and ISA connector pin D06	
11	IRQ3	Serial port (COM2) and ISA connector pin B25	
12	IRQ4	Serial port (COM1) and ISA connector pin B24	
13	IRQ5	Audio subsystem and ISA connector pin B23	
14	IRQ6	Diskette drive controller and ISA connector pin B22	
15	IRQ7	Parallel port (LPT1)	[3]
--	IRQ2	NOT AVAILABLE (Cascade from interrupt controller 2)	

NOTES:

[1]

PCI Interrupt	Source
IRQA-	SCSI I/F, all PCI slots
IRQB-	All PCI slots
IRQC-	All PCI slots
IRQD-	Ethernet I/F, all PCI slots

[2] System management sources:

a. ECC error detection
b. Processor temperature threshold
c. Fan fault sense

[3] Alternate available interrupts: IRQ5, 9,10,11,14, or 15

Note that the PCI interrupts are funneled through IRQ11. Also, several system management functions are funneled through IRQ13.

In 8259-compatible mode, maskable Interrupt processing is controlled and monitored through standard AT-type I/O-mapped registers. These registers are listed in Table 4-12.

Table 4-12.
Maskable Interrupt Control Registers

I/O Port	Register
020h	Base Address, Int. Cntlr. 1
021h	Initialization Command Word 2-4, Int. Cntlr. 1
0A0h	Base Address, Int. Cntlr. 2
0A1h	Initialization Command Word 2-4, Int. Cntlr. 2

The initialization and operation of the interrupt control registers follows standard AT-type protocol.

PCI interrupt redirection in 8259-mode is handled by the OSB ASIC. Two I/O mapped registers are used to redirect the INTA-..INTD- signals to the IRQn signal lines. Register 0C00h selects the PCI interrupt to be redirected while register 0C01h determines which IRQn the INTx is to be directed to. The power up (default) configuration has PCI interrupt redirection disabled.

I/O Addr. 0C00h, PCI Interrupt Index
Default Value = 00h

Bit	Function
7..3	Reserved - read 0's
2..0	PCI Interrupt Select: 000 = Unused PCI interrupt 001 = Unused PCI interrupt 010 = EDMA2 (from IRQ14/IRQ15) 011 = Unused PCI interrupt 100 = INTA- 101 = INTB- 110 = INTC- 111 = INTD-

I/O Addr. 0C01h, PCI Interrupt Redirection Register
Default Value = 00h

Bit	Function	
7..4	Reserved - read 0's	
3..0	Interrupt Routing:	
	0000 = Disabled	1000 = Reserved
	0001 = IRQ1	1001 = IRQ9
	0010 = Reserved	1010 = IRQ10
	0011 = IRQ3	1011 = IRQ11
	0100 = IRQ4	1100 = IRQ12
	0101 = IRQ5	1101 = Reserved
	0110 = IRQ6	1110 = IRQ14
	0111 = IRQ7	1111 = IRQ15

Redirected PCI interrupts that can be generated as either edge or level-triggered require that I/O register 04D0h be set to correspond according to how the source of the PCI interrupt is set. Bits <15..1> of 04D0h correspond to IRQ's 15..1 respectively (1 = level triggered, 0 = edge triggered).

4.5.1.2 APIC Mode

The APIC mode is specifically intended for multi-processor systems that require distribution of inter-processor interrupts as well as those generated by PCI and ISA functions. In APIC mode the maskable interrupts are routed through the IOAPIC component, which communicates with the microprocessor's local APIC over a three-line APIC bus.

The IO APIC component contains a redirection register used during POST to map the PCI interrupts to specific IRQs. The general priority of interrupts IRQ0-15 remains the same in APIC mode as for 8259 mode.

4.5.2 NONMASKABLE INTERRUPTS

Nonmaskble interrupts cannot be masked (inhibited) within the microprocessor itself but may be maskable by software using logic external to the microprocessor. There are two nonmaskable interrupt signals: the NMI- and the SMI-. These signals have service priority over all maskable interrupts, with the SMI- having top priority over all interrupts including the NMI-.

4.5.2.1 NMI- Generation

The Non-Maskable Interrupt (NMI-) signal can be generated by one of the following actions:

- Parity errors detected on the ISA bus (activating IOCHK-).
- Parity errors detected on a PCI bus (activating SERR- or PERR-).
- Microprocessor internal error (activating IERRA or IERRB)

The IOCHK-, SERR-, and PERR- signals are routed through the OSB ASIC, which in turn activates the NMI to the microprocessor.

The NMI Status Register at I/O port 061h contains NMI source and status data as follows:

NMI Status Register 61h

Bit	Function
7	NMI Status: 0 = No NMI from system board parity error. 1 = NMI requested, read only
6	IOCHK- NMI: 0 = No NMI from IOCHK- 1 = IOCHK- is active (low), NMI requested, read only
5	Interval Timer 1, Counter 2 (Speaker) Status
4	Refresh Indicator (toggles with every refresh)
3	IOCHK- NMI Enable/Disable: 0 = NMI from IOCHK- enabled 1 = NMI from IOCHK- disabled and cleared (R/W)
2	System Board Parity Error (PERR/SERR) NMI Enable: 0 = Parity error NMI enabled 1 = Parity error NMI disabled and cleared (R/W)
1	Speaker Data (R/W)
0	Inteval Timer 1, Counter 2 Gate Signal (R/W) 0 = Counter 2 disabled 1 = Counter 2 enabled

Functions not related to NMI activity.

After the active NMI has been processed, status bits <7> or <6> are cleared by pulsing bits <2> or <3> respectively.

The NMI Enable Register (070h, <7>) is used to enable/disable the NMI signal. Writing 80h to this register masks generation of the NMI-. Note that the lower six bits of register at I/O port 70h affect RTC operation and should be considered when changing NMI- generation status.

Register 0C14h bits <3,2> provide individual enable/disable control for the PERR and SERR signals respectively. The power up default has all three sources enabled for NMI generation.

4.5.2.2 SMI- Generation

The SMI- (System Management Interrupt) is typically used for power management functions. When power management is enabled, inactivity timers are monitored. When a timer times out, SMI- is asserted and invokes the microprocessor's SMI handler. The SMI- handler works with the APM BIOS to service the SMI- according to the cause of the timeout. Note that some system management functions are handled through the maskable interrupt control logic.

The SMI- is also generated by the user invoking the Quicklock feature, even though this function is not considered a power management function.

4.6 INTERVAL TIMER

The interval timer generates pulses at software (programmable) intervals. A 8254-compatible timer is integrated into the support chip that provides the PCI/ISA bridge function. The timer function provides three counters, the functions of which are listed in Table 4-13.

Table 4-13.
Interval Timer Functions

Counter	Function	Gate	Clock In	Clock Out
0	System Clock	Always on	1.193 MHz	IRQ0
1	Refresh	Always on	1.193 MHz	Refresh Req.
2	Speaker Tone	Port 61, bit<0>	1.193 MHz	Speaker Input

The interval timer is controlled through the I/O mapped registers listed in Table 4-14.

Table 4-14.
Interval Timer Control Registers

I/O Port	Register
040h	Read or write value, counter 0
041h	Read or write value, counter 1
042h	Read or write value, counter 2
043h	Control Word

Interval timer operation follows standard AT-type protocol. For a detailed description of timer registers and operation, refer to the *Compaq Extended Industry Standard Architecture Expansion Bus Technical Reference Guide.*

4.7 SYSTEM CLOCK DISTRIBUTION

The system uses an ICS9159-14 or compatible part for generation of most clock signals. Tables 4-15 and 4-16 lists the clock signals and to which components they are distributed.

Table 4-15.
Clock Generation and Distribution

Signal	Source	Destination
60, 66, MHz [1]	ICS9159	CPU, 82441, 82442, OSB, PCI Slots
48 MHz	"	OSB
24 MHz	"	87306
14.31818 MHz	Crystal	ICS 9159, OSB, GD5446, ISA slots
8 MHz (BCLK)	82371	ISA slots
32 KHz	Crystal	87306

[1] Depending on speed configuration.

4.8 REAL-TIME CLOCK AND CONFIGURATION MEMORY

The Real-time clock (RTC) and configuration memory (also referred to as CMOS) are integrated into the PC87306 I/O controller used in all models. The RTC uses the first 14 of 256 bytes of configuration memory and is MC146818-compatible. Figure 4-8 shows the configuration memory mapping.

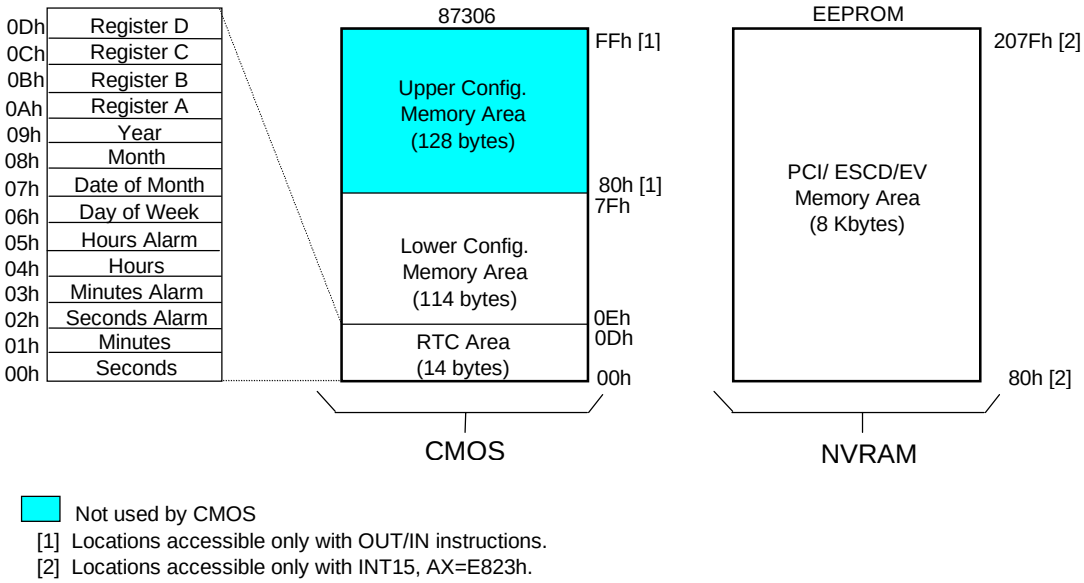


Figure 4–8. Configuration Memory Map

As indicated above, the 87306 controller provides 256 bytes of configuration memory, divided into two 128-byte banks. The first 128 bytes of RTC/configuration memory can be accessed using conventional OUT and IN assembly language instructions using I/O ports 70h/71h. The second bank or upper area is not used for CMOS and is available as scratch pad memory.

An 8-KB EEPROM provides additional non-volatile (NVRAM) storage of additional PCI, ESCD, and Environmental Variable (EV) data. The EEPROM is physically located on the backplane and accessed through a special register using a serial interface that operates similar to the I^2C protocol.

The BIOS function INT15, AX=E823h should be used for general access to the RTC/configuration memory.

A 3-VDC battery is used for maintaining the RTC and configuration memory while the system is powered down. This battery is soldered on the system board and is designed to last from 5-7 years. Once expired, the soldered battery is by-passed by connecting a replacement battery (Compaq p/n 160274-001 or equivalent 4.5 VDC @ 660 ma alkaline battery) to header E1 (pins 1-4, and moving the jumper from pins 6 and 7 to pins 5 and 6.

4.8.1 CONFIGURATION MEMORY BYTE DEFINITIONS

Table 4-17 lists the mapping of the configuration memory.

Table 4-17.
Configuration Memory (CMOS) Map

Location	Function	Location	Function
00-0Dh	Real-rime clock	40h-51h	Backup chassis serial number
0Eh	Diagnostic status	52h	SIMM type
0Fh	System reset code	53h	SWSMI command
10h	Diskette drive type	54h	SWSMI data
11h	Reserved	55h	APM command
12h	Hard drive type	56h	Multiprocessor byte
13h	Security functions	57h	Miscellaneous flags
14h	Equipment installed	58h-77h	Saved CMOS location 10h-2Fh
15h	Base memory size, low byte/KB	78h-7Fh	Administrator password
16h	Base memory size, high byte/KB	80h	ECMOS diagnostic byte
17h	Extended memory, low byte/KB	81h-82h	Total super ext. memory tested good
18h	Extended memory, high byte/KB	83h	Microprocessor chip ID
19h	Hard drive 1, primary controller	84h	Microprocessor chip revision
1Ah	Hard drive 2, primary controller	86h	Hood removal
1Bh	Hard drive 1, secondary controller	8Dh-8Fh	POST error logging
1Ch	Hard drive 2, secondary controller	90h-91h	Total super extended memory configured
1Dh	Enhanced hard drive support	92h	Miscellaneous configuration byte
1Eh	Reserved	93h	Miscellaneous PCI features
1Fh	Power management functions	9Ch	Mode-2 Configuration
24h	System board ID	9Dh	ESS audio configuration
25h	System architecture data	9Eh	ECP DMA configuration
26h	Auxiliary peripheral configuration	9Fh-AFh	Serial number
27h	Speed control external drive	B0h-C3h	Custom drive types 65, 66, 68, 15
28h	Expanded/base mem. size, IRQ12	C7h	Serial port 1 address and IRQ config. data
29h	Miscellaneous configuration	C8h	Serial port 2 address and IRQ config. data
2Ah	Hard drive timeout	DEh-DFh	Checksum of locations 90h to DDh
2Bh	System inactivity timeout	E0h-FFh	Client Management error log
2Ch	Monitor timeout, Num Lock Cntrl	100h-111h	Chassis serial number
2Dh	Additional flags	112h-117h	Manufacturing diagnostics data
2Eh-2Fh	Checksum of locations 10h-2Dh	118h-11Bh	Time stamp for hood removal
30h-31h	Total extended memory tested	11Ch-21Bh	Monitor EDID data
32h	Century	21Ch-21Fh	BIOS boot spec (IPL order)
33h	Miscellaneous flags set by BIOS	220h-223h	BIOS boot spec (BCV order)
34h	International language	224h-127Fh	PCI and ISA PnP ESCD data
35h	APM status flags	1280h-128Fh	Wellness variables
36h	ECC POST test single bit	1290h-12CFh	Critical error log
37h-3Fh	Power-on password	12D0h-130Fh	Non-critical error log
--	--	1310h-207Fh	EV storage area

NOTE: Assume unmarked gaps are reserved.

Default values (where applicable) are given for a standard system as shipped from the factory. The contents of configuration memory can be cleared by moving the jumper on header E1 pins 1,2 to pins 2,3.

RTC Control Register A, Byte 0Ah

Bit	Function
7	Update in Progress. Read only. 0 = Time update will not occur before 2444 us 1 = Time update will occur within 2444 us
6..4	Divider Chain Control. R/W. 00x = Oscillator disabled. 010 = Normal operation (time base frequency = 32.768 KHz). 11x = Divider chain reset.
3..0	Periodic Interrupt Control. R/W. Specifies the periodic interrupt interval. 0000 = none 1000 = 3.90625 ms 0001 = 3.90625 ms 1001 = 7.8125 ms 0010 = 7.8125 ms 1010 = 15. 625 ms 0011 = 122.070 us 1011 = 31.25 ms 0100 = 244.141 us 1100 = 62.50 ms 0101 = 488.281 us 1101 = 125 ms 0110 = 976.562 us 1110 = 250 ms 0111 = 1.953125 ms 1111 = 500 ms

RTC Control Register B, Byte 0Bh

Bit	Function
7	Time Update Enable/disable 0 = Normal operation, 1 = Disable time updating for time set
6	Periodic Interrupt Enable/Disable. 0 = Disable, 1 = Enable interval specified by Register A
5	Alarm Interrupt Enable/disable 0 = Disabled, 1 = Enabled
4	End-of-Update Interrupt Enable/Disable 0 = Disabled, 1 = Enabled
3	Reserved (read 0)
2	Time/Date Format Select 0 = BCD format, 1 = Binary format
1	Time Mode 0 = 12-lhour mode, 1 = 24-hour mode
0	Automatic Daylight Savings Time Enable/Disable 0 = Disable 1 = Enable (Advance 1 hour on 1st Sunday in April, retreat 1 hour on last Sunday in October).

RTC Status Register C, Byte 0Ch

Bit	Function
7	If set, interrupt output signal active (read only)
6	If set, indicates periodic interrupt flag
5	If set, indicates alarm interrupt
4	If set, indicates end-of-update interrupt
3..0	Reserved

RTC Status Register D, Byte 0Dh

Bit	Function
7	RTC Power Status 0 = RTC has lost power 1 = RTC has not lost power
6..0	Reserved

Configuration Byte 0Eh, Diagnostic Status

Default Value = 00h

This byte contains diagnostic status data.

Configuration Byte 0Fh, System Reset Code

Default Value = 00h

This byte contains the system reset code.

Configuration Byte 10h, Diskette Drive Type

Bit	Function
7..4	Primary (Drive A) Diskette Drive Type
3..0	Secondary (Drive B) Diskette Drive Type

Valid values for bits <7..4> and bits <3..0>:

0000 = Not installed
0001 = 360-KB drive
0010 = 1.2-MB drive
0011 = 720-KB drive
0100 = 1.44-MB/1.25-MB drive
0110 = 2.88-MB drive
(all other values reserved)

Configuration Byte 12h, Hard Drive Type

Bit	Function
7..4	Primary Controller 1, Hard Drive 1 Type: 0000 = none 1000 = Type 8 0001 = Type 1 1001 = Type 9 0010 = Type 2 1010 = Type 10 0011 = Type 3 1011 = Type 11 0100 = Type 4 1100 = Type 12 0101 = Type 5 1101 = Type 13 0110 = Type 6 1110 = Type 14 0111 = Type 7 1111 = other (use bytes 19h)
3..0	Primary Controller 1, Hard Drive 2 Type: 0000 = none 1000 = Type 8 0001 = Type 1 1001 = Type 9 0010 = Type 2 1010 = Type 10 0011 = Type 3 1011 = Type 11 0100 = Type 4 1100 = Type 12 0101 = Type 5 1101 = Type 13 0110 = Type 6 1110 = Type 14 0111 = Type 7 1111 = other (use bytes 1Ah)

Configuration Byte 13h, Security Functions

Default Value = 00h

Bit	Function
7	Reserved
6	QuickBlank Enable After Standby: 0 = Disable 1 = Enable
5	Administrator Password: 0 = Not present 1 = Present
4	Reserved
3	Diskette Boot Enable: 0 = Enable 1 = Disable
2	QuickLock Enable: 0 = Disable 1 = Enable
1	Network Server Mode/Security Lock Override: 0 = Disable 1 = Enable
0	Password State (Set by BIOS at Power-up) 0 = Not set 1 = Set

Configuration Byte 14h, Equipment Installed

Bit	Function
7,6	No. of Diskette Drives Installed: 00 = 1 drive 10 = Reserved 01 = 2 drives 11 = Reserved
5..2	Reserved
1	Coprocessor Present 0 = Coprocessor not installed 1 = Coprocessor installed
0	Diskette Drives Present 0 = No diskette drives installed 1 = Diskette drive(s) installed

Configuration Byte 15h and 16h, Base Memory Size

Bytes 15h and 16h hold a 16-bit value that specifies the base memory size in increments of 1-KB (1024) bytes. Valid base memory sizes are 512-KB and 640-KB.

Configuration Byte 17h and 18h, Extended Memory Size

Bytes 17h and 18h hold a 16-bit value that specifies the extended memory size in increments of 1-KB (1024) bytes.

Configuration Bytes 19h-1Ch, Hard Drive Types

Byte 19h contains the hard drive type for drive 1 of the primary controller if byte 12h bits <7..4> hold 1111b. Byte 1Ah contains the hard drive type for drive 2 of the primary controller if byte 12h bits <3..0> hold 1111b. Bytes1Bh and 1Ch contain the hard drive types for hard drives 1 and 2 of the secondary controller.

Configuration Byte 1Dh, Enhanced IDE Hard Drive Support

Default Value = F0h

Bit	Function
7	EIDE - Drive C (83h)
6	EIDE - Drive D (82h)
5	EIDE - Drive E (81h)
4	EIDE - Drive F (80h)
3..0	Reserved

Values for bits <7..4> :

0 = Disable

1 = Enable for auto-configure

Configuration Byte 1Fh, Power Management Functions

Default Value = 00h

Bit	Function
7..4	Reserved
3	Slow Processor Clock for Low Power Mode 0 = Processor runs at full speed 1 = Processor runs at slow speed
2	Reserved
1	Monitor Off Mode 0 = Turn monitor power off after 45 minutes in standby 1 = Leave monitor power on
0	Energy Saver Mode Blinking 0 = Disable 1 = Enable

Configuration Byte 24h, System Board Identification

Default Value = 7Eh

Configuration memory location 24h holds the system board ID.

Configuration Byte 25h, System Architecture Data

Default Value = 0Bh

Bit	Function
7..4	Reserved
3	Unmapping of ROM: 0 = Allowed 1 = Not allowed
2	Reserved
1,0	Diagnostic Status Byte Address 00 = Memory locations 80C00000h-80C00004h 01 = I/O ports 878h-87Ch 11 = neither place

Configuration Byte 26h, Auxiliary Peripheral Configuration

Default Value = 00h

Bit	Function
7,6	I/O Delay Select 00 = 420 ns (default) 01 = 300 ns 10 = 2600 ns 11 = 540 ns
5	Alternative A20 Switching 0 = Disable port 92 mode 1 = Enable port 92 mode
4	Reserved
3	Graphics Type 0 = Color 1 = Monochrome
2	Hard Drive Primary/Secondary Address Select: 0 = Primary 1 = Secondary
1,0	Reserved

Configuration Byte 27h, Speed Control/External Drive

Default Value = 00h

Bit	Function
7	Boot Speed 0 = Max MHz 1 = Fast speed
6..0	Reserved

Configuration Byte 28h, Expanded and Base Memory, IRQ12 Select

Default Value = 00h

Bit	Function
7	IRQ12 Select 0 = Mouse 1 = Expansion bus
6,5	Base Memory Size: 00 = 640 KB 01 = 512 KB 10 = 256 KB 11 = Invalid
4..0	Internal Compaq Memory: 00000 = None 00001 = 512 KB 00010 = 1 MB 00011 = 1.5 MB . . 11111 = 15.5 MB

Configuration Byte 29h, Miscellaneous Configuration Data

Default Value = 00h

Bit	Function
7..5	Reserved
4	Primary Hard Drive Enable (Non-PCI IDE Controllers) 0 = Disable 1 = Enable
3..0	Reserved

Configuration Byte 2Ah, Hard Drive Timeout

Default Value = 00h

Bit	Function
7..5	Reserved
4..0	Hard Drive Timeout 00000 = Disabled 00001 = 1 minute 00010 = 2 minutes . . 10101 = 21 minutes

Configuration Byte 2Bh, System Inactivity Timeout

Default Value = 41h

Bit	Function
7,6	Power Conservation Boot 00 = Reserved 01 = PC on 10 = PC off 11 = Reserved
5	Reserved
4..0	System Inactive Timeout. (Index to SIT system timeout record) 00000 = Disabled

Configuration Byte 2Ch, ScreenSave and NUMLOCK Control

Default Value = 01h

Bit	Function
7	Reserved for Use On Portables
6	Numlock Control 0 = Numlock off at power on 1 = Numlock on at power on
5..0	ScreenSave Timeout. (Index to SIT monitor timeout record) 000000 = Disabled

Configuration Byte 2Dh, Additional Flags

Default Value = 00h

Bit	Function
7..5	Reserved
4	Memory Test 0 = Test memory on power up only 1 = Test memory on warm boot
3	POST Error Handling (BIOS Defined) 0 = Display “Press F1 to Continue” on error 1 = Skip F1 message
2..0	Reserved

Configuration Byte 2Eh, 2Fh, Checksum

These bytes hold the checksum of bytes 10h to 2Dh.

Configuration Byte 30h, 31h, Total Extended Memory Tested

This location holds the amount of system memory that checked good during the POST.

Configuration Byte 32h, Century

This location holds the Century value in a binary coded decimal (BCD) format.

Configuration Byte 33h, Miscellaneous Flags

Default Value = 80h

Bit	Function
7	Memory Above 640 KB 0 = No, 1 = Yes
6	Reserved
5	Weitek Numeric Coprocessor Present: 0 = Not installed, 1 = Installed
4	Standard Numeric Coprocessor Present: 0 = Not installed, 1 = Installed
3..0	Reserved

Configuration Byte 34h, International Language Support

Default Value = 00h

Configuration Byte 35h, APM Status Flags

Default Value = 11h

Bit	Function
7..6	Power Conservation State: 00 = Ready 01 = Standby 10 = Suspend 11 = Off
5,4	Reserved
3	32-bit Connection: 0 = Disconnected, 1 = Connected
2	16-bit Connection 0 = Disconnected, 1 = Connected
1	Real Mode Connection 0 = Disconnected, 1 = Connected
0	Power Management Enable: 0 = Disabled 1 = Enabled

Configuration Byte 36h, ECC POST Test Single Bit Errors

Bit	Function
7	Row 7 Error Detect
6	Row 6 Error Detect
5	Row 5 Error Detect
4	Row 4 Error Detect
3	Row 3 Error Detect
2	Row 2 Error Detect
1	Row 1 Error Detect
0	Row 0 Error Detect

0 = No single bit error detected.
1 = Single bit error detected.

Configuration Byte 37h-3Fh, Power-On Password

These eight locations hold the power-on password.

Configuration Bytes 40h, 51h, Backup Chassis Serial Number

Configuration Byte 52h, SIMM Type

Bit	Function
7	Row 7
6	Row 6
5	Row 5
4	Row 4
3	Row 3
2	Row 2
1	Row 1
0	Row 0

0 = FPM DRAM
1 = EDO DRAM

Configuration Byte 53h, 54h, SW SMI Command/Data Bytes

Configuration Byte 55h, APM Command Byte

Configuration Byte 56h, Multiprocessor Byte

Bit	Function
7..4	Reserved
3, 2	Microprocessors Installed (set during POST): <3>, P1 (U31-BSP) <2>, P0 (U20)
1..0	Microprocessor Table (OS type) 00 = No table (UP) 01 = PIC mode (UP) 10 = Default 5 compatible table/ISA INTs (Novell) 11 = Full table/PCI INTs (WinNT)

Configuration Byte 57h, COMM/IR Port Designation

Bit 0 of this byte defines whether the COMM port is to be used for standard serial communication use (bit <0> = 0) or infrared interface use (bit <0> = 1). Bits <7..1> are reserved.

Configuration Byte 58h-77h, Saved CMOS Locations 10h-2Fh

These bytes hold a copy of CMOS locations 10h-2Fh **if** the Administrator password is set.

Configuration Bytes 78h-7Fh, Administrator Password

Configuration Byte 80h, CMOS Diagnostic Flags Byte

Default Value = 00h. Set bit indicates function is valid.

Bit	Function
7	CMOS Initialization (Set CMOS to Default)
6	Reserved
5	PnP should not reject SETs because Diags is active
4	Reserved
3	Manufacturing diagnostics diskette found
2	Invalid electronic serial number
1	Boot maintenance partition once
0	Invalid CMOS checksum

Configuration Byte 81h, 82h, Total Super Extended Memory Tested

This byte holds the value of the amount of extended system memory that tested good during POST. The amount is given in 64-KB increments.

Configuration Byte 83h, Microprocessor Identification

These bytes hold the component ID and chip revision of the microprocessor.

Configuration Byte 84h, Microprocessor Revision

Configuration Byte 86h, Hood Removal Function

Bit	Function
7..3	Reserved
2	Administrator Mode 0 = Non-administrator mode 1 = Administrator mode
1	No Boot Enabled/Disabled 0 = Disabled 1 = Enabled
0	Hood Removal Function 0 = Disabled 1 = Enabled

Configuration Byte 8Dh-8Fh, POST Error Logging

Default Value = 00h (all locations)

These bytes hold the logging errors. When all bits are cleared, the bytes are ready to record errors.

Configuration Byte 90h, 91h, Total Super Extended Memory Configured

This byte holds the value of the amount of extended system memory that is configured. The amount is given in 64-KB increments.

Configuration Byte 92h, Miscellaneous Configuration Byte

Default Value = 18h

Bit	Function
7	PCI VGA Snoop 0 = Disable 1 = Enable
6,5	Reserved
4	Diskette Write Control: 0 = Disable 1 = Enable
3..1	Reserved
0	Diskette Drive Swap Control: 0 = Don't swap 1 = Swap drive A: and B:

Configuration Byte 93h, PCI Configuration Byte

Default Value = 00h

Bit	Function
7..2	Reserved
1	PCI Bus Master Enable 0 = Enabled 1 = Disabled
0	PCI VGA Palette Snoop 0 = Disable 1 = Enable

If palette snooping is enabled, then a primary PCI graphics card may share a common palette with the ISA graphics card. Palette snooping should only be enabled if all of the following conditions are met:

- An ISA card connects to a PCI graphics card through the VESA connector.
- The ISA card is connected to a color monitor.
- The ISA card uses the RAMDAC on the PCI card
- The palette snooping feature (sometimes called "RAMDAC shadowing") on the PCI card is enabled and functioning properly.

Configuration Byte 9Ch, Mode-2 Configuration Byte

Default Value = 1Ch

Bit	Function
7,6	Reserved
5	Mode 2 Support 0 = Disable 1 = Enable
4	Secondary Hard Drive Controller 0 = Disable 1 = Enable
3,2	Secondary Hard Drive Controller IRQ 00 = IRQ10 01 = IRQ11 10 = IRQ12 11 = IRQ15
1,0	Reserved

Configuration Byte 9Dh, ESS Audio Configuration Byte

Default Value = 12h

Bit	Function
7	Reserved for Game Port Enable
6,5	Audio Address 00 = 22xh 01 = 23xh 10 = 24xh 11 = 25xh
4,3	DMA Channel 00 = Disabled 01 = DMA0 10 = DMA1 11 = DMA3
2,1	IRQ Select 00 = IRQ9 01 = IRQ5 10 = IRQ7 11 = IRQ10
0	ESS Audio Chip Enable 0 = Enabled 1 = Disabled

Configuration Byte 9Eh, ECP DMA Configuration Byte

Default Value = 03h

Bit	Function
7..4	Reserved
3	SafeStart Control: 0 = Disable 1 = Enable
2..0	ECP DMA Channel 000 = Invalid 100 = Disabled All other values (001-011, 101-111) refer to channel no.

Configuration Byte 9Fh-AFh, Asset Tag Serial Number

Configuration Bytes B0h-C3h; Custom Hard Drive Information

These bytes contain the number of cylinders, heads, and sectors per track for hard drives C, D, E, and F respectively. The mapping for each drive is as follows:

Drive 65 (C)	Drive 66 (D)	Drive 68 (E)	Drive 15 (F)	Function
B0h	B5h	BAh	BFh	No. of Cylinders, Low Byte
B1h	B6h	BBh	C0h	No. of Cylinders, High Byte
B2h	B7h	BCh	C1h	No. of Heads
B3h	B8h	BDh	C2h	Max ECC Bytes
B4h	B9h	BEh	C3h	No. of Sectors Per Track

Configuration Byte C7h, C8h, Serial Ports 1 and 2 (Respectively) Configuration Bytes

Default Value = FEh, 7Dh

Bit	Function
7..2	Base I/O Address (in packed format) (Algorithm: [Addr. - 200h] / 8) (i.e., 3Fh = 3F8h, 1Fh = 2F8h, 00 = 200h)
1..0	Interrupt: 00 = Reserved 01 = IRQ3 10 = IRQ4 11 = Reserved

Configuration Bytes DEh, DFh; Checksum of Locations 90h-DDh

Configuration Bytes E0h-FFh; Client Management Error Log

Configuration Byte 100h, 111h, Chassis Serial Number

Configuration Bytes 112h-117h, Manufacturing Diagnostic Bytes

The data stored in this location is accessable with the INT 15, AX=E821h BIOS function.

Configuration Bytes 118h-11Bh, Hood Removal Time Stamp Bytes

The data stored in this location indicates the time of hood (chassis cover) removal.

Configuration Bytes 11Ch-21Bh, Monitor EDID Data

This location holds monitor EDID data stored early in POST for up to two monitors (2 x 128 bytes).

Configuration Bytes 21Ch-21Fh, BIOS Boot Spec (Initial Program Load Order)

Configuration Bytes 220h-223h, BIOS Boot Spec (Boot Connection Vector Order)

Configuration Bytes 224h-127Fh, PCI and ISA PnP ESCD Storage Area (4188 bytes)

Configuration Bytes 1280h-128Fh, Wellness Variables (16 bytes)

Configuration Bytes 1290h-12CFh, Critical Error Log (64 bytes)

Configuration Bytes 12D0h-130Fh, Non-Critical Error Log (64 bytes)

Configuration Bytes 1310h-207Fh, Environmental Variable Storage Area (3440 bytes)

These bytes hold binary string data that defines a system's specific environment such as management data, serial number tracking, and other data used by such agents as the Compaq Insight Manager. This portion of CMOS is accessed as content-addressable memory using BIOS INT 15h, AX=D824h (retrieve) and INT 15h, AX=D825 (write) and INT 15h, AX=D826h (get nth EV). The names of the Environmental Variables (EVs) are stored as ASCII strings in a non-case sensitive format. The EVs should be structured (grouped) according to function for greater efficiency.

4.9 I/O MAP AND REGISTER ACCESSING

This section describes the system I/O map and methods of access.

4.9.1 SYSTEM I/O MAP

Table 4-18.
System I/O Map

I/O Port	Function
0000..000Fh	DMA Controller 1
0020..0021h	Interrupt Controller 1
0040..0043h	Timer 1
0060h	Keyboard Controller Data Byte
0061h	NMI, Speaker Control
0064h	Keyboard Controller Command/Status Byte
0070h	NMI Enable, RTC Address
0071h	RTC Data
0078h, 0079h	General Purpose I/O Ports 1 & 2
0080..008Fh	DMA Page Registers
0092h	Port A, Fast A20/Reset
00A0..00A1h	Interrupt Controller 2
00B2h, 00B3h	APM Control/Status Ports
00C0..00DFh	DMA Controller 2
00EE..00EFh	Alternate Fast A20/Reset
00F0h	Math Coprocessor Busy Clear
0170..0177h	Hard Drive (IDE) Controller 2
01F0..01FFh	Hard Drive (IDE) Controller 1
0201..024Fh	Audio subsystem control (primary & secondary addresses)
0278..027Bh	Parallel Port (LPT2)
02F8..02FFh	Serial Port (COM2)
0371.. 0375h	Diskette Drive Controller Alternate Addresses
0376h	IDE Controller Alternate Address
0377h	IDE Controller Alternate Address, Diskette Drive Controller Alternate Address
0378..037Fh	Parallel Port (LPT1)
0388..038Bh	FM synthesizer (alias addresses)
0398, 0399h	87306 Controller Configuration Registers (Index, Data)
03B0..03DFh	Graphics Controller
03E8..03EFh	Serial Port (COM3)
03F0..03F5h	Diskette Drive Controller Primary Addresses
03F6, 03F7h	Diskette Drive Controller Primary Addresses, Hard Drive Controller Primary Addresses
03F8..03FFh	Serial Port (COM1)
04D0, 04D1h	Master, Slave Edge/Level INTR Control Register
0C00, 0C01h	PCI IRQ Mapping Index, Data
0C06, 0C07h	Reserved - Compaq proprietary use only
0C50, 0C51h	Client Management Index, Data
0C52h	General Purpose Port
0C7Ch	Machine ID
0C80, 0C81h	Scan Chain High/Low Bytes
0C82h	Auto Rev Data
0C83h	Machine ID
0CD6h, 0CD7h	Power Management Registers
0CF8h	PCI Configuration Address (dword access)
0CFCh	PCI Configuration Data (byte, word, or dword access)
FF00..FF07h	IDE Bus Master Register

NOTE: Assume unmarked gaps are reserved/unused.

4.9.2 87306 I/O CONTROLLER CONFIGURATION

The 87306 I/O controller contains various functions such as the keyboard interface, diskette interface, serial interface, and parallel interface. While the control of these interfaces uses standard AT-type I/O addressing, the configuration of these functions must be through indexed ports unique to the 87306. In this system, ports 0398h and 0399h are used for accessing the indexed configuration registers of the 87306 I/O controller.

Table 4-19 lists the indexed configuration registers of the 87306. In accessing an indexed configuration register, the index value is written to 0398h and the data is then either written to or read from port 0399h.

Table 4-19.
87306 I/O Controller
Indexed Configuration Registers

Index	Function
00h	Function Enable Register (Parallel/serial ports, diskette drive cntlr.)
01h	Function Address Register (parallel/serial ports)
02h	Power and Test Register (power down, serial port cntrl., config. lock, EPP/ECP cntrl.)
03h	Function Control Register
04h	Printer Control Register (parallel port, RTC)
05h	Keyboard and RTC Control Register
06h	Power Management Control Register
07h	Tape, UART and Parallel Port Register
08h	Super I/O Identification Register
09h	Advanced Super I/O Configuration Register
0Ah	Chip Select 0 Low Address Register
0Bh	Chip Select 0 Configuration Register
0Ch	Chip Select 1 Low Address Register
0Dh	Chip Select 1 Configuration Register
0Eh	Infrared Configuration Register
0Fh	GPIO Port Base Address Configuration Register
10h	Chip Select 0 High Address Register
11h	Chip Select 1 High Address Register
12h	Super I/O Configuration Register 0
18h	Super I/O Configuration Register 1
19h	LPT Base Address Configuration Register
1Bh	Plug 'n Play Configuration Register 0
1Ch	Plug 'n Play Configuration Register 1

The General Purpose I/O (GPIO) ports of the 87306 are readable at I/O addresses 78h (for GPIO-1) and 79h (for GPIO-2). Although 78h and 79h are the default locations, the GPIO ports are re-locatable through indexed address 399.0Fh (listed above). On these systems, the GPIO ports are used for storing bus/core speed configuration (GPIO-1) and Auto REV data (GPIO-2). Refer to indexed "bus/core speed configuration" and "Auto REV" subjects for GPIO register details.

Chapter 5
INPUT/OUTPUT INTERFACES

5.1 INTRODUCTION

This chapter describes the system's interfaces that provide input and output (I/O) porting of data and specifically discusses digital data interfaces that are controlled through I/O-mapped registers. Most of the I/O interfaces are integrated functions of the support chipset and the 87306 I/O controller. The network interface controller and the SCSI adapter are supported through specific components mounted on the system board. The following I/O interfaces are covered in this chapter:

5.2 ENHANCED IDE INTERFACE

The enhanced IDE (EIDE) interface consists of a controller (integrated into the OSB ASIC) that supports up to four IDE devices. Devices that may connect to the IDE interface include:

- Hard drives
- CD-ROM drives
- Power Drives (writeable CD-ROM drives)
- 120-MB floppy drives

Two 40-pin keyed IDE data connectors are provided on the system board. Each connector can support two devices. The enhanced IDE is capable of performing PCI bus master transfers at rates up to 22 MBps.

5.2.1 IDE PROGRAMMING

The IDE interface is configured as a PCI device and controlled through standard I/O mapped registers.

5.2.1.1 IDE Configuration Registers

The IDE controller is integrated into the OSB ASIC and configured as a PCI device with bus mastering capability. The PCI configuration registers for the IDE controller function (PCI device #15, function #1) are listed in Table 5-1.

Table 5-1.
IDE PCI Configuration Registers (OSB ASIC)

PCI Configuration Address	Register	Value on Reset
00-01h	Vender ID	AE33h
02-03h	Device ID	0E11h
04-05h	PCI Command	0000h
06-07h	PCI Status	0000h
08h	Revision ID	0Ah
09h	Programming	xxxxh
0Ah	Sub-Class	01h
0Bh	Base Class Code	01h
0Dh	Master Latency Timer	0000h
0Eh	Header Type	80h
10-27h	Base Addr. Reg. 0-4	xx
2C-2Dh	Subsystem. Device ID	AE33h
2E-2Fh	Subsystem Vender ID	0E11h
3C-3Fh	IRQ Select, GNT/Latency	0000 01xx
70,71h	IDE Timing (Primary Drv.0)	0808h
72,73h	IDE Timing (Primary Drv.1)	0808h
74,75h	IDE Timing (Secondary Drv.0)	0808h
76,77	IDE Timing (Secondary Drv.1)	0808h
80,81h	EDMA Control/Status	xx

NOTE:
Assume unmarked gaps are reserved and/or not used.

5.2.1.2 IDE Bus Master Control Registers

The IDE interface can perform PCI bus master operations using the I/O mapped control registers listed in Table 5-2.

Table 5-2.
IDE Bus Master Control Registers

I/O Addr. Offset	Size (Bytes)	Register	Default Value
00h	2	Bus Master IDE Command (Primary)	00h
02h	2	Bus Master IDE Status (Primary)	00h
04h	4	Bus Master IDE Descriptor Ptr (Pri.)	0000 0000h
08h	2	Bus Master IDE Command (Secondary)	00h
0Ah	2	Bus Master IDE Status (Secondary)	00h
0Ch	4	Bus Master IDE Descriptor Ptr (Sec.)	0000 0000h

5.2.1.3 IDE ATA Control Registers

The IDE controller decodes the addressing of the standard AT attachment (ATA) registers for the connected drive, which is where the ATA control registers actually reside. The primary and secondary interface connectors are mapped as shown in Table 5-3.

Table 5-3.
IDE ATA Control Registers

Primary I/O Addr.	Secondary I/O Addr.	Register	R/W
1F0h	170h	Data	R/W
1F1h	171h	Error	R
1F1h	171h	Features	W
1F2h	172h	Sector Count	R/W
1F3h	173h	Sector Number	R/W
1F4h	174h	Cylinder Low	R/W
1F5h	175h	Cylinder High	R/W
1F6h	176h	Drive/Head	R/W
1F7h	177h	Status	R
1F7h	177h	Command	W
3F6h	376h	Alternate Status	R
3F6h	376h	Drive Control	W
3F7h	377h	Drive Address	R
3F7h	377h	n/a for hard drive	W

The following paragraphs describe the IDE ATA control registers.

Data Register, I/O Port 1F0h/170h

This register is used for transferring all data to and from the hard drive controller. This register is also used for transferring the sector table during format commands. All transfers are high-speed 16-bit I/O operation except for Error Correction Code (ECC) bytes during Read/Write Long commands.

Error Register, I/O Port 1F1h/171h (Read Only)

The Error register contains error status from the last command executed by the hard drive controller. The contents of this register are valid when the following conditions exist:

- Error bit is set in the Status register
- Hard drive controller has completed execution of its internal diagnostics

The contents of the Error register are interpreted as a diagnostic status byte after the execution of a diagnostic command or when the system is initialized.

Bit	Function
7	Bad Block Mark Detected in Requested Sector ID Field (if set)
6	Non-correctable Data Error (if set)
5	Reserved
4	Requested Sector ID Field Not Found (if set)
3	Reserved
2	Requested Command Aborted Due To Invalid Hard Drive Status or Invalid Command Code (if set)
1	Track 0 Not Found During Re-calibration Command (if set)
0	Data Address Mark Not Found After Correct ID Field (if set)

Set Features Register, I/O Port 1F1h/171h (Write Only)

This register is command-specific and may be used to enable and disable features of the interface.

Sector Count Register, I/O Port 1F2h/172h

This register defines either:

- the number of sectors of data to be read or written
  or
- the number of sectors per track for format commands

If the value in this register is zero, a count of 256 sectors is specified. The sector count is decremented as each sector is accessed, so that the value indicates the number of sectors left to access when an error occurs in a multi-sector operation. During the Initialize Drive Parameters command, this register contains the number of sectors per track.

Sector Number Register, I/O Port 1F3h/173h

The Sector Number register contains the starting sector number for a hard drive access.

Cylinder Low, Cylinder High Registers, I/O Port 1F4h, 1F5h/174h, 175h

These registers contain the starting cylinder number for each hard drive access. The three most-significant bits of the value are held in byte address 1F5h (bits <2..0>) while the remaining bits are held in location 1F4h.

Drive Select/Head Register, I/O Port 1F6h/176h

Bit	Function
7	Reserved
6,5	Sector Size: 00 = Reserved 01 = 512 bytes/sector 10, 11 = Reserved
4	Drive Select: 0 = Drive 1 1 = Drive 2
3..0	Head Select Number: 0000 = 0 1000 = 8 0001 = 1 1001 = 9 0010 = 2 1010 = 10 0011 = 3 1011 = 11 0100 = 4 1100 = 12 0101 = 5 1101 = 13 0110 = 6 1110 = 14 0111 = 7 1111 = 15

NOTE:

Setting bit <4> to 1 when Drive 2 is not present may cause remaining controller registers to not respond until Drive 1 is selected again.

Status Register, I/O Port 1F7h/177h (Read Only)

The contents of this register are updated at the completion of each command. If the Busy bit is set, no other bits are valid. Reading this register clears the IRQ14 interrupt.

Bit	Function
7	Controller Busy. If set, controller is executing a command.
6	READY- Signal Active (if set).
5	WRITE FAULT- Signal Active (if set).
4	SEEK COMPLETE- Signal Active (if set)
3	Data Request. If set, the controller is ready for a byte or word-length data transfer. Bit should be verified before each transfer.
2	Correctable Data Error Flag. If set, data error has occurred and has been corrected.
1	INDEX- Signal Active (if set).
0	Error Detected. When set, indicates error has occurred. O.ther bits in register should be checked to determine error source.

NOTE:

Register status of an error condition does not change until register is read.

The alternate Status register at location 3F6h holds the same status data as location 1F7h but does not clear hardware conditions when read.

Command Register, I/O Port 1F7h/177h (Write Only)

The IDE controller commands are written to this register. The command write action should be prefaced with the loading of data into the appropriate registers. Execution begins when the command is written to 1F7h/177h. Table 5-4 lists the standard IDE commands.

Table 5-4.
IDE Controller Commands

Command	Value
Initialize Drive Parameters	91h
Seek	7xh
Recalibrate	1xh
Read Sectors with Retries	20h*
Read Long with Retries	22h*
Write Sectors with Retries	30h*
Write Long with Retries	32h*
Verify Sectors with Retries	40h
Format Track	50h
Execute Controller Diagnostic	90h
Idle	97h, E3h
Idle Immediate	95h, E1h
Enter Low Power and Enable/Disable Timeout	96h
Enter Idle and Enable/Disable Timeout	97h
Check Status	98h
Identify	ECh
Read Buffer	E4h
Write Buffer	E8h
NOP	00h
Read DMA with Retry	C8h
Read DMA without Retry	C9h
Read Multiple	C4h
Set Features	EFh
Set Multiple Mode	C6h
Sleep	99h, E6h
Standby	96h, E2h
Standby Immediate	94h, E0h
Write DMA with Retry	CAh
Write DMA without Retry	CBh
Write Multiple	C5h
Write Same	E9h
Write Verify	3Ch

* Without retries, add one to the value.

Alternate Status Register, I/O Port 3F6h/376h (Read Only)

The alternate Status register at location 3F6h holds the same status data as location 1F7h but does not clear hardware conditions when read.

Drive Control Register, I/O Port 3F6h/376h (Write Only)

Bit	Function
7..3	Reserved
2	Controller Control: 0 = Re-enable 1 = Reset
1	Interrupt Enable/Disable 0 = Disable interrupts 1 = Enable interrupts
0	Reserved

Drive Access Register, I/O Port 3F7h/377h (Read Only)

Bit	Function
7	Reserved
6	WRITE GATE- Signal Active (if set)
5..2	Head Select: 0000 = 15 1000 = 7 0001 = 14 1001 = 6 0010 = 13 1010 = 5 0011 = 12 1011 = 4 0100 = 11 1100 = 3 0101 = 10 1101 = 2 0110 = 9 1110 = 1 0111 = 8 1111 = 0
1,0	Drive Select: 00 = Disabled 01 = Drive 1 selected 10 = Drive 0 selected 11 = Invalid

5.2.2 IDE CONNECTOR

This system uses a standard 40-pin connector for IDE devices. Device power is supplied through a separate connector.

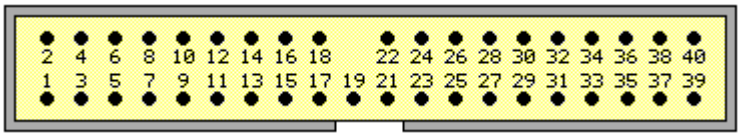


Figure 5–1. 40-Pin IDE Connector.

Table 5-5.
40-Pin IDE Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	RESET-	Reset	21	DRQ	DMA Request
2	GND	Ground	22	GND	Ground
3	DD7	Data Bit <7>	23	IOW-	I/O Write
4	DD8	Data Bit <8>	24	GND	Ground
5	DD6	Data Bit <6>	25	IOR-	I/O Read
6	DD9	Data Bit <9>	26	GND	Ground
7	DD5	Data Bit <5>	27	IORDY	I/O Channel Ready
8	DD10	Data Bit <10>	28	CSEL	Cable Select
9	DD4	Data Bit <4>	29	DAK-	DMA Acknowledge
10	DD11	Data Bit <11>	30	GND	Ground
11	DD3	Data Bit <3>	31	IRQn	Interrupt Request [1]
12	DD12	Data Bit <12>	32	IO16-	16-bit I/O
13	DD2	Data Bit <2>	33	DA1	Address 1
14	DD13	Data Bit <13>	34	DSKPDIAG	Pass Diagnostics
15	DD1	Data Bit <1>	35	DA0	Address 0
16	DD14	Data Bit <14>	36	DA2	Address 2
17	DD0	Data Bit <0>	37	CS0-	Chip Select
18	DD15	Data Bit <15>	38	CS1-	Chip Select
19	GND	Ground	39	HDACTIVE-	Drive Active (front panel LED) [2]
20	--	Key	40	GND	Ground

NOTES:

[1] Primary connector wired to IRQ14, secondary connector wired to IRQ15.

[2] Pin 39 is used for spindle sync and drive activity (becomes SPSYNC/DACT-) when synchronous drive is connected.

5.3 DISKETTE DRIVE INTERFACE

The diskette drive interface supports up to two diskette drives, each which connect to a standard 34-pin diskette drive connector. All models come standard with a 3.5 inch 1.44-MB diskette drive installed as drive A. An additional diskette drive (either a 3.5 inch 720-KB, 1.44-MB, or 2.88-MB drive or a 5.25 inch 360-KB or 1.2-MB drive) may also be installed as drive B. The drive designation is determined by which connector is used on the diskette drive cable. The drive attached to the end connector is drive A while the drive attached to the second (next to the end) connector) is drive B.

The diskette drive interface function is integrated into the 87306 component. The internal logic of the 87306 I/O controller is software-compatible with standard 82077-type logic. The diskette drive controller has three operational phases in the following order:

- Command phase - The controller receives the command from the system.
- Execution phase - The controller carries out the command.
- Results phase - Status and results data is read back from the controller to the system.

The Command phase consists of several bytes written in series from the CPU to the data register (3F5h/375h). The first byte identifies the command and the remaining bytes define the parameters of the command. The Main Status register (3F4h/374h) provides data flow control for the diskette drive controller and must be polled between each byte transfer during the Command phase.

The Execution phase starts as soon as the last byte of the Command phase is received. An Execution phase may involve the transfer of data to and from the diskette drive, a mechnical control function of the drive, or an operation that remains internal to the diskette drive controller. Data transfers (writes or reads) with the diskette drive controller are by DMA, using the DRQ2 and DACK2- signals for control.

The Results phase consists of the CPU reading a series of status bytes (from the data register (3F5h/375h)) that indicate the results of the command. Note that some commands do not have a Result phase, in which case the Execution phase can be followed by a Command phase.

During periods of inactivity, the diskette drive controller is in a non-operation mode known as the Idle phase.

5.3.1 DISKETTE DRIVE PROGRAMMING

5.3.1.1 Diskette Drive Interface Configuration

The diskette drive controller must be configured for a specific address and also must be enabled before it can be used. Address selection and enabling of the diskette drive interface are affected through the non-shaded bits of the following configuration register of the 87306 I/O controller:

Function Enable Register, Indexed Addr. 399.00h

Bit	Function
7	Not used on this system
6	IDE Enable (always = 0 on this system)
5	Diskette Drive Controller Base Address Select: 0 = Primary address (3F1h), 1 = Secondary address (371h)
4	Diskette Drive Controller Encoding (always = 0 on this system)
3	Diskette Drive Controller Enable: 0 = Disabled, 1 = Enabled
2	Not used on this system.
1	Serial Interface (UART 1) Enable: 0 = Disabled, 1 = Enabled
0	Parallel Interface Enable: 0 = Disabled, 1 = Enabled

Non-related functions.

5.3.1.2 Diskette Drive Interface Control

The BIOS function INT 13 provides basic control of the diskette drive interface. The diskette drive interface can be controlled by software through I/O-mapped registers listed in Table 5-6.

Table 5-6.
Diskette Drive Controller Registers

Primary Address	Alternate Address	Register	R/W
3F1h	371h	Media ID	R
3F2h	372h	Drive Control	W
3F4h	374h	Main Status	R
3F5h	375h	Data	R/W
3F7h	377h	Drive Status	R
		Data Transfer Rate	W

The base address (3F1h or 371h) and enabling of the diskette drive controller is selected through the Function Enable Register (FER, addr. 399.00h) of the 87306 I/O controller. Address selection and enabling is automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The following paragraphs describe the diskette drive interface control registers.

Media ID Register, I/O Port 3F1h/371h (Read Only)

Bit	Function
7..5	Media Type: xx1 = Invalid 000 = 5.25 inch drive 010 = 2.88 MB (3.5 inch drive) 100 = 1.44 MB (3.5 inch drive) 110 = 720 KB (3.5 inch drive)
4..2	Reserved
1,0	Tape Select: 00 = None 10 = Drive 2 01 = Drive 1 11 = Drive 3

Drive Control Register, I/O Port 3F2h/372h (Write Only)

Bit	Function
7,6	Reserved
5	Drive 2 Motor 0 = Off, 1 = On
4	Drive 1 Motor 0 = Off, 1 = On
3	Interrupt / DMA Enable 0 = Disabled, 1 = Enabled
2	Controller Enable 0 = Reset controller, 1 = Enable controller
1,0	Drive Select 00 = Drive 1 01 = Drive 2 10 = Reserved 11 = Tape drive

Main Status Register, I/O Port 3F4h/374h (Read Only)

Bit	Function
7	Request for Master. When set, indicates the controller is ready to send or receive data from the CPU. Cleared immediately after a byte transfer. Indicates interrupt pin status during non-DMA phase.
6	Data I/O Direction. 0 = Expecting a write 1 = Expecting a read
5	Non-DMA Execution. When set, indicates controller is in the execution phase of a byte transfer in non-DMA mode.
4	Command In Progress. When set, indicates that first byte of command phase has been received. Cleared when last byte in result phase is read.
3..0	Drive Busy Indicators. Bit is set after the last byte of the command phase of a seek or recalibrate command is given by the corresponding drive: <3>, Drive 3 <2>, Drive 2 <1>, Drive 1 <0>, Drive 0

Data Register, I/O Port 3F5h/375h

Data commands are written to, and data and status bytes are read from this register.

Data Transfer Rate Register, I/O Port 3F7h/377h (Write Only)

Bit	Function
7	Software Reset
6	Low Power Mode (if set)
5	Reserved
4..2	Write Precompensation Delay 000 = Default values for selected data rate (default)
1,0	Data Rate Select: 00 = 500 Kb/s 01 = 300 Kb/s 10 = 250 Kb/s 11 = 1 or 2 Mb/s (depending on TUP reg. Bit <1>)

5.3.2 DISKETTE DRIVE CONNECTOR

This system uses a standard 34-pin connector (refer to Figure 5-2 and Table 5-7 for the pinout) for diskette drives. Drive power is supplied through a separate connector.

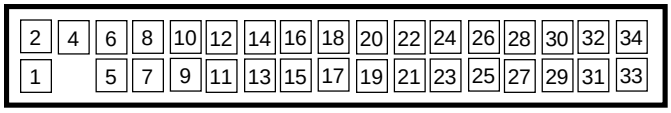


Figure 5–2. 34-Pin Diskette Drive Connector.

Table 5-7.
34-Pin Diskette Drive Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	18	DIR-	Drive head direction control
2	LOW DEN-	Low density select	19	GND	Ground
3	---	(KEY)	20	STEP-	Drive head track step control
4	MEDIA ID-	Media identification	21	GND	Ground
5	GND	Ground	22	WR DATA-	Write data
6	DRV 4 SEL-	Drive 4 select	23	GND	Ground
7	GND	Ground	24	WR ENABLE-	Enable for WR DATA-
8	INDEX-	Media index is detected	25	GND	Ground
9	GND	Ground	26	TRK 00-	Heads at track 00 indicator
10	MTR 1 ON-	Activates drive motor	27	GND	Ground
11	GND	Ground	28	WR PRTK-	Media write protect status
12	DRV 2 SEL-	Drive 2 select	29	GND	Ground
13	GND	Ground	30	RD DATA-	Data and clock read off disk
14	DRV 1 SEL-	Drive 1 select	31	GND	Ground
15	GND	Ground	32	SIDE SEL-	Head select (side 0 or 1)
16	MTR 2 ON-	Activates drive motor	33	GND	Ground
17	GND	Ground	34	DSK CHG-	Drive door opened indicator

5.4 SERIAL INTERFACES

The serial interfaces transmit and receive asynchronous serial data with external devices. The serial interface function is provided by the 87306 I/O controller component, which integrates two 16550/16450-compatible UARTs. Each UART supports a DB-9 connector on the rear of the chassis.

5.4.1 SERIAL INTERFACE PROGRAMMING

5.4.1.1 Serial Interface Configuration

The serial interfaces must be configured for a specific address range (COM1, COM2, etc.) and also must be enabled before it can be used. Address selection and enabling of the serial interface are affected through the non-shaded bits of the following configuration registers of the 87306 I/O controller. Address selection and enabling are automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

Function Enable Register, Indexed Addr. 399.00h

Bit	Function
7	Not used on this system
6	IDE Enable (always = 0 on this system)
5	Diskette Drive Controller Base Address Select 0 = Primary address (3F1h), 1 = Secondary address (371h)
4	Diskette Drive Controller Encoding (always = 0 on this system)
3	Diskette Drive Controller Enable: 0 = Disabled, 1 = Enabled
2	Serial Interface (UART 2) Enable: 0 = Disabled, 1 = Enabled
1	Serial Interface (UART 1) Enable: 0 = Disabled, 1 = Enabled
0	Parallel Interface Enable: 0 = Disabled, 1 = Enabled

Non-related functions.

Function Address Register, Indexed Addr. 399.01h

Bit	Function
7,6	COM3/COM4 Base Address Selection COM3 IRQ4 COM4 IRQ3 00 = 3E8h 2E8h 01 = 338h 238h 10 = 2E8h 2E0h 11 = 220h 228h
5,4	Serial Interface COMn Select (UART2): 00 = COM1 10 = COM3 (refer to bits <7,6>) 01 = COM2 11 = COM4 (refer to bits <7,6>)
3,2	Serial Interface COMn Select (UART1): 00 = COM1 10 = COM3 (refer to bits <7,6>) 01 = COM2 11 = COM4 (refer to bits <7,6>)
1,0	Parallel Interface Base Address (LPTn) & IRQ Select: 00 = 378h (LPT1), IRQ5 10 = 278h (LPT2), IRQ5 01 = 3BCh (LPT3), IRQ7 11 = Reserved

Non-related functions.

5.4.1.2 Serial Interface Control

The BIOS function INT 14 provides basic control of the serial interface. The serial interface can be controlled by software through the registers listed in Table 5-8.

Table 5-8.
Serial Interface Control Registers

Address	Register	R/W
Base	Receive Buffer / Transmit Holding [1]	R/W
Base, Base + 1	Baud Rate Divisor Latch [2]	R/W
Base + 1	Interrupt Enable	R/W
Base + 2	Interrupt ID	RO
Base + 3	Line Control	R/W
Base + 4	Modem Control	R/W
Base + 5	Line Status	RO
Base + 6	Modem Status	RO
Base + 7	Scratch Pad	R/W

NOTES:

Base Address:
COM1 = 3F8h COM3,4 = refer to reg. 399.01h
COM2 = 2F8h

[1] This register holds receive data when read from and transmit data when written to.
[2] When bit <7> of the Line Control register is set (1), writing to 3F8h and 3F9h programs the divisor rate for the baud rate generator.

Receive Buffer / Transmit Holding Register, I/O Port 3F8h/2F8h

When read by the CPU, this byte contains receive data. When written to by the CPU, the byte contains data to be transmitted.

Baud Rate Divisor Latch Register, I/O Port 3F8h, 3F9h/2F8, 2F9h

When bit <7> of the Line Control register is set (1), a write to this pair of locations loads the decimal value used to divide the 1.8462-MHz clock to create the desired baud rate for serial transmission. The possible baud rates are shown as follows:

Baud Rate	Decimal Divisor	Baud Rate	Decimal Divisor
50	2304	2400	48
75	1536	3600	32
110	1047	4800	24
134.5	857	7200	16
150	768	9600	12
300	384	19200	6
600	192	38400	3
1200	96	57600	2
1800	64	115200	1
4000/6000	58		

Divisor = 1846200 / (Desired baud rate X 16)

Interrupt Enable Register, I/O Port 3F9h/2F9h

Bits <3..0> of this register are used for enabling interrupt sources. A set bit enables interrupt generation by the associated source.

Bit	Function
7..4	Reserved
3	Modem Status Interrupt Enable (if set) (CTS, DSR, RI, CD)
2	Receiver Line Status Interrupt Enable (if set) (Overrun error, parity error, framing error, break)
1	Transmitter Holding Register Empty Interrupt Enable (if set)
0	Baud Rate Divisor Interrupt Enable (if set)

Interrupt ID Register, I/O Port 3FAh/2FAh (Read Only)

This read-only register indicates the serial controller as the source of the interrupt (bit <0>) as well as the reason (bits <3..1>) for the interrupt. Reading this register clears the interrupt and sets bit <0>.

Bit	Function
7,6	FIFO Enable/Disable 0 = Disabled 1 = Enabled
5,4	Reserved
3..1	Interrupt Source: 000 = Modem status (lowest priority) 001 = Transmitter holding reg. Empty 010 = Received data available 011 = Receiver line status reg. 100,101 = Reserved 110 = Character time-out (highest priority) 111 = Reserved
0	Interrupt Pending (if cleared)

FIFO Control Register, I/O Port 3FAh/2FAh (Write Only)

This write-only register enables and clears the FIFOs and set the trigger level and DMA mode.

Bit	Function
7,6	Receiver Trigger Level 00 = 1 byte 10 = 8 bytes 01 = 4 bytes 11 = 14 bytes
5..3	Reserved
2	Transmit FIFO Reset (if set)
1	Receive FIFO Reset (if set)
0	FIFOs Enable/Disable 0 = Disable TX/RX FIFOs, 1 = Enable TX/RX FIFOs

Line Control Register, I/O Port 3FBh/2FBh

This register specifies the data transmission format.

Bit	Function
7	RX Buffer / TX Holding Reg. And Divisor Rate Reg. Access 0 = RX buffer, TX holding reg., and Interrupt En. Reg. Are accessable. 1 = Divisor Latch reg. is accessable.
6	Break Control (forces SOUT signal low if set)
5	Stick Parity. If set, even parity bit is logic 0, odd parity bit is logic 1
4	Parity Type 0 = Odd, 1 = Even
3	Parity Enable: 0 = Disabled, 1 = Enabled
2	Stop Bit: 0 = 1 stop bit, 1 = 2 stop bits
1,0	Word Size: 00 = 5 bits 10 = 7 bits 01 = 6 bits 11 = 8 bits

Modem Control Register, I/O Port 3FCh/2FCh

This register controls the modem signal lines

Bit	Function
7..5	Reserved
4	Internal Loopback Enabled (if set)
3	Serial Interface Interrupts Enabled (if set)
2	Reserved
1	RTS Signal Active (if set)
0	DTR Signal Active (if set)

Line Status Register, I/O Port 3FDh/2FDh (Read Only)

This register contains the status of the current data transfer. Bits <2..0> are cleared when read.

Bit	Function
7	Parity Error, Framing Error, or Break Cond. Exists (if set)
6	TX Holding Reg. and Transmitter Shift Reg. Are Empty (if set)
5	TX Holding Reg. Is Empty (if set)
4	Break Interrupt Has Occurred (if set)
3	Framing Error Has Occurred (if set
2	Parity Error Has Occurred (if set)
1	Overrun Error Has Occurred (if set)
0	Data Register Ready To Be Read (if set)

Modem Status Register, I/O Port 3FEh/2FEh (Read Only)

This register contains the status of the modem signal lines. A set bit indicates that the associated signal is active.

Bit	Function
7	DCD- Active
6	RI- Active
5	DSR Active
4	CTS Active
3	DCD- Changed Since Last Read
2	RI- Changed From Low to High Since Last Read
1	DSR- Has Changed State Since Last Read
0	CTS- Has Changed State Since Last Read

Scratch Pad Register, I/O Port 3FFh/2FFh

This register is not used in this system.

5.4.2 SERIAL CONNECTOR

The DB-9 connector is shown in the following figure and the pinout of the connector is listed in Table 5-8.

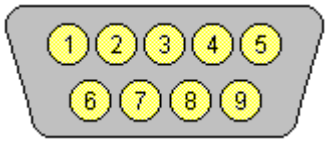


Figure 5–3. Serial Interface Connector (Male DB-9 as viewed from rear of chassis)

Table 5-9.
DB-9 Serial Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	CD	Carrier Detect	6	DSR	Data Set Ready
2	RX Data	Receive Data	7	RTS	Request To Send
3	TX Data	Transmit Data	8	CTS	Clear To Send
4	DTR	Data Terminal Ready	9	RI	Ring Indicator
5	GND	Ground	--	--	--

Each DB-9 port is independently configurable as to it's COMn (address) designation.

5.5 PARALLEL INTERFACE

The parallel interface provides connection to a peripheral device that has a compatible interface, the most common being a printer. The parallel interface function is integrated into the 87306 I/O controller component and provides bi-directional 8-bit parallel data transfers with a peripheral device. The parallel interface supports three modes of operation:

- Standard Parallel Port (SPP) mode
- Enhanced Parallel Port (EPP) mode
- Extended Capabilities Port (ECP) mode

These three modes provide complete support as specified for an IEEE 1284 parallel port.

5.5.1 STANDARD PARALLEL PORT MODE

The Standard Parallel Port (SPP) mode uses software-based protocol and includes two sub-modes of operation, compatible and extended, both of which can provide data transfers up to 150 KB/s. In the compatible mode, CPU write data is simply presented on the eight data lines. A CPU read of the parallel port yields the last data byte that was written.

The following steps define the standard procedure for communicating with a printing device:

1. The system checks the Printer Status register. If the Busy, Paper Out, or Printer Fault signals are indicated as being active, the system either waits for a status change or generates an error message.
2. The system sends a byte of data to the Printer Data register, then pulses the printer STROBE signal (through the Printer Control register) for at least 500 ns.
3. The system then monitors the Printer Status register for acknowledgment of the data byte before sending the next byte.

In extended mode, a direction control bit (CTR 37Ah, bit <5>) controls the latching of output data while allowing a CPU read to fetch data present on the data lines, thereby providing bi-directional parallel transfers to occur.

The SPP mode uses three registers for operation: the Data register (DTR), the Status register (STR) and the Control register (CTR). Address decoding in SPP mode includes address lines A0 and A1.

5.5.2 ENHANCED PARALLEL PORT MODE

In Enhanced Parallel Port (EPP) mode, increased data transfers are possible (up to 2 MB/s) due to a hardware protocol that provides automatic address and strobe generation. EPP revisions 1.7 and 1.9 are both supported. For the parallel interface to be initialized for EPP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with EPP mode. If compatible, then EPP mode can be used. In EPP mode, system timing is closely coupled to EPP timing. A watchdog timer is used to prevent system lockup.

Five additional registers are available in EPP mode to handle 16- and 32-bit CPU accesses with the parallel interface. Address decoding includes address lines A0, A1, and A2.

5.5.3 EXTENDED CAPABILITIES PORT MODE

The Extended Capabilities Port (ECP) mode, like EPP, also uses a hardware protocol-based design that supports transfers up to 2 MB/s. Automatic generation of addresses and strobes as well as Run Length Encoding (RLE) decompression is supported by ECP mode. The ECP mode includes a bi-directional FIFO buffer that can be accessed by the CPU using DMA or programmed I/O. For the parallel interface to be initialized for ECP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with ECP mode. If compatible, then ECP mode can be used.

Ten control registers are available in ECP mode to handle transfer operations. In accessing the control registers, the base address is determined by address lines A2-A9, with lines A0, A1, and A10 defining the offset address of the control register. Registers used for FIFO operations are accessed at their base address + 400h (i.e., if configured for LPT1, then 378h + 400h = 778h).

The ECP mode includes several sub-modes as determined by the Extended Control register. Two submodes of ECP allow the parallel port to be controlled by software. In these modes, the FIFO is cleared and not used, and DMA and RLE are inhibited.

5.5.4 PARALLEL INTERFACE PROGRAMMING

5.5.4.1 Parallel Interface Configuration

The parallel interface must be configured for a specific address range (LPT1, LPT2, etc.) and also must be enabled before it can be used. When configured for EPP or ECP mode, additional considerations must be taken into account. Address selection, enabling, and EPP/ECP mode parameters of the parallel interface are affected through the non-shaded bits of the following configuration registers of the 87306 I/O controller. Address selection and enabling are automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

Function Enable Register, Indexed Addr. 399.00h

Bit	Function
7	Not used on this system
6	IDE Enable (always = 0 on this system)
5	Diskette Drive Controller Base Address Select 0 = Primary address (3F1h), 1 = Secondary address (371h)
4	Diskette Drive Controller Encoding (always = 0 on this system)
3	Diskette Drive Controller Enable: 0 = Disabled, 1 = Enabled
2	Not used on this system.
1	Serial Interface (UART 1) Enable: 0 = Disabled, 1 = Enabled
0	Parallel Interface Enable: 0 = Disabled, 1 = Enabled

Non-related functions.

Function Address Register, Indexed Addr. 399.01h

Bit	Function
7,6	COM3/COM4 Base Address Selection COM3 IRQ4 COM4 IRQ3 00 = 3E8h 2E8h 01 = 338h 238h 10 = 2E8h 2E0h 11 = 220h 228h
5,4	Not used on this system.
3,2	Serial Interface COMn Select: 00 = COM1 10 = COM3 (refer to bits <7,6>) 01 = COM2 11 = COM4 (refer to bits <7,6>)
1,0	Parallel Interface Base Address (LPTn) & IRQ Select: 00 = 378h (LPT1), IRQ5 10 = 278h (LPT2), IRQ5 01 = 3BCh (LPT3), IRQ7 11 = Reserved

Non-related functions.

Printer Control Register, Indexed Addr. 399.04h

Bit	Function
7	RTC RAM Mask
6	Parallel I/F Interrupt Control 0 = Interrupt line has Tristate output 1 = Interrupt line has open drain output (drive low or tristate).
5	Parallel I/F Interrupt Polarity 0 = Polarity defined by SIO3 register 1 = Polalrity is inverted
4	Reserved
3	ECP Clock Freeze 0 = ECP mode does not affect stopping of crystal. 1 = Crystal/ECP clock is not stopped in ECP mode.
2	ECP Mode Enable/Disable 0 = Disabled 1 = Enabled
1	EPP Version Select: 0 = Ver. 1.7 1 = Ver. 1.9
0	EPP Enable/Disable 0 = Disabled 1 = Enabled (if bit <2> is 0)

Non-related functions.

Tape, UARTs, and Parallel Port Register, Indexed Addr. 399.07h

Bit	Function
7..3	Reserved
2	EPP Timeout Interupt Enable/Disable 0 = Disable 1 = Timeout interrupt is generated on selected IRQ line
1,0	Reserved

Non-related functions.

5.5.4.2 Parallel Interface Control

The BIOS function INT 17 provides simplified control of the parallel interface. Basic functions such as initialization, character printing, and printer status are provide by subfunctions of INT 17. The parallel interface is controllable by software through a set of I/O mapped registers. The number and type of registers available depends on the mode used (SPP, EPP, or ECP). Table 5-10 lists the parallel registers and associated functions based on mode.

Table 5-10.
Parallel Interface Control Registers

Register	I/O Address	SPP Mode Ports	EPP Mode Ports	ECP Mode Ports
Data	Base	LPT1,2,3	LPT1,2	LPT1,2,3
Status	Base + 1h	LPT1,2,3	LPT1,2	LPT1,2,3
Control	Base + 2h	LPT1,2,3	LPT1,2	LPT1,2,3
Address	Base + 3h	--	LPT1,2	--
Data Port 0	Base + 4h	--	LPT1,2	--
Data Port 1	Base + 5h	--	LPT1,2	--
Data Port 2	Base + 6h	--	LPT1,2	--
Data Port 3	Base + 7h	--	LPT1,2	--
Parallel Data FIFO	Base + 400h	--	--	LPT1,2,3
ECP Data FIFO	Base + 400h	--	--	LPT1,2,3
Test FIFO	Base + 400h	--	--	LPT1,2,3
Configuration Register A	Base + 400h	--	--	LPT1,2,3
Configuration Register B	Base + 401h	--	--	LPT1,2,3
Extended Control Register	Base + 402h	--	--	LPT1,2,3

Base Address:
LPT1 = 378h
LPT2 = 278h
LPT3 = 3BCh

The following paragraphs describe the individual registers. Note that only the LPT1-based addresses are given in these descriptions.

Data Register, I/O Port 378h

Data written to this register is presented to the data lines D0-D7. A read of this register when in SPP-compatible mode yields the last byte written. A read while in SPP-extended or ECP mode yields the status of data lines D0-D7 (i.e., receive data).

In ECP mode in the forward (output) direction, a write to this location places a tagged command byte into the FIFO and reads have no effect.

Status Register, I/O Port 3F9h, Read Only

This register contains the current printer status. Reading this register clears the interrupt condition of the parallel port.

Bit	Function
7	Printer Busy (if 0)
6	Printer Acknowledgment Of Data Byte (if 0)
5	Printer Out Of Paper (if 1)
4	Printer Selected/Online (if 1)
3	Printer Error (if 0)
2	Reserved
1	EPP Interrupt Occurred (if set while in EPP mode)
0	EPP Timeout Occurred (if set while in EPP mode)

Control Register, I/O Port 37Ah

This register provides the printer control functions.

Bit	Function
7,6	Reserved
5	Direction Control for PS/2 and ECP Modes: 0 = Forward. Drivers enabled. Port writes to peripheral (default) 1 = Backward. Tristates drivers and data is read from peripheral
4	Acknowledge Interrupt Enable 0 = Disable ACK interrupt 1 = Enable interrupt on rising edge of ACK
3	Printer Select (if 0)
2	Printer Initialize (if 1)
1	Printer Auto Line Feed (if 0)
0	Printer Strobe (if 0)

Address Register, I/O Port 37Bh (EPP Mode Only)

This register is used for selecting the EPP register to be accessed.

Data Port Registers 0-3, I/O Ports 37C-Fh (EPP Mode Only)

These registers are used for reading/writing data. Port 0 is used for all transfers. Ports 1-3 are used for transferring the additional bytes of 16- or 32-bit transfers through port 0.

FIFO Register, I/O Port 7F8h (ECP Mode Only)

While in ECP/forward mode, this location is used for filling the 16-byte FIFO with data bytes. Reads have no effect (except when used in Test mode). While in ECP/backward mode, reads yield data bytes from the FIFO.

Configuration Register A, I/O Port 7F8h (ECP Mode Only)

A read of this location yields 10h, while writes have no effect.

Configuration Register B, I/O Port 7F9h (ECP Mode, Read Only)

A read of this location yields the status defined as follows:

Bit	Function
7	Reserved (always 0)
6	Status of Selected IRQ*n*.
5,4	Selected IRQ Indicator: 00 = IRQ7 11 = IRQ5 All other values invalid.
3	Reserved (always 1)
2..0	Reserved (always 000)

Extended Control Register B, I/O Port 7FAh (ECP ModeOnly)

This register defines the ECP mode functions.

Bit	Function
7..5	ECP Submode Select: 000 = Standard forward mode (37Ah <5> forced to 0). Writes are controlled by software and FIFO is reset. 001 = PS/2 mode. Reads and writes are software controlled and FIFO is reset. 010 = Parallel Port FIFO forward mode (37Ah <5> forced to 0). Writes are hardware controlled. 011 = ECP FIFO mode. Direction determined by 37Ah, <5>. Reads and writes are hardware controlled.
4	ECP Interrupt Mask: 0 = Interrupt is generated on ERR- assertion. 1 = Interrupt is inhibited.
3	ECP DMA Enable/Disable. 0 = Disabled 1 = Enabled
2	ECP Interrupt Generation with DMA 0 = Enabled 1 = Disabled
1	FIFO Full Status (Read Only) 0 = Not full (at least 1 empty byte 1 = Full
0	FIFO Empty Status (Read Only) 0 = Not empty (contains at least 1 byte) 1 = Empty

5.5.5 PARALLEL INTERFACE CONNECTOR

Figure 5-4 and Table 5-11 show the connector and pinout of the parallel inrteface connector.

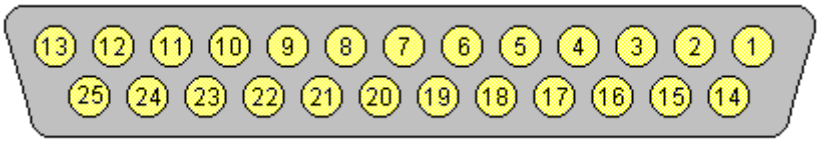


Figure 5–4. Parallel Interface Connector (Female DB-25 as viewed from rear of chassis)

Table 5-11.
DB-25 Parallel Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	STB-	Strobe	14	LF-	Line Feed
2	D0	Data 0	15	ERR-	Error
3	D1	Data 1	16	INIT-	Initialize Paper
4	D2	Data 2	17	SLCTIN-	Select In
5	D3	Data 3	18	GND	Ground
6	D4	Data 4	19	GND	Ground
7	D5	Data 5	20	GND	Ground
8	D6	Data 6	21	GND	Ground
9	D7	Data 7	22	GND	Ground
10	ACK-	Acknowledge	23	GND	Ground
11	BSY	Busy	24	GND	Ground
12	PE	Paper End	25	GND	Ground
13	SLCT	Select	--	--	--

5.6 KEYBOARD/POINTING DEVICE INTERFACE

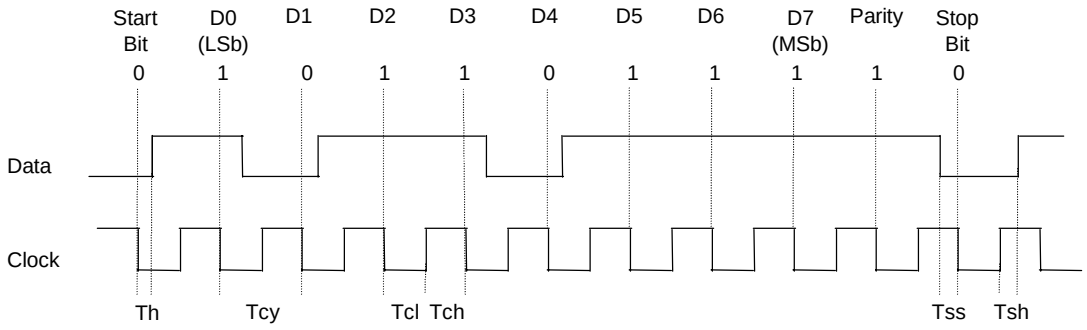
The keyboard/pointing device interface provides the connection of an enhanced keyboard and a mouse using PS/2-type connections. The keyboard/pointing device interface function is provided by the 87306 I/O controller component, which integrates 8042-compatible keyboard controller logic (hereafter referred to as simply the "8042") to communicate with the keyboard and pointing device using bi-directional serial data transfers. The 8042 handles scan code translation and password lock protection for the keyboard as well as communications with the pointing device. This section describes the interface itself. The keyboard is discussed in the Appendix C.

5.6.1 KEYBOARD INTERFACE OPERATION

The data/clock link between the 8042 and the keyboard is uni-directional for Keyboard Mode 1 and bi-directional for Keyboard Modes 2 and 3. (These modes are discussed in detail in Appendix C). This section describes Mode 2 (the default) mode of operation.

Communication between the keyboard and the 8042 consists of commands (originated by either the keyboard or the 8042) and scan codes from the keyboard. A command can request an action or indicate status. The keyboard interface uses IRQ1 to get the attention of the CPU.

The 8042 can send a command to the keyboard at any time. When the 8042 wants to send a command, the 8042 clamps the clock signal from the keyboard for a minimum of 60 us. If the keyboard is transmitting data at that time, the transmission is allowed to finish. When the 8042 is ready to transmit to the keyboard, the 8042 pulls the data line low, causing the keyboard to respond by pulling the clock line low as well, allowing the start bit to be clocked out of the 8042. The data is then transferred serially, LSb first, to the keyboard (Figure 5-5). An odd parity bit is sent following the eighth data bit. After the parity bit is received, the keyboard pulls the data line low and clocks this condition to the 8042. When the keyboard receives the stop bit, the clock line is pulled low to inhibit the keyboard and allow it to process the data.



Parameter	Minimum	Maximum
Tcy (Cycle Time)	0 us	80 us
Tcl (Clock Low)	25 us	35 us
Tch (clock High)	25 us	45 us
Th (Data Hold)	0 us	25 us
Tss (Stop Bit Setup)	8 us	20 us
Tsh (Stop Bit Hold)	15 us	25 us

Figure 5–5. 8042-To-Keyboard Transmission of Code EDh, Timing Diagram

Control of the data and clock signals is shared by the 8042and the keyboard depending on the originator of the transferred data. Note that the clock signal is always generated by the keyboard. After the keyboard receives a command from the 8042, the keyboard returns an ACK code. If a parity error or timeout occurs, a Resend command is sent to the 8042.

Table 5-12 lists and describes commands that can be issued by the 8042 to the keyboard.

Table 5-12.
8042-To-Keyboard Commands

Command	Value	Description
Set/Reset Status Indicators	EDh	Enables LED indicators. Value EDh is followed by an option byte that specifies the indicator as follows: Bits <7..3> not used Bit <2>, Caps Lock (0 = off, 1 = on) Bit <1>, NUM Lock (0 = off, 1 = on) Bit <0>, Scroll Lock (0 = off, 1 = on)
Echo	EEh	Keyboard returns EEh when previously enabled.
Invalid Command	EFh/F1h	These commands are not acknowledged.
Select Alternate Scan Codes	F0h	Instructs the keyboard to select another set of scan codes and sends an option byte after ACK is received: 01h = Mode 1 02h = Mode 2 03h = Mode 3
Read ID	F2h	Instructs the keyboard to stop scanning and return two keyboard ID bytes.
Set Typematic Rate/Display	F3h	Instructs the keyboard to change typematic rate and delay to specified values: Bit <7>, Reserved - 0 Bits <6,5>, Delay Time 00 = 250 ms 01 = 500 ms 10 = 750 ms 11 = 1000 ms Bits <4..0>, Transmission Rate: 00000 = 30.0 ms 00001 = 26.6 ms 00010 = 24.0 ms 00011 = 21.8 ms : 11111 = 2.0 ms
Enable	F4h	Instructs keyboard to clear output buffer and last typematic key and begin key scanning.
Default Disable	F5h	Resets keyboard to power-on default state and halts scanning pending next 8042 command.
Set Default	F6h	Resets keyboard to power-on default state and enable scanning.
Set Keys - Typematic	F7h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Make/Brake	F8h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Make	F9h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Typematic/Make/Brake	FAh	Clears keyboard buffer and sets default scan code set. [1]
Set Type Key - Typematic	FBh	Clears keyboard buffer and prepare to receive key ID. [1]
Set Type Key - Make/Brake	FCh	Clears keyboard buffer and prepare to receive key ID. [1]
Set Type Key - Make	FDh	Clears keyboard buffer and prepare to receive key ID. [1]
Resend	FEh	8042 detected error in keyboard transmission.
Reset	FFh	Resets program, runs keyboard BAT, defaults to Mode 2.

Note:
[1] Used in Mode 3 only.

5.6.2 POINTING DEVICE INTERFACE OPERATION

The pointing device (typically a mouse) connects to a 6-pin DIN-type connector that is identical to the keyboard connector both physically and electrically. The operation of the interface (clock and data signal control) is the same as for the keyboard. The pointing device interface uses the IRQ12 interrupt.

5.6.3 KEYBOARD/POINTING DEVICE INTERFACE PROGRAMMING

5.6.3.1 8042 Configuration

The keyboard/pointing device interface must be enabled and configured for a particular speed before it can be used. Enabling and speed parameters of the 8042 logic are affected through the non-shaded bits of the configuration register (shown below) of the 87306 I/O controller. Enabling and speed control are automatically set by the BIOS during POST but can also be accomplished with the Setup utility and other software.

Keyboard and RTC Control Register, Indexed Addr. 399.05h

Bit	Function
7	8042 Clock Source Select: 0 = X1 clock 1 = SYSCLK
6	Reserved
5	RAMSEL (CMOS Bank Select): 0 = Lower CMOS area 1 = Higher CMOS area
4	Reserved
3	RTC Enable: 0 = Disabled 1 = Enabled
2	Reserved (but must read/write 1 for 8042 functionality)
1	8042 Speed Control (In effect if bit <7> is 0) 0 = 8042 clock = X1 freq. / 3 (8 MHz nom.) 1 = 8042 clock = X1 freq. / 2 (12 MHz nom.)
0	8042 Enable: 0 = Disable (8042 clock inhibited) 1 = Enable

Non-related functions.

5.6.3.2 8042 Control

The BIOS function INT 16 is typically used for controlling interaction with the keyboard. Sub-functions of INT 16 conduct the basic routines of handling keyboard data (i.e., translating the keyboard's scan codes into ASCII codes). The keyboard/pointing device interface is accessed by the CPU through I/O mapped ports 60h and 64h, which provide the following functions:

- Output buffer reads
- Input buffer writes
- Status reads
- Command writes

Ports 60h and 64h can be accessed using the IN instruction for a read and the OUT instruction for a write. Prior to reading data from port 60h, the "Output Buffer Full" status bit (64h, bit <0>) should be checked to ensure data is available. Likewise, before writing a command or data, the "Input Buffer Empty" status bit (64h, bit <1>) should also be checked to ensure space is available.

I/O Port 60h

I/O port 60h is used for accessing the input and output buffers. This register is used to send and receive data from the keyboard and the pointing device. This register is also used to send the second byte of multi-byte commands to the 8042 and to receive responses from the 8042 for commands that require a response.

A read of 60h by the CPU yields the byte held in the output buffer. The output buffer holds data that has been received from the keyboard and is to be transferred to the system.

A CPU write to 60h places a data byte in the input byte buffer and sets the CMD/ DATA bit of the Status register to DATA. The input buffer is used for transferring data from the system to the keyboard. All data written to this port by the CPU will be transferred to the keyboard **except** bytes that follow a multibyte command that was written to 64h

I/O Port 64h

I/O port 64h is used for reading the status register and for writing commands. A read of 64h by the CPU will yield the status byte defined as follows:

Bit	Function
7..4	General Purpose Flags.
3	CMD/DATA Flag (reflects the state of A2 during a CPU write). 0 = Data 1 = Command
2	General Purpose Flag.
1	Input Buffer Full. Set (to 1) upon a CPU write. Cleared by IN A, DBB instruction.
0	Output Buffer Full (if set). Cleared by a CPU read of the buffer.

A CPU write to I/O port 64h places a command value into the input buffer and sets the CMD/DATA bit of the status register (bit <3>) to CMD. Table 5-13 lists the commands that can be sent to the 8042 by the CPU. The 8042 uses IRQ1 for gaining the attention of the CPU.

Table 5-13.
CPU Commands To The 8042

Value	Command Description
20h	Put current command byte in port 60h.
60h	Load new command byte. This is a two-byte operation described as follows: 1. Write 60h to port 64h. 2. Write the command byte to port 60h as follows: Bit <7> Reserved <6> Keyboard Code Conversion 0 = Do not convert codes 1 = Convert codes to 9-bit 8088/8086-compatible format Bit <5> Pointing Device Enable 0 = Enable pointing device 1 = Disable pointing device Bit <4> Keyboard Enable 0 = Enable keyboard 1 = Disable keyboard Bit <3> Reserved Bit <2> System Flag 0 = Cold boot 1 = CPU reset (exit from protected mode) Bit <1> Pointing Device Interrupt Enable 0 = Disable interrupt 1 = Enable interrupt Bit <0> Keyboard Interrupt Enable 0 = Disable interrupt 1 = Enable interrupt
A4h	Test password installed. Tests whether or not a password is installed in the 8042: If FAh is returned, password is installed. If F1h is returned, no password is installed.
A5h	Load password. This multi-byte operation places a password in the 8042 using the following manner: 1. Write A5h to port 64h. 2. Write each character of the password in 9-bit scan code (translated) format to port 60h. 3. Write 00h to port 60h.
A6h	Enable security. This command places the 8042 in password lock mode following the A5h command. The correct password must then be entered before further communication with the 8042 is allowed.
A7h	Disable pointing device. This command sets bit <5> of the 8042 command byte, pulling the clock line of the pointing device interface low.
A8h	Enable pointing device. This command clears bit <5> of the 8042 command byte, activating the clock line of the pointing device interface.
A9h	Test the clock and data lines of the pointing device interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
AAh	Initialization. This command causes the 8042 to inhibit the keyboard and pointing device and places 55h into the output buffer.
ABh	Test the clock and data lines of the keyboard interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
ADh	Disable keyboard command (sets bit <4> of the 8042 command byte).
AEh	Enable keyboard command (clears bit <4> of the 8042 command byte).

Continued

Table 5-13. CPU Commands To The 8042 *(Continued)*

Value	Command Description
C0h	Read input port of the 8042. This command directs the 8042 to transfer the contents of the input port to the output buffer so that they can be read at port 60h. The contents are as follows: Bit <7> Password Enable: 0 = Disabled 1 = Enabled Bit <6> External Boot Enable: 0 = Enabled 1 = Disabled Bit <5> Setup Enable: 0 = Enabled 1 = Disabled Bit <4> VGA Enable: 0 = Enabled 1 = Disabled Bit <3> Diskette Writes: 0 = Disabled 1 = Enabled Bit <2> Reserved Bit <1> Pointing Device Data Input Line Bit <0> Keyboard Data Input Line
C2h	Poll Input Port High. This command directs the 8042 to place bits <7..4> of the input port into the upper half of the status byte on a continous basis until another command is received.
C3h	Poll Input Port Low. This command directs the 8042 to place bits <3..0> of the input port into the lower half of the status byte on a continous basis until another command is received.
D0h	Read output port. This command directs the 8042 to transfer the contents of the output port to the output buffer so that they can be read at port 60h. The contents are as follows: Bit <7> Keyboard data stream Bit <6> Keyboard clock Bit <5> IRQ12 (pointing device interrupt) Bit <4> IRQ1 (keyboard interrupt) Bit <3> Pointing device clock Bit <2> Pointing device data Bit <1> A20 Control: 0 = Hold A20 low 1 = Enable A20 Bit <0> Reset Line Status; 0 = Inactive 1 = Active
D1h	Write output port. This command directs the 8042 to place the next byte written to port 60h into the output port (only bit <1> can be changed).
D2h	Echo keyboard data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the keyboard. No 11-to-9 bit translation takes place but an interrupt (IRQ1) is generated if enabled.
D3h	Echo pointing device data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the pointing device. An interrupt (IRQ12) is generated if enabled.
D4h	Write to pointing device. Directs the 8042 to send the next byte written to 60h to the pointing device.
E0h	Read test inputs. Directs the 8042 to transfer the test bits 1 and 0 into bits <1,0> of the output buffer.
F0h-FFh	Pulse output port. Controls the pulsing of bits <3..0> of the output port (0 = pulse, 1 = don't pulse). Note that pulsing bit <0> will reset the system.

5.6.4 KEYBOARD/POINTING DEVICE INTERFACE CONNECTOR

There are separate connectors for the keyboard and pointing device. Both connectors are identical both physically and electrically. Figure 5-6 and Table 5-14 show the connector and pinout of the keyboard/pointing device interface connectors.

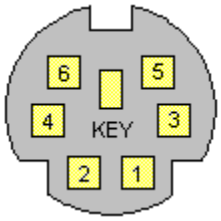


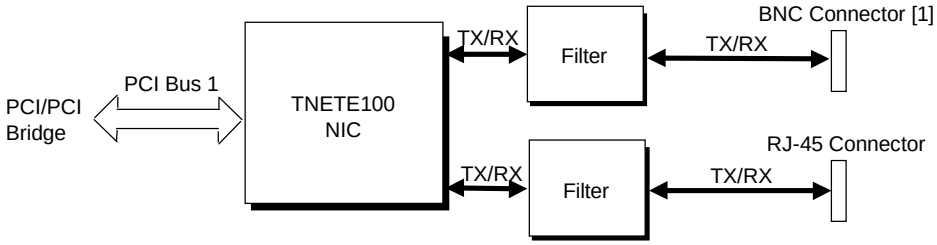
Figure 5–6. Keyboard or Pointing Device Interface Connector (as viewed from rear of chassis)

Table 5-14.
Keyboard/Pointing Device Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	DATA	Data	4	+ 5 VDC	Power
2	NC	Not Connected	5	CLK	Clock
3	GND	Ground	6	NC	Not Connected

5.7 NETWORK INTERFACE CONTROLLER

The system board integrates a network interface controller (NIC) that supports 10 Mbps Ethernet communications using IEEE 802.3 (ISO 8802-3) protocol. The NIC can automatically detect connection to a 100 Mbs circuit and switch to IEEE 802.12 protocol. Two physical connection options are available; an RJ-45 jack for twisted-pair Ethernet (TPE) systems (10 Base-T) and a BNC connector for THIN NET systems (10 Base-2). The Ethernet interface (Figure 5-7) is based on the TNETE100 component, which operates off the PCI bus.



[1] BNC connector not included on some versions

Figure 5–7. Network Interface Controller Block Diagram

The presence of the BNC connector can be checked by software through the registers shown as follows:

I/O Port 79h, Auto REV/Configuration Byte

Bit	Function
7,6	Backplane Type: 00 = 3-0-4 10 = 1-1-3 01 = 4-0-3 11 = 2-1-2
5	BNC Connector: 0 = Installed, 1 = Not installed
4..0	Auto REV Data

Non-related functions.

5.7.1 NIC CONNECTORS

The network interface provides two choices of connection to a system as shown in the following figures.

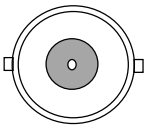
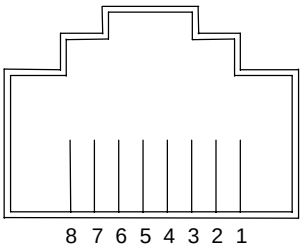


Figure 5–8. Ethernet BNC Connector

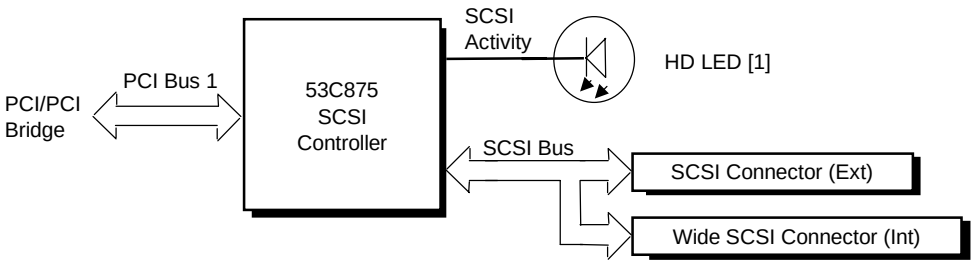


Pin	Description
1	Transmit
2	Receive
3	Receive Low
6	Transmit Low

Figure 5–9. Ethernet RJ-45 Connector

5.8 ULTRA SCSI ADAPTER

The system board integrates an Ultra SCSI adapter that provides an Ultra and Wide-Ultra interfaces for compatible SCSI peripheral devices. The interfaces are provided through a SYMBIOS 53C875 controller that is backward-compatible with previous SCSI implementations.



NOTE:
[1] LED located on power supply assembly.

Figure 5–10. SCSI Adapter, Block Diagram

The adapter follows standard SCSI guidelines in supporting up to seven devices using SCSI identification numbers 0-6 (ID #7 is reserved for the adapter). Each SCSI device chain must be terminated at both ends.

> **NOTE:** The adapter includes two connectors; and external Ultra SCSI connector and an internal Wide-Ultra SCSI connector. The internal connector is attached to a SCSI hard drive in the standard configuration. A system with multiple SCSI devices must have those devices interfacing through either the internal connector **or** the external connector, **but not both**.

The BIOS code for the 53C875 is included in the system's BIOS ROM and is copied during POST to the option ROM space at segment E8000h. The BIOS provides the following functions:

- INT 13h for multiple controllers and drives.
- Pass-through SCSI commands
- Synchronous and wide negotiations (initiated using pass-through)
- Fault prediction support (Compaq-supported drives only)

5.8.1 SCSI CONNECTORS

The SCSI adapter supports two interface connections; an externally accessable Ultra SCSI connector (Figure 5-11) and a Wide-Ultra SCSI connector (Figure 5-12) on the system board that is connected with the standard hard drive. The SCSI adapter supports only one connector at a time.

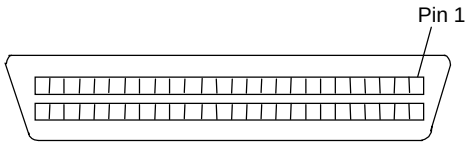


Figure 5–11. Ultra SCSI Connector (50-pin, as viewed from rear of chassis)

Table 5-15.
Ultra SCSI Connector Pinout

Pin	Signal	Function	Pin	Signal	Function
1	GND	Ground	26	DB0-	Data Bit 0
2	GND	Ground	27	DB1-	Data Bit 1
3	GND	Ground	28	DB2-	Data Bit 2
4	GND	Ground	29	DB3-	Data Bit 3
5	GND	Ground	30	DB4-	Data Bit 4
6	GND	Ground	31	DB5-	Data Bit 5
7	GND	Ground	32	DB6-	Data Bit 6
8	GND	Ground	33	DB7-	Data Bit 7
9	GND	Ground	34	DBP	Data Bus Pulse
10	GND	Ground	35	GND	Ground
11	GND	Ground	36	GND	Ground
12	GND	Ground	37	GND	Ground
13	RSVD	Reserved	38	TERMPWR	Termination Power
14	GND	Ground	39	GND	Ground
15	GND	Ground	40	GND	Ground
16	GND	Ground	41	ATN-	Attention
17	GND	Ground	42	GND	Ground
18	GND	Ground	43	BSY-	Busy
19	GND	Ground	44	ACK-	Acknowledge
20	GND	Ground	45	SBRST-	Burst
21	GND	Ground	46	MSG-	Message Activity
22	GND	Ground	47	SEL-	Select
23	GND	Ground	48	C-/D	Control/Data Transfer Indicator
24	GND	Ground	49	REQ-	Request
25	GND	Ground	50	I-/O	Input/Output Indicator

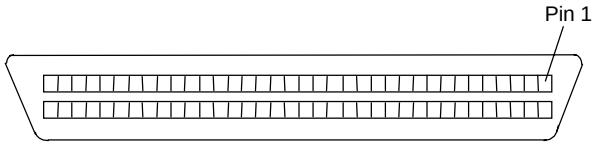


Figure 5–12. Wide-Ultra SCSI Connector (68-pin, as viewed from top of system board)

Table 5-16.
Wide-Ultra SCSI Connector Pinout

Pin	Signal	Function	Pin	Signal	Function
1	GND	Ground	35	DB12	Data Bit 12
2	GND	Ground	36	DB13	Data Bit 13
3	GND	Ground	37	DB14	Data Bit 14
4	GND	Ground	38	DB15	Data Bit 15
5	GND	Ground	39	DBP-	Data Bus Parity
6	GND	Ground	40	DB0-	Data Bit 0
7	GND	Ground	41	DB1-	Data Bit 1
8	GND	Ground	42	DB2-	Data Bit 2
9	GND	Ground	43	DB3-	Data Bit 3
10	GND	Ground	44	DB4-	Data Bit 4
11	GND	Ground	45	DB5-	Data Bit 5
12	GND	Ground	46	DB6-	Data Bit 6
13	GND	Ground	47	DB7-	Data Bit 7
14	GND	Ground	48	DBP-	Data Bus Parity
15	GND	Ground	49	GND	Ground
16	GND	Ground	50	GND	Ground
17	TERMPWR	Termination Power	51	TERMPWR	Termination Power
18	TERMPWR	Termination Power	52	TERMPWR	Termination Power
19	GND	Ground	53	Int_Out-	Interrupt Out
20	GND	Ground	54	SBRST-	Burst
21	GND	Ground	55	ATN-	Attention
22	GND	Ground	56	GND	Ground
23	GND	Ground	57	BSY-	Busy
24	GND	Ground	58	ACK-	Acknowledge
25	GND	Ground	59	RESET-	Reset
26	GND	Ground	60	MSG-	Message Activity
27	GND	Ground	61	SEL-	Select
28	GND	Ground	62	C-/D	Control/Data Transfer Indicator
29	GND	Ground	63	REQ-	Request
30	GND	Ground	64	I-/O	Input/Output Indicator
31	GND	Ground	65	DB8-	Data Bit 8
32	GND	Ground	66	DB9-	Data Bit 9
33	GND	Ground	67	DB10-	Data Bit 10
34	GND	Ground	68	DB11-	Data Bit 11

Chapter 6
AUDIO SUBSYSTEM

6.1 INTRODUCTION

This chapter describes the audio subsystem that is integrated onto the system board. The audio subsystem is compatible with software written for industry-standard sound subsystems. The audio subsystem can capture and playback .WAV files (as used in most Windows applications). Support for FM synthesis for playback of MIDI (.MID) files is also included.

This appendix covers the following subjects:

6.2 FUNCTIONAL DESCRIPTION

A block diagram of the audio subsystem is shown in Figure 6-1. The architecture is based on the ES1868 audio controller, which provides the ADC, DAC, FM synthesis, and mixing functions. Output volume is affected by either software or by the potentiometer on the subsystem edge. The software volume control uses 6-bit resolution providing 64 levels. Connections are provided for CD-ROM and system speaker connections.

Four analog interfaces are provided to connect to external audio devices and are discussed in the following paragraphs.

Line In - This input uses a three-conductor (stereo) mini-jack for connecting left and right channel line-level signals (20-K ohm impedance). A typical connection would be to a tuner's Line Out or Record Out jacks, or to a tape deck's Line Out or Playback Output jacks. A less optimum but acceptable connection would be to the headphone output of the tape deck or CD player.

Line Out - This output uses a three-conductor (stereo) mini-jack for connecting left and right channel line-level signals (20-K ohm impedance). A typical connection would be to a tape recorder's Line In or Record In jacks or to an amplifier's Line In jacks.

Mic In - This input uses a three-conductor (stereo) mini-jack that is specifically designed for connecting a condenser microphone with an impedance of 1-K ohms. This is the default recording input after a system reset.

Headphone Out - This output uses a three-conductor (stereo) mini-jack for connecting a pair of stereo headphones with a minimum impedance of 16 ohms. This jack can also be used to connect a pair of powered speakers (i.e., the type designed to be used with portable radio/cassette/CD players). Using this connector defeats (mutes) the internal speaker and Line Out signals.

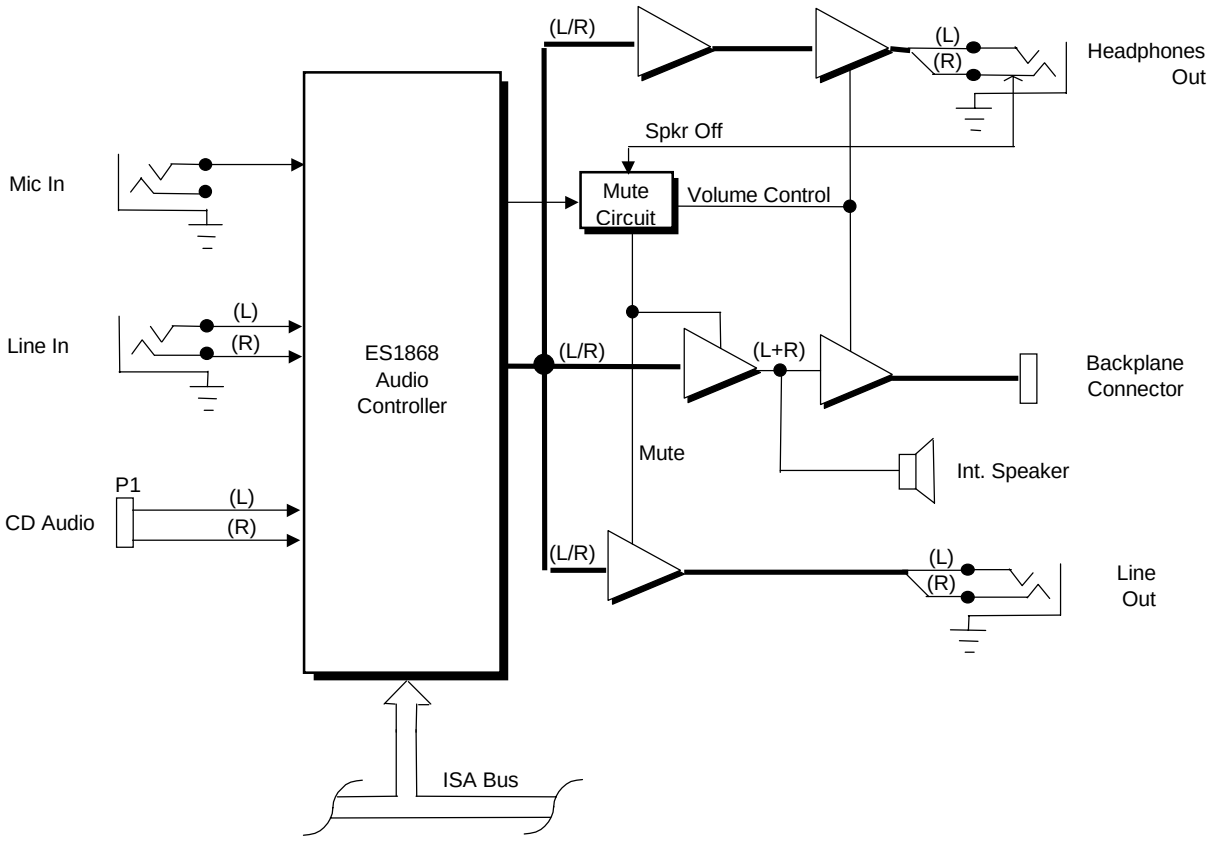


Figure 6–1. Audio Subsystem Block Diagram

6.2.1 PCM AUDIO PROCESSING

The audio subsystem uses pulse code modulation (PCM) for processing audio that is applied from external sources to the Mic In and Line In input jacks, as well as audio from an installed CD-ROM drive. The PCM method is also used in playback of .WAV file data commonly used in Windows applications.

6.2.1.1 ADC Operation

The Analog-to-Digital Converter (ADC) receives an analog signal and, using pulse code modulation (PCM) converts it into digital data that can be handled by normal logic circuitry. The conversion process consists of measuring (sampling) the analog signal at intervals to determine the amplitude and frequency (see Figure 6-2). The frequency of sampling intervals is a programmable parameter known as the sampling rate. The higher the sampling rate, the more accurate the digital representation will be.

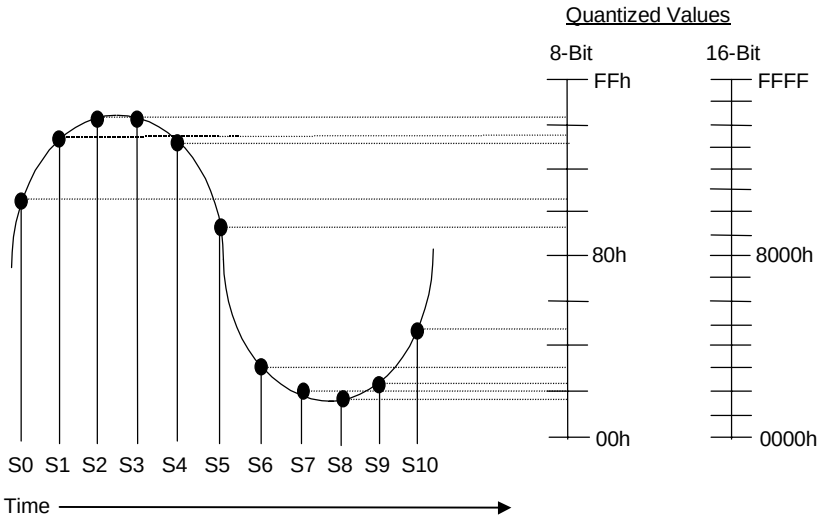


Figure 6–2. Analog Signal Sampling/Quantizing

Each sample is quantized into a digital code that specifies the voltage level of the analog signal at that particular time. The quantizing format options are as follows:

Mono or stereo
8- or 16-bit
Signed or unsigned

6.2.1.2 DAC Operation

The digital-to-analog conversion (DAC) simply reverses the procedure of the ADC. The digital audio data stream is received by the DAC and the quantized values are decoded at the sampling rate (Figure 6-3A) into DC levels, resulting in a descrete level wave form (Figure 6-3B). A filter provides the final shaping of the wave (Figure 6-3C) before it is applied to the analog output circuitry.

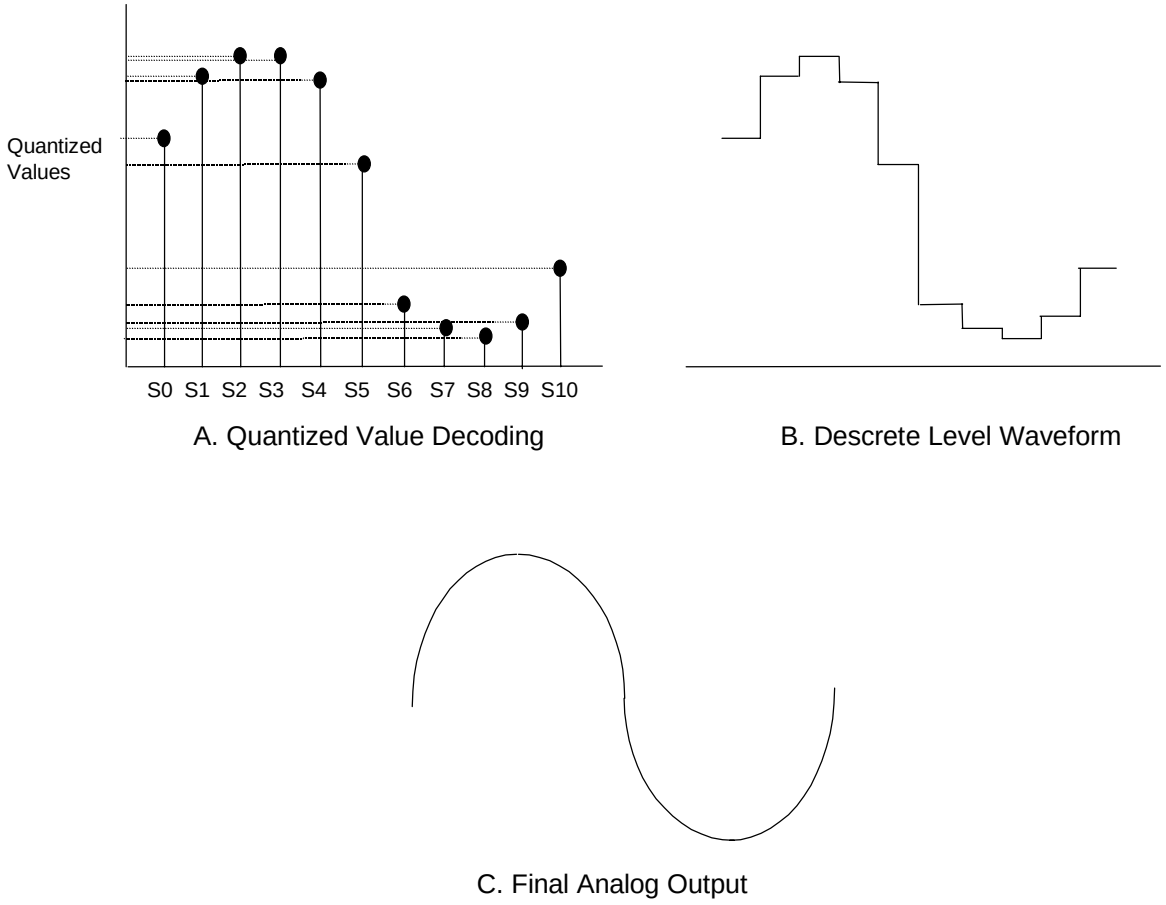


Figure 6–3. DAC Operation

Compressed sound formats provide efficient use of space by concentrating sampling/quantizing in the middle of the sound spectrum and is suited for voice capture/playback. The DAC of the ES1868 controller supports two type of compressed sound; ADPCM and ESPCM. The ADPCM compressed format is compatible with common industry sound subsystems while ESPCM is a proprietary format that offers greater performance.

6.2.1.3 PCM Configuration Modes

PCM operation can be configured for compatible (common sound board functionality) mode or set up for extended mode, which has some performance advantages. Table 6-1 lists the differences between the modes of operation.

Table 6-1.
Audio Mode Differences

Function	Compatibility Mode	Extended Mode
FIFO Size Available	64 bytes (SW Control)	256 bytes (HW Control)
Mono 8-bit ADC, DAC	44 KHz Max Sampling)	44 KHz Max Sampling
Mono 16-bit ADC, DAC	22 KHz Max Sampling	44 KHz Max Sampling
Stereo 8-bit ADC, DAC	22 KHz Max Sampling	44 KHz Max Sampling
Stereo 16-bit ADC	n/a	44 KHz Max Sampling
Stereo 16-bit DAC	11 KHz Max Sampling	44 KHz Max Sampling
Signed/Unsigned Control	No	Yes
AGC During Capture	Mono Only (22 KHz)	No
Programmed I/O Block Transfer	No	Yes
FIFO Status Flags	No	Yes
Auto Reload DMA	Yes	Yes
Time Base for Programmable Time	1 MHz or 1.5 MHz	800 KHz or 400 KHz
ADC/DAC Jitter	+/- 2 usec	None

6.2.1.4 PCM Bus Cycles

The I/O and DMA cycles used by PCM operations to process .WAV data follow standard ISA bus conventions. All bus transfers occur at the bytes level. Programmed I/O cycles are always used for programming the control registers and may also be used for transferring audio data to and from the audio subsystem as well. Quantized audio data is built using the “little endian” format (LSB occupies the lowest memory address). Data transfers over the ISA occur as shown below.

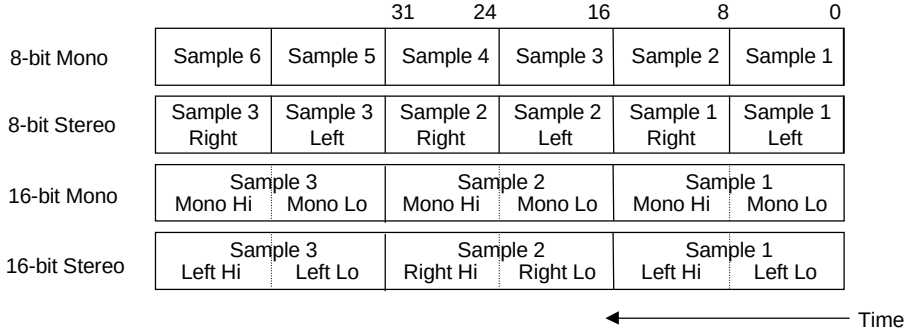


Figure 6–4. Audio Subsystem-to-ISA Bus PCM Audio Data Formats / Byte Ordering

6.2.2 FM SYNTHESIS AUDIO PROCESSING

The audio subsystem supports playback of MIDI (.MID) files. A .MID file does not contain audio information in the same way that .WAV files do. In .MID files, audio data consists of note on/off, tone type, and amplification information. Audio stored in the .MID file format has the benefit of taking up far less space than audio stored as .WAV files.

The ES1868 controller includes a 20-voice, four-operator frequency modulated (FM) synthesizer. In FM synthesis, one signal (the carrier) is forced to vary from it's center frequency by another signal (the modulator) resulting in a sideband or "harmonic" frequency. The frequency of the harmonic is determined by the original carrier frequency and the modulating frequency. The number of harmonics generated is determined by the strength (amplitude) of the modulating signal. The microsystem that produces the FM signal is called a patch (Figure 6-5).

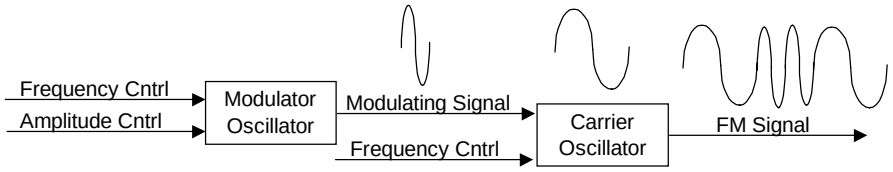


Figure 6–5. FM Synthesis Patch

Note that while an analog representation is shown in Figure D-6, synthesis occurs as a digital operation with the results being sent to the DAC.

The FM synthesis process is a playback-only operation involving the writing of .MID data to the audio subsystem over the ISA bus. The only reads involve checking the controller for status. Figure 6-6 shows the ISA bus transaction for FM synthesis. Note that if a succeeding data byte is meant for the same location as the previous byte, the address does not need to be re-written.

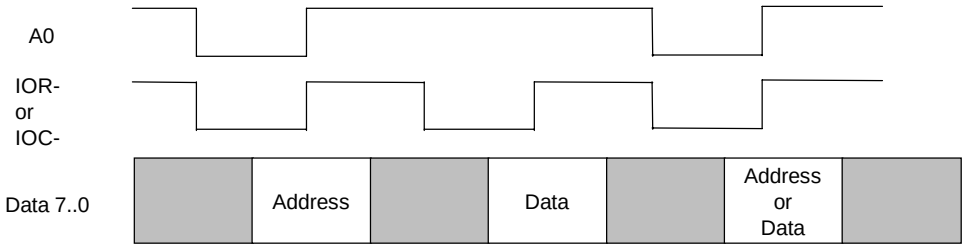


Figure 6–6. Audio Car-to-ISA Bus FM Audio Data Format

6.3 AUDIO SUBSYSTEM PROGRAMMING

All programming aspects of the audio subsystem relate directly to the programmability of the ES1868 controller, upon which the audio subsystem is based. This section describes only the basic mapping of the audio functions. For a detailed description of the ES1868s registers and capabilities refer to the *ES1868 AudioDrive Data Sheet, ESS Technology, Inc*. document number SAM0011.

6.3.1 CONFIGURATION

The audio subsystem is automatically configured as to base address, DMA, and interrupts following installation and power up through an on-board EEPROM that provides Plug ‘n Play support. Software can identify the ES1868 controller by reading indexed address 2n5.40h successively, which should yield the values 17h, 98h, followed by the base address of the ES1868.

The typical reset/power-up configuration for the audio subsystem is as follows:

Base Address:	220h
Interrupt:	IRQ5
DMA Channel:	1
Power Management:	Automatic

The audio subsystem can be configured or either single DMA channel mode or dual DMA channel mode. Single DMA channel mode means that capture and playback operations share the same (playback) DMA channel and only one operation, capture **or** playback, is possible at a time. Dual DMA channel operation allows simultaneous capture/playback (full duplex) operation to occur if desired, but requires the use of two DMA channels. Typically, dual DMA operation would use DMA channel 1 for capture (recording) and DMA channel 0, 1, or 3 for playback.

6.3.2 CONTROL

The audio subsystem is controlled through I/O mapped registers listed in Table 6-2.

Table 6-2.
Audio Subsystem I/O Map

I/O Address	Function	I/O Address	Function
201h	Joystick	2nAh	Read Buffer Input Data
2n0-2n3	FM Synthesizer Address/Data [1]	2nCh (Read)	Status
2n4h	Mixer Address	2nCh (Write)	Command/Data
2n5h	Mixer Data	2nEh	Data Available Status
2n6h (Read)	Activity/Power Status	2nFh	FIFO I/O Address (Extended Mode)
2n6h (Write)	Reset Control	3n0, 3n1h	MPU-401 Port
2n7h	Power Management	388-38Bh	FM Synthesizer (alias of 2n0-2n3h)
2n8, 2n9h	FM Synthesizer Address/Data [2]	--	--

NOTES:
n = 2 for primary address (default), = 4 for secondary address.
[1] 20-voice operation
[2] 11-voice operation
Not supported

6.3.2.1 PCM Control

The audio subsystem can operate in either Sound Blaster-compatible mode (the default) or in extended capability mode.

Table 6-3 lists the audio mixer control registers used by software written for Sound Blaster and other common audio peripherals. These registers are accessed by writing the index value to I/O port 2n4h and reading the value from or writing the value to I/O port 2n5h.

Table 6-3.
Compatibility Mode Audio Mixer Control Register Mapping

Index	Function	Index	Function
00h	Mixer Reset	22h	Master Volume
04h	Voice Volume	26h	FM Volume
0Ah	Mic Volume	28h	CD Volume
0Ch	ADC Recording Source [1]	2Eh	Line Volume
0Eh	Stereo/Mono Switch [1]	--	--

NOTE: Refer to OEM's ES1868 data sheet for detailed register descriptions.
[1] The filter functions used in Sound Blaster subsystems are not used in the audio subsystem.

The Extended Mode registers are listed in Table 6-4. Like the compatibility registers listed previously, these registers are accessed by writing the index value to I/O port 2n4h and reading the value from or writing the value to I/O port 2n5h. Extended mode offers better performance by providing more precise (higher bit resolution) control of audio levels and more control of audio processing.

Table 6-4.
Extended Mode Audio Mixer Control Register Mapping

Index	Function	Index	Function
14h	Voice Volume	60, 62h	Master Volume (Left, Right)
1Ah	Mic Volume	64h	Master Volume Control
1Ch	ADC (recording) Source	66h	Volume Int. Req. Clear
1Eh	Stereo/Mono Switch	74h	DMA Transfer(2nd) Count Reload (Low)
32h	Master Volume	76h	DMA Transfer (2nd) Count Reload (Hi)
36h	FM Volume	78h	2nd DMA Control 1
38h	CD Volume	7Ah	2nd DMA Control 2
3Eh	Line Volume	7Eh	Test Register

NOTE: Refer to OEM's ES1868 data sheet for detailed registers descriptions.

6.3.2.2 FM Synthesis Control

The FM synthesis logic is typically mapped at 388h-38Bh. A total of 243 registers in two banks are available. Accessing the registers is accomplished by first writing the index to register 388h (for bank 0) or 38Ah (for bank 1) followed by writing the data to either 389h or 38Bh (for bank 0 or bank 1 respectively). If a succeeding data byte is destined for the same location then the address need not be re-written. Location 388h can be read for FM synthesizer status. Table 6-5 lists the FM synthsizer control registers.

Table 6-5.
FM Synthesizer Control Register Mapping

Index	Bank 0 Function	Bank 1 Function
01h	Test - all 0s	Test - all 0s
02h	Timer 1	Not Used
03h	Timer 2	Not Used
04h	Timer Mask/Timer Start	4-Operator Configure
05h	Not Used	4-Operator Enable
08h	Key Scale (KSR) # Determiner	Not Used
20-35h	AM, Vib, EG Type, KSR, Mult.	Same as bank 0
40-55h	Key Scale Level, Tone Level	Same as bank 0
60-75h	Attack Rate, Decay Rate	Same as bank 0
80-95h	Sustain Level, Release Rate	Same as bank 0
A0-A8h	Frequency Number	Same as bank 0
B0-B8h	Key On, Block Octave, Frequency No.	Same as bank 0
BDh	Depth of Block Octave, Frequency No.	Not Used
C0-C8h	Stereo Left/Right, Feedback, Connection	Same as bank 0
E0-F5h	Wave Select	Same as bank 0

NOTE: Refer to OEM's ES1868 data sheet for detailed registers descriptions.
Abbreviations:

AM Amplitude Modulation (tremolo)
Vib Vibrato

6.4 SPECIFICATIONS

Table 6-6.
Audio Subsystem Specifications

Paramemter	Measurement
Sampling Rate	5.51 KHz to 44 KHz (prgmbl)
Maximum Input Voltage:	
Mic In	.125 Vp-p
Line In	1.4 Vrms
Impedance	
Mic In	1 K ohms (nom)
Line In	30 K ohms (nom)
Line Out	30 K ohms (nom)
Headphone Out	16 ohms (min)
Mic Preamp Gain	26 db
Volume Range	
Input	0 - 22.5 db
Output	-46.5 - +10 db
Frequency Response (speaker)	450 - 4000 Hz

This page is intentionally blank.

Chapter 7
POWER and SIGNAL DISTRIBUTION

7.1 INTRODUCTION

This chapter describes the power supply and method of general power and signal distribution in the Compaq Professional Workstation. Topics covered in this chapter include:

7.2 POWER SUPPLY ASSEMBLY

The power supply assembly is contained in a single unit that features a selectable input voltage: 90-135 VAC and 180-265 VAC. The power supply provides +3.5 VDC, +5 VDC, -5 VDC, +12 VDC, and -12 VDC, and is rated at 240 watts.

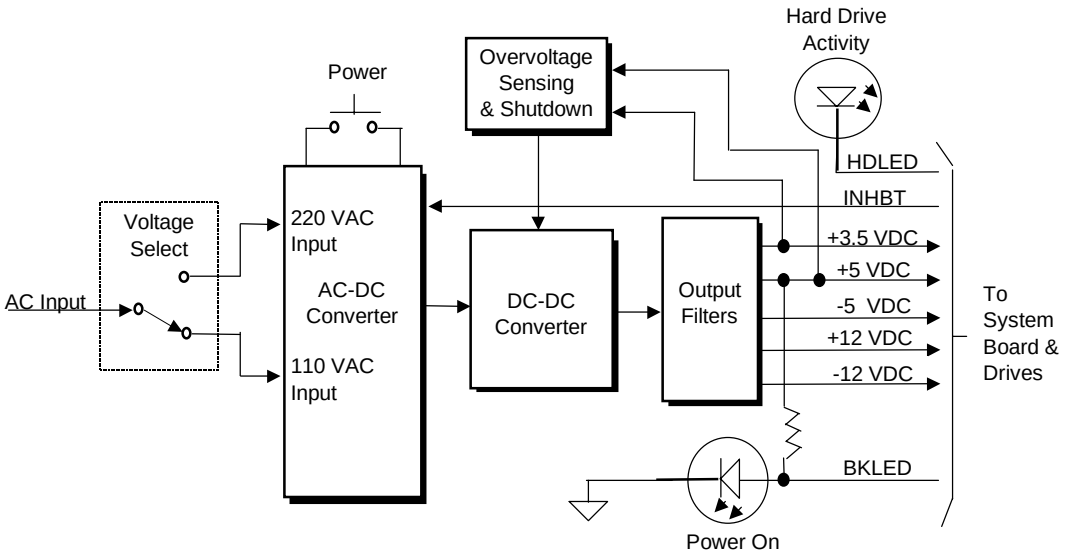


Figure 7–1. Power Supply Assembly, Block Diagram

A fault-detection circuit automatically shuts down the power supply until all faults are removed and the AC power switch is cycled (turned Off, then On). The minimum time period required to recycle the AC power and return to normal power supply operation is 10 seconds. Power supply faults that can trigger the protection circuitry include:

- Thermal overload - The protection circuit triggers if the power supply becomes too hot as a result of fan failure or a restriction of air flow.
- Overvoltage - The +5 VDC output will activate the overvoltage crowbar circuit that triggers the protection circuit when the output exceeds +5.60 VDC to +6.80 VDC. The +3.5 VDC output will activate the overvoltage crowbar circuit when the output is sensed to be in the +3.7 VDC to +5.0 VDC range.
- Short Circuit - The protection circuit triggers if any power supply output is shorted to ground or to another output. This function reduces shock or fire hazard

> **NOTE:** The minimum loading requirements for the power supply must be met at all times to ensure normal operation and to meet specifications.

The power LED is normally on in a steady state with the system on. When the system is in a low power condition the BKLED signal pulses the power LED causing it to blink at approximately a 1-Hz rate.

Table 7-1 shows the specifications for the power supply.

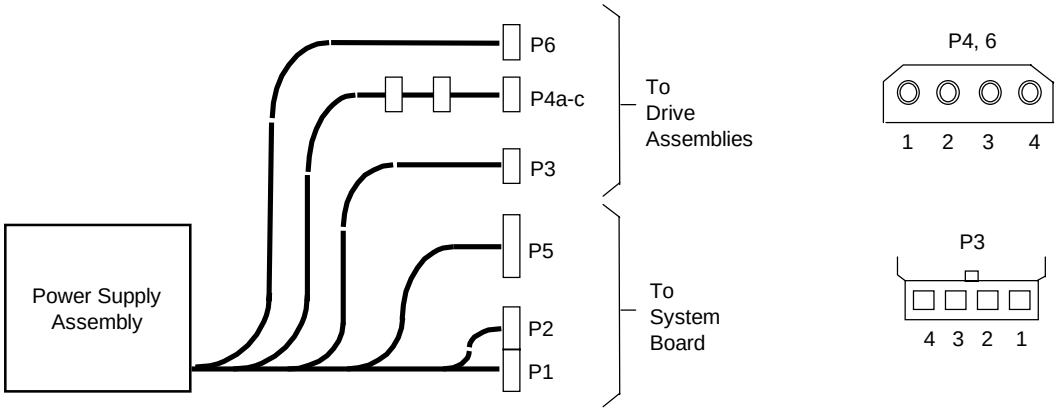
Table 7-1.
Power Supply Specifications

Parameter			
Input Line Voltage Range:			
110 VAC (North American) Setting:	90 - 132 VAC		
220 VAC Setting:	180-264 VAC		
Line Frequency	47 - 63 Hz		
Input Current Requirement:			
Cold Start:	< 80 A		
Hot Start:	< 80 A		
Maximum Steady State:	6.0 A		
Outputs:	Regulation	Max Current	Surge
+3.5 VDC	+/-1%	8.0 A	8.0 A
+5 VDC	+/-5 %	22.0 A	22.0 A
-5 VDC	+/-10 %	0.3 A	0.3 A
+12 VDC	+/-5 %	6.0 A	9.0 A
-12 VDC	+/-10 %	0.3 A	0.3 A
Maximum Output Ripple (all outputs)	1 % P/P of voltage		

7.3 POWER DISTRIBUTION

7.3.1 3.5/5/12 VDC DISTRIBUTION

The power supply assembly includes a multi-connector cable assembly that routes +3.5 VDC, +5 VDC, -5 VDC, +12 VC, and -12 VDC to the system board as well as to the individual drive assemblies.



Connector	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11
P1	PWRGD	+5	+12	-12	GND	GND					
P2	GND	GND	-5	+5	+5	+5					
P3	+5	GND	GND	+12							
P4a-c, P6	+12	GND	GND	+5							
P5	GND	GND	GND	+3.5	+3.5	+3.5RS	RSRTN	nc	INHBT	HDLED	BKLED

NOTE: All + and - values are VDC.
nc = not connected
RS = Remote sense
= not used

Figure 7–2. Power Cable Diagram

7.3.2 LOW VOLTAGE DISTRIBUTION

The system board used in this system include a provision for producing low voltages (i.e., voltages lower than 3.5 VDC) for reduced power modes and also for upgrade microprocessors that use lower voltages. Figure 7-3 shows a block diagram of these switching-type converters.

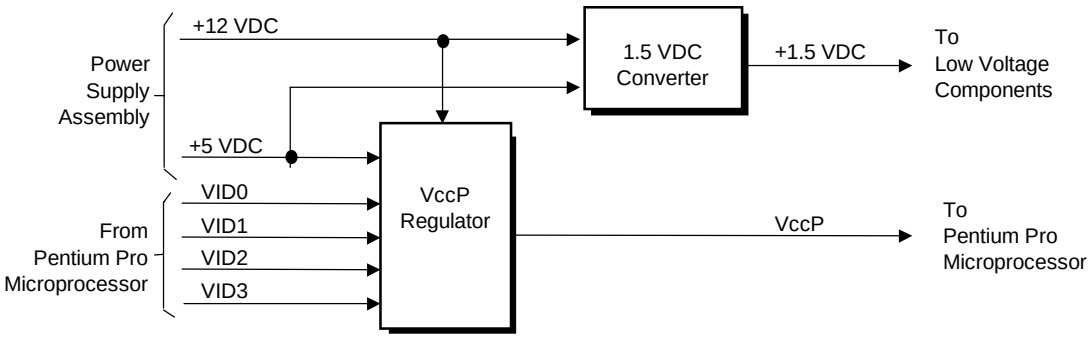


Figure 7–3. Low Voltage Power Converters, Block Diagram

The VccP regulator produces the VccP (Pentium Pro processor core) voltage according to the state of the VID3..0 signals from the Pentium Pro microprocessor. This allows automatic selection of the proper core voltage depending on the installed microprocessor component. The possible voltages available are listed as follows:

VID3..0	VccP	VID3..0	VccP
0000	3.5 VDC	1000	2.7 VDC
0001	3.4 VDC	1001	2.6 VDC
0010	3.3 VDC	1010	2.5 VDC
0011	3.2 VDC	1011	2.4 VDC
0100	3.1 VDC	1100	2.3 VDC
0101	3.0 VDC	1101	2.2 VDC
0110	2.9 VDC	1110	2.1 VDC
0111	2.8 VDC	1111	CPU not installed

7.4 SIGNAL DISTRIBUTION

Figure 7-4 shows general signal distribution between the main subassemblies of the system unit.

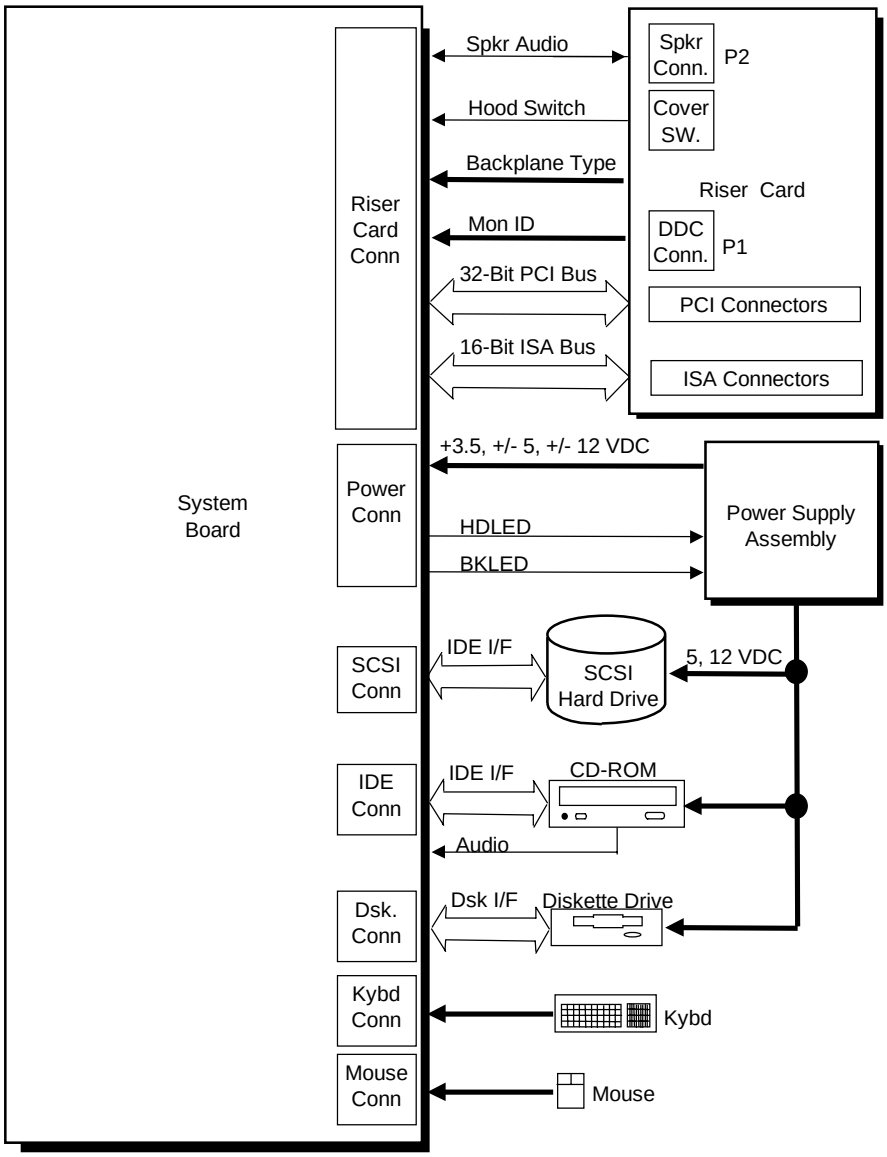


Figure 7–4. Signal Distribution Diagram

This page is intentionally blank.

Chapter 8
BIOS ROM

8.1 INTRODUCTION

The Basic Input/Output System (BIOS) of the computer is a collection of machine language programs stored as firmware in read-only memory (ROM). The BIOS ROM includes such functions as Power-On Self Test (POST), PCI device initialization, Plug ‘n Play and power management activities, and Setup. This chapter includes the following topics:

The firmware contained in the BIOS ROM supports the following operating systems:

- DOS 6.2
- Windows 3.1
- Windows for Workgroups 3.11
- Windows 95
- Windows NT 3.5
- OS/2 ver 2.1
- OS/2 Warp
- SCO Unix

The microprocessor accesses the BIOS ROM as a 128-KB block from E0000h to FFFFFh. The BIOS data is shadowed in a 64-KB block in the upper memory area. The BIOS segments are dynamically paged in and out of the 64-KB block as they are needed.

> **NOTE:** This section describes BIOS in general and highlights BIOS functions unique to this particular system. For detailed information regarding the BIOS, refer to the *Compaq Basic Input/Output System Technical Reference Guide.*

8.2 INITIALIZATION

Initialization occurs after power up and provides the following functions:

Bootstrap Processor Selection - In a multiprocessor system, one of the microprocessors must assume the bootstrap duties as the designated Bootstrap Processor (BSP). An algorithm is used within each microprocessor to set a flag (in CPU register APIC_BASE.BSP) indicating it to be the BSP. Essentially, the first processor to accomplish setting the flag "wins" to become the BSP. Physical position (socket number) does not figure into the BSP decision.

L1 Cache Configuration - In a multiprocessor system the BSP's L1 cache will be configured for write-through, otherwise the L1 cache will function as a write-back cache.

Microprocessor Identification - The CPUID instruction is executed to fetch the processor ID and revision, which is written into locations FFFE0h-FFFE2h as well as into extended CMOS.

P6 Patch Code Loading - Any patches required by the P6 microprocessor(s) are downloaded from the BIOS ROM into memory to be accessed with a Far call.

Memory Type Range Register Initialization - This procedure includes flushing the caches and programming the MMTR's for 0 to top-of-memory parameters.

Memory Controller Initialization - The 82441 memory controller is initialized in two stages. Stage 1 establishes the type of memory installed, sets DRAM timing, and maps memory to PCI space. Stage 2 initializes BDA memory variables to the sizes of base memory (stored at 0040:010Eh) and expansion memory (stored at 0040:0110h). After the parameters have been set, the PCI Configuration Space is disabled.

PCI/ISA Bridge Initialization - The PCI/ISA bridge function of the OSB ASIC is configured for such parameters as DEVSEL- timing (set to slowest PCI master), retry masking (enabled), SERR-/PERR-/NMI- acknowledge cycles (enabled), arbitration timing (8 PCICLKs), and PCI bus frequency (33 MHz). Minimum grant timing is typically set at 16 PCICLKs. The top-of-memory space, DMA/PCI mapping, and DCH mapping is dynamically configured during POST, as are the PCI interrupts. These parameters are loaded into PCI configuration space (refer to chapter 4), which is then disabled from further access.

AT Core Functions - The typical AT-type functions such as IRQ and DMA handling, and interval timer functions are initialized for compatibility with standard AT operations.

8.3 SETUP UTILITY

The Setup Utility (resident on the hard drive) displays the system's current configuration and allows the user to set the system parameters. The configuration parameters are stored in configuration memory described in section 4.8 "RTC/Configuration." A backup copy of configuration data is also saved in the boot block flash ROM. The user activates Setup by either pressing F1 during the boot sequence (while the cursor is located at the upper right corner of the display). The system reboots following changes made with the Set Up utility.

8.4 OVERVIEW OF COMPAQ-SPECIFIC BIOS FUNCTIONS

The BIOS for this system provides support for Compaq-specific INT 15 functions listed in Table 8-1.

Table 8-1.
Compaq-Specific BIOS Interrupts (INT15)

AX	Function	Mode
D820h	Read serial number	Real & Prot.
D821h	Write serial number	Real & Prot.
D822h	Read wellness data	16-bit
D823h	Write wellness data	16-bit
D824h	Get binary EV	16-bit
D825h	Set binary EV	16-bit
D826h	Get nth EV	16-bit
D8A0h	Read chassis serial number	32-bit
D8A2h	Read wellness data	32-bit
D8A3h	Write wellness data	32-bit
D8A4h	Get binary EV	32-bit
D8A5h	Set binary EV	32-bit
D8A6h	Get nth EV	32-bit
E400h	Get advanced system info	Real, 16-, & 32-bit Prot.
E480h	Set advanced system info	Real, 16-, & 32-bit Prot.
E800h	Get system ID	16-bit
E801h	Get super extended mem. info	
E804h	Install soft drive types	
E805h	Set language type	
E806h	Get language type	
E807h	Get System Information Table	Real, 16-, & 32-bit Prot.
E80Bh	Boot diagnostic portion	
E80Ch	Unprotect/protect ROM image	
E813h	Get EDID/DDC information	Real, 16-, & 32-bit Prot.
E814h	Get system board revision	Real, 16-, & 32-bit Prot.
E816h	Temperature status	
E817h	Get drive attribute	Real
E818h	Get drive off-line test	Real
E819h	Read chassis serial number	Real, 16-, & 32-bit Prot.
E81Ah	Write chassis serial number	Real
E81Bh	Get drive threshold	Real
E81Ch	Write Client Management log	Real, 16-, & 32-bit Prot.
E81Dh	Read Client Management log	Real, 16-, & 32-bit Prot.
E81Eh	Get hard drive ID	Real
E821h	Write/read diag. CMOS bytes	
E822h	Disable/enable flash ROM	
E823h	Read/write CMOS	Real, 16-, & 32-bit Prot.
E827h	Read/Write DIMM EEPROM	Real, 16-, & 32-bit Prot.
E828h	Inhibit Power Supply Support	Real, 16-, & 32-bit Prot.
E830h	Get product name	
E841h	Set system defaults	16-bit
E880h	Get system ID	32-bit

Functions that are not supported will return the appropriate settings (AH=86h, CF=1) if called. All 32-bit protected mode calls are accessed by using the BIOS32 Service Directory.

8.5 NETWORK MANAGEMENT SUPPORT

This system includes BIOS and hardware support for network management tools such as Compaq Insight Manager. Specific BIOS calls can be used by software to access information stored in System Information Tables (SIT) regarding the operation and health status of the system unit. Hardware components that support network management software are referred to as client management logic and include portions of the OSB ASIC, the 87306 I/O controller, and serial scan chain logic.

Client management functions handled by the OSB are controlled by indexed registers access through I/O ports 0C50h (index) and 0C51h (data) as well as the OSB's GPIO port 0C52h.

Table 8-1.
Client Management Indexed Registers (OSB)

Index	Register
00h	ID Register
02h	Temperature Status / Clear
03h	Temperature Interrupt and SMI Enable
12h	I^2C I/F Control (GPOC <3..0>)
80h	Super I/O Security Control
81h	Super I/O Index Address Low
82h	Super I/O Index Address High
83h	Super I/O Index Data
84h	Super I/O Data Address Low
85h	Super I/O Data Address High
86h	Super I/O Write Block Register 0
87h	Super I/O Write Block Register 1
88h	Super I/O Write Block Register 2
89h	Super I/O Write Block Register 3

Disabled

Client management functions handled by the 87306 are accessed through that component's GPIO ports 78h and 79h and associated serial scan chain (SSC) logic. This setup allows several client management functions to share IRQ13, which is commonly used by management software.

I/O Port 078h, 87306 GPIO-1 Register (SSC Reg. 1), R/W

Bit	Function
7	Serial Scan Chain Clock. This bit is toggled low to enable 8 bits (a byte) to be shifted into a register to be read at port 79h.
6	Serial Scan Chain Load. This bit is toggled low (before accessing bit <7>) to read the scan chain from the beginning.
5	Disable Hot Spare Boot Timer: 0 = Disable, 1 = Enabled, allowing timer to expire, forcing the HSB sequence to the next processor.
4	Correctable ECC Error Generation To IRQ13: 0 = Disable, 1 = Enable
3	Fan 2 Error Control: 0 = Disable, 1 = Enable
2	Fan 1 Error Control: 0 = Disable, 1 = Enable
1	Temperature Caution 2: 0 = Enable, 1 = Disable
0	Temperature Caution 2: 0 = Enable, 1 = Disable

I/O Port 079h, 87306 GPIO-2 Register (SSC Reg. 2), RO

Bit	Function
7..0	Serial Scan Chain Data

The serial scan chain can be accessed by software using the following procedure:

1. Write to I/O port 78h, clearing bit <6> (to 0). Write again to set bit <6> (to 1), resulting in loading the serial scan chain logic with the most recent data.
2. Write to I/O port 78h, clearing bit <7> (to 0). Write again to set bit <7> (to 1), causing a counter to generate 8 clocks at 20 MHz. The clock pulses shift the first byte of data from the SSC logic to the GPIO-2 register.
3. Read I/O port 79h.
4. Repeats steps 2 and 3 until the desired byte is read or the end of data is reached.

The serial scan chain data format is as follows:

Serial Scan Chain Data (read successively @ I/O port 79h)

Byte	Bit	Function
0	7-0	Board ID
1	7-0	Auto REV
2		Information Byte #1
	7	CFG_INTR- (switch 6 of SW1)
	6	CFG_IGNNE- (switch 5 of SW1)
	5	CFG_A20M (switch 4 of SW1)
	4	CFG_NMI (switch 3 of SW1)
	3	Riser 1 Card Type
	2	Riser 2 Card Type
	1	Fan Failure
	0	Temperature Caution
3		Information Byte #2
	7-3	Reserved
	1	IERRB (CPUB had an internal error)
	0	IERRA (CPUA had an internal error)

8.5.1 SYSTEM IDENTIFICATION

The INT 15, AX=E800h BIOS function can be used to identify the system board. The system ID will be returned in the BX register as follows:

System	System ID
Professional Workstation	02E8h

The INT 15 AX=E800h BIOS function points to the System Information Table (SIT). The SIT is a comprehensive list of fixed configuration information. Bytes 2 and 3 of SIT record 06h are the low and high order bytes (respectively) of the decimal value of the processor speed. Refer to the *Compaq Basic Input/Output System (BIOS) Technical Reference Guide* for more information on the SIT.

8.5.2 SECURITY PROTECTION

The security-related functions provided by the 87306 are protected by Client Management (CM) logic. Network management software can configure the CM logic to block access to the following 87306 functions:

- Diskette drive disable/write disable
- Serial port disable
- Parallel port disable
- Administrator password entry
- Power-On password entry

Network management software can access indexed CM logic registers (index 81h-89h, accessible through ports C50h and C51h) for blocking control of 87306 functions. In blocking 87306 functions, the CM logic monitors ISA I/O cycles and can detect, through index-matching, when an attempt is made to access a function provided by the 87306. If the CM logic has been set to block access, then the AEN or IOWC- signal, both which the CM logic provides to the 87306, is disabled, effectively inhibiting the I/O access.

8.5.3 HOOD REMOVAL SENSOR

This system includes a hood removal indication function. The system can, upon power-up, notify the user if the computer cover (hood) has been removed. The sensor consists of a plunger switch mounted on the backplane (riser card). When the cover is removed, the switch is activated and the battery-backed logic places a high at the OSB's GPIO port 0C52h. This bit will remain set (whether or not the cover is replaced) until the system is powered up and the user completes the boot sequence successfully, at which time the hood alarm bit (<4>) will be cleared. Through Setup, the user can set this function to one of three levels of support for a "hood removed" condition:

Level 0 - Hood removal indication is essentially disabled at this level. During POST, Bit <4> is cleared and no other action is taken by BIOS.

Level 1 - During POST the "The computer's cover has been removed since the last system start up" message is displayed and time stamps in CMOS and SIT are updated.

Level 2 - During POST the "The computer's cover has been removed since the last system start up" message is displayed, time stamps in CMOS and SIT are updated, and user is prompted for administrator password.

> **NOTE:** If the user invokes Setup through F10 the administrator password is not requested again.

The System Information Table (SIT) record format for the hood removal time stamp is as follows:

System Information Table, System Hood Removal Record (13h)

Byte	Bit	Function
00h	7-0	Record ID (13h)
01h	7-0	Length of record
02-05h		Hood Removal Time Stamp:
	31-25	Year (0-99, representing 1996-2095)
	24-21	Month (1-12)
	20-16	Day (1-31)
	15-11	Hours (0-23)
	10-5	Minutes (0-59)
	4-0	Seconds (0-59)
06h	7-0	Hood Removal Support Enable/Disable Byte Offset (0-255)
07h		Hood Removal Support Enable/Disable Bit Location:
	7..4	CMOS Type (0011b, use INT 15h for flat model CMOS)
	3..0	Bit location (0000b)
08h	7..0	Hood Removal NOBOOT Enable/Disable Byte Offset (0-255)
09h		Hood Removal NOBOOT Enable/Disable Bit Location:
	7..4	CMOS Type (0011b, use INT 15h for flat model CMOS)
	3..0	Bit location (0001b)

8.5.4 DIMM SUPPORT FUNCTION

The BIOS includes DIMM support consisting of the following:

- Access control with the serial (I^2C) EEPROM of the DIMM
- Runtime information on ECC-correctable single bit errors
- POST message if ECC-correctable errors are detectable during POST memory test

DIMMs with 128 bytes of EEPROM can be used although 256-byte EEPROM DIMMs are recommended for full support of Compaq intelligent manageability features. The following BIOS functions have been added to provide specific support of DIMMs:

INT 15h AX=E827h, BH=00h; Read DIMM EEPROM

ENTRY: AX = E827h
BH = 00h
BL = DIMM No. (0-3)
CX = Number of bytes to read
DX = Offset of first byte to read
DS: (E) SI = Address of data buffer to receive data

RETURN: CX = No. of bytes read
CF = 0 (Success)
AH = 0
1 (Failure)
AH = Error Code:
01h, No DIMM EEPROM or socket empty
02h, Boundary error (offset or no. of bytes to read exc. cap)
86h, Not supported

INT 15h AX=E827h, BH=01h; Write DIMM EEPROM

ENTRY: AX = E827h
BH = 01h
BL = DIMM No. (0-3)
CX = Number of bytes to be written
DX = Offset of first byte to be written
DS: (E) SI = Address of data buffer holding write data

RETURN: CX = No. of bytes written
CF = 0 (Success)
AH = 0
1 (Failure)
AH = Error Code:
01h, No DIMM EEPROM or socket empty
02h, Boundary error (offset or no. of bytes to read exc. cap)
86h, Not supported

INT 15h AX=E827h, BH=02h; Get ECC-Corrected Single Bit Error Status

ENTRY: AX = E827h
BH = 02h

RETURN: CF = 0 (Success)
AH = 0
BX = 0000h (if no single bit ECC corrected error has occurred)
bit <0>, Error occurred on DIMM/SIMM pair 0
bit <1>, Error occurred on DIMM/SIMM pair 1
bit <2>, Error occurred on DIMM/SIMM pair 2
bit <3>, Error occurred on DIMM/SIMM pair 3
CF = 1 (Failure)
AH = 86h (Not supported)

The POST memory test checks for ECC-corrected single bit errors after each 64K of memory tested in a similar fashion as is done with parity. The errors are counted on a per DIMM basis and notify the user at the end of the test in the following format:

"207-ECC Corrected Single Bit Errors in DIMM/SIMM Pair(s) x,x…"

x = DIMM/SIMM pair numbers 0 through 3.

8.5.5 DRIVE FAULT PREDICTION

The Compaq BIOS provides direct Drive Fault Prediction support for both IDE- and SCSI-type hard drives. This feature is provided through several INT 15 BIOS calls listed in Table 8-1. If BIOS returns data indicating an imminent drive failure, the Compaq BIOS issues the following message:

"1721-Intellisafe SCSI Hard Drive detects imminent failure"

Diagnostic software can then be run to evaluate the problem.

8.5.6 MEDIA WRITE PROTECTION

The write-protect function that determines diskette write control is extended to cover all drives that use removable read/write media (i.e., if diskette write protect is invoked, then any diskette drive, power drive (SCSI and/or ATAPI), and floptical drive installed will be inaccessible for (protected from) writes). Client management software should check the following bytes of SIT record 07h for the location and access method for this bit:

System Information Table, Peripheral and Input Device Record (07h) (partial listing)

Byte	Bit	Function
1Fh	7-0	Removable Read/Write Media Write Protect Enable Byte Offset (0-255)
20h		Removable Read/Write Media Write Protect Enable Bit Location:
	7..4	CMOS Type: 0000 = CMOS 0001 = High CMOS 0010 = NVRAM 0011 = Flat model NVRAM
	3..0	Bit Location: 0000 = Bit 0 0100 = Bit 4 0001 = Bit 1 0101 = Bit 5 0010 = Bit 2 0110 = Bit 6 0011 = Bit 3 0111 = Bit 7

8.5.7 POWER SWITCH INHIBIT FUNCTION

The power switch of the system unit can be disconnected from and reconnected to the power supply by software through the following BIOS function:

INT 15h AX=E828h, BH=00h; Disconnect On/Off Switch From Power Supply

ENTRY: AX = E828h
BH = 00h

RETURN: CF = 0 (Success)
AH = 0
CF = 1 (Failure)
AH = 86h (Not supported)

INT 15h AX=E828h, BH=01h; Reconnect On/Off Switch To Power Supply

ENTRY: AX = E828h
BH = 01h

RETURN: CF = 0 (Success)
AH = 0
CF = 1 (Failure)
AH = 86h (Not supported)

NOTE: If the On/Off switch has been pressed while it was disconnected, a call to reconnect the switch will result in a power down of the system.

8.5.8 TEMPERATURE SENSOR

A temperature sensor component is mounted in the cavity of the microprocessor socket. This sensor component detects when the microprocessor has reached a programmed temperature level and initiates appropriate action. The LM75 sensor is programmed by BIOS for a level for initiating a caution to the user. Detection of a caution temperature level results in asserting IRQ13 through the serial scan chain logic described earlier.

The sensing feature is set up by BIOS during POST through an I^2C-type interface. Different microprocessor steps will have unique operating temperature optimums so that a processor upgrade may require that the BIOS be upgraded as well. The caution level is typically set at 60° C.

8.5.9 CHASSIS ID

The chassis identification number is held in the EEPROM that stores CMOS data including the system serial number and asset tag. The EEPROM is accessed through an I^2C interface. The BIOS ROM function INT 15 AX=E819h is used to retrieve the chassis ID number.

8.5.10 AUTO REV DATA

The system board includes byte locations used for holding the Auto REV value. This data can be checked by firmware or software for system definition. The auto REV data is checked by reading the serial scan chain data at GPIO port 2 (I/O 79h) as described earlier.

8.5.11 HOT SPARE BOOT

This system includes a Hot Spare Boot (HSB) function that, in a multiple-processor system, detects the failure of one processor and, rebooting the system automatically, switches bootstrapping responsibilities over to the second microprocessor. A typical case would be an internal error occurring within microprocessor P1 (such as a micro code or cache parity error) resulting in an NMI. The NMI handler would use the serial scan chain to check the source of the NMI (by checking the IERRA/IERRB bits), log the bad CPU, and shutdown the system. During reset, the BIOS would detect the failed processor from CMOS and would not toggle the disable HSB timer bit in SSCR1. The HSB timer would then be allowed to expire and the system would place the failed microprocessor in a tri-state condition and reset the system. When the Host/PCI bridge controller senses that P1 is not responding with the BREQ signals then P2 is assumed to be the BSP with the active local APIC and the boot sequence is completed. The failed microprocessor is left tri-stated and unused.

8.6 POWER MANAGEMENT SUPPORT

This system includes specific BIOS and hardware support for power management to reduce energy consumption. In addition, the microprocessor's internal mechanism for power reduction (STPCLK) is available for power reduction use.

Power management functions are configured typically through Setup. With power management enabled, inactivity timer countdown is monitored. When an inactivity timer times out due to inactivity of enabled system events, an SMI to the microprocessor is generated to invoke the SMI handler. The SMI handler works with the APM driver, APM BIOS, and/or power management software to take appropriate action based on which inactivity timer timed out. This action can include spinning down the hard drive, powering down the display monitor, or powering down certain components.

The system remains in a reduced mode until an interrupt generated by a certain activity (identified as a wakeup event) is detected, after which the microprocessor brings the system out of the reduced power mode to support the activity.

The following actions can be configured independently as system events (that prevent the system from entering a reduced power mode) and wakeup events (that bring the system out of reduced power mode).

- Advanced Power Management (APM) Control register writes (software event)
- External SMI
- Fast Off timer
- Programmed I/O activity (range programmable)
- IRQ1 (keyboard)
- IRQ3 (COM1, COM3, mouse)
- IRQ4 (COM2, COM4, mouse)
- IRQ8 (RTC alarm)
- IRQ12 (PS/2 mouse)

The system and wakeup events are programmed through the OSB ASIC's indexed power management registers accessed through I/O ports 0CD6h (index) and 0CD7h (data). The I/O ports used for APM communication with the SMI handler are I/O ports 0B2h (Control) and 0B3h (Status).

8.6.1 HARD DRIVE SPINDOWN CONTROL

For IDE hard drives, the timeout parameter stored in the SIT record 04h and indexed through CMOS location 2Ah (bits <4..0>) represents the period of hard drive inactivity required to elapse before the IDE hard drive is allowed to spin down. The timeout value is downloaded from CMOS to a timer on the hard drive. The timeout period can be set to values of 0 (timeout disabled) to 75 minutes in 5-minute increments. In the case of a SCSI hard drive, a timeout will result in the issuing of the STOP UNIT command on the SCSI bus and BIOS will attempt to spin-down the SCSI hard drive. A timed-out and spun-down hard drive will automatically spin back up upon the next drive access. It is normal for the user to detect a certain amount of access latency in this situation.

8.6.2 MONITOR CONTROL

This system provides monitor power control for monitors that conform to the VESA display power management signaling protocol. This protocol defines different power consumption conditions and uses the HSYNC and VSYNC signals to select a monitor's power condition. Table 8-3 lists the monitor power conditions.

Table 8-3.
Monitor Power Management Conditions

HSYNC	VSYNC	Power Mode	Description
Active	Active	On	Monitor is completely powered up. If activated, the inactivity counter counts down during system inactivity and if allowed to tiemout, generates an SMI to initiate the Suspend mode.
Active	Inactive	Suspend	Monitor's high voltage section is turned off and CRT heater (filament) voltage is reduced from 6.6 to 4.4 VDC. The Off mode inactivity timer counts down from the preset value and if allowed to timeout, another SMI is generated and serviced, resulting in the monitor being placed into the Off mode. Wake up from Suspend mode is typically a few seconds.
Inactive	Inactive	Off	Monitor's high voltage section and heater circuitry is turned off. Wake up from Off mode is a little longer than from Suspend.

The timeout parameter set in the SIT record 03h and indexed at CMOS location 2Ch (bits <4..0>) represents the period of system I/O inactivity required to elapse before the monitor is placed into Suspend mode.

A separate timer function (enabled through CMOS location 1Fh, bit <1>) can be enabled to place the monitor into the Off mode after 45 minutes of being in Suspend mode.

8.6.3 MICROPROCESSOR CONTROL

The Pentium Pro microprocessor can be configured to enter a low power condition. By setting bit <26> of the microprocessor's Power-On Configuration Model Specific Register (EBL_CR_POWERON @ 2Ah), the Pentium Pro will turn off it's core clocks when a HLT (Halt) instruction is received. The STPCLK function is also supported by this system.

8.7 SECURITY FEATURE SUPPORT

8.7.1 FLASH ROM WRITE PROTECTION

The system BIOS firmware is contained in a flash ROM device that can be re-written with updated code if necessary. The ROM is write-protected with a Black Box security feature. The Black Box feature uses the Administrator password to protect against unauthorized writes to the flash ROM. During the boot sequence, the BIOS checks for the presence of the ROMPAQ diskette. If ROMPAQ is detected and the password is locked into the Black Box with the Protect Resources command, an Access Resources command followed by Administrator password entry and warm boot must occur before the ROM can be flashed. If the Permanently Lock Resources command has been invoked, the power must be cycled before the ROM can be flashed.

8.7.2 POWER ON PASSWORD

When enabled, the user is prompted to enter the password during POST. If an incorrect entry is made, the system halts and does not boot. The Power-On password is stored in eight bytes at configuration memory locations 37h-3Fh. These locations are physically located within the 87306. At the time a new password is written into 37h-3Fh, the password is also written into Black Box* logic. The Black Box logic is used for power-on password protection support instead of the port 92 sequence used on other systems. The Black Box logic prevents inadvertent or unauthorized access to the password bytes of the 87306 by monitoring I/O ports 70/71h for access to the 37h-3Fh CMOS range and inhibiting the AEN signal to the 87306 if such access is detected. Slot 1 of the Black Box logic can be written to at runtime, allowing the user to change the power on password without cycling power and going through the F10 method. The Black Box password in slot 1 cannot be read.

The power-on password function can be disabled by setting DIP SW1 position 1 to on (closed).

8.7.3 ADMINISTRATOR PASSWORD

The administrator password is stored in eight bytes at configuration memory locations 78h-7Fh. If the administrator password function is enabled, the user is prompted to enter the password before running F10-Setup or before booting from a ROMPAQ diskette. If an incorrect entry is made, the system halts and does not boot. The administrator password is also stored in slot 0 of the Black Box* logic. Black Box logic prevents inadvertent or unauthorized writing to the Flash ROM by acting as the sentry for the administrator password.

* Black Box logic is Compaq-proprietary and controlled exclusively through the BIOS ROM.

8.7.4 QUICKLOCK/QUICKBLANK

The QuickLock feature allows, if enabled in F10-Setup through CMOS location 13h bit <2>, the user to lock the keyboard and mouse by invoking the **Ctrl-Alt-L** keystrokes. This initiates an SMI and the SMI handler then takes the appropriate action. If the QuickBlank feature is enabled at that time then the screen will be blanked as well.

> **NOTE:** Although the SMI is used for initiating QuickLock/QuickBlank functions, these functions are not considered power management features.

8.7.5 DISKETTE DRIVE CONTROL

The diskette drive is locked out of the boot process if CMOS location 13h bit <3> is set. In this instance the BIOS will only boot from the hard drive. In addition, no writes to the diskette drive will be allowed if I/O port 78h bit <7> is cleared (the power-up default is a "1"). The diskette drive is completely disabled if bit <3> of the FER register (399.00h) is cleared. Access to this function can be blocked by BIOS' Client Management discussed previously.

8.7.6 SERIAL/PARALLEL PORT DISABLE

The serial and parallel ports can be disabled through bits <1> and <0> respectively of the FER register (399.00h) as follows:

Bit = 1, port is enabled
Bit = 0, port is disabled.

Access to this function can be blocked by BIOS' Client Management discussed previously.

8.8 PnP SUPPORT

The BIOS includes Plug 'n Play (PnP) support for PnP version 1.0A. Table 8-1 shows the PnP functions supported:

Table 8-1.
PnP BIOS Functions

Function	Register
00h	Get number of system device nodes
01h	Get system device node
02h	Set system device node
03h	Get event
04h	Send message

8.9 RESET ROUTINE

There are two types of reset events: hard and soft. Traditionally, a hard reset is generated only during power-up and produced only by the circuitry driving the PWRGOOD signal. However, the 82371 controller has the ability to generate a hard reset through software. First, a one (1) must be written to bit <1> of I/O port 0CF9h. A one must then be written to bit 2 of the same I/O port. These two steps cause the PIIX-3 to create a hard reset by asserting its CPURST#, PCIRST#, and RSTDRV outputs for at least 1 ms. After the reset, the PIIX-3 automatically clears bit 2 of I/O port 0CF9h.

Appendix A
ERROR MESSAGES AND CODES

A.1 INTRODUCTION

This appendix lists the error codes and a brief description of the probable cause of the error. Note that not all errors listed in this appendix may be applicable to a particular system depending on the model and/or configuration.

A.2 POWER-ON MESSAGES

Table A-1.
Power-On Messages

Message	Beeps	Probable Cause
CMOS Time and Date Not Set	(None)	Invalid time or date
(none)	2 short	Power-On successful
Run Setup	(None)	Any failure

A.3 BEEP CODE MESSAGES

Table A-2.
Beep Code Messages

Beeps	Error	Probable Cause
1	Refresh Failure	Faulty memory refresh circuitry.
3	Base 64-KB Memory Failure	Memory failure in first 64-KB.
4	Timer Not Operational	Same as above or timer 1 not functioning.
5	Processor Error	CPU-generated error.
6	8042 Gate A20 Failure	Keyboard controller faulty, BIOS cannot switch to protected mode.
7	Processor Exception Interrupt Error	CPU-generated exception interrupt.
8	Display Memory R/W Error	Missing graphics/video adapter or faulty video memory (system still boots).
9	ROM Checksum Error	Checksum value does not match value in BIOS.
10	CMOS Shutdown Register R/W Error	CMOS RAM shutdown register failure.
11	Cache Error	Faulty cache.

A.4 POWER-ON SELF TEST (POST) MESSAGES

Table A-3.
Power-On Self Test (POST) Messages

Error Message	Probable Cause
Bad PnP Serial ID Checksum	Serial ID checksum of PnP card was invalid.
Address Lines Short!	Error in address decoding circuitry on system board.
Cache Memory Failure, Do Not Enable Cache!	Defective cache memory, CPU has failed.
CMOS Battery Failed	Low RTC/CMOS battery
CMOS Checksum Invalid	Previous and current checksum value mismatch.
CMOS System Options Not Set	Corrupt or non-existant CMOS values.
CMOS Display Type Mismatch	Graphics/video type in CMOS does not match type detected by BIOS.
CMOS Memory Size Mismatch	Memory amount detected does not match value stored in CMOS.
CMOS Time and Date Not Set	Time and date are invalid.
Diskette Boot Failure	Boot disk in drive A: is corrupt.
DMA Bus Timeout	Bus driven by device for more than 7.8 us
DMA Controller Error	Error in one or both DMA controllers.
Drive Not Ready Error	BIOS cannot access the diskette drive.
Diskette Drive Controller Failure	BIOS cannot communicate with diskette drive controller.
Diskette Drive Controller Resource Conflict	Diskette drive controller has requested a resource already in use.
Diskette Drive A: Failure	BIOS cannot access drive A:.
Diskette Drive B: Failure	BIOS cannot access drive B:
Gate A20 Failure	Gate A20 of keyboard controller not working.
Invalid Boot Diskette	BIOS can read but cannot boot system from drive A:.
Keyboard Controller Error	Keyboard controller failure.
Keyboard is Locked…Please Unlock It	Locked keyboard.
Keyboard Stuck Key Detected	Key pressed down.
Master DMA Controller Error	Error exists in master DMA controller.
Master Interrupt Controller Error	Master interrupt controller failure.
Memory Size Decreased	Amount of memory detected is less than stated value in CMOS.
NVRAM Checksum Error, NVRAM Cleared	ESCD data was re-initialized due to NVRAM checksum error.
NVRAM Cleared By Jumper	NVRAM has been cleared by removal of jumper.
NVRAM Data Invalid, NVRAM Cleared	Invalid entry in ESCD.
Off Board Parity Error Addr. (HEX) = X	Parity error occurred in expansion memory, x= address of error.
Parallel Port Resource Conflict	Parallel port has requested a resource already in use.
PCI Error Log is Full	PCI conflict error limit (15) has been reached.
PCI I/O Port Conflict	Two devices requested the same resource.
PCI Memory Conflict	Two devices requested the same resource.
Primary Boot Device Not Found	Designated primary boot device could not be found.
Primary IDE Cntrl. Resource Conflict	Primary IDE controller requested a resource already in use.
Primary Input Device Not Found	Designated primary input device could not be found.
Secondary IDE Controller Resource	Secondary IDE controller has requested a resource already in use.
Serial Port 1 Resource Conflict	Serial port 1 requested a resource already in use.
Serial Port 2 Resource Conflict	Serial port 2 requested a resource already in use.
Slave DMA Controller Error	Error exists in slave DMA controller.
Slave Interrupt Controller Error	Slave interrupt controller failure.
Static Device Resource Conflict	A non-PnP ISA card has requested a resource already in use.
System Board Device Resource Conflict	A non-PnP ISA card has requested a resource already in use.
System Memory Size Mismatch	Amount of memory detected on system board is different from amount indicated in CMOS.

NOTE:
PCI and PnP messages are displayed with bus, device, and function information.

A.5 PROCESSOR ERROR MESSAGES (1xx-xx)

Table A-4.
Processor Error Messages

Message	Probable Cause	Message	Probable Cause
101-01	CPU test failed	105-08	Port 61 bit <1> not at one
101-02	32-bit CPU test failed	105-09	Port 61 bit <0> not at one
101-91..94	Multiplication test failed	105-10	Port 61 I/O test failed
102-01	FPU initial sts. word incorrect	105-11	Port 61 bit <7> not at zero
102-02	FPU initial cntrl. Word incorrect	105-12	Port 61 bit <2> not at zero
102-03	FPU tag word not all ones	105-13	No interrupt generated by failsafe timer
102-04	FPU tag word not all zeros	105-14	NMI not triggered by failsafe timer
102-05	FPU exchange command failed	106-01	Keyboard controller test failed
102-06	FPU masked exception error	107-01	CMOS RAM test failed
102-07	FPU unmasked exception error	108-02	CMOS interrupt test failed
102-08	FPU wrong mask status bit set	108-03	CMOS not properly initialized (interrupt test)
102-09	FPU unable to store real number	109-01	CMOS clock load data test failed
102-10	FPU real number calc test failed	109-02	CMOS clock rollover test failed
102-11	FPU speed test failed	109-03	CMOS not properly initialized (clock test)
102-12	FPU pattern test failed	110-01	Programmable timer load data test failed
102-15	FPU is inoperative or not present	110-02	Programmable timer dynamic test failed
102-16	Weitek not responding	110-03	Program timer 2 load data test failed
102-17	Weitek failed register trnsfr. Test	111-01	Refresh detect test failed
102-18	Weitek failed arithemetic ops test	112-01	Speed test Slow mode out of range
102-19	Weitek failed data conv. Test	112-02	Speed test Mixed mode out of range
102-20	Weitek failed interrupt test	112-03	Speed test Fast mode out of range
102-21	Weitek failed speed test	112-04	Speed test unable to enter Slow mode
103-01	DMA page registers test failed	112-05	Speed test unable to enter Mixed mode
103-02	DMA byte controller test failed	112-06	Speed test unable to enter Fast mode
103-03	DMA word controller test failed	112-07	Speed test system error
104-01	Master int. cntlr. test fialed	112-08	Unable to enter Auto mode in speed test
104-02	Slave int. cntlr. test failed	112-09	Unable to enter High mode in speed test
104-03	Int. cntlr. SW RTC inoperative	112-10	Speed test High mode out of range
105-01	Port 61 bit <6> not at zero	112-11	Speed test Auto mode out of range
105-02	Port 61 bit <5> not at zero	112-12	Speed test variable speed mode inoperative
105-03	Port 61 bit <3> not at zero	113-01	Protected mode test failed
105-04	Port 61 bit <1> not at zero	114-01	Speaker test failed
105-05	Port 61 bit <0> not at zero	116-xx	Way 0 read/write test failed
105-06	Port 61 bit <5> not at one	199-00	Installed devices test failed
105-07	Port 61 bit <3> not at one	--	--

A.6 MEMORY ERROR MESSAGES (2xx-xx)

Table A-5.
Memory Error Messages

Message	Probable Cause
200-04	Real memory size changed
200-05	Extended memory size changed
200-06	Invalid memory configuration
200-07	Extended memory size changed
200-08	CLIM memory size changed
201-01	Memory machine ID test failed
202-01	Memory system ROM checksum failed
202-02	Failed RAM/ROM map test
202-03	Failed RAM/ROM protect test
203-01	Memory read/write test failed
203-02	Error while saving block in read/write test
203-03	Error while restoring block in read/write test
204-01	Memory address test failed
204-02	Error while saving block in address test
204-03	Error while restoring block in address test
204-04	A20 address test failed
204-05	Page hit address test failed
205-01	Walking I/O test failed
205-02	Error while saving block in walking I/O test
205-03	Error while restoring block in walking I/O test
206-xx	Increment pattern test failed
210-01	Memory increment pattern test
210-02	Error while saving memory during increment pattern test
210-03	Error while restoring memory during increment pattern test
211-01	Memory random pattern test
211-02	Error while saving memory during random memory pattern test
211-03	Error while restoring memory during random memory pattern test
214-xx	Noise test failed
215-xx	Random address test

A.7 KEYBOARD ERROR MESSAGES (30x-xx)

Table A-6.
Keyboard Error Messages

Message	Probable Cause	Message	Probable Cause
300-xx	Failed ID test	303-05	LED test, LED command test failed
301-01	Kybd short test, 8042 self-test failed	303-06	LED test, LED command test failed
301-02	Kybd short test, interface test failed	303-07	LED test, LED command test failed
301-03	Kybd short test, echo test failed	303-08	LED test, command byte restore test failed
301-04	Kybd short test, kybd reset failed	303-09	LED test, LEDs failed to light
301-05	Kybd short test, kybd reset failed	304-01	Keyboard repeat key test failed
302-xx	Failed individual key test	304-02	Unable to enter mode 3
302-01	Kybd long test failed	304-03	Incorrect scan code from keyboard
303-01	LED test, 8042 self-test failed	304-04	No Make code observed
303-02	LED test, reset test failed	304-05	Cannot /disable repeat key feature
303-03	LED test, reset failed	304-06	Unable to return to Normal mode
303-04	LED test, LED command test failed	--	--

A.8 PRINTER ERROR MESSAGES (4xx-xx)

Table A-7.
Printer Error Messages

Message	Probable Cause	Message	Probable Cause
401-01	Printer failed or not connected	402-10	Interrupt test and control reg. failed
402-01	Printer data register failed	402-11	Interrupt test, data/cntrl. reg. failed
402-02	Printer control register failed	402-12	Interrupt test and loopback test failed
402-03	Data and control registers failed	402-13	Int. test, LpBk. test., and data register failed
402-04	Loopback test failed	402-14	Int. test, LpBk. test., and cntrl. register failed
402-05	Loopback test and data reg. failed	402-15	Int. test, LpBk. test., and data/cntrl. reg. failed
402-06	Loopback test and cntrl. reg. failed	402-16	Unexpected interrupt received
402-07	Loopback tst, data/cntrl. reg. failed	402-01	Printer pattern test failed
402-08	Interrupt test failed	498-00	Printer failed or not connected
402-09	Interrupt test and data reg. failed	--	--

A.9 VIDEO (GRAPHICS) ERROR MESSAGES (5xx-xx)

Table A-8.
Video (Graphics) Error Messages

Message	Probable Cause	Message	Probable Cause
501-01	Video controller test failed	508-01	320x200 mode, color set 0 test failed
502-01	Video memory test failed	509-01	320x200 mode, color set 1 test failed
503-01	Video attribute test failed	510-01	640x200 mode test failed
504-01	Video character set test failed	511-01	Screen memory page test failed
505-01	80x25 mode, 9x14 cell test failed	512-01	Gray scale test failed
506-01	80x25 mode, 8x8 cell test failed	514-01	White screen test failed
507-01	40x25 mode test failed	516-01	Noise pattern test failed

A.10 DISKETTE DRIVE ERROR MESSAGES (6xx-xx)

Table A-9.
Diskette Drive Error Messages

Message	Probable Cause	Message	Probable Cause
6xx-01	Exceeded maximum soft error limit	6xx-20	Failed to get drive type
6xx-02	Exceeded maximum hard error limit	6xx-21	Failed to get change line status
6xx-03	Previously exceeded max soft limit	6xx-22	Failed to clear change line status
6xx-04	Previously exceeded max hard limit	6xx-23	Failed to set drive type in ID media
6xx-05	Failed to reset controller	6xx-24	Failed to read diskette media
6xx-06	Fatal error while reading	6xx-25	Failed to verify diskette media
6xx-07	Fatal error while writing	6xx-26	Failed to read media in speed test
6xx-08	Failed compare of R/W buffers	6xx-27	Failed speed limits
6xx-09	Failed to format a tract	6xx-28	Failed write-protect test
6xx-10	Failed sector wrap test	--	--

600-xx = Diskette drive ID test
601-xx = Diskette drive format
602-xx = Diskette read test
603-xx = Diskette drive R/W compare test
604-xx = Diskette drive random seek test
605-xx = Diskette drive ID media
606-xx = Diskette drive speed test
607-xx = Diskette drive wrap test
608-xx = Diskette drive write-protect test
609-xx = Diskette drive reset controller test
610-xx = Diskette drive change line test
694-00 = Pin 34 not cut on 360-KB drive
697-00 = Diskette type error
698-00 = Drive speed not within limits
699-00 = Drive/media ID error (run Setup)

A.11 SERIAL INTERFACE ERROR MESSAGES (11xx-xx)

Table A-10.
Serial Interface Error Messages

Message	Probable Cause	Message	Probable Cause
1101-01	Port test, UART DLAB bit failure	1101-12	Port test, DRVR/RCVR cntrl. signal failure
1101-02	Port test, line input or UART fault	1101-13	Port test, UART cntrl. signal interrupt failure
1101-03	Port test, address line fault	1101-14	Port test, DRVR/RCVR data failure
1101-04	Port test, data line fault	1109-01	Clock register initialization failure
1101-05	Port test, UART cntrl. signal failure	1109-02	Clock register rollover failure
1101-06	Port test, UART THRE bit failure	1109-03	Clock reset failure
1101-07	Port test, UART Dta RDY bit failure	1109-04	Input line or clock failure
1101-08	Port test, UART TX/RX buffer failure	1109-05	Address line fault
1101-09	Port test, interrupt circuit failure	1109-06	Data line fault
1101-10	Port test, COM1 set to invalid INT	1150-xx	Comm port setup error (run Setup)
1101-11	Port test, COM2 set to invalid INT	--	--

A.12 MODEM COMMUNICATIONS ERROR MESSAGES (12xx-xx)

Table A-11.
Serial Interface Error Messages

Message	Probable Cause	Message	Probable Cause
1201-XX	Modem internal loopback test	1204-03	Data block retry limit reached [4]
1201-01	UART DLAB bit failure	1204-04	RX exceeded carrier lost limit
1201-02	Line input or UART failure	1204-05	TX exceeded carrier lost limit
1201-03	Address line failure	1204-06	Time-out waiting for dial tone
1201-04	Data line fault	1204-07	Dial number string too long
1201-05	UART control signal failure	1204-08	Modem time-out waiting for remote response
1201-06	UART THRE bit failure	1204-09	Modem exceeded maximum redial limit
1201-07	UART DATA READY bit failure	1204-10	Line quality prevented remote response
1201-08	UART TX/RX buffer failure	1204-11	Modem time-out waiting for remote connection
1201-09	Interrupt circuit failure	1205-XX	Modem auto answer test
1201-10	COM1 set to invalid inturrupt	1205-01	Time-out waiting for SYNC [5]
1201-11	COM2 set to invalid	1205-02	Time-out waiting for response [5]
1201-12	DRVR/RCVR control signal failure	1205-03	Data block retry limit reached [5]
1201-13	UART control signal interrupt failure	1205-04	RX exceeded carrier lost limit
1201-14	DRVR/RCVR data failure	1205-05	TX exceeded carrier lost limit
1201-15	Modem detection failure	1205-06	Time-out waiting for dial tone
1201-16	Modem ROM, checksum failure	1205-07	Dial number string too long
1201-17	Tone detect failure	1205-08	Modem time-out waiting for remote response
1202-XX	Modem internal test	1205-09	Modem exceeded maximum redial limit
1202-01	Time-out waiting for SYNC [1]	1205-10	Line quality prevented remote response
1202-02	Time-out waiting for response [1]	1205-11	Modem time-out waiting for remote connection
1202-03	Data block retry limit reached [1]	1206-XX	Dial multi-frequency tone test
1202-11	Time-out waiting for SYNC [2]	1206-17	Tone detection failure
1202-12	Time-out waiting for response [2]	1210-XX	Modem direct connect test
1202-13	Data block retry limit reached [2]	1210-01	Time-out waiting for SYNC [6]
1202-21	Time-out waiting for SYNC [3]	1210-02	Time-out waiting for response [6]
1202-22	Time-out waiting for response [3]	1210-03	Data block retry limit reached [6]
1202-23	Data block retry limit reached [3]	1210-04	RX exceeded carrier lost limit
1203-XX	Modem external termination test	1210-05	TX exceeded carrier lost limit
1203-01	Modem external TIP/RING failure	1210-06	Time-out waiting for dial tone
1203-02	Modem external data TIP/RING fail	1210-07	Dial number string too long
1203-03	Modem line termination failure	1210-08	Modem time-out waiting for remote response
1204-XX	Modem auto originate test	1210-09	Modem exceeded maximum redial limit
1204-01	Time-out waiting for SYNC [4]	1210-10	Line quality prevented remote response
1204-02	Time-out waiting for response [4]	1210-11	Modem time-out waiting for remote connection

NOTES:

[1] Local loopback mode
[2] Analog loopback originate mode
[3] Analog loopback answer mode
[4] Modem auto originate test
[5] Modem auto answer test
[6] Modem direct connect test

A.13 HARD DRIVE ERROR MESSAGES (17xx-xx)

Table A-12.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
17xx-01	Exceeded max. soft error limit	17xx-51	Failed I/O read test
17xx-02	Exceeded max. Hard error limit	17xx-52	Failed file I/O compare test
17xx-03	Previously exceeded max. soft error limit	17xx-53	Failed drive/head register test
17xx-04	Previously exceeded max.hard error limit	17xx-54	Failed digital input register test
17xx-05	Failed to reset controller	17xx-55	Cylinder 1 error
17xx-06	Fatal error while reading	17xx-56	Failed controller RAM diagnostics
17xx-07	Fatal error while writing	17xx-57	Failed controller-to-drive diagnostics
17xx-08	Failed compare of R/W buffers	17xx-58	Failed to write sector buffer
17xx-09	Failed to format a track	17xx-59	Failed to read sector buffer
17xx-10	Failed diskette sector wrap during read	17xx-60	Failed uncorrectable ECC error
17xx-19	Cntlr. failed to deallocate bad sectors	17xx-62	Failed correctable ECC error
17xx-40	Cylinder 0 error	17xx-63	Failed soft error rate
17xx-41	Drive not ready	17xx-65	Exceeded max. bad sectors per track
17xx-42	Failed to recalibrate drive	17xx-66	Failed to initialize drive parameter
17xx-43	Failed to format a bad track	17xx-67	Failed to write long
17xx-44	Failed controller diagnostics	17xx-68	Failed to read long
17xx-45	Failed to get drive parameters from ROM	17xx-69	Failed to read drive size
17xx-46	Invalid drive parameters from ROM	17xx-70	Failed translate mode
17xx-47	Failed to park heads	17xx-71	Failed non-translate mode
17xx-48	Failed to move hard drive table to RAM	17xx-72	Bad track limit exceeded
17xx-49	Failed to read media in file write test	17xx-73	Previously exceeded bad track limit
17xx-50	Failed I/O write test	--	--

1700-xx = Hard drive ID test
1701-xx = Hard drive format test
1702-xx = Hard drive read test
1703-xx = Hard drive read/write compare test
1704-xx = Hard drive random seek test
1705-xx = Hard drive controller test
1706-xx = Hard drive ready test
1707-xx = Hard drive recalibrate test
1708-xx = Hard drive format bad track test
1709-xx = Hard drive reset controller test
1710-xx = Hard drive park head test
1714-xx = Hard drive file write test
1715-xx = Hard drive head select test
1716-xx = Hard drive conditional format test
1717-xx = Hard drive ECC test
1719-xx = Hard drive power mode test
1721-xx = SCSI hard drive imminent failure
1724-xx = Net work preparation test
1736-xx = Drive monitoring test
1799-xx = Invalid hard drive type

A.14 HARD DRIVE ERROR MESSAGES (19xx-xx)

Table A-13.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
19xx-01	Drive not installed	19xx-21	Got servo pulses second time but not first
19xx-02	Cartridge not installed	19xx-22	Never got to EOT after servo check
19xx-03	Tape motion error	19xx-23	Change line unset
19xx-04	Drive busy erro	19xx-24	Write-protect error
19xx-05	Track seek error	19xx-25	Unable to erase cartridge
19xx-06	Tape write-protect error	19xx-26	Cannot identify drive
19xx-07	Tape already Servo Written	19xx-27	Drive not compatible with controller
19xx-08	Unable to Servo Write	19xx-28	Format gap error
19xx-09	Unable to format	19xx-30	Exception bit not set
19xx-10	Format mode error	19xx-31	Unexpected drive status
19xx-11	Drive recalibration error	19xx-32	Device fault
19xx-12	Tape not Servo Written	19xx-33	Illegal command
19xx-13	Tape not formatted	19xx-34	No data detected
19xx-14	Drive time-out error	19xx-35	Power-on reset occurred
19xx-15	Sensor error flag	19xx-36	Failed to set FLEX format mode
19xx-16	Block locate (block ID) error	19xx-37	Failed to reset FLEX format mode
19xx-17	Soft error limit exceeded	19xx-38	Data mismatch on directory track
19xx-18	Hard error limit exceeded	19xx-39	Data mismatch on track 0
19xx-19	Write (probably ID) error	19xx-40	Failed self-test
19xx-20	NEC fatal error	19xx-91	Power lost during test

1900-xx = Tape ID test failed
1901-xx = Tape servo write failed
1902-xx = Tape format failed
1903-xx = Tape drive sensor test failed
1904-xx = Tape BOT/EOT test failed
1905-xx = Tape read test failed
1906-xx = Tape R/W compare test failed
1907-xx = Tape write-protect failed

A.15 VIDEO (GRAPHICS) ERROR MESSAGES (24xx-xx)

Table A-14.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
2402-01	Video memory test failed	2418-02	EGA shadow RAM test failed
2403-01	Video attribute test failed	2419-01	EGA ROM checksum test failed
2404-01	Video character set test failed	2420-01	EGA attribute test failed
2405-01	80x25 mode, 9x14 cell test failed	2421-01	640x200 mode test failed
2406-01	80x25 mode, 8x8 cell test failed	2422-01	640x350 16-color set test failed
2407-01	40x25 mode test failed	2423-01	640x350 64-color set test failed
2408-01	320x200 mode color set 0 test failed	2424-01	EGA Mono. text mode test failed
2409-01	320x200 mode color set 1 test failed	2425-01	EGA Mono. graphics mode test failed
2410-01	640x200 mode test failed	2431-01	640x480 graphics mode test failed
2411-01	Screen memory page test failed	2432-01	320x200 256-color set test failed
2412-01	Gray scale test failed	2448-01	Advanced VGA controller test failed
2414-01	White screen test failed	2451-01	132-column AVGA test failed
2416-01	Noise pattern test failed	2456-01	AVGA 256-color test failed
2417-01	Lightpen text test failed, no response	2458-xx	AVGA BitBLT test failed
2417-02	Lightpen text test failed, invalid response	2468-xx	AVGA DAC test failed
2417-03	Lightpen graphics test failed, no resp.	2477-xx	AVGA data path test failed
2417-04	Lightpen graphics test failed, invalid resp.	2478-xx	AVGA BitBLT test failed
2418-01	EGA memory test failed	2480-xx	AVGA linedraw test failed

A.16 AUDIO ERROR MESSAGES (3206-xx)

Table A-15.
Audio Error Message

Message	Probable Cause
3206-xx	Audio subsystem internal error

A.17 NETWORK INTERFACE ERROR MESSAGES (60xx-xx)

Table A-16.
Network Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6000-xx	Pointing device interface error	6054-xx	Token ring configuration test failed
6014-xx	Ethernet configuration test failed	6056-xx	Token ring reset test failed
6016-xx	Ethernet reset test failed	6068-xx	Token ring int. loopback test failed
6028-xx	Ethernet int. loopback test failed	6069-xx	Token ring ext. loopback test failed
6029-xx	Ethernet ext. loopback test failed	6089-xx	Token ring open

A.18 SCSI INTERFACE ERROR MESSAGES (65xx-xx, 66xx-xx, 67xx-xx)

Table A-17.
SCSI Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6nyy-02	Drive not installed	6nyy-33	Illegal controller command
6nyy-03	Media not installed	6nyy-34	Invalid SCSI bus phase
6nyy-05	Seek failure	6nyy-35	Invalid SCSI bus phase
6nyy-06	Drive timed out	6nyy-36	Invalid SCSI bus phase
6nyy-07	Drive busy	6nyy-39	Error status from drive
6nyy-08	Drive already reserved	6nyy-40	Drive timed out
6nyy-09	Reserved	6nyy-41	SSI bus stayed busy
6nyy-10	Reserved	6nyy-42	ACK/REQ lines bad
6nyy-11	Media soft error	6nyy-43	ACK did not deassert
6nyy-12	Drive not ready	6nyy-44	Parity error
6nyy-13	Media error	6nyy-50	Data pins bad
6nyy-14	Drive hardware error	6nyy-51	Data line 7 bad
6nyy-15	Illegal drive command	6nyy-52	MSG, C/D, or I/O lines bad
6nyy-16	Media was changed	6nyy-53	BSY never went busy
6nyy-17	Tape write-protected	6nyy-54	BSY stayed busy
6nyy-18	No data detected	6nyy-60	Controller CONFIG-1 register fault
6nyy-21	Drive command aborted	6nyy-61	Controller CONFIG-2 register fault
6nyy-24	Media hard error	6nyy-65	Media not unloaded
6nyy-25	Reserved	6nyy-90	Fan failure
6nyy-30	Controller timed out	6nyy-91	Over temperature condition
6nyy-31	Unrecoverable error	6nyy-92	Side panel not installed
6nyy-32	Controller/drive not connected	6nyy-99	Autoloader reported tape not loaded properly

n = 5, Hard drive
= 6, CD-ROM drive
= 7, Tape drive.

yy = 00, ID
= 03, Power check
= 05, Read
= 06, SA/Media
= 08, Controller;
= 23, Random read
= 28, Media load/unload

A.19 POINTING DEVICE INTERFACE ERROR MESSAGES (8601-xx)

Table A-18.
Pointing Device Interface Error Messages

Message	Probable Cause	Message	Probable Cause
8601-01	Mouse ID fails	8601-06	Left block not selected
8601-02	Left mouse button is inoperative	8601-07	Right block not selected
8601-03	Left mouse button is stuck closed	8601-08	Timeout occurred
8601-04	Right mouse button is inoperative	8601-09	Mouse loopback test failed
8601-05	Right mouse button is stuck closed	8601-10	Pointing device is inoperative

A.20 CEMM PRIVILEDGED OPS ERROR MESSAGES

Table A-19.
CEMM Privileged Ops Error Messages

Message	Probable Cause	Message	Probable Cause
00	LGDT instruction	04	LL3 instruction
01	LIDT instruction	05	MOV CRx instruction
02	LMSW instruction	06	MOV DRx instruction
03	LL2 instruction	07	MOV TRx instruction

A.21 CEMM EXCEPTION ERROR MESSAGES

Table A-20.
CEMM Exception Error Messages

Message	Probable Cause	Message	Probable Cause
00	Divide	10	Invalid TSS
01	Debug	11	Segment not present
02	NMI or parity	12	Stack full
03	INT 0 (arithmetic overflow)	13	General protection fault
04	INT 3	14	Page fault
05	Array bounds check	16	Coprocessor
06	Invalid opcode	32	Attempt to write to protected area
07	Coprocessor device not available	33	Reserved
08	Double fault	34	Invalid software interrupt
09	Coprocessor segment overrun	--	--

Appendix B
ASCII CHARACTER SET

B.1 INTRODUCTION

This appendix lists, in Table B-1, the 256-character ASCII code set including the decimal and hexadecimal values. All ASCII symbols may be called while in DOS or using standard text-mode editors by using the combination keystroke of holding the **Alt** key and using the Numeric Keypad to enter the decimal value of the symbol. The extended ASCII characters (decimals 128-255) can only be called using the **Alt** + Numeric Keypad keys.

NOTE: Regarding keystrokes, refer to notes at the end of the table. Applications may interpret multiple keystroke accesses differently or ignore them completely.

Table B-1.
ASCII Character Set

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
0	00	Blank	32	20	Space	64	40	@	96	60	‘
1	01	☺	33	21	!	65	41	A	97	61	a
2	02	☻	34	22	“	66	42	B	98	62	b
3	03	♥	35	23	#	67	43	C	99	63	c
4	04	♦	36	24	$	68	44	D	100	64	d
5	05	♣	37	25	%	69	45	E	101	65	e
6	06	♠	38	26	&	70	46	F	102	66	f
7	07	•	39	27	‘	71	47	G	103	67	g
8	08	◘	40	28	(	72	48	H	104	68	h
9	09	○	41	29	)	73	49	I	105	69	I
10	0A	◙	42	2A	*	74	4A	J	106	6A	j
11	0B	♂	43	2B	+	75	4B	K	107	6B	k
12	0C	♀	44	2C	`	76	4C	L	108	6C	l
13	0D	♪	45	2D	-	77	4D	M	109	6D	m
14	0E	♫	46	2E	.	78	4E	N	110	6E	n
15	0F	☼	47	2F	/	79	4F	O	111	6F	o
16	10	►	48	30	0	80	50	P	112	70	p
17	11	◄	49	31	1	81	51	Q	113	71	q
18	12	↕	50	32	2	82	52	R	114	72	r
19	13	‼	51	33	3	83	53	S	115	73	s
20	14	¶	52	34	4	84	54	T	116	74	t
21	15	§	53	35	5	85	55	U	117	75	u
22	16	▬	54	36	6	86	56	V	118	76	v
23	17	↨	55	37	7	87	57	W	119	77	w
24	18	↑	56	38	8	88	58	X	120	78	x
25	19	↓	57	39	9	89	59	Y	121	79	y
26	1A	→	58	3A	:	90	5A	Z	122	7A	z
27	1B	←	59	3B	;	91	5B	[	123	7B	{
28	1C	∟	60	3C	<	92	5C	\	124	7C	|
29	1D	↔	61	3D	=	93	5D	]	125	7D	}
30	1E	▲	62	3E	>	94	5E	^	126	7E	~
31	1F	▼	63	3F	?	95	5F	_	127	7F	△ [1]

Continued

Table B-1. ASCII Code Set *(Continued)*

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
128	80	Ç	160	A0	á	192	C0	•	224	E0	•
129	81	ü	161	A1	í	193	C1	•	225	E1	ß
130	82	é	162	A2	ó	194	C2	•	226	E2	•
131	83	â	163	A3	ú	195	C3	•	227	E3	•
132	84	ä	164	A4	ñ	196	C4	•	228	E4	•
133	85	à	165	A5	Ñ	197	C5	•	229	E5	•
134	86	å	166	A6	ª	198	C6	•	230	E6	µ
135	87	ç	167	A7	º	199	C7	•	231	E7	•
136	88	ê	168	A8	¿	200	C8	•	232	E8	•
137	89	ë	169	A9	•	201	C9	•	233	E9	•
138	8A	è	170	AA	¬	202	CA	•	234	EA	•
139	8B	ï	171	AB	½	203	CB	•	235	EB	•
140	8C	î	172	AC	¼	204	CC	•	236	EC	•
141	8D	ì	173	AD	¡	205	CD	•	237	ED	•
142	8E	Ä	174	AE	«	206	CE	•	238	EE	•
143	8F	Å	175	AF	»	207	CF	•	239	EF	•
144	90	É	176	B0	•	208	D0	•	240	F0	•
145	91	æ	177	B1	•	209	D1	•	241	F1	±
146	92	Æ	178	B2	•	210	D2	•	242	F2	•
147	93	ô	179	B3	•	211	D3	•	243	F3	•
148	94	ö	180	B4	•	212	D4	•	244	F4	•
149	95	ò	181	B5	•	213	D5	•	245	F5	•
150	96	û	182	B6	•	214	D6	•	246	F6	÷
151	97	ù	183	B7	•	215	D7	•	247	F7	•
152	98	ÿ	184	B8	•	216	D8	•	248	F8	°
153	99	Ö	185	B9	•	217	D9	•	249	F9	·
154	9A	Ü	186	BA	•	218	DA	•	250	FA	·
155	9B	¢	187	BB	•	219	DB	•	251	FB	•
156	9C	£	188	BC	•	220	DC	•	252	FC	•
157	9D	¥	189	BD	•	221	DD	•	253	FD	²
158	9E	•	190	BE	•	222	DE	•	254	FE	•
159	9F	*f*	191	BF	•	223	DF	•	255	FF	Blank

NOTES:

[1] Symbol not displayed.

Keystroke Guide:

Dec #	Keystroke(s)
0	Ctrl 2
1-26	Ctrl A thru Z respectively
27	Ctrl [
28	Ctrl
29	Ctrl]
30	Ctrl 6
31	Ctrl -
32	Space Bar
33-43	Shift and key w/corresponding symbol
44-47	Key w/corresponding symbol
48-57	Key w/corresponding symbol, numerical keypad w/Num Lock active
58	Shift and key w/corresponding symbol
59	Key w/corresponding symbol
60	Shift and key w/corresponding symbol
61	Key w/corresponding symbol
62-64	Shift and key w/corresponding symbol
65-90	Shift and key w/corresponding symbol or key w/corresponding symbol and Caps Lock active
91-93	Key w/corresponding symbol
94, 95	Shift and key w/corresponding symbol
96	Key w/corresponding symbol
97-126	Key w/corresponding symbol or Shift and key w/corresponding symbol and Caps Lock active
127	Ctrl -
128-255	Alt and decimal digit(s) of desired character

Appendix C
KEYBOARD

C.1 INTRODUCTION

This appendix describes the Compaq keyboard that is included as standard with the system unit. The keyboard complies with the industry-standard classification of an "enhanced keyboard" and includes a separate cursor control key cluster, twelve "function" keys, and enhanced programmability for additional functions.

This appendix covers the following keyboard types (some of which may be available only as an option):

- The Windows-version keyboard includes three additional keys for specific support of the Windows operating system.
- The Erase-Ease keyboard features a split spacebar that can be user-programmed to provide easy access to the backspace function or set to operate as the normal spacebar.
- The scanner keyboard includes a built-in document scanner for scanning loose-leaf hardcopy.

> **NOTE:** This appendix discusses only the keyboard unit. The keyboard interface is a function of the system unit and is discussed in Chapter 5, Input/Output Interfaces.

Topics covered in this appendix include the following:

C.2 KEYSTROKE PROCESSING

A functional block diagram of the keystroke processing elements is shown in Figure C-1. Power (+5 VDC) is obtained from the system through the PS/2-type interface. The keyboard uses a Z86C14 (or equivalent) microprocessor. The Z86C14 scans the key matrix drivers every 10 ms for pressed keys while at the same time monitoring communications with the keyboard interface of the system unit. When a key is pressed, a Make code is generated. A Break code is generated when the key is released. The Make and Break codes are collectively referred to as scan codes. All keys generate Make and Break codes with the exception of the Pause key, which generates a Make code only.

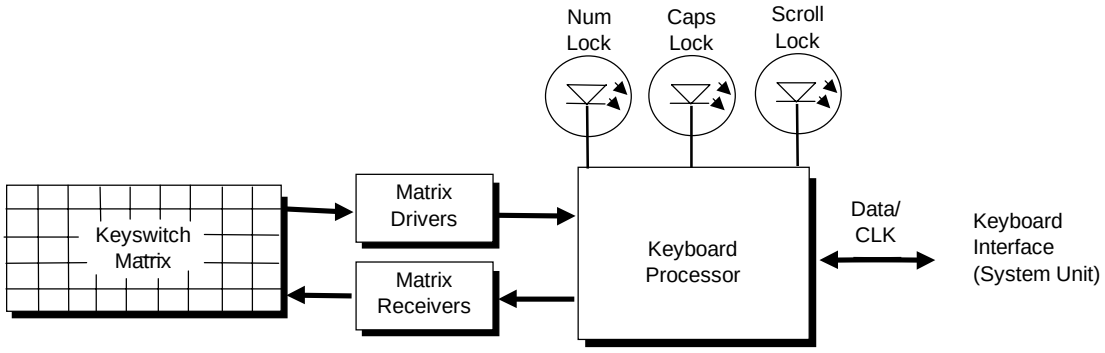


Figure C–1. Keystroke Processing Elements, Block Diagram

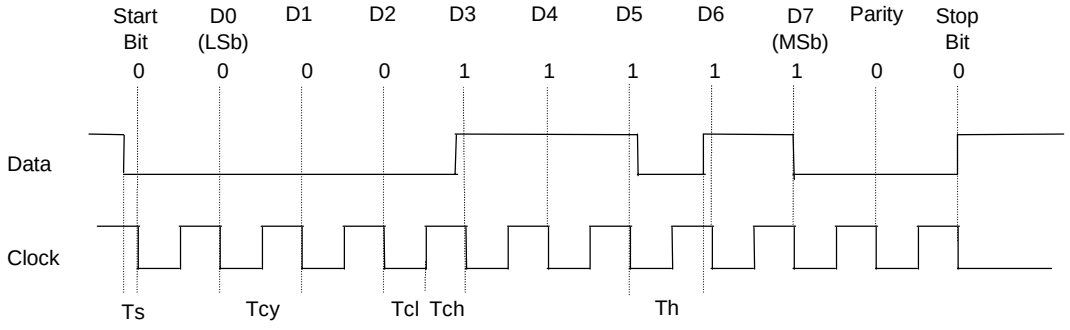
When the system is turned on, the keyboard processor generates a Power-On Reset (POR) signal after a period of 150 ms to 2 seconds. The keyboard undergoes a Basic Assurance Test (BAT) that checks for shorted keys and basic operation of the keyboard processor. The BAT takes from 300 to 500 ms to complete.

If the keyboard fails the BAT, an error code is sent to the CPU and the keyboard is disabled until an input command is received. After successful completion of the POR and BAT, a completion code (AAh) is sent to the CPU and the scanning process begins.

The keyboard processor includes a 16-byte FIFO buffer for holding scan codes until the system is ready to receive them. Response and typematic codes are not buffered. If the buffer is full (16 bytes held) a 17th byte of a successive scan code results in an overrun condition and the overrun code replaces the scan code byte and any additional scan code data (and the respective key strokes) are lost. Multi-byte sequences must fit entirely into the buffer before the respective keystroke can be registered.

C.2.1 TRANSMISSIONS TO THE SYSTEM

The keyboard processor sends two main types of data to the system; commands (or responses to system commands) and keystroke scan codes. Before the keyboard sends data to the system (specifically, to the 8042-type logic within the system), the keyboard verifies the clock and data lines to the system. If the clock signal is low (0), the keyboard recognizes the inhibited state and loads the data into a buffer. Once the inhibited state is removed, the data is sent to the system. Keyboard-to-system transfers consist of 11 bits as shown in Figure C-2.



Parameter	Minimum	Maximum
Tcy (Cycle Time)	60 us	80 us
Tcl (Clock Low)	30 us	35 us
Tch (clock High)	30 us	45 us
Th (Data Hold)	45 us	62 us
Ts (Data Setup)	8 us	14 us

Figure C–2. Keyboard-To-System Transmission of Code 58h, Timing Diagram

The system can halt keyboard transmission by setting the clock signal low. The keyboard checks the clock line every 60 us to verify the signal state. If a low is detected, the keyboard will finish the current transmission **if** the rising edge of the clock pulse for the parity bit has not occurred.

The enhanced keyboard has three operating modes:

- Mode 1 - PC-XT compatible
- Mode 2 - PC-AT compatible (default)
- Mode 3 - Select mode (keys are programmable as to make-only, break-only, typematic)

Modes can be selected by the user or set by the system. Mode 2 is the default mode. Each mode produces a different set of scan codes. When a key is pressed, the keyboard processor sends that key's make code to the 8042 logic of the system unit. The When the key is released, a release code is transmitted as well (except for the Pause key, which produces only a make code). The 8042-type logic of the system unit responds to scan code reception by asserting IRQ1, which is processed by the interrupt logic and serviced by the CPU with an interrupt service routine. The service routine takes the appropriate action based on which key was pressed.

C.2.2 KEYBOARD LAYOUTS

C.2.2.1 Standard Enhanced Keyboards

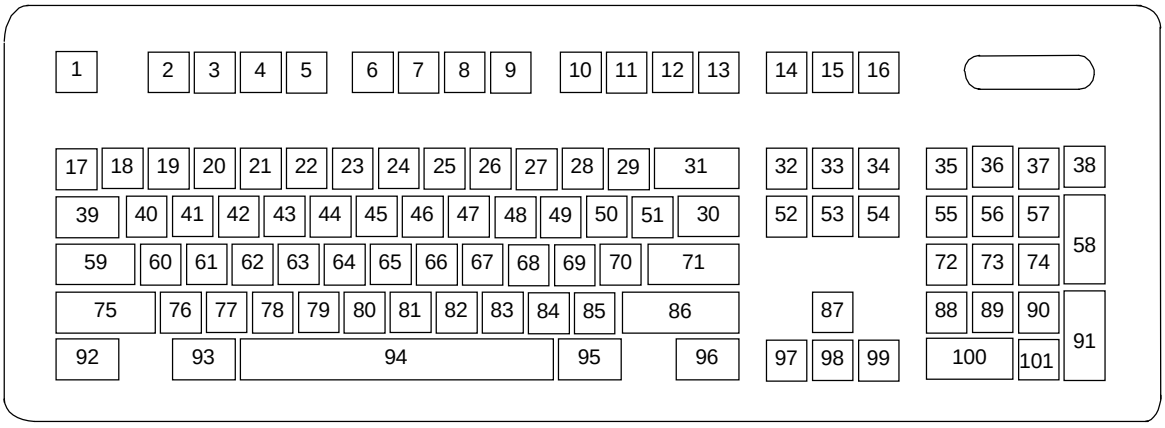


Figure C–3. U.S. English (101-Key) Keyboard Key Positions

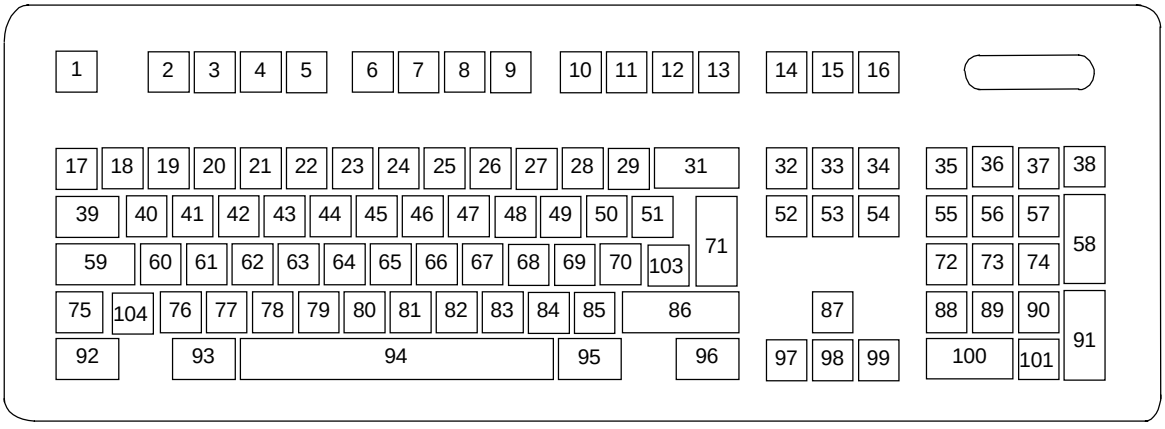


Figure C–4. National (102-Key) Keyboard Key Positions

C.2.2.2 Windows Enhanced Keyboards

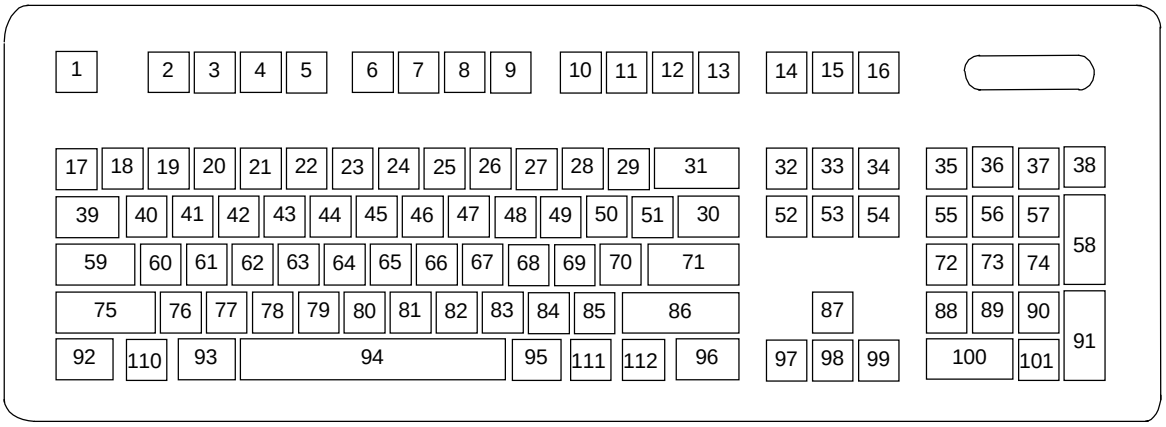


Figure C–5. U.S. English Windows (101W-Key) Keyboard Key Positions

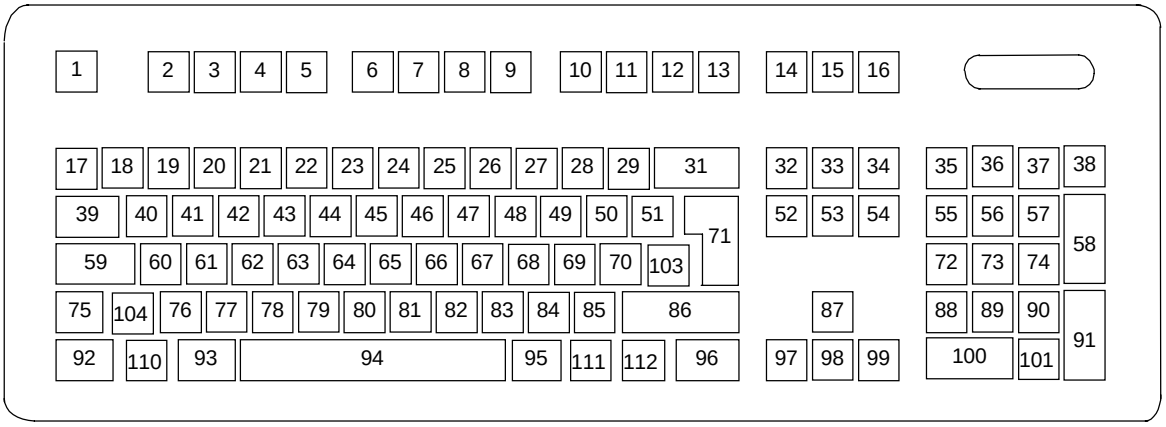


Figure C–6. National Windows (102W-Key) Keyboard Key Positions

C.2.2.3 Windows Enhanced Keyboards w/Erase-Ease

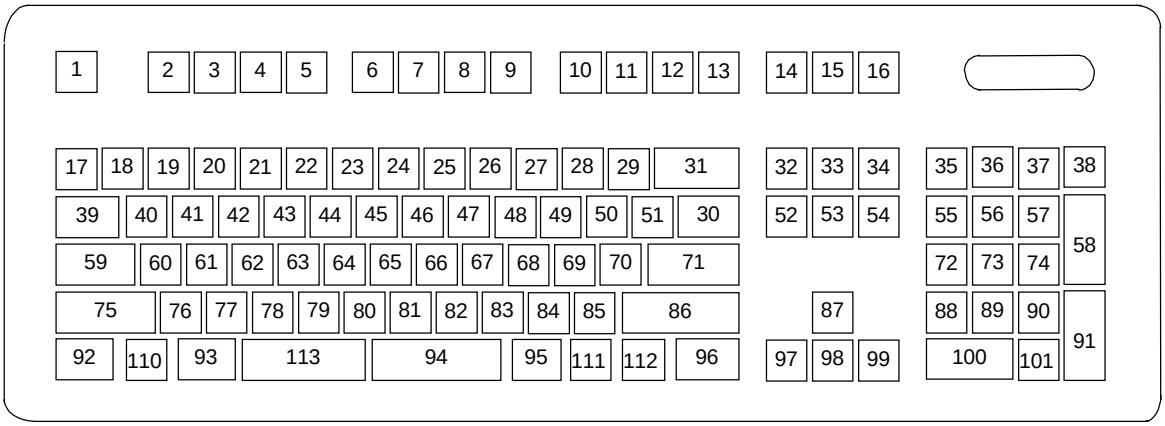


Figure C–7. U.S. English Windows (101WE-Key) Keyboard Key Positions

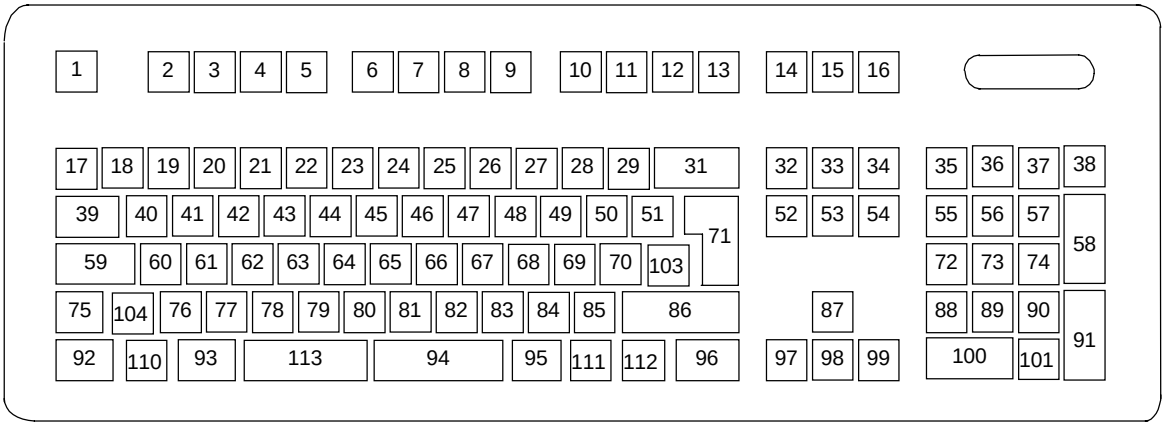


Figure C–8. National Windows (102WE-Key) Keyboard Key Positions

C.2.3 KEYS

All keys generate a make code (when pressed) and a break code (when released) with the exception of the **Pause** key (pos. 16), which produces a make code only. All keys, again, with the exception of the **Pause** key, are also typematic, although the typematic action of the **Shift**, **Ctrl**, **Alt**, **Num Lock**, **Scroll Lock**, **Caps Lock**, and **Ins** keys is suppressed by the BIOS. Typematic keys, when held down, send the make code repetitively at a predetermined rate until the key is released. If two keys are held down, the last key pressed will be typematic.

C.2.3.1 Special Single-Keystroke Functions

The following keys provide the intended function in most applications and environments.

Caps Lock - The **Caps Lock** key (pos. 59), when pressed and released, invokes a BIOS routine that turns on the caps lock LED and shifts into upper case key positions 40-49, 60-68, and 76-82. When pressed and released again, these keys revert to the lower case state and the LED is turned off. Use of the **Shift** key will reverse which state these keys are in based on the **Caps Lock** key.

Num Lock - The **Num Lock** key (pos. 32), when pressed and released, invokes a BIOS routine that turns on the num lock LED and shifts into upper case key positions 55-57, 72-74, 88-90, 100, and 101. When pressed and released again, these keys revert to the lower case state and the LED is turned off.

The following keys provide special functions that require specific support by the application.

Print Scrn - The **Print Scrn** (pos. 14) key can, when pressed, generate an interrupt that initiates a print routine. This function may be inhibited by the application.

Scroll Lock - The **Scroll Lock** key (pos. 15) when pressed and released, , invokes a BIOS routine that turns on the scroll lock LED and inhibits movement of the cursor. When pressed and released again, the LED is turned off and the function is removed. This keystroke is always serviced by the BIOS (as indicated by the LED) but may be inhibited or ignored by the application.

Pause - The **Pause** (pos. 16) key, when pressed, can be used to cause the keyboard interrupt to loop, i.e., wait for another key to be pressed. This can be used to momentarily suspend an operation. The key that is pressed to resume operation is discarded. This function may be ignored by the application.

The **Esc**, **Fn** (function), **Insert**, **Home**, **Page Up**/**Down**, **Delete**, and **End** keys operate at the discretion of the application software.

C.2.3.2 Multi-Keystroke Functions

Shift - The **Shift** key (pos. 75/86), when held down, produces a shift state (upper case) for keys in positions 17-29, 30, 39-51, 60-70, and 76-85 as long as the **Caps Lock** key (pos. 59) is toggled off. If the **Caps Lock** key is toggled on, then a held **Shift** key produces the lower (normal) case for the identified pressed keys. The **Shift** key also reverses the **Num Lock** state of key positions 55-57, 72, 74, 88-90, 100, and 101.

Ctrl - The **Ctrl** keys (pos. 92/96) can be used in conjunction with keys in positions 1-13, 16, 17-34, 39-54, 60-71, and 76-84. The application determines the actual function. Both **Ctrl** key positions provide identical functionality. The pressed combination of **Ctrl** and **Break** (pos. 16) results in the generation of BIOS function INT 1Bh. This software interrupt provides a method of exiting an application and generally halts execution of the current program.

Alt - The **Alt** keys (pos. 93/95) can be used in conjunction with the same keys available for use with the **Ctrl** keys with the exception that position 14 (**SysRq**) is available instead of position 16 (**Break**). The **Alt** key can also be used in conjunction with the numeric keypad keys (pos. 55-57, 72-74, and 88-90) to enter the decimal value of an ASCII character code from 1-255. The application determines the actual function of the keystrokes. Both **Alt** key positions provide identical functionality.

The combination keystroke of **Alt** and **SysRq** results in software interrupt 15h, AX=8500h being executed. It is up to the application to use or not use this BIOS function.

The **Ctrl** and **Alt** keys can be used together in conjunction with keys in positions 1-13, 17-34, 39-54, 60-71, and 76-84. The **Ctrl** and **Alt** key positions used and the sequence in which they are pressed make no difference as long as they are held down at the time the third key is pressed. The **Ctrl**, **Alt,** and **Delete** keystroke combination (required twice if in the Windows environment) initiates a system reset (warm boot) that is handled by the BIOS.

C.2.3.3 Windows Keystrokes

Windows-enhanced keyboards include three additional key positions. Key positions 110 and 111 (marked with the Windows logo) have the same functionality and are used by themselves or in combination with other keys to perform specific "hot-key" type functions for the Windows operating system. The defined functions of the Windows logo keys are listed as follows:

Keystroke	Function
Window Logo	Open Start menu
Window Logo + F1	Display pop-up menu for the selected object
Window Logo + TAB	Activate next task bar button
Window Logo + E	Explore my computer
Window Logo + F	Find document
Window Logo + CTRL + F	Find computer
Window Logo + M	Minimize all
Shift + Window Logo + M	Undo minimize all
Window Logo + R	Display Run dialog box
Window Logo + PAUSE	Perform system function
Window Logo + 1-0	Reserved for OEM use (see following text)

The combination keystroke of the Window Logo + 1-0 keys are reserved for OEM use for auxiliary functions (speaker volume, monitor brightness, password, etc.).

Key position 112 (marked with an application window icon) is used in combination with other keys for invoking Windows application functions.

C.2.3.4 Erase-Ease Keystrokes

The Erase-Ease keyboards feature a split space-bar key that operates as two separate keys (positions 113 and 94). The two keys can be configured for one of three modes:

Mode A:
(Power-on default)

113	94
Backspace	Spacebar

Mode B:

113	94
Spacebar	Backspace

Mode C:

113	94
Spacebar	Spacebar

To switch between modes the user holds down the left **ALT**, left **CTRL**, and left **Shift** keys while pressing the Erase-Ease (pos. 113) key once.

C.2.4 KEYBOARD COMMANDS

Table C-1 lists the commands that the keyboard can send to the system (specifically, to the 8042-type logic).

Table C-1.
Keyboard-to-System Commands

Command	Value	Description
Key Detection Error/Over/run	00h [1] FFh [2]	Indicates to the system that a switch closure couldn't be identified.
BAT Completion	AAh	Indicates to the system that the BAT has been successful.
BAT Failure	FCh	Indicates failure of the BAT by the keyboard.
Echo	EEh	Indicates that the Echo command was received by the keyboard.
Acknowledge (ACK)	FAh	Issued by the keyboard as a response to valid system inputs (except the Echo and Resend commands).
Resend	FEh	Issued by the keyboard following an invalid input.
Keyboard ID	83ABh	Upon receipt of the Read ID command from the system, the keyboard issues the ACK command followed by the two IDS bytes.

Note:
[1] Modes 2 and 3.
[2] Mode 1 only.

C.2.5 SCAN CODES

The scan codes generated by the keyboard processor are determined by the mode the keyboard is operating in.

- Mode 1: In Mode 1 operation, the keyboard generates scan codes compatible with 8088-/8086-based systems. To enter Mode 1, the scan code translation function of the keyboard controller must be disabled. Since translation is not performed, the scan codes generated in Mode 1 are identical to the codes required by BIOS. Mode 1 is initiated by sending command F0h with the 01h option byte. Applications can obtain system codes and status information by using BIOS function INT 16h with AH=00h, 01h, and 02h.

- Mode 2: Mode 2 is the default mode for keyboard operation. In this mode, the 8042 logic translates the make codes from the keyboard processor into the codes required by the BIOS. This mode was made necessary with the development of the Enhanced III keyboard, which includes additional functions over earlier standard keyboards. Applications should use BIOS function INT 16h, with AH=10h, 11h, and 12h for obtaining codes and status data. In Mode 2, the keyboard generates the Break code, a two-byte sequence that consists of a Make code immediately preceded by F0h (i.e., Break code for 0Eh is "F0h 0Eh").

- Mode 3: Mode 3 generates a different scan code set from Modes 1 and 2. Code translation must be disabled since translation for this mode cannot be done.

Table C-2.
Keyboard Scan Codes

Key Pos.	Legend	Make / Break Codes (Hex) Mode 1	Mode 2	Mode 3
1	Esc	01/81	76/F0 76	08/na
2	F1	3B/BB	05/F0 05	07/na
3	F2	3C/BC	06/F0 06	0F/na
4	F3	3D/BD	04/F0 04	17/na
5	F4	3E/BE	0C/F0 0C	1F/na
6	F5	3F/BF	03/F0 03	27/na
7	F6	40/C0	0B/F0 0B	2F/na
8	F7	41/C1	83/F0 83	37/na
9	F8	42/C2	0A/F0 0A	3F/na
10	F9	43/C3	01/FO 01	47/na
11	F10	44/C4	09/F0 09	4F/na
12	F11	57/D7	78/F0 78	56/na
13	F12	58/D8	07/F0 07	5E/na
14	Print Scrn	E0 2A E0 37/E0 B7 E0 AA E0 37/E0 B7 [1] [2] 54/84 [3]	E0 2A E0 7C/E0 F0 7C E0 F0 12 E0 7C/E0 F0 7C [1] [2] 84/F0 84 [3]	57/na
15	Scroll Lock	46/C6	7E/F0 7E	5F/na
16	Pause	E1 1D 45 E1 9D C5/na E0 46 E0 C6/na [3]	E1 14 77 E1 F0 14 F0 77/na E0 7E E0 F0 7E/na [3]	62/na
17	`	29/A9	0E/F0 E0	0E/F0 0E
18	1	02/82	16/F0 16	46/F0 46
19	2	03/83	1E/F0 1E	1E/F0 1E
20	3	04/84	26/F0 26	26/F0 26
21	4	05/85	25/F0 25	25/F0 25
22	5	06/86	2E/F0 2E	2E/F0 2E
23	6	07/87	36/F0 36	36/F0 36
24	7	08/88	3D/F0 3D	3D/F0 3D
25	8	09/89	3E/F0 3E	3E/F0 3E
26	9	0A/8A	46/F0 46	46/F0 46
27	0	0B/8B	45/F0 45	45/F0 45
28	-	0C/8C	4E/F0 4E	4E/F0 4E
29	=	0D/8D	55/F0 55	55/F0 55
30	\	2B/AB	5D/F0 5D	5C/F0 5C
31	Backspace	0E/8E	66/F0 66	66/F0 66
32	Insert	E0 52/E0 D2 E0 AA E0 52/E0 D2 E0 2A [4] E0 2A E0 52/E0 D2 E0 AA [6]	E0 70/E0 F0 70 E0 F0 12 E0 70/E0 F0 70 E0 12 [5] E0 12 E0 70/E0 F0 70 E0 F0 12 [6]	67/na
33	Home	E0 47/E0 D2 E0 AA E0 52/E0 D2 E0 2A [4] E0 2A E0 47/E0 C7 E0 AA [6]	E0 6C/E0 F0 6C E0 F0 12 E0 6C/E0 F0 6C E0 12 [5] E0 12 E0 6C/E0 F0 6C E0 F0 12 [6]	6E/na
34	Page Up	E0 49/E0 C7 E0 AA E0 49/E0 C9 E0 2A [4] E0 2A E0 49/E0 C9 E0 AA [6]	E0 7D/E0 F0 7D E0 F0 12 E0 7D/E0 F0 7D E0 12 [5] E0 12 E0 7D/E0 F0 7D E0 F0 12 [6]	6F/na
35	Num Lock	45/C5	77/F0 77	76/na
36	/	E0 35/E0 B5 E0 AA E0 35/E0 B5 E0 2A [1]	E0 4A/E0 F0 4A E0 F0 12 E0 4A/E0 F0 4A E0 12 [1]	77/na
37	*	37/B7	7C/F0 7C	7E/na
38	-	4A/CA	7B/F0 7B	84/na
39	Tab	0F/8F	0D/F0 0D	0D/na
40	Q	10/90	15/F0 15	15/na

Continued

([x] Notes listed at end of table.)

Table C-2. Keyboard Scan Codes *(Continued)*

Key		Make / Break Codes (Hex)		
Pos	**Legend**	**Mode 1**	**Mode 2**	**Mode 3**
41	W	11/91	1D/F0 1D	1D/F0 1D
42	E	12/92	24/F0 24	24/F0 24
43	R	13/93	2D/F0 2D	2D/F0 2D
44	T	14/94	2C/F0 2C	2C/F0 2C
45	Y	15/95	35/F0 35	35/F0 35
46	U	16/96	3C/F0 3C	3C/F0 3C
47	I	17/97	43/F0 43	43/F0 43
48	O	18/98	44/F0 44	44/F0 44
49	P	19/99	4D/F0 4D	4D/F0 4D
50	[	1A/9A	54/F0 54	54/F0 54
51	]	1B/9B	5B/F0 5B	5B/F0 5B
52	Delete	E0 53/E0 D3 E0 AA E0 53/E0 D3 E0 2A [4] E0 2A E0 53/E0 D3 E0 AA [6]	E0 71/E0 F0 71 E0 F0 12 E0 71/E0 F0 71 E0 12 [5] E0 12 E0 71/E0 F0 71 E0 F0 12 [6]	64/F0 64
53	End	E0 4F/E0 CF E0 AA E0 4F/E0 CF E0 2A [4] E0 2A E0 4F/E0 CF E0 AA [6]	E0 69/E0 F0 69 E0 F0 12 E0 69/E0 F0 69 E0 12 [5] E0 12 E0 69/E0 F0 69 E0 F0 12 [6]	65/F0 65
54	Page Down	E0 51/E0 D1 E0 AA E0 51/E0 D1 E0 2A [4] E0 @a E0 51/E0 D1 E0 AA [6]	E0 7A/E0 F0 7A E0 F0 12 E0 7A/E0 F0 7A E0 12 [5] E0 12 E0 7A/E0 F0 7A E0 F0 12 [6]	6D/F0 6D
55	7	47/C7 [6]	6C/F0 6C [6]	6C/na [6]
56	8	48/C8 [6]	75/F0 75 [6]	75/na [6]
57	9	49/C9 [6]	7D/F0 7D [6]	7D/na [6]
58	+	4E/CE [6]	79/F0 79 [6]	7C/F0 7C
59	Caps Lock	3A/BA	58/F0 58	14/F0 14
60	A	1E/9E	1C/F0 1C	1C/F0 1C
61	S	1F/9F	1B/F0 1B	1B/F0 1B
62	D	20/A0	23/F0 23	23/F0 23
63	F	21/A1	2B/F0 2B	2B/F0 2B
64	G	22/A2	34/F0 34	34/F0 34
65	H	23/A3	33/F0 33	33/F0 33
66	J	24/A4	3B/F0 3B	3B/F0 3B
67	K	25/A5	42/F0 42	42/F0 42
68	L	26/A6	4B/F0 4B	4B/F0 4B
69	;	27/A7	4C/F0 4C	4C/F0 4C
70	‘	28/A8	52/F0 52	52/F0 52
71	Enter	1C/9C	5A/F0 5A	5A/F0 5A
72	4	4B/CB [6]	6B/F0 6B [6]	6B/na [6]
73	5	4C/CC [6]	73/F0 73 [6]	73/na [6]
74	6	4D/CD [6]	74/F0 74 [6]	74/na [6]
75	Shift (left)	2A/AA	12/F0 12	12/F0 12
76	Z	2C/AC	1A/F0 1A	1A/F0 1A
77	X	2D/AD	22/F0 22	22/F0 22
78	C	2E/AE	21/F0 21	21/F0 21
79	V	2F/AF	2A/F0 2A	2A/F0 2A
80	B	30/B0	32/F0 32	32/F0 32

Continued

([x] Notes listed at end of table.)

Table C-2. Keyboard Scan Codes *(Continued)*

Key Pos.	Legend	Make / Break Codes (Hex) Mode 1	Mode 2	Mode 3
81	N	31/B1	31/F0 31	31/F0 31
82	M	32/B2	3A/F0 3A	3A/F0 3A
83	,	33/B3	41/F0 41	41/F0 41
84	.	34/B4	49/F0 49	49/F0 49
85	/	35/B5	4A/F0 4A	4A/F0 4A
86	Shift (right)	36/B6	59/F0 59	59/F0 59
87	↑	E0 48/E0 C8 E0 AA E0 48/E0 C8 E0 2A [4] E0 2A E0 48/E0 C8 E0 AA [6]	E0 75/E0 F0 75 E0 F0 12 E0 75/E0 F0 75 E0 12 [5] E0 12 E0 75/E0 F0 75 E0 F0 12 [6]	63/F0 63
88	1	4F/CF [6]	69/F0 69 [6]	69/na [6]
89	2	50/D0 [6]	72/F0 72 [6]	72/na [6]
90	3	51/D1 [6]	7A/F0 7A [6]	7A/na [6]
91	Enter	E0 1C/E0 9C	E0 5A/F0 E0 5A	79/F0 79[6]
92	Ctrl (left)	1D/9D	14/F0 14	11/F0 11
93	Alt (left)	38/B8	11/F0 11	19/F0 19
94	(Space)	39/B9	29/F0 29	29/F0 29
95	Alt (right)	E0 38/E0 B8	E0 11/F0 E0 11	39/na
96	Ctrl (right)	E0 1D/E0 9D	E0 14/F0 E0 14	58/na
97	←	E0 4B/E0 CB E0 AA E0 4B/E0 CB E0 2A [4] E0 2A E0 4B/E0 CB E0 AA [6]	E0 6B/Eo F0 6B E0 F0 12 E0 6B/E0 F0 6B E0 12[5] E0 12 E0 6B/E0 F0 6B E0 F0 12[6]	61/F0 61
98	↓	E0 50/E0 D0 E0 AA E0 50/E0 D0 E0 2A [4] E0 2A E0 50/E0 D0 E0 AA [6]	E0 72/E0 F0 72 E0 F0 12 E0 72/E0 F0 72 E0 12[5] E0 12 E0 72/E0 F0 72 E0 F0 12[6]	60/F0 60
99	→	E0 4D/E0 CD E0 AA E0 4D/E0 CD E0 2A [4] E0 2A E0 4D/E0 CD E0 AA [6]	E0 74/E0 F0 74 E0 F0 12 E0 74/E0 F0 74 E0 12[5] E0 12 E0 74/E0 F0 74 E0 F0 12[6]	6A/F0 6A
100	0	52/D2 [6]	70/F0 70 [6]	70/na [6]
101	.	53/D3 [6]	71/F0 71 [6]	71/na [6]
102	na	7E/FE	6D/F0 6D	7B/F0 7B
103	na	2B/AB	5D/F0 5D	53/F0 53
104	na	36/D6	61/F0 61	13/F0 13
110	(Win95) [7]	E0 5B/E0 DB E0 AA E0 5B/E0 DB E0 2A [4] E0 2A E0 5B/E0 DB E0 AA [6]	E0 1F/E0 F0 1F E0 F0 12 E0 1F/E0 F0 1F E0 12 [5] E0 12 E0 1F/E0 F0 1F E0 F0 12 [6]	8B/F0 8B
111	(Win95) [7]	E0 5C/E0 DC E0 AA E0 5C/E0 DC E0 2A [4] E0 2A E0 5C/E0 DC E0 AA [6]	E0 2F/E0 F0 27 E0 F0 12 E0 27/E0 F0 27 E0 12 [5] E0 12 E0 27/E0 F0 27 E0 F0 12 [6]	8C/F0 8C
112	(Win Apps) [7]	E0 5D/E0 DD E0 AA E0 5D/E0 DD E0 2A [4] E0 2A E0 5D E0 DD E0 AA [6]	E0 2F/E0 F0 2F E0 F0 12 E0 2F/E0 F0 2F E0 12 [5] E0 12 E0 2F/E0 F0 2F E0 F0 12 [6	8D/F0 8D
113	(Erase-Ease) [8]	0E/8E	66/F0 66	66/na

NOTES:

All codes assume Shift, Ctrl, and Alt keys inactive unless otherwise noted.
NA = Not applicable
[1] Shift (left) key active.
[2] Ctrl key active.
[3] Alt key active.
[4] Left Shift key active. For active right Shift key, substitute AA/2A make/break codes for B6/36 codes.
[5] Left Shift key active. For active right Shift key, substitute F0 12/12 make/break codes for F0 59/59 codes.
[6] Num Lock key active.
[7] Windows keyboards only
[8] Erase-Ease keyboards only

C.3 SCANNER DESCRIPTION

The scanner keyboard, available as an option, integrates a scanner with a SpaceSaver Windows ’95 keyboard, providing the ability to scan hardcopy looseleaf documents for faxing or electronic storage. The scanner provides resolutions up to 400 dpi and 256 shades of gray and outputs through a standard serial interface to the system unit. Using optical character recognition (OCR) support software, printed textual data can be converted into editable files.

Operation of the scanner starts automatically when a sheet is inserted into the Contact Image Sensor (CIS). A button on the left side of the keyboard allows then operator to open a menu, halt scanning in progress, or invoke a serial port test. Figure C-9 shows a block diagram of the key scanner elements.

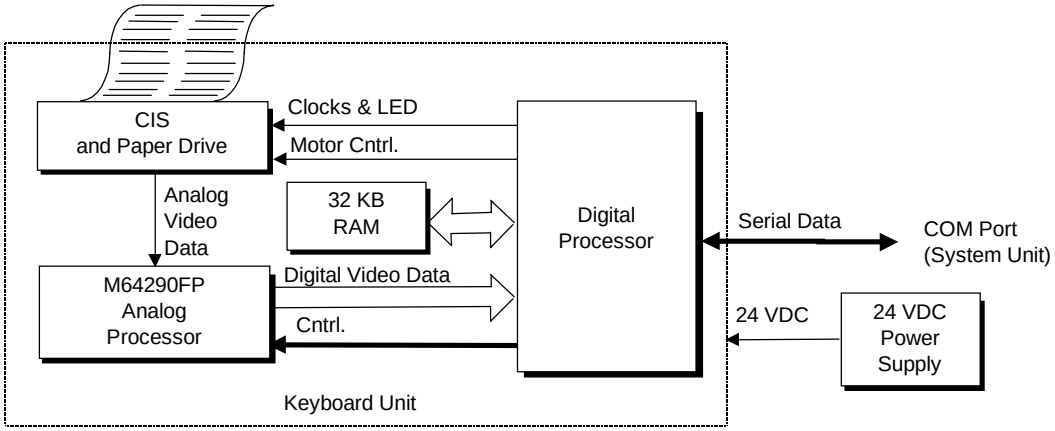


Figure C–9. Scanner Elements, Block Diagram

The Contact Image Sensor (CIS) and paper drive unit handles the hardcopy input. As each sheet is placed into the input slot, the sheet activates the mechanism and is drawn through and scanned by an LED illumination/photodiode sensor array. The drive motor provides 96 steps per revolution (3.75 degress per step) and is geared for 0.005 inch document movement per step for a resolution of 200 dpi. Half-stepping provides 400 dpi vertical resolution.

An analog video data stream is developed and routed to the Digital-to-Analog (D/A) Processor for conversion to digital video data that is routed to the Digital Processor. The Digital Processor provides most of the control of the scanner operation. A 32-KB RAM provides storage of executable code, pixel-to-pixel correction values, image processing line/diffusion data, and transmission data buffering.

The scanner elements are powered from an external 24 VDC power supply. Internal components use +5, +9, and -12 VDC.

C.3.1 SCANNER OPERATION

The scanner requires minimum user interface for normal operation. Insertion of a sheet of hardcopy activates the scanner. Operating parameters such as resolution, brightness, and motor speed are programmable for optimum performance. Other characteristics such as gamma correction, modulation transfer function (MTF), image compression, and pixel normalization are optimized through the use of pre-computed tables that are downloaded for image correction and adjustments when necessary.

The user interface is provided through a button located to the left of the sheet insertion tray. This normally-open switch provides the following functions depending on when pressed:

When Pressed	Function
During Power-Up	Scanner enters communications loopback mode. Mode remains in effect until the next power cycle (cold boot).
Scanner at idle	Actives a menu for changing/viewing parameters.
During a scan	Aborts the scan and reverses the motor, backing the document out of the scanner.

An inserted document activates one or more of five sensing fingers mounted on a shaft. The shaft begins rotation, turning an opaque flag that breaks an opto-interrupter beam between an LED and a phototransistor. The paper sensor signal goes active high, initiating the Digital Processor to begin the scanning process.

An LED/phototransistor assembly similar to the paper sensor is used for skew control. Sensing fingers on each side of the paper path check for misalignment (skew) of the document as it is pulled through the scan area. If the document comes in contact with one of the sensor fingers, an opaque flag is engaged to rotate, blocking an opto-interrupter beam and initiating an abort sequence. The skew LEDs , along with the LEDs used for scanning, are only powered up during the scan operation (i.e., while a document is in the scanner).

A flow chart of the scanning operation is shown in Figure C-10. Photo-Response Non-Uniformity (PRNU) refers to the fact that not every photosensor in the CIS has the same sensitivity. The PRNU correction stage adjusts for each photosensor's sensistivity level by applying a unique offset and gain value for it. A calibration procedure (initially done at the factory) is used to determine the compensation values for the photo array of the CIS. This data is stored in the CALIBRAT.DAT file on the installation disk and copied to the system unit's hard drive. The data is downloaded to the scanner after power up.

The modulation transfer function (MTF) of the optical system and document motion is corrected by downloading the MTF compensation parameters from the system unit to improve the quality of the scanned image.

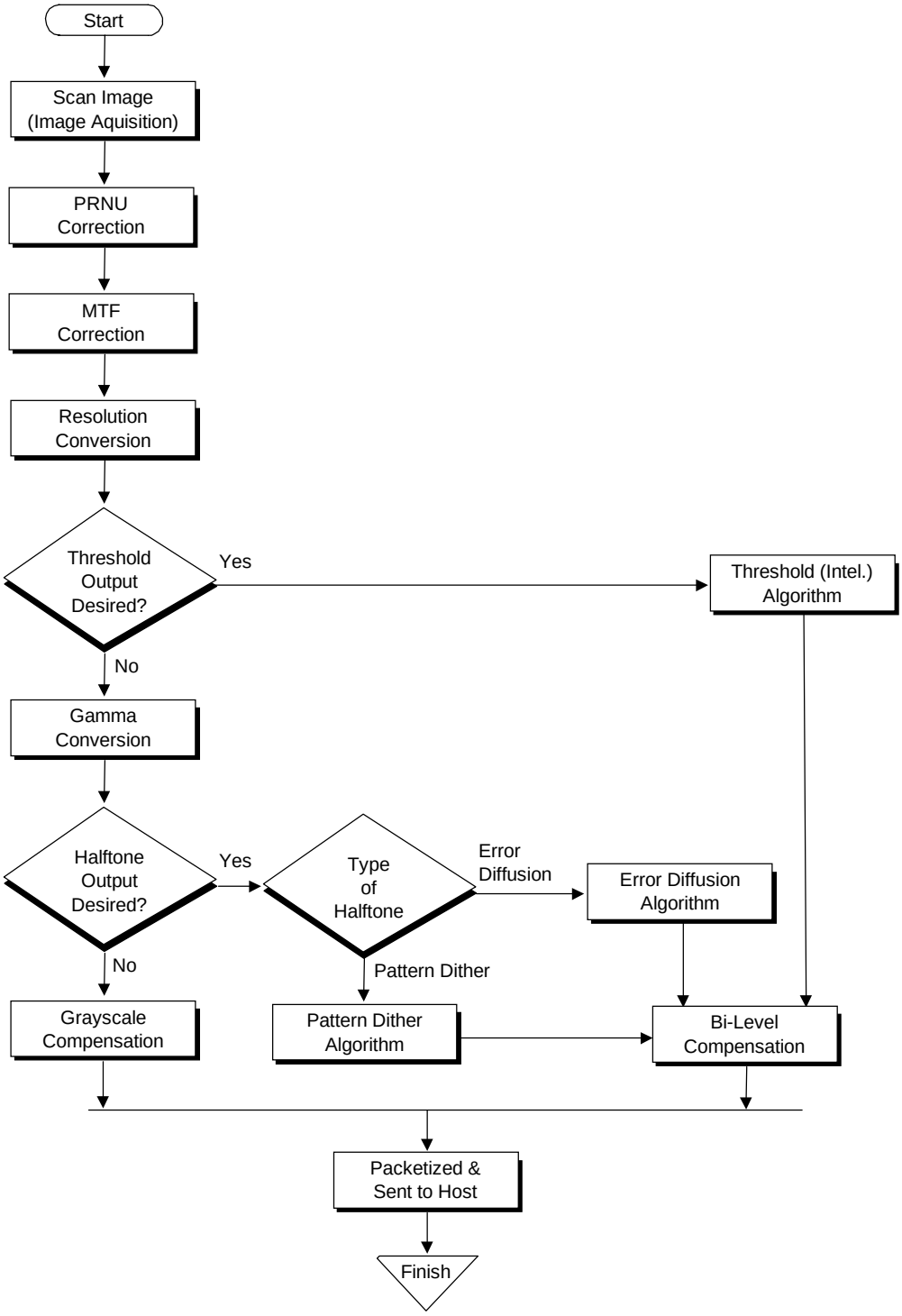


Figure C–10. Scanner operation Flow Chart

C.3.1.1 Resolution/Shade Depth

The drive motor mechanism of the CIS supports a vertical resolution of 400 dpi. The CIS provides a maximum horizontal resolution of 200 dpi. These factors provide true spatial resolutions of 100 and 200 dpi. Using horizontal interpolation, pseudo 300 and 400 dpi spatial resolutions are possible. Shade depth is determined by the number of bits used to control each pixel. The bits per pixel (bpp) parameter can be set to one (for black and white), two, four, or eight (for 256 shades of gray).

The selected resolution/shade depth determines the scanning time of a given sheet. Table C-3 lists the approximate scanning times for a standard 11 inch sheet using specified resolution/shade depths based on the line integration time of 2.5 ms.

Table C-3.
Scanner Performance Chart

		Scan Time for 11" Page		
X / Y	**DPI**	**1 bpp**	**4 bpp**	**8 bpp**
100 / 100	100	7 sec	11 sec	14 sec
200 / 200	200	7 sec	27 sec	36 sec
200 / 300	300 (Pseudo)	12 sec	60 sec	60 sec
200 / 400	400 (Pseudo)	17 sec	62 sec	80 sec

NOTE:
Scan times measured on a Pentium/90-based system with 16 MB RAM.

C.3.1.2 Image Quality

Brightness is fully programmable and independently adjustable using either normal or intelligent methods. The normal method slices each gray scale pixel into either black or white depending on the threshold value selected. The intelligent method automatically adjusts the pixel to the background for the best detail.

The grayscale transfer function can be tailored by gamma correction values that are downloaded from the system. This function can be disabled if desired.

Compensation for the Modulation Transfer Function (MTF) of the optical system and document motion is provided for improving image quality. The MTF parameters are /downloaded from the host if (if enabled).

Image compression is provided through a table-driven compressor. Compression values are loadable from the host and used by one of two types of algorithms: Huffman DPCM for 2- to 8-bit grayscale images, and a proprietary 1-bit compression.

C.3.2 SCANNER INTERFACE

The scanner communicates with the system unit (host) using a serial port as the primary choice of connection. The scanner interface is adaptable to several types of host connections as shown in Table C-4 (unshaded portion describes standard scanner interface with Compaq system unit).

Table C-4.
Scanner I/F Signals

Scanner Signals		Serial Port (PC)			Parallel Port		Serial Port (MacIntosh)	
Pnyb Mode	Mser Mode	RS232 Signal	DB9 Pin	DB25 Pin	Signal	DB25 Pin	Signal	DIN8 Pin
P0	SCLK	CTS	8	5	Select	13	HSKIn	2
P1		DSR	6	6	Paper Out	12	--	--
P2		RI	9	22	Ack	10	--	--
P3		DCD	1	8	Busy	11	--	--
PCLK	DTR	DTR	4	20	Strobe	1	HSKOut	1
SOUT	TXD	RTS	7	4	Init	16	TXD	6
GND	--	GND	5	7	GND	18	GND/RXD+	4/8
PnP	RXD	--	2	3	--	--	RXD-	5

Optional interface configuration.

The scanner uses one of two communication modes; Pnyb and Mser. The scanner selects the mode based on the idle status of the DTR/PCLK signal. If detected in a low state, the scanner uses the Pnyb mode. If PCLK is detected in a high state at idle, then the Mser mode is used.

Switching between the Pnyb and Mser modes is automatic and transparent to the operating system and application. This allows the scanner to be configured through an A/B box to two systems using different interfaces. The system unit (host) must drive the DTR signal at the appropriate level for at least 20 us before transmitting data packets.

A packet consists of an exchange of one or more bytes between the scanner and the host. A session is an exchange of packets between the scanner and the host. A session begins with a single-byte packet called a wakeup code and ends with the transfer of an acknowledgment (ACK) of the last packet received. Either the scanner or the host can initiate a session, and a session can be ended or cancelled by the scanner or the host, regardless of which initiated the session. A session is restricted to the action specified in the wakeup code.

C.3.2.1 Pnyb Mode

In the parallel nibble or "Pnyb" mode, the scanner transfers scanned information to the system unit (host) four bits (a nibble) at a time using the P3..P0 signals, which conform to RS-232 voltage and timing specifications. The P3..P0 signals are mapped to bits <7..4> respectively of the Modem Status Register (primary address 3FEh). The nibbles are clocked into the host with each transition of the PCLK signal. PCLK transitions from low to high clock in a high nibble, which transitions from high to low clock in a low nibble. The host can assume a nibble from the scanner is ready to be read 3.3 us after the PCLK transition requesting it. At the end of a scanner-to-host packet transfer, the host toggles the PCLK signal an extra time (0-to-1-to-0). This extra toggle indicates to the scanner that the last nibble has been read and sets the P3..P0 lines signals to a waiting state.

Data from the system unit (host) is transferred serially (bit-by-bit) as the SO signal along with the PCLK signal. A data bit is clocked with each transition of the PCLK signal so that a byte is transferred with four PCLK cycles. These signals also conform to RS-232 voltage and timing specifications and are mapped at bits <1,0> of the Modem Control Register (primary address 3FCh). The scanner can read data as long as the setup time is at least 1 us and the hold time is at least 3.3 us. The host must allow an additional 50 us after sending the LSb of each of the first five bytes of a multi-byte packet to the scanner. During host-to-scanner transfers, the scanner uses the P3..P0 lines for indicating transmission status to the host.

In the Pnyb mode, the host must insure that the high state of the first PCLK cycle of a session completes in less than 10 us so that the scanner does not interpret a Mser mode transfer.

C.3.2.2 Mser Mode (MacIntosh Connection Only)

The MacIntosh Serial or "Mser" mode uses bit-serial transfers for both scanner-to-host (RXD signal) as well as host-to-scanner (TXD signal) transfers. Transfers are accomplished using 10-bit frames that consist of a start bit, a data byte (LSb first), and a stop bit. The clock (SCLK) signal is provided by the scanner. The Mser mode is similar to isochronous transmission.

C.3.3 SCANNER SPECIFICATIONS/REQUIREMENTS

Table C-5.
Scanner Specifications

Parameter	Specification [1]
Dimensions (Complete keyboard unit):	
Width	20.5 in (52.07 cm)
Height	2.5 in (6.35 cm)
Depth	9 in (22.86 cm)
Weight (Complete keyvoard unit)	10.1 lb (4.58 kg)
Scanner Paper Sizes:	
Minimum	2.0 x 3.0 in (5.1 x 7.6 cm)
Maximum	8.5 x 30 in 21.6 x 76.2 cm)
Maximum Scanned Resolution (input)	2400 x 2400 dpi
Maximum Scanning Resolution (output)	400 dpi
Maximum Scan Time (8.5 x 11" sheet)	6 seconds [2]
Power Requirements (Scanner only):	
Input Voltage	24 VDC
Maximum Current Drain (scanning)	990 ma
Environmental Conditions:	
Tempurature, operating	50°-104° F (10°-40° C)
Tempurature, non-operating	-4°-140° F (-20°-60° C)
Humidity, operating	20-80% RH
Humidity, non-operating	5-95% RH

NOTE:
[1] Metric numbers shown in parenthesis.
[2] Based on Pentium/90-based system w/16 MB RAM

The scanner imposes the following requirements on the host system:

- 486 or better microprocessor
- Serial port
- Windows 3.1, Windows for Workgroups 3.11, or Windows 95 or later
- 4 megabytes of RAM (8 megabytes recommended)
- 50 megabytes free disk space

Appendix D
MATROX MILLENNIUM GRAPHICS CARD

D.1 INTRODUCTION

This appendix describes the Matrox Millennium Graphics Card used in some models. The Matrox Millennium Graphics Card is based on the MGA 2064Wgraphics controller. This appendix covers the following subjects:

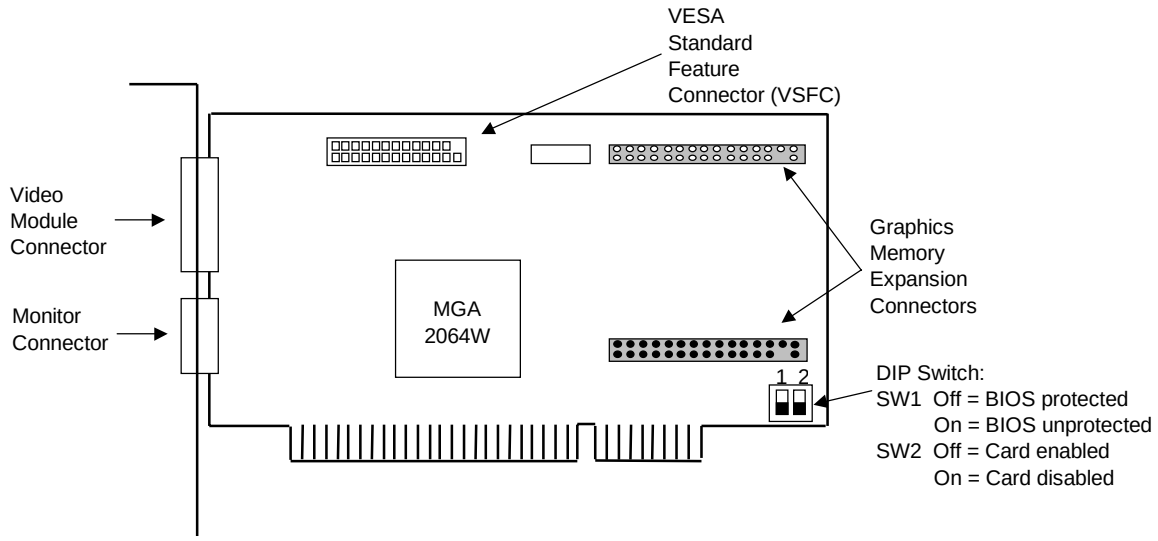


Figure D–1. Matrox Millennium Graphics Card Layout

D.2 FUNCTIONAL DESCRIPTION

The Matrox MGA Millennium Graphics Card installs in a PCI slot. This graphics card is based on the MGA 2064W graphics controller and comes standard with two megabytes of WRAM for the frame buffer (Figure D-2). The RAMDAC functions are provided by the TVP 3026 component. The card can be disabled by setting DIP switch position 2 to Off if another graphics controller is to be used in the system.

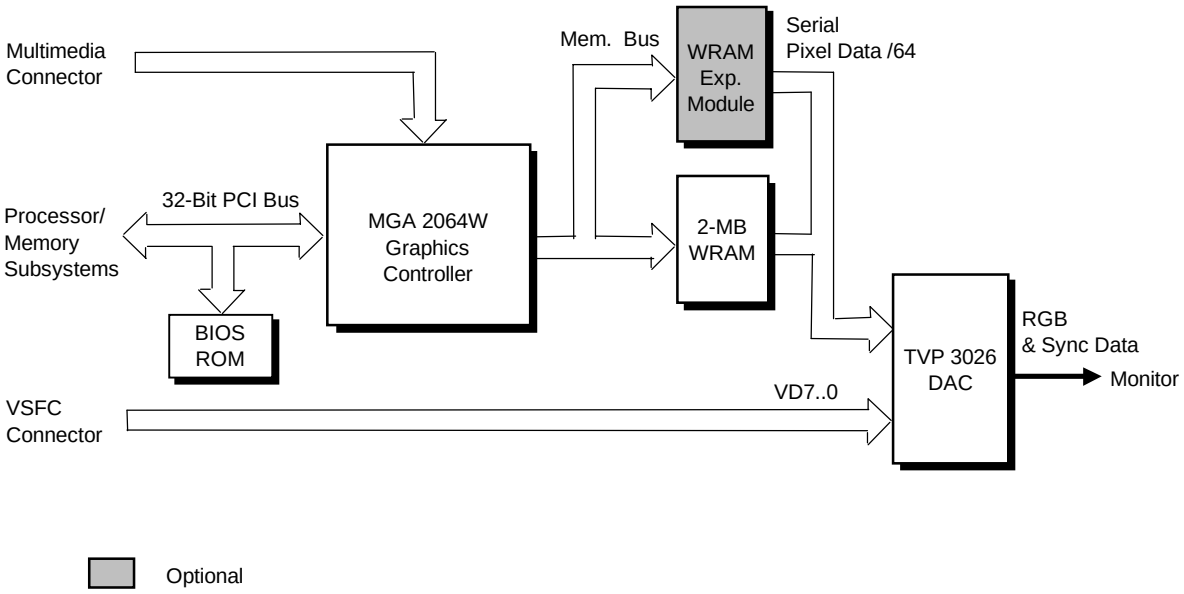


Figure D–2. Matrox MGA Millennium Graphics Card Block diagram

The Matrox Millennium Graphics Card includes the following features:

- Hardware-accelerated true-color mode support
- Hardware-assited texture mapping
- Aligned BitBLT support
- WRAM Dual-color block write mode support
- Phase-Locked-Loop (PLL) clock select for programmable dot/memory frequencies
- Hardware cursor controller (64x64x2 cursor) compatible with XGA and X-Windows
- Overscan support for creating custom screen borders

The Windows RAM (WRAM) used by the Millennium card provides high performance for full motion video requirements. By handling most block transfers (BLTs) internally, the WRAM relieves the graphics controller from having to provide direct support for most video and drawing tasks.

The standard two megabytes of WRAM is expandable by adding a 2- or 6-MB WRAM module, increasing the total graphics memory to eight megabytes. Adding WRAM increases the resolution and color depth capability of the graphics controller (refer to Table D-2).

The BIOS for the graphics controller is contained in flash ROM. To upgrade the BIOS, the ROM can be flashed with new firmware from a diskette. Before initiating the flash procedure, DIP switch position 1 must be set to On.

D.3 DISPLAY CONFIGURATIONS

D.3.1 TEXT CONFIGURATIONS

The text display uses a multiplane configuration where a character, its attributes, and fonts are stored in separate frame buffer memory planes. Table D-1 lists the text configurations provided by the graphics subsystem. Note that text configurations for CGA.MDA, EGA, and VGA share common video BIOS modes that result in same format, but provide different pixel resolutions.

Table D-1.
Text Configuration Display Modes

Software Interface	BIOS Mode	Pixel Resolution	Color Depth	Format
CGA	00h	320 x 200	16	40 x 25
	01h	320 x 200	16	40 x 25
	02h	640 x 200	16	80 x 25
	03h	640 x 200	16	80 x 25
MDA	07h	720 x 350	Mono	80 x 25
EGA	00h	320 x 350	16	40 x 25
	01h	320 x 350	16	40 x 25
	02h	640 x 350	16	80 x 25
	03h	640 x 350	16	80 x 25
VGA	00h	360 x 400	16	40 x 25
	01h	360 x 400	16	40 x 25
	02h	720 x 400	16	80 x 25
	03h	720 x 400	16	80 x 25
	07h	720 x 400	Mono	80 x 25
EVGA	14h	1056 x 400	16	132 x 25
	45h	1056 x 350	16	132 x 43
	55h	1056 x 350	16	132 x 25

D.3.2 GRAPHICS CONFIGURATIONS

The Matrox Millennium graphics card directly supports standard CGA, EGA, and VGA modes. Using the supplied drivers, the Matrox Millennium graphics card supports the extended VGA modes listed in the following table:

Table D-2.
Extended VGA Display Modes

VESA Mode	Pixel Resolution	Color Depth	Max. Refresh Rate [1]	Amount of WRAM Required
100h	640 x 400 @ 8 bpp	256	200 Hz	2 MB
101h	640 x 480 @ 8 bpp	256	200 Hz	2 MB
102h	800 x 600 @ 4 bpp	16	200 Hz	2 MB
103h	800 x 600 @ 8 bpp	256	200 Hz	2 MB
104h	1024 x 768 @ `4 bpp	16	130 Hz	2 MB
105h	1024 x 768 @ 8 bpp	256	130 Hz	2 MB
107h	1280 x 1024 @ 8 bpp	256	100 Hz	2 MB
110h	640 x 480 @ 15 bpp	32K	200 Hz	2 MB
111h	640 x 480 @ 16 bpp	64K	200 Hz	2 MB
112h	640 x 480 @ 32 bpp	16M	200 Hz	2 MB
113h	800 x 600 @ 15 bpp	32K	200 Hz	2 MB
114h	800 x 600 @ 16 bpp	64K	200 Hz	2 MB
115h	800 x 600 @ 32 bpp	16M	200 Hz	2 MB
116h	1024 x 768 @ 15 bpp	32K	130 Hz	2 MB
117h	1024 x 768 @ 16 bpp	64K	130 Hz	2 MB
118h	1024 x 768 @ 32 bpp	16M	130 Hz	4 MB
119h	1280 x 1024 @ 15 bpp	32K	100 Hz	4 MB
11Ah	1280 x 1024 @ 16 bpp	64K	100 Hz	4 MB
11Bh	1280 x 1024 @ 32bpp	16M	100 Hz	8 MB
11Ch	1600 x 1200 @ 8 bpp	256	78 Hz	2 MB
11Dh	1600 x 1200 @ 15 bpp	32K	78 Hz	4 MB
11Eh	1600 x 1200 @16 bpp	64K	78 Hz	4 MB

NOTES:

[1] Default refresh rate for VESA modes is 60 Hz. Higher rates can be set through MGA CAD and DOS software.

Operation is non-interleaved for all modes. The Matrox Millennium graphics card includes a ROM that contains the video graphics BIOS firmware and is directly compatible with software written for VGA, EGA, and CGA modes. For extended graphics modes, drivers are supplied with systems that include this card. For detailed programming information refer to appropriate Matrox documentation.

D.4 PROGRAMMING

D.4.1 CONFIGURATION

The Matrox Millennium graphics card works off the PCI bus and is configured through the MGA 2064W's PCI configuration space registers (listed in Table D-3) using PCI protocol. These registers are configured by BIOS during POST to the default configuration.

Table D-3.
MGA 2064W PCI Configuration Space Registers

PCI Config. Address	Function	PCI Config. Address	Function
00h	Vender ID (102Bh)/Device ID (0519h)	14h	Relocateable I/O Base Address
04h	PCI Command	30h	Expansion ROM Base Address
08h	Status	3Ch	Interrupt Line / Interrupt Pin
10h	Display Memory Base Address	--	--

For a discussion of accessing PCI configuration space registers refer to chapter 4. For a detailed description of registers refer to Matrox documentation for the MGA 2064W controller.

D.4.2 CONTROL

Table D-4 lists the standard VGA control registers of the MGA 2064W. These registers can be directly accessed by software written for standard VGA modes.

Table D-4.
Standard VGA Mode I/O Mapping

I/O Address	Function	I/O Address	Function
3B5.00..26h*	CRT Controller (mono)	3C6h..3C9h	RAMDAC
3BAh	VSYNC Control, Display Status	3CAh	Read VSYNC Status
3C1.00..14h*	Attribute Controller	3CCh	Misc. Control, Read
3C2h	Misc. Control / Status	3CF.00..08h	Graphics Controller
3C5h.00..04h*	Sequencer	3D5.00..26h*	CRT Controller (color)
--	--	3DAh	VSYNC Control, Display Status (color)

* Index at base minus 1 (i.e., if base is 3B5h, index is at 3B4h).

Extended VGA modes require the use of drivers supplied by Matrox with the system containing the card. Refer to Matrox documentation for detailed programming information on extended modes.

D.5 CONNECTORS

There are two connectors associated with the graphics subsystem; the display monitor connector and the VGA passthrough connector (also known as the VESA Standard Feature Connector (VSFC)).

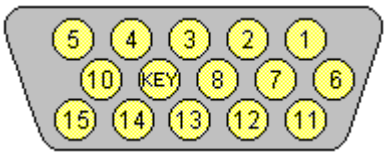


Figure D–3. VGA Monitor Connector, (Female DB-15, as viewed from rear).

Table D-5.
DB-15 Monitor Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	R	Red Analog	9	NC	Not Connected
2	G	Blue Analog	10	GND	Ground
3	B	Green Analog	11	Mon. ID	Monitor Identification
4	Mon ID	Monitor Identification	12	SDA	DDC2-B Data
5	GND	Ground	13	HSync	Horizontal Sync
6	R GND	Red Analog Ground	14	VSync	Vertical Sync
7	G GND	Blue Analog Ground	15	SCL	DDC2-B Clock
8	B GND	Green Analog Ground	--	--	--

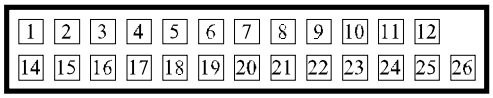


Figure D–4. VGA Pass-Through Connector (VSFC) (26-Pin Header)

Table D-6.
VGA Passthrough Connector (VSFC) Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	14	P0	Pixel Data 0
2	GND	Ground	15	P1	Pixel Data 1
3	GND	Ground	16	P2	Pixel Data 2
4	EVIDEO-	Overlay Enable	17	P3	Pixel Data 3
5	ESYNC-	External Sync Enable	18	P4	Pixel Data 4
6	EDCLK	External Clock Enable	19	P5	Pixel Data 5
7	NC	not connected	20	P6	Pixel Data 6
8	GND	Ground	21	P7	Pixel Data 7
9	GND	Ground	22	DCLK	Pixel Data Clock
10	GND	Ground	23	BLANK	DAC Output Blanking
11	GND	Ground	24	HSYNC	Horizontal Sync
12	NC	not connected	25	VSYNC	Vertical Sync
13	--	KEY	26	GND	Ground

D.6 SPECIFICATIONS

Table D–7. Matrox Millennium Graphics Card Specifications

Paramemter	
Default Mode	VGA text mode 3
Current Drain:	
No memory module	0.6 A
w/ 2-MB WRAM module	0.8 A
w/ 8-MB WRAM module	1.0 A
Video Output:	
Standard	OS/2
Voltage level:	
Black or blank	0.0 V
White	0.700 V
System Requirements:	
CPU Type	486 or better
System RAM amount	4 MB
OS	DOS 5.0, OS/2 2.1 or Warp, WinNT 3.5, Win 3.1 [1]
Physical Dimensions (excluding brackets)	16.5 cm x 9.5 cm x 1.2 cm
Environmental Specifications:	
Ambient Operating Temperature	0° C - 55° C
Storage Temperature	-40° C - 75° C
Maximum Operating Alttitude	3,000 m
Maximum Non-Operating Altitude	12,000 m
Operating Humidity	20 - 80 % rh (non-cond)
Storage Humidity	5 - 95 % rh (non-cond)

NOTE:

[1] Later versions of listed operating systems should be acceptable.

This page is intentionally blank.

Appendix E
ELSA GLoria-L GRAPHICS CARD

E.1 INTRODUCTION

This appendix describes the ELSA GLoria-L Graphics Card used in some models. This graphics card use a 64-bit 3-D graphics engine and double-buffering features to provide high performance 2-D and 3-D imaging. This card is directly compatible with software written for standard VGA applications. The card installs in a PCI slot and the video drivers are included with the system to support the extended modes.

> **NOTE:** This appendix provides an overview of the ELSA product. For detailed information, the OEM documentation should be referenced.

This appendix covers the following subjects:

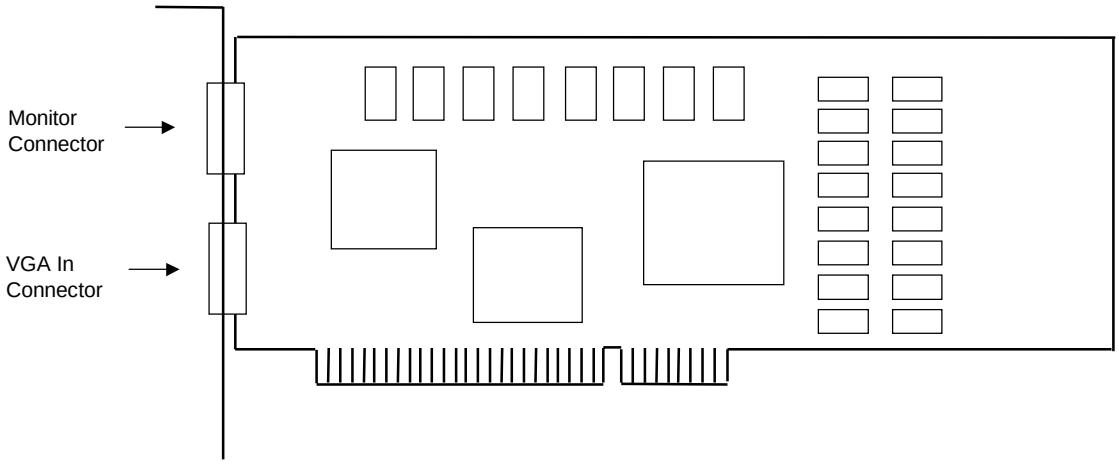


Figure E–1. ELSA GLoria-L Graphics Card Layout

E.2 FUNCTIONAL DESCRIPTION

The GLoria-L Graphics Card installs in a PCI slot. The card is based on the GLINT 500TX 2D/3D rendering processor supported by two separate memory sections; a local buffer using DRAM and a frame buffer using dual-ported VRAM. The 500TX processor provides hardware-accelerated support for the OpenGL professional 3D API. Drivers are supplied for operation using Direct3D and DirectDraw, and Windows 95 and Windows NT 2-D applications.

For 2-D/3-D operations, two memory buffers (local and frame) are provided. The Local buffer is utilized for texture data, stencils, and Z-buffering. The card includes eight megabytes of DRAM for the local buffer and is expandable to 16 megabytes. The Frame buffer holds the main display data and incorporates eight megabytes of VRAM. The pixel data of the final display is outputted directly to the IBM RGB526 DB22 RAMDAC that converts the digital data to an analog output for the monitor.

The GLoria-L Graphics Card incorporates the GLINT Delta Geometry Pipeline Processor. The GLINT Delta reduces CPU intervention by providing a hardware solution for 3D geometry setup. In addition, the GLINT Delta performs PCI bus adapter chores, providing an intermediate interface for the GLINT 500TX and S3 ViRGE components, which are qualified PCI devices in of themselves.

The S3 ViRGE VGA processor is supported by it's own 1-MB frame buffer and BIOS. The ViRGE and it's BIOS are addressed during POST in standard video space.

> **NOTE:** The ViRGE can be disabled and an external VGA controller used in its place. This is accomplished by setting the DIP switch on the GLoria-L card to the "On" position and connecting the RGB output of the external VGA controller to the VGA In connector of the GLoria-L card.

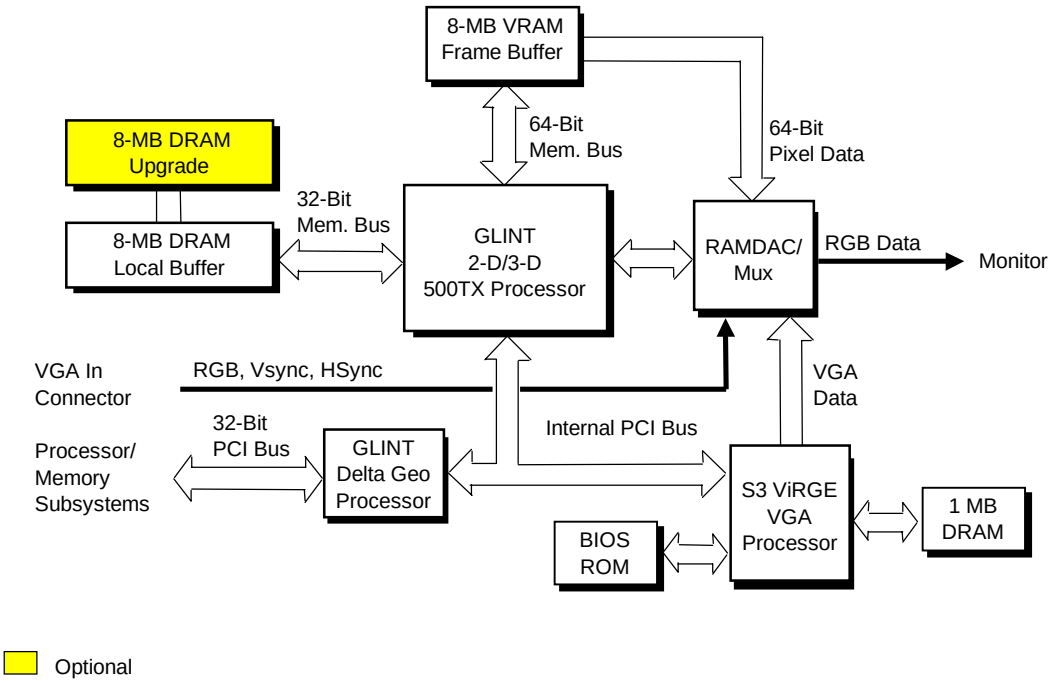


Figure E–2. ELSA GLoria-L Graphics Card Block diagram

E.3 GRAPHICS MODES

Table E-1.
ELSA GLoria-L Graphics Modes

Resolution	Refresh Rates (Hz)	Available Texture Memory [3]	Double Buffering Support [1]			
				15 bpp [2]		
			8 bpp	5:5:5	5:5:5DB	32 bpp (8:8:8)
640 x 480	60, 70, 75, 80, 85, 100	6.83 MB	BLT	BLT/Flip	Pixel	BLT/Flip
800 x 600	60, 70, 75, 80, 85, 100	6.17 MB	BLT	BLT/Flip	Pixel	BLT/Flip
1024 x 768	60, 70, 75, 80, 85, 100	5.0 MB	BLT	BLT/Flip	Pixel	BLT/Flip
1152 x 864	60, 70, 75, 80, 85, 100	4.20 MB	BLT	BLT/Flip	Pixel	BLT/Flip
1280 x 1024	60, 70, 75, 80, 85, 100	3.0 MB	BLT	BLT/Flip	Pixel	No
1536 x 1152	60, 70, 75, 80	1.25 MB	BLT	BLT/Flip	Pixel	No
1600 x 1200	60, 70, 75	0.68 MB	BLT	BLT/Flip	Pixel	No
1600 x 1280	60, 70	0.19 MB	BLT	BLT/Flip	Pixel	No

NOTES:

[1] BLT - Double buffering accomplished by block transferring the contents of the back buffer into the front buffer.

Flip - Double buffering accomplished by page-switching the output between the two buffers (limited to one window)

Pixel - Double buffering supported on a per-pixel basis. Each 32-bit element in both buffers contains two 15-bit pixels plus one bit to tell the RAMDAC which pixel to display. This allows for fast switching of multiple, independently-buffered windows.

[2] Software will select the appropriate mode (typically the 5:5:5DB (Pixel) mode since as it will deliver higher performance (several independent windows)).

[3] Amounts shown for standard 8-MB local buffer memory; can be increased by adding 8-MB upgrade option.

E.4 CONNECTORS

There are two connectors associated with the graphics cards; the display monitor connector and the VGA passthrough or "VGA In" connector.

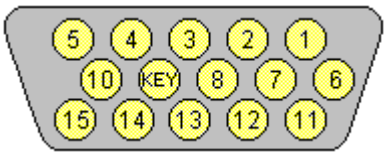


Figure E–3. VGA Monitor Connector, (Female DB-15, as viewed from rear).

Table E-2.
DB-15 Monitor Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	R	Red Analog	9	NC	Not Connected
2	G	Blue Analog	10	GND	Ground
3	B	Green Analog	11	Mon. ID	Monitor Identification
4	Mon ID	Monitor Identification	12	SDA	DDC2-B Data
5	GND	Ground	13	HSync	Horizontal Sync
6	R GND	Red Analog Ground	14	VSync	Vertical Sync
7	G GND	Blue Analog Ground	15	SCL	DDC2-B Clock
8	B GND	Green Analog Ground	--	--	--

The VGA IN connector allows an external VGA controller to be substituted for the ViRGE VGA component. The DIP switch must be set to the "On" position for the external VGA controller to be active.

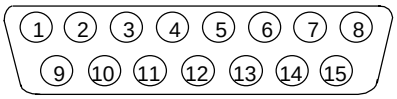


Figure E–4. VGA In Connector (15-Pin Sub-D, as viewed from rear)

Table E-3.
VGA In Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	VSYNC	Vertical Sync In	9	GND/SNS	Ground/Sense (conn. to pin3)
2	HSYNC	Horizontal Sync In	10	MON ID 2	Monitor ID 2
3	GND	Ground (sync)	11	B VID GND	Blue Video Ground
4	B VID	Blue Video In	12	MON ID 1	Monitor ID 1
5	DDC CLK	Clock In/Out	13	G VID GND	Green Video Ground
6	G VID	Green Video In	14	MON ID 0	Monitor ID 0
7	DDC CLK	Clock In/Out	15	R VID GND	Red Video Ground
8	R VID	Red Video In	--	--	--

E.5 SPECIFICATIONS

Table E-4.
ELSA GLoria-L Graphics Card Specifications

Parameter	GLoria-L Graphics Card
Chipset:	
2-D/3-D Processor	GLINT 500TX (50 MHz)
Geometry Processor	GLINT Delta (40 MHz)
VGA Processor	S3 ViRGE (50 MHz)
RAMDAC	RGB526DB (220 MHz)
Memory:	
Local Buffer	8 MB of 50 ns DRAM [1]
Frame Buffer	8 MB of 60 ns VRAM
VGA Processing	1 MB of 70 ns DRAM
Maximum Vertical Refresh Rate	200 Hz
Maximum Pixel Clock	200 MHz
Hardware Accelerated 3-D:	
32-/bit Z-Buffering	Yes
Gouraud Shading	Yes
Stencils	Yes
Texture Mapping	Yes
Current Drain:	
Standard Memory	+5 VDC @ 2.1 A
w/Memory Upgrade	+5 VDC @ 3.0 A

NOTES:

[1] Expandable to 16 megabytes with 8-MB upgrade module (Compaq p/n 270111-001)

INDEX