AL440LX Motherboard
Technical Product Specification

August 1997

Order Number 677028-001

The AL440LX motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the AL440LX Motherboard Specification Update.

Revision History

Revision	Revision History	Date
-001	First Release of the AL440LX Motherboard Technical Product Specification	August 1997

This product specification applies only to standard AL440LX motherboards with BIOS identifier 4A4LL0X0.86A.XXXX.PXX.

Changes to this specification will be published in the AL440LX Motherboard Specification Update before being incorporated into a revision of this document.

Contents

Figures

Tables

1 Motherboard Description

1.1 Overview

The AL440LX motherboard supports the following features:

Form factor

- ATX form factor of 12 x 7.75 inches

Processor

- Single Pentium® II processor
- 66 MHz bus speed
- Supports all Pentium II processor speeds, voltages, and bus frequencies
- 512 KB second-level cache on the substrate in the Single Edge Contact (S.E.C.) cartridge
- Slot 1 connector

Main memory

- Three 168-pin DIMM sockets
- Supports up to 384 MB of synchronous DRAM (SDRAM) memory
- ECC or non-ECC memory

Intel 440LX AGPset and PCI/IDE Interface

- Intel 82443LX PCI/A.G.P. controller (PAC)
  - Integrated PCI bus mastering controller
  - Integrated Accelerated Graphics Port (A.G.P.) controller
- Intel 82371AB PCI/ISA/IDE Xcelerator (PIIX4)
  - Supports up to four IDE drives or devices
  - Multifunction PCI-to-ISA bridge
  - USB and DMA controllers
  - Two fast IDE interfaces
  - Power management logic
  - Real-time clock

I/O features

- National PC97307 Super I/O controller
  - Integrates standard I/O functions: floppy-drive interface, one multimode parallel port, two FIFO serial ports, keyboard and mouse controller, IrDA†-compatible interface
- Two Universal Serial Bus (USB) interfaces

Five usable expansion slots:

- One ISA slot
- Three PCI slots
- One shared PCI/ISA slot

Other features

- Intel/Phoenix BIOS
- Onboard A.G.P. connector
- Plug and Play compatible
- Single-jumper configuration
- Advanced Power Management (APM)
- Wake on Ring header

Software drivers and utilities are available from Intel.

1.2 Manufacturing Options

The following are manufacturing options:

- Audio subsystem
  - — Yamaha OPL3-SA codec audio component
  - — Yamaha OPL4-ML wavetable synthesizer component
  - — Yamaha reference-design wavetable module
  - — Back panel audio connectors: Line In, Line Out, Mic In
  - — MIDI game port
  - — Line In connector
  - — CD-ROM audio connector
- Management extension hardware
- Wake on LAN† header
- Chassis security header
- Telephony connector
- SCSI hard disk LED header

1.3 Motherboard Components

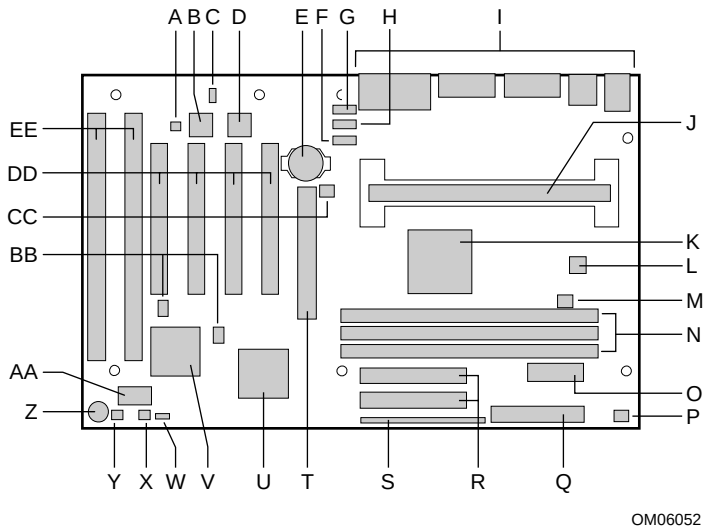

Figure 1. Motherboard Components

A	Optional chassis security header	Q	Floppy drive connector
B	Optional Yamaha OPL4-ML component	R	IDE connectors
C	Optional Wake on LAN header	S	Front panel header
D	Optional Yamaha OPL3-SA3 component	T	Accelerated Graphics Port (A.G.P.) connector
E	Battery	U	Intel 82371AB (PIIX4)
F	Optional Line In connector	V	National PC97307 I/O controller
G	Optional CD-ROM audio connector	W	Configuration header
H	Optional telephony connector	X	Optional SCSI hard disk LED header
I	Back-panel I/O connectors	Y	Wake on Ring header
J	Slot 1 connector	Z	Speaker
K	Intel 82443LX (PAC)	AA	2 Mbit TSOP flash
L	Optional management extension hardware	BB	Optional Yamaha wavetable module headers
M	Fan 3 header (active heatsink fan)	CC	Fan 2 header
N	DIMM sockets	DD	PCI connectors
O	Primary power connector	EE	ISA connectors
P	Fan 1 header		

1.4 Form Factor

The motherboard is designed to fit into a standard ATX form-factor chassis. The outer dimensions are 12 x 7.75 inches. Figure 2 shows that the mechanical form factor, the I/O connector locations, and the mounting hole locations are in compliance with the ATX specification (see Section 6.2).

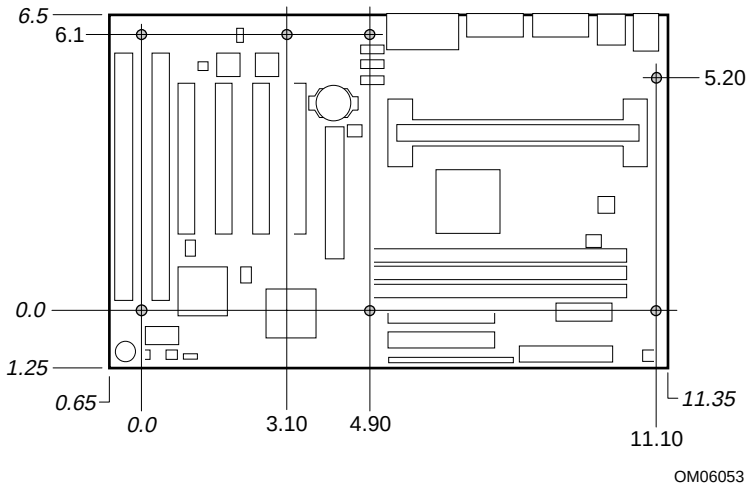

Figure 2. Motherboard Dimensions

1.5 I/O Shield

The back panel I/O shield for the motherboard must meet specific dimension and material requirements. Systems based on this motherboard need the back panel I/O shield to pass certification testing. Figure 3 shows the critical dimensions of the chassis-dependent I/O shield. Figure 4 shows the critical dimensions of the chassis-independent I/O shield. Both figures indicate the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 6.2 for information about the ATX specification.

NOTE

An I/O shield specifically designed for the Intel ATX chassis is available from Intel.

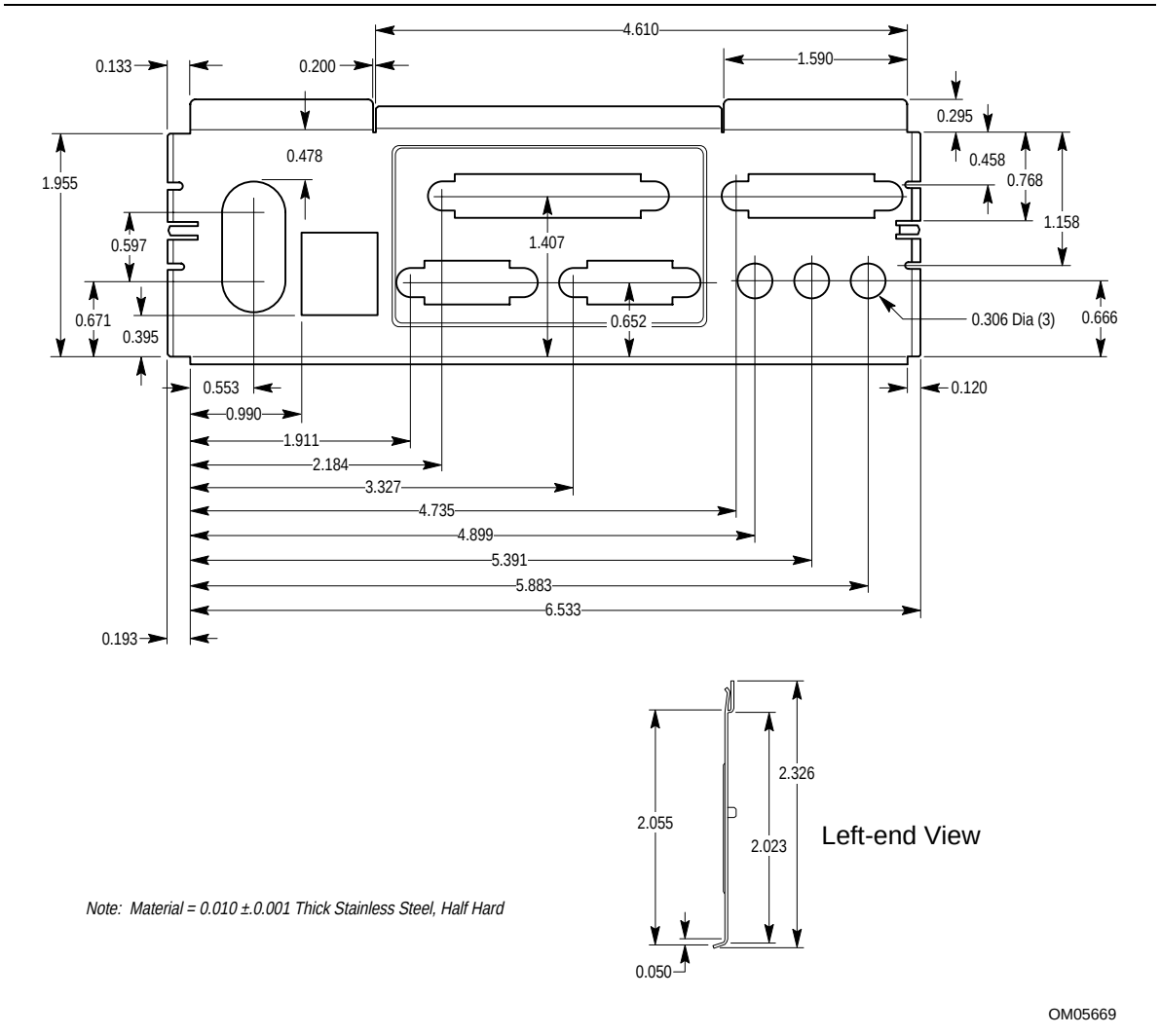

Figure 3. Back Panel I/O Shield Dimensions (ATX Chassis-Dependent)

NOTE

A chassis-independent I/O shield designed to be compliant with the ATX chassis specification 2.01 is available from Intel.

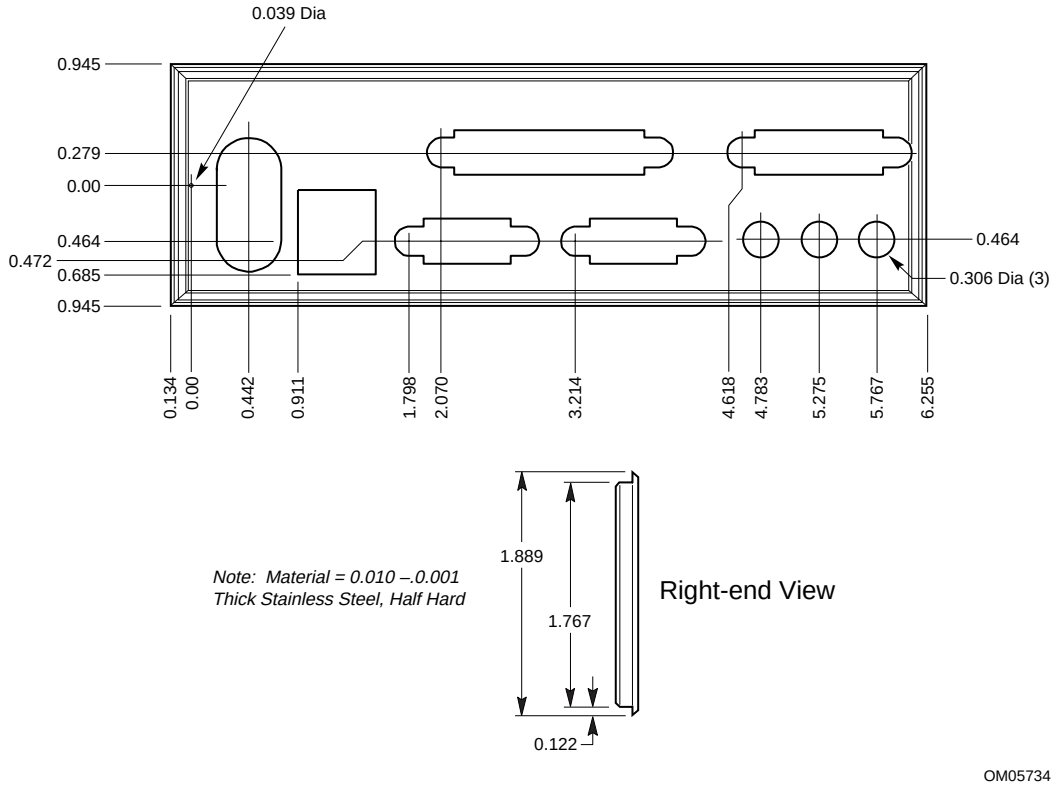

Figure 4. Back Panel I/O Shield Dimensions (ATX Chassis-Independent)

1.6 Processor

The motherboard supports a single Pentium II processor. The processor's VID pins automatically program the voltage regulator on the motherboard to the required processor voltage. The motherboard currently supports processors that run internally at 233, 266, or 300 MHz and have a 512 KB second-level cache.

The processor implements MMX™ technology and maintains full backward compatibility with the 8086, 80286, Intel386™, Intel486™, Pentium, and Pentium Pro processors. The processor's numeric coprocessor significantly increases the speed of floating-point operations and complies with ANSI/IEEE standard 754-1985.

1.6.1 Processor Packaging

The processor is packaged in a Single Edge Contact (S.E.C.) cartridge. The cartridge includes the processor core, second-level cache, thermal plate, and back cover.

The processor connects to the motherboard through the Slot 1 connector, a 242-pin edge connector. When mounted in Slot 1, the processor is secured by a retention mechanism attached to the motherboard. The heatsink is stabilized by a heatsink support that is attached to the motherboard.

1.6.2 Second Level Cache

The second-level cache is located on the substrate of the S.E.C. cartridge. The cache includes burst pipelined synchronous static RAM (BSRAM) and tag RAM. There are four BSRAM components totaling 512 KB in size. All supported onboard memory can be cached.

1.6.3 Processor Upgrades

The motherboard can be upgraded with Pentium II processors that run at higher speeds. When upgrading the processor, use the BIOS configuration mode to change the processor speed (see Section 1.15.2).

1.7 Memory

1.7.1 Main Memory

The motherboard has three dual inline memory module (DIMM) sockets. Minimum memory size is 8 MB; maximum memory size is 384 MB. The BIOS automatically detects memory type, size, and speed.

The motherboard supports the following memory features:

- 168-pin DIMMs with gold-plated contacts
- 66 MHz SDRAM only
- Non-ECC (64-bit) and ECC (72-bit) memory
- 3.3 V memory only
- Single- or double-sided DIMMs in the following sizes:

DIMM Size	Non-ECC Configuration	ECC Configuration
8 MB	1 Mbit x 64	1 Mbit x 72
16 MB	2 Mbit x 64	2 Mbit x 72
32 MB	4 Mbit x 64	4 Mbit x 72
64 MB	8 Mbit x 64	8 Mbit x 72
128 MB	16 Mbit x 64	16 Mbit x 72

Memory can be installed in one, two, or three sockets. Memory size and speed can vary between sockets.

1.7.2 SDRAM

Synchronous DRAM (SDRAM) improves memory performance through memory access that is synchronous with the memory clock. This simplifies the timing design and increases memory speed because all timing is dependent on the number of memory clock cycles.

NOTE

To function properly, SDRAM DIMMs must meet the Intel 4-clock, 66 MHz, unbuffered SDRAM specification for either 64-bit or 72-bit SDRAM. See Section 6.2 for information about these specifications.

1.7.3 ECC Memory

Error checking and correcting (ECC) memory detects multiple-bit errors and corrects single-bit errors. When ECC memory is installed, the BIOS supports both ECC and non-ECC mode. ECC mode is enabled in the Setup program. The BIOS automatically detects if ECC memory is installed and provides the Setup option for selecting ECC mode. If any non-ECC memory is installed, the Setup option for ECC configuration does not appear and ECC operation is not available.

The following table describes the effect of using Setup to put each memory type in each supported mode. Whenever ECC mode is selected in Setup, some performance loss occurs.

	Memory Error Detection Mode Established in Setup Program	
	ECC Disabled	**ECC Enabled**
Non-ECC DIMM	No error detection	N/A
ECC DIMM	No error detection	Single-bit error correction, multiple-bit error detection

1.8 Chipset

The Intel 440LX chipset is the third generation of desktop PCIset and is designed for the Pentium II processor. It consists of the Intel 82443LX PCI/A.G.P. controller (PAC) and the Intel 82371AB PCI/ISA IDE Xccelerator (PIIX4) bridge chip.

1.8.1 Intel 82443LX PCI/A.G.P. Controller (PAC)

The PAC provides bus-control signals, address paths, and data paths for transfers between the processor's host bus, PCI bus, Accelerated Graphics Port (A.G.P.), and main memory. The PAC comes in a 492-pin BGA package and features:

- Processor interface control
  - — Processor host bus speed up to 66 MHz
  - — 32-bit addressing
  - — GTL+ compliant host bus
- Integrated DRAM controller
  - — Support for synchronous DRAM (SDRAM)
  - — 64/72-bit path-to-memory
  - — Auto detection of memory type
  - — Support for 4-, 16-, 64-Mbit DRAM devices
  - — Symmetrical and asymmetrical DRAM addressing
  - — Support for 3.3 V DRAMs
- Accelerated Graphics Port Interface
  - — Compliance with A.G.P. specification (see Section 6.2 for specification information)
  - — Support for 3.3 V A.G.P. devices with data transfer rates up to 133 MHz
  - — Synchronous coupling to the host-bus frequency
- Fully-synchronous PCI bus interface
  - — Compliance with PCI specification (see Section 6.2 for specification information)
  - — PCI-to-DRAM access greater than 100 MB/sec
  - — Support for five PCI bus masters in addition to the host and PCI-to-ISA I/O bridge
  - — Delayed transactions
  - — PCI parity checking and generation support
- Data Buffering
  - — Host-to-DRAM, PCI-to-DRAM, and A.G.P.-to-DRAM write-data buffering
  - — Write-combining for host-to-PCI burst writes
  - — Supports concurrent host, PCI, and A.G.P. transactions to main memory
- Support for system management mode (SMM)

1.8.2 Intel 82371AB PCI ISA IDE Xcelerator (PIIX4)

The PIIX4 is a multifunction PCI device implementing the PCI-to-ISA bridge, PCI IDE functionality, Universal Serial Bus (USB) host/hub function, and enhanced power management. The PIIX4 comes in a 324-pin MBGA package that features:

- Multifunction PCI-to-ISA bridge
  - Support for the PCI bus at 33 MHz
  - Compliance with PCI specification (see Section 6.2 for specification information)
  - Full ISA or extended I/O (EIO) bus support
- USB controller
  - Two USB ports (see Section 6.2 for compliance level)
  - Support for legacy keyboard and mouse
  - Support for UHCI design guide revision 1.1 interface
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers at up to 16 MB/sec
  - Support for Ultra DMA/33 synchronous DMA mode transfers up to 33 MB/sec
  - Bus master mode with an 8 x 32-bit buffer for bus master PCI IDE burst transfers
- Enhanced DMA controller
  - Two 8237-based DMA controllers
  - Support for PCI DMA with three PC/PCI channels and distributed DMA protocols
  - Fast type-F DMA for reduced PCI bus usage
- Interrupt controller based on 82C59
  - Support for 15 interrupts
  - Programmable for edge/level sensitivity
- Power management logic
  - Sleep/resume logic
  - Support for wake-on-modem through Ring Indicator input
- Real-Time Clock
  - 256 byte battery-backed CMOS SRAM
  - Includes date alarm
- 16-bit counters/timers based on 82C54

1.8.3 Accelerated Graphics Port (A.G.P.)

The Accelerated Graphics Port (A.G.P.) is a high-performance interconnect for graphic-intensive applications, such as 3D applications. A.G.P. is independent of the PCI bus and is intended for exclusive use with graphical-display devices. A.G.P. provides these performance features:

- Pipelined-memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for near 100 percent bus efficiency
- AC timing for 133 MHz data transfer rates, allowing data throughput of 500 MB/sec

A.G.P. complies with the 66 MHz PCI specification. See Section 6.2 for information about the A.G.P. and PCI specifications.

1.8.4 Universal Serial Bus (USB)

The motherboard has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The motherboard fully supports the universal host controller interface (UHCI) and uses UHCI-compatible software drivers. See Section 6.2 for information about the USB specification. USB features include:

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Supports isochronous and asynchronous transfer types over the same set of wires
- Supports up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed (sub-channel) USB device is attached to the cable. Use shielded cable that meets the requirements for high-speed (fully-rated) devices.

1.8.5 IDE Support

The motherboard has two independent bus-mastering PCI IDE interfaces. These interfaces support PIO Mode 3, PIO Mode 4, ATAPI devices (e.g., CD-ROM), and Ultra DMA/33 synchronous-DMA mode transfers. The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The BIOS automatically detects the IDE device transfer rate and translation mode.

Programmed I/O operations usually require a substantial amount of processor bandwidth. However, in multitasking operating systems, the bandwidth freed by bus mastering IDE can be devoted to other tasks while disk transfers are occurring.

1.8.6 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program.

An external coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3 V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 V applied.

1.9 Super I/O Controller

The PC97307 Super I/O Controller from National Semiconductor is an ISA Plug and Play compatible (see Section 6.2), multifunction I/O device that provides the following features:

- Serial ports
  - — Two 16450/16550A-software compatible UARTs
  - — Internal send/receive 16-byte FIFO buffer
  - — Four internal 8-bit DMA options for the UART with SIR support (USI)
- Multimode bidirectional parallel port
  - — Standard mode: IBM and Centronics compatible
  - — Enhanced parallel port (EPP) mode with BIOS and driver support
  - — High-speed extended capabilities port (ECP) mode
- Floppy disk controller
  - — DP8473 and N82077 compatible
  - — 16-byte FIFO
  - — PS/2† diagnostic-register support
  - — High-performance digital data separator (DDS)
  - — PC-AT† and PS/2 drive-mode support
- Keyboard and mouse controller
  - — Industry standard 8042A compatible
  - — General-purpose microcontroller
  - — 8-bit internal data bus
- Supports an IrDA and Consumer IR-compliant infrared interface

By default, the I/O controller interfaces are automatically configured during boot up. The I/O controller can also be manually configured in the Setup program.

1.9.1 Serial Ports

Two 9-pin D-Sub serial port connectors are located on the back panel and are compatible with 16450 and 16550A UARTs.

1.9.2 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel. In the Setup program, the parallel port can be configured for the following:

- Compatible (standard mode)
- Bidirectional (PS/2 compatible)
- Extended Parallel Port (EPP)
- Enhanced Capabilities Port (ECP)

1.9.3 Floppy Controller

The I/O controller is software compatible with the DP8473 and N82077 floppy drive controllers and supports both PC-AT and PS/2 modes. In the Setup program, the floppy interface can be configured for the following floppy drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.2 MB, 3.5-inch (driver required)
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

1.9.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The 5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an over-current condition is removed.

NOTE

The mouse and keyboard can be plugged into either of the PS/2 connectors. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI Megakey keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power on/reset. A power on/reset password can be specified in Setup.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del> for a software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power-On Self Test (POST).

1.9.5 Infrared Support

On the front panel I/O connector, there are six pins that support Hewlett Packard HSDL-1000 compatible infrared (IR) transmitters and receivers. In the Setup program, Serial Port 2 can be directed to a connected IR device. The connection can be used to transfer files to or from portable devices like laptops, PDAs, and printers. The Infrared Data Association (IrDA) specification supports data transfers of 115 Kbaud at a distance of 1 meter. See Section 6.2 for information about the IrDA specification.

1.9.5.1 Consumer Infrared Support

On the front panel I/O connector, there is one pin that supports consumer infrared devices (remote controls). This pin supports receive-only operations at data rates of up to 685.57 Kbaud.

Consumer infrared devices can be used to control telephony and multimedia operations, such as volume or CD track changes. A software and hardware interface is needed for a computer to support the consumer infrared feature.

1.10 Audio Subsystem

1.10.1 OPL3-SA3 Audio System

The optional onboard audio subsystem features the Yamaha OPL3-SA3 (YMF715) device. The features of the device include:

- A 16-bit audio codec
- OPL3 FM synthesis
- An integrated 3D enhanced stereo controller including all required analog components
- An interface for MPU-401 and a joystick
- Stereo analog-to-digital and digital-to-analog converters
- Analog mixing, anti-aliasing, and reconstruction filters
- Supports 16-bit address decoding
- Line, microphone, and monaural inputs
- ADPCM, A-law, or μlaw digital audio compression and decompression
- Full digital control of all mixer and volume control functions
- Software switching between rear panel Mic In and Line In connectors
- Plug and Play compatible
- Sound Blaster Pro† and Microsoft Windows Sound System compatible

1.10.2 OPL4-ML Wavetable Synthesizer

The optional onboard wavetable synthesizer features the single-chip OPL4-ML (YMF704). The OPL4-ML integrates the OPL3 audio system, general MIDI processor, and wavetable ROM into a single component. The features of the device include:

- Complies with general MIDI system 1
- Interface compatible with MPU-401 UART mode
- FM synthesis is compatible with the OPL3 audio system
- Wavetable synthesis that generates up to 24 voices simultaneously
- 100-pin SQFP package (YMF704-S)

1.10.3 Audio Subsystem Resources

The following table shows the IRQ, DMA channel, and base I/O address options for the audio subsystem. Options are listed in order of preference specified by Yamaha. These options are automatically chosen by the Plug and Play interface, so there are no default settings. Onboard audio can be enabled or disabled in the Setup program.

Table 1. Audio Subsystem Resources

Resource	IRQ (Options)	DMA channel (Options)	I/O Address (Options)
Sound Blaster† (DMA playback, DMA shared with Windows Sound System capture)	10 7 5,7, 10,11	1 0,1,3	220-22Fh 240-24Fh 16 bytes on 16-byte boundary in the range of 220-280h
Windows Sound System (DMA playback)	5 11 5,7, 10,11	0 0,1,3	530-537h E80-E87h 8 bytes on 8-byte boundary in the range of 530-F48h
MPU-401 (IRQ shared with Sound Blaster)			330-331h 300-301h 2 bytes on 2-byte boundary in the range of 300-334h
MIDI / Game Port			201h 1 byte on 1-byte boundary in the range of 201-20Fh
AdLib†			388-38Dh 6 bytes on 8-byte boundary in the range of 388-3F8h

1.10.4 Audio Drivers and Utilities

Audio software and utilities are available from Intel's World Wide Web site (see Section 6.1). Audio driver support is provided for the Microsoft Windows† 3.1, Microsoft Windows 95, Microsoft Windows NT† (versions 3.51 and 4.0), and IBM OS/2† Warp† (versions 3.0 and 4.0) operating systems.

1.10.5 Audio Connectors

The audio connectors are optional and include the following connectors:

- Back panel connectors: Line In, Line Out, Mic In (see Section 1.14.4)
- CD-ROM audio
- Telephony
- Line In
- Hardware wavetable

See Section 1.14 for the location and pinouts of the audio connectors.

1.10.5.1 CD-ROM Audio Connector

An optional 1 x 4-pin ATAPI-style connector (J1F1) is available for connecting an internal CD-ROM drive to the audio mixer. The connector is designed for audio add-in cards and is compatible with most cables supplied with ATAPI CD-ROM drives.

1.10.5.2 Telephony Connector

An optional 1 x 4-pin ATAPI-style connector (J2F1) is available for connecting the monaural audio signals of an internal telephony device to the audio subsystem. A monaural audio-in and audio-out signal interface is necessary for telephony applications such as speakerphones, fax/modem, and answering machines.

1.10.5.3 Line In Connector

An optional 1 x 4-pin ATAPI-style Line In connector (J2F2) is available for connecting the left and right channel signals of an internal audio device to the audio subsystem. An audio-in signal interface of this type is necessary for applications such as TV tuners.

1.10.5.4 Hardware Wavetable Headers

Two optional 2 x 3-pin headers (J6B1, J6C1) are available for a wavetable add-in module. An optional OPL4-ML reference design module that can be plugged into the motherboard may be licensed from Yamaha Corporation. Compatible wavetable module cards are available from several vendors.

1.11 Management Extension Hardware

The optional management extension hardware provides low-cost instrumentation capabilities on a single-chip ASIC. The features include:

- Integrated temperature sensor
- Fan speed sensors
- Power supply voltage monitoring to detect levels above or below acceptable values
- Remote reset capabilities from a remote peer or server through LANDesk® Client Manager, Version 3.0 and service layers (when available)
- Header for an external chassis-security feature

See Section 6.2 for information about the management extension hardware specification.

The following picture shows a block diagram of the management extension hardware.

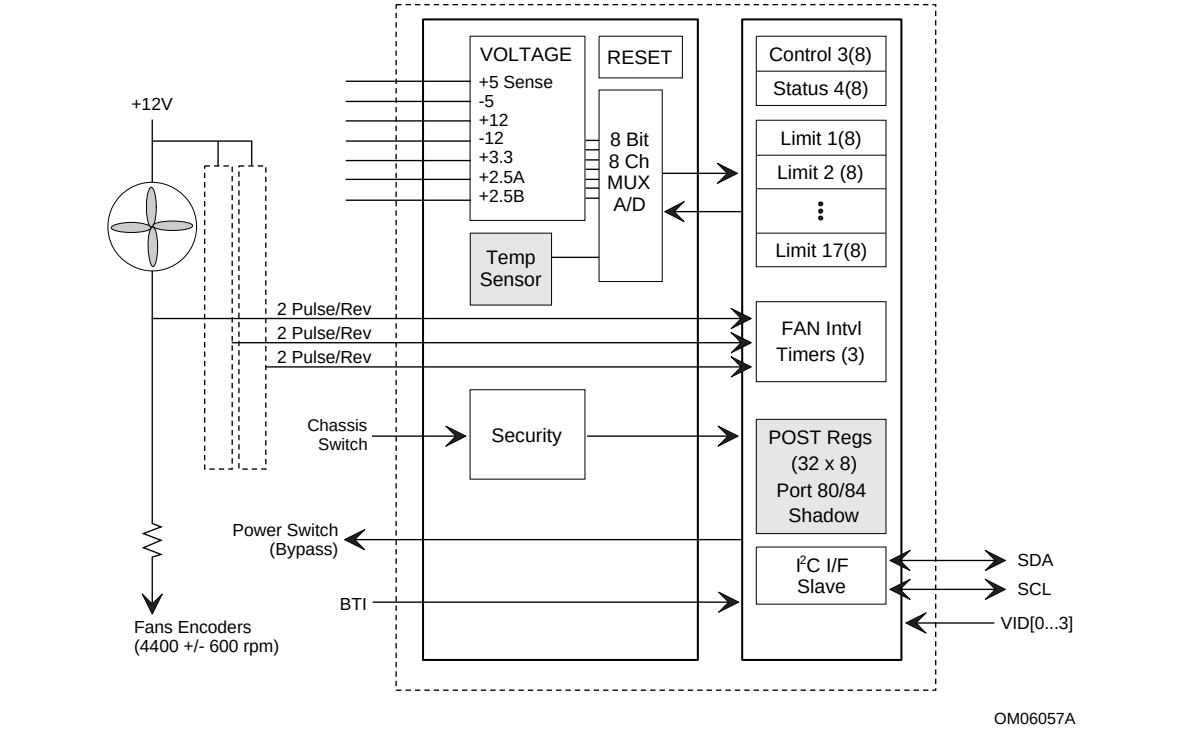

Figure 5. Block Diagram of Management Extension ASIC

1.11.1 Chassis Security Header

The management extension hardware supports an optional chassis security feature that detects if the chassis is opened while the computer is powered on. The security feature uses a mechanical switch on the chassis that is attached to an optional 1 x 2-pin header (J2B1). The mechanical switch is closed for normal computer operation. See Section 1.14 for the location and pinouts of the chassis security header.

1.12 Wake on LAN Header

The optional Wake on LAN header (J1C1) is a 1 x 3-pin header for remote wakeup of the computer through a network. Wake on LAN requires a PCI add-in network interface card (NIC) with remote wakeup capabilities. The remote wakeup header on the NIC must be connected to the onboard Wake on LAN header. The NIC monitors network traffic at the MII interface and when it detects a Magic Packet† it asserts a wakeup signal that powers up the computer. See Section 1.14 for the location and pinouts of the Wake on LAN header.

NOTE

For Wake on LAN, the 5-V standby line for the power supply must be capable of delivering +5 V ± 5 % at 720 mA.

1.13 Wake on Ring Header

The Wake on Ring header (J8A1) is a 1 x 2-pin header that allows the computer to wake from sleep mode when a call is received on a telephony device, such as a modem, configured for operation on COM1. The first incoming call powers up the computer. A second call must be made to access the computer. See Section 1.14 for the location and pinouts of the Wake on Ring header.

1.14 Motherboard Connectors

The following figure shows the location of the motherboard connectors.

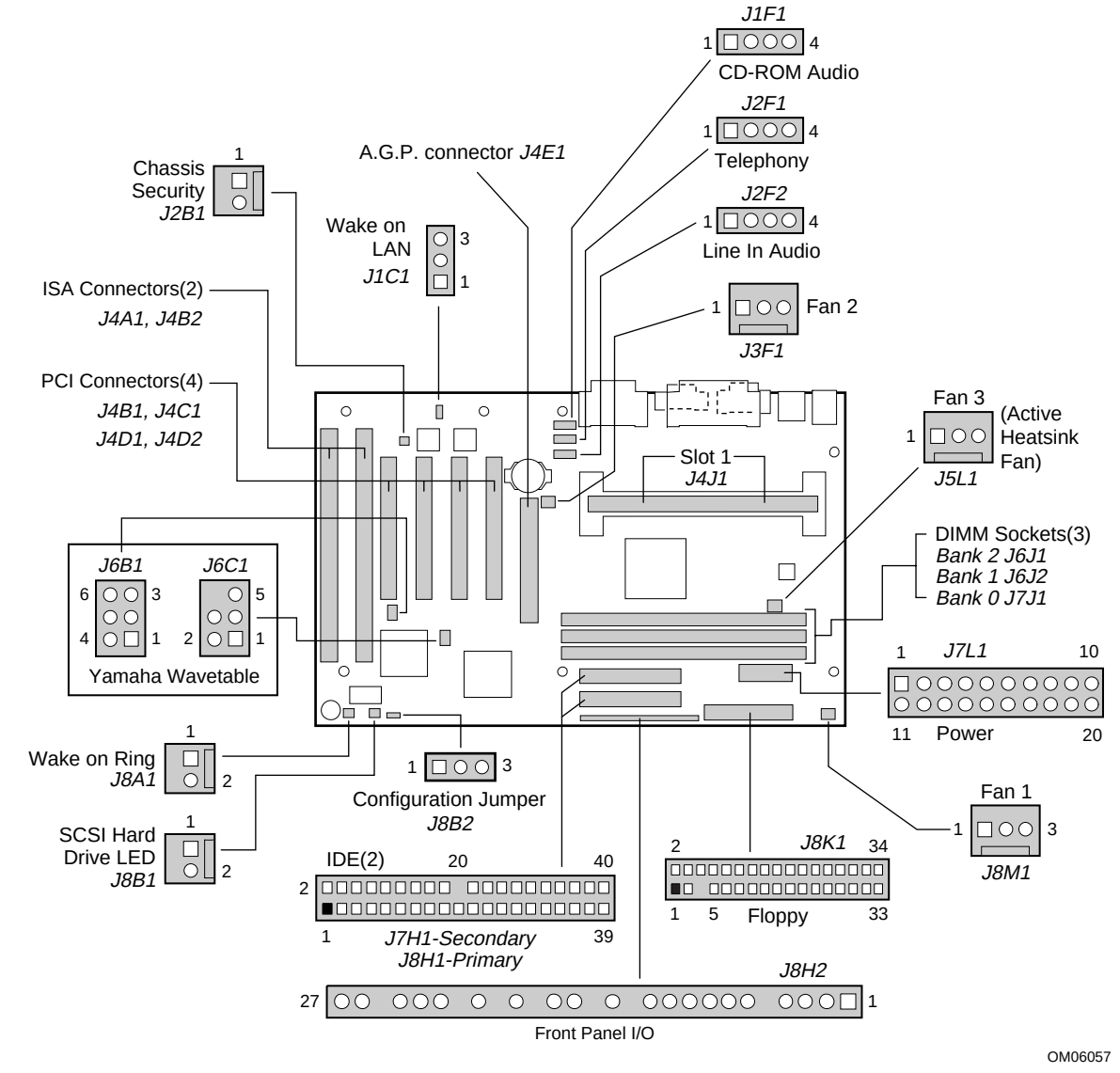

Figure 6. Motherboard Connectors

Table 2. Chassis Security Header (J2B1)

Pin	Signal Name
1	Ground
2	CHS_SEC

Table 3. Wake on LAN Header (J1C1)

Pin	Signal Name
1	+5 VSB
2	Ground
3	WOL

Table 4. ATAPI CD Audio Connector (J1F1)

Pin	Signal Name
1	CD_IN-Left
2	Ground
3	Ground
4	CD_IN-Right

Table 5. ATAPI-Style Telephony Connector (J2F1)

Pin	Signal Name
1	Audio Out (monaural)
2	Ground
3	Ground
4	Audio In (monaural)

Table 6. ATAPI-Style Line In Connector (J2F2)

Pin	Signal Name
1	Left Line In
2	Ground
3	Ground
4	Right Line In (monaural)

Table 7. Fan 1 Header (J8M1)

Pin	Signal Name
1	Ground
2	FAN_CTRL (+12 V)
3	FAN_SEN*

* If the optional management extension hardware is not available, pin 3 is ground.

Table 8. Fan 2 Header (J3F1)

Pin	Signal Name
1	Ground
2	FAN_CTRL (+12 V)
3	FAN_SEN*

* If the optional management extension hardware is not available, pin 3 is ground.

Table 9. Fan 3 Header (J5L1) (Active Heatsink Fan)

Pin	Signal Name
1	Ground
2	+12 V
3	ground

Table 10. SCSI Hard Drive LED Input Header (J8B1)

Pin	Signal Name
1	DRV_ACT#
2	No connect

Table 11. Wake on Ring Header (J8A1)

Pin	Signal Name
1	Ground
2	RINGA

Table 12. Yamaha Wavetable Module Headers (J6B1 and J6C1)

Connector (J6B1)		Connector (J6C1)	
Pin	**Signal Name**	**Pin**	**Signal Name**
1	SYNCS#	1	RSTSLOT
2	SIN	2	Vcc
3	Vcc	3	AUD33MHZ
4	Ground	4	MIDI Out
5	BCK	5	Ground
6	LACK	6	Key

Note: There are two 2 x 3 headers in a standard position that connect to the Yamaha wavetable module.

Table 13. Floppy Drive Connector (J8K1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	FDDS1# (Drive Select B)
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	FDM01# (Motor Enable B)
17	MSEN1	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	MSEN0	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

Table 14. PCI IDE Connectors (J7H1, J8H1)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable Select pullup)
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	Address 1	34	Reserved
35	Address 0	36	Address 2
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

NOTE: Signal names in brackets ([ ]) are for the secondary IDE connector.

Table 15. Accelerated Graphics Port (J4E1)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+12V	B1	No Connect	A34	Vcc3.3	B34	Vcc3.3
A2	No Connect	B2	Vcc	A35	AD22	B35	AD21
A3	Reserved	B3	Vcc	A36	AD20	B36	AD19
A4	No Connect	B4	No Connect	A37	Ground	B37	Ground
A5	Ground	B5	Ground	A38	AD18	B38	AD17
A6	INTA#	B6	INTB#	A39	AD16	B39	C/BE2#
A7	RST#	B7	CLK	A40	Vcc3.3	B40	Vcc3.3
A8	GNT1#	B8	REQ#	A41	FRAME#	B41	IRDY#
A9	Vcc3.3	B9	Vcc3.3	A42	Reserved	B42	Reserved
A10	ST1	B10	ST0	A43	Ground	B43	Ground
A11	Reserved	B11	ST2	A44	Reserved	B44	Reserved
A12	PIPE#	B12	RBF#	A45	Vcc3.3	B45	Vcc3.3
A13	Ground	B13	Ground	A46	TRDY#	B46	DEVSEL#
A14	No Connect	B14	No Connect	A47	STOP#	B47	Vcc3.3
A15	SBA1	B15	SBA0	A48	No Connect	B48	PERR#
A16	Vcc3.3	B16	Vcc3.3	A49	Ground	B49	Ground
A17	SBA3	B17	SBA2	A50	PAR	B50	SERR#
A18	Reserved	B18	SB_STB	A51	AD15	B51	C/BE1#
A19	Ground	B19	Ground	A52	Vcc3.3	B52	Vcc3.3
A20	SBA5	B20	SBA4	A53	AD13	B53	AD14
A21	SBA7	B21	SBA6	A54	AD11	B54	AD12
A22	Key	B22	Key	A55	Ground	B55	Ground
A23	Key	B23	Key	A56	AD9	B56	AD10
A24	Key	B24	Key	A57	C/BE0#	B57	AD8
A25	Key	B25	Key	A58	Vcc3.3	B58	Vcc3.3
A26	AD30	B26	AD31	A59	Reserved	B59	AD_STB0
A27	AD28	B27	AD29	A60	AD6	B60	AD7
A28	Vcc3.3	B28	Vcc3.3	A61	Ground	B61	Ground
A29	AD26	B29	AD27	A62	AD4	B62	AD5
A30	AD24	B30	AD25	A63	AD2	B63	AD3
A31	Ground	B31	Ground	A64	Vcc3.3	B64	Vcc3.3
A32	Reserved	B32	AD_STB1	A65	AD0	B65	AD1
A33	C/BE3#	B33	AD23	A66	SMB0	B66	SMB1

1.14.1 Power Supply Connector

When used with an ATX-compliant power supply that supports remote power on/off, the motherboard can turn off the system power through software control. See Section 6.2 for information about the ATX specification.

To enable soft-off control in software, advanced power management must be enabled in the Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

Table 16. Power Supply Connector (J7L1)

Pin	Signal Name
1	+3.3 V
2	+3.3 V
3	Ground
4	+5 V
5	Ground
6	+5 V
7	Ground
8	PWRGD (Power Good)
9	+5 VSB
10	+12 V
11	+3.3 V
12	-12 V
13	Ground
14	PS-ON# (power supply remote on/off control)
15	Ground
16	Ground
17	Ground
18	-5 V
19	+5 V
20	+5 V

1.14.2 Front Panel Connectors

The front panel connector includes headers for these I/O connections:

- Speaker
- Reset switch
- Power LED
- Hard drive activity LED
- Infrared (IrDA) port
- Sleep switch
- Power switch

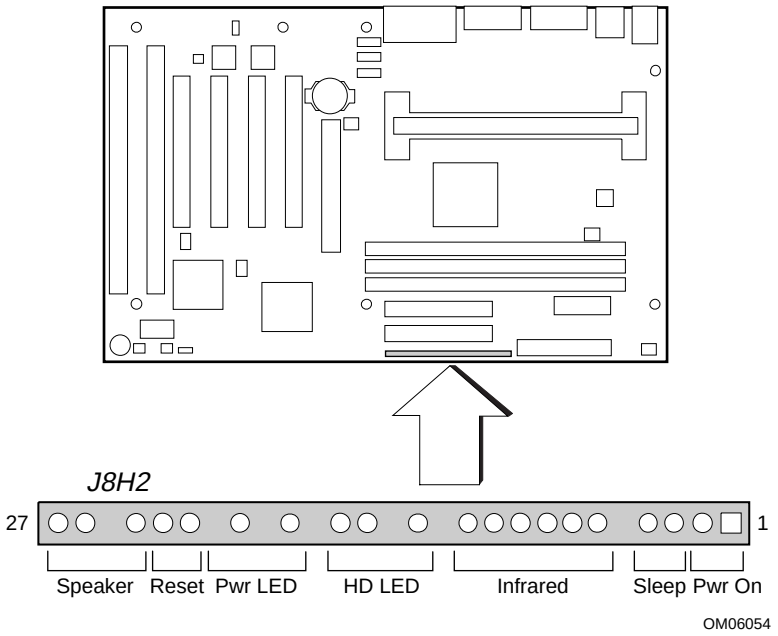

Figure 7. Front Panel I/O Connectors

Table 17. Front Panel I/O Connectors

Connector	Pin	Signal Name	Connector	Pin	Signal Name
A. Speaker	27	SPKR_HDR	none	12	No connect
	26	PIEZO_IN	E. IrDA	11	CONIR (Consumer IR)
	25	Key		10	IrTX
	24	Ground		9	Ground
B. Reset	23	SW_RST		8	IrRX
	22	Ground		7	Key
none	21	No connect/Key		6	+5 V
C. Sleep/Power LED	20	PWR_LED	none	5	No connect
	19	Key	F. Sleep/Resume	4	SLEEP_PU (pullup)
	18	Ground		3	SLEEP
none	17	No connect/Key	G. Power On	2	Ground
D. Hard Drive LED	16	HD_PWR		1	SW_ON#
	15	HD Active#			
	14	Key			
	13	HD_PWR +5 V			

1.14.2.1 Speaker

A speaker can be installed on the motherboard as a manufacturing option. The speaker is enabled by a jumper on pins 26-27 of the front panel connector. The onboard speaker can be disabled by removing the jumper, and an offboard speaker can be connected in its place. The speaker (onboard or offboard) provides error beep code information during the POST in the event that the computer cannot use the video interface. The speaker is not connected to the audio subsystem and does not receive output from the audio subsystem.

1.14.2.2 Reset

This header can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the motherboard resets and runs the POST.

1.14.2.3 Power LED/Sleep/Message Waiting

This header can be connected to an LED that will light when the computer is powered on. Table 18 shows the possible states for this LED.

Table 18. Power LED (J7L1)

LED State	Description
Off	Power off
Green	Power on
Yellow	Sleep
Blink	Message waiting

1.14.2.4 Hard Drive LED

This header can be connected to an LED to provide a visual indicator that data is being read from or written to an IDE hard drive. For the LED to function properly, the IDE drive must be connected to the onboard IDE controller. This LED will also show activity for devices connected to the SCSI hard drive LED header. See Section 1.14.3 for information about the SCSI hard drive LED header.

1.14.2.5 Infrared Connector

Serial Port 2 can be configured to support an IrDA module connected to this 6-pin header. After the IrDA interface is configured, files can be transferred to or from portable devices such as laptops, PDAs and printers using application software.

1.14.2.6 Sleep/Resume Switch

When APM is enabled in the system BIOS, and the operating system's APM driver is loaded, the system can enter sleep (standby) mode in one of the following ways:

- Optional front panel sleep/resume button
- Prolonged system inactivity using the BIOS inactivity timer feature (see Section 4.5)

The 2-pin header located on the front panel I/O connector supports a front panel sleep/resume switch, which must be a momentary SPST type that is normally open.

Closing the sleep/resume switch sends a System Management Interrupt (SMI) to the processor, which immediately goes into System Management Mode (SMM). While the system is in sleep mode it is fully capable of responding to and servicing external interrupts (such as an incoming fax) even though the monitor turns on only if a keyboard or mouse interrupt occurs. To reactivate or resume the system, the sleep/resume switch must be pressed again, or the keyboard or mouse must be used.

1.14.2.7 Power On Connector

This header can be connected to a front panel power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the motherboard.) At least two seconds must pass before the power supply will recognize another on/off signal.

1.14.3 SCSI Hard Drive LED Header

The SCSI hard drive LED header is a 1 x 2-pin header (J8B1) that allows add-in SCSI controller applications to use the same LED as the onboard front-panel LED. This header can be connected to the LED output of the add-in controller card. The LED will indicate when data is being read or written using the add-in controller. See Section 1.14.2.4 for information about the onboard IDE hard drive LED header. See page 28 for the SCSI hard drive LED header pinouts.

1.14.4 Back Panel Connectors

Figure 8 shows the location of the back panel I/O connectors, which include:

- PS/2-style keyboard and mouse connectors
- Two USB connectors
- External audio jacks: Line Out, Line In, and Mic In (optional)
- Two serial ports
- One parallel port
- MIDI/game port (optional)

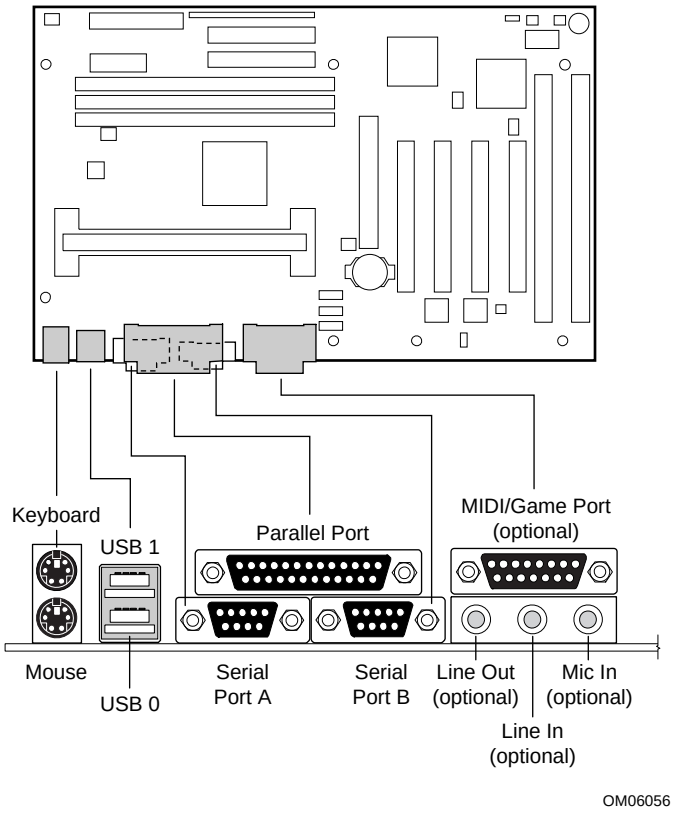

Figure 8. Back Panel I/O Connectors

Table 19. PS/2 Keyboard/Mouse Connectors

Pin	Signal Name
1	Data
2	No connect
3	Ground
4	+5 V (fused)
5	Clock
6	No connect

Table 20. USB Connectors

Pin	Signal Name
1	Power
2	USBP0# [USBP1#]
3	USBP0 [USBP1]
4	Ground

Table 21. Serial Port Connectors

Pin	Signal Name
1	DCD
2	Serial In #
3	Serial Out #
4	DTR#
5	Ground
6	DSR
7	RTS
8	CTS
9	RI

Table 22. Audio Line Out Connector

Pin	Signal Name
Sleeve	Ground
Tip	Audio Left Out
Ring	Audio Right Out

Table 23. Audio Line In Connector

Pin	Signal Name
Sleeve	Ground
Tip	Audio Left In
Ring	Audio Right In

Table 24. Audio Mic In Connector

Pin	Signal Name
Sleeve	Ground
Tip	Mono In
Ring	Electret Bias Voltage

Table 25. Parallel Port Connector

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data bit 0	15	Fault#
3	Data bit 1	16	INIT#
4	Data bit 2	17	SLCT IN#
5	Data bit 3	18	Ground
6	Data bit 4	19	Ground
7	Data bit 5	20	Ground
8	Data bit 6	21	Ground
9	Data bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Error	25	Ground
13	Select		

Table 26. MIDI / Game Port Connector

Pin	Signal Name	Pin	Signal Name
1	+5 V (fused)	9	+5 V (fused)
2	GP4 (JSBUTO)	10	GP6 (JSBUT2)
3	GP0 (JSX1R)	11	GP2 (JSX2R)
4	Ground	12	MIDI-OUTR
5	Ground	13	GP3 (JSY2R)
6	GP1 (JSY1R)	14	GP7 (JSBUT3)
7	GP5 (JSBUT1)	15	MIDI-INR
8	+5 V (fused)		

1.14.5 Add-in Board Expansion Connectors

There are three PCI slots, one ISA slot, and one shared slot (for a PCI or ISA card). The PCI bus supports up to four bus masters through the four PCI connectors (see Section 6.2 for information about compliance with the PCI specification).

Table 27. PCI Bus Connectors

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#)*	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK)*	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	no connect (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	no connect (PRSNT1#)*	A40	+5 V (SDONE)*	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	+5 V (SBO#)*	B41	+3.3 V
A11	Reserved	B11	no connect (PRSNT2#)*	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	Reserved	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

* These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

Table 28. ISA Bus Connectors

Pin	Signal Name	Pin	Signal Name
B1	Ground	A1	IOCHK# (IOCHCK#)
B2	RESET (RESDRV)	A2	SD7
B3	+5 V	A3	SD6
B4	IRQ9	A4	SD5
B5	-5 V	A5	SD4
B6	DRQ2	A6	SD3
B7	-12 V	A7	SD2
B8	SRDY# (NOWS#)	A8	SD1
B9	+12 V	A9	SD0
B10	Ground	A10	IOCHRDY (CHRDY)
B11	SMEMW# (SMWTC#)	A11	AEN
B12	SMEMR# (SMRDC#)	A12	SA19
B13	IOW# (IOWC#)	A13	SA18
B14	IOR# (IORC#)	A14	SA17
B15	DACK3#	A15	SA16
B16	DRQ3	A16	SA15
B17	DACK1#	A17	SA14
B18	DRQ1	A18	SA13
B19	REFRESH#	A19	SA12
B20	BCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DACK2#	A26	SA5
B27	TC	A27	SA4
B28	BALE	A28	SA3
B29	+5 V	A29	SA2
B30	OSC	A30	SA1
B31	Ground	A31	SA0
Key		Key	
D1	MEMCS16# (M16#)	C1	SBHE#
D2	IOCS16# (IO16#)	C2	LA23
D3	IRQ10	C3	LA22

Note: Items in parentheses are alternate versions of signal names.

continued ☛

Table 28. ISA Bus Connectors (continued)

Pin	Signal Name	Pin	Signal Name
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0#	C8	LA17
D9	DRQ0	C9	MEMR# (MRDC#)
D10	DACK5#	C10	MEMW# (MWTC#)
D11	DRQ5	C11	SD8
D12	DACK6#	C12	SD9
D13	DRQ6	C13	SD10
D14	DACK7#	C14	SD11
D15	DRQ7	C15	SD12
D16	+5 V	C16	SD13
D17	Master16# (MASTER#)	C17	SD14
D18	Ground	C18	SD15

Note: Items in parentheses are alternate versions of signal names.

1.15 Jumper Settings

The configuration header (J8B2) requires a single jumper to set the configuration mode for the Setup program. This allows all motherboard configuration to be done in Setup. The following figure shows the location of the configuration header on the motherboard.

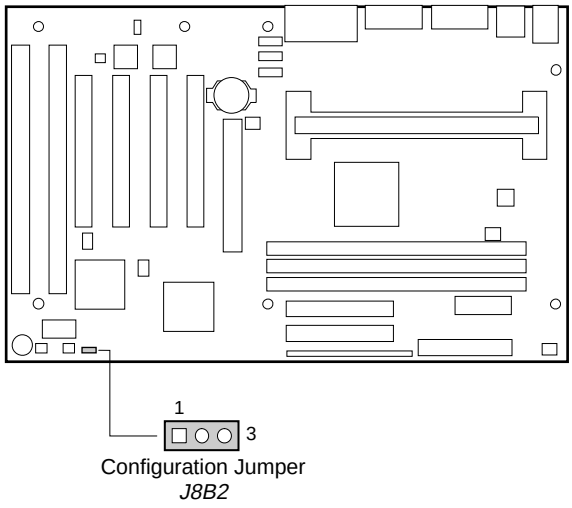

Figure 9. Single-Jumper Configuration

Table 29. Configuration Jumper Settings

Function	Jumper J8B2	Configuration
Normal	1-2	The BIOS uses current configuration information and passwords for booting.
Configure	2-3	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	none	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing the jumper.

NOTE

There is no jumper setting for configuring the processor speed or bus frequency. The feature for configuring the processor speed is in the Setup program using configure mode. See Section 1.15.2 for information about configure mode.

1.15.1 Normal Mode

This mode is for normal computer booting and operations. Connect pins 1 and 2 with a jumper on the configuration header (J8B2) to enable the mode. The BIOS uses the current bus/processor frequency ratio, configuration information, and passwords to boot the computer. Access to the Setup program can be restricted using an administrative or user password.

In normal mode, the BIOS attempts an automatic recovery if the configuration information in flash memory is corrupted.

1.15.2 Configure Mode

This mode is for configuring the processor speed and clearing passwords. Connect pins 2 and 3 with a jumper on the configuration header (J8B2) to enable the mode. In this mode, Setup automatically executes after the POST runs, and no password is required. Setup provides the Maintenance menu with options for setting the processor speed and clearing passwords. All other Setup screens are available. Configure mode uses the default BIOS settings for booting, not the current user or administrative settings. The default settings include the lowest bus/processor frequency ratio the processor supports. When the computer is rebooted, Setup uses the original user and administrative settings with the exception of the options that were changed.

For the configuration changes to take effect after exiting the Setup program, power down the computer, set the configuration jumper to normal mode (see Section 1.15.1), and boot the computer.

In configure mode, the BIOS attempts an automatic recovery if the configuration information flash memory is corrupted.

1.15.3 Recovery Mode

This mode is for upgrading the BIOS or recovering BIOS data. Remove the jumper (no pins connected) from the configuration header (J8B2) to enable this mode. After the computer is powered-on, the BIOS attempts to upgrade or recover the BIOS data from a diskette in the floppy drive. Beep codes indicate the recovery status: one beep indicates the start of the recovery, two beeps indicate a successful recovery, and multiple beeps indicate a failed recovery. If a diskette is not in the boot drive, the BIOS attempts to run the POST, does not boot the operating system, and displays a message that the jumper is not properly installed.

For the changes to take effect after a successful recovery, power down the computer, set the jumper to normal mode (see Section 1.15.1), and boot the computer.

1.16 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991.

The MTBF prediction is for:

- Redesigning the motherboard for alternate components if failure rates exceed reliability expectations
- Estimating repair rates and spare parts requirements

MTBF data is calculated from predicted data @ 55 °C.

The MTBF prediction for the motherboard is 176,587 hours.

1.17 Environmental Specifications

Table 30. Environmental Specifications

Parameter	Specification		
Temperature			
Nonoperating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 G trapezoidal waveform		
	Velocity change of 170 inches/sec		
Packaged	Half sine 2 millisecond		
	Product Weight	**Free Fall (inches)**	**Velocity Change (inches/sec)**
	<20 lbs	36	167
	21-40 lbs	30	152
	41-80 lbs	24	136
	81-100 lbs	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz : 0.01g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz : 0.02g² Hz (flat)		
Packaged	10 Hz to 40 Hz : 0.015g² Hz (flat)		
	40 Hz to 500 Hz : 0.015g² Hz sloping down to 0.00015 g² Hz		

1.18 Power Consumption

Table 31 lists the power specifications for a computer that contains a motherboard with a 266 MHz Pentium II processor, 32 MB RAM, 256 KB cache, 3.5-inch floppy drive, 1.6 GB IDE hard drive, 4X IDE CD-ROM, and PCI graphics card. This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 95 desktop mode are measured at 1024 x 768 x 256 colors and 70 Hz refresh rate. AC watts are measured with a typical 200W supply, nominal input voltage and frequency, with true RMS wattmeter at the line input.

Table 31. Power Usage

Mode	AC (watts) Out of 110 VAC Wall Outlet
DOS prompt, APM disabled	58.7 W
Windows 95 desktop, APM disabled	60.0 W
Windows 95 desktop, APM enabled, in SMM	28.0 W

1.18.1 Power Supply Considerations

For typical configurations, the motherboard is designed to operate with at least a 200 W power supply (see Section 6.2 for the specification). A higher-wattage power supply should be used for heavily-loaded configurations. The power supply must meet the following requirements:

- Rise time for power supply: 2 ms to 20 ms
- Minimum delay for reset to Power Good: 100 ms
- Minimum Powerdown warning: 1 ms
- 3.3 V output must reach its minimum regulation level within ± 20 ms of the +5 V output reaching its minimum regulation level

The following table lists the power supply's tolerances for DC voltages:

Table 32. DC Voltage

DC Voltage	Acceptable Tolerance
+3.3 V	± 5%
+5 V	± 5%
+5 VSB (standby)	± 5%
-5 V	± 5%
+12 V	± 5%
-12 V	± 5%

1.19 Thermal Considerations

The following table provides maximum component case temperatures for motherboard components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the motherboard.

CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5 °C to 10 °C might cause components to exceed their maximum case temperature. For information about the maximum operating temperature, see the environmental specifications in Section 1.17.

Table 33. Thermal Considerations for Components

Component	Maximum Case Temperature		Motherboard Location
Pentium II processor	233 MHz	75 °C (thermal plate)	J4J1 (Slot 1 connector)
	266 MHz	75 °C (thermal plate)	
	300 MHz	70 °C (thermal plate)	
Intel 82443LX (PAC)	85 °C (case)		U5H1
Intel 82371AB (PIIX4)	85 °C (case)		U7D1

The following figure shows motherboard components that may be sensitive to thermal changes.

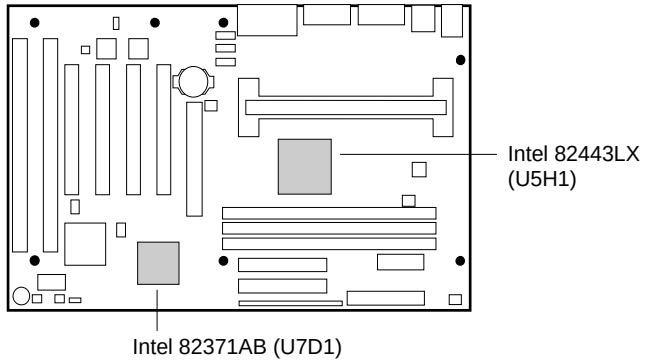

Figure 10. Thermally-Sensitive Components

1.20 Regulatory Compliance

The board's printed circuit assembly complies with the following safety and Electromagnetic Compatibility (EMC) regulations when correctly installed in a compatible host system.

1.20.1 Safety

This printed circuit assembly complies with the following safety and EMC regulations when correctly installed in a compatible host system. Certification reports for this printed circuit assembly are maintained under File E139761, Vol. 11, Sec. 2.

1.20.1.1 UL 1950 - CSA 950-95, 3rd edition, Dated 7-28-95

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment (USA & Canada).

1.20.1.2 CSA C22.2 No. 950-95, 3rd Edition

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment (Canada).

1.20.1.3 UL Classified to IEC 950

See section 1.20.1.4.

1.20.1.4 IEC 950, 2nd edition

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment (International).

1.20.2 EMC

This printed circuit assembly complies with the following EMC regulations when correctly installed in a compatible host system.

1.20.2.1 EN 55 022, Class B

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment (Europe).

1.20.2.2 EN 50 082-1

Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4 (Europe).

1.20.3 Product Certification Markings

This printed circuit assembly has the following product certification markings:

- European CE Marking: Consists of a marking on the motherboard and shipping container.
- UL Recognition Mark: UL Safety certification is identified with the UL File No. E139761 on the component side of the motherboard and the PB number on the solder side of the motherboard. Motherboard material flammability is compliant with the 94V-1 or 94V-0 standard.
- Canadian Compliance: Consists of small c followed by a stylized backward UR on component side of motherboard.

2 Motherboard Resources

NOTE

For more detailed information about the resources used for onboard audio, see the Audio Subsystem section in Chapter 1.

2.1 Memory Map

Table 34. Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 393216 K	100000 - 18000000	383 MB	Extended memory
1008 K - 1024 K	FC000 - FFFFF	16 KB	Boot block
1000 K - 1008 K	FA000 - FBFFF	8 KB	ESCD (Plug and Play configuration and DMI)
996 K - 1000 K	F9000 - F9FFF	4 KB	Reserved for BIOS
992 K - 996 K	F8000 - F8FFF	4 KB	OEM Logo or Scan User Flash
928 K - 992 K	E8000 - F7FFF	64 KB	POST BIOS
896 K - 928 K	E0000 - E7FFF	32 KB	POST BIOS (Available as UMB)
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to ISA and PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.2 DMA Channels

Table 35. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Audio
1	8- or 16-bits	Audio / parallel port
2	8- or 16-bits	Floppy drive
3	8- or 16-bits	Parallel port (for ECP)/audio
4		Reserved - cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.3 I/O Map

Table 36. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX4- DMA 1
0020 - 0021	2 bytes	PIIX4 - interrupt controller 1
002E - 002F	2 bytes	Super I/O controller configuration registers
0040 - 0043	4 bytes	PIIX4 - Counter/Timer 1
0048 - 004B	4 bytes	PIIX4- Counter/Timer 2
0060	1 byte	Keyboard Controller Byte - Reset IRQ
0061	1 byte	PIIX4 - NMI, Speaker Control
0064	1 byte	Keyboard controller, CMD/STAT Byte
0070, bit 7	1 bit	PIIX4 - enable NMI
0070, bits 6:0	7 bits	PIIX4 - real time clock, address
0071	1 byte	PIIX4 - real time clock, data
0078	1 byte	Reserved - motherboard configuration
0079	1 byte	Reserved - motherboard configuration
0080 - 008F	16 bytes	PIIX4 - DMA page registers
00A0 - 00A1	2 bytes	PIIX4 - interrupt controller 2
00B2 - 00B3	2 bytes	APM control
00C0 - 00DE	31 bytes	PIIX4 - DMA 2
00F0	1 byte	Reset numeric error
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
0201	1 byte	Audio / game port
0220 - 022F	16 bytes	Audio (Sound Blaster compatible)
0228 - 022F	8 bytes	LPT3
0240 - 024F	16 bytes	Audio (Sound Blaster compatible)
0278 - 027F	8 bytes	LPT2
0290 - 0297	8 bytes	Management extension hardware
02E8 - 02EF	8 bytes	COM4/Video (8514A)
02F8 - 02FF	8 bytes	COM2
0300 - 0301	2 bytes	MPU-401 (MIDI)
0330 - 0331	2 bytes	MPU-401 (MIDI)
0332 - 0333	2 bytes	MPU-401 (MIDI)
0334 - 0335	2 bytes	MPU-401 (MIDI)
0376	1 byte	Secondary IDE channel command port
0377	1 byte	Floppy channel 2 command
0377, bit 7	1 bit	Floppy disk change, channel 2
0377, bits 6:0	7 bits	Secondary IDE channel status port

continued ☛

Table 36. I/O Map (continued)

Address (hex)	Size	Description
0378 - 037F	8 bytes	LPT1
0388- 038D	6 bytes	AdLib (FM synthesizer)
03B4 - 03B5	2 bytes	Video (VGA†)
03BA	1 byte	Video (VGA)
03C0 - 03CA	11 bytes	Video (VGA)
03CC	1 byte	Video (VGA)
03CE - 03CF	2 bytes	Video (VGA)
03D4 - 03D5	2 bytes	Video (VGA)
03DA	1 byte	Video (VGA)
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Floppy Channel 1
03F6	1 byte	Primary IDE channel command port
03F7 (Write)	1 byte	Floppy channel 1 command
03F7, bit 7	1 bit	Floppy disk change channel 1
03F7, bits 6:0	7 bits	Primary IDE channel status port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0530 - 0537	8 bytes	Windows Sound System
0604 - 060B	8 bytes	Windows Sound System
LPT*n* + 400h	8 bytes	ECP port, LPT*n* base address + 400h
0CF8 - 0CFB*	4 bytes	PCI configuration address register
0CF9**	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
0E80 - 0E87	8 bytes	Windows Sound System
0F40- 0F47	8 bytes	Windows Sound System
0F86 - 0F87	2 bytes	Yamaha OPL3-SA configuration
FF00 - FF07	8 bytes	IDE bus master register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers

* DWORD access only

** Byte access only

NOTE

See Section 1.10.3 for the I/O addresses that can be used by the audio components on the motherboard. This table does not list I/O addresses that may be used by add-in cards in the system.

2.4 PCI Configuration Space Map

Table 37. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel 82440LX (PAC)
00	01	00	Intel 82440LX (PAC) A.G.P. bus
00	07	00	Intel 82371AB (PIIX4) PCI/ISA bridge
00	07	01	Intel 82371AB (PIIX4) IDE bus master
00	07	02	Intel 82371AB (PIIX4) USB
00	07	03	Intel 82371AB (PIIX4) power management
00	0D	00	PCI expansion slot 1 (J4D2)
00	0E	00	PCI expansion slot 2 (J4D1)
00	0F	00	PCI expansion slot 3 (J4C1)
00	10	00	PCI expansion slot 4 (J4B1)

2.5 Interrupts

Table 38. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2*
4	COM1*
5	LPT2 (Plug and Play option) / audio / user available
6	Floppy drive
7	LPT1*
8	Real time clock
9	Reserved
10	User available
11	Windows Sound System* / user available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ

2.6 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI expansion slots and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX4 PCI-to-ISA bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and therefore share the same interrupt. Table 39 lists the PIRQ signals and shows how the signals are connected to the onboard PCI interrupt sources.

Table 39. PCI Interrupt Routing Map

PIIX4 PIRQ Signal	First PCI Expansion Slot: J4D2	Second PCI Expansion Slot: J4D1	Third PCI Expansion Slot: J4C1	Fourth PCI Expansion Slot: J4B1	A.G.P. Slot: J4E1	USB	Power Management
PIRQA	INTA	INTD	INTC	INTB			INTA
PIRQB	INTB	INTA	INTD	INTC	INTA		
PIRQC	INTC	INTB	INTA	INTD	INTB		
PIRQD	INTD	INTC	INTB	INTA		INTA	

For example, assume an add-in card has one interrupt (group INTA) into the fourth PCI slot. In this slot, an interrupt source from group INTA connects to the PIRQD signal, which is already connected to the onboard video and USB PCI sources. The add-in card shares an interrupt with these onboard interrupt sources.

Now, however, plug an add-in card that has one interrupt (group INTA) into the first PCI slot. Plug a second add-in card that has two interrupts (groups INTA and INTB) into the second PCI slot. INTA in the first slot is connected to signal PIRQA. INTA in the second slot is connected to signal PIRQB, and INTB is connected to signal PIRQC. With no other cards added, the three interrupt sources on the first two cards each have a PIRQ signal to themselves. Typically, they will not share an interrupt.

NOTE

The PIIX4 can connect each PIRQ line internally to one of the IRQ signals (3,4,5,7,9,11,14,15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

3 Overview of BIOS Features

3.1 Introduction

The motherboard uses an Intel/Phoenix BIOS, which is stored in flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the flash memory contains the Setup program, Power-On Self Test (POST), Advanced Power Management (APM), the PCI auto-configuration utility, and Windows 95-ready Plug and Play. See Section 6.2 for the supported versions of these specifications.

This motherboard supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a the revision code. The initial production BIOS is identified as 4A4LL0X0.86A.XXXX.PXX.

3.1.1 BIOS Upgrades

A new version of the BIOS can be upgraded from a diskette using the iFLASH.EXE utility that is available from Intel. This utility does BIOS upgrades as follows:

- Updates the flash BIOS from a file on a disk
- Updates the language section of the BIOS
- Makes sure that the upgrade BIOS matches the target system to prevent accidentally installing a BIOS for a different type of system.

BIOS upgrades and the iFLASH.EXE utility are available from Intel through the Intel World Wide Web site. See Section 6.1 for information about this site.

NOTE

Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.

3.1.2 BIOS Flash Memory Organization

The Intel PA28FB200BX 2-Mbit flash component is organized as 256 KB x 8 bits and is divided into areas as described in Table 40. The table shows the addresses in the ROM image in normal mode (the addresses change in BIOS Recovery Mode).

Table 40. Flash Memory Organization

Address (Hex)	Size	Description
FFFFC000 - FFFFFFFF	16 KB	Boot Block
FFFFA000 - FFFFBFFF	8 KB	Vital Product Data (VPD) Extended System Configuration Data (ESCD) (DMI configuration data / Plug and Play data)
FFFF9000 - FFFF9FFF	4 KB	Used by BIOS (e.g., for Event Logging)
FFFF8000 - FFFF8FFF	4 KB	OEM logo or Scan Flash Area
FFFC0000 - FFFF7FFF	224 KB	Main BIOS Block

3.1.3 Plug and Play: PCI Autoconfiguration

The BIOS automatically configures PCI devices and Plug and Play devices. PCI devices may be onboard or add-in cards. Plug and Play devices are ISA add-in cards built to meet the Plug and Play specification. Autoconfiguration lets a user insert or remove PCI or Plug and Play cards without having to configure the system. When a user turns on the system after adding a PCI or Plug and Play card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card or to system resources. The assignment of PCI interrupts to ISA IRQs is nondeterministic. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in the extended system configuration data (ESCD) format.

For information about the versions of PCI and Plug and Play supported by this BIOS, see Section 6.2. Copies of the specifications can be obtained from the Intel World Wide Web site (see Section 6.1).

3.1.4 PCI IDE Support

If Auto is selected as a primary or secondary IDE device (see Section 4.2.2) in Setup, the BIOS automatically sets up the two local-bus IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to PIO Mode 4 and recognizes any ATAPI devices, including CD-ROM drives and tape drives (see Section 6.2 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them so as to optimize capacity and performance. To take advantage of the high-capacity storage devices, hard drives are automatically configured for logical block addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. To override the autoconfiguration options, use the specific IDE device options in Setup. The ATAPI specification recommends that ATAPI devices be configured as shown in Table 41.

Table 41. Recommendations for Configuring an ATAPI Device

	Primary Cable		Secondary Cable	
Configuration	Drive 0	Drive 1	Drive 0	Drive 1
Normal, no ATAPI	ATA			
Disk and CD-ROM for enhanced IDE systems	ATA		ATAPI	
Legacy IDE system with only one cable	ATA	ATAPI		
Enhanced IDE with CD-ROM and a tape or two CD-ROMs	ATA		ATAPI	ATAPI

3.1.5 ISA Plug and Play

If Plug and Play operating system (see Section 4.3) is selected in Setup, the BIOS autoconfigures only ISA Plug and Play cards that are required for booting (IPL devices). If Plug and Play operating system is not selected in Setup, the BIOS autoconfigures all Plug and Play ISA cards.

3.1.6 ISA Legacy Devices

Since ISA legacy devices are not autoconfigurable, the resources for them must be reserved. Resources can be reserved in the Setup program or with an ISA configuration utility. The ISA configuration utility can be downloaded from the Intel World Wide Web site (see Section 6.1).

3.1.7 Desktop Management Interface (DMI)

Desktop Management Interface (DMI) is an interface for managing computers in an enterprise environment. The main component of DMI is the management information format (MIF) database, which contains information about the computing system and its components. Using DMI, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel LANDesk Client Manager to use DMI. The BIOS stores and reports the following DMI information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

OEMs can use a utility that programs flash memory so the BIOS can report on system and chassis information. This utility is available through Intel sales offices. See Section 6.1 for information about contacting a local Intel sales office. See Section 6.2 for information about the latest DMI specification.

DMI does not work directly under non-Plug and Play operating systems (e.g., Windows NT). However, the BIOS supports a DMI table interface for such operating systems. Using this support, a DMI service-level application running on a non-Plug and Play OS can access the DMI BIOS information.

3.1.8 Advanced Power Management (APM)

The BIOS supports APM and standby mode. See Section 6.2 for the version of the APM specification that is supported. The energy saving standby mode can be initiated in the following ways:

- Time-out period specified in Setup
- Suspend/resume switch connected to the front panel sleep connector
- From the operating system, such as the Suspend menu item in Windows 95

In standby mode, the motherboard reduces power consumption by using SMM capabilities, spinning down hard drives, and reducing power to or turning off VESA† DPMS-compliant monitors. Power-management mode can be enabled or disabled in Setup (see Section 4.5).

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default; but the operating system must support an APM driver for the power-management features to work. For example, Windows 95 supports the power-management features upon detecting that APM is enabled in the BIOS.

3.1.9 Language Support

The Setup program and help messages can be supported in 32 languages. Five languages are available: American English, German, Italian, French, and Spanish. The default language is American English, which is present unless another language is programmed into the BIOS using the flash memory update utility. See Section 3.1.1 for information about the BIOS update utility.

The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets. Translations of other languages may become available at a later date.

3.1.10 Boot Options

In the Setup program, the user can choose to boot from a floppy drive, hard drive, CD-ROM, or the network. The default setting is for the floppy drive to be the primary boot device and the hard drive to be the secondary boot device. By default the third and fourth devices are disabled.

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. See Section 6.2 for information about the El Torito specification. Under the Boot menu in the Setup program, CD-ROM is listed as a boot device. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device.

The network can be selected as a boot device. This selection allows booting from a network add-in card with a remote boot ROM installed.

3.1.11 OEM Logo or Scan Area

A 4 KB flash-memory user area at memory location FFFF8000h-FFFF8FFFh is for displaying a custom OEM logo during POST. A utility is available from Intel to assist with installing a logo into the flash memory. Contact Intel customer support for further information. See Section 6.1 for information on contacting Intel customer support.

3.1.12 USB Support

The USB connectors allow any of several USB devices to be attached to the computer. Typically, the device driver for USB devices is managed by the operating system. However, because keyboard and mouse support may be needed in the Setup program before the operating system boots, the BIOS supports USB keyboards and mice.

3.1.13 BIOS Setup Access

Access to the Setup program can be restricted using passwords. User and supervisor passwords can be set using the Security menu in Setup. The default is no passwords enabled. See Section 4.4 for information about setting user and supervisor passwords.

3.1.14 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode (see Section 1.15.3).

To create a BIOS recovery diskette, a bootable diskette must be created and the recovery files copied to it. The recovery files are available from Intel, contact Intel customer support for further information. See Section 6.1 for information on contacting Intel customer support.

4 BIOS Setup Program

The Setup program is for viewing and changing the BIOS settings for a computer. Setup is accessed by pressing the <F2> key after the Power-On Self Test (POST) memory test begins and before the operating system boot begins.

Table 42 shows the menus available from the menu bar at the top of the Setup screen.

Table 42. Setup Menu Bar

Setup Menu Screen	Description
Maintenance	Specifies the processor speed and clears the Setup passwords. This is only available in configure mode. Refer to Section 1.15.2 for information about configure mode.
Main	Allocates resources for hardware components.
Advanced	Specifies advanced features available through the chipset.
Security	Specifies passwords and security features.
Power	Specifies power management features.
Boot	Specifies boot options and power supply controls.
Exit	Saves or discards changes to the Setup program options.

Table 43 shows the function keys available for menu screens.

Table 43. Setup Function Keys

Setup Key	Description
<F1> or <Alt-H>	Brings up a help screen for the current item.
<Esc>	Exits the menu.
<←> or <→>	Selects a different menu screen.
<↑> or <↓>	Moves cursor up or down.
<Home> or <End>	Moves cursor to top or bottom of the window.
<PgUp> or <PgDn>	Moves cursor to top or bottom of the window.
<F5> or <->	Selects the previous value for a field.
<F6> or <+> or <Space>	Selects the next value for a field.
<F9>	Load the default configuration values for the current menu.
<F10>	Save the current values and exit Setup.
<Enter>	Executes command or selects the submenu.

4.1 Maintenance Menu

This menu is for setting the processor speed and clearing the Setup passwords. Setup only displays this menu in configure mode. See Section 1.15.2 for information about setting configure mode.

Table 44. Maintenance Menu

Feature	Options	Description
Processor Speed	• 200 • 233 • 266 • 300	Specifies the processor speed in megahertz.
Clear All Passwords	No options	Clears the user and supervisor passwords.

4.2 Main Menu

This menu reports processor and memory information and is for configuring the system date, system time, floppy options, and IDE devices.

Table 45. Main Menu

Feature	Options	Description
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
Cache RAM	No options	Displays size of second-level cache.
Total Memory	No options	Displays the total amount of RAM on the motherboard.
BIOS Version	No options	Displays the version of the BIOS.
Language	English (US)	Selects the default language used by the BIOS.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Month, day, and year	Specifies the current date.
Floppy Options, submenu	No option	When selected, displays the Floppy Options submenu.
Primary IDE Master, submenu	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave, submenu	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master, submenu	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
Secondary IDE Slave, submenu	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.2.1 Floppy Options Submenu

This submenu is for configuring floppy drives.

Table 46. Floppy Options Submenu

Feature	Options	Description
Diskette A:	• Disabled • 360 KB, 5¼″ • 1.2 MB, 5¼″ • 720 KB, 3½″ • **1.44/1.25 MB, 3½″ (default)** • 2.88 MB, 3½″	Specifies the capacity and physical size of diskette drive A.
Diskette B:	• **Disabled (default)** • 360 KB, 5¼″ • 1.2 MB, 5¼″ • 720 KB, 3½″ • 1.44/1.25 MB, 3½″ • 2.88 MB, 3½″	Specifies the capacity and physical size of diskette drive B.
Floppy Write Protect	• **Disabled (default)** • Enabled	Disables or enables write protect for the diskette drive(s).

4.2.2 IDE Device Configuration Submenus

This submenu is for configuring IDE devices, including:

- Primary IDE master
- Primary IDE slave
- Secondary IDE master
- Secondary IDE slave

Table 47. IDE Device Configuration Submenus

Feature	Options	Description
Type	• None • ATAPI Removable • CD-ROM • User • **Auto (default)**	Specifies the IDE configuration mode for IDE devices. User allows the cylinders, heads, and sectors fields to be changed. Auto automatically fills in the values for the cylinders, heads, and sectors fields.
Cylinders	1 to *XXXX*	Specifies number of disk cylinders.
Heads	1 to 16	Specifies number of disk heads.
Sectors	1 to 64	Specifies number of disk sectors.
Maximum Capacity	No options	Reports the maximum capacity for the hard disk. Value calculated from number of cylinders, heads, and sectors.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard drive to memory. Check the hard drive's specifications for optimum setting.
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables logical block addressing (LBA) in place of the Cylinders, Heads, and Sectors fields. ⚠ **CAUTION** *Changing the LBA Mode Control after a hard drive has been formatted can corrupt data on the drive.*
Transfer Mode	• Standard • Fast PIO 1 • Fast PIO 2 • Fast PIO 3 • **Fast PIO 4 (default)**	Specifies method for transferring data between the hard drive and system memory.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2	Specifies the ultra DMA mode for the hard drive.

4.3 Advanced Menu

This menu is for setting advanced features that are available through the chipset.

Table 48. Advanced Menu

Feature	Options	Description
Plug & Play O/S	• No • **Yes (default)**	Specifies if a Plug and Play operating system is being used. No lets the BIOS configure all devices. Yes lets the operating system configure Plug and Play devices. Not required with a Plug and Play operating system.
Reset Configuration Data	• **No (default)** • Yes	Clears the BIOS configuration data on the next boot.
Memory Cache	• Disabled • **Enabled (default)**	Enables or disables the memory cache.
ECC Configuration	• **Non-ECC (default)** • ECC	Specifies ECC memory operation.
Resource Configuration, submenu	No options	Configures memory blocks and IRQs for legacy ISA devices. When selected, displays the Resource Configuration submenu.
Peripheral Configuration, submenu	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
Keyboard Features, submenu	No options	Configures keyboard features. When selected, displays the Keyboard Features submenu.
Video Configuration, submenu	No options	Configures video features. When selected, displays the Video Configuration submenu.
DMI Events Logging, submenu	No options	Configures DMI Events Logging. When selected, displays the DMI Events Logging submenu.

4.3.1 Resource Configuration Submenu

This submenu is for configuring the memory and interrupts.

Table 49. Resource Configuration Submenu

Feature	Options	Description
Memory Reservation	• C800 - CBFF **Available (default)** | Reserved • CC00- CFFF **Available (default)** | Reserved • D000 - D3FF **Available (default)** | Reserved • D400 - D7FF **Available (default)** | Reserved • D800 - DBFF **Available (default)** | Reserved • DC00 - DFFF **Available (default)** | Reserved • Memory hole **Disabled (default)** | Conventional | Extended	Reserves specific upper memory blocks for use by legacy ISA devices. Memory hole frees address space in RAM for an legacy ISA boards.
IRQ Reservation	• IRQ3 **Available (default)** | Reserved • IRQ4 **Available (default)** | Reserved • IRQ5 **Available (default)** | Reserved • IRQ7 **Available (default)** | Reserved • IRQ10 **Available (default)** | Reserved • IRQ11 **Available (default)** | Reserved	Reserves specific IRQs for use by legacy ISA devices. An * (asterisk) displayed next to an IRQ indicates an IRQ conflict.

4.3.2 Peripheral Configuration Submenu

This submenu is for the configuring the computer peripherals.

Table 50. Peripheral Configuration Submenu

Feature	Options	Description
Serial port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. Auto assigns the first free COM port, normally COM1, the address 3F8h and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Serial port B	• Disabled • Enabled • **Auto (default)**	Configures serial port B. Auto assigns the first free COM port, normally COM2, the address 2F8h and the interrupt IRQ3. An * (asterisk) displayed next to an address indicates a conflict with another device. If either serial port address is set, that address will not appear in the list of options for the other serial port. If an *ATI mach32*† or an *ATI mach64*† video controller is active as an add-in card, the COM4, 2E8h address will not appear in the list of options for either serial port.
Mode	• **Normal (default)** • IrDA • ASK-IR	Specifies the mode for Serial Port B for normal (COM 2) or infrared applications.
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. Auto assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. Output Only operates in AT†-compatible mode. Bi-directional operates in bidirectional PS/2-compatible mode. EPP is Extended Parallel Port mode, a high-speed bidirectional mode. ECP is Enhanced Capabilities Port mode, a high-speed bidirectional mode.
Floppy disk controller	• Disabled • **Enabled (default)**	Configures the floppy disk controller.
IDE controller	• Disabled • Primary • Secondary • **Both (default)**	Configures the IDE controller. Both specifies both the primary and secondary the primary and secondary channel are used.
Audio	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
Legacy USB Support	• **Disabled (default)** • Enabled	Enables support for legacy universal serial bus devices.

4.3.3 Keyboard Features Submenu

This submenu is for setting keyboard features.

Table 51. Keyboard Features Submenu

Feature	Options	Description
Numlock	• **Auto (default)** • On • Off	Specifies the power on state of the Numlock feature on the numeric keypad of the keyboard.
Key Click	• **Disabled (default)** • Enabled	Enables the key click option.
Keyboard auto-repeat rate	• **30/sec (default)** • 26.7/sec • 21.8/sec • 18.5/sec • 13.3/sec • 10/sec • 6/sec • 2/sec	Selects the key repeat rate.
Keyboard auto-repeat delay	• ¼ sec • **½ sec (default)** • ¾ sec • 1 sec	Selects the delay before key repeat.

4.3.4 Video Configuration Submenu

This submenu is for configuring video features.

Table 52. Video Configuration Submenu

Feature	Options	Description
Palette Snooping	• **Disabled (default)** • Enabled	Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card.

4.3.5 DMI Event Logging Submenu

This submenu is for setting keyboard features.

Table 53. DMI Event Logging Submenu

Feature	Options	Description
Event log capacity	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
View DMI event log	No options	Enables viewing of DMI event log.
Clear all DMI event logs	• **No (default)** • Yes	Clears the DMI Event Log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of DMI events.
ECC Event Logging	• **Disabled (default)** • Enabled	Enables logging of ECC events.
Mark DMI events as read	No options	Marks all DMI events as read.

4.4 Security Menu

This menu is for setting passwords and security features.

Table 54. Security Menu

Feature	Options	Description
User Password Is	No options	Reports if there is a user password set.
Supervisor Password Is	No options	Reports if there is a supervisor password set.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Unattended Start	• **Disabled (default)** • Enabled	Enables the unattended start feature. When enabled, the computer boots, but the keyboard is locked. The user must enter a password to unlock the computer or boot from a floppy diskette.

4.5 Power Menu

This menu is for setting power management features.

Table 55. Power Menu

Feature	Options	Description
Power Management	• Disabled • **Enabled (default)**	Enables or disables the BIOS power management feature.
Fan Always On	• No • **Yes (default)**	Forces fan(s) connected to the onboard fan header(s) to remain on when the computer is in a power management state.
Inactivity Timer	• **Off (default)** • 1 Minute • 2 Minutes • 4 Minutes • 6 Minutes • 8 Minutes • 12 Minutes • 16 Minutes	Specifies the amount of time before the computer enters standby mode.
Hard Drive	• Disabled • **Enabled (default)**	Enables power management for hard disks during standby and suspend modes.
VESA Video Power Down	• Disabled • **Enabled (default)**	Enables power management for video during standby and suspend modes.

4.6 Boot Menu

This menu is for setting the boot features and the boot sequence.

Table 56. Boot Menu

Feature	Options	Description
Restore on AC/Power Loss	• Stay Off • **Last State (default)** • Power On	Specifies how the computer responds following a power failure. Stay Off keeps power off until power button pressed. Last State restores previous power state before a power failure. Power On restores power without restoring previous power state.
On Modem Ring	• Stay Off • **Power On (default)**	Specifies how the computer responds to an incoming call on an installed modem when the power is off.
On LAN	• Stay Off • **Power On (default)**	Specifies how the computer responds to a LAN wakeup event when the power is off.
On PME	• Stay Off • **Power On (default)**	Specifies how the computer responds to a PCI power management enable event when the power is off.
QuickBoot Mode	• Enabled • **Disabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
First Boot Device Second Boot Device Third Boot Device Fourth Boot Device	• Removable devices • Hard Drive • ATAPI CD-ROM Drive • Network boot	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering.
Hard Drive, submenu	No options	Lists available hard drives. When selected, displays the Hard Drive submenu.
Removable Devices, submenu	No options	Lists available removable devices. When selected, displays the Removable Devices submenu.

4.6.1 Hard Drive Submenu

This submenu is for configuring the boot sequence for hard drives.

Table 57. Hard Drive Submenu

Options	Description
• Installed hard drive • Bootable ISA Cards	Specifies the boot sequence for the hard drives attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.6.2 Removable Devices Submenu

This submenu is for configuring the boot sequence for removable devices.

Table 58. Removable Devices Submenu

Options	Description
• Legacy Floppy Drives	Specifies the boot sequence for the removable hard drives attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.7 Exit Menu

This menu is for exiting the Setup program, saving changes, and loading and saving defaults.

Table 59. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS RAM.
Exit Discarding Changes	Exits without saving any changes made in Setup.
Load Setup Defaults	Loads the default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

5.1 BIOS Error Messages

Table 60. BIOS Error Messages

Error Message	Explanation
Diskette drive A error or Diskette drive B error	Drive A: or B: is present but fails the POST diskette tests. Check that the drive is defined with the proper diskette type in Setup and that the diskette drive is installed correctly.
Extended RAM Failed at offset: *nnnn*	Extended memory not working or not configured properly at offset *nnnn*.
Failing Bits: *nnnn*	The hex number nnnn is a map of the bits at the RAM address (System, Extended, or Shadow memory) that failed the memory test. Each 1 in the map indicates a failed bit.
Fixed Disk 0 Failure or Fixed Disk 1 Failure or Fixed Disk Controller Failure	Fixed disk is not working or not configured properly. Check to see if fixed disk is installed properly. Run Setup be sure the fixed-disk type is correctly identified.
Incorrect Drive A type - run SETUP	Type of floppy drive for drive A: not correctly identified in Setup.
Incorrect Drive B type - run SETUP	Type of floppy drive for drive B: not correctly identified in Setup.
Invalid NVRAM media type	Problem with NVRAM (CMOS) access.
Keyboard controller error	The keyboard controller failed test. Try replacing the keyboard.
Keyboard error	Keyboard not working.
Keyboard error nn	BIOS discovered a stuck key and displays the scan code nn for the stuck key.
Keyboard locked - Unlock key switch	Unlock the system to proceed.
Monitor type does not match CMOS - Run SETUP	Monitor type not correctly identified in Setup.
Operating system not found	Operating system cannot be located on either drive A: or drive C:. Enter Setup and see if fixed disk and drive A: are properly identified.
Parity Check 1	Parity error found in the system bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Parity Check 2	Parity error found in the I/O bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Press <F1> to resume, <F2> to Setup	Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change any settings.

continued ☛

Table 60. BIOS Error Messages (continued)

Error Message	Explanation
Real time clock error	Real-time clock fails BIOS test. May require motherboard repair.
Shadow RAM Failed at offset: *nnnn*	Shadow RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System battery is dead - Replace and run SETUP	The CMOS clock battery indicator shows the battery is dead. Replace the battery and run Setup to reconfigure the system.
System cache error - Cache disabled	RAM cache failed the BIOS test. BIOS disabled the cache.
System CMOS checksum bad - run SETUP	System CMOS RAM has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. Run Setup and reconfigure the system either by getting the default values and/or making your own selections.
System RAM Failed at offset: *nnnn*	System RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System timer error	The timer test failed. Requires repair of system motherboard.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display. These cards can be purchased from JDR Microdevices or other sources.

The following table provides the POST codes that can be generated by the BIOS. Some codes are repeated in the table because that code applies to more than one operation.

Table 61. Port 80h Codes

Code	Description of POST Operation
02h	Verify real mode
03h	Disable non-maskable interrupt (NMI)
04h	Get processor type
06h	Initialize system hardware
08h	Initialize chipset with initial POST values
09h	Set IN POST flag
0Ah	Initialize CPU registers
0Bh	Enable CPU cache
0Ch	Initialize caches to initial POST values
0Eh	Initialize I/O component
0Fh	Initialize the local bus IDE
10h	Initialize power management
11h	Load alternate registers with initial POST valuesnew
12h	Restore CPU control word during warm boot
13h	Initialize PCI bus mastering devices
14h	Initialize keyboard controller
16h	BIOS ROM checksum
17h	Initialize cache before memory autosize
18h	8254 timer initialization
1Ah	8237 DMA controller initialization
1Ch	Reset programmable interrupt controller
20h	Test DRAM refresh
22h	Test keyboard controller
24h	Set ES segment register to 4 GB
26h	Enable A20 line
28h	Autosize DRAM
29h	Initialize POST memory manager

continued ☛

Table 61. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
2Ah	Clear 512 KB base RAM
2Ch	RAM failure on address line *xxxx**
2Eh	RAM failure on data bits *xxxx** of low byte of memory bus
2Fh	Enable cache before system BIOS shadow
30h	RAM failure on data bits *xxxx** of high byte of memory bus
32h	Test CPU bus-clock frequency
33h	Initialize POST dispatch manager
34h	Test CMOS RAM
35h	Initialize alternate chipset registers
36h	Warm start shut down
37h	Reinitialize the chipset (MB only)
38h	Shadow system BIOS ROM
39h	Reinitialize the cache (MB only)
3Ah	Autosize cache
3Ch	Configure advanced chipset registers
3Dh	Load alternate registers with CMOS valuesnew
40h	Set Initial CPU speed new
42h	Initialize interrupt vectors
44h	Initialize BIOS interrupts
45h	POST device initialization
46h	Check ROM copyright notice
47h	Initialize manager for PCI option ROMs
48h	Check video configuration against CMOS RAM data
49h	Initialize PCI bus and devices
4Ah	Initialize all video adapters in system
4Bh	Display QuietBoot screen
4Ch	Shadow video BIOS ROM
4Eh	Display BIOS copyright notice
50h	Display CPU type and speed
51h	Initialize EISA motherboard
52h	Test keyboard
54h	Set key click if enabled
56h	Enable keyboard
58h	Test for unexpected interrupts
59h	Initialize POST display service
5Ah	Display prompt "Press F2 to enter SETUP"
5Bh	Disable CPU cache

continued ☛

Table 61. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
5Ch	Test RAM between 512 and 640 KB
60h	Test extended memory
62h	Test extended memory address lines
64h	Jump to UserPatch1
66h	Configure advanced cache registers
67h	Initialize multiprocessor APIC
68h	Enable external and processor caches
69h	Setup System Management Mode (SMM) area
6Ah	Display external L2 cache size
6Ch	Display shadow-area message
6Eh	Display possible high address for UMB recovery
70h	Display error messages
72h	Check for configuration errors
74h	Test real-time clock
76h	Check for keyboard errors
7Ah	Test for key lock on
7Ch	Set up hardware interrupt vectors
7Eh	Initialize coprocessor if present
80h	Disable onboard Super I/O ports and IRQs
81h	Late POST device initialization
82h	Detect and install external RS232 ports
83h	Configure non-MCD IDE controllers
84h	Detect and install external parallel ports
85h	Initialize PC-compatible PnP ISA devices
86h	Re-initialize onboard I/O ports
87h	Configure motherboard configurable devices
88h	Initialize BIOS Data Area
89h	Enable Non-Maskable Interrupts (NMIs)
8Ah	Initialize extended BIOS data area
8Bh	Test and initialize PS/2 mouse
8Ch	Initialize floppy controller
8Fh	Determine number of ATA drives
90h	Initialize hard-disk controllers
91h	Initialize local-bus hard-disk controllers
92h	Jump to UserPatch2
93h	Build MPTABLE for multiprocessor boards
94h	Disable A20 address line (Rel. 5.1 and earlier)
95h	Install CD ROM for boot

continued ☛

Table 61. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
96h	Clear huge ES segment register
97h	Fix up multiprocessor table
98h	Search for option ROMs
99h	Check for SMART Drive
9Ah	Shadow option ROMs
9Ch	Set up power management
9Eh	Enable hardware interrupts
9Fh	Determine number of ATA and SCSI drives
A0h	Set time of day
A2h	Check key lock
A4h	Initialize typematic rate
A8h	Erase F2 prompt
AAh	Scan for F2 key stroke
ACh	Enter SETUP
AEh	Clear IN POST flag
B0h	Check for errors
B2h	POST done - prepare to boot operating system
B4h	One short beep before boot
B5h	Terminate QuietBoot
B6h	Check password (optional)
B8h	Clear global descriptor table
B9h	Clean up all graphics
BAh	Initialize DMI parameters
BBh	Initialize PnP Option ROMs
BCh	Clear parity checkers
BDh	Display MultiBoot menu
BEh	Clear screen (optional)
BFh	Check virus and backup reminders
C0h	Try to boot with INT 19
C1h	Initialize POST Error Manager (PEM)
C2h	Initialize error logging
C3h	Initialize error display function
C4h	Initialize system error handler

continued ☛

Table 61. Port 80h Codes (continued)

Code	Description of POST Operation (The following are for boot block in flash ROM)
E0h	Initialize the chipset
E1h	Initialize the bridge
E2h	Initialize the processor
E3h	Initialize system timer
E4h	Initialize system I/O
E5h	Check force recovery boot
E6h	Checksum BIOS ROM
E7h	Go to BIOS
E8h	Set huge segment
E9h	Initialize multiprocessor
EAh	Initialize OEM special code
EBh	Initialize PIC and DMA
ECh	Initialize memory type
EDh	Initialize memory size
EEh	Shadow boot block
EFh	System memory test
F0h	Initialize interrupt vectors
F1h	Initialize runtime clock
F2h	Initialize video
F3h	Initialize beeper
F4h	Initialize boot
F5h	Clear huge segment
F6h	Boot to mini-DOS
F7h	Boot to full DOS

5.3 BIOS Beep Codes

Beeps codes represent a terminal error. If the BIOS detects a terminal error condition, it outputs an error beep code, halts the POST, and attempts to display a port 80h code on the POST card's LED display.

Table 62. Beep Codes

Beeps	80h Code	Description
1	B4h	One short beep before boot
1-2	98h	Search for option ROMs
1-2-2-3	16h	BIOS ROM checksum
1-3-1-1	20h	Test DRAM refresh
1-3-1-3	22h	Test keyboard controller
1-3-4-1	2Ch	RAM failure on address line *xxxx**
1-3-4-3	2Eh	RAM failure on data bits *xxxx** of low byte of memory bus
1-4-1-1	30h	RAM failure on data bits *xxxx** of high byte of memory bus
2-1-2-3	46h	Check ROM copyright notice
2-2-3-1	58h	Test for unexpected interrupts

6 Specifications and Customer Support

6.1 Online Support

Find information about Intel boards under “Product Info” or “Customer Support” at this World Wide Web site:

http://www.intel.com/

6.2 Specifications

The motherboard complies with the following specifications:

Table 63. Compliance with Specifications

Specification	Description	Revision Level
A.G.P.	Accelerated Graphics Port Interface Specification	Revision 1.0, July, 1996, Intel Corporation. The specification is available through the Accelerated Graphics Implementers Forum at: http://www.agpforum.org/.
APM	Advanced Power Management BIOS interface specification	Revision 1.2, February, 1996 Intel Corporation, Microsoft Corporation
ATA-3	Information Technology - AT Attachment-3 Interface	X3T10/2008D Revision 6 ATA Anonymous FTP Site: fission.dt.wdc.com
ATAPI	ATA Packet Interface for CD-ROMs	SFF-8020i Revision 2.5 (SFF) Fax Access: (408) 741-1600
ATX	ATX form factor specification	Revision 2.01, February 1997 Intel Corporation, The specification is available at: http://www.intel.com/
DMI	Desktop Management Interface BIOS specification	Version 2.0, October 16, 1995 American Megatrends Inc., Award Software International Inc., Dell Computer Corporation, Intel Corporation, Phoenix Technologies Ltd., SystemSoft Corporation
El Torito	Bootable CD-ROM format specification	Version 1.0, January 25, 1995 Phoenix Technologies Ltd., IBM Corporation. The El Torito specification is available on the Phoenix Web site http://www.ptltd.com/techs/specs.html.
EPP	Enhanced Parallel Port	IEEE 1284 standard, Mode [1 or 2], v1.7

continued ☛

Table 63. Compliance with Specifications (continued)

IrDA	Serial Infrared Physical Layer Link specification	Version 1.1, October 17, 1995 Infrared Data Association.
Management extension hardware	LM78 Microprocessor System Hardware Monitor	Current Web site: http://www.national.com/pf/LM/LM78.html
PCI	PCI Local Bus specification	Revision 2.1, June 1, 1995, PCI Special Interest Group
Phoenix BIOS	PhoenixBIOS	Revision 4.0, February 27, 1997, Phoenix Technologies Ltd.
Plug and Play	Plug and Play BIOS specification	Version 1.0a, May 5, 1994 Compaq Computer Corporation, Phoenix Technologies Ltd., Intel Corporation
SDRAM DIMMs (64-bit)	4-Clock, 66 MHz, 64-bit Unbuffered DIMM specification	Revision 1.0, January 27, 1997, Intel Corporation
SDRAM DIMMs (72-bit)	4-Clock 66 MHz 72-bit Unbuffered DIMM specification	Revision 1.0, January 27, 1997, Intel Corporation
USB	Universal serial bus specification	Revision 1.0, January 15, 1996 Compaq Computer Corporation, Digital Equipment Corporation, IBM PC Company, Intel Corporation, Microsoft Corporation, NEC, Northern Telecom

Index

D

E

F

G - H

I

J - K

L

M

N - O

P

R

S

T

U

V

W