KU440EX Motherboard

Technical Product Specification

May 1998

Order Number 704768-001

The KU440EX motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the KU440EX Motherboard Specification Update.

Revision History

Revision	Revision History	Date
001	Final release of the KU440EX Motherboard Technical Product Specification.	April 1998

This product specification applies only to standard KU440EX motherboards with BIOS identifier 4K4UE0X0.86A.000X.P0X.

Changes to this specification will be published in the KU440EX Motherboard Specification Update before being incorporated into a revision of this document.

Contents

1 Motherboard Description

1.1 Overview

The KU440EX motherboard is a versatile platform that offers a wide variety of features. Many of the options, however, are implemented – at least in part – on the riser. Throughout this manual, the ‡ symbol is used to indicate such an option. Because there is no standard riser, no detailed description of an implementation can be given. See Section 6.1 to obtain the reference design for the NLX riser.

The KU440EX motherboard uses the NLX form factor (8.25 x 10.0 inches) and has the following features:

Microprocessor:

- Single Pentium® II processor operating at 233, 266, 300, or 333 MHz
- Intel® Celeron™ processor operating at 266 MHz
- 66 MHz host bus speed
- Slot 1 connector which provides an upgrade path that includes higher performance processors

Main memory:

- Two 168-pin DIMM sockets
- Supports from 8 MB up to 256 MB of synchronous DRAM (SDRAM) memory

Intel® 82440EX AGPset and PCI/IDE Interface

- Intel 82443EX PCI/A.G.P. controller (PAC)
  - Integrated PCI bus mastering controller
  - Integrated Accelerated Graphics Port (A.G.P.) controller
- Intel 82371EB PCI ISA IDE Xcelerator (PIIX4E)
  - Supports up to four IDE drives or devices
  - Multifunction PCI-to-ISA bridge
  - Universal Serial Bus (USB) and DMA controllers
  - Two fast IDE interfaces
  - Power management logic
  - Real-time clock

I/O features:

- SMC FDC37M707QFP I/O controller
  - Integrates standard I/O functions
- Two USB ports

Audio subsystem:

- Crystal Audio 4235 ISA controller

Graphics subsystem

- ATI Rage† IIC A.G.P. controller
- 2 or 4 MB SGRAM

Expansion slots

- Riser dependent

Other features

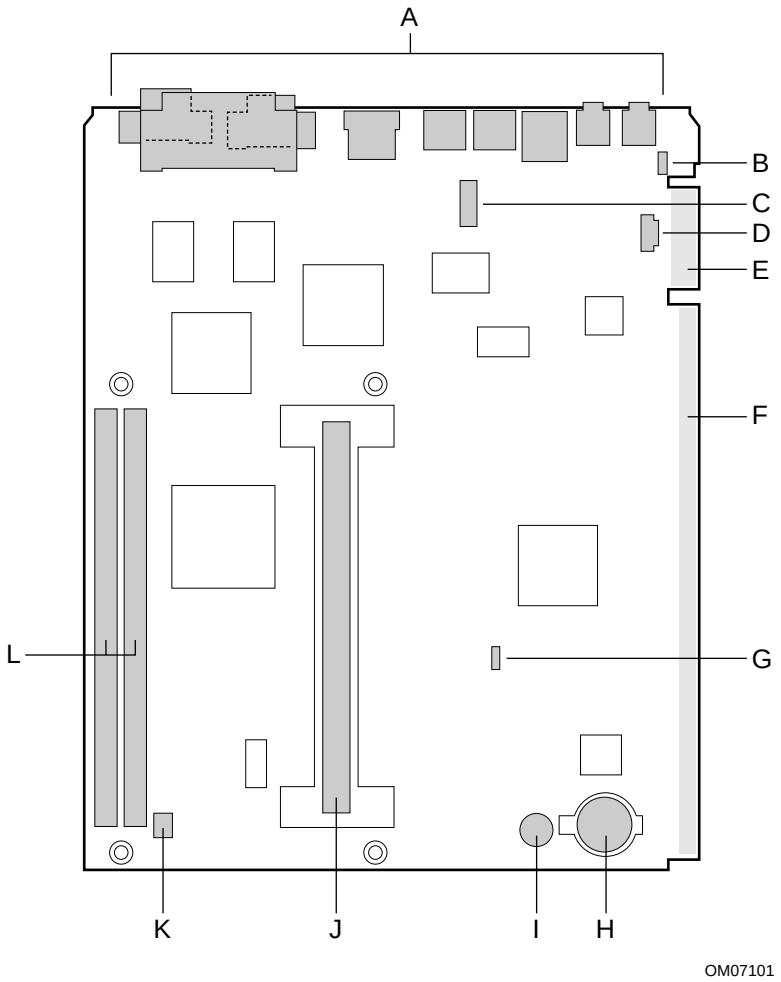
- Plug and Play compatible
- Support for Advanced Power Management (APM)
- Advanced Configuration and Power Management Interface (ACPI) ready
- Support for WfM 1.1a
- Support for Management Level 3.0

1.2 Manufacturing Options

The following is a list of manufacturing options. Not all manufacturing options are available in all marketing channels. Please contact your Intel representative to determine which options are available to you.

- ATI Rage Pro Turbo A.G.P. controller
- 4 MB SGRAM

1.3 Motherboard Components



A	Back panel connectors	G	Configuration jumper
B	Microphone routing jumper	H	Battery
C	COM2 header	I	Piezoelectric speaker
D	CD-ROM audio connector	J	Slot 1 connector
E	NLX edge connector (supplemental)	K	Processor fan connector
F	NLX edge connector	L	DIMM sockets

Figure 1. Motherboard Components

1.4 Form Factor

The motherboard is designed to fit into a or a full NLX form-factor chassis. The outer dimensions are 8.25 x 10.0 inches. (Full NLX dimensions are 9.0 x 13.0 inches.) Figure 2 shows that the mechanical form factor, the I/O connector locations, and the mounting hole locations are in compliance with the NLX specification (see Section 6.2).

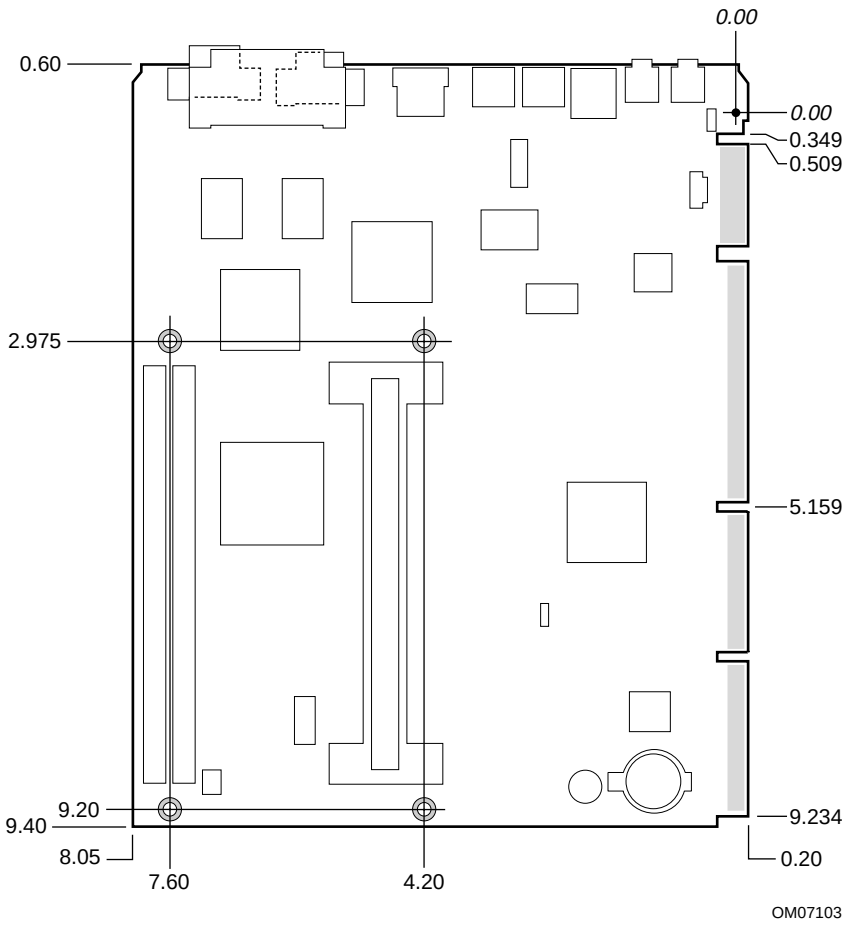


Figure 2. Motherboard Dimensions

1.5 I/O Shield

The back panel I/O shield for the motherboard must meet specific dimension and material requirements. Systems based on this motherboard need the back panel I/O shield to pass certification testing. Figure 3 shows the critical dimensions of the chassis-dependent I/O shield. The figure indicate the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the NLX specification. See Section 6.2 for information about the NLX specification.

NOTE

A chassis-independent I/O shield designed to be compliant with the NLX specification 1.2 is available from Intel.

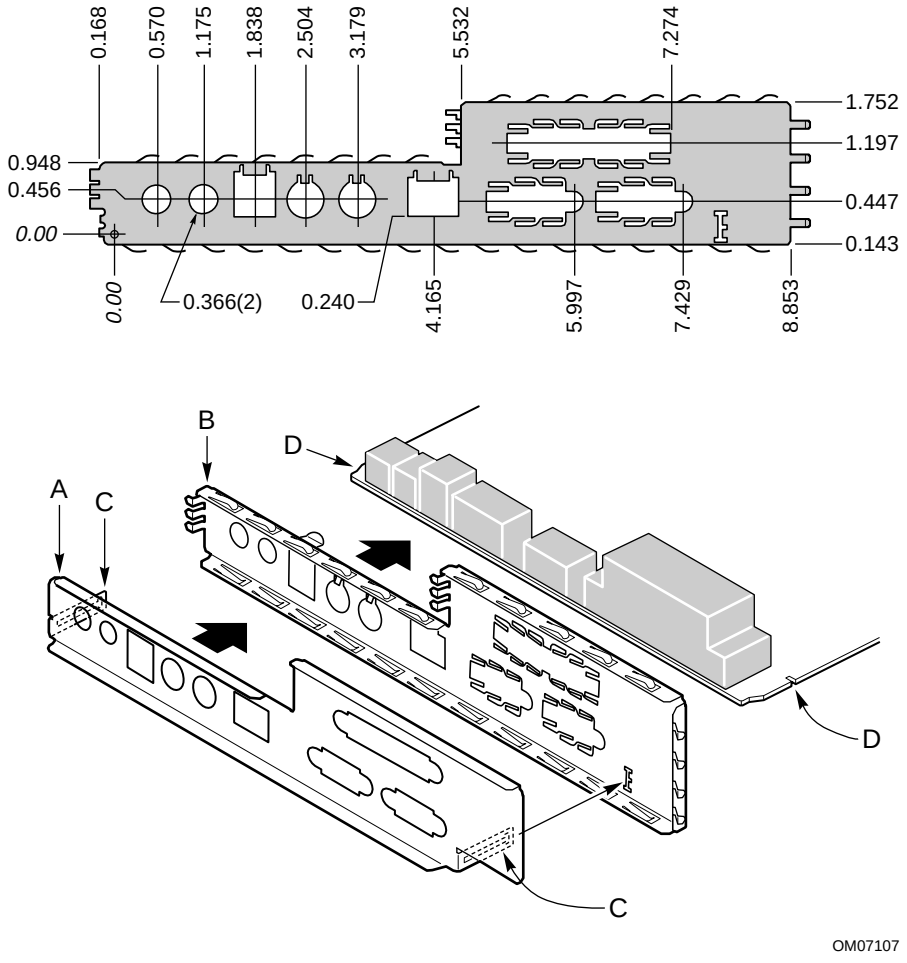


Figure 3. Back Panel I/O Shield Dimensions

1.6 Microprocessor

The motherboard supports a single Pentium II or Celeron processor. The processor's VID pins automatically program the voltage regulator on the motherboard to the required processor voltage. In addition, the 66 MHz host bus speed is automatically selected.

The motherboard will support either the low cost cartridge retention mechanism (LC-RM) or the retention mechanism specifically designed for the Celeron processor (C-RM).

NOTE

The motherboard has 0.159" mounting holes to accommodate the new plastic studs. The older style studs are too small and can not *be used.*

The motherboard supports the following processor configurations:

Processor Type	Processor Speed	Host Bus Speed	Retention Module
Pentium II	233 MHz 266 MHz 300 MHz 333 MHz	66 MHz	LC-RM
Celeron	266 MHz	66 MHz	C-RM

1.6.1 Microprocessor Packaging

The Pentium II processor is packaged in a Single Edge Contact (S.E.C.) cartridge. The cartridge includes the processor core, second-level cache subsystem, thermal plate, and back cover.

The Celeron processor is packaged in a Single Edge Processor (S.E.P.) package that includes the processor core only.

The processor connects to the motherboard through the Slot 1 connector, a 242-pin edge connector. When mounted in Slot 1, the processor is secured by a retention mechanism attached to the motherboard. A passive heatsink is stabilized by the heatsink support.

1.6.2 Second Level Cache

The Pentium II second-level cache is located on the substrate of the S.E.C. cartridge. The cache includes 512 KB of burst pipelined synchronous static RAM (BSRAM) and tag RAM. All supported onboard memory can be cached.

The Celeron processor does not have second level cache.

1.6.3 Microprocessor Upgrades

The motherboard can be upgraded with future steppings of the Pentium II or Celeron processor that run at higher speeds. When upgrading the processor, use the BIOS configure mode to change the processor speed (see Section 1.18).

1.7 Main Memory

The motherboard has two dual inline memory module (DIMM) sockets. Synchronous DRAM (SDRAM) can be installed in one or both sockets. In addition, the motherboard supports both serial presence detect (SPD) and non-SPD data structures.

Using the SPD data structure, programmed into an E^2PROM on the DIMM, the BIOS can determine the SDRAM's size and speed. Using the non-SPD data structure, the BIOS will dynamically determine SDRAM size and speed. Minimum memory size is 8 MB; maximum memory size is 256 MB. Memory size and speed can vary between sockets.

The motherboard supports the following memory features:

- 168-pin DIMMs with gold-plated contacts
- 66 MHz unbuffered SDRAM
- Non-ECC (64-bit) memory
- 3.3 V memory only
- Single- or double-sided DIMMs in the following sizes:

DIMM Size	Non-ECC Configuration
8 MB	1 Mbit x 64
16 MB	2 Mbit x 64
32 MB	4 Mbit x 64
64 MB	8 Mbit x 64
128 MB	16 Mbit x 64

NOTE

All memory components and DIMMs used with the KU440EX motherboard must comply with the PC Unbuffered DIMM Specification. You can access this document through the Internet at: http://www.intel.com/design/pcisets/memory/.

See Section 6.2 for information about this specification.

1.8 Chipset

The Intel® 440EX AGPset includes a Host-PCI bridge integrated with both an optimized DRAM controller and an Accelerated Graphics Port (A.G.P.) interface. The I/O subsystem of the 440EX is based on the PIIX4E, which is a highly integrated PCI-ISA/IDE Accelerator Bridge. This chipset consists of the Intel 82443EX PCI/A.G.P. controller (PAC) and the Intel 82371EB PCI/ISA IDE Xccelerator (PIIX4E) bridge chip.

1.8.1 Intel® 82443EX PCI/A.G.P. Controller (PAC)

The PAC provides bus-control signals, address paths, and data paths for transfers between the processor's host bus, the PCI bus, the A.G.P., and main memory. The PAC features:

- Processor interface control
  - — Support for processor host bus frequencies of 66 MHz
  - — 32-bit addressing
  - — Desktop Optimized GTL+ compliant host bus interface
- Integrated DRAM controller, with support for:
  - — +3.3 V only DIMM DRAM configurations
  - — Up to two double sided DIMMs
  - — Synchronous 66-MHz SDRAM
  - — DIMM serial presence detect via the SMBus interface
  - — 16- and 64-Mbit devices with 2 K, 4 K, and 8 K page sizes
  - — x 4, x 8, x 16, and x 32 DRAM widths
  - — SDRAM 64-bit data interface
  - — Symmetrical and asymmetrical DRAM addressing
- A.G.P. interface
  - — Complies with the A.G.P. specification Rev 1.0 (see Section 6.2 for specification information)
  - — Support for +3.3 V PCI devices, A.G.P.-66/133 devices
  - — Synchronous coupling to the host-bus frequency
- PCI bus interface
  - — Complies with the PCI specification Rev 2.1, +5 V 33 MHz interface (see Section 6.2 for specification information)
  - — Asynchronous coupling to the host-bus frequency
  - — PCI parity generation support
  - — Data streaming support for PCI-to-DRAM
  - — Support for three PCI bus masters in addition to the host and PCI-to-ISA I/O bridge
  - — Support for concurrent host, A.G.P., and PCI transactions to main memory
- Data buffering
  - — DRAM write buffer with read-around-write capability
  - — Dedicated host-to-DRAM, PCI0-to-DRAM, and PCI1/A.G.P.-to-DRAM read buffers
  - — A.G.P. dedicated inbound/outbound FIFOs (133/66 MHz), used for temporary data storage
- Power management functions
  - — Support for system suspend/resume
  - — Compliant with ACPI power management
- SMBus support for desktop management functions
- Support for system management mode (SMM)

1.8.2 Intel® 82371EB PCI ISA IDE Xcelerator (PIIX4E)

The PIIX4E is a multifunction PCI device implementing the PCI-to-ISA bridge, PCI IDE functionality, Universal Serial Bus (USB) host/hub functionality, and enhanced power management. The PIIX4E features:

- Multifunction PCI-to-ISA bridge
  - Support for the PCI bus at 33 MHz
  - Complies with the PCI specification (see Section 6.2 for specification information)
  - Full ISA bus support
- USB controller
  - Two USB ports (see Section 6.2 for specification information)
  - Support for legacy keyboard and mouse
  - Support for the Universal Host Controller Interface (UHCI) Design Guide, revision 1.1, interface
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers up to 16 MB/sec
  - Support for Ultra DMA/33 synchronous DMA mode transfers up to 33 MB/sec
  - Bus master mode with an 8 x 32-bit buffer for bus master PCI IDE burst transfers
- Enhanced DMA controller
  - Two 8237-based DMA controllers
  - Support for PCI DMA with three PC/PCI channels and distributed DMA protocols
- Interrupt controller based on 82C59
  - Support for 15 interrupts
  - Programmable for edge/level sensitivity
- Power management logic
  - Sleep/resume logic
  - Support for Wake on LAN† technology
  - Support for ACPI (see Section 6.2 for specification information)
- Real-Time Clock
  - 256-byte battery-backed CMOS SRAM
  - Includes date alarm
- 16-bit counters/timers based on 82C54

1.8.2.1 Universal Serial Bus (USB)

The motherboard has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The motherboard fully supports the universal host controller interface (UHCI) and uses UHCI-compatible software drivers. See Section 6.2 for information about the USB specification. USB features include:

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices

- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

1.8.2.2 IDE Support

The motherboard has two independent bus-mastering PCI IDE interfaces. These interfaces support PIO Mode 3, PIO Mode 4, ATAPI devices (such as CD-ROM), and Ultra DMA/33 synchronous-DMA mode transfers. The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The BIOS automatically detects the IDE device transfer rate and translation mode.

Programmed I/O operations usually require a substantial amount of processor bandwidth. However, in multitasking operating systems, the bandwidth freed by bus mastering IDE can be devoted to other tasks while disk transfers are occurring.

1.8.2.3 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program.

NOTE

The recommended method of accessing the date in systems with Intel® motherboards is indirectly from the Real Time Clock (RTC) via the BIOS. The BIOS on Intel motherboards and baseboards contains a century checking and maintenance feature that checks the least two significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

For more information on proper date access in systems with Intel motherboards please see http://support.intel.com/support/year2000/motherboard.htm

A coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3 V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 V applied.

1.9 I/O Interface Controller

The motherboard uses the SMC FDC37M707QFP I/O controller which features:

- Single diskette drive interface
- ISA Plug-and-Play compatible register set
- Two serial ports
- FIFO support on both serial and floppy interfaces
- One parallel port with ECP and EPP support
- PS/2† style mouse and keyboard interfaces
- PCI PME interface to PIIX4E
- Intelligent auto power management, including:
  - — Shadowed write-only registers for ACPI compliance
  - — Programmable wake-up event interface
  - — Wake on Modem support is available on the riser‡
  - — Support for Wake on Ring through an external modem connected to COM1

The Setup program provides configuration options for the I/O controller.

1.9.1 Serial Ports

The motherboard has two serial ports. COM1 is a 9-pin D-Sub serial port connector located on the back panel, and COM2 is a header located at J5J1. Both serial ports have NS16C550-compatible UARTs that support data transfers at speeds up to 115.2 Kbits/sec with BIOS support.

1.9.2 Infrared Support

There is no infrared header on the motherboard; however, the edge connector does accommodate infrared signals from the riser. If an IrDA† connector is available on the riser, use the BIOS Peripheral Configuration Submenu to change the mode for Serial Port B from COM2 to infrared applications. You will no longer be able to use Serial Port B.

1.9.3 Parallel Port

The connector for the multimode bi-directional parallel port is a 25-pin D-Sub connector located on the back panel of the motherboard. In the Setup program, there are four options for parallel port operation:

- Output only (standard mode)
- Bi-directional (PS/2 compatible)
- Bi-directional Enhanced Parallel Port (EPP). A driver from the peripheral manufacturer is required for operation. See Section 6.2 for EPP compatibility
- Bi-directional high-speed Extended Capabilities Port (ECP)

1.9.4 Diskette Drive Controller

The I/O controller is software compatible with the 82077 diskette drive controller and supports a single diskette drive in either PC-AT† and PS/2 modes. In the Setup program, the diskette drive interface can be configured for the following diskette drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.2 MB, 3.5-inch (driver required)
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

1.9.5 PS/2 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel of the motherboard. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an over-current condition is removed.

NOTE

The mouse and keyboard can be plugged into either PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains code which provides the traditional keyboard and mouse control functions and also supports Power On/Reset password protection. A Power On/Reset password can be specified in the BIOS Setup program.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del>, software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power On Self Test (POST).

1.10 Audio Subsystem

The audio subsystem consists of the following:

- Crystal Semiconductor CS4235 audio codec
- Back panel and onboard audio connectors

1.10.1 Crystal Semiconductor CS4235 Audio Codec

The CS4235 audio codec's features include:

- Compatibility with Roland MPU-401, Sound Blaster†, Sound Blaster Pro†, and Windows Sound System
- Advanced MPC3-compliant input and output mixer

1.10.2 Audio Connectors

The audio connectors include the following:

- Back panel connectors: stereo line-level output (Line-out) and Mic-in
- CD-ROM (2 mm) audio header

1.10.3 Audio Drivers and Utilities

Audio software and utilities are available from Intel's World Wide Web site (see Section 6.1). Audio driver support is provided for Microsoft Windows† 3.1, Microsoft Windows 95, and Microsoft Windows NT† operating systems.

Audio software and utilities are available from Intel's World Wide Web site (see Section 6.1).

1.11 Graphics Subsystem

The graphics subsystem features the ATI Rage IIC graphics controller. See Intel's World Wide Web site (see Section 6.1) for graphics drivers.

1.11.1 ATI Rage IIC Controller

The ATI Rage IIC provides the following features:

- A.G.P. support
- Full bus mastering support
- Triple 8-bit palette DAC with gamma correction. Pixel rates up to 230 MHz
- Supports DDC1 and DDC2B+ for Plug and Play monitors
- Game acceleration including support for Microsoft's DirectDraw†: double buffering, virtual sprites, transparent blit, masked blit, and context chaining
- Direct3D† texture lighting
- 2/4 MB of 83 MHz SGRAM on the motherboard

1.11.2 ATI Rage Pro 1X AGP (Optional)

The ATI Rage Pro 1X AGP supports motion video acceleration.

- Multistream video for video conferencing
- Filtered horizontal/vertical, up/down scaling enhances playback quality
- Enhanced line buffer allows vertical filtering of native MPEG-2 size (720 x 480) images
- DVD/MPEG-2 decode assist
- Filter circuitry that eliminates video artifacts caused by displaying interlaced video on noninterlaced displays
- Hardware mirroring for flipping video images in video conferencing systems
- Bi-directional bus mastering engine with planar YUV-to-packed format converter
- YUV-to-RGB color space converter with support for both packed and planar YUV:
  - YUV 4:2:2, YUV 4:1:0, and YUV 4:2:0
  - RGB 32, RGB 16/15, RGB 8, and monochrome

1.12 LAN Subsystem

The Intel® EtherExpress™ PRO/100 Wired for Management (WfM) PCI LAN subsystem is an Ethernet† LAN interface that provides both 10Base-T and 100Base-TX connectivity. Features include:

- 32-bit direct bus mastering on the PCI bus
- Shared memory structure in the host memory that copies data directly to/from host memory
- 10Base-T and 100Base-TX capability using a single RJ-45 connector with connection and activity status LEDs
- IEEE 802.3µ Auto-Negotiation for the fastest available connection
- Jumperless configuration; the LAN subsystem is completely software configurable

1.12.1 Intel® 82558 LAN Controller

The Intel® 82558 LAN Controller provides the following functions:

- CSMA/CD Protocol Engine
- PCI bus interface (Rev 2.1 compliant)
- DMA engine for movement of commands, status, and network data across the PCI bus
- Integrated physical layer interface, including:
  - — Complete functionality necessary for the 10Base-T and 100Base-TX interfaces; when in 10 Mbit/sec mode, the interface drives the cable directly
  - — A complete set of MII management registers for control and status reporting
  - — 802.3µ Auto-Negotiation for automatically establishing the best operating mode when connected to other 10Base-T or 100Base-TX devices
- Integrated power management features, including:
  - — Support for ACPI
  - — Support for Wake on LAN technology
- Digitally controlled adaptive equalizations and transmission

1.13 Wake on LAN Technology

Wake on LAN technology enables remote wakeup of the computer through a network. Wake on LAN technology requires a PCI add-in network interface card (NIC) with remote wakeup capabilities. The remote wakeup connector on the NIC must be connected to the onboard Wake on LAN technology connector. The NIC monitors network traffic at the Media Independent Interface (MII); upon detecting a Magic Packet†, the NIC asserts a wakeup signal that powers up the computer.

This feature is available on the riser. See Section 1.17 for the location and pinouts of the NLX edge connector.

⚠ CAUTION

For Wake on LAN, the +5 V standby line for the power supply must be capable of delivering +5 V ± 5% at 720 mA. Failure to provide adequate standby current when implementing Wake on LAN, can damage the power supply.

1.14 Hardware Monitor Subsystem

The hardware monitor subsystem provides low-cost instrumentation capabilities. The features of the hardware monitor subsystem include:

- Support for an optional chassis intrusion connector‡
- An integrated ambient temperature sensor
- Fan speed sensors (see Figure 4 for the location of fan connector on the motherboard)
- Power supply voltage monitoring to detect levels above or below acceptable values

When suggested ratings for temperature, fan speed, or voltage are exceeded, an interrupt is activated. The hardware monitor component connects to the SMBus.

1.15 Fan Speed Control

The motherboard includes two independent circuits for controlling various system cooling fans: one on the motherboard and the other on the riser.

1.15.1 Fan Header

The processor fan header (J1A1) on the motherboard is intended to drive a processor-mounted fan either full-speed or off, depending on the operating state of the system.

1.15.2 Fan Control Signal on the Riser

The fan control (FAN_CTL) signal is defined by the NLX specification as a means to control the speeds of fans connected to an NLX riser or power supply. The KU440EX motherboard is capable of driving FAN_CTL at different output levels, depending on the operating state of the system. Initially, two levels are defined for high and low fan speed operation. Based on the cooling needs and capabilities of a given system platform, the system OEM can redefine these output levels (by means of the SMBIOS table entries) to achieve a better balance of acoustic and thermal performance.

1.15.3 System Management Support

While the system is running an APM OS, the BIOS controls both fan circuits as shown in Table 1. With an ACPI OS, the voltage to both circuits is dependent on the system state, as shown in Table 2.

Table 1. Fan Speed Control under APM OS

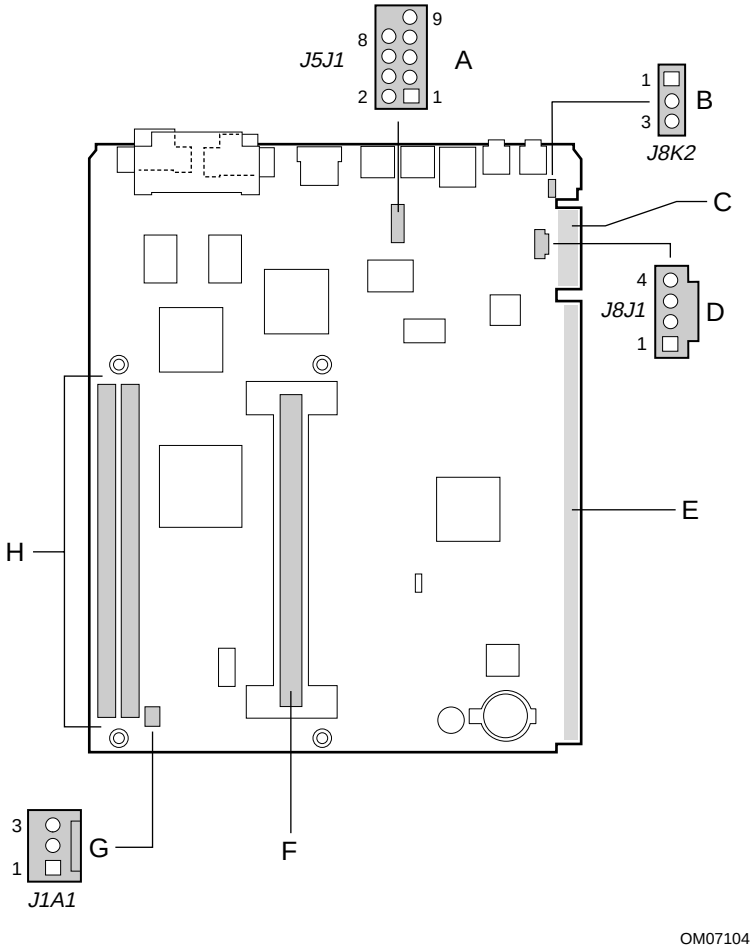
APM system states	Processor fan voltage	FAN_CTL signal to riser
Full on APM Enabled/Standby	+12 V (default)	OEM-definable “High speed” (default = +12 V)
APM Suspend off	0 V (default)	OEM-definable “Low speed” (default = 8 V)

Table 2. Fan Speed Control under ACPI OS

ACPI System States	Processor Fan Voltage	FAN_CTL Signal to Riser
S0	+12V	+12 V
S1	OS Control	ACPI software/Operating System
S2	No support	No support
S3	No support	No support
S4	Future Upgrade (+0 V)	(+0 V)
S5	0 V	+0 V

1.16 Motherboard Connectors

Figure 4 shows the location of the motherboard connectors.



A	COM2 header	E	NLX edge connector
B	Microphone routing jumper	F	Slot 1 connector
C	NLX edge connector (supplemental)	G	Processor fan connector
D	CD-ROM audio connector (2mm)	H	DIMM sockets

Figure 4. Motherboard Connectors

Table 3. Serial Port B Header (J5J1)

Pin	Signal Name
1	DCD
2	DSR
3	Serial In#
4	RTS
5	Serial Out#
6	CTS
7	DTR
8	RI (Ring in)
9	Ground
10	Key

Table 4. Microphone Routing Jumper (J8K2)

Settings	Configuration
1-2	Front panel Mic In
2-3	Motherboard Mic In

Table 5. CD Audio (J8J1)

Pin	Signal Name
1	CD_Left
2	Ground
3	Ground
4	CD_Right

Table 6. Fan Connector (J1A1)

Pin	Signal Name
1	Ground
2	12 V/0 V
3	FAN_SEN

1.16.1 Power Supply Connector‡

When used with an NLX-compliant power supply that supports remote power on/off, the motherboard can turn off the system power through software control. See Section 6.2 for information about the NLX specification.

To enable soft-off control in software, advanced power management must be enabled in the Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

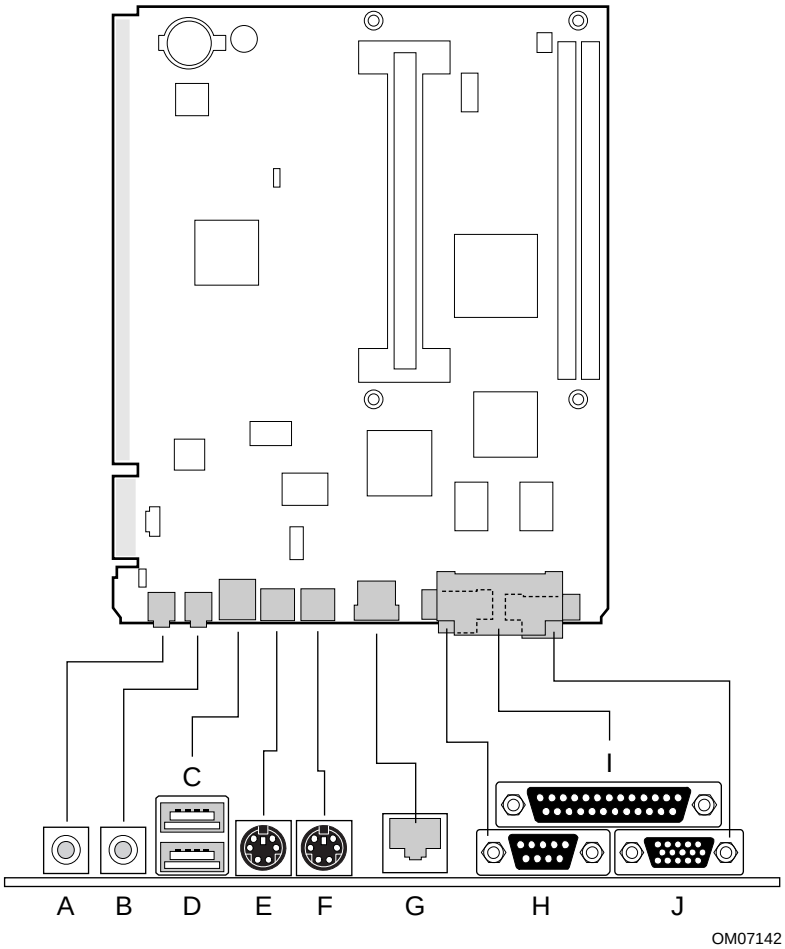
Table 7. Power Supply Connector

Pin	Signal Name
1	+3.3 V
2	+3.3 V
3	Ground
4	+5 V
5	Ground
6	+5 V
7	Ground
8	PWRGD (Power Good)
9	+5 V (STANDBY)
10	+12 V
11	+3.3 V
12	-12 V
13	Ground
14	PS-ON# (power supply remote on/off control)
15	Ground
16	Ground
17	Ground
18	-5 V
19	+5 V
20	+5 V

1.16.2 Back Panel Connectors

Figure 5 shows the location of the back panel I/O connectors, which include:

- External audio jacks: Mic In and Line Out
- Two USB connectors (stacked)
- PS/2-keyboard and mouse connectors
- RJ-45 LAN connector
- One serial port
- One video port
- One parallel port



A	Mic In	F	PS/2 Keyboard/Mouse
B	Line Out	G	RJ-45 LAN
C	USB Port 1	H	Serial Port A
D	USB Port 0	I	Parallel Port
E	PS/2 Keyboard/Mouse	J	Video

Figure 5. Back Panel I/O Connectors

Table 8. Audio Mic In Connector (J8K1)

Pin	Signal Name
Sleeve	Ground
Tip	Mono In
Ring	Electret Bias Voltage

Table 9. Audio Line Out Connector (J7K1)

Pin	Signal Name
Sleeve	Ground
Tip	Audio Left Out
Ring	Audio Right Out

Table 10. Stacked USB Connectors (J6K2)

Pin	Signal Name
1	+5 V (fused)
2	USBP0# [USBP1#]
3	USBP0 [USBP1]
4	Ground

Signal names in brackets ([ ]) are for USB Port 1.

Table 11. PS/2 Keyboard/Mouse Connectors (J5K1, J6K1)

Pin	Signal Name
1	Data
2	No connect
3	Ground
4	+5 V (fused)
5	Clock
6	No connect

Table 12. RJ-45 LAN Connector (J4K1)

Pin	Signal Name
1	Tx+
2	Tx-
3	Rx+
4	GND
5	GND
6	Rx-
7	GND
8	GND

Table 13. Serial Port A Connector (J3K1)

Pin	Signal Name
1	DCD
2	Serial In#
3	Serial Out#
4	DTR#
5	Ground
6	DSR
7	RTS
8	CTS
9	RI

Table 14. Video Connector (J1K1)

Pin	Signal Name
1	RED
2	GREEN
3	BLUE
4	AC GROUND
5	Ground
6	Ground
7	Ground
8	Ground
9	Fused VCC
10	Ground
11	AC GROUND
12	MONID1
13	HSYNC
14	VSYNC
15	MONID2

Table 15. Parallel Port Connector (J2K1)

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data bit 0	15	Fault#
3	Data bit 1	16	INIT#
4	Data bit 2	17	SLCT IN#
5	Data bit 3	18	Ground
6	Data bit 4	19	Ground
7	Data bit 5	20	Ground
8	Data bit 6	21	Ground
9	Data bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Error	25	Ground
13	Select		

1.17 NLX Card Edge Connector

The NLX riser connector on the motherboard consists of a 340 (2 x 170) position and a supplemental 26 (2 x 13) position gold finger contact. All edge connector pin definitions are defined in the NLX specification, version 1.2.

According to the NLX specification, the motherboard edge connector provides the following:

- PCI signals (the motherboard supports up to four PCI devices)
- ISA signals
- Two IDE channels
- One diskette drive interface
- Infrared signals
- Miscellaneous front panel signals
- Power connection for the motherboard

See Section 6.2 for information about the NLX Specification.

Table 16, Table 17, and Table 18 specify the pinouts located on the primary connector; Table 19 specifies the pinouts located on the supplemental connector.

Table 16. PCI Segment, Riser Interconnect

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A1	-12V	PWR	NA	NA	B1	PCSPKR_RT	AUDIO	O	NA
A2	REQ4#	PCI	I	RIS	B2	+12V	PWR	NA	NA
A3	+12V	PWR	NA	NA	B3	PCSPKR_LFT	AUDIO	O	NA
A4	GNT4#	PCI	O	RIS	B4	+12V	PWR	NA	NA
A5	3.3VDC	PWR	NA	NA	B5	PCICLK0	PCI	O	MB
A6	PCIINT3#	PCI	I	RIS	B6	GND	PWR	NA	NA
A7	3.3VDC	PWR	NA	NA	B7	PCICLK1	PCI	O	MB
A8	PCIINT0#	PCI	I	RIS	B8	SER_IRQ	MISC	I/O	MB
A9	PCIINT1#	PCI	I	RIS	B9	PCIINT2#	PCI	I	RIS
A10	PCICLK2	PCI	O	MB	B10	3.3VDC	PWR	NA	NA
A11	3.3VDC	PWR	NA	NA	B11	PCICLK3	PCI	O	MB
A12	PCI_RST#	PCI	O	MB	B12	GND	PWR	NA	NA
A13	GNT0#	PCI	O	RIS	B13	GNT3#	PCI	O	RIS
A14	PCICLK4	PCI	O	MB	B14	3.3VDC	PWR	NA	NA
A15	GND	PWR	NA	NA	B15	GNT2#	PCI	O	RIS
A16	GNT1#	PCI	O	RIS	B16	AD[31]	PCI	I/O	RIS
A17	3.3VDC	PWR	NA	NA	B17	REQ0#	PCI	I	RIS

continued

Table 16. PCI Segment, Riser Interconnect (continued)

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A18	REQ2#	PCI	I	RIS	B18	GND	PWR	NA	NA
A19	REQ3#	PCI	I	RIS	B19	AD[29]	PCI	I/O	RIS
A20	AD[30]	PCI	I/O	RIS	B20	AD[28]	PCI	I/O	RIS
A21	GND	PWR	NA	NA	B21	AD[26]	PCI	I/O	RIS
A22	AD[25]	PCI	I/O	RIS	B22	3.3VDC	PWR	NA	NA
A23	REQ1#	PCI	I	RIS	B23	AD[24]	PCI	I/O	RIS
A24	AD[27]	PCI	I/O	RIS	B24	C/BE[3]#	PCI	I/O	RIS
A25	3.3VDC	PWR	NA	NA	B25	AD[22]	PCI	I/O	RIS
A26	AD[23]	PCI	I/O	RIS	B26	GND	PWR	NA	NA
A27	AD[20]	PCI	I/O	RIS	B27	AD[21]	PCI	I/O	RIS
A28	AD[18]	PCI	I/O	RIS	B28	AD[19]	PCI	I/O	RIS
A29	GND	PWR	NA	NA	B29	AD[16]	PCI	I/O	RIS
A30	AD[17]	PCI	I/O	RIS	B30	3.3VDC	PWR	NA	NA
A31	IRDY#	PCI	I/O	RIS	B31	C/BE[2]#	PCI	I/O	RIS
A32	DEVSEL#	PCI	I/O	RIS	B32	FRAME#	PCI	I/O	RIS
A33	3.3VDC	PWR	NA	NA	B33	TRDY#	PCI	I/O	RIS
A34	STOP#	PCI	I/O	RIS	B34	GND	PWR	NA	NA
A35	PERR#	PCI	I/O	RIS	B35	SDONE	PCI	I/O	RIS
A36	SERR#	PCI	I/O	RIS	B36	LOCK#	PCI	I/O	RIS
A37	GND	PWR	NA	NA	B37	SBO#	PCI	I/O	RIS
A38	C/BE[1]#	PCI	I/O	RIS	B38	3.3VDC	PWR	NA	NA
A39	AD[13]	PCI`	I/O	RIS	B39	AD[15]	PCI	I/O	RIS
A40	AD[10]	PCI	I/O	RIS	B40	PAR	PCI	I/O	RIS
A41	GND	PWR	NA	NA	B41	AD[14]	PCI	I/O	RIS
A42	C/BE[0]#	PCI	I/O	RIS	B42	GND	PWR	NA	NA
A43	AD[00]	PCI	I/O	RIS	B43	AD[11]	PCI	I/O	RIS
A44	AD[06]	PCI	I/O	RIS	B44	AD[12]	PCI	I/O	RIS
A45	3.3VDC	PWR	NA	NA	B45	AD[09]	PCI	I/O	RIS
A46	AD[05]	PCI	I/O	RIS	B46	3.3VDC	PWR	NA	NA
A47	AD[01]	PCI	I/O	RIS	B47	AD[08]	PCI	I/O	RIS
A48	AD[03]	PCI	I/O	RIS	B48	AD[07]	PCI	I/O	RIS
A49	GND	PWR	NA	NA	B49	AD[04]	PCI	I/O	RIS
A50	AD[02]	PCI	I/O	RIS	B50	GND	PWR	NA	NA
A51	5VDC	PWR	NA	NA	B51	PCI_PM#	PCI	I/O	MB

I/O Column Definitions Relative to Motherboard
O = Output from motherboard to riser
I = Input from riser to motherboard
Termination Column Definitions:
MB = Termination/Pullup/Pulldown/debounce is on motherboard
RIS = Termination/Pullup/Pulldown is on riser card
N/A = Not on motherboard or riser

Table 17. ISA Segment, Riser Interconnect

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A52	RSTDRV	ISA	O	MB	B52	5VDC	PWR	NA	NA
A53	IOCHK#	ISA	I	MB	B53	IRQ9	ISA	O	MB
A54	SD[6]	ISA	I/O	MB	B54	DRQ2	ISA	I	MB
A55	SD[7]	ISA	I/O	MB	B55	SD[3]	ISA	I/O	MB
A56	SD[4]	ISA	I/O	MB	B56	0WS#	ISA	I	MB
A57	5VDC	PWR	NA	NA	B57	SD[1]	ISA	I/O	MB
A58	SD[2]	ISA	I/O	MB	B58	AEN	ISA	O	MB
A59	SD[5]	ISA	I/O	MB	B59	IOCHRDY	ISA	I	MB
A60	SD[0]	ISA	I/O	MB	B60	SA[18]	ISA	I/O	MB
A61	SMEMW#	ISA	O	MB	B61	SMEMR#	ISA	O	MB
A62	SA[19]	ISA	I/O	MB	B62	SA[16]	ISA	I/O	MB
A63	IOW#	ISA	I/O	MB	B63	IOR#	ISA	I/O	MB
A64	SA[17]	ISA	I/O	MB	B64	DRQ3	ISA	I	MB
A65	GND	PWR	NA	NA	B65	SA[15]	ISA	I/O	MB
A66	DACK#3	ISA	O	MB	B66	GND	PWR	NA	NA
A67	SA[14]	ISA	I/O	MB	B67	SA[13]	ISA	I/O	MB
A68	DACK1#	ISA	O	MB	B68	5VDC	PWR	NA	NA
A69	DRQ1	ISA	I	MB	B69	REFRESH#	ISA	I/O	MB
A70	SA[12]	ISA	I/O	MB	B70	SA[11]	ISA	I/O	MB
A71	SYSCLK	ISA	O	MB	B71	SA[10]	ISA	I/O	MB
A72	SA[9]	ISA	I/O	MB	B72	IRQ7	ISA	I	MB
A73	5VDC	PWR	NA	NA	B73	IRQ6	ISA	I	MB
A74	IRQ5	ISA	I	MB	B74	SA[8]	ISA	I/O	MB
A75	SA[7]	ISA	I/O	MB	B75	SA[6]	ISA	I/O	MB
A76	IRQ3	ISA	I	MB	B76	DACK2#	ISA	O	MB
A77	IRQ4	ISA	I	MB	B77	SA[4]	ISA	I/O	MB
A78	SA[5]	ISA	I/O	MB	B78	GND	PWR	NA	NA
A79	TC	ISA	O	MB	B79	SA[3]	ISA	I/O	MB
A80	BALE	ISA	O	MB	B80	SA[2]	ISA	I/O	MB
A81	GND	PWR	NA	NA	B81	SA[1]	ISA	I/O	MB
A82	OSC	ISA	O	MB	B82	SA[0]	ISA	I/O	MB
A83	IOCS16#	ISA	I	MB	B83	SBHE#	ISA	I/O	MB
A84	MEMCS16#	ISA	I	MB	B84	LA[23]	ISA	I/O	MB
A85	IRQ11	ISA	I	MB	B85	LA[22]	ISA	I/O	MB
A86	IRQ10	ISA	I	MB	B86	LA[21]	ISA	I/O	MB

continued

Table 17. ISA Segment, Riser Interconnect (continued)

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A87	IRQ15	ISA	I	MB	B87	LA[20]	ISA	I/O	MB
A88	IRQ12	ISA	I	MB	B88	LA[19]	ISA	I/O	MB
A89	GND	PWR	NA	NA	B89	LA[18]	ISA	I/O	MB
A90	IRQ14	ISA	I	MB	B90	LA[17]	ISA	I/O	MB
A91	DRQ0	ISA	I	MB	B91	DACK0#	ISA	O	MB
A92	MEMR#	ISA	I/O	MB	B92	DACK5#	ISA	O	MB
A93	MEMW#	ISA	I/O	MB	B93	SD[8]	ISA	I/O	MB
A94	SD[9]	ISA	I/O	MB	B94	DACK6#	ISA	O	MB
A95	DRQ5	ISA	I	MB	B95	SD[10]	ISA	I/O	MB
A96	DRQ6	ISA	I	MB	B96	5VDC	PWR	NA	NA
A97	5VDC	PWR	NA	NA	B97	SD[11]	ISA	I/O	MB
A98	SD[12]	ISA	I/O	MB	B98	DRQ7	ISA	I	MB
A99	DACK7#	ISA	O	MB	B99	SD[13]	ISA	I/O	MB
A100	SD[14]	ISA	I/O	MB	B100	SD[15]	ISA	I/O	MB
A101	MASTER#	ISA	I	MB	B101	GND	PWR	NA	NA

I/O Column Definitions Relative to Motherboard
O = Output from motherboard to riser
I = Input from riser to motherboard
Termination Column Definitions:
MB = Termination/Pullup/Pulldown/debounce is on motherboard
RIS = Termination/Pullup/Pulldown is on riser card
N/A = Not on motherboard or riser

Table 18. IDE, Floppy, and Front Panel Section, Riser Interconnect

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A102	IDEA_DD8	IDE	I/O	MB	B102	GND	PWR	NA	NA
A103	IDEA_RESET#	IDE	O	MB	B103	IDEA_DD7	IDE	I/O	MB
A104	IDEA_DD9	IDE	I/O	MB	B104	IDEA_DD6	IDE	I/O	MB
A105	5VDC	PWR	NA	NA	B105	IDEA_DD5	IDE	I/O	MB
A106	IDEA_DD4	IDE	I/O	MB	B106	IDEA_DD11	IDE	I/O	MB
A107	IDEA_DD10	IDE	I/O	MB	B107	IDEA_DD12	IDE	I/O	MB
A108	IDEA_DD3	IDE	I/O	MB	B108	GND	PWR	NA	NA
A109	IDEA_DD13	IDE	I/O	MB	B109	IDEA_DD14	IDE	I/O	MB
A110	IDEA_DD1	IDE	I/O	MB	B110	IDEA_DD2	IDE	I/O	MB
A111	GND	PWR	NA	NA	B111	IDEA_DD0	IDE	I/O	MB
A112	IDEA_DIOW#	IDE	O	MB	B112	IDEA_DD15	IDE	I/O	MB
A113	IDEA_DMARQ	IDE	I	MB	B113	IDEA_DIOR#	IDE	O	MB

continued

Table 18. IDE, Floppy, and Front Panel Section, Riser Interconnect (continued)

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A114	IDEA_IORDY	IDE	I	MB	B114	IDEA_CSEL	IDE	O	MB
A115	IDEA_DMACK#	IDE	O	MB	B115	IDEA_INTRQ	IDE	I	MB
A116	RESERVED	RES	NA	NA	B116	5VDC	PWR	NA	NA
A117	IDEA_DA2	IDE	O	MB	B117	IDEA_DA1	IDE	O	MB
A118	IDEA_CS0#	IDE	O	MB	B118	IDEA_DA0	IDE	O	MB
A119	5VDC	PWR	NA	NA	B119	IDEA_CS1#	IDE	O	MB
A120	IDEA_DASP#	IDE	I	RIS	B120	IDEB_DD8	IDE	I/O	MB
A121	IDEB_RESET#	IDE	O	MB	B121	IDEB_DD7	IDE	I/O	MB
A122	IDEB_DD9	IDE	I/O	MB	B122	GND	PWR	NA	NA
A123	IDEB_DD6	IDE	I/O	MB	B123	IDEB_DD10	IDE	I/O	MB
A124	IDEB_DD5	IDE	I/O	MB	B124	5VDC	PWR	NA	NA
A125	IDEB_DD11	IDE	I/O	MB	B125	IDEB_DD4	IDE	I/O	MB
A126	IDEB_DD12	IDE	I/O	MB	B126	IDEB_DD3	IDE	I/O	MB
A127	GND	PWR	NA	NA	B127	IDEB_DD13	IDE	I/O	MB
A128	IDEB_DD2	IDE	I/O	MB	B128	IDEB_DD14	IDE	I/O	MB
A129	IDEB_DD15	IDE	I/O	MB	B129	IDEB_DD1	IDE	I/O	MB
A130	IDEB_DIOW#	IDE	I/O	MB	B130	IDEB_DD0	IDE	I/O	MB
A131	IDEB_DMARQ	IDE	I	MB	B131	IDEB_DIOR#	IDE	O	MB
A132	IDEB_IORDY	IDE	I	MB	B132	IDEB_CSEL	IDE	O	MB
A133	GND	PWR	NA	NA	B133	IDEB_INTRQ	IDE	I	MB
A134	IDEB_DMACK#	IDE	O	MB	B134	IDEB_DA1	IDE	O	MB
A135	RESERVED	RES	NA	NA	B135	IDEB_DA2	IDE	O	MB
A136	IDEB_DA0	IDE	O	MB	B136	IDEB_CS1#	IDE	O	MB
A137	IDEB_CS0#	IDE	O	MB	B137	IDEB_DASP#	IDE	I	RIS
A138	DRV2#	FLOPPY	GND	NA	B138	GND	PWR	NA	NA
A139	5VDC	PWR	NA	NA	B139	DRATE0	FLOPPY	O	NA
A140	RESERVED	RES	NA	NA	B140	FDS1#	FLOPPY	O	NA
A141	DENSEL	FLOPPY	O	NA	B141	FDS0#	FLOPPY	O	NA
A142	FDME0#	FLOPPY	O	NA	B142	DIR#	FLOPPY	O	NA
A143	INDX#	FLOPPY	I	RIS	B143	MSEN1	FLOPPY	I	NA
A144	FDME1#	FLOPPY	O	NA	B144	GND	PWR	NA	NA
A145	GND	PWR	NA	NA	B145	WRDATA#	FLOPPY	O	NA
A146	WE#	FLOPPY	O	NA	B146	TRK0#	FLOPPY	I	RIS
A147	STEP#	FLOPPY	O	NA	B147	MSEN0	FLOPPY	I	NA
A148	WP#	FLOPPY	I	RIS	B148	RDDATA#	FLOPPY	I	RIS

continued

Table 18. IDE, Floppy, and Front Panel Section, Riser Interconnect (continued)

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A149	HDSEL#	FLOPPY	O	NA	B149	DSKCHG#	FLOPPY	I	RIS
A150	SDA	MISC	I/O	MB	B150	GND	PWR	NA	NA
A151	SCL	MISC	O	MB	B151	IRSL0	MISC	I/O	NA
A152	FAN_TACH1	MISC	I	NA	B152	IRSL1	MISC	I/O	NA
A153	FAN_TACH2	MISC	I	NA	B153	IRSL2	MISC	I/O	NA
A154	FAN_TACH3	MISC	I	NA	B154	IRTX	MISC	I/O	NA
A155	FAN_CTL	MISC	I	NA	B155	IRRX	MISC	I/O	RIS
A156	5VDC	PWR	NA	NA	B156	FP_SLEEP	MISC	I	MB
A157	USB1/3_N	MISC	I/O	RIS	B157	FP_RST#	MISC	I	MB
A158	USB1/3_P	MISC	I/O	RIS	B158	GND	PWR	NA	NA
A159	USB1/3_OC#	MISC	I	RIS	B159	PWRLED#	MISC	O	RIS
A160	USB2/4_N	MISC	I/O	RIS	B160	PWOK	PWR	I	NA
A161	USB2/4_P	MISC	I/O	RIS	B161	SOFT_ON/OFF#	PWR	I	MB
A162	USB2/4_OC#	MISC	I	RIS	B162	PS_ON#	PWR	O	NA
A163	GND	PWR	NA	NA	B163	LAN_WAKE	MISC	I	MB
A164	VBAT	MISC	O	RIS	B164	LAN_ACTVY_ LED#	MISC	O	NA
A165	TAMP_DET#	MISC	I	MB	B165	MDM_WAKE#	MISC	I	MB
A166	MSG_WAIT_ LED#	MISC	O	RIS	B166	1394_PWR	PWR	I	NA
A167	1394_GND	PWR	O	NA	B167	RESERVED	RES	NA	NA
A168	RESERVED	RES	NA	NA	B168	RESERVED	RES	NA	NA
A169	5V (standby)	PWR	I	NA	B169	RESERVED	RES	NA	NA
A170	3.3VSENSE	PWR	O	NA	B170	-5V	PWR	NA	NA

I/O Column Definitions Relative to Motherboard
O = Output from motherboard to riser
I = Input from riser to motherboard
Termination Column Definitions:
MB = Termination/Pullup/Pulldown/debounce is on motherboard
RIS = Termination/Pullup/Pulldown is on riser card
N/A = Not on motherboard or riser

Table 19. Signals, NLX Riser with Supplemental Connector

Pin	Signal Name	Type	I/O *	Description	Signal Type
X1	CD_IN_LT	AUDIO	I	CD-ROM Line-in left.	Analog 1 V RMS
X2	AGND	PWR	NA	Low pass filtered ground for audio circuitry on the riser.	NA
X3	MIC_IN	AUDIO	I	Pre-amplified microphone input. Pre-amp circuitry to reside on riser or in microphone.	Analog 1 V RMS
X4	LINE_OUT_LT	AUDIO	O	Analog Line-out left.	Analog 1 V RMS
X5	FP_SPKR_EN	AUDIO	I	This signal indicates if headphones have been plugged into the front panel LINE-OUT jack. The signal is connected to one of the wipers on the audio jack and is HIGH when the headphones are plugged into the front audio jack and LOW when they are not. The signal is pulled low through a pull-down on the motherboard (Typically 100K).	TTL
X6	VOL_DN# **	AUDIO	I	Connects to Volume Down switch on front panel, appropriate pull-up resistor on motherboard. The motherboard provides debounce protection and a pull-up resistor.	TTL
X7	GND	PWR	NA	Ground	NA
X8	SMI# **	SYS	I	System Management Interrupt that is an input to the motherboard.	open drain
X9	RESERVED	RES	NA	Reserved	NA
X10	RESERVED	RES	NA	Reserved	NA
X11	RESERVED	RES	NA	Reserved	NA
X12	AGND	PWR	NA	Low pass filtered ground for audio circuitry on the riser.	NA
X13	MODEM_MIC	AUDIO	O	Pre-amplified microphone mono output signal from motherboard to telephony device.	Analog 1 V RMS
Y1	CD_IN_RT	AUDIO	I	CD-ROM Line-in right.	Analog 1 V RMS
Y2	CD_IN_GND	PWR	I	Isolated CD-ROM ground.	NA
Y3	AVCC	PWR	O	Clean power from the motherboard to audio circuitry on the NLX riser; could be an isolated power source; 1.5 Ampere max. Limitation because of the connector / gold finger limitation.	5-9 V DC
Y4	LINE_OUT_RT	AUDIO	O	Analog Line-out right.	Analog 1 V RMS

continued

Table 19. Signals, NLX Riser with Supplemental Connector (continued)

Pin	Signal Name	Type	I/O *	Description	Signal Type
Y5	FP_MIC_EN **	AUDIO	I	This signal indicates if a microphone has been plugged into the front panel MIC_IN jack. The signal is connected to a wiper on the MIC_IN jack and is LOW when the microphone is plugged in and HIGH when it is not. The signal is pulled LOW through a pull down on the motherboard (Typically 100K).	TTL
Y6	VOL_UP# **	AUDIO	I	Connects to Volume Up switch on front panel, appropriate pull-up resistor on motherboard. The motherboard provides debounce protection and a pull-up resistor.	TTL
Y7	AC_RST# **	AC'97	O	AC'97 master H/W reset.	TTL
Y8	AC_SD_IN **	AC'97	I	Serial, time division, multiplexed, AC'97 input stream to the motherboard from the codec on the riser (output from the codec).	TTL
Y9	GROUND	PWR	NA	Digital (main motherboard) ground plane.	NA
Y10	AC_SD_OUT **	AC'97	O	A84	MEMCS16#
Y11	AC_SYNC **	AC'97	O	A85	IRQ11
Y12	AC_BIT_CLK **	AC'97	I	A86	IRQ10
Y13	MODEM_SPKR	AUDIO	O	Analog mono output signal from telephony device to motherboard.	Analog 1 V RMS

* I/O column: relative to motherboard
"O" = output, from motherboard to riser
"I" = input, from riser to motherboard.

** These signals are not supported.

1.18 Jumper Settings

The motherboard has a single, 3-pin configuration jumper block at location (J6C1). Figure 6 shows the location of the configuration jumper block. Table 20 describes the jumper settings for the three modes.

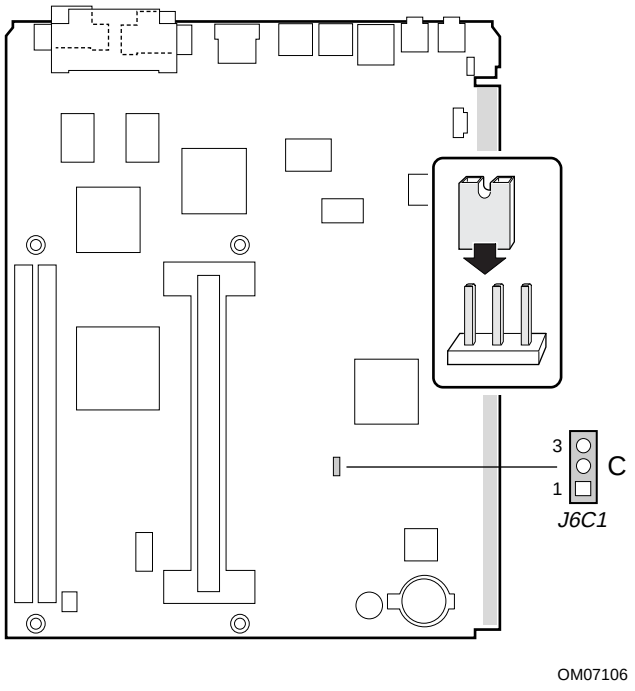


Figure 6. Location of the Configuration Jumper Block

Table 20. Configuration Jumper Settings

Function	Jumper J6C1	Configuration
Normal	1-2	The BIOS uses current configuration information and passwords for booting.
Configure	2-3	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	none	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

⚠ CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing the jumper.

1.19 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is for estimating repair rates and spare parts requirements.

MTBF data is calculated from predicted data @ 55 °C.

The MTBF prediction for the motherboard is 136,338 hours.

1.20 Environmental Specifications

Table 21. Environmental Specifications

Parameter	Specification		
Temperature			
Nonoperating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 G trapezoidal waveform		
	Velocity change of 170 inches/sec		
Packaged	Half sine 2 millisecond		
	Product Weight (lbs)	**Free Fall (inches)**	**Velocity Change (inches/sec)**
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz : 0.01g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz : 0.02g² Hz (flat)		
Packaged	10 Hz to 40 Hz : 0.015g² Hz (flat)		
	40 Hz to 500 Hz : 0.015g² Hz sloping down to 0.00015 g² Hz		
Humidity			
Non-operating	95% RH at 30° C non-condensing		

1.21 Power Consumption

Table 22 lists the power usage for a computer that contains a motherboard with a 266 MHz Celeron processor, 32 MB RAM, 0 KB cache, 3.5-inch floppy drive, 2.1 GB IDE hard drive, 16X IDE CD-ROM and integrated Rage IIC with 4 MB of video memory. This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 95 desktop mode are measured at 65K colors and 75 Hz refresh rate. AC watts are measured with a typical 145 W supply, nominal input voltage and frequency, and with a true RMS wattmeter at the line input.

Table 22. Power Usage

		DC (amps) at:				
Mode	**AC (watts)**	**+3.3 V**	**+5 V**	**+12 V**	**-12 V**	**+5 V SB**
DOS prompt, APM disabled	49.0	1.78 A	2.92 A	.444 A	.032 A	.38 A
Windows 95 desktop, APM disabled	49.5	1.63 A	2.88 A	.452 A	.032 A	.38 A
Windows 95 desktop, APM enabled, in System Management Mode (SMM)	35.6	2.176 A	2.488 A	.302 A	.032 A	.38 A

For typical configurations, the motherboard is designed to operate with a 90 to 200 W power supply. A higher-wattage power supply should be used for heavily-loaded configurations. The power supply must comply with the following recommendations found in the indicated sections of the NLX form factor specification (see Section 6.2).

- The potential relation between 3.3VDC and +5VDC power rails
- The current capability of the +5V (standby) line
- All timing parameters
- All voltage tolerances

1.22 Thermal Considerations

Table 23 lists maximum component case temperatures for motherboard components that could be sensitive to thermal changes. Case temperatures could be affected by factors such as the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the motherboard.

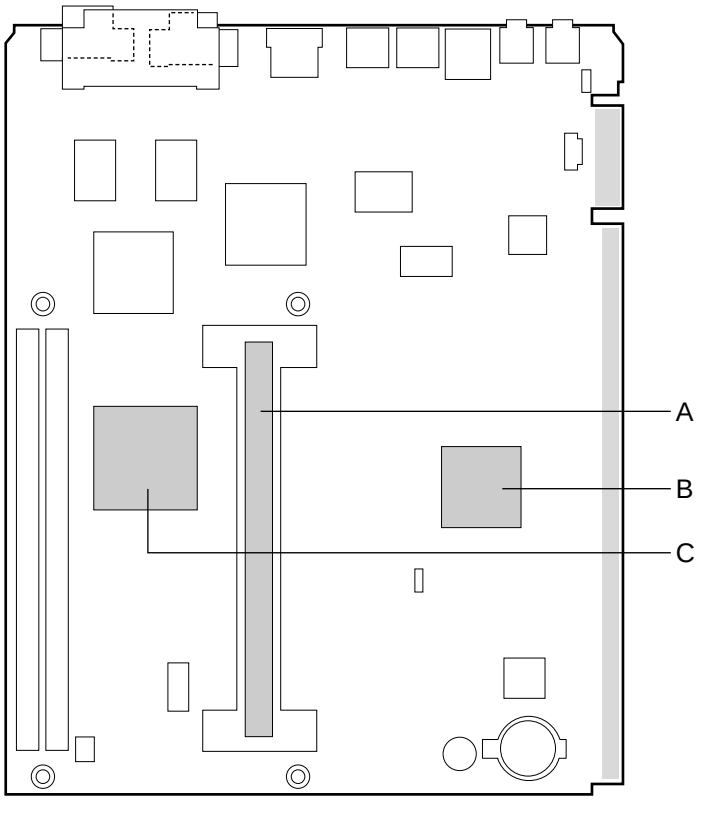
⚠ CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5 °C to 10 °C might cause components to exceed their maximum case temperature. For information about the maximum operating temperature, see the environmental specifications in Section 1.20.

Table 23. Thermal Considerations for Components

Component	Maximum Temperature		Motherboard Location
Pentium II processor	233 MHz	**75°C (thermal plate)**	J3D1 (Slot 1 connector)
	266 MHz	**75°C (thermal plate)**	
	300 MHz	**72.3°C (thermal plate)**	
	333 MHz	**65°C (thermal plate)**	
Celeron processor	266 MHz	**85 °C (case)**	J3D1 (Slot 1 connector)

Figure 7 shows motherboard components that may be sensitive to thermal changes.



A Processor (in Slot 1 connector)
B Intel 82443EX
C Intel 82371EB

Figure 7. Thermally-Sensitive Components

Table 24 shows the DC power requirements for systems in either Sleep or Normal operating modes. Power consumption is independent of the operating system used and other variables.

Table 24. Processor Fan Voltage (J1A1)

Mode	Voltage
Sleep	0
Normal	12

1.23 Regulatory Compliance

This motherboard complies with the following safety and EMC regulations when correctly installed in a compatible host system.

Table 25. Safety Regulations

Regulation	Title
UL 1950 - CSA 950-95, 3rd edition, Dated 07-28-95	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA & Canada)
EN 60 950, 2nd Edition, 1992 (with Amendments 1, 2 & 3)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)
IEC 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60 950. (Norway, Sweden, Denmark & Finland)

Table 26. EMC Regulations

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 & 15, Subpart B, pertaining to unintentional radiators. (USA)
CISPR 22, 2nd Edition, 1993	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
EN 55 022, 1995	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN 50 082-1 (1992)	Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)
VCCI Class B (ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
ICES-003, Issue 2	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)

This motherboard has the following product certification markings:

- European CE Marking: Consists of a marking on the board and shipping container.
- UL Recognition Mark: Consists of the UL File No. E139761 on the component side of the board and the PB No. on the solder side of the board. Board material flammability is 94V-1 or -0.
- Each board will be marked with an FCC Declaration of Conformity.
- Canadian Compliance: Consists of small c followed by a stylized backward UR on component side of the board.

2 Motherboard Resources

2.1 Memory Map

Table 27. Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 292144 K	100000 - 10000000	256 MB	Extended memory
896 K - 1024 K	E8000 - FFFFF	96 KB	System BIOS
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to ISA and PCI buses)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
0 K - 640 K	00000 - 9FFFF	640 KB	Conventional memory

2.2 DMA Channels

Table 28. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Audio
1	8- or 16-bits	Audio / parallel port
2	8- or 16-bits	Floppy drive
3	8- or 16-bits	Parallel port (for ECP)/audio
4		Reserved - cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.3 I/O Map

Table 29. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	DMA controller 1
0020 - 0021	2 bytes	Interrupt controller 1
002E - 002F	2 bytes	Super I/O controller configuration registers
0040 - 0043	4 bytes	Counter/Timer 1
0048 - 004B	4 bytes	Counter/Timer 2
0060	1 byte	Keyboard controller
0061	1 byte	NMI, speaker control
0064	1 byte	Keyboard controller
0070 - 0071	2 bytes	Real time clock controller
0080 - 008F	16 bytes	DMA page registers
00A0 - 00A1	2 bytes	Interrupt controller 2
00B2 - 00B3	2 bytes	APM control
00C0 - 00DE	31 bytes	DMA controller 2
00F0 - 00FF	16 bytes	Numeric processor
0120 - 0127	8 bytes	Audio controller
0170 - 0177	8 bytes	Secondary IDE controller
01F0 - 01F7	8 bytes	Primary IDE controller
0200 - 0207	8 bytes	Audio / game port / joy stick
0220 - 022F	16 bytes	Audio (Sound Blaster compatible)
0228 - 022F	8 bytes	LPT3
0274 - 0277	4 bytes	I/O read data port for ISA Plug and Play enumerator
0278 - 027F	8 bytes	LPT2
0330 - 0331	2 bytes	MPU-401 (MIDI)
0376 - 0377	2 bytes	Secondary IDE controller
0378 - 037F	8 bytes	LPT1
0388- 038D	6 bytes	AdLib† (FM synthesizer)
03B0 - 03BB	12 bytes	Video (monochrome)
03C0 - 03DF	32 bytes	Video (VGA†)
03F0 - 03F5, 03F7	7 bytes	Floppy controller
03F6	1 byte	Primary IDE controller
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0530 - 0537	8 bytes	Windows Sound System
LPT*n* + 400h	8 bytes	ECP port, LPT*n* base address + 400h
0CF8 - 0CFF*	8 bytes	PCI configuration registers
0CF9**	1 byte	Turbo and reset control register
7000 - 700C 8000 - 8037	13 bytes 55 bytes	SMBus I/O Register Power Management I/O Registers

* DWORD access only

** Byte access only

2.4 PCI Configuration Space Map

Table 30. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel® 82443EX (PAC)
00	01	00	Intel 82443EX (PAC) A.G.P. bus
00	07	00	Intel 82371EB (PIIX4E**)** PCI/ISA bridge
00	07	01	Intel 82371EB (PIIX4E) IDE bus master
00	07	02	Intel 82371EB (PIIX4E) USB
00	07	03	Intel 82371EB (PIIX4E) power management
00	06	00	Intel 83558 Ethernet controller (if present)
01	00	00	ATI Rage II C
00	12‡	00	PCI expansion slot 1‡
00	14‡	00	PCI expansion slot 2‡

2.5 Interrupts

Table 31. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard controller
2	Reserved, cascade interrupt from slave PIC
3	COM2 (User available if COM2 is not present)
4	COM1*
5	LPT2 (Plug and Play option) / audio / user available
6	Diskette Drive controller
7	LPT1*
8	Real time clock
9	Reserved
10	USB/User available
11	Windows Sound System* / user available
12	PS/2 mouse port (if present, else user available)
13	Reserved, numeric processor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ‡

2.6 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI expansion slots‡ and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX4E PCI-to-ISA bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and therefore share the same interrupt. Table 32 lists the PIRQ signals and shows how the signals are connected to the PCI expansion slots‡ and to onboard PCI interrupt sources.

Table 32. PCI Interrupt Routing Map

PIIX4 PIRQ Signal	First PCI Expansion Slot‡	Second PCI Expansion Slot‡	Third PCI Expansion Slot‡	Onboard Video	USB	Ethernet LAN Controller
PIRQA	INTA	INTB	INTC	INTA		
PIRQB	INTB	INTC	INTD			
PIRQC	INTC	INTD	INTA			
PIRQD	INTD	INTA	INTB		INTA	INTA

For example, assume an add-in card has one interrupt (group INTD) into the second PCI slot. In this slot, an interrupt source from group INTA connects to the PIRQD signal, which is already connected to the onboard video and USB PCI sources. The add-in card shares an interrupt with these onboard interrupt sources.

NOTE

The PIIX4E can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 11, 14, 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

3 Overview of BIOS Features

The motherboard uses an Intel/Phoenix BIOS, which is stored in flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the flash memory contains the Setup program, Power-On Self Test (POST), Advanced Power Management (APM), the PCI auto-configuration utility, and Windows 95-ready Plug and Play. See Section 6.2 for the supported versions of these specifications.

This motherboard supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as 4K4UE0X0.86A.xxxx.P01.

3.1 BIOS Upgrades

The BIOS can be upgraded from a diskette using the Intel Flash Memory Update utility that is available from Intel. This utility upgrades the BIOS as follows:

- Updates the flash BIOS from a file on a disk
- Updates the language section of the BIOS
- Makes sure that the upgrade BIOS matches the target system to prevent accidentally installing a BIOS for a different type of system.

BIOS upgrades and the Intel Flash Memory Update utility are available from Intel through the Intel World Wide Web site. See Section 6.1 for information about this site.

NOTE

Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.

3.2 BIOS Flash Memory Organization

The Intel® 28F002 2-Mbit flash component is organized as 256 KB x 8 bits and is divided into areas as described in Table 33. The table shows the addresses in the ROM image in normal mode (the addresses change in BIOS Recovery Mode).

Table 33. Flash Memory Organization

Address (Hex)	Size	Description
FFFFC000 - FFFFFFFF	16 KB	Boot Block
FFFFA000 - FFFFBFFF	8 KB	Vital Product Data (VPD) Extended System Configuration Data (ESCD) (SMBIOS configuration data / Plug and Play data)
FFFF9000 - FFFF9FFF	4 KB	Used by BIOS (for activities such as Event Logging)
FFFF8000 - FFFF8FFF	4 KB	OEM logo or Scan Flash Area
FFFC0000 - FFFF7FFF	224 KB	Main BIOS Block

3.3 Plug and Play: PCI Autoconfiguration

The BIOS can automatically configure PCI devices and Plug and Play devices. PCI devices may be onboard or add-in cards. Plug and Play devices are ISA devices built to meet the Plug and Play specification. Autoconfiguration lets a user insert or remove PCI or Plug and Play cards without having to configure the system. When a user turns on the system after adding a PCI or Plug and Play card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card or to system resources. The assignment of PCI interrupts to ISA IRQs is nondeterministic. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in the extended system configuration data (ESCD) format.

For information about the versions of PCI and Plug and Play supported by this BIOS, see Section 6.2. Copies of the specifications can be obtained from the Intel World Wide Web site (see Section 6.2).

3.4 PCI IDE Support

If you select Auto in Setup, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to PIO Mode 4 and recognizes any ATAPI devices, including CD-ROM drives, tape drives and Ultra DMA drives (see Section 6.2 for the supported version of ATAPI). Add-in ISA IDE controllers are not supported. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in Setup. The ATAPI Specification recommends that ATAPI devices be configured as shown in Table 34.

Table 34. Recommendations for Configuring an ATAPI Device

	Primary Cable		Secondary Cable	
Configuration	Drive 0	Drive 1	Drive 0	Drive 1
Normal, no ATAPI	ATA			
Disk and CD-ROM for enhanced IDE systems	ATA		ATAPI	
Legacy IDE system with only one cable	ATA	ATAPI		
Enhanced IDE with CD-ROM and a tape or two CD-ROMs	ATA		ATAPI	ATAPI

3.5 ISA Plug and Play

If Plug and Play O/S (see Section 4.3) is selected in Setup, the BIOS autoconfigures only ISA Plug and Play cards that are required for booting (IPL devices). If Plug and Play O/S is not selected in Setup, the BIOS autoconfigures all Plug and Play ISA cards.

3.6 ISA Legacy Devices

Since ISA legacy devices are not autoconfigurable, the resources for them must be reserved. Resources can be reserved in the Setup program or with an ISA configuration utility. The ISA configuration utility can be downloaded from the Intel World Wide Web site (see Section 6.1).

3.7 System Management BIOS (SMBIOS)

System Management BIOS (SMBIOS) is an interface for managing computers in an enterprise environment. The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel® LANDesk® Client Manager to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

OEMs can use a utility that programs flash memory so the BIOS can report on system and chassis information. This utility is available through Intel sales offices. See Section 6.1 for information about contacting a local Intel sales office. See Section 6.2 for information about the latest SMBIOS specification.

SMBIOS does not work directly under non-Plug and Play operating systems (such as Windows NT). However, the BIOS supports a SMBIOS table interface for such operating systems. Using this support, a SMBIOS service-level application running on a non-Plug and Play OS can access the SMBIOS BIOS information.

3.8 Advanced Power Management (APM)

See Section 6.2 for the version of the APM specification that is supported. The energy saving standby mode can be initiated in the following ways:

- Time-out period specified in Setup
- Suspend/resume switch connected to the front panel sleep connector‡
- From the operating system, such as the Suspend menu item in Windows 95

In standby mode, the motherboard can reduce power consumption by spinning down hard drives, and reducing power to or turning off VESA† DPMS-compliant monitors. Power-management mode can be enabled or disabled in Setup (see Section 4.5).

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default; but the operating system must support an APM driver for the power-management features to work. For example, Windows 95 supports the power-management features upon detecting that APM is enabled in the BIOS.

3.9 Advanced Configuration and Power Interface (ACPI)

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. ACPI requires an ACPI-aware operating system. ACPI features include:

- Plug and Play (including bus and device enumeration) and Advanced Power Management (APM) functionality normally contained in the BIOS
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 30-watt system operation in the Power On Suspend sleeping state, and less than 5-watt system operation in the Soft Off sleeping state
- A Soft-off feature that enables the operating system to power off the computer
- Support for multiple wake up events (see Table 37)
- Support for a front panel power and sleep mode switch. Table 35 describes the system states based on how long the switch is pressed‡

Table 35. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off	Less than four seconds	Power on
On	Less than four seconds	Sleep
On	More than four seconds	Power off
Sleep	Less than four seconds	Wake up

3.9.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 36 lists the power states supported by the motherboard along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 36. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power *
G0 - working state	S0 - working	C0 - working	D0 - working state	Full power > 60 W
G1 - sleeping state	S1 - Processor stopped	C1 - stop grant	D1, D2, D3- device specification specific.	5 W < power < 30 W
G2/S5	S5 - Soft off. Context not saved. Cold boot is required.	No power	D3 - no power except for wake up logic.	Power < 5 W **
G3 - mechanical off. The power supply A/C main inputs are disconnected.	No power to the system.	No power	D3 - no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

* Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.

** Dependent on the standby power consumption of wake-up devices used in the system.

3.9.2 Wake Up Devices and Events

The table below describes which devices or specific events can wake the computer from specific states.

Table 37. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S5
RTC alarm	S1, S5
Modem	S1, S5
USB	S1
PS/2 keyboard	S1
PS/2 mouse	S1

3.9.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure motherboard devices that do not have other hardware standards for enumeration and configuration. PCI devices on the motherboard, for example, are not enumerated by ACPI.

3.9.4 BIOS Support

The BIOS supports both APM and ACPI. If the board is used with an ACPI-aware operating system, the BIOS provides ACPI support. Otherwise, it defaults to APM support.

3.10 Language Support

The Setup program and help messages can be supported in 32 languages. Five languages are available: American English, German, Italian, French, and Spanish. The default language is American English, which is present unless another language is programmed into the BIOS using the flash memory update utility. See Section 3.1 for information about the BIOS update utility.

3.11 Boot Options

In the Setup program, the user can choose to boot from a floppy drive, hard drive, CD-ROM, network, or any BIOS boot specification (BBS) compliant device. The default setting is for the floppy drive to be the primary boot device and the hard drive to be the secondary boot device. By default the third and fourth devices are disabled.

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. See Section 6.2 for information about the El Torito specification. Under the Boot menu in the Setup program, CD-ROM is listed as a boot device. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device.

The network can be selected as a boot device. This selection allows booting from a network add-in card with a remote boot ROM installed.

3.12 OEM Logo or Scan Area

A 4 KB flash-memory user area at memory location FFFF8000h-FFFF8FFFh is for displaying a custom OEM logo during POST. A utility is available from Intel to assist with installing a logo into the flash memory. Contact Intel customer support for further information. See Section 6.1 for information on contacting Intel customer support.

3.13 USB Legacy Support

USB legacy support enables USB keyboards and mice to be used even when no operating system USB drivers are in place. By default, USB legacy support is disabled. USB legacy support is only intended to be used in accessing BIOS Setup and installing an operating system that supports USB.

This sequence describes how USB legacy support operates in the default (disabled) mode.

1. When you power up the computer, USB legacy support is disabled.
2. POST begins.
3. USB legacy support is temporarily enabled by the BIOS. This allows you to use a USB keyboard to enter the Setup program or the maintenance mode.
4. POST completes and disables USB legacy support (unless it was set to Enabled while in Setup).
5. The operating system loads. While the operating system is loading, USB keyboards and mice are not recognized. After the operating system loads the USB drivers, the USB devices are recognized.

To install an operating system that supports USB, enable USB Legacy support in BIOS Setup and follow the operating system's installation instructions. Once the operating system is installed and the USB drivers configured, USB legacy support is no longer used. USB Legacy Support can be left enabled in BIOS Setup if needed.

Notes on using USB legacy support:

- If USB legacy support is enabled, don't mix USB and PS/2 keyboards and mice. For example, do not use a PS/2 keyboard with a USB mouse, or a USB keyboard and a PS/2 mouse.
- Do not use USB devices with an operating system that does not support USB. USB legacy is not intended to support the use of USB devices in a non USB operating system.
- USB legacy support is for keyboards and mice only. Hubs and other USB devices are not supported.

3.14 BIOS Setup Access

Access to the Setup program can be restricted using passwords. User and administrative passwords can be set using the Security menu in Setup. The default is no passwords enabled. See Section 4.4 for information about setting user and administrative passwords.

3.15 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode.

To create a BIOS recovery diskette, a bootable diskette must be created and the recovery files copied to it. The recovery files are available from Intel, contact Intel customer support for further information. See Section 6.1 for information on contacting Intel customer support.

4 BIOS Setup Program

The Setup program is for viewing and changing the BIOS settings for a computer. Setup is accessed by pressing the <F2> key after the Power-On Self Test (POST) memory test begins and before the operating system boot begins.

Table 38 shows the menus available from the menu bar at the top of the Setup screen.

Table 38. Setup Menu Bar

Setup Menu Screen	Description
Maintenance	Specifies the processor speed and clears the Setup passwords. This menu is only available in configure mode. Refer to Section 1.18 for information about configure mode.
Main	Allocates resources for hardware components.
Advanced	Specifies advanced features available through the chipset.
Security	Specifies passwords and security features.
Power	Specifies power management features.
Boot	Specifies boot options and power supply controls.
Exit	Saves or discards changes to the Setup program options.

Table 39 shows the function keys available for menu screens.

Table 39. Setup Function Keys

Setup Key	Description
<F1> or <Alt-H>	Brings up a help screen for the current item.
<Esc>	Exits the menu.
<←> or <→>	Selects a different menu screen.
<↑> or <↓>	Moves cursor up or down.
<Home> or <End>	Moves cursor to top or bottom of the window.
<PgUp> or <PgDn>	Moves cursor to top or bottom of the window.
<F5> or <->	Selects the previous value for a field.
<F6> or <+> or <Space>	Selects the next value for a field.
<F9>	Load the default configuration values for the current menu.
<F10>	Save the current values and exit Setup.
<Enter>	Executes command or selects the submenu.

4.1 Maintenance Menu

The maintenance menu is for setting the processor speed and clearing the Setup passwords. Setup only displays this menu in configure mode. See Section 1.18 for information about setting configure mode.

Table 40. Maintenance Menu

Feature	Options	Description
Processor Speed	• 233 • 266 • 300 • 333	Specifies the processor speed in megahertz. This setup screen will only show speeds up to and including the maximum speed of the processor installed on the motherboard. With a host bus operating at 66 MHz, the board supports processors at the following speeds: 266, 300, and 333 MHz.
Clear All Passwords	No options	Clears the user and administrative passwords.

4.2 Main Menu

This menu reports processor and memory information and is for configuring the system date and system time.

Table 41. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
Cache RAM	No options	Displays size of second-level cache, if present.
System Memory	No options	Displays the total amount of RAM on the motherboard.
Memory Bank 0 Memory Bank 1	No options	Displays size and type of DIMM installed in each memory bank.
Language	• **English (US) (default)** • Italian • Francais • Deutsch • Espanol	Displays the default language used by the BIOS.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Month, day, and year	Specifies the current date.

4.3 Advanced Menu

This menu is for setting advanced features that are available through the chipset.

Table 42. Advanced Menu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if a Plug and Play operating system is being used. *No* lets the BIOS configure all devices. *Yes* lets the operating system configure Plug and Play devices. Not required with a Plug and Play operating system.
Reset Configuration Data	• **No (default)** • Yes	Clears the BIOS configuration data on the next boot.
Numloc	• **Auto (default)** • On • Off	Specifies the power on state of the Num Lock feature on the numeric keypad of the keyboard.
Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
Primary IDE Master, submenu	No options	Specifies Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Floppy Configuration, submenu	No options	When selected, displays the Floppy Options submenu.
SMBIOS Events Logging	No options	Configures SMBIOS Events Logging. When selected, displays the SMBIOS Events Logging submenu.
Video Configuration	No options	Configures video features. When selected, displays the Video Configuration submenu.
Resource Configuration	No options	Configures memory blocks and IRQs for legacy ISA devices. When selected, displays the Resource Configuration submenu.

4.3.1 Peripheral Configuration Submenu

This submenu is for the configuring the computer peripherals.

Table 43. Peripheral Configuration Submenu

Feature	Options	Description
Serial port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. *Auto* assigns the first free COM port, normally COM1, the address 3F8h and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address for serial port A.
Interrupt	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for serial port A.
Serial port B	• Disabled • Enabled • **Auto (default)**	Configures serial port B. *Auto* assigns the first free COM port, the address 2F8h and the interrupt IRQ3. An * (asterisk) displayed next to an address indicates a conflict with another device. If either serial port address is set, that address will not appear in the list of options for the other serial port.
Mode	• **Normal (default)** • IrDA • ASK-IR	Specifies the mode for serial port B for normal or infrared applications.
Base I/O address	• 3F8 • **2F8 (default)** • 3E8 • 2E8	Specifies the base I/O address for serial port B.
Interrupt	• **IRQ 3 (default)** • IRQ 4	Specifies the interrupt for serial port B.
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. *Output Only* operates in AT†-compatible mode. *Bi-directional* operates in bi-directional PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.

continued

Table 43. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Base I/O address	• **378 (default)** • 278 • 228	Specifies the base I/O address for the parallel port.
Interrupt	• IRQ 5 • **IRQ 7 (default)**	Specifies the interrupt for the parallel port.
Audio	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
LAN	• Disabled • **Enabled (default)**	Enables or disables onboard LAN.
PXE	• Disabled • **Enabled (default)**	Enables or disables the PXE.
USB Legacy (Optional)	• **Disabled (default)** • Enabled	Enables or disables the optional legacy USB support.

4.3.2 IDE Configuration

Table 44. IDE Configuration

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the Primary IDE Controller. *Secondary* enables only the Secondary IDE Controller. *Both* enables both IDE controllers.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu
Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.3.3 IDE Configuration Submenus

This submenu is for configuring IDE devices, including:

- Primary IDE master
- Primary IDE slave
- Secondary IDE master
- Secondary IDE slave

Table 45. IDE Configuration Submenus

Feature	Options	Description
Type	• None • ATAPI Removable • Other ATAPI • CD-ROM • User • IDE Removable • **Auto (default)**	Specifies the IDE configuration mode for IDE devices. *User* allows the cylinders, heads, and sectors fields to be changed. *Auto* automatically fills in the values for the cylinders, heads, and sectors fields.
Maximum Capacity	No options	Reports the maximum capacity for the hard disk.
Multi-Sector Transfers	• **Disabled (default)** • 2 Sectors • 4 Sectors • 8 Sectors • 16 Sectors	Specifies number of sectors per block for transfers from the hard drive to memory. Check the hard drive's specifications for optimum setting.
LBA Mode Control	• **Disabled (default)** • Enabled	Enables or disables the LBA mode control.
Transfer Mode	• **Standard (default)** • Fast PIO 1 • Fast PIO 2 • Fast PIO 3 • Fast PIO 4 • FPIO 3 / DMA 1 • FPIO 4 / DMA 2	Specifies the method for moving data to/from the drive.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2	Specifies the Ultra DMA mode for the drive.

4.3.4 Floppy Options Submenu

This submenu is for configuring the floppy drive.

Table 46. Floppy Options Submenu

Feature	Options	Description
Floppy Disk Controller	• Auto • Disabled • **Enabled (default)**	Disables or enables the integrated floppy disk controller.
Diskette A:	• Disabled • 360 KB, 5¼″ • 1.2 MB, 5¼″ • 720 KB, 3½″ • **1.44/1.25 MB, 3½″ (default)** • 2.88 MB, 3½″	Specifies the capacity and physical size of diskette drive A.
Floppy Write Protect	• **Disabled (default)** • Enabled	Disables or enables write protect for the diskette drive.

4.3.5 DMI Event Logging

This submenu is for configuring the DMI event logging features.

Table 47. DMI Event Logging Submenu

Feature	Options	Description
Event log capacity	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
View DMI event log	No options	Enables viewing of SMBIOS event log.
Clear all DMI event logs	• **No (default)** • Yes	Clears the SMBIOS event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of SMBIOS events.
Mark DMI events as read	No options	Marks all SMBIOS events as read.

4.3.6 Video Configuration Submenu

This submenu is for configuring video features.

Table 48. Video Configuration Submenu

Feature	Options	Description
Palette Snooping	• **Disabled (default)** • Enabled	Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card.
AGP Aperture Size	• **64 MB (default)** • 256 MB	Specifies the aperture size for the A.G.P. video controller.

4.3.7 Resource Configuration Submenu

This submenu is for configuring the memory and interrupts.

Table 49. Resource Configuration Submenu

Feature	Options	Description
Memory Reservation	• C800 - CBFF **Available (default)** | Reserved • CC00- CFFF **Available (default)** | Reserved • D000 - D3FF **Available (default)** | Reserved • D400 - D7FF **Available (default)** | Reserved • D800 - DBFF **Available (default)** | Reserved • DC00 - DFFF **Available (default)** | Reserved	Reserves specific upper memory blocks for use by legacy ISA devices.
IRQ Reservation	• IRQ3 **Available (default)** | Reserved • IRQ4 **Available (default)** | Reserved • IRQ5 **Available (default)** | Reserved • IRQ7 **Available (default)** | Reserved • IRQ10 **Available (default)** | Reserved • IRQ11 **Available (default)** | Reserved	Reserves specific IRQs for use by legacy ISA devices. An * (asterisk) displayed next to an IRQ indicates an IRQ conflict.

4.4 Security Menu

This menu is for setting passwords and security features.

Table 50. Security Menu

Feature	Options	Description
User Password Is	No options	Reports if there is a user password set.
Administrative Password Is	No options	Reports if there is a administrative password set.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Set Administrative Password	Password can be up to seven alphanumeric characters.	Specifies the administrative password.
Clear User	No Options	Clears the user password.
User Setup Access	• Disabled • **View only (default)** • Limited access • Enabled	Enables or disables User Setup Access. *Disabled* prevents the user from accessing Setup. View only and limited access options are available only when the administrative password is set.
Unattended Start	• **Disabled (default)** • Enabled	Enables the unattended start feature. When enabled, the computer boots, but the keyboard is locked. The user must enter a password to unlock the computer or boot from a floppy diskette.

4.5 Power Menu

This menu is for setting power management features.

Table 51. Power Menu

Feature	Options	Description
Power Management	• Disabled • **Enabled (default)**	Enables or disables the BIOS power management feature.
Fan always on	• Yes • **No (default)**	If enabled, the fan will continue to run when the system has been powered off.
Inactivity Timer	• **Off (default)** (default) • 1 Minute • 5 Minutes • 10 Minutes • 20 Minutes • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters standby mode.
Hard Drive	• Disabled • **Enabled (default)**	Enables power management for hard disks during standby and suspend modes.
VESA Video Power Down	• Disabled • **Standby (default)** • Suspend • Sleep	Specifies power management for video during standby and suspend modes.

4.6 Boot Menu

This menu is for setting the boot features and the boot sequence.

Table 52. Boot Menu

Feature	Options	Description
Quick Boot Mode	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Power On • Stay Off • **Last State (default)**	Specifies the mode of operation if an AC/Power loss occurs. *Power On* restores power to the computer. *Stay Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before power loss occurred.
On Modem Ring	• Stay Off • **Power On (default)**	Specifies how the computer responds to an incoming call on an installed modem when the system is off.
On LAN	• Stay Off • **Power On (default)**	Specifies how the computer responds to a LAN wakeup event when the power is off.

continued

Table 52. Boot Menu (continued)

Feature	Options	Description
On PME	• **Stay Off (default)** • Power On	Specifies how the computer responds to a PME wakeup event when the power is off.
First Boot Device Second Boot Device Third Boot Device Fourth Boot Device Fifth Boot Device	• Removable devices • Hard Drive • ATAPI CD-ROM Drive • Network Boot • LSA	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering. LSA option is available only if LAN is present.
Hard Drive	No options	Lists available hard drives. When selected, displays the Hard Drive submenu.
Removable Devices	No options	Lists available removable devices. When selected, displays the Removable Devices submenu.

4.6.1 Hard Drive Submenu

This submenu is for configuring the boot sequence for hard drives.

Table 53. Hard Drive Submenu

Options	Description
• Bootable Add in Card	Specifies the boot sequence for the hard drives attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.6.2 Removable Devices Submenu

This submenu is for configuring the boot sequence for removable devices.

Table 54. Removable Devices Submenu

Options	Description
• Legacy Floppy Drives	Specifies the boot sequence for the removable devices attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.7 Exit Menu

This menu is for exiting the Setup program, saving changes, and loading and saving defaults.

Table 55. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS RAM.
Exit Discarding Changes	Exits without saving any changes made in Setup.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

5.1 BIOS Error Messages

Table 56. BIOS Error Messages

Error Message	Explanation
Diskette drive A error	Drive A is present but fails the POST diskette tests. Check that the drive is defined with the proper diskette type in Setup and that the diskette drive is installed correctly.
Extended RAM Failed at offset: *nnnn*	Extended memory not working or not configured properly at offset *nnnn*.
Failing Bits: *nnnn*	The hexadecimal number *nnnn* is a map of the bits at the RAM address (System, Extended, or Shadow memory) that failed the memory test. Each 1 in the map indicates a failed bit.
Fixed Disk 0 Failure or Fixed Disk 1 Failure or Fixed Disk Controller Failure	Fixed disk is not working or not configured properly. Check to see if fixed disk is installed properly. Run Setup be sure the fixed-disk type is correctly identified.
Incorrect Drive A type - run SETUP	Type of diskette drive for drive A not correctly identified in Setup.
Invalid NVRAM media type	Problem with NVRAM (CMOS) access.
Keyboard controller error	The keyboard controller failed test. Try replacing the keyboard.
Keyboard error	Keyboard not working.
Keyboard error nn	BIOS discovered a stuck key and displays the scan code nn for the stuck key.
Keyboard locked - Unlock key switch	Unlock the system to proceed.
Monitor type does not match CMOS - Run SETUP	Monitor type not correctly identified in Setup.
Operating system not found	Operating system cannot be located on either drive A or drive C. Enter Setup and see if fixed disk and drive A are properly identified.
Parity Check 1	Parity error found in the system bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Parity Check 2	Parity error found in the I/O bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Press <F1> to resume, <F2> to Setup	Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change any settings.
Real time clock error	Real-time clock fails BIOS test. May require motherboard repair.

continued

Table 56. BIOS Error Messages (continued)

Error Message	Explanation
Shadow RAM Failed at offset: *nnnn*	Shadow RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System battery is dead - Replace and run SETUP	The CMOS clock battery indicator shows the battery is dead. Replace the battery and run Setup to reconfigure the system.
System cache error - Cache disabled	RAM cache failed the BIOS test. BIOS disabled the cache.
System CMOS checksum bad - run SETUP	System CMOS RAM has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. Run Setup and reconfigure the system either by getting the default values and/or making your own selections.
System RAM Failed at offset: *nnnn*	System RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System timer error	The timer test failed. Requires repair of system motherboard.

nnnn = hexadecimal number

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display. These cards can be purchased from JDR Microdevices or other sources.

The following table provides the POST codes that can be generated by the BIOS. Some codes are repeated in the table because that code applies to more than one operation.

Table 57. Port 80h Codes

Code	Description of POST Operation
02h	Verify real mode
03h	Disable non-maskable interrupt (NMI)
04h	Get processor type
06h	Initialize system hardware
08h	Initialize chipset with initial POST values
09h	Set IN POST flag
0Ah	Initialize processor registers
0Bh	Enable processor cache
0Ch	Initialize caches to initial POST values
0Eh	Initialize I/O component
0Fh	Initialize the local bus IDE
10h	Initialize power management
11h	Load alternate registers with initial POST *valuesnew*
12h	Restore processor control word during warm boot
13h	Initialize PCI bus mastering devices
14h	Initialize keyboard controller
16h	BIOS ROM checksum
17h	Initialize cache before memory autosize
18h	8254 timer initialization
1Ah	8237 DMA controller initialization
1Ch	Reset programmable interrupt controller
20h	Test DRAM refresh
22h	Test keyboard controller
24h	Set ES segment register to 4 GB
26h	Enable A20 line
28h	Autosize DRAM

continued

Table 57. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
29h	Initialize POST memory manager
2Ah	Clear 512 KB base RAM
2Ch	RAM failure on address line *xxxx**
2Eh	RAM failure on data bits *xxxx** of low byte of memory bus
2Fh	Enable cache before system BIOS shadow
30h	RAM failure on data bits *xxxx** of high byte of memory bus
32h	Test processor bus-clock frequency
33h	Initialize POST dispatch manager
34h	Test CMOS RAM
35h	Initialize alternate chipset registers
36h	Warm start shut down
37h	Reinitialize the chipset (motherboard only)
38h	Shadow system BIOS ROM
39h	Reinitialize the cache (motherboard only)
3Ah	Autosize cache
3Ch	Configure advanced chipset registers
3Dh	Load alternate registers with CMOS *valuesnew*
40h	Set Initial processor speed new
42h	Initialize interrupt vectors
44h	Initialize BIOS interrupts
45h	POST device initialization
46h	Check ROM copyright notice
47h	Initialize manager for PCI option ROMs
48h	Check video configuration against CMOS RAM data
49h	Initialize PCI bus and devices
4Ah	Initialize all video adapters in system
4Bh	Display QuietBoot screen
4Ch	Shadow video BIOS ROM
4Eh	Display BIOS copyright notice
50h	Display processor type and speed
51h	Initialize EISA motherboard
52h	Test keyboard
54h	Set key click if enabled
56h	Enable keyboard
58h	Test for unexpected interrupts
59h	Initialize POST display service
5Ah	Display prompt "Press F2 to enter SETUP"
5Bh	Disable processor cache

continued

Table 57. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
5Ch	Test RAM between 512 and 640 KB
60h	Test extended memory
62h	Test extended memory address lines
64h	Jump to UserPatch1
66h	Configure advanced cache registers
67h	Initialize multiprocessor APIC
68h	Enable external and processor caches
69h	Setup System Management Mode (SMM) area
6Ah	Display external L2 cache size
6Ch	Display shadow-area message
6Eh	Display possible high address for UMB recovery
70h	Display error messages
72h	Check for configuration errors
74h	Test real-time clock
76h	Check for keyboard errors
7Ah	Test for key lock on
7Ch	Set up hardware interrupt vectors
7Eh	Initialize coprocessor if present
80h	Disable onboard Super I/O ports and IRQs
81h	Late POST device initialization
82h	Detect and install external RS232 ports
83h	Configure non-MCD IDE controllers
84h	Detect and install external parallel ports
85h	Initialize PC-compatible PnP ISA devices
86h	Re-initialize onboard I/O ports
87h	Configure motherboard configurable devices
88h	Initialize BIOS Data Area
89h	Enable Non-Maskable Interrupts (NMIs)
8Ah	Initialize extended BIOS data area
8Bh	Test and initialize PS/2 mouse
8Ch	Initialize diskette controller
8Fh	Determine number of ATA drives
90h	Initialize hard-disk controllers
91h	Initialize local-bus hard-disk controllers
92h	Jump to UserPatch2
93h	Build MPTABLE for multiprocessor boards
94h	Disable A20 address line (Rel. 5.1 and earlier)
95h	Install CD-ROM for boot

continued

Table 57. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
96h	Clear huge ES segment register
97h	Fix up multiprocessor table
98h	Search for option ROMs
99h	Check for SMART Drive
9Ah	Shadow option ROMs
9Ch	Set up power management
9Eh	Enable hardware interrupts
9Fh	Determine number of ATA and SCSI drives
A0h	Set time of day
A2h	Check key lock
A4h	Initialize typematic rate
A8h	Erase F2 prompt
Aah	Scan for F2 key stroke
Ach	Enter SETUP
Aeh	Clear IN POST flag
B0h	Check for errors
B2h	POST done - prepare to boot operating system
B4h	One short beep before boot
B5h	Terminate QuietBoot
B6h	Check password (optional)
B8h	Clear global descriptor table
B9h	Clean up all graphics
Bah	Initialize SMBIOS parameters
BBh	Initialize PnP Option ROMs
BCh	Clear parity checkers
BDh	Display MultiBoot menu
Beh	Clear screen (optional)
BFh	Check virus and backup reminders
C0h	Try to boot with INT 19h
C1h	Initialize POST Error Manager (PEM)
C2h	Initialize error logging
C3h	Initialize error display function
C4h	Initialize system error handler
E0h	Initialize the chipset
E1h	Initialize the bridge
E2h	Initialize the processor

continued

Table 57. Port 80h Codes (continued)

Code	Description of POST Operation (The following are for boot block in flash ROM)
E3h	Initialize system timer
E4h	Initialize system I/O
E5h	Check force recovery boot
E6h	Checksum BIOS ROM
E7h	Go to BIOS
E8h	Set huge segment
E9h	Initialize multiprocessor
Eah	Initialize OEM special code
Ebh	Initialize PIC and DMA
Ech	Initialize memory type
Edh	Initialize memory size
Eeh	Shadow boot block
Efh	System memory test
F0h	Initialize interrupt vectors
F1h	Initialize runtime clock
F2h	Initialize video
F3h	Initialize beeper
F4h	Initialize boot
F5h	Clear huge segment
F6h	Boot to mini-DOS
F7h	Boot to full DOS

* If the BIOS detects error 2Ch, 2Eh, or 30h (base 512 K RAM error), it displays an additional word-bitmap (xxxx) indicating the address line or bits that failed. For example, "2C 0002" means address line 1 (bit one set) has failed. "2E 1020" means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. The BIOS also sends the bitmap to the port-80 LED display. It first displays the check point code, followed by a delay, the high-order byte, another delay, and then the low-order byte of the error. It repeats this sequence continuously.

5.3 BIOS Beep Codes

Whenever a recoverable error occurs during Power-On Self Test (POST), the BIOS displays an error message describing the problem. The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (no card installed or faulty) or if an external ROM module does not properly checksum to zero.

An external ROM module (such as video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST Terminal Error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 58. Beep Codes

Beeps	Port 80h Code	Explanation
1-2-2-3	16h	BIOS ROM checksum
1-3-1-1	20h	Test DRAM refresh
1-3-1-3	22h	Test keyboard controller
1-3-3-1	28h	Autosize DRAM
1-3-3-2	29h	Initialize POST memory manager
1-3-3-3	2Ah	Clear 512 KB base RAM
1-3-4-1	2Ch	RAM failure on address line xxxx
1-3-4-3	2Eh	RAM failure on data bits xxxx of low byte of memory bus
1-4-1-1	30h	RAM failure on data bits xxxx of high byte of memory bus
2-1-2-2	45h	POST device initialization
2-1-2-3	46h	Check ROM copyright notice
2-2-3-1	58h	Test for unexpected interrupts
2-2-4-1	5Ch	Test RAM between 512 and 640 KB
1-2	98h	Search for option ROMs. One long, two short beeps on checksum failure

6 Specifications and Customer Support

6.1 Online Support

Find information about Intel boards under “Product Info” or “Customer Support” at this World Wide Web site:

http://www.intel.com/

6.2 Specifications

The motherboard complies with the following specifications:

Table 59. Compliance with Specifications

Specification	Description	Revision Level
A.G.P.	Accelerated Graphics Port Interface Specification	Revision 1.0, July, 1996, Intel Corporation. The specification is available through the Accelerated Graphics Implementers Forum at: http://www.agpforum.org/.
APM	Advanced Power Management BIOS interface specification	Revision 1.2, February, 1996 Intel Corporation, Microsoft Corporation
ACPI	Advanced Configuration and Power Interface specification	Revision 1.0, December 22, 1996 Intel Corporation, Microsoft Corporation, and Toshiba Corporation
ATA-3	Information Technology - AT Attachment-3 Interface	X3T10/2008D Revision 6 ATA Anonymous FTP Site: fission.dt.wdc.com
ATAPI	ATA Packet Interface for CD-ROMs	SFF-8020i Revision 2.5 (SFF) Fax Access: (408) 741-1600
NLX	NLX form factor specification	Revision 2.01, February 1997 Intel Corporation, The specification is available at: http://www.intel.com/
NLX	NLX form factor specification	Version 1.0, December, 1997 Intel Corporation
SMBIOS	SMBIOS specification	Version 2.1 - 16 June 1997 Award Software International Inc., Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, SystemSoft Corporation.
El Torito	Bootable CD-ROM format specification	Version 1.0, January 25, 1995 Phoenix Technologies Ltd., IBM Corporation. The El Torito specification is available on the Phoenix Web site http://www.ptltd.com/techs/specs.html.

continued

Table 59. Compliance with Specifications (continued)

Specification	Description	Revision Level
EPP	Enhanced Parallel Port	IEEE 1284 standard, Mode [1 or 2], v1.7
IrDA	Serial Infrared Physical Layer Link specification	Version 1.1, October 17, 1995 Infrared Data Association.
PCI	PCI Local Bus specification	Revision 2.1, June 1, 1995, PCI Special Interest Group http://www.pcisig.com
Phoenix BIOS	Phoenix BIOS	Revision 4.0, February 27, 1997, Phoenix Technologies Ltd.
Plug and Play	Plug and Play BIOS specification	Version 1.0a, May 5, 1994 Compaq Computer Corporation, Phoenix Technologies Ltd., Intel Corporation
SDRAM DIMMs (64-bit)	PC SDRAM Unbuffered DIMM specification	Revision 0.9, October 22, 1997, Intel Corporation
USB	Universal serial bus specification	Revision 1.0, January 15, 1996 Compaq Computer Corporation, Digital Equipment Corporation, IBM PC Company, Intel Corporation, Microsoft Corporation, NEC, Northern Telecom