Intel® Desktop Board SU810

Technical Product Specification

September 1999

Order Number 741219-002

The Desktop Board SU810 may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Desktop Board SU810 Specification Update.

Revision History

Revision	Revision History	Date
001	First Release of the SU810 Motherboard Technical Product Specification	July 1999
002	Second release of the document. Revisions include: • Changed document title to *Intel® Desktop Board SU810 Technical Product Specification* • Added support for Intel® Celeron™ processors at 500 MHz • Removed references to ECC memory support • Updated Chapter 4 with most recent BIOS screen information	September 1999

This product specification applies to only standard SU810 boards with BIOS identifier SU81010A.86A.

Changes to this specification will be published in the Desktop Board SU810 Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the SU810 board. It describes the standard board product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the board and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on this board
2	A map of electrical and mechanical board resources including connector and jumper locations
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and POST codes

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions, which, if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#).
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the board, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
kB	Kilobyte (1024 bytes).
kbit	Kilobit (1024 bits).
MB	Megabyte (1,048,576 bytes).
Mbit	Megabit (1,048,576 bits).
GB	Gigabyte (1,073,741,824 bytes).
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltage references are DC unless otherwise specified.
†	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

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5 Error Messages and Beep Codes

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Tables

1 Board Description

What This Chapter Contains

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the SU810 board's major features.

Table 1. Feature Summary

Form Factor	NLX (10.00 inches by 8.25 inches)
Processor	Support for an Intel® Celeron™ processor in a PPGA package
Memory	• Two 168-pin dual inline memory module (DIMM) sockets • Support for up to 512 MB of 100 MHz synchronous DRAM (SDRAM) • Support for serial presence detect (SPD) and non-SPD DIMMs
Chipset	Intel® 810 Chipset, consisting of: • Intel® 82810 DC-100 Graphics/Memory Controller Hub (GMCH) with a 4 MB SDRAM display cache • Intel® 82801AA I/O Controller Hub (ICH) • Intel® 82802AB 4 Mbit Firmware Hub (FWH)
I/O Control	SMSC LPC47B272 I/O controller
Peripheral Interfaces	• Two serial ports • Two universal serial bus (USB) ports • One parallel port • Two IDE interfaces with Ultra DMA support (routed to NLX riser card edge) • One diskette drive interface (routed to NLX riser card edge)
Expansion Capabilities	Riser dependent
BIOS	• Intel/AMI BIOS stored in an Intel 82802AB 4 Mbit Firmware Hub (FWH) • Support for Advanced Power Management (APM), Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS

For information about	Refer to
The board's compliance level with APM, ACPI, Plug and Play, and SMBIOS	Section 1.3, page 14

1.1.2 Manufacturing Options

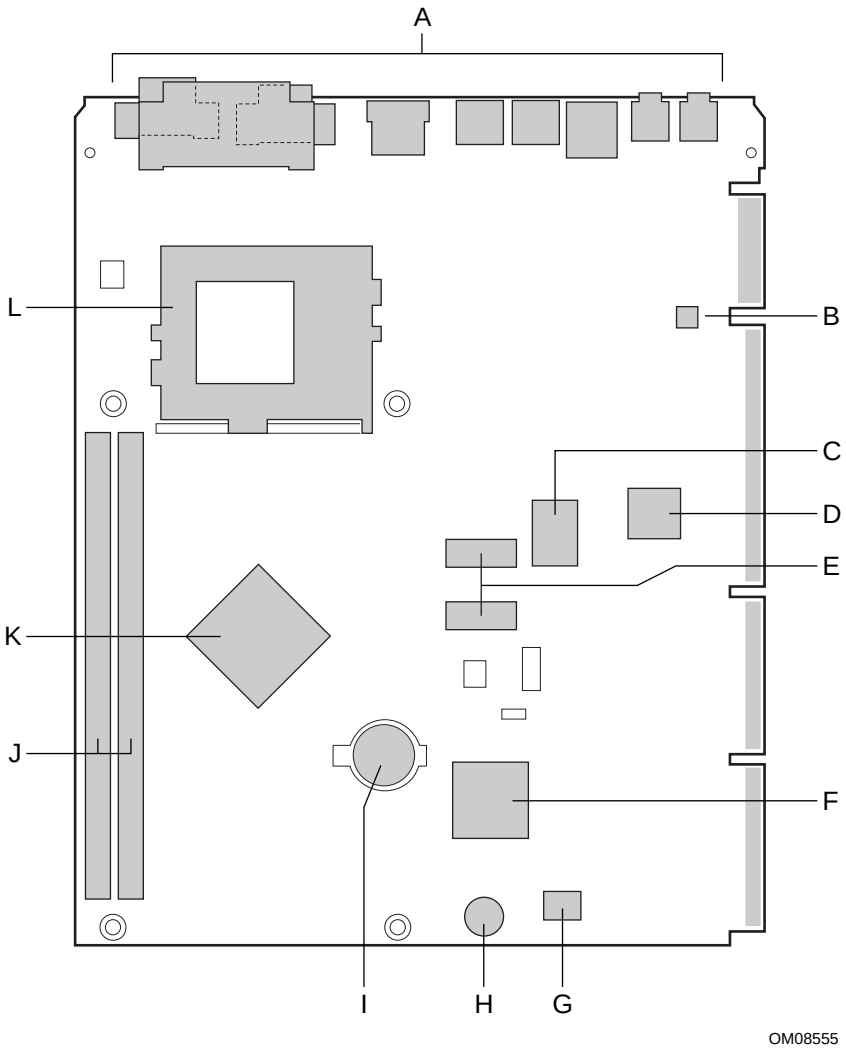
Table 2 describes the SU810 board's manufacturing options. Not every manufacturing option is available in all marketing channels. Please contact your Intel representative to determine which manufacturing options are available to you.

Table 2. Manufacturing Options

GMCH0 Component	Replaces Intel 82810 Graphics/Memory Controller Hub (GMCH); does not include 4 MB SDRAM display cache
LAN Subsystem	• Intel® 82559 PCI LAN controller • RJ-45 LAN connector
Hardware Monitor Component	Provides low-cost instrumentation capabilities
Alert on LAN† technology (Alert on LAN 2 Component)	Provides a management interface between the board's monitoring hardware and a remote console

1.1.3 Board Layout

Figure 1 shows the location of the major components on the board.

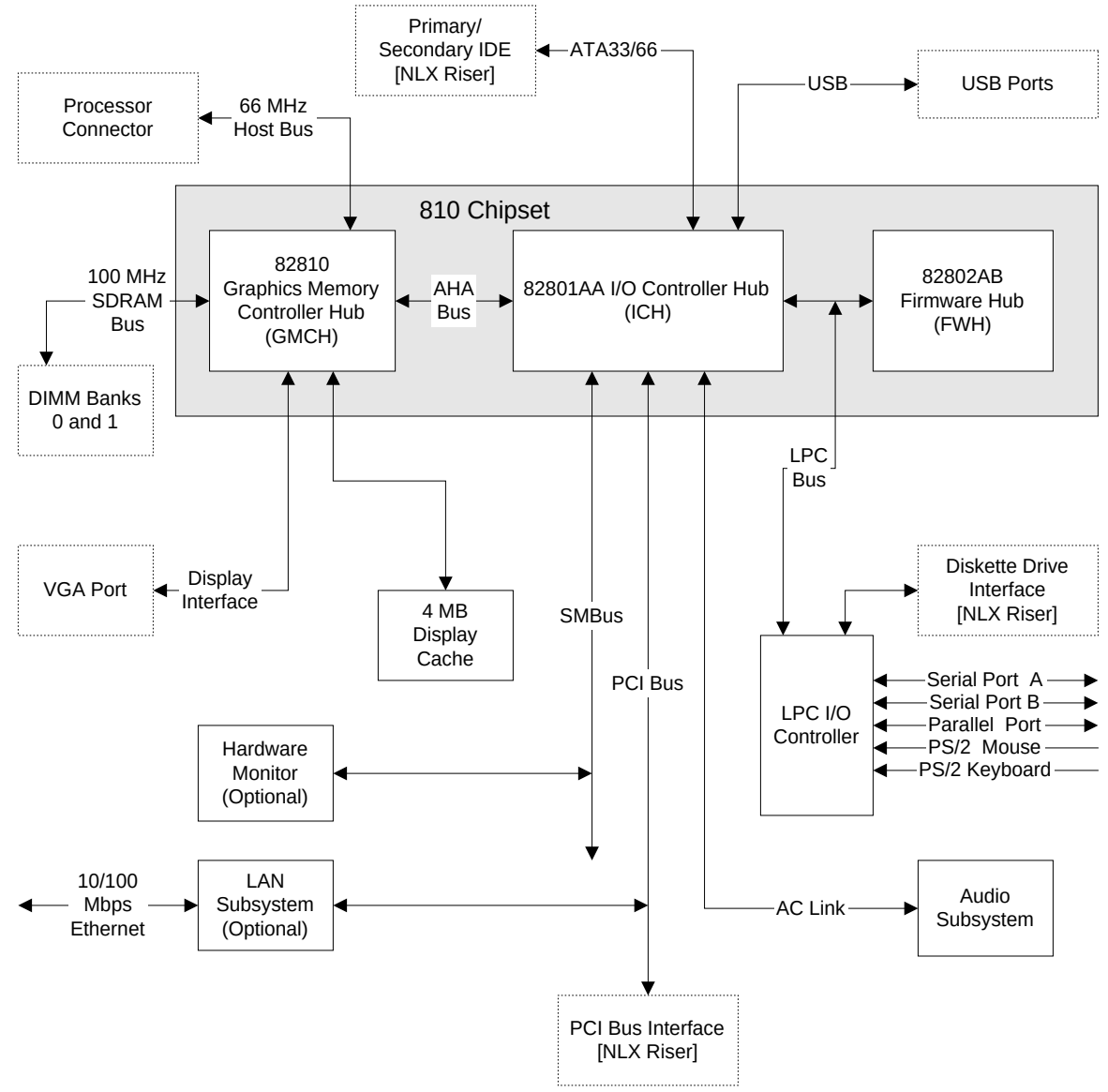


A	Back panel connectors	G	Intel 82802AB 4 Mbit Firmware Hub (FWH)
B	Analog Devices AD1881 Audio Codec	H	Speaker
C	SMSC LPC47B272 I/O controller	I	Battery
D	Intel 82559 10/100 Mbps PCI LAN Controller	J	DIMM sockets
E	Display cache	K	Intel 82810 DC-100 GMCH
F	Intel 82801AA I/O Controller Hub (ICH)	L	Processor socket

Figure 1. Board Components

1.1.4 Block Diagram

Figure 2 is a block diagram of the major functional areas of the board.



[NLX Riser] = Signals routed to the NLX card edge connector

OM08829

Figure 2. Block Diagram

1.2 Online Support

You will find information about Intel desktop boards under “Product Info” or “Customer Support” at these World Wide Web sites:

http://www.intel.com/design/motherbd
http://support.intel.com/support/motherboards/desktop

1.3 Design Specifications

Table 3 lists the specifications applicable to the SU810 board.

Table 3. Specifications

Specification	Description	Revision Level
AC ‘97	Audio Codec ‘97	Revision 2.1, May 1998, Intel Corporation ftp://download.intel.com/pc-supp/platform/ac97
ACPI	Advanced Configuration and Power Interface specification	Revision 1.0, July 1, 1998 Intel Corporation, Microsoft Corporation, and Toshiba Corporation. The specification is available at: http://www.teleport.com/~acpi/
AGP	Accelerated Graphics Port Interface Specification (2X only)	Revision 2.0, May 4, 1998, Intel Corporation. The specification is available through the Accelerated Graphics Implementers Forum at: http://www.agpforum.org/
AMI BIOS	American Megatrends	AMIBIOS 98: www.amibios.com
APM	Advanced Power Management BIOS interface specification	Revision 1.2, February, 1996 Intel Corporation, Microsoft Corporation
ATA-3	Information Technology - AT Attachment-3 Interface	X3T10/2008D Revision 6 ATA Anonymous FTP Site: fission.dt.wdc.com
ATAPI	ATA Packet Interface for CD-ROMs	SFF-8020i Revision 2.5 (SFF) Fax Access: (408) 741-1600
El Torito	Bootable CD-ROM format specification	Version 1.0, January 25, 1995 Phoenix Technologies Ltd., IBM Corporation. This specification is available on the Phoenix Web site at: http://www.ptltd.com/techs/specs.html
EPP	Enhanced Parallel Port	IEEE 1284 standard, Mode [1 or 2], v1.7
LPC	Low Pin Count Interface Specification	Revision 1.0, September 29, 1997, Intel Corporation. This specification is available at: http://www.intel.com/design/chipsets/industry/lpc.htm

continued

Table 3. Specifications (continued)

Specification	Description	Revision Level
NLX Motherboard	NLX Form Factor Specification	Version 1.2, March 1997 Intel Corporation. The specification is available at: http://www.teleport.com/~nlx/spec/index.htm
NLX Power Supply	NLX Power Supply Recommendations	Version 1.1, May 1997 Intel Corporation. The specification is available at: http://www.teleport.com/~nlx/spec/index.htm
NLX Riser Card	NLX Generic Riser Card Design Overview	Version 1.2, August 1998 Intel Corporation. The specification is available at: http://www.teleport.com/~nlx/spec/index.htm
PCI	PCI Local Bus Specification	Revision 2.2, December 18, 1998, PCI Special Interest Group. The specification is available at: http://www.pcisig.com/
PCI	PCI Bus Power Management Interface Specification	Revision 1.1, December 18, 1998, PCI Special Interest Group. The specification is available at: http://www.pcisig.com/
Plug and Play	Plug and Play BIOS Specification	Version 1.0a, May 5, 1994 Compaq Computer Corporation, Phoenix Technologies Ltd., Intel Corporation
SDRAM	PC SDRAM Unbuffered DIMM Specification PC SDRAM DIMM Specification PC Serial Presence Detect (SPD) Specification	Revision 1.0, February, 1998, Intel Corporation Revision 1.5, November, 1997, Intel Corporation Revision 1.2A, December, 1997
SMBIOS	System Management BIOS	Version 2.3, 12 August 1998 Award Software International Inc., Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, American Megatrends Inc., and SystemSoft Corporation. http://developer.intel.com/ial/wfm/design/smbios
UHCI	Universal Host Controller Interface	Design Guide Revision 1.1, March 1996 Intel Corporation. The specification is available at: http://www.usb.org/developers
USB	Universal Serial Bus Specification	Revision 1.1, September 23, 1998 Compaq Computer Corporation, Digital Equipment Corporation, IBM PC Company, Intel Corporation, Microsoft Corporation, NEC, Northern Telecom http://usb.org/developers
WfM	Wired for Management Baseline	Version 2.0, December 18, 1998, Intel Corporation This specification is available at: http://developer.intel.com/ial/WfM/wfmspecs.htm

1.4 Processor

⚠ CAUTION

The board supports processors that draw a maximum of 15.2 amps. Using a processor that draws more than 15.2 amps can damage the processor, the board, and the power supply. See the processor's data sheet for current usage requirements.

The board supports a single Celeron processor as shown in Table 4. The host bus speed is automatically selected.

Table 4. Processors Supported by the Board

Processor Type	Processor Speed	Host Bus Frequency	L2 Cache Size
Celeron processor	300A MHz	66 MHz	128 KB
	333 MHz	66 MHz	128 KB
	366 MHz	66 MHz	128 KB
	400 MHz	66 MHz	128 KB
	433 MHz	66 MHz	128 KB
	466 MHz	66 MHz	128 KB
	500 MHz	66 MHz	128 KB

All supported onboard memory can be cached, up to the cachability limit of the processor.

For information about	Refer to
Processor support for the SU810 board	http://support.intel.com/support/motherboards/desktop
Processor data sheets	http://www.intel.com/design/litcentr

1.5 System Memory

CAUTION

To be fully compliant with all applicable Intel® SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. If your memory modules do not support SPD, you will see a notification to this effect on the screen at power-up. The BIOS will attempt to configure the memory controller for normal operation; however, DIMMs may not function at the determined frequency. Also, BIOS Recovery cannot be accomplished using non-SPD DIMMs. SPD data structure is required for the recovery process.

CAUTION

Because the main system memory is also used as video memory, the SU810 requires 100 MHz SDRAM DIMMs even though the processor front side bus is 66 MHz. It is highly recommended that SPD DIMMs be used, since this allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted.

The board has two DIMM sockets. The minimum memory size is 16 MB and the maximum memory size is 512 MB. The BIOS automatically detects memory type, size, and speed. Memory can be installed in one or both sockets. Memory size can vary between sockets.

The board supports the following memory features:

- 3.3 V, 168-pin DIMMs with gold-plated contacts
- 100 MHz SDRAM
- Serial Presence Detect (SPD) or non-SPD memory
- 64-bit (non-ECC) memory
- Unbuffered single- or double-sided DIMMs

The board is designed to support DIMMs in the configurations listed in Table 5 below.

Table 5. System Memory Configuration

DIMM Size	Configuration
16 MB	2 Mbit x 64
32 MB	4 Mbit x 64
64 MB	8 Mbit x 64
128 MB	16 Mbit x 64
256 MB (Note)	32 Mbit x 64

Note: 256 MB DIMMs used with this board must be built with 128 Mbit device technology.

For information about	Refer to
The *PC Serial Presence Detect Specification*	Table 3, page 14
Obtaining copies of PC SDRAM specifications	http://www.intel.com/design/pcisets/memory

1.6 Intel® 810 Chipset

The Intel® 810 chipset consists of the following devices:

- 82810 Graphics Memory Controller Hub (GMCH)
- 82801AA I/O Controller Hub (ICH)
- 82802AB Firmware Hub (FWH)

The chipset provides the host, memory, AGP, and I/O interfaces shown in Figure 3.

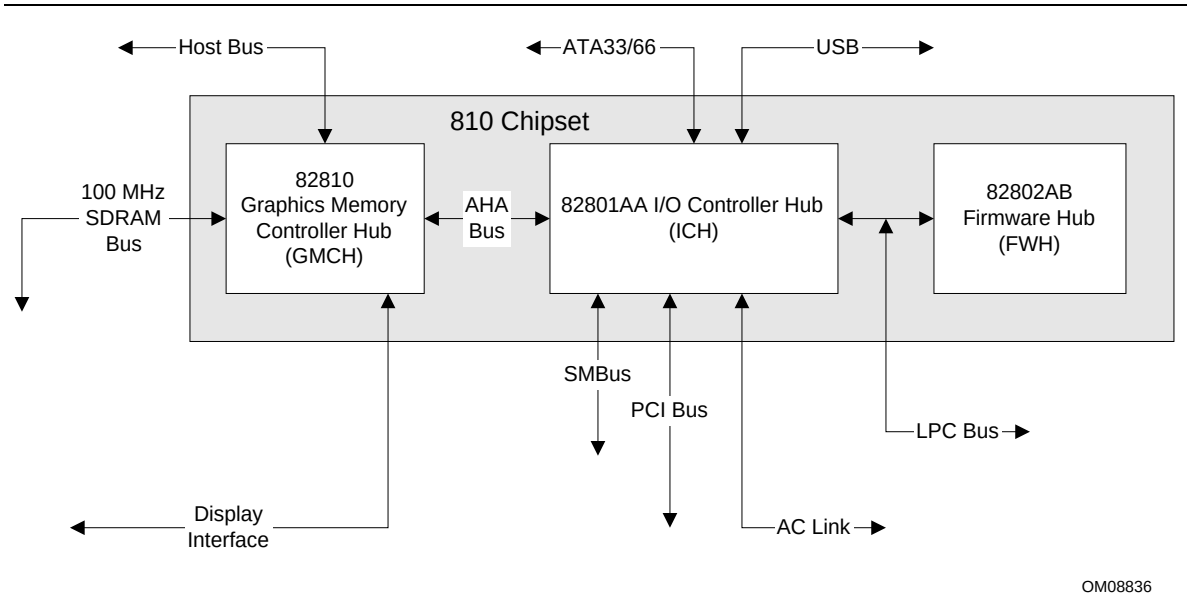


Figure 3. Intel 810 Chipset Block Diagram

For information about	Refer to
The Intel 810 chipset	http://www.developer.intel.com
The resources used by the chipset	Chapter 2
The chipset's compliance with ACPI, APM, AC '97	Section 1.3, page 14

1.6.1 AGP

AGP is a high-performance bus for graphics-intensive applications, such as 3D. AGP, while based on the *PCI Local Bus Specification*, Rev. 2.1, is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amount of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent bus efficiency

For information about	Refer to
The onboard AGP controller	Section 1.8, page 24
The location of the VGA port connector	Figure 4, page 42
Obtaining the *Accelerated Graphics Port Interface Specification*	Table 3, page 14

1.6.2 USB

The board has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The two USB ports are implemented with stacked back-panel connectors. The board fully supports UHCI and uses UHCI-compatible software drivers. USB features include:

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

With an optional jumper, USB port 0 on the back panel can be disabled or rerouted to an optional front panel USB connector on an NLX riser.

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 4, page 42
The signal names of the USB connectors	Table 24, page 45
The jumper settings for USB port 0	Section 2.10.1, page 55
The USB specification and UHCI design guide	Table 3, page 14

1.6.3 IDE Support

The board has two independent bus-mastering IDE interfaces. These interfaces support:

- ATAPI devices (such as CD-ROM drives)
- ATA devices using the transfer modes listed in Table 52 on page 82

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The board supports laser servo (LS-120) diskette technology through its IDE interfaces. The LS 120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

⌦ NLX FEATURE

The IDE interface signals are routed to the NLX card edge connector.

For information about	Refer to
BIOS Setup program's Boot menu	Table 61, page 90
The signal names of the NLX card edge connector	NLX form factor specification, available at: http://www.teleport.com/~nlx/spec/index.htm

1.6.4 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multi-century calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3 V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTE

If the battery and AC power fail, standard defaults, not custom defaults, will be loaded into CMOS RAM at power-on.

For information about	Refer to
Proper date access in systems with Intel desktop boards	http://www.support.intel.com/year2000

1.7 I/O Controller

The SMSC LPC47B272 I/O controller provides the following features:

- Low pin count (LPC) interface
- Two serial ports
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.2 MB, 1.44 MB, or 2.88 MB diskette drive
- Intelligent power management, including a programmable wake up event interface
- Fan control:
  - Two pulse width modulation (PWM) fan speed control outputs
  - Two fan tachometer inputs

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
SMSC LPC47B272 I/O controller	http://www.smsc.com

1.7.1 Serial Ports

The board has two serial ports. Serial port A is routed to 9-pin D-Sub serial port connector located on the back panel. Serial port B is routed to a 9-pin connector at location J6D2. The serial ports' NS16C550-compatible UARTs support data transfers at speeds up to 115.2 Kbits/sec with BIOS support. The serial ports can be assigned as COM1 (3F8), COM2 (2F8), COM3 (3E8), or COM4 (2E8).

For information about	Refer to
The location of the serial port connectors	Figure 4, page 42
The signal names of serial port A connector	Table 21, page 44
The signal names of serial port B connector	Table 27, page 45

1.7.2 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel. In the BIOS Setup program, the parallel port can be configured for the following:

- Output only (AT†-compatible mode)
- Bi-directional (PS/2-compatible)
- EPP
- ECP

For information about	Refer to
The location of the parallel port connector	Figure 4, page 42
The signal names of the parallel port connector	Table 20, page 44

1.7.3 Diskette Drive Controller

The I/O controller supports a single diskette drive that is compatible with the 82077 diskette drive controller and supports both PC-AT† and PS/2 modes.

NOTE

The I/O controller supports 1.2 MB, 3.5-inch diskette drives, but a special driver is required for this type of drive.

NLX FEATURE

The diskette drive interface signals are routed to the NLX card edge connector.

For information about	Refer to
The supported diskette drive capacities and sizes	Table 56, page 86
The signal names of the NLX card edge connector	The NLX form factor specification is available at: http://www.teleport.com/~nlx/spec/index.htm

1.7.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

NOTE

The keyboard and mouse can be plugged into either of the PS/2 connectors. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 4, page 42
The signal names of the keyboard and mouse connectors	Table 23, page 45

1.8 Graphics Subsystem

The graphics subsystem provides the following features:

- Intel 82810 GMCH DC-100 graphics support, including:
  - Integrated 2-D and 3-D graphics engines
  - Integrated hardware motion compression engine
  - Integrated 230 MHz DAC
- 4 MB of SDRAM display cache

A manufacturing option of this board replaces the GMCH component with the GMCH0 and removes the 4 MB SDRAM display cache.

Table 6 lists the refresh rates supported by graphics subsystem.

Table 6. Supported Graphics Refresh Rates

Resolution	Available Refresh Rates (Hz)
640 x 200 x 16 colors	70
640 x 350 x 16 colors	70
640 x 400 x 256 colors	60, 70, 75, 85
640 x 400 x 64 K colors	60, 70, 75, 85
640 x 400 x 16 M colors	70
640 x 480 x 16 colors	60, 72, 75, 85
640 x 480 x 256 colors	60, 70, 72, 75, 85
640 x 480 x 32 K colors	60, 75, 85
640 x 480 x 64 K colors	60, 70, 72, 75, 85
640 x 480 x 16 M colors	60, 70, 72, 75, 85
800 x 600 x 256 colors	60, 75, 85
800 x 600 x 32 K colors	60, 70, 72, 75, 85
800 x 600 x 64 K colors	60, 70, 72, 75, 85
800 x 600 x 16 M colors	60, 70, 72, 75, 85
1024 x 768 x 256 colors	60, 70, 75, 85
1024 x 768 x 32 K colors	60, 75, 85
1024 x 768 x 64 K colors	60, 70, 72, 75, 85
1024 x 768 x 16 M colors	60, 70, 72, 75, 85
1056 x 800 x 16 colors	70
1280 x 1024 x 256 colors	60, 70, 72, 75, 85
1280 x 1024 x 32 K colors	60, 75, 85
1280 x 1024 x 64 K colors	60, 70, 72, 75
1280 x 1024 x 16 M colors	60, 70, 72, 75, 85

For information about	Refer to
Obtaining graphics software and utilities	http://support.intel.com/support/motherboards/desktop

1.9 Audio Subsystem

The board includes an Audio Codec ’97 (AC ’97) compatible audio subsystem consisting of these devices:

- Intel 82801AA ICH (AC link output)
- Analog Devices ADI 1881 analog codec

Features of the audio subsystem include:

- Independent channels for PCM in, PCM out, and Mic in
- 16-bit stereo I/O up to 48 kHz
- Multiple sample rates

For information about	Refer to
Obtaining audio software and utilities	http://support.intel.com/support/motherboards/desktop

1.9.1 ADI 1881 Analog Codec

The ADI 1881 is a fully AC ’97 compliant codec. The codec's features include:

- 16-bit stereo full-duplex codec
- High quality CD input with ground sense
- Stereo line level output
- Power management support
- Full duplex variable sampling rate (7 kHz to 48 kHz) with 1 Hz resolution
- Phat† Stereo 3-D stereo enhancement

1.9.2 Audio Connectors

The audio connectors, located on the back panel, include the following:

- Line out
- Mic in

Other audio signals are accessible through an NLX riser with a supplemental connector.

For information about	Refer to
The location of the audio connectors	Figure 4, page 42
The signal names of the Line out connector	Table 25, page 45
The signal names of the Mic in connector	Table 26, page 45
Audio signals routed to the NLX supplemental connector	Table 33, page 52

NOTE

Some of the audio connectors are optional and are not installed on all versions of the board.

1.10 LAN Subsystem (Optional)

The Intel 82559 Fast Ethernet Wired for Management (WfM) PCI LAN subsystem provides both 10Base-T and 100Base-TX connectivity. Features include:

- 32-bit, 33 MHz direct bus mastering on the PCI bus
- Shared memory structure in the host memory that copies data directly to/from host memory
- 10Base-T and 100Base-TX capability using a single RJ-45 connector with connection and activity status LEDs
- IEEE 802.3u Auto-Negotiation for the fastest available connection
- Jumperless configuration; the LAN subsystem is completely software-configurable

For information about	Refer to
The WfM specification	Table 3, page 14

1.10.1 Intel® 82559 PCI LAN Controller

The Intel 82559 PCI LAN controller's features include:

- CSMA/CD Protocol Engine
- PCI bus interface
- DMA engine for movement of commands, status, and network data across the PCI bus
- Integrated physical layer interface, including:
  - Complete functionality necessary for the 10Base-T and 100Base-TX network interfaces; when in 10 Mbit/sec mode, the interface drives the cable directly
  - A complete set of Media Independent Interface (MII) management registers for control and status reporting
  - 802.3u Auto-Negotiation for automatically establishing the best operating mode when connected to other 10Base-T or 100Base-TX devices, whether half- or full-duplex capable
- Integrated power management features, including:
  - Support for APM
  - Support for Wake on LAN† technology

For information about	Refer to
The LAN subsystem's PCI specification compliance	Table 3, page 14

1.10.2 LAN Subsystem Software

The Intel 82559 Fast Ethernet WfM PCI LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	http://support.intel.com/support/motherboards/desktop

1.10.3 RJ-45 LAN Connector LEDs

Two LEDs are built into the RJ-45 LAN connector. Table 7 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 7. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	10 Mbit/sec speed is selected
	On	100 Mbit/sec speed is selected
Yellow	Off	LAN link is not established
	On (steady state)	LAN link is established
	On (brighter and pulsing)	The computer is communicating with another computer on the LAN

1.11 Hardware Management Features

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Hardware monitor component
- Alert on LAN 2 component

For information about	Refer to
The WfM specification	Table 3, page 14

1.11.1 Hardware Monitor Component (Optional)

The Analog Devices ADM1025 hardware monitor component provides low-cost instrumentation capabilities. The features of the component include:

- Internal ambient temperature sensing
- Remote thermal diode sensing for direct monitoring of processor temperature
- Power supply monitoring (+12, +5, +3.3, +3.3 VSB, +2.5, V_{CCP}) to detect levels above or below acceptable values
- SMBus interface

The hardware monitor component's SMBus address is 5A.

For information about	Refer to
Analog Devices ADM1025 component	http://www.analog.com

1.11.2 Alert on LAN 2 Component (Optional)

The optional alert on LAN 2 component is a companion device to the 82559 LAN controller. Together, the two devices provide a management interface between a remote console (or management server) and the client system monitoring instrumentation (the ICH and/or the hardware monitor component). The functions of the alert on LAN 2 component include:

- Sends alert (SOS), heartbeat, or pong (ping response) packets to the 82559 LAN controller
- Receives specially filtered packets needed for advanced power management modes such as reset, power-up, or power-down
- Senses missing processor (via slot signal) and sends alert
- Supports system management interrupt (SMI#)
- Senses operating system lockup, system hang, and failure to boot

1.12 Power Management Features

Power management is implemented at several levels, including:

- Software support:
  - — Advanced Power Management (APM)
  - — Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - — Power connector
  - — Fan connectors
  - — Wake on LAN technology
  - — Instantly Available Power Managed PC technology (IAPC)
  - — Wake on Ring
  - — Resume on Ring

1.12.1 Software Support

The software support for power management includes:

- APM
- ACPI

If the board is used with an ACPI-aware operating system, the BIOS can provide ACPI support. Otherwise, it defaults to APM support.

1.12.1.1 APM

APM makes it possible for the computer to enter an energy-saving standby mode. The standby mode can be initiated in the following ways:

- Time-out period specified in the BIOS Setup program
- Suspend/resume switch connected to the front panel sleep connector
- From the operating system, such as the Suspend menu item in Windows† 95

In standby mode, the board can reduce power consumption by spinning down hard drives, and reducing power to or turning off VESA† DPMS-compliant monitors. Power management mode can be enabled or disabled in the BIOS Setup program.

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default, but the operating system must support an APM driver for the power management features to work. For example, Windows 95 supports the power management features upon detecting that APM is enabled in the BIOS.

For information about	Refer to
Enabling or disabling power management in the BIOS Setup program	Section 4.6, page 89
The board's compliance level with APM	Table 3, page 14

1.12.1.2 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires the support of an operating system that provides full ACPI functionality. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM functionality normally contained in the BIOS.
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives.
- Methods for achieving less than 30-watt system operation in the Power-on Suspend sleeping state, and less than 5-watt system operation in the Suspend-to-Disk sleeping state.
- A Soft-off feature that enables the operating system to power-off the computer.
- Support for multiple wake-up events (see Table 10 on page 32).
- Support for a front panel power and sleep-mode switch. Table 8 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 8. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI G2/S5 state)	Less than four seconds	Power on
Off (ACPI G2/S5 state)	More than four seconds	Remains off
On (ACPI G0 state)	Less than four seconds	Soft off/Suspend
On (ACPI G0 state)	More than four seconds	Fail safe power off
Sleep (ACPI G1 state)	Less than four seconds	Wake up
Sleep (ACPI G1 state)	More than four seconds	Power off

For information about	Refer to
The board's compliance level with ACPI	Table 3, page 14

1.12.1.2.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 9 lists the power states supported by the board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 9. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power*
G0 - working state.	S0 - working.	C0 - working.	D0 - working state.	Full power > 60 W.
G1 - sleeping state.	S1 - CPU stopped.	C1 - stop grant.	D1, D2, D3- device specification specific.	5 W < power < 30 W.
G1 - sleeping state.	S3 - Suspend-to-RAM. Context saved to RAM.	No power.	D3 - no power except for wake up logic.	Power < 5 W**.
G2/S5.	S5 - Soft off. Context not saved. Cold boot is required.	No power.	D3 - no power except for wake up logic.	Power < 5 W**.
G3 - mechanical off. AC power is disconnected from the computer.	No power to the system.	No power.	D3 - no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

* Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.

** Dependent on the standby power consumption of wake-up devices used in the system.

1.12.1.2.2 Wake Up Devices and Events

Table 10 lists the devices or specific events that can wake the computer from specific states.

Table 10. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S3, S5
RTC alarm	S1, S3
LAN	S1, S3
Modem	S1, S3
IR command	S1
USB	S1, S3
PS/2 keyboard	S1, S3
PS/2 mouse	S1

1.12.1.2.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug-and-Play device enumeration and configuration. ACPI is used only to enumerate and configure board devices that do not have other hardware standards for enumeration and configuration. PCI devices on the board, for example, are not enumerated by ACPI.

1.12.2 Hardware Support

CAUTION

If Wake on LAN and Instantly Available technology features are used, ensure that the power supply provides adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.12.2 on page 59 for additional information.

The board provides several hardware features that support power management, including:

- Power connector
- Fan connectors
- Wake on LAN technology
- Instantly Available technology
- Wake on Ring
- Resume on Ring

Wake on Ring and Resume on Ring enable telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) and the power management mode being used (APM or ACPI).

NOTE

The use of Wake on Ring and Resume on Ring technologies from an ACPI state requires the support of an operating system that provides full ACPI functionality.

1.12.2.1 Power Connector

When used with an NLX-compliant power supply that supports remote power-on/off, the board can turn off the system power through software control. To enable soft-off control in software, advanced power management must be enabled in the BIOS Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

NLX FEATURE

The board does not have a power connector. Power is routed to the board from an NLX riser card.

For information about	Refer to
The signal names of the NLX card edge connector	NLX form factor specification, available at: http://www.teleport.com/~nlx/spec/index.htm

1.12.2.2 Fan Connectors

The board has two fan connectors, one of which is a manufacturing option. The functions of these connectors are described in Table 11.

Table 11. Fan Connector Descriptions

Connector	Function
Processor fan	Provides +12 V DC for a processor fan or active fan heatsink.
System fan (optional)	Provides +12 V DC for a system or chassis fan. The fan voltage can be switched on or off, depending on the power management state of the computer.

For information about	Refer to
The location of the fan connectors	Figure 4, page 42
The signal names of the fan connectors	Section 2.8, page 42

1.12.2.3 Wake on LAN Technology

CAUTION

For Wake on LAN technology, the 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.12.2 on page 59 for additional information.

Wake on LAN technology enables remote wakeup of the computer through a network. The LAN subsystem, whether onboard or as a PCI bus network adapter, monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet† Frame, the LAN subsystem asserts a wakeup signal that powers-up the computer. The board supports Wake on LAN technology through the PCI bus PME# signal.

1.12.2.4 Instantly Available Technology

⚠ CAUTION

For Instantly Available technology, the 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.12.2 on page 59 for additional information.

Instantly Available technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off. When signaled by a wake up device or event, the system quickly returns to its last known wake state. Table 10 on page 32 lists the devices and events that can wake the computer from the S3 state.

The board supports the *PCI Bus Power Management Specification*. For information on the versions of these specifications, see Section 1.3. Add-in boards that also support these specifications can participate in power management and can be used to wake the computer.

1.12.2.5 Wake on Ring

The operation of Wake on Ring can be summarized as follows:

- Powers up the computer from either the APM soft-off mode or the ACPI S5 state
- Requires two calls to access the computer:
  - — First call restores the computer
  - — Second call enables access (when the appropriate software is loaded)
- Detects incoming call differently for external as opposed to internal modems:
  - — For external modems, hardware on the board monitors the ring indicator (RI) input of serial port A (serial port B does not support this feature)
  - — For internal modems, a cable must be routed from the modem to a Wake on Ring connector on the NLX riser (if supported by the riser)

1.12.2.6 Resume on Ring

The operation of Resume-on-Ring can be summarized as follows:

- Resumes operation from either the APM sleep mode or the ACPI S1 state
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems; does not use the Wake on Ring connector
- Requires that the modem interrupt be unmasked for correct operation

2 Technical Reference

What This Chapter Contains

2.1 Introduction

Sections 2.2 – 2.6 contain several standalone tables. Table 12 describes the system memory map, Table 13 describes the DMA channels, Table 14 describes the I/O map, Table 15 describes the PCI configuration space map, and Table 16 describes the interrupts. The remaining sections in this chapter are introduced by text found below their respective section headings.

2.2 Memory Map

Table 12. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K – 524288 K	100000 – 1FFFFFFF	511 MB	Extended memory
960 K – 1024 K	F0000 – FFFFF	64 KB	Runtime BIOS
896 K – 960 K	E0000 – EFFFF	64 KB	Reserved
800 K – 896 K	C8000 – DFFFF	96 KB	Available high DOS memory (open to ISA bus and PCI bus)
640 K – 800 K	A0000 – C7FFF	160 KB	Video memory and BIOS
639 K – 640 K	9FC00 – 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K – 639 K	80000 – 9FBFF	127 KB	Extended conventional memory
0 K – 512 K	00000 – 7FFFF	512 KB	Conventional memory

2.3 DMA Channels

Table 13. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Audio
1	8 or 16 bits	Audio/parallel port
2	8 or 16 bits	Diskette Drive
3	8 or 16 bits	Parallel port (for ECP or EPP)/audio
4		Reserved – cascade channel
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.4 I/O Map

Table 14. I/O Map

Address (hex)	Size	Description
0000 – 000F	16 bytes	DMA Controller
0020 – 0021	2 bytes	Programmable Interrupt Control (PIC)
0040 – 0043	4 bytes	System Timer
0060	1 byte	Keyboard controller byte – reset IRQ
0061	1 byte	System Speaker
0064	1 byte	Keyboard controller, CMD/STAT byte
0070 – 0071	2 bytes	System CMOS / Real Time Clock
0072 – 0073	2 bytes	System CMOS
0080 – 008F	16 bytes	DMA Controller
0092	1 byte	Fast A20 and PIC
00A0 – 00A1	2 bytes	PIC
00B2 – 00B3	2 bytes	APM Control
00C0 – 00DF	32 bytes	DMA
00F0	1 byte	Numeric data processor
0170 – 0177	8 bytes	Secondary IDE channel
01F0 – 01F7	8 bytes	Primary IDE channel
0228 – 022F[1]	8 bytes	LPT3
0278 – 027F[1]	8 bytes	LPT2
02E8 – 02EF[1]	8 bytes	COM4/video (8514A)
02F8 – 02FF[1]	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 – 037F	8 bytes	LPT 1
03B0 – 03BB	12 bytes	Intel 82810 – DC100 Graphics/Memory Controller Hub (GMCH)
03C0 – 03DF	32 bytes	Intel 82810 – Graphics/Memory Controller Hub (GMCH)
03E8 – 03EF	8 bytes	COM3
03F0 – 03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F8 – 03FF	8 bytes	COM1
04D0 – 04D1	2 bytes	Edge/level triggered PIC

continued

Table 14. I/O Map (continued)

Address (hex)	Size	Description
LPTn + 400h	8 bytes	ECP port, LPTn base address + 400h
0CF8 – 0CFB[2]	4 bytes	PCI configuration address register
0CF9[3]	1 byte	Turbo and reset control register
0CFC – 0CFF	4 bytes	PCI configuration data register
FFA0 – FFA7	8 bytes	Primary bus master IDE registers
FFA8 – FFAF	8 bytes	Secondary bus master IDE registers
96 contiguous bytes starting on a 128-byte divisible boundary		ICH (ACPI + TCO (Total Cost of Ownership))
64 contiguous bytes starting on a 64-byte divisible boundary		Board resource
256 contiguous bytes starting on a 256-byte divisible boundary		ICH Audio Mixer
64 contiguous bytes starting on a 64-byte divisible boundary		ICH Audio Bus Mixer
32 contiguous bytes starting on a 32-byte divisible boundary		ICH (USB)
16 contiguous bytes starting on a 16-byte divisible boundary		ICH (SMB)
4096 contiguous bytes starting on a 4096-byte divisible boundary		Intel 82810AA PCI Bridge
32 contiguous bytes starting on a 32-byte divisible boundary		Intel 82559 LAN Controller
96 contiguous bytes starting on a 128-byte divisible boundary		LPC47B272 PME Status

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

NOTE

Some additional I/O addresses are not available due to ICH addresses aliasing. For information about ICH addressing, refer to Intel web site at:

http://developer.intel.com/design/chipsets/datashts/

2.5 PCI Configuration Space Map

Table 15. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82810 component
00	01	00	Graphics controller of Intel 82810 component
00	1E	00	Hub link to PCI bridge
00	1F	00	PCI-to-LPC bridge
00	1F	01	IDE controller
00	1F	02	USB controller #1
00	1F	03	SMBus controller
00	1F	04	Reserved
00	1F	05	AC ’97 audio controller
00	1F	06	AC ’97 modem controller
01	01	00	Intel 82559 PCI LAN controller
01	07 (Note)	00	PCI slot 5
01	09 (Note)	00	PCI slot 4
01	0B (Note)	00	PCI slot 3
01	0D (Note)	00	PCI slot 2
01	0F (Note)	00	PCI slot 1

Note: As recommended by the NLX specification

2.6 Interrupts

Table 16. Interrupts

IRQ	System Resource
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard Buffer Full
2	Reserved, Cascade Interrupt From Slave PIC
3	COM2*
4	COM1*
5	LPT2 (Plug and Play option)/Audio/User available
6	Diskette Drive
7	LPT1*
8	Real Time Clock
9	Reserved for ICH system management bus
10	User available
11	Windows Sound System*/User available
12	Onboard Mouse Port (if present, else user available)
13	Reserved, Math Coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH PCI-to-ISA bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the board and therefore share the same interrupt. Table 17 lists the PIRQ signals and shows how the signals are routed to onboard PCI interrupt sources. PIRQs are routed to the NLX riser card edge connector for use in riser card PCI slots.

Table 17. PCI Interrupt Routing Map

ICH PIRQ Signal Name	PCI Slot 1 (see note below)	PCI Slot 2 (see note below)	PCI LAN Controller
PIRQA	INTA	INTD	
PIRQB	INTB	INTA	
PIRQC	INTC	INTB	INTC
PIRQD	INTD	INTC	

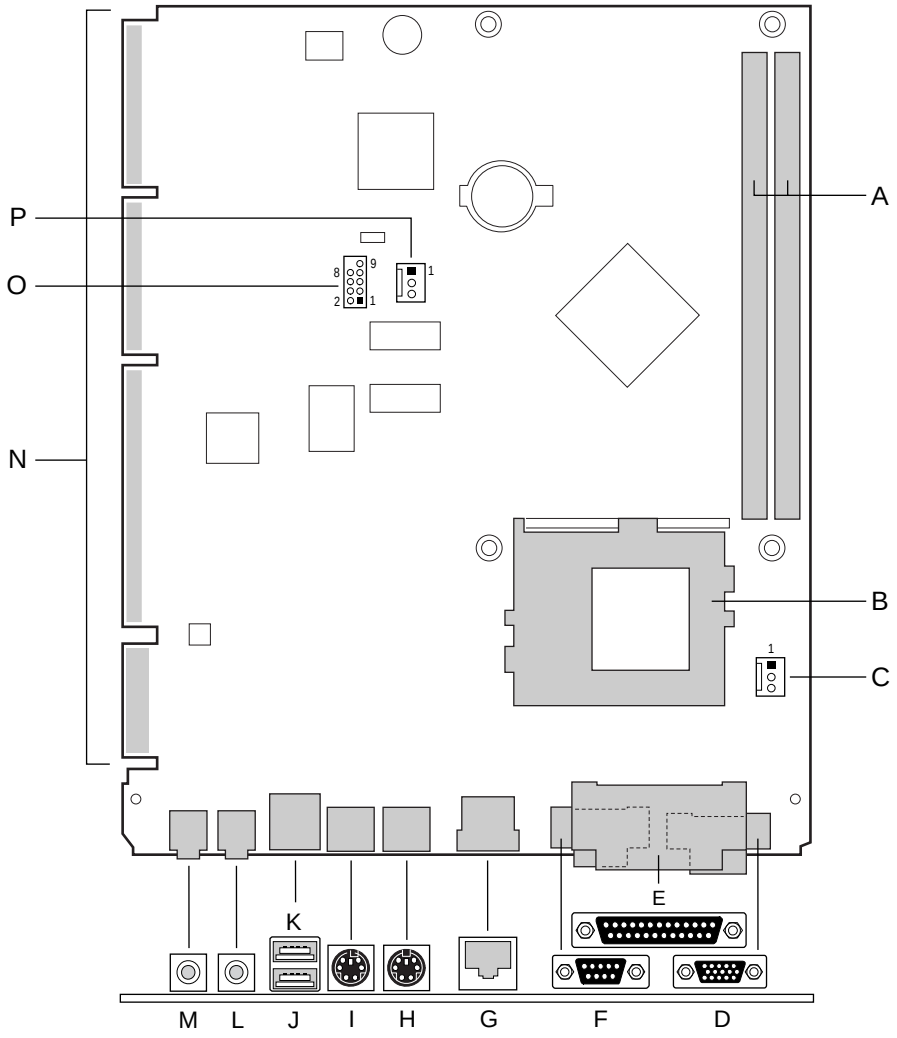
Note: The PCI slots referred to in this table are PCI slots on the NLX riser.

NOTE

The ICH can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 10, 11, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

2.8 Connectors

Figure 4 shows the location of the board connectors.



A	DIMM sockets	I	PS/2 keyboard or mouse (see Table 23)
B	Processor socket	J	USB port 1 (see Table 24)
C	Processor fan (see Table 18)	K	USB port 0 (see Table 24)
D	VGA port (see Table 19)	L	Audio line out (see Table 25)
E	Parallel port (see Table 20)	M	Mic in (see Table 26)
F	Serial port A (see Table 21)	N	NLX riser card edge (see Section 2.9)
G	RJ-45 LAN (see Table 22)	O	Serial port B (see Table 27)
H	PS/2 keyboard or mouse (see Table 23)	P	System fan (optional) (see Table 28)

Figure 4. Board Connectors

CAUTION

Only the back panel connectors of this board have overcurrent protection. The internal board connectors are not overcurrent protected, and should connect only to devices inside the computer chassis, such as fans and internal peripherals. Do not use these connectors for powering-up devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality may occur if passive (non-amplified) speakers are connected to this output.

Table 18. Processor Fan Connector (J1H1)

Pin	Signal Name
1	Ground
2	FANPWR
3	FAN1_TACH

Table 19. VGA Port Connector

Pin	Signal Name
1	Red
2	Green
3	Blue
4	No connect
5	Ground
6	Ground
7	Ground
8	Ground
9	Fused VCC
10	Ground
11	No connect
12	MONID1
13	HSYNC
14	VSYNC
15	MONID2

Table 20. Parallel Port Connector

Pin	Standard Signal Name	ECP Signal Name	EPP Signal Name
1	STROBE#	STROBE#	WRITE#
2	PD0	PD0	PD0
3	PD1	PD1	PD1
4	PD2	PD2	PD2
5	PD3	PD3	PD3
6	PD4	PD4	PD4
7	PD5	PD5	PD5
8	PD6	PD6	PD6
9	PD7	PD7	PD7
10	ACK#	ACK#	INTR
11	BUSY	BUSY#, PERIPHACK	WAIT#
12	PERROR	PE, ACKREVERSE#	PE
13	SELECT	SELECT	SELECT
14	AUDOFD#	AUDOFD#, HOSTACK	DATASTB#
15	FAULT#	FAULT#, PERIPHREQST#	FAULT#
16	INIT#	INIT#, REVERSERQST#	RESET#
17	SLCTIN#	SLCTIN#	ADDRSTB#
18 - 25	GND	GND	GND

Table 21. Serial Port A Connector

Pin	Signal Name	Pin	Signal Name
1	DCD (Data Carrier Detect)	6	DSR (Data Set Ready)
2	SIN# (Serial Data In)	7	RTS (Request to Send)
3	SOUT# (Serial Data Out)	8	CTS (Clear to Send)
4	DTR (Data Terminal Ready)	9	RI (Ring Indicator)
5	Ground		

Table 22. RJ-45 LAN Connector

Pin	Signal Name
1	TX+
2	TX-
3	RX+
4	Floating plane termination
5	Floating plane termination
6	RX-
7	Floating plane termination
8	Floating plane termination

Table 23. PS/2 Keyboard/Mouse Connectors

Pin	Signal Name
1	Data
2	Not connected
3	Ground
4	Fused +5 V
5	Clock
6	Not connected

Table 24. USB Port Connectors

USB Port 0	Pin	Signal Name	USB Port 1	Pin	Signal Name
	1	+5 V (fused)		1	+5 V (fused)
	2	USBP0#		2	USBP1#
	3	USBP0		3	USBP1
	4	Ground		4	Ground

Table 25. Audio Line-Out Connector

Pin	Signal Name
Tip	Audio left out
Ring	Audio right out
Sleeve	Ground

Table 26. Mic-In Connector

Pin	Signal Name
Tip	Mono in
Ring	Mic bias voltage
Sleeve	Ground

Table 27. Serial Port B Connector (J6D2)

Pin	Signal Name	Pin	Signal Name
1	DCD (Data Carrier Detect)	2	DSR (Data Set Ready)
3	SIN# (Serial Data In)	4	RTS (Request to Send)
5	SOUT# (Serial Data Out)	6	CTS (Clear to Send)
7	DTR (Data Terminal Ready)	8	RI (Ring Indicator)
9	Ground		

Table 28. System Fan Connector (J5D1)

Pin	Signal Name
1	Ground
2	FAN_CTRL
3	NC

2.9 NLX Card Edge Connector

The NLX riser connector on the board consists of a 340-position (2 x 170) and a supplemental 26 position (2 x 13) gold finger contact. All edge connector pin definitions are defined in the NLX specification, version 1.2.

According to the NLX specification, the board edge connector provides the following:

- PCI signals (the board supports up to four PCI devices)
- Two IDE channels
- One diskette drive interface
- Miscellaneous front panel signals
- Power connection for the board

See Section 1.3 for information about the NLX specification.

Table 30, Table 31, and Table 32 specify the pinouts located on the primary connector; Table 33 specifies the pinouts located on the supplemental connector. All edge connector pin definitions are defined in the NLX specification, version 1.2.

The ICH supports a total of five PCI bus masters. Table 29 tells how many PCI bus masters are available for the NLX riser based on the board configuration.

Table 29. Available PCI Bus Masters

If the board has these PCI bus masters…	The maximum number of PCI bus masters available to an NLX riser card is…	These are the REQ# / GNT# signal pairs routed to the NLX riser card…
ICH only (no onboard PCI LAN)	5	REQ# / GNT# 0, 1, 2, 3, and 4
ICH + onboard PCI LAN	4	REQ# / GNT# 0, 1, 2, and 3

NOTE

If the NLX riser has more PCI bus connectors than there are REQ# / GNT# signal pairs routed to the riser, not all of the PCI bus connectors on the riser will support bus mastering. For example, if the board has only REQ# / GNT# signal pairs 0 and 1 routed to the NLX riser connector and the riser has three PCI bus connectors, the connector tied to REQ# / GNT# signal pair 2 will not support bus mastering.

NOTE

ISA bus signals (as defined in the NLX Riser specification) are not provided on the SU810 board at the NLX riser card edge connector.

Table 30. PCI Segment, Riser Interconnect

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A1	-12V	PWR	NA	NA	B1	NC	AUDIO	O	NA
A2	REQ4#	PCI	I	RIS	B2	+12V	PWR	NA	NA
A3	+12V	PWR	NA	NA	B3	PCSPKR_LFT	AUDIO	O	NA
A4	GNT4#	PCI	O	RIS	B4	+12V	PWR	NA	NA
A5	3.3VDC	PWR	NA	NA	B5	PCICLK0	PCI	O	MB
A6	PCIINT3#	PCI	I	RIS	B6	GND	PWR	NA	NA
A7	3.3VDC	PWR	NA	NA	B7	PCICLK1	PCI	O	MB
A8	PCIINT0#	PCI	I	RIS	B8	SER_IRQ	MISC	I/O	MB
A9	PCIINT1#	PCI	I	RIS	B9	PCIINT2#	PCI	I	RIS
A10	PCICLK2	PCI	O	MB	B10	3.3VDC	PWR	NA	NA
A11	3.3VDC	PWR	NA	NA	B11	PCICLK3	PCI	O	MB
A12	PCI_RST#	PCI	O	MB	B12	GND	PWR	NA	NA
A13	GNT0#	PCI	O	RIS	B13	GNT3#	PCI	O	RIS
A14	PCICLK4	PCI	O	MB	B14	3.3VDC	PWR	NA	NA
A15	GND	PWR	NA	NA	B15	GNT2#	PCI	O	RIS
A16	GNT1#	PCI	O	RIS	B16	AD[31]	PCI	I/O	RIS
A17	3.3VDC	PWR	NA	NA	B17	REQ0#	PCI	I	RIS
A18	REQ2#	PCI	I	RIS	B18	GND	PWR	NA	NA
A19	REQ3#	PCI	I	RIS	B19	AD[29]	PCI	I/O	RIS
A20	AD[30]	PCI	I/O	RIS	B20	AD[28]	PCI	I/O	RIS
A21	GND	PWR	NA	NA	B21	AD[26]	PCI	I/O	RIS
A22	AD[25]	PCI	I/O	RIS	B22	3.3VDC	PWR	NA	NA
A23	REQ1#	PCI	I	RIS	B23	AD[24]	PCI	I/O	RIS
A24	AD[27]	PCI	I/O	RIS	B24	C/BE[3]#	PCI	I/O	RIS
A25	3.3VDC	PWR	NA	NA	B25	AD[22]	PCI	I/O	RIS
A26	AD[23]	PCI	I/O	RIS	B26	GND	PWR	NA	NA
A27	AD[20]	PCI	I/O	RIS	B27	AD[21]	PCI	I/O	RIS
A28	AD[18]	PCI	I/O	RIS	B28	AD[19]	PCI	I/O	RIS
A29	GND	PWR	NA	NA	B29	AD[16]	PCI	I/O	RIS
A30	AD[17]	PCI	I/O	RIS	B30	3.3VDC	PWR	NA	NA
A31	IRDY#	PCI	I/O	RIS	B31	C/BE[2]#	PCI	I/O	RIS
A32	DEVSEL#	PCI	I/O	RIS	B32	FRAME#	PCI	I/O	RIS
A33	3.3VDC	PWR	NA	NA	B33	TRDY#	PCI	I/O	RIS
A34	STOP#	PCI	I/O	RIS	B34	GND	PWR	NA	NA
A35	PERR#	PCI	I/O	RIS	B35	SDONE	PCI	I/O	RIS
A36	SERR#	PCI	I/O	RIS	B36	LOCK#	PCI	I/O	RIS

continued

Table 30. PCI Segment, Riser Interconnect (continued)

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A37	GND	PWR	NA	NA	B37	SBO#	PCI	I/O	RIS
A38	C/BE[1]#	PCI	I/O	RIS	B38	3.3VDC	PWR	NA	NA
A39	AD[13]	PCI‘	I/O	RIS	B39	AD[15]	PCI	I/O	RIS
A40	AD[10]	PCI	I/O	RIS	B40	PAR	PCI	I/O	RIS
A41	GND	PWR	NA	NA	B41	AD[14]	PCI	I/O	RIS
A42	C/BE[0]#	PCI	I/O	RIS	B42	GND	PWR	NA	NA
A43	AD[00]	PCI	I/O	RIS	B43	AD[11]	PCI	I/O	RIS
A44	AD[06]	PCI	I/O	RIS	B44	AD[12]	PCI	I/O	RIS
A45	3.3VDC	PWR	NA	NA	B45	AD[09]	PCI	I/O	RIS
A46	AD[05]	PCI	I/O	RIS	B46	3.3VDC	PWR	NA	NA
A47	AD[01]	PCI	I/O	RIS	B47	AD[08]	PCI	I/O	RIS
A48	AD[03]	PCI	I/O	RIS	B48	AD[07]	PCI	I/O	RIS
A49	GND	PWR	NA	NA	B49	AD[04]	PCI	I/O	RIS
A50	AD[02]	PCI	I/O	RIS	B50	GND	PWR	NA	NA
A51	5VDC	PWR	NA	NA	B51	PCI_PM#	PCI	I/O	MB

Note: Pin B8 (SER_IRQ) needs to be connected to the output of the IRQ Serializer.

I/O Column Definitions Relative to the Board:
O = Output from board to riser
I = Input from riser to board
NA = Not an input or output signal
Termination Column Definitions:
MB = Termination/Pullup/Pulldown/debounce is on board
RIS = Termination/Pullup/Pulldown is on riser card
NA = Not on board or riser

Table 31. ISA Segment, Riser Interconnect

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A57	5VDC	PWR	NA	NA	B75	DMA_66 Detect Primary	ISA	I/O	MB
A65	GND	PWR	NA	NA	B78	GND	PWR	NA	NA
A73	5VDC	PWR	NA	NA	B84	NOGO	ISA	I/O	MB
A78	DMA_66 Detect Secondary	ISA	I/O	MB	B86	LAN_present/ disable	ISA	I/O	MB
A81	GND	PWR	NA	NA	B87	REQ[A] #	PCI	I	RIS
A89	GND	PWR	NA	NA	B88	GNT[A]	PCI	O	RIS
A97	5VDC	PWR	NA	NA	B89	P_REQ5#	PCI	I	RIS
B52	5VDC	PWR	NA	NA	B90	P_GNT5#	PCI	O	RIS
B66	GND	PWR	NA	NA	B96	5VDC	PWR	NA	NA
B68	5VDC	PWR	NA	NA	B101	GND	PWR	NA	NA

I/O Column Definitions Relative to the Board:
O = Output from board to riser
I = Input from riser to board
NA = Not an input or output signal
Termination Column Definitions:
MB = Termination/Pullup/Pulldown/debounce is on the board
RIS = Termination/Pullup/Pulldown is on riser card
NA = Not on board or riser

NOTE

In Table 31 above, any signal from A52-A101 and B52-B101 that is not listed, is not connected.

Table 32. IDE, Floppy, and Front Panel Section, Riser Interconnect

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A102	IDEA_DD8	IDE	I/O	MB	B102	GND	PWR	NA	NA
A103	IDEA_RESET#	IDE	O	MB	B103	IDEA_DD7	IDE	I/O	MB
A104	IDEA_DD9	IDE	I/O	MB	B104	IDEA_DD6	IDE	I/O	MB
A105	5VDC	PWR	NA	NA	B105	IDEA_DD5	IDE	I/O	MB
A106	IDEA_DD4	IDE	I/O	MB	B106	IDEA_DD11	IDE	I/O	MB
A107	IDEA_DD10	IDE	I/O	MB	B107	IDEA_DD12	IDE	I/O	MB
A108	IDEA_DD3	IDE	I/O	MB	B108	GND	PWR	NA	NA
A109	IDEA_DD13	IDE	I/O	MB	B109	IDEA_DD14	IDE	I/O	MB
A110	IDEA_DD1	IDE	I/O	MB	B110	IDEA_DD2	IDE	I/O	MB
A111	GND	PWR	NA	NA	B111	IDEA_DD0	IDE	I/O	MB
A112	IDEA_DIOW#	IDE	O	MB	B112	IDEA_DD15	IDE	I/O	MB
A113	IDEA_DMARQ	IDE	I	MB	B113	IDEA_DIOR#	IDE	O	MB

continued

Table 32. IDE, Floppy, and Front Panel Section, Riser Interconnect (continued)

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A114	IDEA_IORDY	IDE	I	MB	B114	IDEA_CSEL	IDE	O	MB
A115	IDEA_DMACK#	IDE	O	MB	B115	IDEA_INTRQ	IDE	I	MB
A116	RESERVED	RES	NA	NA	B116	5VDC	PWR	NA	NA
A117	IDEA_DA2	IDE	O	MB	B117	IDEA_DA1	IDE	O	MB
A118	IDEA_CS0#	IDE	O	MB	B118	IDEA_DA0	IDE	O	MB
A119	5VDC	PWR	NA	NA	B119	IDEA_CS1#	IDE	O	MB
A120	NC	IDE	I	RIS	B120	IDEB_DD8	IDE	I/O	MB
A121	IDEB_RESET#	IDE	O	MB	B121	IDEB_DD7	IDE	I/O	MB
A122	IDEB_DD9	IDE	I/O	MB	B122	GND	PWR	NA	NA
A123	IDEB_DD6	IDE	I/O	MB	B123	IDEB_DD10	IDE	I/O	MB
A124	IDEB_DD5	IDE	I/O	MB	B124	5VDC	PWR	NA	NA
A125	IDEB_DD11	IDE	I/O	MB	B125	IDEB_DD4	IDE	I/O	MB
A126	IDEB_DD12	IDE	I/O	MB	B126	IDEB_DD3	IDE	I/O	MB
A127	GND	PWR	NA	NA	B127	IDEB_DD13	IDE	I/O	MB
A128	IDEB_DD2	IDE	I/O	MB	B128	IDEB_DD14	IDE	I/O	MB
A129	IDEB_DD15	IDE	I/O	MB	B129	IDEB_DD1	IDE	I/O	MB
A130	IDEB_DIOW#	IDE	I/O	MB	B130	IDEB_DD0	IDE	I/O	MB
A131	IDEB_DMARQ	IDE	I	MB	B131	IDEB_DIOR#	IDE	O	MB
A132	IDEB_IORDY	IDE	I	MB	B132	IDEB_CSEL	IDE	O	MB
A133	GND	PWR	NA	NA	B133	IDEB_INTRQ	IDE	I	MB
A134	IDEB_DMACK#	IDE	O	MB	B134	IDEB_DA1	IDE	O	MB
A135	3.3Vaux	PWR	NA	NA	B135	IDEB_DA2	IDE	O	MB
A136	IDEB_DA0	IDE	O	MB	B136	IDEB_CS1#	IDE	O	MB
A137	IDEB_CS0#	IDE	O	MB	B137	IDEB_DASP#	IDE	I	RIS
A138	DRV2#	FLOPPY	GND	NA	B138	GND	PWR	NA	NA
A139	5VDC	PWR	NA	NA	B139	DRATE0	FLOPPY	O	NA
A140	RESERVED	RES	NA	NA	B140	FDS1#	FLOPPY	O	NA
A141	DENSEL	FLOPPY	O	NA	B141	FDS0#	FLOPPY	O	NA
A142	FDME0#	FLOPPY	O	NA	B142	DIR#	FLOPPY	O	NA
A143	INDX#	FLOPPY	I	RIS	B143	NC	FLOPPY	I	NA
A144	FDME1#	FLOPPY	O	NA	B144	GND	PWR	NA	NA
A145	GND	PWR	NA	NA	B145	WRDATA#	FLOPPY	O	NA
A146	WE#	FLOPPY	O	NA	B146	TRK0#	FLOPPY	I	RIS
A147	STEP#	FLOPPY	O	NA	B147	NC	FLOPPY	I	NA
A148	WP#	FLOPPY	I	RIS	B148	RDDATA#	FLOPPY	I	RIS

continued

Table 32. IDE, Floppy, and Front Panel Section, Riser Interconnect (continued)

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A149	HDSEL#	FLOPPY	O	NA	B149	DSKCHG#	FLOPPY	I	RIS
A150	SDA	MISC	I/O	MB	B150	GND	PWR	NA	NA
A151	SCL	MISC	O	MB	B151	NC	MISC	I/O	NA
A152	FAN_TACH1	MISC	I	NA	B152	NC	MISC	I/O	NA
A153	NC	MISC	I	NA	B153	NC	MISC	I/O	NA
A154	NC	MISC	I	NA	B154	IRTX	MISC	I/O	NA
A155	FAN_CTL	MISC	I	NA	B155	IRRX	MISC	I/O	RIS
A156	5VDC	PWR	NA	NA	B156	FP_SLEEP	MISC	I	MB
A157	USB1/3_N	MISC	I/O	RIS	B157	FP_RST#	MISC	I	MB
A158	USB1/3_P	MISC	I/O	RIS	B158	GND	PWR	NA	NA
A159	USB1/3_OC#	MISC	I	RIS	B159	PWRLED#	MISC	O	RIS
A160	NC	MISC	I/O	RIS	B160	PWOK	PWR	I	NA
A161	NC	MISC	I/O	RIS	B161	SOFT_ON/OFF#	PWR	I	MB
A162	NC	MISC	I	RIS	B162	PS_ON#	PWR	O	NA
A163	GND	PWR	NA	NA	B163	LAN_WAKE	MISC	I	MB
A164	VBAT	MISC	O	RIS	B164	LAN_ACTVY_LED#	MISC	O	NA
A165	TAMP_DET#	MISC	I	MB	B165	MDM_WAKE#	MISC	I	MB
A166	MSG_WAIT_ LED#	MISC	O	RIS	B166	NC	PWR	I	NA
A167	NC	PWR	O	NA	B167	RESERVED	RES	NA	NA
A168	RESERVED	RES	NA	NA	B168	RESERVED	RES	NA	NA
A169	5V (standby)	PWR	I	NA	B169	RESERVED	RES	NA	NA
A170	3.3VSENSE	PWR	O	NA	B170	NC	PWR	NA	NA

I/O Column Definitions Relative to the Board:
- O = Output from board to riser
- I = Input from riser to board
- NA = Not an input or output signal

Termination Column Definitions:
- MB = Termination/Pullup/Pulldown/debounce is on the board
- RIS = Termination/Pullup/Pulldown is on riser card
- NA = Not on board or riser

Table 33. Signals, NLX Riser with Supplemental Connector

Pin	Signal Name	Type	I/O*	Description	Signal Type
X1	CD_IN_LT	AUDIO	I	CD-ROM Line-in left.	Analog 1 V RMS
X2	AGND	PWR	NA	Low-pass filtered ground for audio circuitry on the riser.	NA
X3	MIC_IN	AUDIO	I	Pre-amplified microphone input. Pre-amp circuitry to reside on riser or in microphone.	Analog 1 V RMS
X4	LINE_OUT_LT	AUDIO	O	Analog line out left.	Analog 1 V RMS
X5	FP_SPKR_EN	AUDIO	I	This signal indicates if headphones have been plugged into the front panel LINE OUT jack. The signal is connected to one of the wipers on the audio jack and is HIGH when the headphones are plugged into the front audio jack and LOW when they are not. The signal is pulled-low through a pull-down on the board (Typically 100 K).	TTL
X6	VOL_DN#**	AUDIO	I	Connects to Volume Down switch on front panel, appropriate pull-up resistor on the board. The board provides debounce protection and a pull-up resistor.	TTL
X7	GND	PWR	NA	Ground.	NA
X8	SMI#**	SYS	I	System Management Interrupt that is an input to the board.	open drain
X9	AC_SD_IN1	AC'97	I	Serial, time division, multiplexed, AC'97 input stream to the board from the codec on the riser (output from the codec).	TTL
X10	AC_SD_IN2 **	AC'97	I	Not supported by ICH.	TTL
X11	AC_SD_IN3 **	AC'97	I	Not supported by ICH.	TTL
X12	AGND	PWR	NA	Low-pass filtered ground for audio circuitry on the riser.	NA
X13	MODEM_MIC	AUDIO	O	Pre-amplified microphone mono output signal from board to telephony device.	Analog 1 V RMS
Y1	CD_IN_RT	AUDIO	I	CD-ROM Line-in right.	Analog 1 V RMS
Y2	CD_IN_GND	PWR	I	Isolated CD-ROM ground.	NA
Y3	AVCC	PWR	O	Clean power from the board to audio circuitry on the NLX riser; could be an isolated power source; 1.5 Ampere max. Limitation because of the connector / gold finger limitation.	5-9 V DC
Y4	LINE_OUT_RT	AUDIO	O	Analog line out right.	Analog 1 V RMS

continued

Table 33. Signals, NLX Riser with Supplemental Connector (continued)

Pin	Signal Name	Type	I/O *	Description	Signal Type
Y5	FP_MIC_EN	AUDIO	I	This signal indicates if a microphone has been plugged into the front panel MIC_IN jack. The signal is connected to a wiper on the MIC_IN jack and is LOW when the microphone is plugged in and HIGH when it is not. The signal is pulled-LOW through a pull-down on the board (Typically 100 K).	TTL
Y6	VOL_UP#**	AUDIO	I	Connects to Volume Up switch on front panel, appropriate pull-up resistor on the board. The board provides debounce protection and a pull-up resistor.	TTL
Y7	AC_RST#	AC'97	O	AC'97 master H/W reset.	TTL
Y8	AC_SD_IN0	AC'97	I	Serial, time division, multiplexed, AC'97 input stream to the board from the codec on the riser (output from the codec).	TTL
Y9	GROUND	PWR	NA	Digital (main board) ground plane.	NA
Y10	AC_SD_OUT	AC'97	O	Serial, time division, multiplexed, AC '97 output from the board to the codec on the riser (input to the codec)	TTL
Y11	AC_SYNC	AC'97	O	48 kHz fixed rate sync signal from the board to the codec on the riser.	TTL
Y12	AC_BIT_CLK	AC'97	I	12.288 MHz serial data clock.	TTL
Y13	MODEM_SPKR	AUDIO	O	Analog mono output signal from telephony device to board.	Analog 1 V RMS

* I/O column: relative to board, "O" = output, from board to riser; "I" = input, from riser to board.

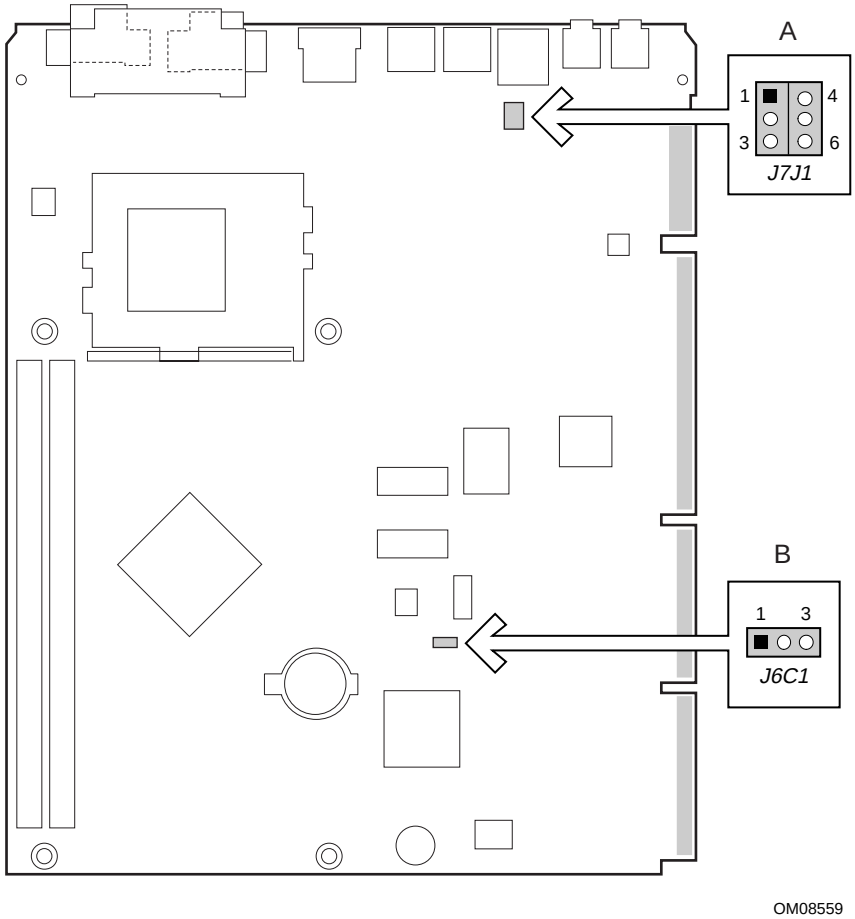
** These signals are not supported.

2.10 Jumper Blocks

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, damage to the board could occur.

The board has two jumper blocks. Figure 5 shows the location of the jumper blocks.



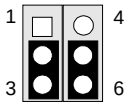
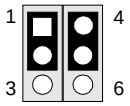
Item	Description	Reference Designator
A	USB port 0 routing jumper block (optional)	J7J1
B	BIOS setup configuration jumper block	J6C1

Figure 5. Location of the Jumper Blocks

2.10.1 USB Port 0 Routing Jumper Block (Optional)

This 6-pin jumper block routes the signals of USB port 0. Table 34 describes the jumper settings for USB port 0. Figure 4 on page 42 shows the location of USB port 0.

Table 34. USB Port 0 Routing Jumper Settings (J7J1)

Jumper Setting		Configuration
2-3 and 5-6		USB Port 0 signals are routed to the NLX riser
1-2 and 4-5		USB Port 0 signals are routed to the back panel

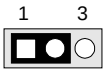
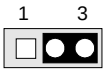
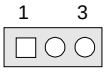
⌦ NLX FEATURE

Front panel routing for USB port 0 signals requires an NLX riser with a USB connector to access the port.

2.10.2 BIOS Setup Configuration Jumper Block

This 3-pin jumper block sets the BIOS Setup program's mode. Table 35 describes the jumper settings for the three modes: normal, configuration, and recovery.

Table 35. BIOS Setup Configuration Jumper Settings (J6C1)

Function/Mode	Jumper Setting	Configuration
Normal	1-2 	The BIOS uses current configuration information and passwords for booting.
Configure	2-3 	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None 	The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

For information about	Refer to
BIOS recovery	Section 3.6, page 70
How to access the BIOS Setup program	Section 4.1, page 75
The maintenance menu of the BIOS Setup program	Section 4.2, page 76

2.11 Mechanical Considerations

2.11.1 Form Factor

The board is designed to fit into a standard NLX form-factor chassis. The outer dimensions are 8.25 x 10.0 inches. Figure 6 shows the mechanical form factor, the I/O connector locations, and the mounting hole locations. They are in compliance with the *NLX Motherboard Specification* (see Section 6.2). Dimensions are shown in inches. For dimensions given to two decimal places, (X.XX) the tolerance is ±0.02 inches. For dimensions given to three decimal places (X.XXX), the tolerance is ±0.010 inches.

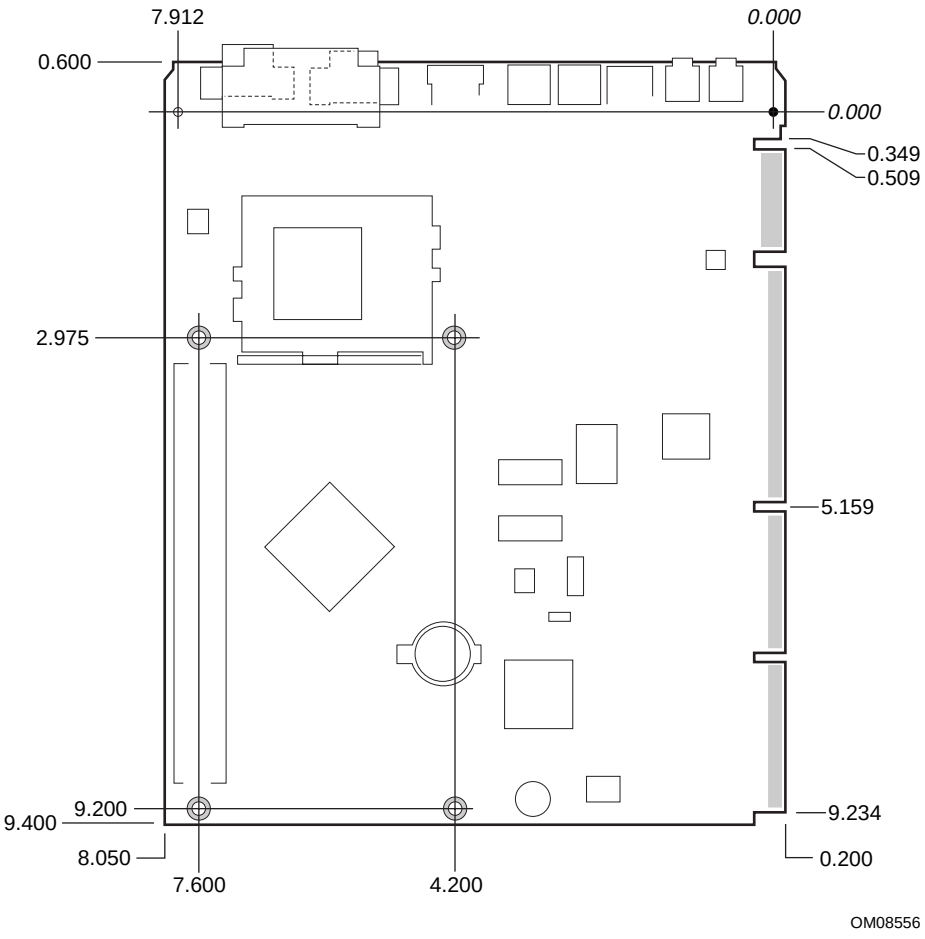


Figure 6. Board Dimensions

2.11.2 I/O Shield

The back panel I/O shield for the board must meet specific dimension and material requirements. Systems based on this board need the I/O shield to pass certification testing. Figure 7 shows the shield's critical dimensions in inches. The figure indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the *NLX Motherboard Specification.* See Section 1.3 on page 14 for information about the specification.

NOTE

A back panel I/O shield designed to be compliant with the NLX Motherboard Specification is available from Intel.

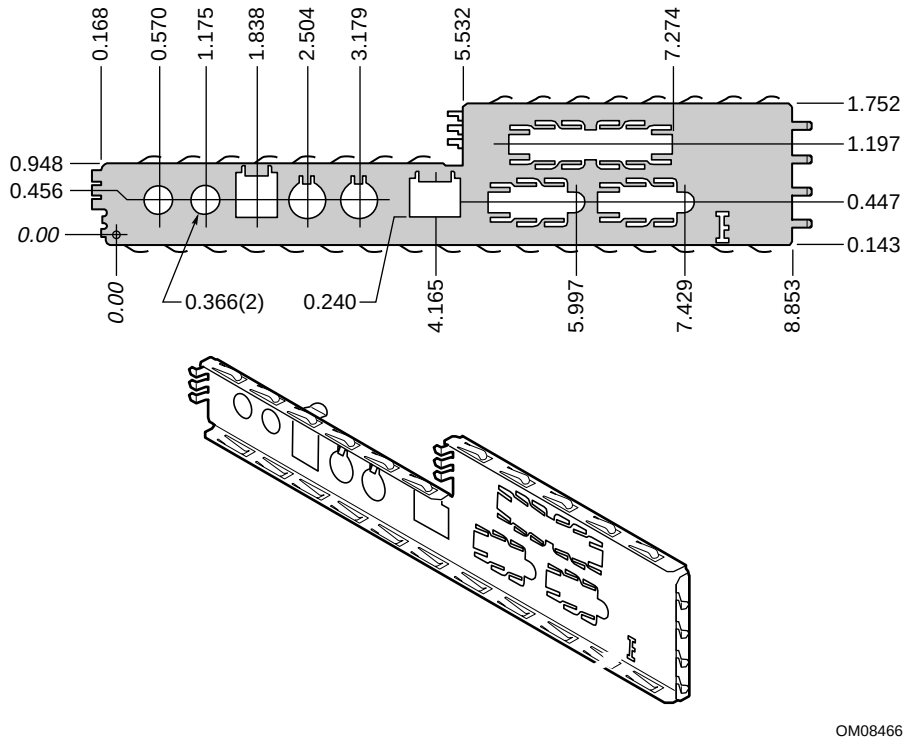


Figure 7. Back Panel I/O Shield Dimensions

2.12 Electrical Considerations

2.12.1 Power Consumption

Table 36 lists voltage and current specifications for a computer that contains the board and the following:

- 433 MHz Celeron processor with a 128 KB cache
- 64 MB SDRAM
- 3.5-inch diskette drive
- 2.1 GB IDE hard disk drive
- 8X IDE CD-ROM-drive

This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 98 desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with a typical 145 W power supply, nominal input voltage and frequency, with a true RMS wattmeter at the line input.

NOTE

Actual system power consumption depends upon system configuration. The power supply should comply with the recommendations found in the NLX Power Supply Recommendations document (see Table 3 on page 14 for specification information).

Table 36. Power Usage

		DC Amps at:				
Enabled APM Mode	**AC Watts**	**+3.3 V**	**+5 V**	**+12 V**	**-12 V**	**+5 VSB**
DOS prompt, power management disabled	46.9 W	1.29 A	2.94 A	0.19 A	0.02 A	0.04 A
Windows 98 desktop, power management disabled	47.0 W	1.31 A	2.26 A	0.21 A	0.01 A	0.03 A
Windows 98 desktop, APM enabled, in System Management Mode (SMM)	26.3 W	1.27 A	0.46 A	0.17 A	0.00 A	0.03 A

2.12.2 Standby Current Requirements

Table 37 lists the +5 V standby current consumed by the board itself. In a system that includes PCI 2.2 compliant add-in boards that can wake the system using the PME# signal, the power supply must be capable of providing the +5 V standby current that those boards require in addition to the standby current required by the board.

Table 37. Standby Current Usage

Configuration	+5 V Standby Current Required
Board with no onboard LAN	1.3 A
Board with onboard LAN	1.6 A

2.12.3 Fan Power Requirements

Table 38 lists the maximum DC voltage and current requirements for the system fan (fan 1) when the board is in the Sleep mode or Normal operating mode. Power consumption is independent of the operating system used and other variables.

Table 38. System Fan (Fan 1, J5D1) DC Power Requirements

Mode	Voltage	Maximum Current (Amps)
Sleep	+8 VDC	50 mA (current limited)
Normal	+12 VDC	50 mA (current limited)

For information about	Refer to
The location of the system fan connector	Figure 4, page 42
Signal names of the system fan connector	Table 28, page 45

2.12.4 Power Supply Considerations

CAUTION

The 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.12.2 on page 59 for additional information.

System integrators should refer to the power usage values listed in Table 36 and Table 37 when selecting a power supply for use with this board. The power supply must comply with the parameters listed in the *NLX Power Supply Recommendations* and *NLX Motherboard Specification* for the following:

- The potential relation between 3.3 V DC and +5 V DC power rails
- All timing parameters
- All voltage tolerances
- NLX 20-pin power connector
- Soft-Off support

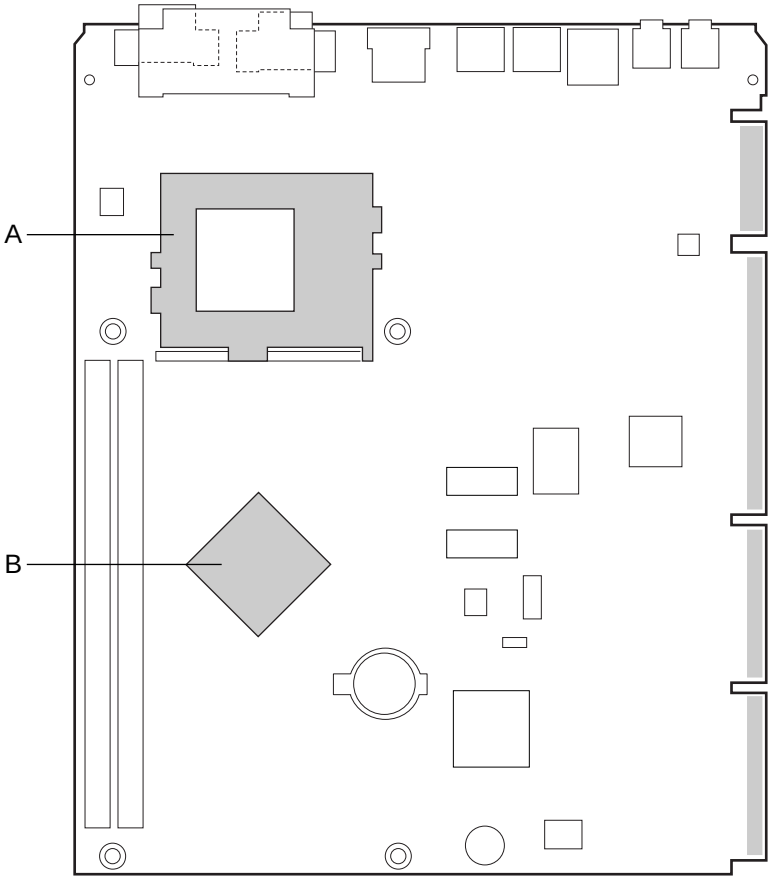
For information about	Refer to
NLX specifications and reference documents	Table 3, page 14

2.13 Thermal Considerations

CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5 °C to 10 °C could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.15.

Figure 8 shows the locations of the thermally sensitive components. Table 39 lists maximum component case temperatures for board components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the board.



A Processor
B Intel 82810 Graphics/Memory Controller Hub (GMCH)

Figure 8. Thermally Sensitive Components

Table 39. Thermal Considerations for Components

Component	Maximum Case Temperature	
Intel 82810 Graphics/Memory Controller Hub (GMCH)	55 °C	
Intel Celeron processor	300A MHz	85 °C
	333 MHz	85 °C
	366 MHz	85 °C
	400 MHz	85 °C
	433 MHz	85 °C
	466 MHz	70 °C
	500 MHz	70 °C

2.14 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 55 ºC.

Board MTBF: 218472.74 Hours.

2.15 Environmental

Table 40 lists the environmental specifications for the board.

Table 40. Board Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	30 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight	Free Fall (inches)	Velocity Change (inches/sec)
	<20 lbs.	36	167
	21-40 lbs.	30	152
	41-80 lbs.	24	136
	81-100 lbs.	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.16 Regulatory Compliance

This section describes the board's compliance with safety and EMC regulations.

2.16.1 Safety Regulations

Table 41 lists the safety regulations the board complies with when it is correctly installed in a compatible host system.

Table 41. Safety Regulations

Regulation	Title
UL 1950/CSA950, 3rd edition, Dated 07-28-95	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Community)
IEC 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

2.16.2 EMC Regulations

Table 42 lists the EMC regulations the board complies with when it is correctly installed in a compatible host system.

Table 42. EMC Regulations

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)
CISPR 22, 2nd Edition, 1993 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
VCCI Class B (ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
EN55022 (1994) (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN50082-1 (1992)	Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)
ICES-003 (1997)	Interference-Causing Equipment Standard, Digital Apparatus, Class B (Including CRC c.1374). (Canada)
AS/NZ 3548	Australian Communications Authority (ACA), Standard for Electromagnetic Compatibility.

2.16.3 Certification Markings

This printed circuit assembly has the following product certification markings:

- UL Joint Recognition Mark: Consists of small c followed by a stylized backward UR and followed by a small US (Component side).
- Manufacturer's recognition mark: Consists of a unique UL recognized manufacturer's logo, along with flammability rating (94V-0) (Solder side).
- UL File Number for boards: E139761 (Component side).
- PB Part Number: Intel bare circuit board part number (Solder side) 734661-001.
- Battery "+ Side-Up" marking: located on the component side of the board in close proximity to the battery holder.
- FCC Logo/Declaration: (Solder side).
- ACA (C-Tick) mark: Consists of a unique letter C, with a tick mark; followed by N-232. Located on the component side of the board and on the shipping container.
- CE Mark: (Component side) The CE mark should also be on the shipping container.

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction

The board uses an Intel/AMI BIOS, which is stored in flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the flash memory contains the BIOS Setup program, POST, APM, the PCI auto-configuration utility, and Plug and Play support.

This board supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as SU81010A.86A.

For information about	Refer to
The board's compliance level with APM and Plug and Play	Table 3, page 14

3.2 BIOS Flash Memory Organization

The Intel 82802AB Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable. Figure 9 shows the organization of the flash memory.

The last two 8 KB blocks of the fault tolerance area are the parameter blocks. These blocks contain data such as BIOS updates, vital product data (VPD), logo, System Management BIOS (SMBIOS) interface, and extended system configuration data (ESCD) information. The backup block contains a copy of the fault tolerance block.

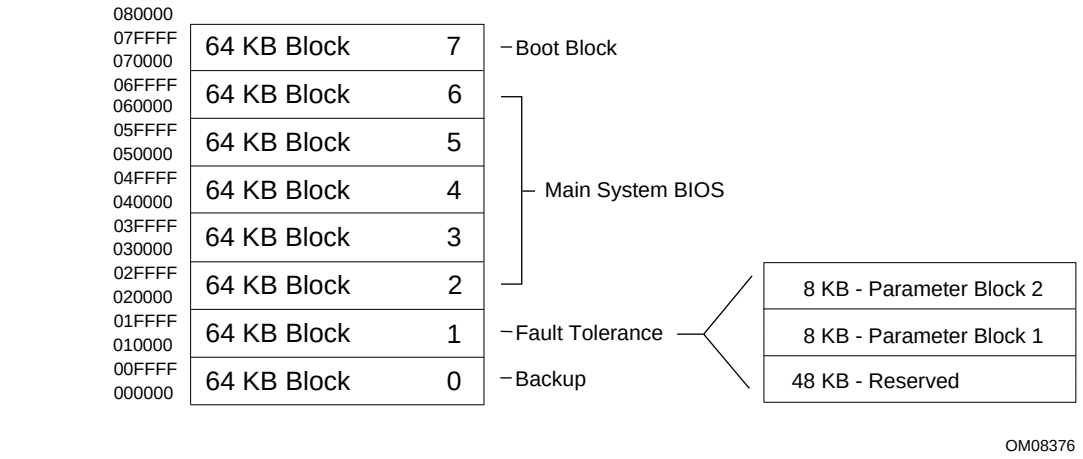


Figure 9. Memory Map of the Flash Memory Device

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI or Plug and Play cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to system resources. The assignment of PCI interrupts to ISA IRQs is non-deterministic. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by the BIOS, see Section 1.3.

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA/66 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.3 for the supported version of ATAPI). Add-in ISA IDE controllers are not supported. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66 features, the following items are required:

- An ATA-66 peripheral device
- An ATA-66 compatible cable
- ATA-66 operating system device drivers

NOTE

ATA-66 compatible cables are backward compatible with drivers using slower IDE transfer protocols. If an Ultra ATA/66 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate for either drive is 33 MB/sec.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel® LANDesk® Client Manager to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT†, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The board's compliance level with SMBIOS	Table 3, page 14

3.5 BIOS Upgrades

A new version of the BIOS can be upgraded from a diskette using the Intel® Flash Memory Update utility that is available from Intel. This utility supports the following BIOS maintenance functions:

- Update the flash BIOS from a file on a diskette
- Change the language section of the BIOS
- Verify that the upgrade BIOS matches the target system to prevent accidentally installing an incompatible BIOS
- BIOS boot block update

BIOS upgrades and the Intel Flash Memory Update utility are available from Intel through the Intel World Wide Web site. See Section 1.2 on page 14 for information about this site.

NOTE

Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.

For information about	Refer to
Intel's world wide web site	Section 1.2, page 14

3.5.1 Language Support

The BIOS Setup program and help messages can be supported in 32 languages. Five languages are available in the BIOS: US English, German, Italian, French, and Spanish. The default language is US English, which is present unless another language is selected in the BIOS Setup program.

The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets. Translations of other languages may become available at a later date.

3.5.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available on the Intel Support World Wide Web site.

3.6 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the non-erasable boot block area, there is no video support. The procedure can only be monitored by listening to the speaker or looking at the diskette drive's LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- A single beep indicates the beginning of the BIOS recovery process.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Upgrade utility are available from Intel Customer Support through the Intel World Wide Web site.

NOTE

BIOS Recovery cannot be accomplished using non-SPD DIMMs. SPD data structure is required for the recovery process.

NOTE

The computer can boot from an LS-120 diskette drive if the drive is configured as an ATAPI removable IDE device (in the Boot menu). When booting from an LS-120 diskette, the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

For information about	Refer to
Contacting Intel customer support	Section 1.2, page 14
The BIOS recovery mode	Section 2.10, page 54
The Boot menu in the BIOS Setup program	Section 4.7, page 90

3.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the primary boot device and the hard drive to be the secondary boot device.

3.7.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order.

The network can be selected as a boot device. This selection allows booting from a network device (onboard LAN or a PCI bus network adapter) with a remote boot ROM installed.

For information about	Refer to
The El Torito specification	Table 3, page 14

3.7.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if no video adapter, keyboard, or mouse is attached.

3.8 USB Legacy Support

USB legacy support enables USB keyboards and mice to be used even when no operating system USB drivers are in place. By default, USB legacy support is disabled. USB legacy support is only intended for accessing the BIOS Setup program and installing an operating system that supports USB.

This sequence describes how USB legacy support operates in the default (disabled) mode.

1. When you power-up the computer, USB legacy support is disabled.
2. POST begins.
3. USB legacy support is temporarily enabled by the BIOS. This allows you to use a USB keyboard to enter the BIOS Setup program or the maintenance mode.
4. POST completes and disables USB legacy support (unless it was set to Enabled while in the BIOS Setup program).
5. The operating system loads. While the operating system is loading, USB keyboards and mice are not recognized. After the operating system loads the USB drivers, the USB devices are recognized.

To install an operating system that supports USB, enable USB legacy support in the BIOS Setup program and follow the operating system's installation instructions. Once the operating system is installed and the USB drivers are configured, USB legacy support is no longer used. USB Legacy support can be left enabled in the BIOS Setup program if needed.

Notes on using USB legacy support:

- If USB legacy support is enabled, don't mix USB and PS/2 keyboards and mice. For example, do not use a PS/2 keyboard with a USB mouse, or a USB keyboard and a PS/2 mouse.
- Do not use USB devices with an operating system that does not support USB. USB legacy is not intended to support the use of USB devices in a non-USB aware operating system.
- USB legacy support is for keyboards and mice only. Hubs and other USB devices are not supported.

3.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions: The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is supervisor mode.

- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 43 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 43. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options *	Can change all options *	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

* If no password is set, any user can change all Setup options.

For information about	Refer to
Setting user and supervisor passwords	Section 4.4.6, page 87

4 BIOS Setup Program

What This Chapter Contains

4.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

Table 44 lists the BIOS Setup program menu functions.

Table 44. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options and power supply controls	Saves or discards changes to Setup program options

NOTE

In this chapter, all examples of the BIOS Setup Program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the board is in configuration mode. Section 2.10.2 on page 55 tells how to put the board in configuration mode.

Table 45 lists the function keys available for menu screens.

Table 45. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen
<↑> or <↓>	Selects an item
<Tab>	Selects a field
<Enter>	Executes command or selects a submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

4.2 Maintenance Menu

Maintenance	Main	Advanced	Security	Power	Boot	Exit

The menu shown in Table 46 is for clearing the Setup passwords. Setup only displays this menu in configuration mode. Section 2.10.2 on page 55 tells how to set the board for configuration mode.

Table 46. Maintenance Menu

Feature	Options	Description
Clear All Passwords	No options	Clears the user and administrative passwords

4.3 Main Menu

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 47 describes the main menu. This menu reports processor and memory information and is for configuring the system date and system time.

Table 47. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
Cache RAM	No options	Displays the size of second-level cache.
Total Memory	No options	Displays the total amount of RAM on the board.
Memory Bank 0 Memory Bank 1	No options	Displays type of DIMM installed in each memory bank.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Month, day, and year	Specifies the current date.

4.4 Advanced Menu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

Table 48 describes the advanced menu. This menu is used for setting advanced features that are available through the chipset.

Table 48. Advanced Menu

Feature	Options	Description
Boot Configuration	No options	Configures Plug and Play and the Numlock key, and resets configuration data. When selected, displays the Boot Settings Configuration submenu.
Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration	No options	Specifies type of connected IDE device.
Diskette Configuration	No options	When selected, displays the Floppy Options submenu.
Event Log Configuration	No options	Configures Event Logging. When selected, displays the Event Log Configuration submenu.
Video Configuration	No options	Configures video settings.

4.4.1 Boot Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 49 is for setting Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

Table 49. Boot Configuration Submenu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if a Plug and Play operating system is being used. *No;* lets the BIOS configure all devices. *Yes;* lets the operating system configure Plug and Play devices. Not required with a Plug and Play operating system.
Reset Config Data	• **No (default)** • Yes	Clears the BIOS configuration data on the next boot.
Numlock	• Off • **On (default)**	Specifies the power-on state of the Numlock feature on the numeric keypad of the keyboard.

4.4.2 Peripheral Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 50 is used for configuring computer peripherals.

Table 50. Peripheral Configuration Submenu

Feature	Options	Description
Serial port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. *Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. When set to Auto, the BIOS assigns resources to the COM port depending on their availability. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address for serial port A, if serial port A is Enabled.
Interrupt	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for serial port A, if serial port A is Enabled.
Serial port B	• Disabled • Enabled • **Auto (default)**	Configures serial port B. *Auto* assigns the first free COM port, normally COM2, the address 2F8h and the interrupt IRQ3. When set to Auto, the BIOS assigns resources to the COM port depending on their availability. An * (asterisk) displayed next to an address indicates a conflict with another device. If either serial port address is set, that address will not appear in the list of options for the other serial port.
Base I/O address	• **2F8 (default)** • 3E8 • 2E8	Specifies the base I/O address for serial port B.
Interrupt	• **IRQ 3 (default)** • IRQ 4	Specifies the interrupt for serial port B.

continued

Table 50. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. Not available if the parallel port is disabled. *Output Only* operates in AT-compatible mode. *Bi-directional* operates in PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O address	• **378 (default)** • 278 • 228	Specifies the base I/O address for the parallel port.
Interrupt	• (IRQ) 5 • **(IRQ) 7 (default)**	Specifies the interrupt for the parallel port.
Audio Device	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
LAN Device	• Disabled • **Enabled (default)**	Enables or disable the onboard LAN subsystem.
Legacy USB Support	• Disabled • Enabled • **Auto (default)**	Enables or disables USB legacy support. (See Section 3.8 on page 72 for more information.)

4.4.3 IDE Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration Primary IDE Master Primary IDE Slave Secondary IDE Master Secondary IDE Slave
Diskette Configuration
Event Log Configuration
Video Configuration

The menu represented in Table 51 is used to configure IDE device options.

Table 51. IDE Configuration Submenu

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary;* enables only the Primary IDE Controller. *Secondary;* enables only the Secondary IDE Controller. *Both;* enables both IDE controllers.
Hard Disk Pre-Delay	**Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.4.3.1 Primary IDE Master Submenu

Maintenance Main	**Advanced**	Security Power	Boot Exit

Boot Configuration
Peripheral Configuration
IDE Configuration **Primary IDE Master** Primary IDE Slave Secondary IDE Master Secondary IDE Slave
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 52 is used to configure the primary master IDE interface.

Table 52. Primary IDE Master Submenu

Feature	Options	Description
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User;* allows the cylinders, heads, and sectors fields to be changed. *Auto;* automatically fills in the values for the cylinders, heads, and sectors fields.
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables the LBA mode control.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.
PIO Mode	• **Auto (default)** • 0 • 1 • 2 • 3 • 4	Configures the PIO mode.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4	Specifies the Ultra DMA mode for the drive.

4.4.3.2 Primary IDE Slave Submenu

Maintenance Main	**Advanced**	Security Power	Boot Exit

Boot Configuration
Peripheral Configuration
IDE Configuration Primary IDE Master **Primary IDE Slave** Secondary IDE Master Secondary IDE Slave
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 53 is used to configure the primary IDE slave interface.

Table 53. Primary IDE Slave Submenu

Feature	Options	Description
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User;* allows the cylinders, heads, and sectors fields to be changed. *Auto;* automatically fills in the values for the cylinders, heads, and sectors fields.
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables the LBA mode control.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.
PIO Mode	• **Auto (default)** • 0 • 1 • 2 • 3 • 4	Configures the PIO mode.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4	Specifies the Ultra DMA mode for the drive.

4.4.3.3 Secondary IDE Master Submenu

Maintenance Main	**Advanced**	Security Power	Boot Exit

Boot Configuration
Peripheral Configuration
IDE Configuration Primary IDE Master Primary IDE Slave **Secondary IDE Master** Secondary IDE Slave
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 54 is used to configure the secondary IDE master interface.

Table 54. Secondary Master IDE Submenu

Feature	Options	Description
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User;* allows the cylinders, heads, and sectors fields to be changed. *Auto;* automatically fills in the values for the cylinders, heads, and sectors fields.
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables the LBA mode control.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.
PIO Mode	• **Auto (default)** • 0 • 1 • 2 • 3 • 4	Configures the PIO mode.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4	Specifies the Ultra DMA mode for the drive.

4.4.3.4 Secondary IDE Slave Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration Primary IDE Master Primary IDE Slave Secondary IDE Master **Secondary IDE Slave**
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 55 is used to configure the secondary IDE slave interface.

Table 55. Secondary IDE Slave Submenu

Feature	Options	Description
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User;* allows the cylinders, heads, and sectors fields to be changed. *Auto;* automatically fills in the values for the cylinders, heads, and sectors fields.
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables the LBA mode control.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.
PIO Mode	• **Auto (default)** • 0 • 1 • 2 • 3 • 4	Configures the PIO mode.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4	Specifies the Ultra DMA mode for the drive.

4.4.4 Diskette Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 56 is for configuring the diskette drive.

Table 56. Diskette Configuration Submenu

Feature	Options	Description
Diskette Controller	• Disabled • **Enabled (default)**	Disables or enables the integrated diskette controller.
Floppy A	• Not Installed • 360 KB 5¼" • 1.2 MB 5¼" • 720 KB 3½" • **1.44/1.25 MB 3½" (default)** • 2.88 MB 3½"	Specifies the capacity and physical size of diskette drive A.
Diskette Write Protect	• **Disabled (default)** • Enabled	Disables or enables write-protect for the diskette drive.

4.4.5 Event Log Configuration

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 57 is for configuring the event logging features.

Table 57. Event Log Configuration Submenu

Feature	Options	Description
Event log	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
View event log	[Enter]	Displays the event log.
Clear all event logs	• **No (default)** • Yes	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of events.
Mark events as read	[Enter]	Marks all events as read.

4.4.6 Video Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 58 is for configuring the video features.

Table 58. Video Configuration Submenu

Feature	Options	Description
Video Configuration	**AGP (default)** PCI	Selects the primary video adapter; AGP or PCI.

4.5 Security Menu

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu shown in Table 59 is for setting passwords and security features.

Table 59. Security Menu

Feature	Options	Description
Supervisor Password Is	No options.	Reports if there is a supervisor password set.
User Password Is	No options.	Reports if there is a user password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Clear User Password (Note 1)	• **Yes (default)** • No	Clears the user password.
User Access Level (Note 2)	• Limited • No Access • View Only • **Full (default)**	Sets BIOS Setup Utility access rights for user level.
Unattended Start (Note 1)	• **Disabled (default)** • Enabled	Enables or disables Wake on LAN technology feature. The keyboard remains locked until a password is entered.

Notes:

1. This feature appears only if a user password has been set.
2. This feature appears only if both a user password and a supervisor password have been set.

4.6 Power Menu

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit

The menu represented in Table 60 is for setting power management features.

Table 60. Power Menu

Feature	Options	Description
Power Management	• Disabled • **Enabled (default)**	Enables or disables the BIOS power management feature.
Inactivity Timer	• Off • 1 Minute • 5 Minutes • 10 Minutes • **20 Minutes (default)** • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters standby mode.
Hard Drive	• Disabled • **Enabled (default)**	Enables power management for hard disks during standby and suspend modes.
Video Power-down	• Disabled • Standby • **Suspend (default)** • Sleep	Specifies power management for video during standby and suspend modes.
ACPI Suspend State	• **S1 State (default)** • S3 State	S1 is the safest mode but consumes more power. S3 consumes less power but some drivers may not support this state.

4.7 Boot Menu

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					IDE Drive Configuration	

The menu represented in Table 61 is used to set the boot features and the boot sequence.

Table 61. Boot Menu

Feature	Options	Description
Quiet Boot	• Disabled • **Enabled (default)**	*Disabled* displays normal POST messages. *Enabled* displays OEM logo instead of POST messages.
Quick Boot	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Stays Off • **Last State (default)** • Power On	Specifies the mode of operation if an AC/Power loss occurs. *Stay Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before power loss occurred. *Power-on* restores power to the computer.
On Modem Ring	• **Stay Off (default)** • Power On	Specifies how the computer responds to an incoming call on an installed modem when the power is off. (APM mode only)
On LAN	• Stay Off • **Power On (default)**	Specifies how the computer responds to a LAN wakeup event when the power is off. (APM mode only)
On PME	• **Stay Off (default)** • Power On	Specifies how the computer responds to a PME wakeup event when the power is off. (APM mode only)
1st Boot Device 2nd Boot Device 3rd Boot Device 4th Boot Device 5th Boot Device	• Floppy • ARMD-FDD (Note 1) • ARMD-HDD (Note 2) • IDE-HDD • ATAPI CDROM • Intel UNDI PXE-2.0 (Note 3) • Disabled	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering. The default settings for the first through fifth boot devices are, respectively: • Floppy • IDE-HDD • ATAPI CDROM • Intel UNDI PXE-2.0 • Disabled

continued

Table 61. Boot Menu (continued)

Feature	Options	Description
IDE Drive Configuration	[Enter]	Invokes the IDE Drive Configuration submenu.

Notes:

1. ARMD-FDD = ATAPI removable device - floppy disk drive
2. ARMD-HDD = ATAPI removable device - hard disk drive
3. UNDI = Universal Network Interface Card (NIC) Driver Interface
   PXE = Pre-boot eXecution Environment

4.7.1 IDE Drive Configuration Submenu

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					IDE Drive Configuration	

The menu represented in Table 62 is used to set the drive number for the devices on the IDE interfaces.

Table 62. IDE Drive Configuration Submenu

Feature	Options	Description
Primary Master IDE	**1st IDE (default)** 2nd IDE 3rd IDE 4th IDE	Sets the IDE drive number assigned to the device on the primary master IDE interface. To set the IDE drive number: 1. Select the IDE drive number with <↑> or <↓>. 2. Press <Enter> to set the selection.
Primary Slave IDE	1st IDE **2nd IDE (default)** 3rd IDE 4th IDE	Sets the IDE drive number assigned to the device on the primary slave IDE interface. To set the IDE drive number: 1. Select the IDE drive number with <↑> or <↓>. 2. Press <Enter> to set the selection.
Secondary Master IDE	1st IDE 2nd IDE **3rd IDE (default)** 4th IDE	Sets the IDE drive number assigned to the device on the secondary master IDE interface. To set the IDE drive number: 1. Select the IDE drive number with <↑> or <↓>. 2. Press <Enter> to set the selection.
Secondary Slave IDE	1st IDE 2nd IDE 3rd IDE **4th IDE (default)**	Sets the IDE drive number assigned to the device on the secondary slave IDE interface. To set the IDE drive number: 1. Select the IDE drive number with <↑> or <↓>. 2. Press <Enter> to set the selection.

4.8 Exit Menu

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 63 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 63. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

What This Chapter Contains

5.1 BIOS Error Messages

Table 64 lists the error messages and provides a brief description of each.

Table 64. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate-A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error	No responses from diskette drive.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error occurred trying to access diskette drive controller.
HDC Failure	Error occurred trying to access hard disk controller.

continued

Table 64. BIOS Error Messages (continued)

Error Message	Explanation
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Is Locked	The system keyboard lock is engaged. The system must be unlocked to continue to boot.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an off-board card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where the error occurred.

Displaying the POST codes requires an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 65 defines the uncompressed INIT code checkpoints, Table 66 describes the boot block recovery code checkpoints, and Table 67 lists the runtime code uncompressed in F000h shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 65. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, do Memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 66. Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize the interrupt vector tables, initialize system timer, initialize DMA controller, and interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize floppy drive.
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS120, Zip†) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 67. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23, 24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, and output devices) to start if present. (See Section 5.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power-on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 5.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 67. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power-on, go to check point # 4Eh).
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 67. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power-on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID and Numlock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.

continued

Table 67. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 68 describes the bus utilization checkpoints.

Table 68. BIOS Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 69 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 69. Upper Nibble of the High Byte Descriptions

Value	Description
0	func#0, disable all devices on the bus concerned.
1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.

Table 70 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 70. Lower Nibble of the High Byte Descriptions

Value	Description
0	Generic DIM (Device Initialization Manager).
1	On-board system devices.
2	ISA devices.
3	EISA devices.
4	ISA PnP devices.
5	PCI devices.

5.4 Speaker

A 47 Ω inductive speaker is mounted on the board. The speaker provides audible error code (beep code) information during the power-on self-test (POST).

For information about	Refer to
The location of the onboard speaker	Figure 1, page 12

5.5 BIOS Beep Codes

Whenever a recoverable error occurs during power-on self-test (POST), the BIOS displays an error message describing the problem (see Table 71). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 71. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g. POST module not found, etc.)