SU810 Motherboard Specification Update

Release Date: November 2000

Order Number: 745863-011

The SU810 motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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REVISION HISTORY

Date of Revision	Version	Description
September 1999	-001	This document is the first Specification Update for the Intel® SU810 motherboard.
October 1999	-002	Added Specification Change 1.
November 1999	-003	Removed Specification Change 1, which was published in revision –002 of the Technical Product Specification.
January 2000	-004	Added Erratum 1 and Documentation Change 1.
February 2000	-005	Added Specification Change 2 and Errata 2-3.
March 2000	-006	Added Erratum 4.
May 2000	-007	Added Specification Changes 3-4 and Erratum 5.
June 2000	-008	Added Specification Change 5.
July 2000	-009	Added Specification Change 6.
September 2000	-010	Added Erratum 6.
November 2000	-011	Added Documentation Change 7.

PREFACE

This document is an update to the specifications contained in the SU810 Motherboard Technical Product Specification (Order number 741219). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Intel® Celeron™ Processor Specification Update* (Order number 243748) for specification updates concerning the Intel Celeron processor. Items contained in the *Intel Celeron Processor Specification Update* that either do not apply to the SU810 motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel® 82810 Chipset: 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH) Specification Update* (Order Number 290659) for specification updates concerning the 82810 GMCH Controller. Items contained in the *82810 GMCH Specification Update* that either do not apply to the SU810 motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any GMCH errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel® 82801 I/O Controller Hub (ICH) Specification Update* (Order Number 290677) for specification updates concerning the 82801 I/O Controller Hub. Items contained in the *Intel 82801 ICH Specification Update* that either do not apply to the SU810 motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any ICH errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *Intel® 82802 Firmware Hub (FWH) Specification Update* (Order Number TBD) for specification updates concerning the 82802 Firmware Hub. Items contained in the *Intel 82802 FWH Specification Update* that either do not apply to the SU810 desktop board or have been worked around are noted in this document. Otherwise, it should be assumed that any ICH errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the SU810 motherboard's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all motherboards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Update for SU810 Motherboards

GENERAL INFORMATION

Basic SU810 Motherboard Identification Information

AA Revision	PBA Revision	BIOS Revision	Notes
741636-503	741634-503	SU81010A.86A.0003.P03	1-6
743282-503	743283-503	SU81010A.86A.0003.P03	1-6
741636-600	741634-600	SU81010A.86A.0005.P05	1-6
743282-600	743283-600	SU81010A.86A.0005.P05	1-6
A15186-600	A15187-600	SU81010A.86A.0008.P08	1-6
A15188-800	A15189-800	SU81010A.86A.0008.P08	1-6

NOTES:

1. The PBA number or AA number is found on a small label on the component side of the board.
2. The 82810 Chipset kit used on this PBA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
82810 GMCH	A2	SL35X
82801AB ICH	B0	SL38J
82802AB FWH	A0	SB48

3. The following errata are contained in the *Intel® Celeron™ Processor Specification Update* (Order Number 243748) for the Celeron processor and either do not apply to the SU810 motherboard or have been worked-around in this PBA and/or BIOS revision: None. All other errata associated with the processor apply to this PBA revision.
4. The following items are contained in the *Intel® 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH) Specification Update* (Order Number 290659) and either do not apply to the SU810 motherboard or have been worked around in this PBA and/or BIOS revision: 1,12. All other errata associated with the GMCH apply to this PBA revision.
5. The following items are contained in the *Intel® 82801 I/O Controller Hub Specification Update* (Order Number 290677) and either do not apply to the SU810 motherboard or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the ICH apply to this PBA revision.
6. The following items are contained in the *Intel® 82802 Firmware Hub Specification Update* (Order Number TBD) and either do not apply to the SU810 desktop board or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the FWH apply to this PBA revision.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the SU810 motherboard. Intel intends to fix some of the errata in a future revision of the motherboard, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the motherboard or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	Published in revision –002 of the Technical Product Specification
2	Doc	Support for faster Intel® Celeron™ processors
3	Doc	Memory bus loading note added to section 1.5, System Memory
4	Doc	Change to description of Section 2.9, NLX card-edge connector
5	Doc	Support for faster Intel Celeron processors
6	Doc	Change to description of restoring custom defaults after power failure
7	Doc	Support for faster Intel® Pentium® III processors
NO.	**PLANS**	**ERRATA**
1	Fixed	User password in bios allows users to change supervisor password
2	Fixed	BIOS does not detect SCSI adapters as boot device
3	Fixed	BIOS may allow system to boot when user password is enabled
4	Fixed	System will hang when using LAN as the first boot device
5	Fixed	Some DIMM configurations may fail memory stress testing
6	Fix	Some SCSI host bus adapters may not boot to the hard disk drive with a bootable CD-ROM drive attached
NO.	**PLANS**	**DOCUMENTATION CHANGES**
1	Doc	Change to description of ATA device support

The errata described in this specification update apply to combinations of PBA revision and BIOS revision as shown in the table below. Descriptions of the individual erratum referred to by number in the table below are found in the ERRATA section of this document.

PBA Revision	BIOS Revision	Errata That Apply
741634-503	SU81010A.86A.0003.P03‡	1-5, 6
	SU81010A.86A.0004.P04‡	3, 5-6
	SU81010A.86A.0005.P05‡	5-6
	SU81010A.86A.0008.P08	6
	SU81010A.86A.0009.P09	6
741634-600	SU81010A.86A.0003.P03‡	1-5, 6
	SU81010A.86A.0004.P04‡	3, 5-6
	SU81010A.86A.0005.P05‡	5-6
	SU81010A.86A.0008.P08	6
	SU81010A.86A.0009.P09	6
743283-503	SU81010A.86A.0003.P03‡	1-5, 6
	SU81010A.86A.0004.P04‡	3, 5-6
	SU81010A.86A.0005.P05‡	5-6
	SU81010A.86A.0008.P08	6
	SU81010A.86A.0009.P09	6
743283-600	SU81010A.86A.0003.P03‡	1-5, 6
	SU81010A.86A.0004.P04‡	3, 5-6
	SU81010A.86A.0005.P05‡	5-6
	SU81010A.86A.0008.P08	6
	SU81010A.86A.0009.P09	6
A15187-600	SU81010A.86A.0003.P03‡	1-5, 6
	SU81010A.86A.0004.P04‡	3, 5-6
	SU81010A.86A.0005.P05‡	5-6
	SU81010A.86A.0008.P08	6
	SU81010A.86A.0009.P09	6
A15189-800	SU81010A.86A.0003.P03‡	1-5, 6
	SU81010A.86A.0004.P04‡	3, 5-6
	SU81010A.86A.0005.P05‡	5-6
	SU81010A.86A.0008.P08	6
	SU81010A.86A.0009.P09	6

‡ Note: This combination of BIOS revision and PBA revision has not undergone regression testing. Use of a PBA with down-revision BIOS is an untested combination and is undertaken at the user's risk.

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *SU810 Motherboard Technical Product Specification* (Order Number 741219). All Specification Changes will be incorporated into a future version of that specification.

1. Published in Revision -002 of the Technical Product Specification

2. Support for Faster Intel® Celeron™ Processors

In Section 1.4, Processor, the following will be added to Table 4, Processors Supported by the Board:

Processor Type	Processor Speed	Host Bus Frequency	L2 Cache Size
Celeron™ processor	533 MHz	66 MHz	128 KB

3. Memory Bus Loading Note Added to Section 1.5, System Memory

Section 1.5, System Memory, will have the following note added:

To obtain best memory bus loading characteristics, DIMM modules should be installed in Bank 0 (J1D2) first, then in Bank 1 (J1D1).

4. Change to Description of Section 2.9, NLX Card-Edge Connector

Section 2.9, NLX Card Edge Connector, will be changed as follows:

The text at the beginning of the section will be replaced in its entirety.

2.9 NLX Card Edge Connector

The NLX riser connector on the board consists of a 340-position (2 x 170) and a supplemental 26 position (2 x 13) gold finger contact.

According to the NLX specification, the board edge connector provides the following:

- PCI signals (the board supports up to four PCI devices)
- Two IDE channels
- One diskette drive interface
- Miscellaneous front panel signals
- Power connection for the board

See Section 1.3 for information about the NLX specification.

Table 30, Table 31 and Table 32 specify the pinouts located on the primary connector; Table 33 specifies the pinouts located on the supplemental connector. Some edge connector pin definitions differ from those defined in the NLX specification, version 1.2.

The ICH supports a total of five PCI bus masters. Table 29 tells how many PCI bus masters are available for the NLX riser based on the board configuration.

The second note following Table 29 will be replaced in its entirety as follows:

NOTE

ISA bus signals (as defined in the NLX Riser specification) are not provided on the SU810 board at the NLX riser card edge connector. Riser cards with ISA add-in connectors may not function correctly with this desktop board. See Table 31 for definitions of signals on the ISA section of the NLX riser connector.

Table 31 and its associated notes will be replaced in their entirety as follows:

Table 31. ISA Segment, Riser Interconnect

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A52	Vcc thru pullup	ISA	NA	MB	B52	5VDC	PWR	NA	NA
A54	Remote Open	Misc	I	RIS	B55	Remote sense	Misc	I	RIS
A55	Remote Closed	Misc	I	RIS	B66	GND	PWR	NA	NA
A56	Position Open/ Closed	Misc	I	RIS	B68	5VDC	PWR	NA	NA
A57	5VDC	PWR	NA	NA	B75	DMA_66 Detect Primary	ISA	I/O	MB
A65	GND	PWR	NA	NA	B77	BIOS NON COMM	Misc	I	MB

continued

Table 31. ISA Segment, Riser Interconnect (continued)

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A73	5VDC	PWR	NA	NA	B78	GND	PWR	NA	NA
A78	DMA_66 Detect Secondary	ISA	I/O	MB	B79	OS NO BOOT	Misc	I	MB
A81	GND	PWR	NA	NA	B80	PW INTR	Misc	I	MB
A89	GND	PWR	NA	NA	B81	GLUE THERMTRIP	Misc	I	MB
A97	5VDC	PWR	NA	NA	B82	SYS FAIL	Misc	I	RIS
					B84	NOGO	ISA	I/O	MB
					B86	LAN_present/ disable	ISA	I/O	MB
					B87	REQ[A] #	PCI	I	RIS
					B88	GNT[A]	PCI	O	RIS
					B89	P_REQ5#	PCI	I	RIS
					B90	P_GNT5#	PCI	O	RIS
					B96	5VDC	PWR	NA	NA
					B101	GND	PWR	NA	NA

I/O Column Definitions Relative to the Board:
O = Output from board to riser
I = Input from riser to board
NA = Not an input or output signal
Termination Column Definitions:
MB = Termination/Pullup/Pulldown/debounce is on the board
RIS = Termination/Pullup/Pulldown is on riser card
NA = Not on board or riser

5. Support for Faster Intel® Celeron™ Processors

In Section 1.4, Processor, the following will be added to Table 4, Processors Supported by the Board:

Processor Type	Processor Speed	Host Bus Frequency	L2 Cache Size
Celeron™ processor	566 MHz	66 MHz	128 KB
	600 MHz	66 MHz	128 KB

NOTE

BIOS Revision SU81010A.86A.0005 or later is required for the Desktop Board to properly support 566 and 600 MHz processors.

In addition, the following board PBA's are required to support these processors:

741634-600 or later

743283-600 or later

A15185-800 or later

A15187-800 or later

6. Change to Description Of Restoring Custom Defaults After Power Failure

The note to Section 1.6.4 Real-time Clock, CMOS SRAM, and Battery will be changed in its entirety as follows:

NOTE

If the battery and AC power fail, the defaults that will be reloaded will depend on the BIOS revision. With BIOS revision SU81010A.86A.0008.P08 or earlier, standard defaults, not custom defaults, will be loaded into CMOS RAM at power-on. With BIOS revision SU81010A.86A.0009.P09 or later, if the battery and AC power fail, custom defaults if available, will be loaded into CMOS RAM at power-on.

7. Support for Faster Intel® Pentium® III Processors

In Section 1.4, Processor, the following will be added to Table 4, Processors Supported by the Board:

Processor Type	Processor Speed	Host Bus Frequency	L2 Cache Size
Pentium® III processor	500E MHz	100 MHz	256 KB
	550E MHz	100 MHz	256 KB
	600E MHz	100 MHz	256 KB
	650 MHz	100 MHz	256 KB
	700 MHz	100 MHz	256 KB
	750 MHz	100 MHz	256 KB
	800 MHz	100 MHz	256 KB

NOTE

BIOS Revision SU81010A.86A.0008.P08 or later is required for the Desktop Board to properly support Pentium® III processors.

In addition, the following board PBA's are required to support these processors:

A15187-800 or later

ERRATA

1. User Password in BIOS Allows Users to Change Supervisor Password

PROBLEM: If the user password is set to Limited Access or Full Access in BIOS, the user then has the ability to change the supervisor password.

IMPLICATION: An unauthorized user could gain access to supervisor functions in the BIOS setup program.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS version SU81010A.86A.0004.P04.

2. BIOS Does Not Detect SCSI Adapters as Boot Device

PROBLEM: The SCSI adapter is not detected as a boot device.

IMPLICATION: Users who wish to use a SCSI hard drive as the primary boot device will not be able to do so.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision SU81010A.86A.0004.P04.

3. BIOS May Allow System to Boot When User Password is Enabled

PROBLEM: If both User Password and Unattended Start are enabled in the BIOS Setup program, the system will boot from the diskette drive without prompting for a password if a bootable diskette is present in the drive.

IMPLICATION: An unauthorized user might be able to gain access to system data.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision SU81010A.86A.0005.P05.

4. System Will Hang When Using LAN as The First Boot Device

PROBLEM: If the local area network is set as the first boot device using the Intel® LANDesk® Service Agent (LSA), the system will not boot from the LAN and will hang while attempting to boot to the next device.

IMPLICATION: The user will not be able to set the LAN as the first boot device in the system BIOS Setup program.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision SU81010A.86A.0004.P04.

5. Some DIMM Configurations May Fail Memory Stress Testing

PROBLEM: Certain lightly loaded DIMM configurations fail memory stress testing. Two configurations that fail most consistently are 64 MB and 128 MB (16 Mb x 8).

IMPLICATION: The memory failures cause the system to lock up.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision SU81010A.86A.0008.P08.

6. Some SCSI Host Bus Adapters May Not Boot to The Hard Disk Drive With a Bootable CD-ROM Drive Attached

PROBLEM: If a bootable CD-ROM is attached to the SCSI host bus adapter (HBA) and set as bootable in the setup menu of the SCSI HBA without bootable media installed, the system may not boot to the attached hard drive.

IMPLICATION: Users who wish to utilize a bootable SCSI CD-ROM in conjunction with a bootable hard drive on an add-in SCSI host bus adapter may not be able to boot to the hard drive if the SCSI adapter is set to recognize the CD-ROM as a bootable device.

WORKAROUND: Enable the CD-ROM as a bootable SCSI device only when using bootable media.

STATUS: This erratum will be fixed in a future BIOS revision.

DOCUMENTATION CHANGES

1. Change to Description of ATA Device Support

Section 3.3.2, PCI IDE Support, will be replaced in its entirety as follows:

3.3.2 PCI IDE SUPPORT

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE channels with independent I/O channel support. The IDE interface supports hard drives up to ATA/66 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.3 for the supported version of ATAPI). Add-in ISA IDE controllers are not supported. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66 features, the following items are required:

- An ATA-66 peripheral device
- An ATA-66 compatible cable
- ATA-66 operating system device drivers
- An ATA-66 capable NLX Riser