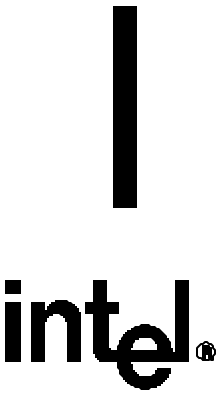

L440GX+ Server Board Specification Update

Release Date: April 2001

Order Number: 245145-025

REVISION HISTORY

Date of Revision	Description
March, 1999	This document is the first Specification Update for the L440GX+ Server Board and Astor II and the Columbus III Chassis
April, 1999	Astor II and Columbus III updates have been removed from the original and placed in their own documents.
May 1999	Updated Erratum 7 to fixed, added erratum 14. Updated Documentation changes 1-3 to fixed, added documentation change 4.
June, 1999	Added BIOS 6.0 and erratum 15.
July 1999	Added BIOS 6.1, added Doc erratum #5
August 1999	Added Board ID information table
September 1999	No new information
October 1999	Added BIOS 9.1 changes/additions
November 1999	Added report of issue with BIOS Japanese Language support, GRM support, Pentium® III 600E MHz processor support
December 1999	Added processor removal procedure from GRMs
February 2000	No new information
March 2000	Doc items added and updated
April 2000	Tables updated, SRCU21 issue added
May 2000	NIC Teaming errata added, EMP Errata added
June 2000	No additions or changes from April
July 2000	No additions or changes from May
August 2000	Board ID table updated; EMP errata update
September 2000	Update to supported processor section
October 2000	No additions or changes
November 2000	No additions or changes
December 2000	Enhanced the “Supported Processors” section of this document, updated L440GX+ Component placement diagram as shown in TPS
January 2001	No new information

February 2001	No new information
March 2001	No new information

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The L440GX+ Server Board may contain design defects or errors known as errata that may cause the product to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Table of Contents

PREFACE

This document is an update to the information contained in the *L440GX+ Server Board Technical Product Specification*. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Specification Clarifications, Errata, and Document Changes.

Refer to the *Pentium® II Processor Specification Update* (Order Number 243337) for specification updates concerning the Pentium II processor. Items contained in the Pentium II Processor Specification Update that either do not apply to the L440GX+ Server Board or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Refer to the latest *Intel 82440GX AGPset Specification Update* for specification updates concerning the Intel 82440GX AGPset. Items contained in these Specification Updates that either do not apply to the L440GX+ Server Board or have been worked around are noted in this document. Otherwise, it should be assumed that any AGPset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications for the L440GX+ Server Board. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specification.

Errata are design defects or errors. Errata may cause the L440GX+ Server Board to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.

GENERAL INFORMATION

Identification Information

Below are the specific boards, BIOS and components covered by this update. The information in the table shows BIOS and Firmware revisions associated with PBA and AA numbers as they were shipped from the factory. Updated revisions of the BIOS and Firmware may be available from the WEB and not yet implemented into the factory.

L440GX+

Baseboard PBA #	Baseboard AA #	Product Codes	BMC Firmware Rev.	BIOS
704293-404	721242-002	BOXL440GX+ LWBB	Release 0.12	Release 2
704293-405	721242-003	BOXL440GX+ LWBB	Release 0.12	Release 3
704293-407	721242-005	BOXL440GX+ LWBB	Release 1.02	Release 6
704293-408	721242-006	BOXL440GX+ LWBB	Release 1.04	Release 7
704293-503	721242-008	BOXL440GX-C LWBBS	Release 1.05	Release 9.2
704293-510	721242-010	BOXL440GX-C LWBBS	Release 1.05	Release 11.1
704293-515	721242-011	BOXL440GX-C LWBBS	Release 1.07	Release 11.1
704293-602	721242-012	BOXL440GX-C LWBBS	Release 1.08	Release 11.2
704293-603	721242-013	BOXL440GX-H LWBBS	Release 1.11	Release 12.1
704293-801	721242-020	BOXL440GX-G LWBBS	Release 1.13	Release 13.0
704293-802	721242-021	BOXL440GX-G LWBBS	Release 1.13	Release 14.0

Supported Processors

NOTE:
The L440GX+ server board will only support processors utilizing a 100MHz front side bus (FSB). Processors utilizing a 133MHz FSB are not supported on the L440GX+ server board.

L440GX+ server boards (product code **BOXL440GX+**) having a **PBA# of 704293-40x** and earlier or an **AA# of 721242-007** or earlier (where x is any number and earlier boards will have a smaller number after the dash) will only support the following processors:

Processor Family	Frequency	Cache size / Type	Packaging
Intel® Pentium® II	350 MHz	512 KB Discrete L2	SECC
Intel Pentium II	400 MHz	512 KB Discrete L2	SECC
Intel Pentium II	450 MHz	512 KB Discrete L2	SECC
Intel® Pentium® III	450 MHz	512 KB Discrete L2	SECC2
Intel Pentium III	500 MHz	512 KB Discrete L2	SECC2
Intel Pentium III	550 MHz	512 KB Discrete L2	SECC2
Intel Pentium III	600 MHz	512 KB Discrete L2	SECC2

L440GX+ server boards (product codes **BOXL440GX-C** or **BOXL440GX-H)** having a **PBA# of 704293-50x** and later or an **AA# of 721242-008** and later (where x is any number and later boards will have a larger number after the dash) are capable of supporting the following processors:

Processor Family	Frequency	Cache size / Type	Packaging
Intel® Pentium® II	350 MHz	512 KB Discrete L2	SECC
Intel Pentium II	400 MHz	512 KB Discrete L2	SECC
Intel Pentium II	450 MHz	512 KB Discrete L2	SECC
Intel® Pentium® III	450 MHz	512 KB Discrete L2	SECC2
Intel Pentium III	500 MHz	512 KB Discrete L2	SECC2
Intel Pentium III	550 MHz	512 KB Discrete L2	SECC2
Intel Pentium III	550E MHz	256 KB ATC L2	SECC2
Intel Pentium III	600 MHz	512 KB Discrete L2	SECC2
Intel Pentium III	600E MHz	256 KB ATC L2	SECC2
Intel Pentium III	650 MHz	256 KB ATC L2	SECC2
Intel Pentium III	700 MHz	256 KB ATC L2	SECC2
Intel Pentium III	750 MHz	256 KB ATC L2	SECC2
Intel Pentium III	800 MHz	256 KB ATC L2	SECC2
Intel Pentium III	850 MHz	256 KB ATC L2	SECC2

L440GX+ server boards (product code **BOXL440GX-G**) having a PBA # of 704294-80x and later or an AA# of 721242-020 and later, are capable of supporting all of the processors listed above including the 1 GHz Pentium III processor.

NOTE:
Installing a processor on a board that was not designed to support it, may cause damage to the server board, the processor, or both.

NOTE:
The system software, including BIOS, BMC firmware, and SDRs, may need to be updated from the factory defaults on some boards to support faster processors.

Summary Table of Changes

The following tables indicate the Errata and the Document Changes that apply to the L440GX+ Server Board. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Intel intends to update the appropriate documentation in a future revision.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	Plans	ERRATA
1	Fixed	ISC 1.8 shows the slot width for PCI Slot #4 as a 64 bit slot
2	No Fix	Turning on an external modem will power up the system
3	No Fix	Master read I2C command (app 51h) fails on public/private I2C bus
4	No Fix	Wake On LAN fails after AC power is applied to the board the 1st time
5	Fixed	Wake On LAN does not wake up system from an S1 sleep state in Microsoft* Windows* 98
6	Fix	Wake on Ring does not wake up system from an S1 sleep state in Microsoft* Windows* 98
7	Fixed	Modem Does not issue page
8	Fixed	L440GX+ incorrectly identifies the Pentium® III as a Pentium® II during POST
9	Fixed	Early versions of the Intel® Pro100+ NIC cause the L440GX+ to power on after exiting NT.
10	No Fix	The BMC will not generate SEL events for either Upper or Lower non-recoverable threshold crossings for analog sensors, even when enabled to do so.
11	No Fix	Manually re-arming digital sensors events via the “Re-Arm Sensor Event” command does not work.
12	Fixed	BMC Firmware is not able to accurately report lower critical temperature events accurately
13	Fixed	Voltage events incorrectly logged in SEL for LVD termination voltage sensors
14	Fixed	Data errors from DMI type 6 and type 17 inquiries

NO.	Plans	ERRATA
15	Fixed	L440GX+ Diagnostics 1.01 does not accurately detect Pentium® III processors
16	Fixed	System Hangs when using BMC forced update
17	Fixed	Enabling fixed disk boot sector write protect option fails
18	Fixed	L440GX+ Diagnostics 1.01 or 1.02 does not detect 256MB and 512MB DIMMS properly
19	Fixed	Japanese language support in system BIOS not functioning as it should
20	No Fix	EMP and console redirection will not function properly if POST Diagnostics screen is disabled (Default) in BIOS Setup
21	Fixed	Dual SRCU21 (Talo) configuration in L440GX+ server board may causes system hang during POST
22	Fixed	NIC Teaming features originally planned for PBA# –515 and AA# -011 were not implemented
23	Fixed	When EMP is set to “Always Active”, accessing the EMP port with a modem cannot be done

NO.	Plans	DOCUMENT CHANGES
1	Fixed	L440GX+ rev. 0.9 TPS – AT Style Front Panel Connector Table 2-13 corrected
2	Fixed	Clarifications made to which Adaptec ARO RAID card is supported in TPS
3	Fixed	All references to Intel® Pentium® Pro in the L440GX+ 0.9 TPS will be changed to Intel® Pentium® II
4	Fixed	Clarification of SCSI termination in product guide
5	Fixed	Clarification of PERR# in L440GX+ TPS
6	Fixed	Corrected BIOS table showing proper System Event Logging formats
7	Fixed	BIOS revs 9.1 and later adds two new BIOS setup options
8	Fixed	Accessing (F2) BIOS setup utility with BIOS Rev 9.1 and later
9	Fixed	SECC processors not supported with Grounded Retention Mechanisms (GRMs)
10	Fixed	Pentium® III 600E and faster processors not supported on older L440GX+ boards
11	Fixed	Revised processor extraction procedure from GRMs
12	Fixed	TPS rev 1.0 incorrectly shows COM port locations on the baseboard in figure 1
13	Fixed	Added processor support table to 2.0 TPS
14	Fix	Update to L440GX+ Component Placement Diagram as shown in 3.0 TPS.

ERRATA

1. ISC 1.8 shows the slot width for PCI Slot #4 as a 64 bit slot

Problem: PCI Slot-4 as referenced by ISC 1.8 shows a 64 bit slot when it is actually a 32 bit slot.
Workaround: None
Status: FIXED - UPGRADING SYSTEM BIOS TO PRODUCTION RELEASE 5 OR GREATER WILL CORRECT THIS ISSUE

2. Turning on an external modem will power up the system

Problem: If the system is configured with the modem enabled and EMP is disabled, applying power to the modem will cause the system to power up. When an external modem is attached to either COM port, the system powers up when the modem is turned on.
Implication: This is a side effect of having the wake on ring event enabled
Workaround: If the system and modem are both powered at the same time with power state retention not set, both the system and modem will function as expected. Or, If the system has AC removed but the modem has AC power applied, both the modem and the system will function as expected.
Status: No Fix planned

3. Master read I2C command (app 51h) fails on public/private I2C bus

Problem: The Master Read I2C command fails to operate correctly on either the public IPMB or the private I2C bus. If used on the public bus, the command may cause the bus to hang, disrupting communication to other controllers on that bus.
Implication: The IPMB or I2C bus may hang
Workaround: None. The Master Read I2C command should not be used
Status: Will not be fixed for the L440GX+. But will be fixed for future products

4. Wake On LAN fails after AC power is applied to the board the 1st time

Problem: Failure only seen when a device is attached to the IMB connector that is powered when the board has ac power removed. This condition causes the 5V_stby rail to maintain 0.5V. This is enough power to hold the data stored in the SRAM of the BMC
Workaround: Cold Boot system after Wake On LAN fails the 1st time.
Status: No Fix

5. Wake On LAN does not wake up system from an S1 sleep state in Microsoft Windows* 98*

Problem: WOL works for powering on the system, but fails to bring the system out of Standby mode.
Workaround: None
Status: Fixed - Windows 98 does not support WOL from Standby with the 1st release of the OS. This has been fixed in Release 2

6. Wake on Ring does not wake up system from an S1 sleep state in Microsoft Windows* 98*

Problem: Using Windows 98, the system will not exit from an S1 Sleep state with a ring indication from a modem attached to any com port.

Workaround: NONE
Status: Fix - Windows 98 does not support WOR in the initial release of the OS. It will be supported in a future Windows 98 Service Pack.

7. Modem Does not issue page

Problem: While issuing pages using an external modem, only TR light on modem remains lit and no pages are issued.
Workaround: None
Status: Fixed – This was fixed in version BMC firmware 1.02

8. L440GX+ incorrectly identifies the Pentium® III as a Pentium® II during POST

Problem: BIOS revisions up to and including Production Release 1 do not post the correct banner during Post when a Pentium III processor is detected.
Workaround: Upgrade to later BIOS
Status: Fixed – This issue has been addressed in BIOS Production Release 3.

9. Early versions of the Intel® EtherExpress™ Pro100+ NIC cause the L440GX+ to power on after exiting NT.

Problem: EtherExpress Pro100+ NICs with PBA# 668081-00x use an A-step of the 82558 network controller which has ESD errata against it causing improper behavior of a system's Power-On capabilities. Therefore, a problem was seen when performing a "Shutdown" from Windows* NT that after the system was powered down the system would automatically Power back up after approximately 2-4 seconds.
Workaround: Upgrade to an EtherExpress Pro100+ NIC with PBA# 697680-001 or later
Status: - Fixed

10. The BMC will not generate SEL events for either Upper or Lower non-recoverable threshold crossings for analog sensors, even when enabled to do so.

Problem: If the Baseboard Management Controller (BMC) detects an Upper or Lower value for a "Non-Recoverable" event, the event is not logged in the System Event Log (SEL). This affects all analog voltage, temperature and fan sensors.
Implications: If "Non-Recoverable" events are programmed into the Server Management Software, the Upper and Lower limits programmed for these events are not logged.
Workaround: Only program the BMC to log Upper and Lower limits for critical and Non-critical events.
Status: – No Fix for L440GX+. This will be addressed in future platforms.

11. Manually re-arming digital sensor events via the "Re-Arm Sensor Event" command does not work

Problem: Manually re-arming digital sensor events via the "Re-Arm Sensor Event" command does not work. This affects the digital fans and chassis intrusion sensor.

Workaround: None – The sensors will automatically re-arm when the sensor state goes from a triggered to a non-triggered state.
Status: No fix for L440GX+ - this will be addressed in future platforms

12. BMC Firmware Rel 0.12 is not able to accurately report lower critical temperature events accurately

Problem: If the temperature sensors read temperatures below 0 Degrees Celsius, the BMC firmware incorrectly reports the temperature as a high temperature value in the system event log.
Workaround: None.
Status: Fixed – Upgrading BMC Firmware to release 1.02 or later will fix this problem.

13. Voltage events are incorrectly logged in SEL for LVD termination voltage sensors

Problem: During POST, the BMC firmware may report Low voltage events to the system event log. This may occur if the BMC firmware scans the LVD voltage sensors before they are set. This is only seen if POST requires additional time prior to the BMC firmware scanning these sensors. Systems with large memory configurations may experience this problem do to the time required to test the memory during POST.
Workaround: Disable the LVD voltage sensors until the BMC firmware is updated to a later release that fixes this problem.
Status: Fixed – Upgrading BMC firmware to release 1.02 or later will fix this issue.

14. Data errors from DMI type 6 and type 17 inquiries.

Problem: During DMI type 6 and type 17 inquiries, incorrect data may be returned
Workaround: None.
Status: Fixed – Upgrading system BIOS to Production release 6 or later will fix this issue.

15. L440GX+ Diagnostics 1.01 does not accurately detect Pentium III processors.

Problem: When the L440GX+ Diagnostics utility auto detects installed hardware, it wrongly displays Pentium® III processors as Pentium® II processors.
Workaround: None. The diagnostics utility will run normally with Pentium III processors installed. This is only a cosmetic reporting issue.
Status: Fixed – L440GX+ Diagnostics 1.02 fixes this issue.

16. System Hangs when using BMC forced update

Problem: When attempting to force update the BMC Firmware using the "BMC FRC Up" jumper, the system will hang after setting the jumper and rebooting to start the update procedure.
Workaround: Use the standard procedure for updating BMC firmware. The "BMC FRC UP" jumper will not be supported until the issue is addressed
Status: FIXED – This issue was fixed in BIOS 7.2

17. Enabling fixed disk boot sector write protect option fails

Problem: After enabling the BIOS option "Fixed Disk Boot Sector Write Protect" the hard disk's boot block is still not protected.
Workaround: None
Status: FIXED – This option is fixed in BIOS 10.0

18. L440GX+ Diagnostics 1.01 or 1.02 dos not detect 256MB and 512MB DIMMS properly

Problem: The L440GX+ Daignostic Utility 1.01 and 1.02 does not accurately detect 256MB or 512MB DIMMs if all DIMM slots are populated.
Workaround: To valdiate the memory subsystem on the L440GX+ using the Diagnostic Utility, use either upto 3 of the larger DIMMS, listed above, or use DIMMs smaller than 256MB.
Status: FIXED – This issue has been addressed in L440GX+ Diagnostics rev 1.03

19. Japanese Language support in system BIOS not functioning as it should

Problem: After selecting Japanese language support in BIOS setup, and rebooting the system, the POST diagnostic screen will have several items scrambled on the screen. In addition, after re-entering BIOS Setup, all BIOS Setup options will be blank.
Workaround: At this time the only workaround is to not select the Japanese Language. If the Japanese language option is selected, you can restore the options in BIOS setup by scroll down to the language support option, which is the only viewable option on the Main Menu, highlight and select Japanese, and the options return.
Status: FIXED - This issue is fixed in BIOS 11.0

20. The Emergency Management Port (EMP) and console redirection will not function properly if the POST Diagnostics screen is disabled (Default) in BIOS Setup

Problem: With system BIOS 9.x or later installed, keeping the default BIOS setting "POST Diagnostics Screen: Disabled" (default), when attempting to access the system via the Emergency Management Port (EMP) or attempting Console redirection, the receiving console will be blank. The connection will be made, however there will be a blank screen preventing the user from seeing anything on the screen.
Workaround: In order to access the system via the Emergency Management port and using console redirection, the BIOS setup option "POST Diagnostic Screen" should be set to "ENABLED". This will cause the default POST Splash Screen to not appear during POST keeping the video in a text mode. Having the POST Splash screen display, changes the video mode to a graphics mode which is NOT supported when accessing the system via the Emergency Management Port.
Status: No Fix – Because the L440GX+ must meet Microsoft's SDG 2.0 requirements, the POST graphical Splash screen must be displayed during POST by default.

21. Dual SRCU21 (Talo) configuration in L440GX+ server board may cause system hang during POST.

Problem: If two SRCU21 adapters are installed in the L440GX+ running a BIOS reversion prior to 12.1, the system may not complete POST and may hang.
Implication: The system may not complete POST and hang.

Workaround: None.
Fix: Update the system BIOS to resolve this issue.
Status: Fixed in L440GX+ system BIOS 12.1.

22. NIC Teaming features originally planned for PBA# -515 and AA# -011, were not implemented

Problem: On-board Network Interface Card (NIC) teaming features, originally scheduled to be supported on the L440GX+ board starting with PBA# 704293-515 and AA# 721242-011, was not implemented in the factory.
Implications: Users trying to configure and use the NIC teaming features on the L440GX+ using the on-board NIC as the "Server NIC", will not be able to do so.
Workarounds: The NIC Teaming features can only be used when one of the Add-in NICs is an Intel® Pro100+ Server NIC.
Status: Fixed - The on-board NIC teaming features were added to L440GX+ server boards having a PBA# of 704293-603 or an AA# 721242-013. All L440GX+ boards build after the PBA and AA numbers listed will have the features enabled.

23. When EMP is set to "Always Active", accessing the EMP port with a modem cannot be done.

Problem: If the Emergency Management Port (EMP) is configured as "Always Active", anyone trying to call into the system using a modem will not be able to. The Modem will never establish a connection
Implications: If EMP is set to "Always Active", meaning the BMC is always controlling the COM2 serial port, anyone trying to perform remote diagnostics to an L440GX+ based system using a modem will not be able to.
Workarounds: Configure the EMP Access mode in BIOS setup to "Pre-Boot Only". This will only allow access to the EMP port using a modem when an OS is not running. IE: when the system is down or during POST. Once POST has completed, control of the EMP port is no longer controlled by the BMC and remote access will be denied.
Status: Fixed – This issue has been addressed in BMC firmware rev 1.14

DOCUMENTATION CHANGES

1. AT style front panel pinout table corrected

A 19-pin single inline header labeled J6J1 is provided for AT-style front panel connections, e.g., power, LED indicators, and reset. The connector has the following pinout:

Table 2-13. AT Front Panel Header Pinout

Pin	Signal
1	Pwr_Cntrl_Fp – 5V_STNDBY
2	Ground
3	No Pin
4	Hd_LED_Pwr – VCC
5	No Pin
6	Fp_HD_Act
7	Hd_LED_Pwr – VCC
8	Ground
9	No Pin
10	Spkr_Int
11	Spkr_Out
12	Ground
13	No Pin
14	Pwr_LED
15	No Pin
16	Ground
17	Rst_Fp
18	Fp_Sleep
19	Ground

Status: This was updated in the L440GX+ Technical Product Specification (TPS) rev. 1.0

2. Clarifications made to which Adaptec ARO RAID card is supported

In the L440GX+ Technical Product Specification (TPS), all references for the Adaptec ARO SCSI RAID card will be changed to "Adaptec ARO-1130U2 RAIDPort", to better identify which Adaptec ARO card the L440GX+ server board has support for.

Status: This was updated in the L440GX+ Technical Product Specification (TPS) rev. 1.0

3. All references to Intel® Pentium® Pro in the L440GX+ 0.9 TPS will be changed to Intel® Pentium® II

To avoid confusion, all references to Intel® Pentium® Pro in the L440GX+ 0.9 TPS will be changed to Intel® Pentium® II

Status: This was updated in the L440GX+ Technical Product Specification (TPS) rev. 1.0

4. Clarification of SCSI termination in L440GX+ Product Guide

To avoid confusion about termination of the L440GX+ SCSI bus when using LVDS devices the following text has been rewritten on page 15 in the second paragraph of the SCSI controller section.

> "The SCSI bus is terminated on the server board with active terminators that cannot be disabled. The onboard device must always be at one end of the bus. The device at the end of the cable must be terminated. LVDS devices generally do not have termination capabilities. Non-LVDS devices generally are terminated through a jumper or resistor pack. If your device does not have a termination jumper or resistor pack, you must add a terminator to the end of the cable. A terminator is not supplied with your board. You must purchase one separately."

Status: To be updated in the L440GX+ Server Board Product Guide, Order Number: 722077-003

5. Clarification of PERR# in the L440GX+ TPS

To avoid confusion about the function of the PCI error (PERR#) signal the L440GX+, Section 7.3.1 PCI Bus Error, located on page 78 of the L440GX+ TPS will be corrected as follows.

> The second sentence reads "the BIOS can be instructed to enable or disable reporting PERR# and SERR# through NMI." This will be corrected to remove all references to PERR#. The Eighth sentence reading "The same is true for PERR#" will be removed.

Status: To be updated in the L440GX+ Technical Product Specification (TPS)

6. Corrected Table showing System Event Logging Formats

The "System Event Logging Format" table located in the L440GX+ BIOS EPS rev 1.0 showed an incorrect format for Single Bit Memory Errors and Multi Bit Memory Errors.

> BIOS complies with the Platform Sensor and Event Interface EPS, Revision 1.0. The BIOS always uses a software ID of 0 to log POST errors. SMM handler uses software ID of 10h. OEM user binary should use software IDs of 1 and SMM User Binary should use an ID of 11h. The Software ID allows external software to find the origin of the event message.
>
> The BIOS uses the following sensor numbers while logging events. Application software can examine the sensor number field in the log record to determine the source of error. The *Platform Sensor and Event Interface EPS* requires that distinct sensor numbers are used for different error sources.

System Event Logging Format

Event Types	**Sensor Type/Sensor #/ Type Code/Data bytes 1,2,3.**
single bit memory error	0C *EF E7 40 DIMM# FF
multi bit memory error	0C *EF E7 41 DIMM# FF
Memory parity error	0C *EF E7 02 FF FF
front panel NMI	13 28 E7 00 FF FF
bus timeout	13 *EF E7 01 FF FF
I/O chk	13 *EF E7 02 FF FF
Software NMI	13 *EF E7 03 FF FF

PCI PERR	13 *EF E7 04 FF FF
Note: * Sensor # = 0EFh (not applicable). Other fields are sufficient enough to identify type of errors.	

The BIOS treats all the above sensors as discrete sensors. The 4 bit offset field in the first event data byte indicates the exact cause of the error. In all the events logged by the BIOS, up to 2 OEM data bytes are used to indicate the physical location of the error, such as the DIMM row number. Application software must examine these bytes to point to the exact source of error within a 'virtual sensor' Table X describes the various fields in the event request message, as sent by the BIOS.

Status: The table and paragraphs shown will replace the original document entry in the next EPS revision.

7. L440GX+ BIOS revs 9.1 and later adds two new BIOS setup options

L440GX+ BIOS rev 9.1 and later have added two new BIOS Setup options in the BIOS setup utility. "Boot-Time Diagnostic Screen: Enable/Disable" and "Extended RAM Step"

The "Boot-Time Diagnostic Screen: Enable/Disable" option gives the ability to enable or disable the system diagnostic screen from displaying during POST. The default for this option is "Disabled". With this option disabled, a "Manufactured by Intel" splash screen will be displayed instead of the diagnostic screen.

The "Extended RAM Step" option gives the ability to define how extended memory is tested during POST. The available options are:"1 MB", "1 KB", "Every Location", "No Memory test". The default setting for this option is "No Memory Test".

This has been added to the L440GX+ Users Guide part number 722077-005

8. Accessing (F2) BIOS setup utility with BIOS Rev 9.1 and later

With the Boot-Time Diagnostic Screen set to "Disabled" (Default) in the BIOS setup utility, the "Manufactured by Intel" splash screen prevents anyone from seeing the "(F2) BIOS Setup" text during POST. To enter the "F2 BIOS setup" option, do the following:

- During POST while the "Manufactured by Intel" banner is displayed, hit the <ESC> key. This will clear the banner from the screen allowing the "F2 BIOS Setup" option to be displayed. Hit the F2 key and POST will enter the BIOS setup utility.

The F2 BIOS Setup option is only hidden when the Diagnostic screen is set to "Disabled".

See the L440GX+ TPS rev 2.0 for a complete description.

9. SECC processors are not supported with Grounded Retention Mechanisms (GRMs)

L440GX+ server boards that support Pentium® III 600E MHz and faster processors have changed from using Universal Retention Mechanisms (URMs) to Grounded Retention Mechanisms (GRMs). The GRM will only support SECC2 type processor packaging. Earlier Pentium III processors, having SECC packaging, are not compatible with GRMs and cannot be used.

This has been added to the L440GX+ Users Guide part number 722077-005

10. Pentium® III 550E and 600E MHz and faster processors are not supported on L440GX+ server boards with PBA# 704293-40x and earlier or AA# 721242-007 and earlier

L440GX+ server boards with a PBA # of 704293-40x and earlier or an AA# of 721242-007 and earlier will not support Pentium III 550E and 600E MHz processors or faster. Only L440GX+ server boards with a PBA# of 704293-50x and later or AA# 721242-008 and later will have support for ALL Pentium III processors supporting a 100MHz front side bus.
Installing a Pentium III 550E or 600E MHz or faster processor on an earlier board will produce an unpredictable and unstable server environment. and may damage either the processor and/or the server board. Having a Pentium III 550E or 600E MHz or faster processor on an earlier board is **NOT** a supported configuration.

11. The following processor extraction procedure is recommended when removing processors from Grounded Retention Mechanisms (GRMs) on the L440GX+

Note: This procedure has been verified in the Intel Astor2 and Columbus III server chassis. The process may vary slightly when using another chassis. Use of additional extraction tools, ie: screwdrivers, pliers, etc… is not recommended as they may slip and damage the board or components on the board.

- It is easiest to remove the processor with the server board mounted in a chassis. This will provide support and help prevent bending of the server board.
- Follow all appropriate Electro-Static Discharge precautions whenever working on or near the server board or any of its add-in components.
- Remove the AC power cord from the power supply. The system AC power is only "Off" if the power cord is removed from the power supply.
- Place the system on its side
- Remove side cover (See your system or chassis documentation for instructions)
- Orient the server board so the white GRM is on the side farthest away from you.
- With your right thumb, push out the top of the white GRM toward the edge of the board. The GRM is very rigid, so only a small amount of tilt is possible.
- While pushing out the white GRM with your right thumb, with your left hand grasp both sides of the processor on the side nearest the white GRM and pull up.
- You should be able to rotate the processor out of the processor slot. Once free of the white GRM, the processor may be removed completely.

12. The 1.0 revision of the L440GX+ TPS incorrectly identifies COM1 and COM2 in Figure 1 of the document.

COM2 should be shown directly next to the Keyboard/mouse connectors. COM1 should be shown between COM2 and the Network interface connector.
Status: This has been fixed in the 2.0 Revision of the L440GX+ TPS

13. Table showing supported processors on the L440GX+

Processor Family	Frequency	Cache size / Type	Packaging
Pentium II	350 MHz	512 KB Discrete L2	SECC
Pentium II	400 MHz	512 KB Discrete L2	SECC
Pentium II	450 MHz	512 KB Discrete L2	SECC
Pentium III	450 MHz	512 KB Discrete L2	SECC2
Pentium III	500 MHz	512 KB Discrete L2	SECC2
Pentium III	550 MHz	512 KB Discrete L2	SECC2
Pentium III	550E MHz	256 KB ATC L2	SECC2
Pentium III	600 MHz	512 KB Discrete L2	SECC2
Pentium III	600E MHz	256 KB ATC L2	SECC2
Pentium III	650 MHz	256 KB ATC L2	SECC2
Pentium III	700 MHz	256 KB ATC L2	SECC2
Pentium III	750 MHz	256 KB ATC L2	SECC2
Pentium III	800 MHz	256 KB ATC L2	SECC2
Pentium III	850 MHz	256 KB ATC L2	SECC2
Pentium III	1 GHz	256 KB ATC L2	SECC2

Note: L440GX+ server boards having a PBA# of 704293-40x and earlier or an AA# of 721242-007 or earlier (where x is any number and earlier boards will have a smaller dash number) will **not** support Pentium III processors operating at 550E MHz, 600E MHz and faster. The PBA or AA number can be found on a white adhesive label near the edge of the component side of the server board below the ISA connector. Older L440GX+ boards will support Pentium III processors operating at frequencies up to and including 600 MHz.

14. Update to the L440GX+ component placement diagram, as shown in the rev 3.0 Technical Product Specification. The new diagram shows the addition of the 10-pin power connector found on L440GX+ server boards having a product code of BOXL440GX-H and later. The 10-pin power connector is used when the L440GX+ server board is integrated into an Intel SC5000 server chassis with redundant power supplies.

Component and Connector Placement

The following diagram shows the placement of major components and connectors on the L440GX+ server board.

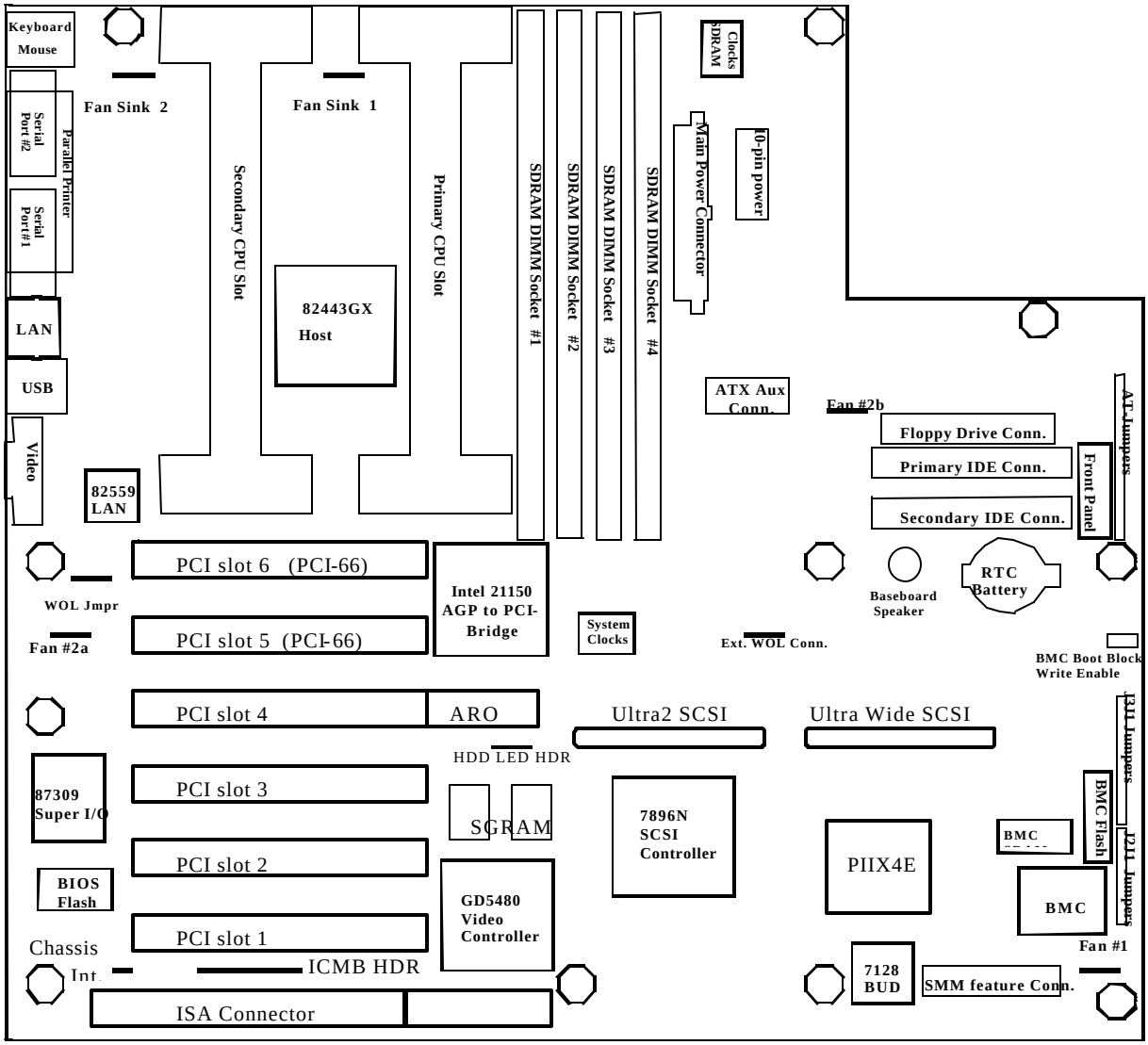

Figure 1-1. L440GX+ Server Board Layout