intel® Technical Advisory

TA-639-2

5200 NE Elam Young Parkway
Hillsboro, OR 97124

March 19, 2003

Intel SE7501WV2/SE7501HG2 DDR 266 DIMM Slew Rate Observation Sighting

Products Affected

Product	Product Codes
SE7501WV2	BWV533SBB
SE7501WV2	SE7501WV2ATA, SE7501WV2SCSI, SE7501WV2SKU02
SE7501HG2	SE7501HG2 & BSE7501HG2

Description

Under certain conditions, Intel® validation teams have observed marginal signal quality on certain strobe signals, DQS_x[17:0], in the registered DDR 266 memory interface of the above listed server board products. Poor signal quality on the DQS signals will result in the MCH DDR read FIFO getting out of sync during memory READ transactions leading to single-bit or multi-bit errors on the DQ_x[63:0] signals. Depending on the system configuration, the system may hang and/or a system NMI should be generated.

This issue has only been observed in a validation environment using a registered 3 DIMMs/channel memory topology. Additionally, this issue has only been observed with DIMM modules exhibiting the following electrical characteristics:

- High slew rate DIMM populated in slot furthest away from the MCH is driving READ data back to the MCH **AND**
- High slew rate considered > 5.5 V/ns as measured in a system **AND**
- High Capacitive loading of the IDLE DIMMs in the slots closer to the MCH

Intel has identified five 3-DIMM/channel configurations that are susceptible to a system hang during testing in a validation environment:

DIMM 1A & 1B	DIMM 2A & 2B	DIMM 3A & 3B
Double-Banked	Double-Banked	Double-Banked
Single-Banked	Double-Banked	Double-Banked
Single-Banked	Single-Banked	Double-Banked
Single-Banked	Double-Banked	Empty
Double-Banked	Double-Banked	Empty

The issue has not been seen with commercially available software applications. Additionally, this issue has not been seen with the following memory topologies or DIMM types:

- 2 DIMMs/channel or 1 DIMM/channel memory topologies
- Un-buffered DIMM modules [Intel E7505 chipset only]

Root Cause

Intel has not yet root caused this issue, however the issue appears to be a platform level issue (meaning there are a number of components working together to cause this issue).

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Corrective Action / Resolution

Exposure to the five susceptible 3-DIMM/channel configurations can be minimized by disabling on die termination on the MCH (ODT). Disabling ODT with the susceptible 3-DIMM configurations has been validated by Intel as an acceptable configuration. On platforms Intel has tested with ODT disabled, Intel has NOT seen susceptibility with DIMMs exhibiting slew rates less than 7V/ns as measured in a system.

Intel has incorporated a software workaround for this issue by disabling ODT ONLY for the affected configurations. This workaround has been incorporated in SE7501WV2 BIOS P06 and later versions, and in SE7501HG2 BIOS P05 and later versions. Intel recommends that all customers update their SE7501WV2 and SE7501HG2 BIOS to these versions in order to avoid encountering this issue. The SE7501WV2 and SE7501HG2 BIOS updates may be obtained from http://support.intel.com at the following locations:

SE7501WV2: http://downloadfinder.intel.com/scripts-df/Product_Filter.asp?ProductID=904
SE7501HG2: http://downloadfinder.intel.com/scripts-df/Product_Filter.asp?ProductID=926

Intel continues to work with memory suppliers to investigate opportunities for adding additional margin to the platform in 3-DIMM/channel memory topologies. Intel is working with the memory industry to help ensure material with slew rates greater than 7V/ns is screened from production.

Please contact your Intel Sales Representative if you require more specific information about this issue.

Enterprise Platforms & Services Division
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