Intel® Server Chassis SR1450

Technical Product Specification

Part Number: D11535-001

Revision 1.0

April 2005

Enterprise Platforms and Services Marketing

Revision History

Date	Revision Number	Modifications
January 2005	0.8	Initial release based on SR1450 Beta product.
February 2005	0.9	SR1450 Silver product updates.
April 2005	1.0	SR1450 production product updates – added fan System Event Log table, and PSMI information.

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1. Intel® Server Chassis SR1450 Feature Summary

The Intel® Server Chassis SR1450 is a 1U server designed to support Intel® Server Board SE7520JR2. Both board and chassis have a feature set designed to support the high-density server market. This chapter provides a high-level overview of the chassis feature set. More detailed descriptions for each feature and sub-system can be found in the following chapters.

1.1 Chassis Views

Front View without outer Bezel – Showing Standard Control Panel Option

Front View with outer bezel – Showing Standard Control Panel Option

Front View without outer Bezel – Showing Intel® Local Control Panel Option

Front View with outer bezel – Showing Intel® Local Control Panel Option

Back View

Figure 1. Front and Back Chassis Views

1.2 Chassis Dimensions

Table 1. Chassis Dimensions

Height	43.25 mm	1.703”
Width	430 mm	16.930”
Depth	698 mm	27.480”
Max. Weight	15.9 kg	35.0 lbs

1.3 System Components

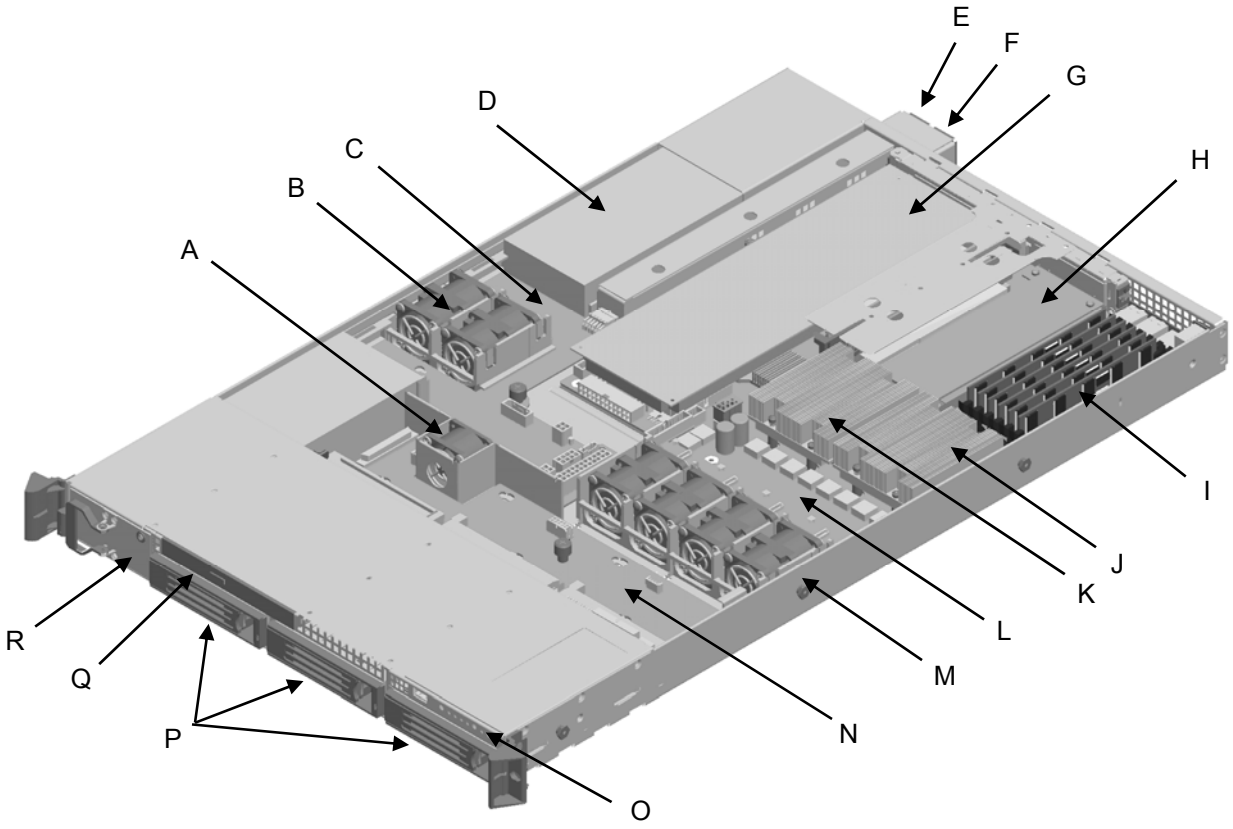


Figure 2. Major Chassis Components

A	One 28mm Fan (Cools first HDD bay & PCI Section)	J	Processor One
B	Two 56mm Fans (Cools Power Supply Section)	K	Processor Two
C	Power Distribution Board (PDB)	L	Server Board (Processor Air Duct Not Shown Here)
D	Back Power Supply Module	M	Four 56mm Fans (Cools Second & Third HDD Bay and Processor/DIMM Section)
E	AC Inlet For Back Power Supply Module	N	3.5” HDD Backplane (SCSI or SATA/SAS Version)
F	AC Inlet For Front Power Supply Module	O	Front Panel (Standard Version Shown)
G	Full Height PCI Adapter Card	P	3.5” HDD Carriers
H	Low Profile PCI Adapter Card	Q	Slim-line Bay (Optical or Floppy Drive)
I	Up to Six DIMMs	R	Front Power Supply Module

Contained on the back of the chassis are cutouts for all external I/O connectors found on the server board. The I/O connector locations are pre-cut, so the use of an I/O shield is not required.

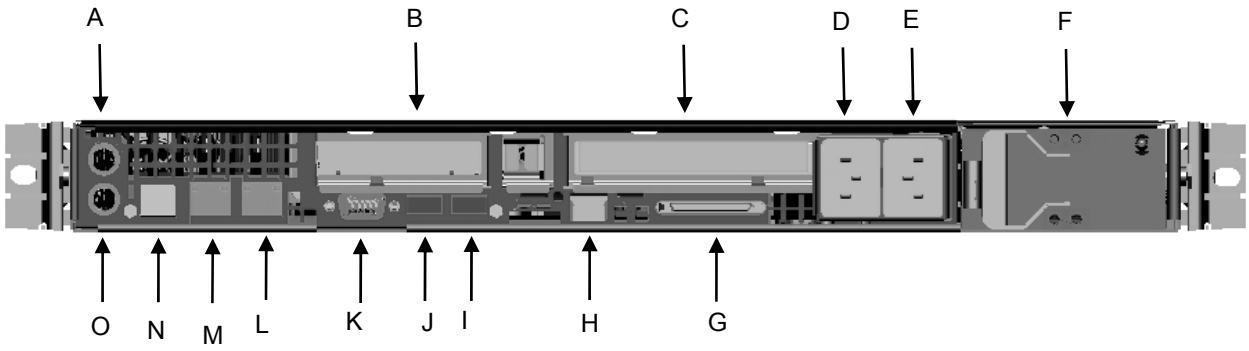


Figure 3. Back Panel Feature Overview

A	PS2 Mouse Connector	I	USB 1 Connector
B	PCI Card Bracket (Low Profile)	J	USB 2 Connector
C	PCI Card Bracket (Full Height)	K	Video Connector
D	AC Power Receptacle (Front Power Supply)	L	NIC 2 Connector
E	AC Power Receptacle (Back Power Supply)	M	NIC 1 Connector
F	Back Power Supply Module	N	RJ45 Serial B port
G	SCSI Connector (SCSI Server Board Version Only)	O	PS2 Keyboard Connector
H	Intel® Management Module (IMM) Advanced Edition with Network Interface Card (Optional)		

1.4 Hard Drive and Peripheral Bays

The Server Chassis SR1450 is designed to support several different hard drive and peripheral configurations. The hard drive bay is designed to support up to three 3.5-inch hot-swappable SATA/SAS or SCSI drives. Each drive configuration requires an orderable kit, which includes the necessary cables, drive trays and applicable backplane.

The slim-line peripheral bay is capable of supporting any of the following slim-line devices: CDROM drive, DVD drive, DVD/CDR drive, or floppy drive. If both an optical drive and floppy drive are required, an optional kit is available to convert the middle 3.5-inch hard drive bay to a floppy drive bay. The kit includes the slim-line floppy drive mounting tray.

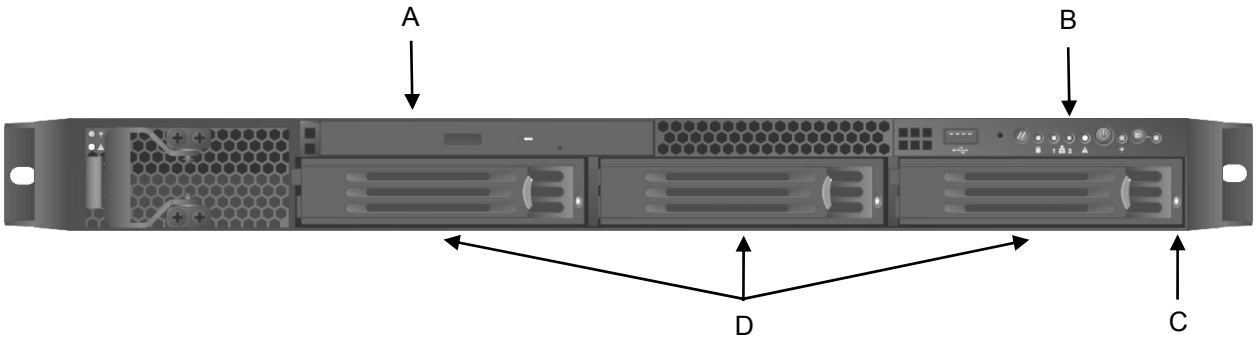


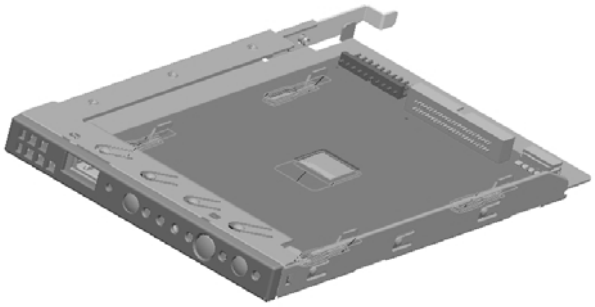
Figure 4. Peripheral Feature Overview

A	Slim-line Drive Bay (Optical Drive or Floppy)
B	Control Panel (Standard Version Shown)
C	Hard Drive Fault/Activity LED
D	3.5-inch Hard Drive Bays (Middle Bay Supports Floppy Conversion Kit)

1.5 Control Panel Options

The Server Chassis SR1450 can support either of two control panels, the Standard Control Panel or the Intel® Local Control Panel with LCD support. The control panel assemblies are pre-assembled and modular in design. The entire module assembly slides into a predefined slot in the front of the chassis.

Standard Control Panel



Local Control Panel With LCD

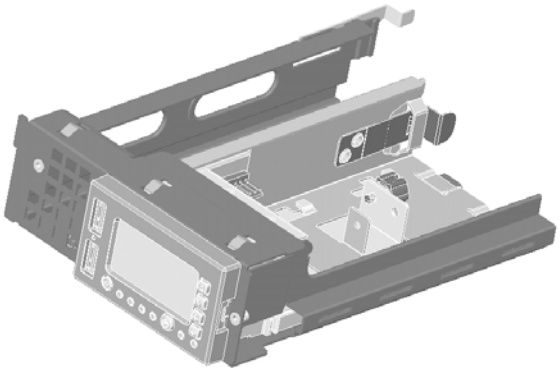


Figure 5. Control Panel Modules

Note: The Server Chassis SR1450 does not come configured with a control panel pre-installed. The Standard Control Panel or the Intel® Local Control Panel must be ordered separately.

The standard control panel supports several push buttons and status LEDs, along with a USB port to centralize system control, monitoring, and accessibility in a compact design. The following diagram provides an overview of the layout and functions of the standard control panel.

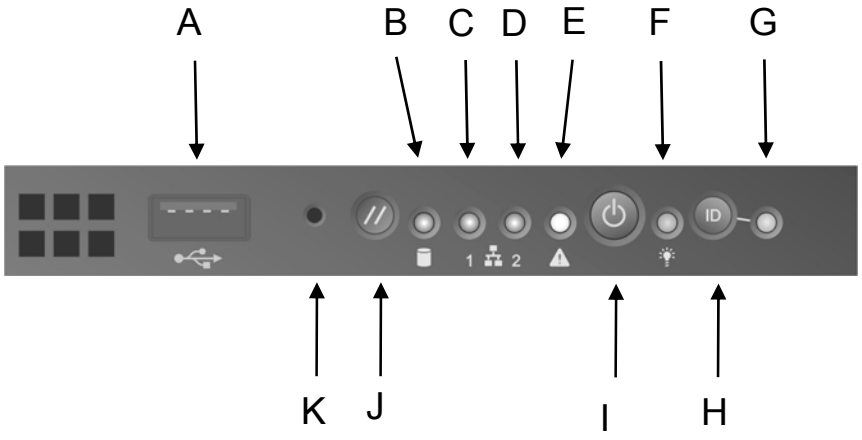


Figure 6. Standard Control Panel Overview

A	USB 2.0 Port	G	System Identification LED

B	Hard Drive Activity LED	H	System Identification Button
C	NIC #1 Activity LED	I	Power / Sleep Button
D	NIC #2 Activity LED	J	System Reset Button
E	System Status LED	K	Recessed NMI Button (Tool Required)
F	Power / Sleep LED		

The Intel® Local Control Panel utilizes a combination of control buttons, LEDs, and LCD display to provide system accessibility, monitoring, and control functions. The following diagram provides an overview of this Local Control Panel.

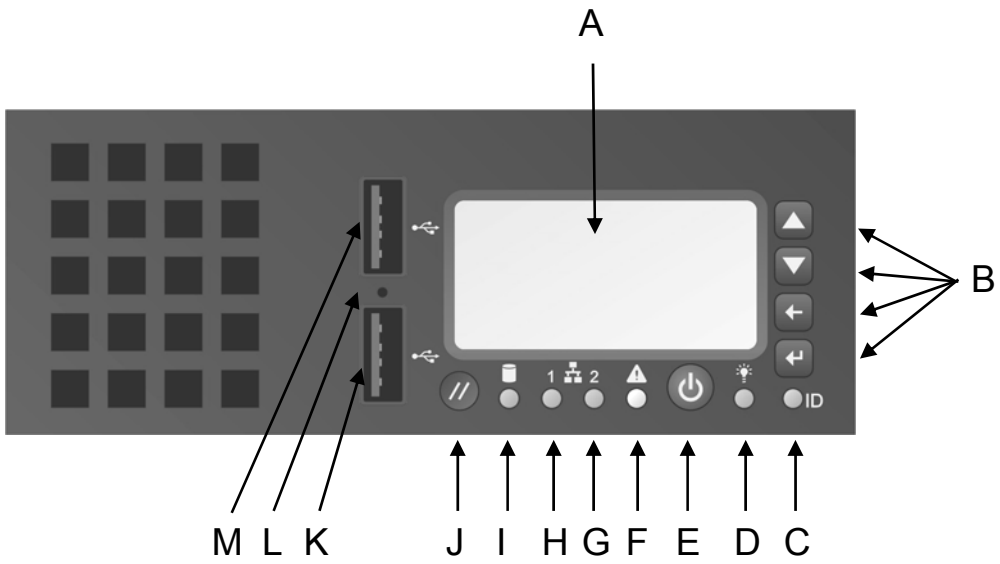


Figure 7. Intel® Local Control Panel LCD Overview

A	LCD Display	G	NIC 2 Activity LED
B	LCD Menu Control Buttons	H	NIC 1 Activity LED
C	System Identification LED	I	Hard Drive Activity LED
D	Power LED	J	System Reset Button
E	System Power Button	K	USB 2.0 Port
F	System Status LED	L	NMI Button (Tool Required)
		M	USB 2.0 Port

Note: The Intel® Local Control Panel can only be used when either the Intel® Management Module Professional Edition or Advanced Edition is installed in the system.

1.6 Power Sub-system

The chassis power sub-system consists of up to two 520-watt power supply modules (supporting a 1+0 or redundant 1+1 configuration) and a power distribution board (PDB). The power sub-system provides several integrated management features including:

- Module status/fault LED (located on each Power Supply Module)
- Power distribution board fault LED (located on the PDB)

- Two fan fault LEDs (located on the PDB)
- Over-temperature protection circuitry
- Over-voltage/current protection circuitry
- 240VA protection circuitry

With the addition of an Intel® Management Module and Intel® Server Management Software, the power subsystem is capable of supporting several system management features including:

- Remote Power On/Off
- Status Alerting
- FRU Information Reporting (each power supply module and PDB)
- PSMI functionality

The power supply operates within the following voltage ranges and ratings:

- 100-127VAC (V) ~ at 50/60 Hertz (Hz); 6.7 A maximum
- 200-240VAC~ at 50/60 Hz; 3.4 A maximum

1.7 System Cooling

The chassis provides four redundant system fans and two redundant power supply fans. Note that the system fans are only redundant when running Low Voltage processors and the power supply fans are only redundant in the 1+1 power supply configuration. There is also one additional non-redundant system fan cooling the PCI section. When external ambient temperatures remain within specified limits, the cooling system will provide sufficient air flow for all hot-swap drive, processors, memory, and add-in card configurations.

1.8 Chassis Security

The chassis provides support for several platform security features including a lockable front bezel, chassis intrusion switch, and a Kensington* style lock attach point.

1.9 Rack and Cabinet Mounting Options

The chassis is designed to support 19-inch wide by up to 30-inch deep server cabinets. The chassis can be configured to support a fixed rack mount kit or a tool-less sliding rail kit. The fixed rack mount kit can be configured to support both 2-post racks and 4-post cabinets. The tool-less sliding rail kit is used to mount the chassis into a standard (19-inch wide by up to 30-inch deep) EIA-310D compatible server cabinet.

1.10 Front Bezels

The optional outer front bezel is made of molded plastic and uses a snap-on design. When installed, it's design allows for maximum airflow. Separate outer front bezels are available to support systems that use either a Standard Control Panel or an Intel® Local Control Panel.

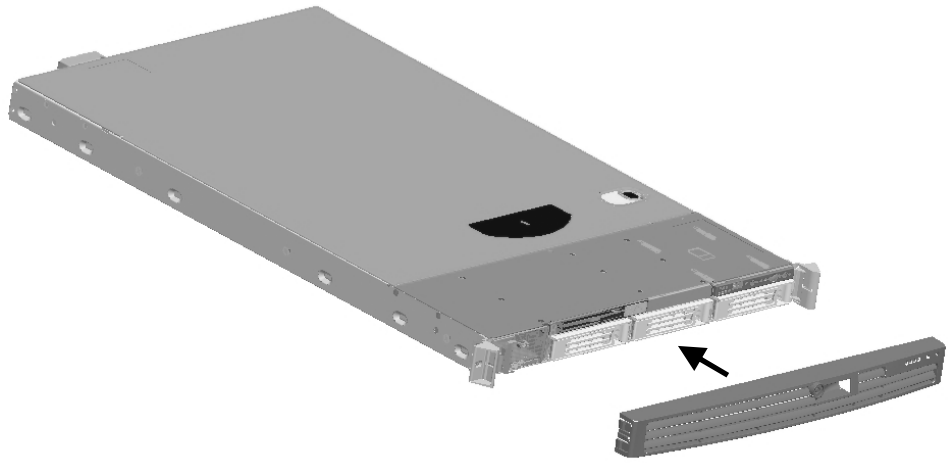


Figure 8. Optional Front Bezel

Light pipes in the outer front bezel support the Standard Control Panel and allow the system status LEDs to be monitored with the outer bezel installed.

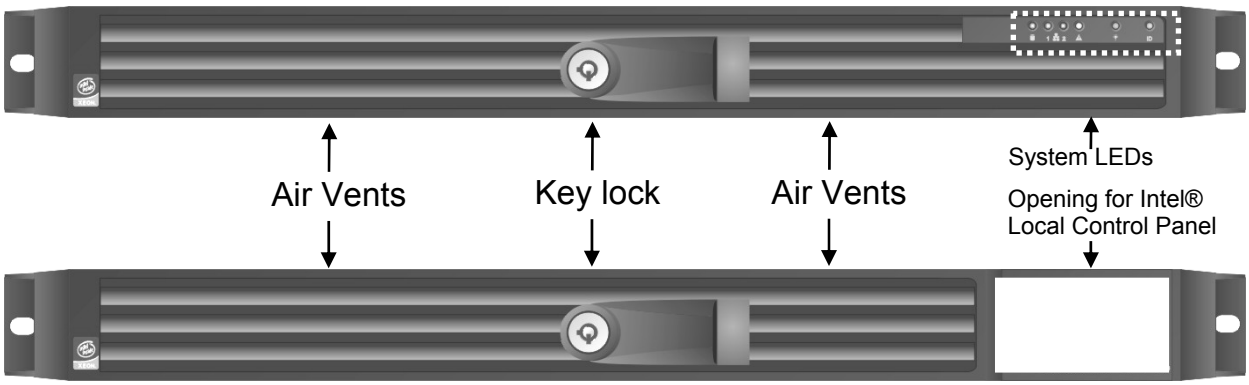


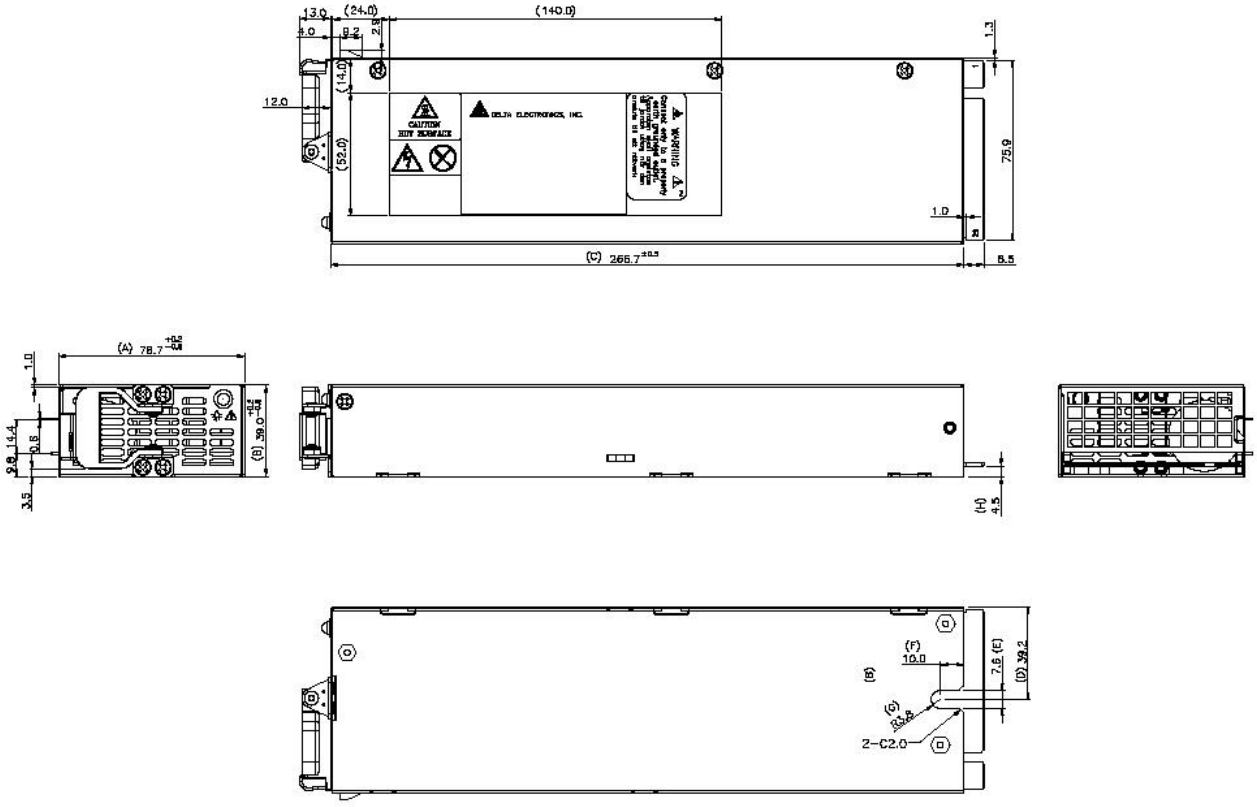
Figure 9. Front Bezel Options

2. Power Sub-System

The power sub-system of the Server Chassis SR1450 consists of 1+1 redundant 520-W power supply modules with 2 outputs: 12V and 5VSB. There is also a power distribution board with 7 additional outputs: 3.3V, 5V, 12V1, 12V2, 12V3, 12V4, and -12V. The form factor fits into a 1U system and provides a wire harness output to the rest of the system. Two IEC-320 C14 AC connectors are provided for each power supply module at the rear of the chassis. There are two redundant 56-mm fans for power subsystem cooling.

2.1 Module Mechanical Overview

The power supply module is specifically designed for use in the Server Chassis SR1450.



Note: All dimensions are in mm.

Figure 10. Module Enclosure Drawing

The chassis is designed to allow for tool-less removal and insertion of the power supply modules. Stop features on the chassis base and chassis top cover ensure a tight fit and prevent the power supply from moving out of place while the system is in transit. The Server Chassis SR1450 ships with one power supply module in the front power supply slot. A filler panel is installed in the back power supply slot (the filler panel is specifically designed for use in the rear power supply slot).

2.2 PDB Mechanical Overview

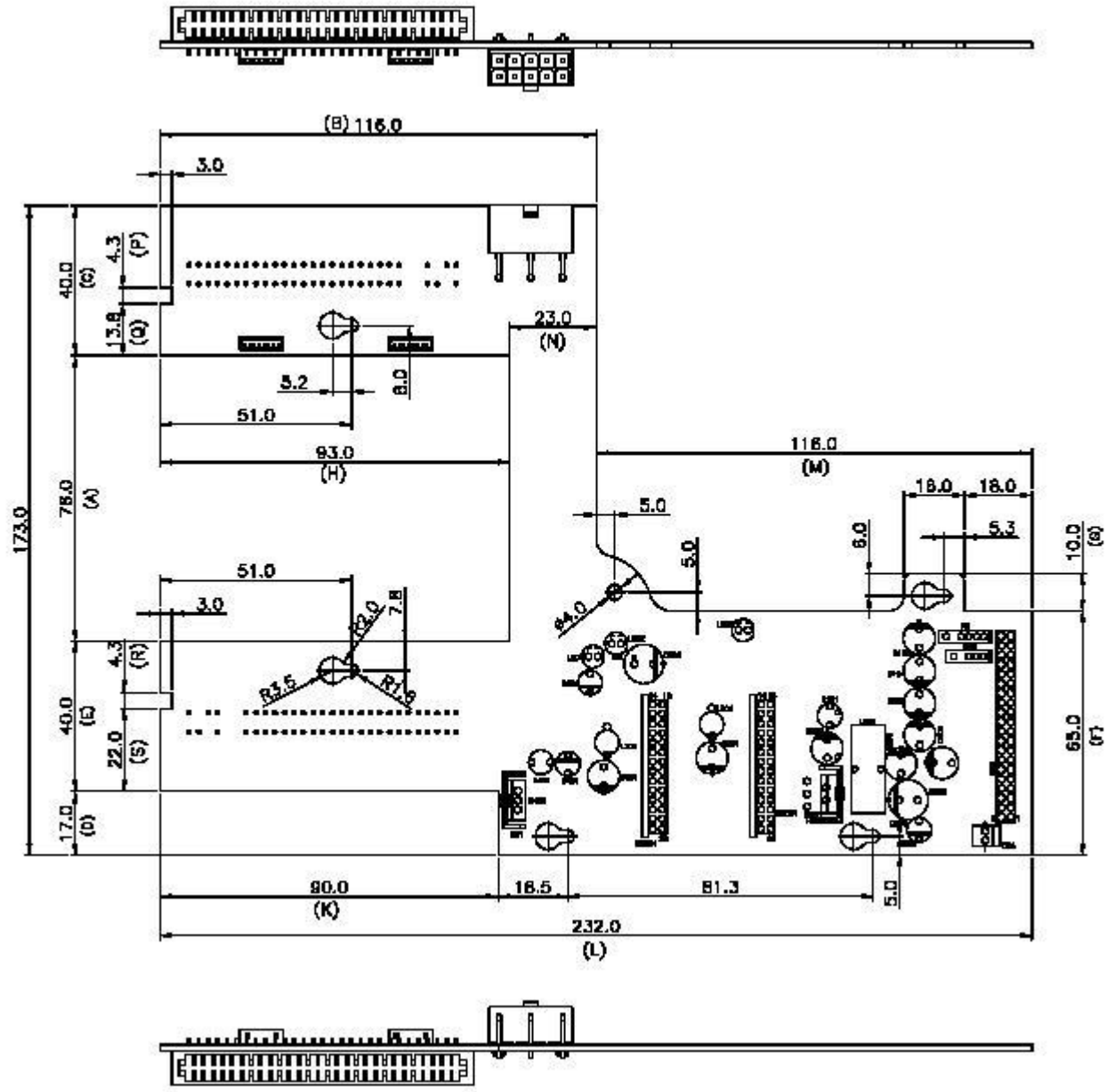


Figure 11. PDB Drawing

2.3 Airflow Requirements

The power sub-system incorporates two 56-mm fans for power subsystem cooling and system cooling. The fans will provide no less than 11.4 CFM airflow through the power supplies when installed in the system. Air flowing through the back power supply is pre-heated from the front power supply (if installed) and exhausts out the back.

2.4 Temperature Requirements

The power supply will operate within all specified limits over the T_{op} temperature range. See Table 56. Environmental Limits Summary. The average air temperature difference (ΔT_{ps}) from the inlet to the outlet of the front power supply will not exceed 15C. The power supply meets UL enclosure requirements for temperature rise limits.

2.5 Module Output Connector

Below is the pin-out for the connection between the power supply module and the PDB.

Table 2. Module Output Connector

PIN	TOP	PIN	BOTTOM
1	AC LINE	1	AC LINE
2	AC LINE	2	NC
3	NC	3	AC NEUTUAL
4	AC NEUTUAL	4	AC NEUTUAL
5	NC	5	NC
6	NC	6	NC
7	GND	7	GND
8	GND	8	GND
9	GND	9	GND
10	GND	10	GND
11	GND	11	GND
12	GND	12	GND
13	GND	13	GND
14	GND	14	+12V
15	+12V	15	+12V
16	+12V	16	+12V
17	+12V	17	+12V
18	+12V	18	+12V
19	+12V	19	+12V
20	+12V	20	+12V
21	+12V	21	+12V
22	GND	22	7V FAN
23	GND	23	+5VSB
24	PS_ON	24	+5VSB
25	PS_KILL	25	RETURNS
26	PWOK	26	I2C SCL
27	SMBALERT	27	I2C SDA
28	+12LS	28	A0
29	Vbias	29	+12VRS

Note: The AC input for each power supply module shall connect through the card edge connector from the power distribution board to the power supply module.

2.6 AC Input Connector On Power Distribution Board

The AC Input Power Connector housing on the PDB is a 10 Pin Molex Mini-Fit Jr. PN# 39-30-0100 or equivalent

Table 2. AC Input Power Connector

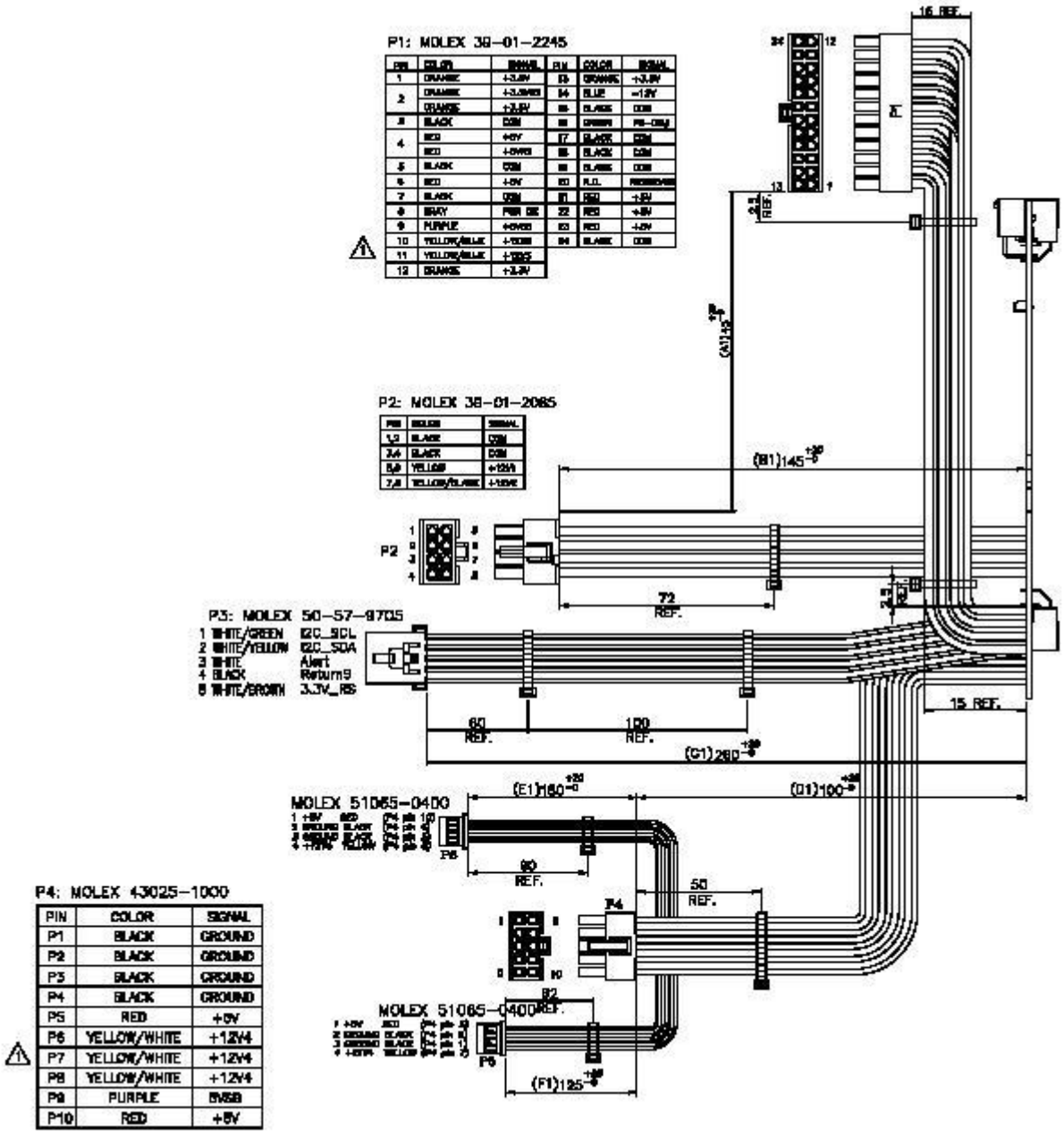
Pin	Signal	Pin	Signal
1	AC1 NEUTRAL	6	AC1 LINE
2	No Connect	7	No Connect
3	GND	8	GND
4	No Connect	9	No Connect
5	AC2 NEUTRAL	10	AC2 LINE

2.7 Output Cable Harness On Power Distribution Board

Listed or recognized component appliance wiring material (AVLV2), CN, rated min 105◦C, 300Vdc shall be used for all output wiring.

Table 3. Cable Lengths

From	Length mm	To connector #	No of pins	Description
Power Distribution Board (PDB)	150	P1	2x12	Server Board Power Connector
Power Distribution Board (PDB)	145	P2	2x4	Processor Power Connector
Power Distribution Board (PDB)	260	P3	1x5	Power Signal Connector
Power Distribution Board (PDB)	100	P4	2x5	Hard Drive Interface Board Power Connector
P4	125	P5	1x4	Slim-line CD-ROM power
P4	180	P6	1x4	Slim-line Floppy Disk Drive power



PIN	COLOR	SIGNAL
P1	BLACK	GROUND
P2	BLACK	GROUND
P3	BLACK	GROUND
P4	BLACK	GROUND
P5	RED	+5V
P6	YELLOW/WHITE	+12V4
P7	YELLOW/WHITE	+12V4
P8	YELLOW/WHITE	+12V4
P9	PURPLE	5VSB
P10	RED	+5V

Figure 12. Power Distribution Board Harness Detail

2.7.1 P1 – Main Power Connector

Connector housing: 24-Pin Molex Mini-Fit Jr. 39-01-2245 or equivalent
Contact: Molex Mini-Fit, HCS, Female, Crimp 44476 or equivalent

Table 4. P1 Main Power Connector

PIN	SIGNAL	18 AWG COLOR	PIN	SIGNAL	18 AWG COLOR
1	+3.3 VDC	Orange	13	+3.3 VDC	Orange
2	+3.3 VDC*	Orange	14	-12 VDC	Blue
3	COM	Black	15	COM	Black
4	+5 VDC*	Red	16	PSON#	Green
5	COM	Black	17	COM	Black
6	+5 VDC	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR OK	Gray	20	Reserved	N.C.
9	5VSB	Purple	21	+5 VDC	Red
10	+12V3	Yellow/Blue Stripe	22	+5 VDC	Red
11	+12V3	Yellow/Blue Stripe	23	+5 VDC	Red
12	+3.3 VDC	Orange	24	COM	Black

Notes:
* 5V Remote Sense Double Crimped into pin 4.
* 3.3V Locate Sense Double Crimped into pin 2.

2.7.2 P2 – Processor Power Connector

Connector housing: 8-Pin Molex 39-01-2085 or equivalent
Contact: Molex 44476-1111 or equivalent

Table 5. P2 Processor Power Connector

PIN	SIGNAL	18 AWG COLOR	PIN	SIGNAL	18 AWG COLOR
1	COM	Black	5	+12V1	Yellow
2	COM	Black	6	+12V1	Yellow
3	COM	Black	7	+12V2	Yellow/Black Stripe
4	COM	Black	8	+12V2	Yellow/Black Stripe

2.7.3 P3 – Power Signal Connector

Connector housing: 5-pin Molex 50-57-9705 or equivalent
Contacts: Molex 16-02-0087 or equivalent

Table 6. P3 Server Board Signal Connector

Pin	Signal	24 AWG Color
1	I^2C Clock	White/Green Stripe
2	I^2C Data	White/Yellow Stripe
3	Alert#	White
4	COM	Black
5	3.3RS	White/Brown Stripe

2.7.4 P4 – Backplane Power Connector

Connector housing: 10-Pin Molex Microfit PN# 43025-1000 or equivalent
Contact: Molex Microfit, Female, Crimp 43030-0007 or equivalent

Table 7. P7 Hard Drive Power Connector

PIN	SIGNAL	24 AWG COLOR	PIN	SIGNAL	24 AWG COLOR
1	COM	Black	6	+12V4	Yellow/White Stripe
2	COM	Black	7	+12V4	Yellow/White Stripe
3	COM	Black	8	+12V4	Yellow/White Stripe
4	COM	Black	9	+5VSB	Purple
5	+5V	Red	10	+5V	Red

2.7.5 P5 – Slim-line CD-ROM Power Connector

Connector housing: 4-Pin Molex PN# 51065-0400 or equivalent
Contact: Molex PN 50212-8000 or equivalent

Table 8. P5 Slim-line CD-ROM Power Connector

Pin	Signal	26 AWG Color
1	+5V (P4 pin 5)	Red
2	Ground (P4 pin 2)	Black
3	Ground (P4 pin 1)	Black
4	+12V4 (P4 pin 7)	Yellow

2.7.6 P6 – Slim-line Floppy Disk Drive Power Connector

Connector housing: 4-Pin Molex PN# 51065-0400 or equivalent
Contact: Molex PN 50212-8000 or equivalent

Table 9. P5 Slim-line Floppy Disk Drive Power Connector

Pin	Signal	26 AWG Color
1	+5V (P4 pin 10)	Red
2	Ground (P4 pin 4)	Black
3	Ground (P4 pin 3)	Black
4	+12V4 (P4 pin 8)	Yellow

2.8 AC Input Voltage Specification

The power supply must operate within all specified limits over the following input voltage range, shown in the table below. No harmonic distortion of up to 10% total harmonic distortion (THD) will cause the power supply to go out of specified limits. The power supply will power off if the AC input is less than 75VAC +/-5VAC range. The power supply will start up if the AC input is greater than 85VAC +/-4VAC. Application of an input voltage below 85VAC shall not cause damage to the power supply, including a fuse blow.

Table 10. AC Input Rating

PARAMETER	MIN	RATED	MAX	Start up VAC	Power Off VAC	Max Input AC Current	Max Rated Input AC Current
Voltage (110)	90 Vrms	100-127 Vrms	140 Vrms	85Vac +/- 4Vac	75Vac +/-5Vac	7.4 Arms[1,3]	6.67 Arms[4]
Voltage (220)	180 Vrms	200-240 Vrms	264 Vrms			3.7 Arms[2,3]	3.4 Arms[4]
Frequency	47 Hz	50/60Hz	63 Hz				

1 Maximum input current at low input voltage range is measured at 90Vac, at max load.
2 Maximum input current at high input voltage range is measured at 180VAC, at max load.
3 This is not to be used for determining agency input current markings.
4 Maximum rated input current is measured at 100VAC and 200VAC.

2.8.1 AC Inlet Connectors

There are two AC inlet connectors, one for each power supply module. Each AC input connector is an IEC 320 C-14 power inlet rated for 10A / 250VAC.

2.8.2 Efficiency

The power supply module has an efficiency of 78% at maximum load and over the specified AC voltages. The PDB board DC converters (5V & 3.3V) have a minimum efficiency of 85% over +12V line voltage range.

2.8.3 AC Line Transient Specification

AC line transient conditions are defined as “sag” and “surge” conditions. A “Sag” condition is also commonly referred to as “brown-out”. This condition occurs when the AC line voltage drops below nominal voltage conditions. A “Surge” condition occurs when the AC line voltage rises above nominal voltage.

The power supply meets the requirements under the following AC line sag and surge conditions.

Table 11. AC Line Sag Transient Performance

AC Line Sag				
Duration	**Sag**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
Continuous	10%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
0 to 1 AC cycle	100%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>10%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable

Table 12. AC Line Surge Transient Performance

AC Line Surge				
Duration	**Surge**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

2.8.4 AC Line Fast Transient (EFT) Specification

The power supply meets the EN61000-4-5 directive and any additional requirements in IEC1000-4-5:1995 and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.
- The supply meets surge-withstand test conditions under maximum and minimum DC-output load conditions.

2.8.5 AC Line Dropout / Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout of one cycle or less the power sub-system must meet dynamic voltage regulation requirements over the rated load. An AC line dropout of one cycle or less (20ms min) shall not cause tripping of any control signals or protection circuits (= 20ms holdup time requirement). If the AC dropout lasts longer than one cycle, the power supply will recover and meet all turn on requirements. The power supply meets the AC dropout requirement over rated AC voltages, frequencies, and output loading conditions. Any dropout of the AC line shall not cause damage to the power supply.

2.8.5.1 AC Line 5VSB Holdup

The 5VSB output voltage should stay in regulation under its full load (static or dynamic) during an AC dropout of 70ms min (=5VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

2.8.6 Power Recovery

The power supply will recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

2.8.6.1 Voltage Brown Out

The power supply complies with the limits defined in EN55024: 1998 using the IEC 61000-4-11:1995 test standard and performance criteria C defined in Annex B of CISPR 24.

A continuous input voltage below the nominal input range shall not damage the power supply or cause overstress to any power supply component. The power supply will return to a normal power up state after a brown out condition. Maximum input current under a continuous brown out shall not blow the fuse. The power supply should tolerate a 3min ramp from 90VAC voltage to 0VAC after the components have reached a steady state condition.

2.8.6.2 Voltage Interruptions

The power supply complies with the limits defined in EN55024: 1998 using the IEC 61000-4-11:1995 test standard and performance criteria C defined in Annex B of CISPR 24.

2.8.7 AC Line Inrush

The AC line inrush current shall not exceed 40A peak for up to one-quarter of the AC cycle, after which, the input current should be no more than the specified maximum input current. The peak inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (T_{op}). It is acceptable that AC line inrush current may reach up to 60A peak for up to 1 ms.

2.8.8 AC Line Isolation Requirements

The power supply meets all safety agency requirements for dielectric strength. Transformer isolation between primary and secondary windings must comply with the 3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage, the highest test voltage should be used. In addition the insulation system must comply with reinforced insulation per safety standard IEC 950. Separation between the primary and secondary circuits and primary to ground circuits complies with the IEC 950 spacing requirements.

2.8.9 AC Line Leakage Current

The maximum leakage current to ground for each power supply is 3.0mA when tested at 240VAC.

2.8.10 AC Line Fuse

Each power supply module has a single line fuse on the Line (Hot) wire of the AC input. The line fusing is acceptable for all safety agency requirements. The input fuse is a slow blow type. AC inrush current will not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

2.8.11 Power Factor Correction

The power supply incorporates a Power Factor Correction circuit.

2.9 DC Output Specification

2.9.1 Grounding

The ground of the pins of the power supply module and power distribution board output connectors provides the power return path. The output connector ground pins shall be connected to safety ground (power supply enclosure). This grounding is designed to ensure passing the maximum allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits are connected to protective earth ground. Resistance of the ground returns to chassis will not exceed 1.0 mΩ. This path may be used to carry DC current.

2.9.2 Remote Sense

The power supply modules and power distribution board have remote sense return (ReturnS) to regulate out ground drops for all output voltages; +3.3V, +5V, +12V1, +12V2, +12V3, -12V, and 5VSB. The power distribution board uses remote sense (3.3VS) to regulate out drops in the system for the +3.3V output. The +5V, +12V1, +12V2, +12V3, –12V and 5VSB outputs only use remote sense referenced to the ReturnS signal. The remote sense input impedance to the power supply must be greater than 200Ω on 3.3VS, 5VS. This is the value of the resistor connecting the remote sense to the output voltage internal to the power supply. Remote sense must be able to regulate a minimum of 300mV drop on the +3.3V output. The remote sense return (ReturnS) must be able to regulate a minimum of 200mV drop in the power ground return. Also, the power supply ground return remote sense (ReturnS) passes through the power distribution board and the output harness to regulate ground drops for its +12V and 5Vsb output voltages. The power supply uses remote sense (12VRS) to regulate drops up to the 240VA protection circuits on the PDB.

2.9.3 Output Power / Currents

The following table defines power and current ratings for the 520W power supply modules and power distribution board. The combined output power of all outputs shall not exceed the rated output power. The power supply must meet both static and dynamic voltage regulation requirements for the minimum loading conditions.

Table 13. Load Ratings

Voltage	Minimum Continuous Load	Maximum Continuous Load	Peak Load
+3.3V	1.5 A	16 A	-
+5V	1.0 A	16 A	-
+12V1	0.8 A	16 A	18 A
+12V2	0.8 A	16 A	18 A
+12V3	0.5 A	16 A	18 A
+12V4	0 A	10 A	16 A
-12V	0 A	0.5 A	-
+5VSB	0.1 A	2.0 A	2.5A

1. Maximum continuous total DC output power should not exceed 520W. 520W includes the two fans powered from the power distribution board.
2. Peak power and current loading are supported for a minimum of 12 seconds.
3. Combined 3.3V and 5V power should not exceed 100W.
4. 3.3V and 5V power is converted from 12V on the power distribution board

2.9.3.1 Standby Outputs

The 5VSB output shall be present when an AC input greater than the power supply turn on voltage is applied.

2.9.4 Voltage Regulation

The power sub-system output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. All outputs are measured with reference to the return remote sense signal (ReturnS). The 5V, 12V1, 12V2, +12V3, +12V4, –12V and 5VSB outputs are measured at the

power distribution connectors referenced to ReturnS. The +3.3V is measured at it's remote sense signal (3.3VS) located at the signal connector.

Table 14. Voltage Regulation Limits

PARAMETER	TOLERANCE	MIN	NOM	MAX	UNITS
+ 3.3V	- 5% / +5%	+3.14	+3.30	+3.46	V_{rms}
+ 5V	- 5% / +5%	+4.75	+5.00	+5.25	V_{rms}
+ 12V1	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
+ 12V2	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
+ 12V3	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
+ 12V4	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
- 12V	- 5% / +9%	-11.40	-12.00	-13.08	V_{rms}
+ 5VSB	- 5% / +5%	+4.75	+5.00	+5.25	V_{rms}

2.9.4.1 Dynamic Loading

The output voltages will remain within limits specified for the step loading and capacitive loading specified in the following table. The load transient repetition rate is tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 15. Transient Load Requirements

Output	Δ Step Load Size (See note 2)	Load Slew Rate	Test Capacitive Load
+3.3V	5.0A	0.25 A/μsec	250 μF
+5V	4.0A	0.25 A/μsec	400 μF
12V1+12V2+12V3+12V4	20.0A	0.25 A/μsec	2200 μF [1,3]
+5VSB	0.5A	0.25 A/μsec	20 μF
-12V	Not Rated	Not Rated	Not Rated

Notes:
1. Step loads on each 12V output may happen simultaneously.
2. For Load Range 2 (light system loading), the tested step load size should be 60% of those listed.
3. The +12V should be tested with 1000μF evenly split between the three +12V rails.

2.9.4.2 Capacitive Loading

The power supply is stable and meets all requirements with the following capacitive loading ranges.

Table 16. Capacitve Loading Conditions

Output	MIN	MAX	Units
+3.3V	250	6,800	μF
+5V	400	4,700	μF
+12V(1, 2, 3, 4)	2000 (500 each)	11,000	μF
-12V	1	350	μF
+5VSB	20	350	μF

2.9.5 Closed Loop Stability

The power supply is unconditionally stable under all line/load/transient load conditions, including capacitive load ranges. A minimum of 45 degrees phase margin and -10dB-gain margin is required. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

2.9.6 Common Mode Noise

The Common Mode Noise on any output does not exceed 350mV pk-pk over the frequency band of 10Hz to 30MHz.

The Common Mode Noise measurement is made across a 100Ω resistor between each of the DC outputs, including ground, at the DC power connector and chassis ground (power subsystem enclosure).

The test set-up uses a FET probe, such as a Tektronix* model P6046 or equivalent.

2.9.7 Ripple / Noise

The maximum allowed ripple/noise output of the power supply is defined in the following table. This is measured over a bandwidth of 0Hz to 20MHz at the power supply and power distribution board output connectors. A 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor are placed at the point of measurement.

Table 17. Ripple and Noise

+3.3V	+5V	+12V(1,2,3,4)	-12V	+5VSB
50mVp-p	50mVp-p	120mVp-p	120mVp-p	50mVp-p

2.9.8 Power Supply Soft Starting

The power supply shall contain a control circuit, which provides monotonic soft start for its outputs (+12V and 5VSB) without overstress of the AC line or any power supply components at any specified AC line or load conditions. There is no requirement for rise time on the 5Vstby but the turn on/off shall be monotonic.

2.9.9 Zero Load Stability Requirements

When the power subsystem operates in a no load condition in a 1+0 or 1+1 power supply module configuration, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

2.9.10 Power Supply Module Hot Swap Requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power subsystem. During this process the subsystem output voltages remain within the limits with the capacitive load range specified. A power supply module hot swap can be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply can be hot swapped by the following method:

Extraction: The power supply may be removed from the system while operating with PSON# asserted, while in standby mode with PSON# de-asserted, or with no AC applied. No connector damage will occur due to the un-mating of the power supply from the power distribution board.

Insertion: The power supply may be inserted into the system with PSON# asserted, with PSON# de-asserted, or with no AC power present for that supply. No connector damage will occur during mating of the output and input connector power.

A hot swap operation will work with operational as well as failed power supplies. The newly inserted power supply module will get turned on into standby or Power On mode once inserted depending on the state of the power subsystem.

2.9.11 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70ms, except for 5VSB - it is allowed to rise from 1.0 to 25ms. The +3.3V, +5V and +12V output voltages should start to rise approximately at the same time. All outputs must rise monotonically. The +5V output needs to be greater than the +3.3V output during any point of the voltage rise. The +5V output must never be greater than the +3.3V output by more than 2.25V. Each output voltage shall reach regulation within 50ms (T_{vout_on}) of each other during turn on of the power supply. Each output voltage shall fall out of regulation within 400msec (T_{vout_off}) of each other during turn off. The following diagrams show timing requirements for the power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied.

Table 18. Output Voltage Timing

Item	Description	MIN	MAX	UNITS
T_{vout_rise}	Output voltage rise time from each main output.	5.0	70 [1]	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	msec
T_{vout_off}	All main outputs must leave regulation within this time.		400	msec

[1] The 5VSB output voltage rise time shall be from 1.0ms to 25.0ms

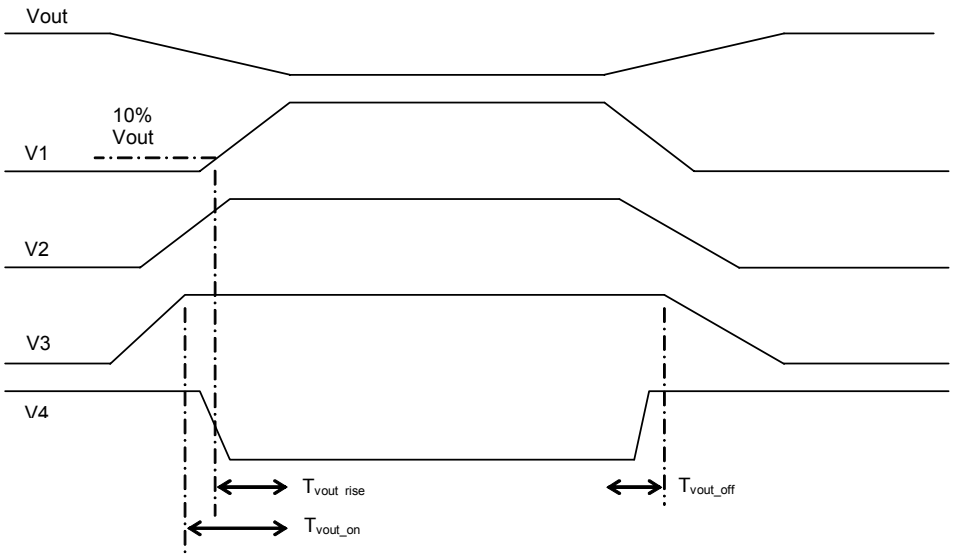


Figure 13. Output Voltage Timing

Table 19. Turn On/Off Timing

Item	Description	MIN	MAX	UNITS
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.		1500	msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	msec
T_{vout_holdup}	Time all output voltages stay within regulation after loss of AC.	21		msec
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK	20		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T_{pson_pwok}	Delay from PSON# deactive to PWOK being de-asserted.		50	msec
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec
T_{pwok_off}	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1		msec
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		msec
T_{sb_vout}	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	msec
T_{5VSB_holdup}	Time the 5VSB output voltage stays within regulation after loss of AC.	70		msec

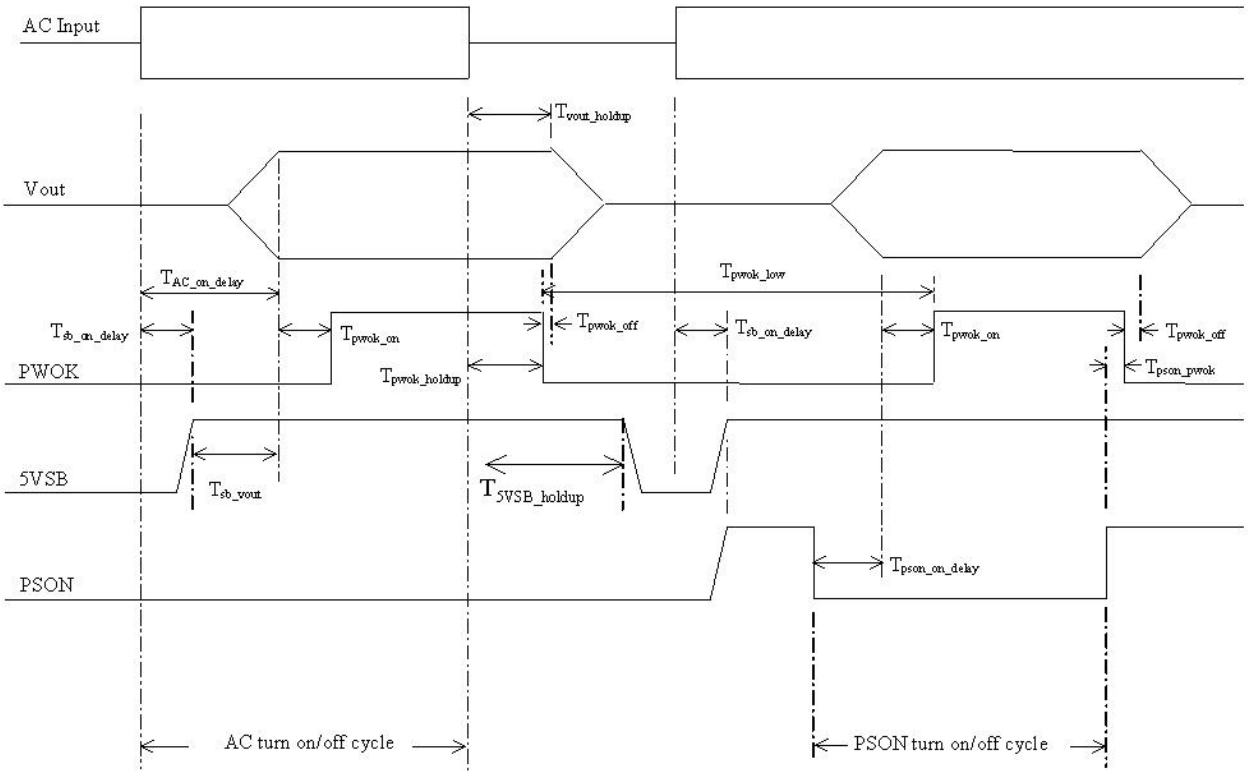


Figure 14. Turn On/Off Timing (Power Supply Signals)

2.9.12 Residual Voltage Immunity in Standby Mode

The power supply is immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500mV. There will be no additional heat generated, nor stress of any internal components with this voltage applied to any individual output, and all outputs simultaneously. It also will not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied and the PSON# signal is de-asserted.

2.9.13 Forced Load Sharing

The main +12V output from power supply modules have forced load sharing. The output shares are within 10% at full load, and 20% at half load. All current sharing functions are implemented internal to the power supply module by making use of the 12LS signal. The power distribution board connects the 12LS signal between the two power supply modules. The failure of a power supply will not affect the load sharing or output voltages of the other supplies still operating. The power supply modules are able to load share with up to 2 power supplies in parallel and operate in a hot-swap / redundant 1+1 configuration. The 5Vsb output is not required to actively share current between power supplies (passive sharing). The 5Vsb output of the power supplies are connected together in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system.

2.10 Protection Circuits

Protection circuits inside the power supply module and power distribution board will cause either the power supply's main +12V output to shutdown, which in turn shuts down the other 3 outputs on the power distribution board or first shuts down any of the 3 outputs on the power distribution board, which in turn also shuts down the power supply module main +12V output. If the power supply module latches off due to a protection circuit tripping, an AC cycle OFF for 15sec min and a PSON# cycle HIGH for 1sec will reset the power supply module and the power distribution board.

2.10.1 Current Limit (OCP) / 240VA Protection

The power supply modules have a current limit circuit to prevent the main +12V output from exceeding the values shown in the following table. If the current limits are exceeded, the power supply will shutdown and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply will not be damaged from repeated power cycling in this condition. The 5VSB output is protected from damage under an over current or shorted condition. The auto-recovery feature is implemented on the 5VSB outputs.

Each DC/DC converter output on the power distribution board has individual OCP protection circuits. The entire power subsystem shall shutdown and latch off after any DC/DC over current condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The following table contains the over current limits. The values are measured at the power distribution board harness connectors. The DC/DC converters shall not be damaged from repeated power cycling in this condition. Also, the +12V output from the power supply module is divided on the power distribution board into 5 channels and each is limited to 240VA of power except +12V5 (+12V5 is not user accessible).

Table 20. Over Current Protection (OCP)

Output Voltage	Min OCP Trip Limits	Max OCP Trip Limits
+3.3V	110% min (= 17.6A min)	187% max (= 30A max)
+5V	110% min (= 17.6A min)	200% max (= 32A max)
-12V	125% min (= 0.625A min)	400% max (= 2.0A max)
+12V1	18A	20A max
+12V2	18A	20A max
+12V3	18A	20A max
+12V4	16A	20A max
+12V5	16A	20A max
+12V	51A	59.5A max
+5VSB	4.5A	6A

2.10.2 Over Voltage Protection (OVP)

The power supply module over voltage protection for +12V and +5VSB are sensed inside the module. The power supply module is shutdown and latched off after an over voltage condition occurs. This latch is cleared by toggling the PSON# signal or by an AC power interruption. The following table contains the over voltage limits. The values are measured at the output of the power supply's connectors. The voltage will never exceed the maximum levels when measured

at the power pins of the power supply connector during any single point of fail. The voltage will never trip any lower than the minimum levels when measured at the power pins of the power supply connector. Exception: +5VSB rail should be able to auto-recover after it's over voltage condition occurs.

Each DC/DC converter output on the power distribution board has individual OVP protection circuits built in and they are sensed on the power distribution board. The entire power subsystem will shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The following table contains the over voltage limits. The values are measured at the harness connectors. The voltage will never exceed the maximum levels when measured at the power pins of the output harness connector during any single point of fail. The voltage will never trip any lower than the minimum levels when measured at the power pins of the power distribution board connector.

Table 21. Over Voltage Protection (OVP) Limits

Output Voltage	MIN (V)	MAX (V)
+3.3V	3.9	4.5
+5V	5.7	6.2
+12V1,2, 3,4,5	13.3	14.5
+12V	13.3	14.5
-12V	-13.3	-14.5
+5VSB	5.7	6.5

2.10.3 Over Temperature Protection (OTP)

The power supply module is protected against over temperature conditions caused by loss of fan cooling, excessive ambient temperature, or excessive loading. Two sensing points are placed at hot spots; one near the exterior face and the other near the interior face of the module. In an OTP condition the Power Supply Unit will shutdown. When the power supply temperature drops to within specified limits, the power supply will restore power automatically, while the 5VSB remains always on. The OTP circuit has built-in hysteresis such that the power supply will not oscillate on and off due to temperature recovering conditions. The OTP trip level has a minimum of 4°C of ambient temperature hysteresis.

2.11 SMBus Monitoring Interface

The power supply module + PDB combo provides a monitoring interface to the system over a server management bus based on the PSMI specification. This shall provide power monitoring, failure conditions, warning conditions, and FRU data. Two pins have been reserved on the connector to provide this information. One pin is the Serial Clock (PSM Clock). The second pin is used for Serial Data (PSM Data). Both pins are bi-directional and are used to form a serial bus. The circuits inside the power supply shall be powered from the 5VSB bus and grounded to ReturnS (remote sense return). No pull-up resistors shall be on SCL or SDA inside the power supply. These pull-up resistors should be located external to the power supply. The EEPROM for FRU data in the power supply shall be hard wired to allow writing data to the device.

There are two usage models depending on the system. The system shall control the usage model by setting the Usage Mode bit.

- Default Mode: In this mode, because there is no software, BIOS, or other agent that will access the power supply via SMBus to do any clearing, the LEDs and registers must automatically clear when a warning event has occurred.

- Intelligent Mode: A system management controller or BIOS agent exists that can read and clear status. In this mode, the LEDs and registers should latch when a warning event occurs so that the system and user can read their status before it changes during transient events.

Over current protection (OCP) trip limits, as defined in Table 20, will cause the power supply to shutdown and latch the LED and SMB_Alert signal no matter what mode the power supply is in, “default” or “intelligent”.

Warning events latch the LED and SMB_Alert signal when in “intelligent” mode. If in the “default” mode, the LED and SMB_Alert signal will de-assert as soon as the condition driving the event clears.

If the power supply fails due to over temperature shutdown, over current shutdown, over power shutdown or fan failure, the LED, SMB_Alert signal, and critical event registers shall still operate correctly. If the supply fails due to loss of AC or open fuse, then the LED and signals will have no power and, therefore, will not operate.

2.11.1 SMBus Device Addresses

The Power Supply and Power Distribution Board device address locations are shown below. There are two signals to set the address location of the Power Supply once it is installed into the system: A0 ad A1.

Table 22. SMBus Device Addresses

Power Supply location	Front	Rear
Power Supply FRU Device	A0h	A2h
Power Supply PSMI Device	B0h	B2h
Power Distribution Board FRU Device	ACh	-
Power Distribution Board PSMI Device	4Ah	-

2.11.2 Hot Plug I2C Requirements

Since the redundant power supplies will be asynchronously installed and powered-on in a system, the SMBus devices on the supply is tolerant of joining the SMBus in the middle of a SMBus transaction and ignore bus activity after being powered on until a valid start of transaction is seen.

2.11.3 Power Supply Failure Communication

Failure signals do not exist between the power supply and the Power Distribution Board. The SMBus Alert signal is asserted when a critical or warning condition occurs with the power supply module. The system polls the power supply via the SMBus to see what type of warning or failure condition has occurred.

2.11.4 Power Supply Present Communication

Power supply presence is determined by the system actively polling the power supplies via the SMBus.

2.11.5 Input Current and Output Current & Output Power Monitoring

The power supply has registers in the monitoring device containing input AC current, +12V output current and +12V output power. There are registers for the present level and stored max level for AC input current and +12V output current and +12V output power. Present (power / current) values are averaged over a 2-10sec time interval and represent the continuous current and power (measurement averaged over 2-10sec interval). Max current / power levels are the maximum level measured (and latched) for the present power in between reset events (no less then 10s interval). Max and present values for +12V output currents, +12V output power, and AC input current are stored in their respective registers.

2.11.6 Output Current / Power "Fuel" Gauge Operation

The +12V output power and +12V output current monitoring feature is for the purpose of a system "fuel" gauge. It measures only the main output. This feature allows a user to tell if system loading is exceeded, or coming close to exceeding the power supply rating on these rails. The SMBAlert signal will assert if the +12V output current or total +12V output power exceeds the associated limit register values. The limit register values are set equal to the maximum power supply ratings. The total output power is calculated by multiplying the measured +12V current by the nominal +12V output voltage. This total output power will not include the lower power rails like 5Vstandby. The measurement accuracy requirements are shown below.

The +12V output current values are stored in two register locations for each measurement point. One register is the Present Current value, which is the present (2-10s averaged) amount of output current on that rail. The other is the Max Current value; which is the maximum value measured in the Present Current register (since last reset). The Max Current value is saved until a reset event occurs.

The +12V output power is stored in two register locations. One register is the Present Power value, which is the present amount of output power (2-10s averaged). The other is the Max Power value, which is the maximum value from the Present Power register (since last reset). The Max Power value is stored until a reset event occurs.

2.11.7 Input Current Meter Operation

The input current monitoring is for the purpose of providing the total system AC input rms current consumption. This allows the user to determine approximate current consumption of their system.

The input current is stored in two register locations. One register is the Present Input Current value, which is the present amount of input current (2-10s averaged). The other is the Max Input Current value, which is the maximum value from the Present Input Current register (since last reset). The Max Input Current value is stored until a reset event occurs.

2.11.8 Max Power/Max Current Reset

The power and current registers are reset to 00h when the power supply is powered OFF via AC or PSON.
Performing a write to the Max Current or Max Power registers will reset the register to the value in the associated present current or present power register. In the case of a momentary loss of AC input power, the register values will be saved as long as the 5VStandby output is present. Once the AC is lost long enough to allow the 5VStandby output to drop out of regulation, the register values will reset to 00h.

2.11.9 Monitor Accuracy

Table 23. PSMI Monitor Accuracy Requirement

Load Range	O/P Current	O/P Power	AC I/P RMS Current
90% to 110%	+/-3 to 5%	+/-5 to 8%	+/-5 to 10%
50% to 90%	+/-4 to 6%	+/-6 to 9%	+/-5 to 10%
15% to 50%	+/-5 to 10%	+/- 6 to 13%	+/-5 to 10%
Min to 15%	TBD	TBD	TBD

Notes:
1. The voltage tolerance on +12V at the output of the power supply module connector is assumed to be +/-3% accurate at static loading conditions.
2. It is assumed the power supply will be able to operate at 110% of rated power and current without shutting down for extended periods of time. The power supply will not be required to meet reliability requirements at >100% loading.

2.11.10 Current Measurement Sampling

Minimum Sampling rate = 1Hz minimum
Window averaging size = 10sec.
The values in the present and maximum value registers are a moving average over the 10 sec window. An anti-aliasing filter is required to prevent aliasing at 1Hz sampling rate.

2.11.11 Register Units

The value and limit register represent Watts, Amps, or other units of measure. The data in the PSMI FRU data configuration shall set the units (the LSB) in each of the registers represented. The value and associated limit register(s) shall have the same units of measure. It is desired that the units represent the maximum value the system will need over its life.

2.11.12 Event Registers

There are two event registers that correspond to critical and warning events in the power supply. A critical event is one in which the power supply shuts down. A warning event is when the power supply is approaching a critical event but the power supply has not yet shut down. Bits in each register track these events.

Critical events include: general failure, over current / power, over temperature, and AC not present.
Warning events include: high current / power, high temperature, and failing fan.

The Event Register should power-on default to 00h. Otherwise, its state should be preserved as long as standby is available to the device.

2.11.13 Clearing Events

In the “default” mode, event registers are automatically cleared when the cause of the event disappears or by writing a 1b to the associated set bit. In the “intelligent” mode, the event bits are cleared by writing a ‘1b’ to the associated set bit. For example, if an event register contains the value 0000 1001b, indicating two asserted events, writing the value 0000 0001b to that register would clear the least significant bit in the register to be cleared, resulting in the register containing the value 0000 1000b. De-asserting PSON will not cause the event bits to lose information (i.e. to clear). Asserting PSON will reset the event bits to 0b. In the case of a momentary loss of AC input power, the bit status will be saved as long as the 5VStandby output is present. Once the AC is lost long enough to allow the 5VStandby output to drop out of regulation, the event bits shall reset to 0b.

2.11.14 Critical Events

Critical events are all controlled and set by the power supply and Power Distribution Board. The system cannot set the level of these events via SMBus. The PSMI device monitors the status of these events.

2.11.15 Temperature Warning Event

The high temperature event register warns the system that the power supply is operating higher than the maximum temperature and the power supply may shutdown due to this high temperature. The trip level for the warning condition is controlled by the power supply and the system cannot affect this level. There will always be a warning condition applied to the event register a significant time before a shutdown condition occurs. Significant time is defined as enough time to allow service personnel to replace the power supply or the system to take action. There is hysterisis in the trip level so that the event does not oscillate between assert and de-assert.

2.11.16 Limit Registers for Power/Current Warning Events

Limit registers are provided to control the threshold for warning events caused by current and power measurements only. Limit registers are not needed for critical events and some warning events such as: fan events or temperature events.

2.11.16.1 Output Current Limit Registers

The output current limit register are compared to the Present Current register for the associated output to determine the status of the output current warning event bit. If the Present Current register exceeds the limit register, the associated bit will be set to 1b. If the PSMI device is operating in “default” mode this bit shall reset to 0b as soon as the Present Current value drops below the limit register value. If the PSMI device is operating in “intelligent” mode, this bit shall latch at 1b. The event is cleared as described in the previous section.

2.11.16.2 Output Power Limit Registers

The output power limit register is compared to the Present Power register to determine the status of the output power warning event bit. If the present power register exceeds the limit register, the associated bit will be set to 1b. If the PSMI device is operating in “default” mode this bit shall reset to 0b as soon as the Present Power value drops below the limit register value. If the PSMI device is operating in “intelligent” mode, this bit will latch at 1b. The event is cleared as described in the previous section.

2.11.16.3 Input Current Limit Registers

The input current limit register will be compared to the Present input current register to determine the status of the input current warning event bit. If the present input current register exceeds the limit register, the associated bit will be set to 1b. If the PSMI device is operating in “default” mode this bit shall reset to 0b as soon as the Present Input Current value drops below the limit register value. If the PSMI device is operating in “intelligent” mode, this bit will latch at 1b. The event is cleared as described in the previous section.

2.11.16.4 PDB Failure

The Power Distribution Board PSMI device has a bit to indicate the PDB has failed. This bit will assert if there is a hard failure or if the PDB is shutdown due to over loading.

2.11.16.5 PDB Over-Current Shutdown

The Power Distribution Board PSMI has 4 bits to indicate one of the four 12V outputs has shutdown due to an over current limit condition.

2.11.17 SMBAlert / LED Mask Register

The SMBAlert/LED Mask register enables/disables which critical and warning event bits contribute to SMBAlert and the LED operation. The bits 1:1 with the bits in the event register. A 1b enables a given condition to contribute to the SMBAlert signal and LED function.
The SMBAlert/LED Mask registers default to 00h on power-on. When the power supply is installed in the system and power is first applied to the PSMI device the system sets the mask registers according to system capabilities. Once power is applied to the PSMI device it retains its mask register information as long as standby power is available.

2.11.18 Power Control via SMBus

The SMBus can control the power supply in the following ways. At startup these bits shall be set to 0b.

2.11.18.1 Operating Mode

This bit controls the operating mode of the PSMI device in the power supply. A 0b puts the device into Default mode. A 1b puts the device into intelligent mode. A description of these modes is in a previous section.

2.11.18.2 Fan Control

There is a bit to force the power supply fan to high speed. Writing a 1b to this bit causes the power supply fan to go to high speed. Writing a 0b causes the fan speed to be controlled by the power supply.

2.11.19 SMBAlert Signal

This signal indicates that the power supply or Power Distribution Board is experiencing a problem that the user should investigate. This will be asserted due to Critical events or Warning events.

The SMBAlert pin is driven from the combination of the Event Register and the SMBAlert/LED Mask register. The SMBAlert signal is asserted whenever there is at least one condition that is set in the event registering that is also enabled in the SMBAlert/LED Mask register. If in "intelligent" mode, software will need to clear all enabled bits in the event register to cause SMBAlert to be de-asserted. In "default" mode SMBAlert and the event register will automatically be cleared when the cause of the event is no longer present.
There is also a SMBAlert bit in the event registers.

2.11.20 Power Supply Module LED Control

There is a single bi-color LED to indicate power supply status. The LED operation is defined below.

Table 24. LED Indicators

Power Supply Condition	LED
No AC power to power supply	OFF
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink AMBER
AC present / Only 5VSB on (PS off)	1Hz Blink GREEN
Output ON and OK	GREEN

There shall be bits that allow the LED state to be forced via SMBus. The following capabilities are required:

- Force Amber ON for failure conditions
- Force Amber 1Hz Blink for warning conditions
- No Force (LED state follows power supply present state)

The power-on default should be 'No Force'. The default is restored whenever PSON transitions to assert.

2.11.21 Power Distribution Board (PDB) LED Control

There are three amber LEDs on the power distribution board: PS fan module#1 LED, PS fan module#2 LED, power distribution board LED. Fan module LEDs will blink at 1Hz to indicate a slow fan condition (predicative failure) and will light up solid amber for a fan failure condition. The power distribution board LED will light up solid amber to indicate a power distribution board failure.

2.12 Power Supply Module and PDB FRU Data

The FRU data format is compliant with the IPMI ver.1.0 (per rev.1.1 from September 25, 1999) specification. The current version of these specifications is available at http:\\developer.intel.com/design/servers/ipmi/spec.htm.

3. Cooling Sub-System

The cooling sub-system is comprised of four 40x40x56mm dual rotor fans, one 40x40x28mm single rotor fan, two 40x40x56mm power supply fans, a CPU air duct, and a Power Supply air duct. These components are used to provide the necessary cooling and airflow to the system. A fan on the processor heat sink is not necessary in this chassis.

In order to maintain the necessary airflow within the system, the CPU air duct, Power Supply air duct, and top cover need to be properly installed.

Note: The Server Chassis SR1450 does support redundant cooling for low voltage processors. Power supply cooling is redundant with the 1+1 power supply configuration only. The 28mm single rotor fan is not redundant, however. Should a fan fail, the system should be brought down as soon as possible to replace the failed fan.

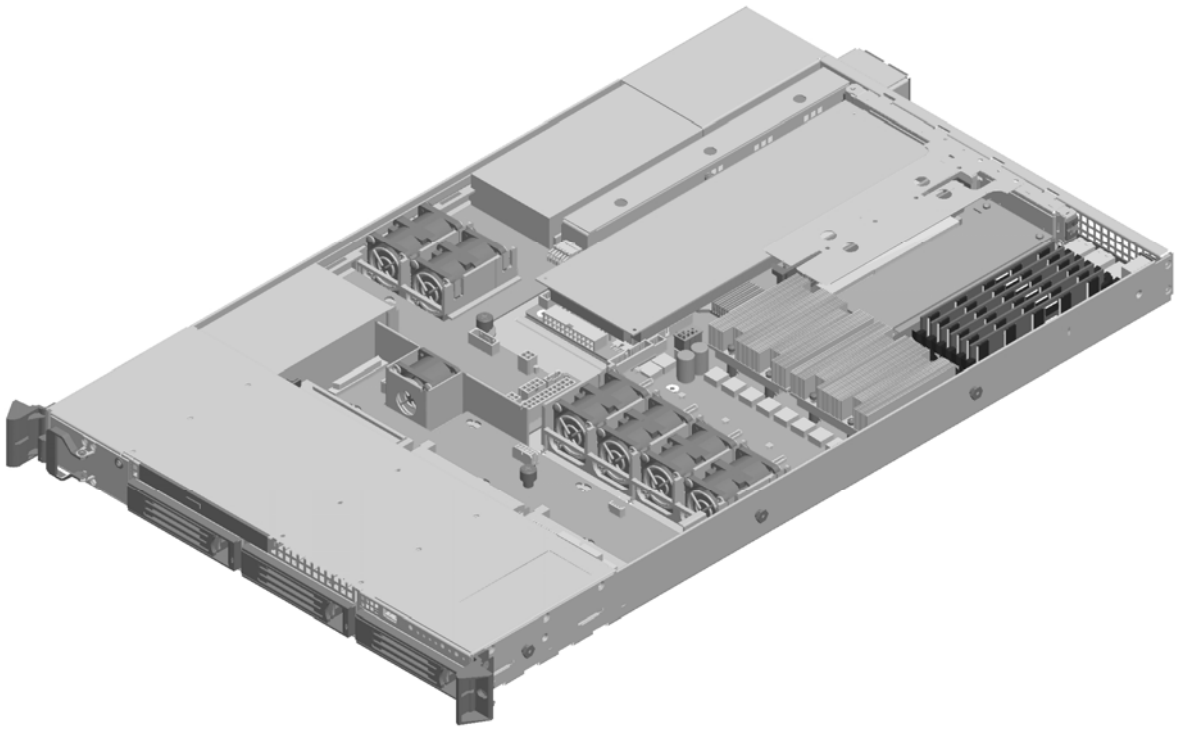


Figure 15. Cooling Sub-System Components

3.1 Four-Fan Module

A fan module consisting of four 40x40x56mm dual rotor multi-speed fans, provides the primary cooling for the processors, memory, the second and third hard drive bays, and components in the low profile PCI zone.

Removal and insertion of the fan module is tool-less and provides for ease of installation and serviceability. The fan module supports a fan distribution board that facilitates individual fan

replacement. Neither the fan module nor the individual fans within it are hot swappable. The server must be turned off before any of the fans can be replaced.

Each dual rotor fan has an 8-pin wire harness, which connects to the fan distribution board. Each fan harness provides power and tachometer lines allowing the fans to be monitored independently by server management software. The fan distribution board has a 20-pin connector which provides the power and communication signal path to the server board.

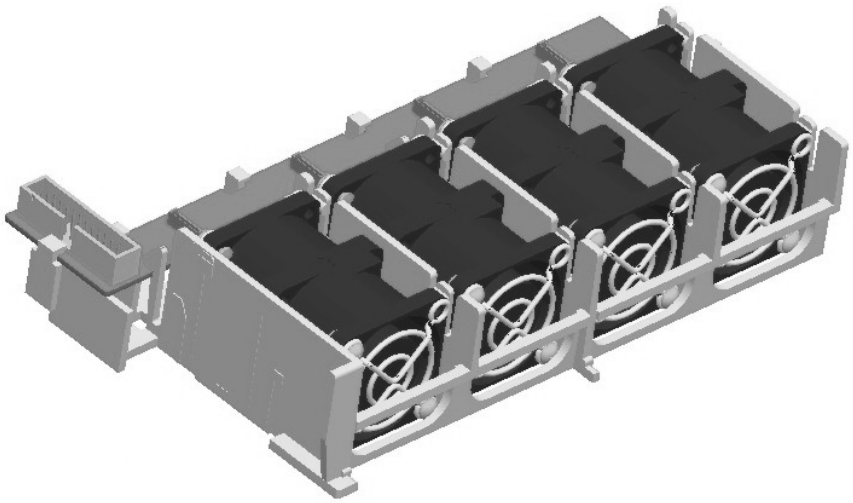


Figure 16. Fan Module Assembly

The following table provides the pin-out for each fan harness.

Table 25. Individual Fan Assy Pin-out (J1, J2, J3, J4)

Pin	Signal Name	Description
1	FAN_SPEED_CNTL2	Controls the fan speed
2	FAN_FAIL	FAN_TACH signal
3	GND	Power Supply Ground
4	Reserved	Reserved
5	GND	Power Supply Ground
6	GND	Power Supply Ground
7	FAN_FAIL	FAN_TACH signal
8	Fan speed control	Variable Speed Fan Power

The following table provides the pin-out of the 20-pin fan control connector on the fan distribution board.

Table 26. Fan Distribution Connector Pin-out (J5)

Signal Name	Pin	Pin	Signal Name
FAN_SPEED_CNTL2	1	11	FAN_SPEED_CNTL2
FAN_SPEED_CNTL2	2	12	Reserved
GND	3	13	GND

Signal Name	Pin	Pin	Signal Name
GND	4	14	GND
FAN_FAIL5	5	15	FAN_FAIL1
FAN_FAIL6	6	16	FAN_FAIL2
FAN_FAIL7	7	17	FAN_FAIL3
FAN_FAIL8	8	18	FAN_FAIL4
Reserved	9	19	Reserved
Reserved	10	20	Reserved

Each fan within the module is capable of supporting multiple speeds. If the internal ambient temperature of the system exceeds the value programmed into the thermal sensor data record (SDR), the Baseboard Management Controller (BMC) firmware will increase the rotational speed for all the fans within the fan module.

Note: There is fan redundancy for the four-fan module when running Low Voltage processors. However, should a fan fail, the system should be shut down as soon as possible to have the fan replaced. The system fans are not hot-swapable.

3.2 PCI Fan

One 40x40x28mm single rotor multi-speed fan provides the primary cooling for the components in the full-height PCI zone, power distribution board, DC/DC converters, and the first hard drive bay. The single rotor fan has a standard 3-pin SSI cable harness that connects directly to a fan header on the server board. This 28mm fan is not redundant.

Removal and insertion of the single rotor fan is tool-less and provides for ease of installation and serviceability. The fan is not hot swappable. The server must be turned off before the fan can be replaced.

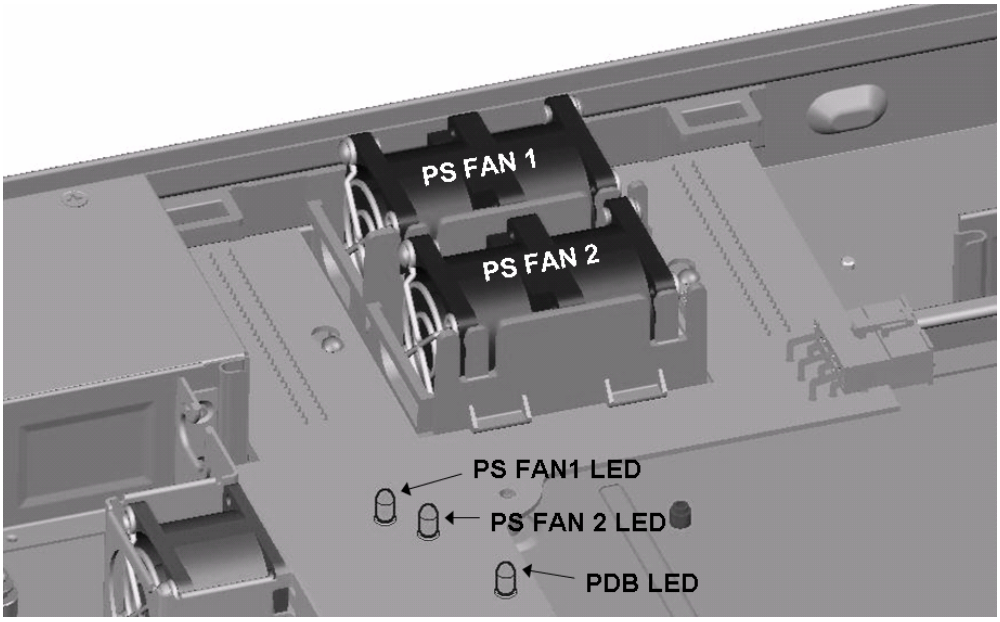
The single rotor fan is capable of supporting multiple speeds. If the internal ambient temperature of the system exceeds the value programmed into the thermal sensor data record (SDR), the Baseboard Management Controller (BMC) firmware will increase the rotational speed for all other system fans.

3.3 Power Supply Fans

The power supply modules support two 40x40x56mm dual rotor multi-speed fans. These fans are redundant in the 1+1 power supply configuration only. They are responsible for the cooling of the power supply modules. The power distribution board monitors and controls these fans independent of conditions in other airflow sections as the power supply airflow section is completely isolated from the rest of the system. The fan speed is based on main +12V power load share signal, which indicates how much +12V power is being consumed. These fans also operate at 5V during standby mode to cool the power supply modules even during standby mode. There are two amber Power Supply fan LEDs on the Power Distribution Board. They blink for predictive failure and light up solid for a stopped fan failure condition. A predictive fail or stopped fan fail will show up in the Intel Management Module System Event Log as “Power Unit 0x01h” failure event. The Intel Server Management event will show up as “Power Unit Failure Detected”. The Power Supply fans are not monitored by the system Firmware with the mBMC configuration. Therefore, no System Event Log or Intel Server Management events will be reported with the mBMC configuration. There is an amber Power Distribution Board LED on the Power Distribution Board which light solid for a hard failure on the Power Distribution Board.

This condition will show up in the Intel Management Module System Event Log as “Power Unit 0x01h” failure event. The Intel Server Management event will show up as “Power Unit Failure Detected”. The Power Distribution Board failure is not monitored by the system Firmware with the mBMC configuration. Therefore, no System Event Log or Intel Server Management events will be reported with the mBMC configuration.

Figure 17. Power Supply Fan Numbering



3.4 CPU Air Duct and Power Supply Air Duct

The chassis requires the use of a CPU air duct and power supply air duct to direct airflow and sustain appropriate air pressure.

A Power Supply air duct is used to isolate airflow of the two power supply fans from the rest of the system. The Power Supply air duct is mounted on top of the power distribution board and is secured with a captive screw.

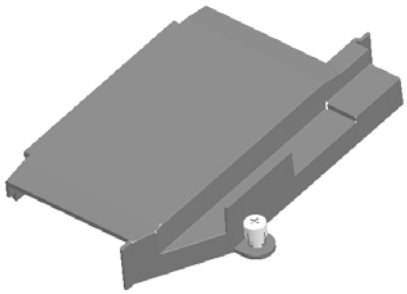


Figure 18. Air Baffle

The CPU air duct must be properly installed to direct airflow through the processor heatsink(s) to the low profile PCI and memory area of the system. The CPU air duct is designed to support either a single or dual processor configuration. For single processor configurations the pre-installed air dam must be left in place in order to maintain necessary air pressure and airflow through the processor heat sink. For dual processor configurations, the air dam must be snapped off of the CPU air duct. The CPU air duct cannot be installed if the air dam is in place and two processors are installed.

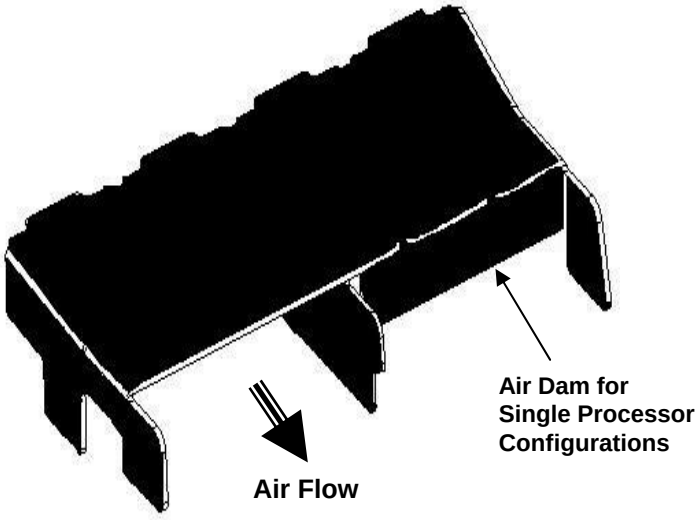


Figure 19. CPU Air Duct

Note: For single processor configurations, if the air dam is removed, the system may not meet the thermal cooling requirements of the processor, which will most likely result in a thermal shutdown of the system.

Note: Once the air dam is removed from the CPU air duct, it cannot be reinstalled.

The CPU air duct has the fan numbering printed on it to correlate system fan location to fan numbering displayed in the Intel Server Management software and the System Event Log. The numbering on the CPU air duct are those displayed in the Intel Server Management software. The conversion table below is used to correlate the system fan location to the System Event Log. System Event Log numbering is different between mBMC and Intel Management Module configurations.

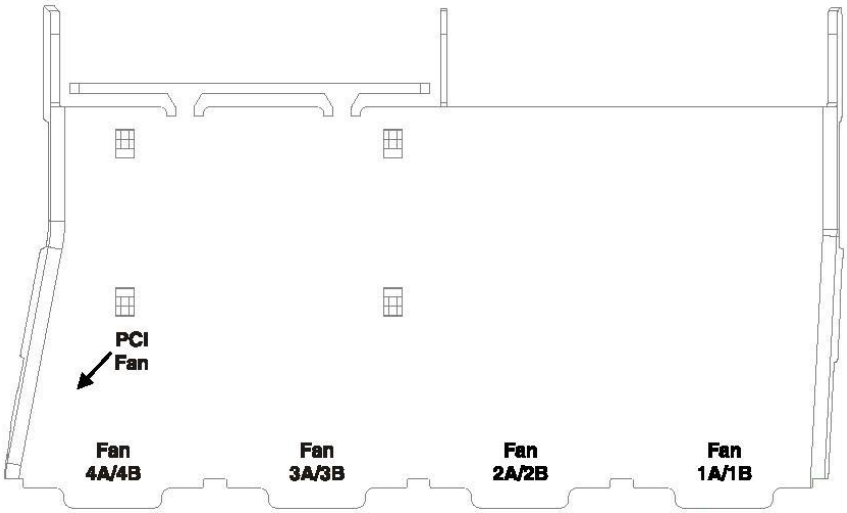


Figure 20. CPU Air Duct Fan Numbering

Table 27. Fan Numbering Conversion Table

Air Duct Number	ISM Value	mBMC SEL Value	IMM SEL Value
1A	1A	1B	40
1B	1B	1C	41
2A	2A	1F	44
2B	2B	20	45
3A	3A	21	46
3B	3B	22	47
4A	4A	D1	42
4B	4B	1E	43
PCI FAN	PCI FAN	23	48

3.5 Hard Drive Bays

Hard drive bays must be populated in order to maintain system thermals. The hot swap hard drive trays must either have a hard drive or a drive blank installed in them. **The hard drive tray is mechanically keyed, older hard drive tray versions will not fit in the Server Chassis SR1450.**

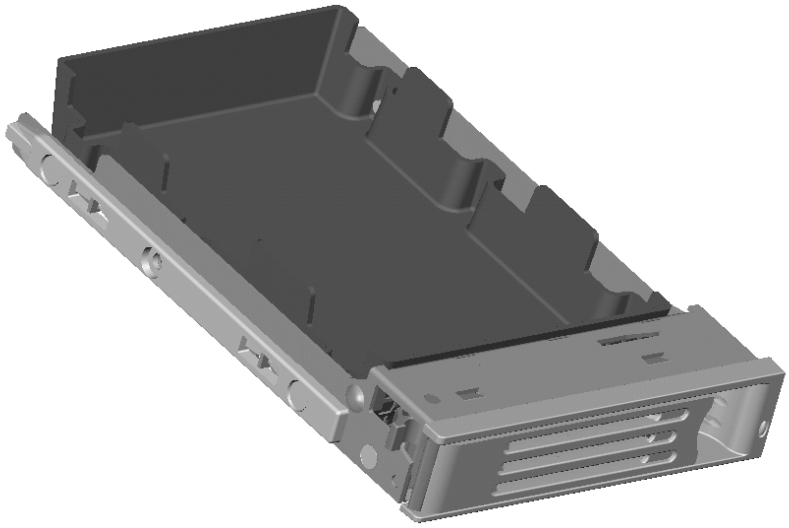


Figure 21. Hot Swap Hard Tray

4. Peripheral and Hard Drive Support

The Server Chassis SR1450 provides three hard drive bays and one slim-line peripheral drive bay at the front of the chassis. The hard drive bays are designed to support both SCSI and SATA/SAS hot-swap backplanes.

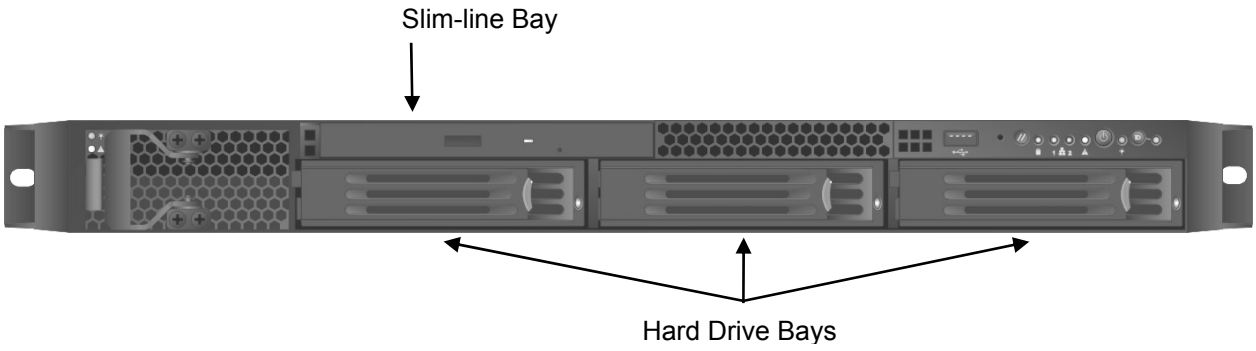


Figure 22. Intel® Server Chassis SR1450 Peripheral Bay Configuration Options

4.1 Slim-line Drive Bay

The chassis provides a slim-line drive bay that can be configured for either CD-ROM, DVD/CDR, or floppy drives. Drives are mounted on a tool-less tray, which allows for easy installation into and removal from the chassis. The slim-line devices are not hot swappable.

4.1.1 Floppy Drive Support

A slim-line floppy drive can be supported in multiple system configurations.

4.1.1.1 Floppy in Slim-line Drive Bay

An interposer card is attached to the back of the floppy drive which provides the power and IO interconnects between the drive, power supply and server board. The interposer card has three connectors; on one side of the interposer is a 28-pin connector, which connects to the back of the drive via a short 28-pin flat ribbon cable. The pin-out for this connector is defined in Table 28. On the opposite side of the interposer is a 4-pin connector that is cabled to the 2x5 pin power lead from the power distribution board connector. The pin-out for this connector is defined in Table 29.

Table 28. 28-Pin Floppy Device Connector Pin-out (J4)

Pin	Name	Pin	Name
1	P5V	15	GND
2	FD_INDEX_L	16	FD_WDATA_L
3	P5V	17	GND
4	FD_DS0_L	18	FD_WGATE_L
5	P5V	19	GND
6	FD_DSKCHG_L	20	FD_TRK0_L
7	Unused	21	GND

Pin	Name	Pin	Name
8	Unused	22	FD_WP_L
9	2M_MEDIA	23	GND
10	FD_MTR0_L	24	FD_RDATA_L
11	Unused	25	GND
12	FD_DIR_L	26	FD_HDSEL_L
13	FD_DENSEL0	27	GND
14	FD_STEP_L	28	GND

Table 29. 4-Pin Floppy Power Connector Pin-out (J3)

Pin	Name
1	P12V
2	GND
3	GND
4	P5V

The power cable is included with the power distribution board. The SCSI and SATA/SAS backplane accessory kits have a 34-pin floppy cable. This cable goes from the adapter board to the legacy floppy connector on the server board. This connector has the following pin-out.

Table 30. 34-Pin Floppy Connector Pin-out (J2)

Name	Pin	Pin	Name
GND	1	2	FD_DENSEL0
GND	3	4	2M_MEDIA
GND	5	6	FD_DRATE0_L
GND	7	8	FD_INDEX_L
GND	9	10	FD_MTR0_L
GND	11	12	FD_DS1_L
GND	13	14	FD_DS0_L
GND	15	16	FD_MTR1_L
Unused	17	18	FD_DIR_L
GND	19	20	FD_STEP_L
GND	21	22	FD_WDATA_L
GND	23	24	FD_WGATE_L
GND	25	26	FD_TRK0_L
Unused	27	28	FD_WP_L
GND_FDD	29	30	FD_RDATA_L
GND	31	32	FD_HDSEL_L
MSEN0	33	34	FD_DSKCHG_L

4.1.1.2 Optional Floppy In Hard Drive Bay

An optional conversion kit is available for system configurations that require both an optical drive and floppy drive. The kit consists of a drive tray and face plate. When assembled with a slim-line floppy drive, the assembly is inserted into the middle hard drive bay. Like the slim-line bay configuration, the power cable is part of the power distribution board cable harness and the 34-pin cable is provided with the SCSI and SATA/SAS backplane accessory kits.

Figure 23. Optional Floppy Drive Configuration In Middle HDD Bay

4.1.2 Optical Drive Support in the Slim-line Bay

A slim-line CDROM or DVD-CDR drive can be supported in the slim-line bay. An interposer card is plugged into the back of the optical drive. The interposer card provides the power and IO interconnects between the drive, power supply and server board. The interposer card has three connectors; the first has 50 pins and is plugged directly into the back of the drive. The pin-out for this 50-pin connector is defined in Table 31. The second connector has 4 pins and is cabled to the 2x5 pin power lead from the power distribution board. This connector is defined in Table 32.

Table 31. 50-pin CD-ROM connector Pin-out (J6)

Name	Pin	Pin	Name
RSV_LCM	1	2	RSV_RCM
RSV_GND	3	4	GND
RST_IDE_S_L	5	6	IDE_SDD<8>
IDE_SDD<7>	7	8	IDE_SDD<9>
IDE_SDD<6>	9	10	IDE_SDD<10>
IDE_SDD<5>	11	12	IDE_SDD<11>
IDE_SDD<4>	13	14	IDE_SDD<12>
IDE_SDD<3>	15	16	IDE_SDD<13>
IDE_SDD<2>	17	18	IDE_SDD<14>
IDE_SDD<1>	19	20	IDE_SDD<15>
IDE_SDD<0>	21	22	IDE_SDDREQ
GND	23	24	IDE_SDIOR_L
IDE_SDIOW_L	25	26	GND
IDE_SIORDY	27	28	IDE_SDDACK_L
IRQ_IDE_S	29	30	NC_IDEIO16_L
IDE_SDA<1>	31	32	NC_CBL_DET_S
IDE_SDA<0>	33	34	IDE_SDA<2>
IDE_SDCS0_L	35	36	IDE_SDCS1_L
IDE_SEC_HD_ACT_L	37	38	P5V
P5V	39	40	P5V
P5V	41	42	P5V
GND	43	44	GND
GND	45	46	GND
IDEP_ALE_H	47	48	GND
Unused	49	50	Unused

Table 32. 4-Pin CD-ROM Power Connector Pin-out (J5)

Pin	Name
1	P12V
2	GND
3	GND
4	P5V

The third connector has 40 pins and is cabled to the legacy IDE connector on the server board. This connector has the following pin-out.

Table 33. 40-Pin CD-ROM Connector Pin-out (J1)

Name	Pin	Pin	Name
RST_IDE_S_L	1	2	GND
IDE_SDD<7>	3	4	IDE_SDD<8>
IDE_SDD<6>	5	6	IDE_SDD<9>
IDE_SDD<5>	7	8	IDE_SDD<10>
IDE_SDD<4>	9	10	IDE_SDD<11>
IDE_SDD<3>	11	12	IDE_SDD<12>
IDE_SDD<2>	13	14	IDE_SDD<13>
IDE_SDD<1>	15	16	IDE_SDD<14>
IDE_SDD<0>	17	18	IDE_SDD<15>
GND	19	20	Unused
IDE_SDDREQ	21	22	GND
IDE_SDIOW_L	23	24	GND
IDE_SDIOR_L	25	26	GND
IDE_SIORDY	27	28	IDEP_ALE_H
IDE_SDDACK_L	29	30	GND
IDE_IDE_S	31	32	NC_IDEIO16_L
IDE_SDA<1>	33	34	IDE_CBL_DET_S
IDE_SDA<0>	35	36	IDE_SDA<2>
IDE_SDCS0_L	37	38	IDE_SDCS1_L
IDE_SEC_HD_ACT_L	39	40	GND

The interposer card and associated cables are included as part of the SCSI and SATA/SAS backplane accessory kits.

4.2 Hard Disk Drive Bays

The Server Chassis SR1450 can be configured to support either hot swap SCSI or SATA/SAS hard disk drives. The 3.5-inch x 1-inch hard disk drives are mounted to hot swap drive trays for easy insertion into and extraction from the drive bay.

Note: All hard drive bays must be populated to maintain system thermals. Drive trays should either have a hard drive or drive blank inserted.

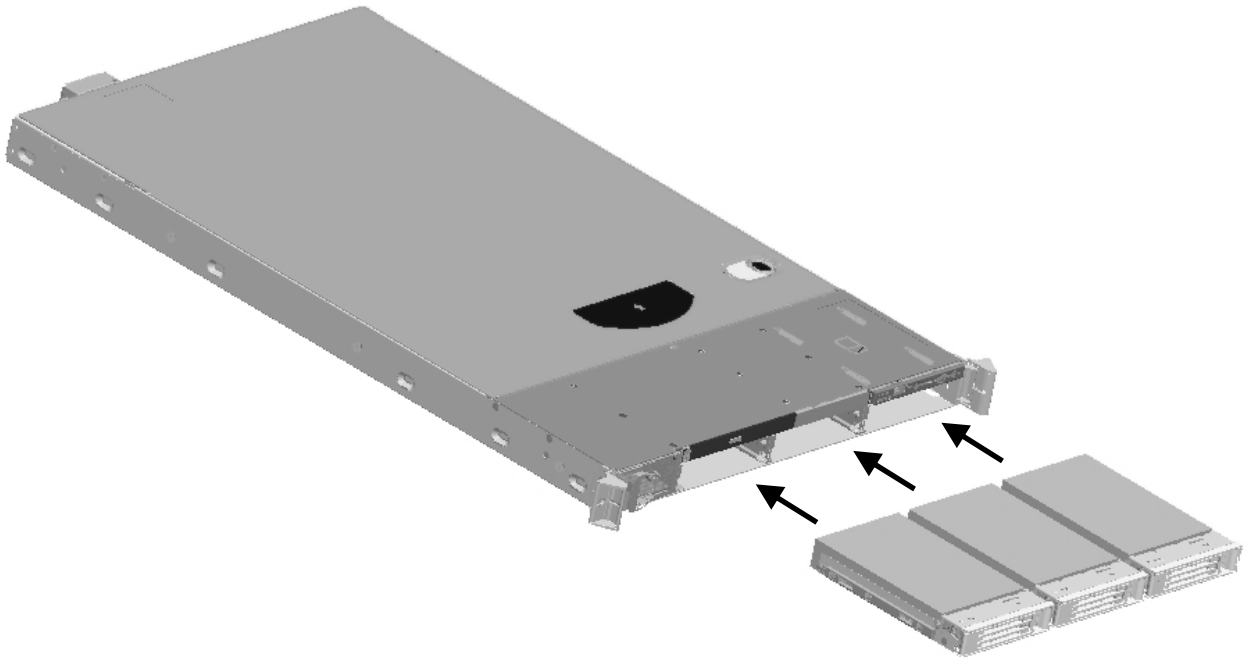


Figure 24. Hard Drive Bays

4.2.1 Hot Swap Hard Disk Drive Trays

Each hard drive must be mounted to a hot swap drive tray, making insertion and extraction of the drive from the chassis very simple. Each drive tray has its own dual purpose latching mechanism which is used to both insert/extract drives from the chassis and lock the tray in place. Each drive tray supports a light pipe providing a drive status indicator, located on the backplane, to be viewable from the front of the chassis.

Note: Depending on the controller used, SATA/SAS hard disk drives may not report errors using the drive's status indicator.

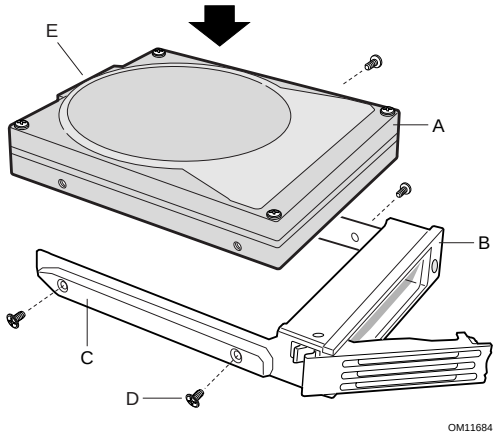


Figure 25. Hard Drive Tray Assembly

A. Hard Drive
B. Drive Carrier
C. Side Rail
D. Mounting Screw
E. Hard Drive Connector

4.2.2 Drive Blanks

Drive blanks must be used when no drive is used in the hard drive tray. Drive blanks simulate the spatial volume of a hard disk, which is required to maintain proper air pressure limits necessary to cool the system.

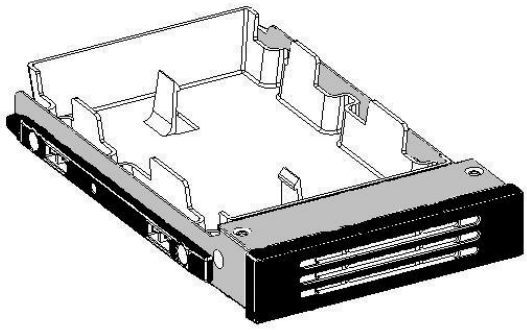


Figure 26. Drive Tray with Drive Blank

4.3 SCSI Hot-Swap Backplane (HSBP)

The Server Chassis SR1450 SCSI hot-swap backplane (HSBP) supports the following feature set:

- QLogic* GEM359 enclosure management controller
  - External non-volatile Flash ROM
  - Two I^2C interfaces
  - Low Voltage Differential (LVD) SCSI Interface
  - SCSI-3 compatible
  - Compliance with SCSI Accessed Fault Tolerant Enclosures (SAF-TE) specification, version 1.00 and addendum
  - Compliance with Intelligent Platform Management Interface (IPMI)
- Support for up to three U320 LVD SCSI Drives
  - Onboard LVD SCSI Termination – SPI-4 compatible
- Temperature Sensor
- Hard Drive Status LEDs
- FRU EEPROM
- One 2x5-pin Power Connector
- Control Panel Connector

4.3.1 Hot-Swap SCSI Backplane Board Layout

The following diagram shows the layout of major components and connectors of the board.

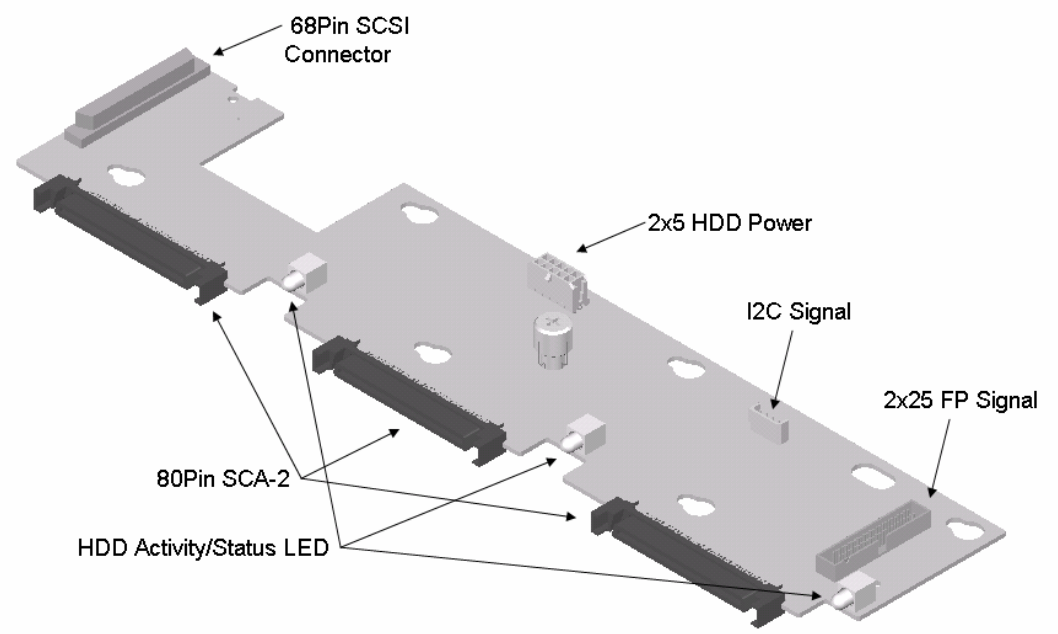


Figure 27. Hot-Swap SCSI Backplane Layout

4.3.2 SCSI Backplane Functional Architecture

This section provides a high-level description of the functionality distributed between the architectural blocks of the SCSI hot swappable backplane. The following figure shows the functional blocks of the hot-swap SCSI backplane.

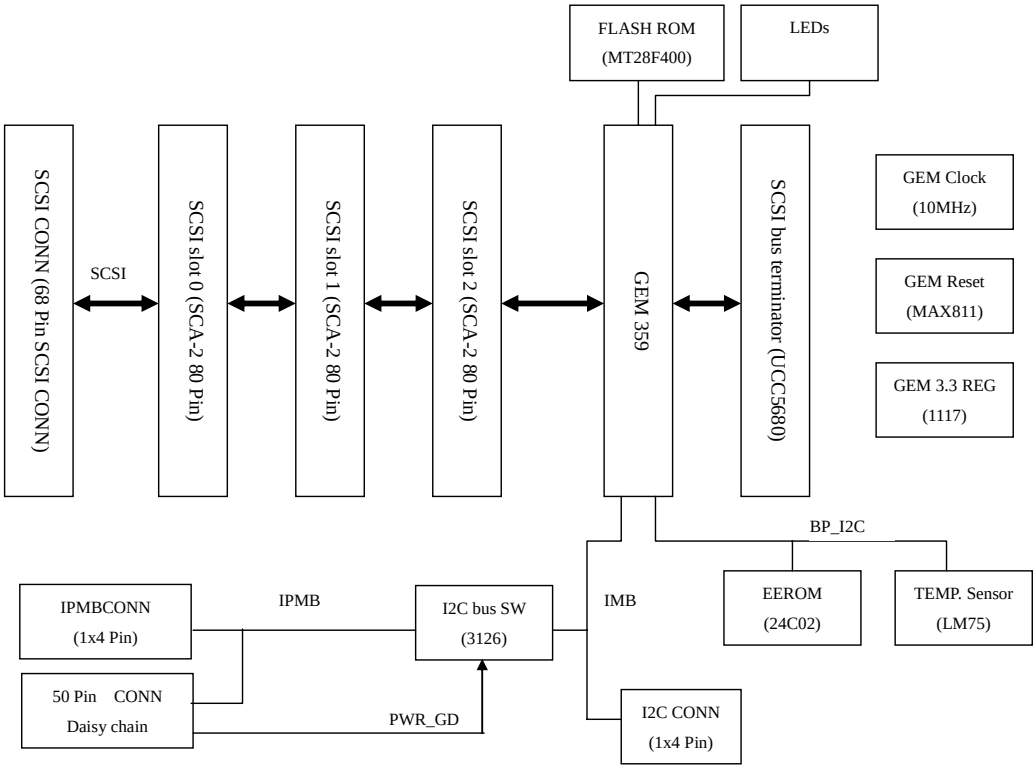


Figure 28. Hot-Swap SCSI Backplane Functional Diagram

4.3.2.1 Enclosure Management Controller

The SCSI backplane utilizes the features of the QLogic* GEM359 for enclosure management, which monitors various aspects of a storage enclosure. The chip provides in-band SAF-TE and SES management through the SCSI interface. Also supported is the IPMI specification by providing management data to the baseboard management controller via the 50-pin connector to the server board.

The GEM359 comes in a 144-pin low-profile Quad Flat Pack package and operates with 3.3V at a clock frequency of 10MHz. It has general input and output pins that allow customization, some of which are used for drive detection and power controller enable/disable functionality.

4.3.2.1.1 SCSI Interface

The GEM359 supports LVD SCSI operation through 8-bit asynchronous SCSI data transfers. The following SCSI Command Set is supported:

- Inquiry
- Read Buffer
- Write Buffer
- Test Unit Ready
- Request Sense
- Send Diagnostic
- Receive Diagnostic

The GEM359 supports the following SAF-TE Command Set:

- Read Enclosure Configuration
- Read Enclosure Status
- Red Device Slot Status
- Read Global Flags
- Write Device Slot Status
- Perform Slot Operation

4.3.2.1.2 I^2C Serial Bus Interface

The GEM359 supports two independent I^2C interface ports with bus speeds of up to 400Kbits. The I^2C core incorporates 8-bit FIFOs for data transfer buffering. The I^2C bus supports the National* LM75 or equivalent I^2C -based temperature sensor. This enables actual temperature value readings to be returned to the host. The Intelligent Platform Management Bus (IPMB) is supported through I^2C port 1.

The following figure provides a block diagram of the I^2C bus connection implemented on the SCSI hot swappable backplane.

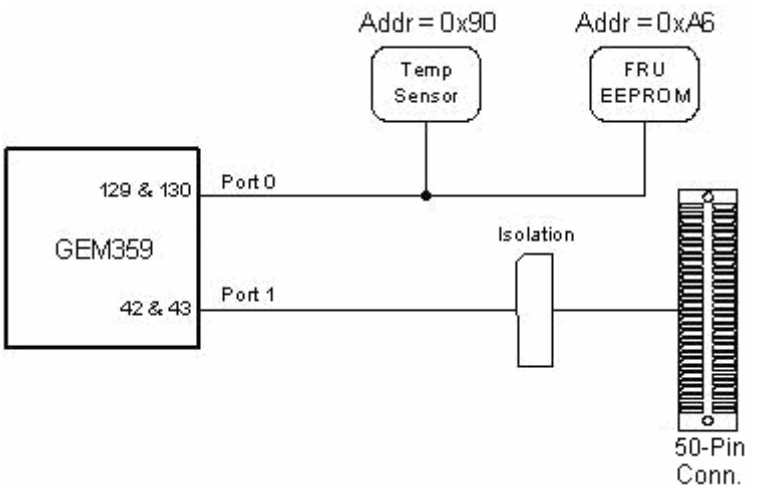


Figure 29. Intel® Server Chassis SR1450 1U SCSI HSBP I2C Bus Connection Diagram

4.3.2.1.3 Temperature Sensor

The SCSI hot swappable backplane provides a National* LM75 or equivalent temperature sensor with over-temperature detector. The host can query the LM75 at any time to read the temperature. The host can program both the temperature alarm threshold and the temperature at which the alarm condition goes away.

4.3.2.1.4 Serial EEPPROM

The SCSI hot swappable backplane provides an Atmel* 24C02 or equivalent serial EEPROM for storing the FRU information. The 24C02 provides 2048 bits of serial electrically erasable and programmable read-only storage.

4.3.2.1.5 External Memory Device

The SCSI hot swappable backplane contains a non-volatile 16K Top Boot Block, 4Mbit Flash memory device that stores the configuration data and operating firmware executed by the GEM359 controller's internal CPU.

The Flash memory operates off the 3.3V rail and housed in a 48-pin TSOP Type 1 package.

4.3.2.1.6 LED Support

The SCSI hot swappable backplane contains a combination green ACTIVITY LED/yellow FAULT LED for each of the three drive connectors. The SCSI hard drive itself drives the ACTIVITY LED portion whenever the drive is accessed. The GEM359 controller drives the FAULT LED portion whenever an error condition is detected.

4.3.3 SCSI Backplane Connector Definitions

As a multi-functional board, several different connectors can be found on the SCSI backplane. This section defines the purpose and pin-out associated with each connector.

4.3.3.1 Power Connector (Backplane to Power Supply Harness)

The SCSI backplane provides power to the three drive bays supporting up to three hard disk drives. A 10-pin power cable is routed from the power distribution board and plugs into a 2 x 5 shrouded plastic PC power connector on the SCSI backplane. The following table shows the power connector pin-out.

Table 34. SCSI Backplane Power Connector Pin-out (J5A1)

Pin	Name	Pin	Name
1	GND	6	P12V
2	GND	7	P12V
3	GND	8	P12V
4	GND	9	P5V_STBY
5	P5V	10	P5V

4.3.3.2 SCSI Connector (Backplane to Baseboard)

A 68-pin SCSI cable is used to interface the SCSI backplane with either the onboard SCSI channel of the server board SE7520JR2, or an add-in PCI SCSI controller installed on either PCI riser card.

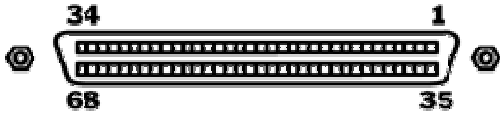


Figure 30. 68-Pin SCSI Cable Connector

Table 35. UltraWide (SE) and Ultra2 (LVD) Ultra320 SCSI Connector Pin-out (J1A1)

Name	Pin	Pin	Name
BP_SCSI_D12P	A1	B1	BP_SCSI_D12N
BP_SCSI_D13P	A2	B2	BP_SCSI_D13N
BP_SCSI_D14P	A3	B3	BP_SCSI_D14N
BP_SCSI_D15P	A4	B4	BP_SCSI_D15N
BP_SCSI_DP1P	A5	B5	BP_SCSI_DP1N
BP_SCSI_D0P	A6	B6	BP_SCSI_D0N
BP_SCSI_D1P	A7	B7	BP_SCSI_D1N
BP_SCSI_D2P	A8	B8	BP_SCSI_D2N
BP_SCSI_D3P	A9	B9	BP_SCSI_D3N
BP_SCSI_D4P	A10	B10	BP_SCSI_D4N
BP_SCSI_D5P	A11	B11	BP_SCSI_D5N
BP_SCSI_D6P	A12	B12	BP_SCSI_D6N
BP_SCSI_D7P	A13	B13	BP_SCSI_D7N
BP_SCSI_DP0P	A14	B14	BP_SCSI_DP0N
GND	A15	B15	GND

Name	Pin	Pin	Name
BP_SCSI_DIFSNS	A16	B16	GND
TERMI_PWR	A17	B17	TERMI_PWR
TERMI_PWR	A18	B18	TERMI_PWR
Unused	A19	B19	Unused
GND	A20	B20	GND
BP_SCSI_ATNP	A21	B21	BP_SCSI_ATNN
GND	A22	B22	GND
BP_SCSI_BSYP	A23	B23	BP_SCSI_BSYN
BP_SCSI_ACKP	A24	B24	BP_SCSI_ACKN
BP_SCSI_RSTP	A25	B25	BP_SCSI_RSTN
BP_SCSI_MSGP	A26	B26	BP_SCSI_MSGN
BP_SCSI_SELP	A27	B27	BP_SCSI_SELN
BP_SCSI_CDP	A28	B28	BP_SCSI_CDN
BP_SCSI_REQP	A29	B29	BP_SCSI_REQN
BP_SCSI_IOP	A30	B30	BP_SCSI_ION
BP_SCSI_D8P	A31	B31	BP_SCSI_D8N
BP_SCSI_D9P	A32	B32	BP_SCSI_D9N
BP_SCSI_D10P	A33	B33	BP_SCSI_D10N
BP_SCSI_D11P	A34	B34	BP_SCSI_D11N

4.3.3.3 Control Panel Interface Connector

The control panel interface connector on the SCSI backplane provides I^2C connectivity. The following table provides the pin-out for the 50-pin connector.

Table 36. SCSI Backplane Control Panel Connector Pin-out (J9B1)

Description	Pin #	Pin #	Description
Unused	1	2	GND
Unused	3	4	GND
Unused	5	6	GND
Unused	7	8	GND
Unused	9	10	GND
Unused	11	12	Unused
Unused	13	14	Unused
Unused	15	16	Unused
Unused	17	18	Unused
Unused	19	20	Unused
Unused	21	22	GND
Unused	23	24	Unused
Unused	25	26	Unused
Unused	27	28	Unused
GND	29	30	Unused
Unused	31	32	Unused
Unused	33	34	Unused
Unused	35	36	Unused

Description	Pin #	Pin #	Description
IPMB_I2C_5VSB_SCL	37	38	GND
IPMB_I2C_5VSB_SDA	39	40	Unused
Unused	41	42	Unused
Unused	43	44	Unused
RST_P6_PWRGOOD	45	46	Unused
Unused	47	48	P5V
PWR_LCD_5VSB	49	50	P5V_STBY

4.3.3.4 SCA2 Hot-Swap SCSI Drive Connectors

The SCSI backplane provides three hot-swap SCA2 connectors, which provide power and SCSI signals using a single connector. Each SCA drive attaches to the backplane using one of these connectors.

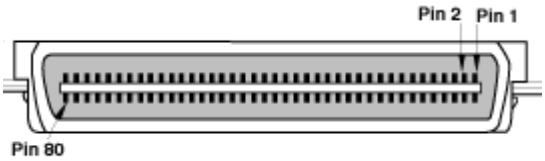


Figure 31. 80-pin SCA2 SCSI Interface

Table 37. 80-Pin SCA2 SCSI Interface Pin-out (J7M1, J4M1, J1M1)

Signal Name	Pin	Pin	Signal Name
GND	41	1	P12V
GND	42	2	P12V
GND	43	3	P12V
SCSI_MATED	44	4	P12V
NC_3V_CHG	45	5	NC_3V_1
BP_SCSI_DIFSNS	46	6	NC_3V_2
BP_SCSI_D11P	47	7	BP_SCSI_D11N
BP_SCSI_D10P	48	8	BP_SCSI_D10N
BP_SCSI_D9P	49	9	BP_SCSI_D9N
BP_SCSI_D8P	50	10	BP_SCSI_D8N
BP_SCSI_IOP	51	11	BP_SCSI_ION
BP_SCSI_REQP	52	12	BP_SCSI_REQN
BP_SCSI_CDP	53	13	BP_SCSI_CDN
BP_SCSI_SELP	54	14	BP_SCSI_SELN
BP_SCSI_MSGP	55	15	BP_SCSI_MSGN
BP_SCSI_RSTP	56	16	BP_SCSI_RSTN
BP_SCSI_ACKP	57	17	BP_SCSI_ACKN
BP_SCSI_BSYP	58	18	BP_SCSI_BSYN
BP_SCSI_ATNP	59	19	BP_SCSI_ATNN
BP_SCSI_DP0P	60	20	BP_SCSI_DP0N
BP_SCSI_D7P	61	21	BP_SCSI_D7N

Signal Name	Pin	Pin	Signal Name
BP_SCSI_D6P	62	22	BP_SCSI_D6N
BP_SCSI_D5P	63	23	BP_SCSI_D5N
BP_SCSI_D4P	64	24	BP_SCSI_D4N
BP_SCSI_D3P	65	25	BP_SCSI_D3N
BP_SCSI_D2P	66	26	BP_SCSI_D2N
BP_SCSI_D1P	67	27	BP_SCSI_D1N
BP_SCSI_D0P	68	28	BP_SCSI_D0N
BP_SCSI_DP1P	69	29	BP_SCSI_DP1N
BP_SCSI_D15P	70	30	BP_SCSI_D15N
BP_SCSI_D14P	71	31	BP_SCSI_D14N
BP_SCSI_D13P	72	32	BP_SCSI_D13N
BP_SCSI_D12P	73	33	BP_SCSI_D12N
SCSI_MATED	74	34	P5V
GND	75	35	P5V
GND	76	36	P5V
HD_ACT_LED_L	77	37	Unused
Unused	78	38	GND
Unused	79	39	Unused
Unused	80	40	Unused
GND	B2	B1	GND

4.4 SATA/SAS Hot-Swap Backplane (HSBP)

The SATA/SAS HSBP supports the following feature set:

- QLogic* GEM424 enclosure management controller
  - External non-volatile SEEPROMs
  - Three I^2C interfaces
  - SATA and SATA-II extension compatible
  - Compliance with SATA Accessed Fault Tolerant Enclosures (SAF-TE) specification, version 1.00 and addendum
  - Compliance with Intelligent Platform Management Interface 1.5 (IPMI)
- Support for up to three SATA or SAS Drives
- Hot Swap Drive support
- Temperature Sensor
- FRU EEPROM
- One 2 x 5-pin Power Connector
- Control Panel Connector
- Drive Status LEDs

4.4.1 SATA/SAS Backplane Layout

The following diagram shows the layout of major components and connectors of the board.

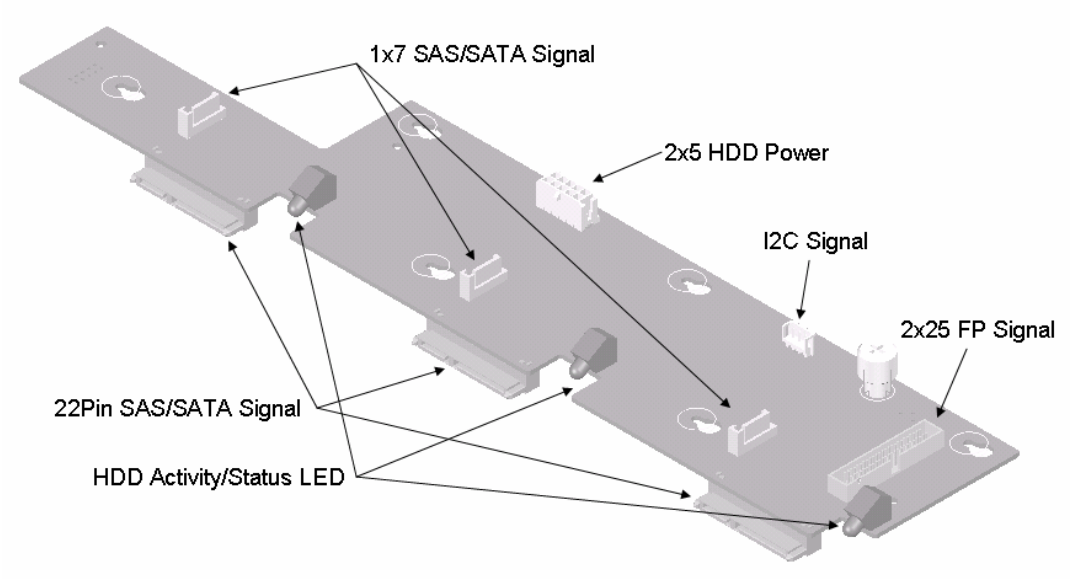


Figure 32. SATA/SAS Backplane Layout

4.4.2 SATA/SAS Backplane Functional Architecture

This section provides a high-level description of the functionality distributed between the architectural blocks of the SATA/SAS HSBP. The following figure shows the functional blocks of the SATA/SAS backplane.

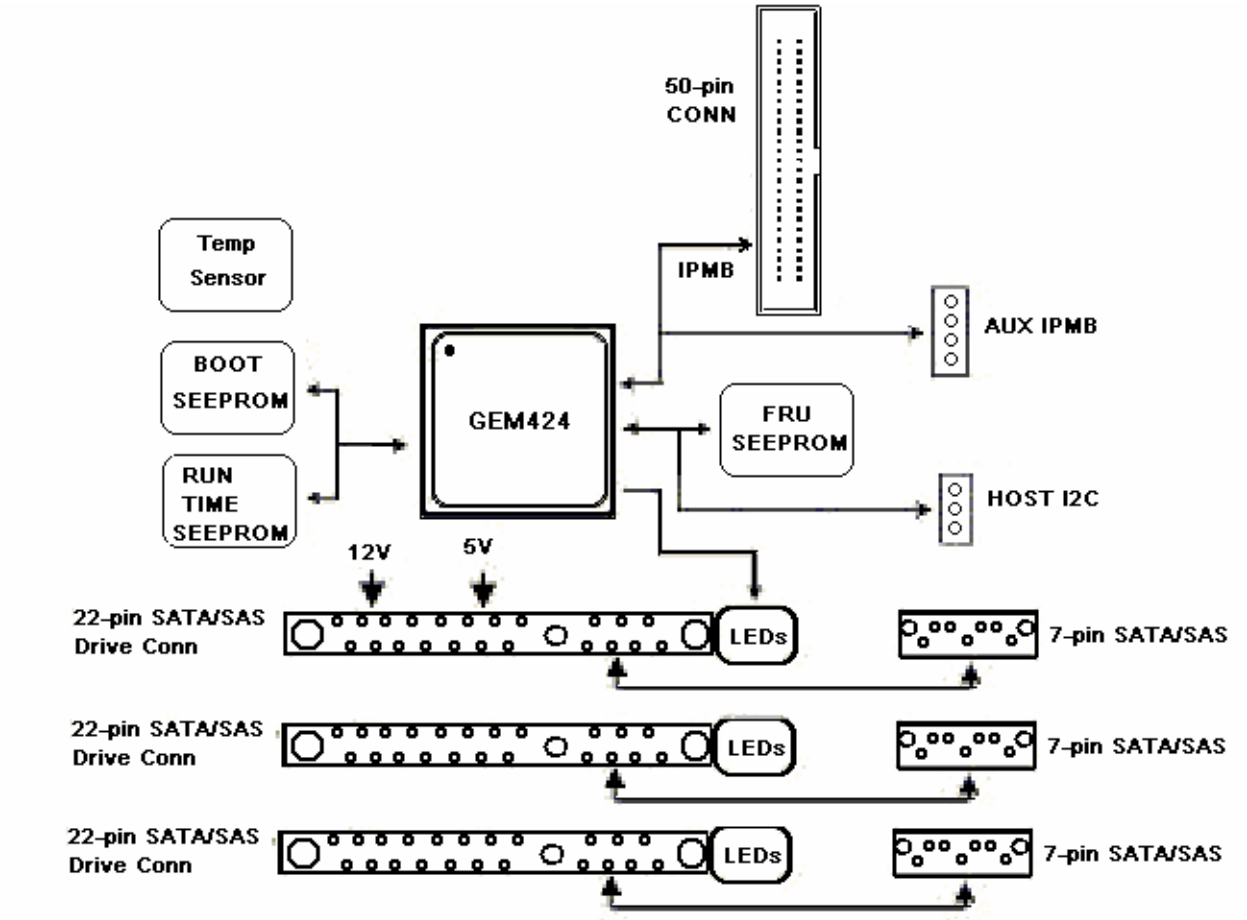


Figure 33. SATA/SAS Backplane Functional Block Diagram

4.4.2.1 Enclosure Management Controller

The SATA/SAS backplane utilizes the features and functionality of the QLogic* GEM424 enclosure management controller, which is capable of monitoring various aspects of a storage enclosure. The chip provides in-band SAF-TE management through the SATA/SAS Host I^2C interface. It also supports the IPMI specification by providing management data to a baseboard management controller through the Intelligent Platform Management Bus (IPMB) via the 50-pin connector to the server board.

The GEM424 comes in a 80-pin Thin Quad Flat Pack (TQFP) package and operates from 3.3-5V and has an input clock frequency of 20MHz. It has general input and output pins that are used for hardware drive detection and driving FAULT and ACTIVITY LEDs.

4.4.2.1.1 SATA/SAS Interface

The GEM424 implements SAF-TE over the HBA I^2C interface. The GEM424 supports the following SAF-TE Command Set:

- Read Enclosure Configuration

- Read Enclosure Status
- Read Device Slot Status
- Read Global Flags
- Write Device Slot Status
- Perform Slot Operation

4.4.2.1.2 I²C Serial Bus Interface

The GEM424 supports two independent I²C interface ports with bus speeds of up to 400Kbits. The I²C core incorporates 8-bit FIFOs for data transfer buffering. The I²C bus supports National* LM75 or equivalent I²C -based temperature sensors. This enables actual temperature value readings to be returned to the host. The Intelligent Platform Management Bus (IPMB) is supported through I²C port 0.

The following figure provides a block diagram of how I²C bus connection is implemented on the SATA/SAS HSBP.

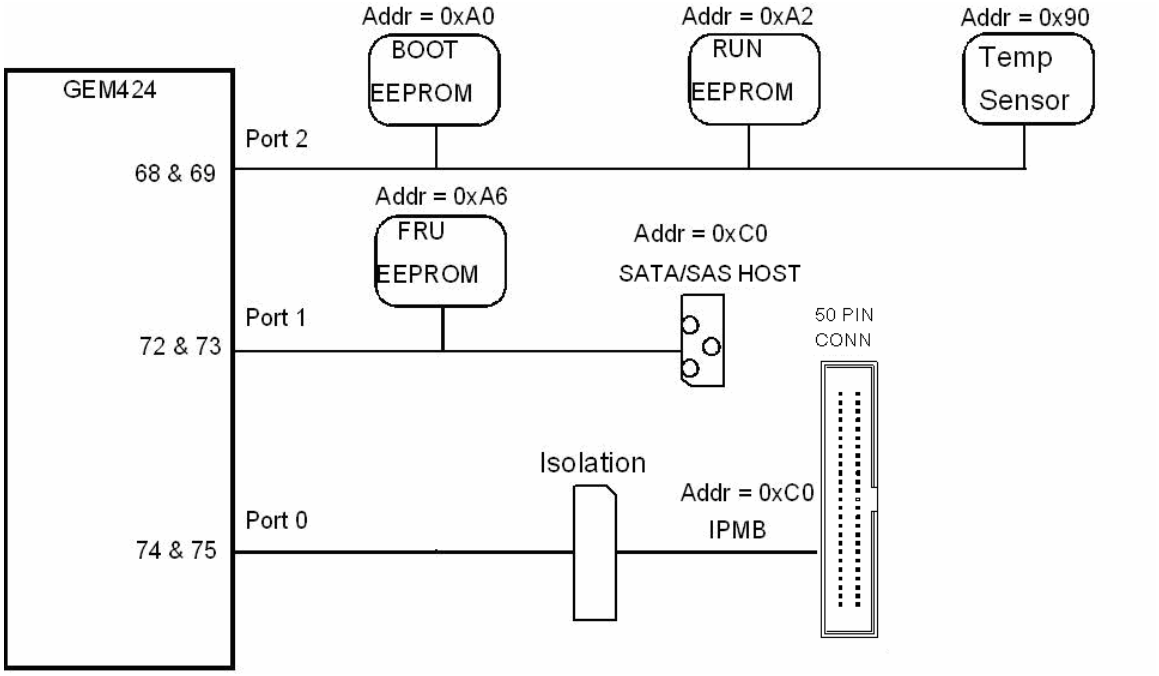


Figure 34. Intel® Server Chassis SR1450 1U SATA/SAS HSBP I²C Bus Connection Diagram

4.4.2.1.3 Temperature Sensor

The SATA/SAS HSBP provides a National* LM75 or equivalent temperature sensor with an over-temperature detector. The host can query the LM75 at any time to read the temperature.

The temperature sensor has an I²C address of 0x90h on Port 0 of the GEM424 controller.

4.4.2.1.4 Serial EEPROM

The SATA/SAS HSBP provides an Atmel* 24C02 or equivalent serial EEPROM for storing the FRU information. The 24C02 provides 2048 bits of serial electrically erasable and programmable read-only storage.

The serial EEPROM has an I^2C address of 0xA6h on Port 1 of the GEM424 controller.

4.4.2.1.5 External Memory Device

The SATA/SAS HSBP contains non-volatile 16K and 64K Serial EEPROM devices for Boot and Run-Time/Configuration code storage respectively. These devices reside on the GEM424's private I^2C bus.

The SEEPROMs operate off the 5.0V rail and are housed in 8-pin SOIC packages.

4.4.2.1.6 LED Support

SR1450 1U SATA/SAS HSBP contains a combination green ACTIVITY LED/amber FAULT LED for each of the three drive connectors. The ACTIVITY LED is driven by the GEM424 or by the drive itself for SATA/SAS hard drives that support the feature, whenever the drive gets accessed. The FAULT LED is driven by the GEM424 controller and is activated whenever an error condition is detected, as defined by the firmware.

Activity and Fault LED functions are only available when a SATA/SAS host controller that supports the SAF-TE protocol over I^2C is connected to the SATA/SAS HSBP via the SATA/SAS Host I^2C connector, J7A1.

Table 38. LED Function

Status LED	Definition
GREEN ON	HDD Activity
AMBER ON	HDD Fail
AMBER Blinking	Rebuild in progress

4.4.3 SATA/SAS Backplane Connector Definitions

4.4.3.1 Power Connector

The SATA backplane provides power for up to three SATA drives. A 6-pin power cable from the power supply harness is routed to the backplane and plugs into a 2x5 shrouded plastic PC power connector. This power supply harness also provides connectors to power one slim-line floppy drive (with the optional floppy to hard drive conversion kit) and one CD-ROM or DVD-ROM drive (in the slimline drive bay). The following table provides the connector pin-out.

Table 39. SATA/SAS Backplane Power Connector Pin-out

Pin	Name	Pin	Name
1	GND	6	P12V
2	GND	7	P12V
3	GND	8	P12V
4	GND	9	P5V_STBY
5	P5V	10	P5V

4.4.3.2 SATA/SAS Connectors (Backplane to Server Board)

The SATA/SAS backplane has three 7-pin SATA/SAS connectors. These connectors relay SATA/SAS signals from the server board or add-in SATA/SAS PCI cards to the drives. Each connector is used for a separate SATA/SAS channel and is configured as a bus master. The following table provides the connector pin-out.

Table 40. 7-Pin SATA/SAS Connector Pin-out (J2B1, J5B1, J8B2)

Pin	Name
1	GND
2	DRV_RX_P
3	DRV_RX_N
4	GND
5	DRV_TX_P
6	DRV_TX_N
7	GND
8	GND
9	GND

4.4.3.3 Hot-Swap SATA/SAS Drive Connectors

The SATA/SAS drive interface combines both SATA/SAS and power signals into a single connector. The following table provides the pin-out.

Table 41. 22-Pin SATA/SAS Connector Pin-out (J2M1, J5M1, J8M1)

Name	Pin	Pin	Name
GND	1	13	GND
DRV_RX_P	2	14	P5V Precharge
DRV_RX_N	3	15	P5V
GND	4	16	P5V
DRV_TX_P	5	17	GND
DRV_TX_N	6	18	HDD_ACT_LED_N
GND	7	19	GND
P3V3	8	20	P12V Precharge
P3V3	9	21	P12V
P3V3	10	22	P12V
GND	11	23	GND
HD_INSTALL_N	12	24	GND

4.4.3.4 Control Panel Interface Connector

The control panel interface connector on the SATA/SAS backplane provides I^2C connectivity. The following table provides the pin-out for the 50-pin connector.

Table 42. Floppy/Control Panel/CD-ROM Connector Pin-out (J9B1)

Description	Pin #	Pin #	Description
Unused	1	2	GND
Unused	3	4	GND
Unused	5	6	GND
Unused	7	8	GND
Unused	9	10	GND
Unused	11	12	Unused
Unused	13	14	Unused
Unused	15	16	Unused
Unused	17	18	Unused
Unused	19	20	Unused
Unused	21	22	GND
Unused	23	24	Unused
Unused	25	26	Unused
Unused	27	28	Unused
GND	29	30	Unused
Unused	31	32	Unused
Unused	33	34	Unused
Unused	35	36	Unused
IPMB_I2C_5VSB_SCL	37	38	GND
IPMB_I2C_5VSB_SDA	39	40	Unused
Unused	41	42	Unused
Unused	43	44	Unused
RST_P6_PWRGOOD	45	46	Unused
Unused	47	48	P5V
PWR_LCD_5VSB	49	50	P5V_STBY

5. Standard Control Panel

The standard control panel supports several push buttons and status LEDs, along with USB to centralize system control, monitoring, and accessibility to within a common compact design.

The control panel assembly comes pre-assembled and is modular in design. The control panel assembly module slides into a predefined slot on the front of the chassis. Once installed, communication to the server board can be achieved by attaching a 50-pin cable to a hot-swap backplane and then to the server board. In addition, a USB cable is routed to a USB port on the server board.

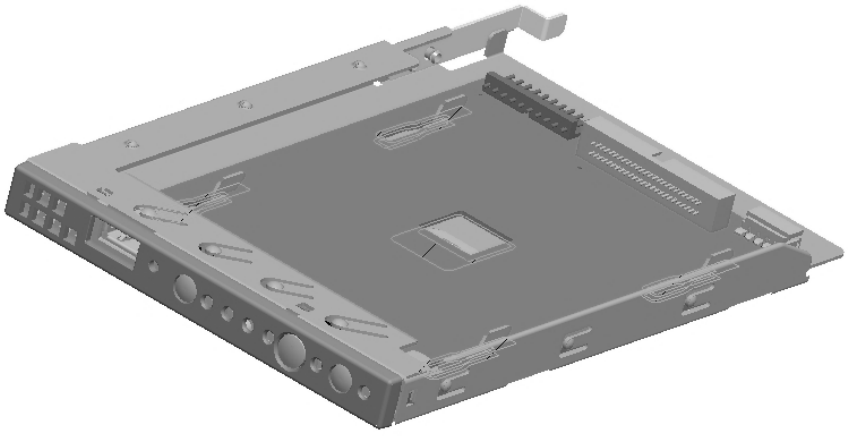


Figure 35. Standard Control Panel Assembly Module

5.1 Control Panel Buttons

The standard control panel assembly houses several system control buttons. Each LED function is listed in the following table.

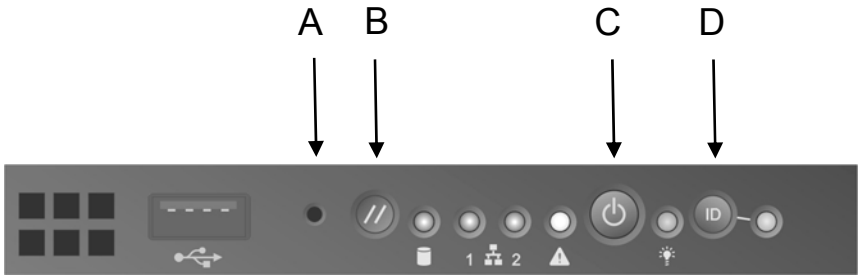


Figure 36. Control Panel Buttons

Table 43. Contol Button and Intrusion Switch Functions

Reference	Feature	Function
A	NMI Button	Pressing the recessed button with a paper clip or pin puts the server in a halt state for diagnostic purposes and allows issuance of a non-maskable interrupt. After issuing the interrupt, a memory download can be performed to determine the cause of the problem.
B	Reset Button	Reboots and initializes the system.
C	Power / Sleep Button	Toggles the system power on/off. This button also functions as a Sleep Button if enabled by an ACPI-compliant operating system.
D	ID Button	Toggles the front panel ID LED and the server board ID LED on/off. The baseboard ID LED is visible through the rear of the chassis, thereby allowing the server to be located from the rear of a rack of servers.

5.2 Control Panel LED Indicators

The control panel houses six LEDs, which are viewable with or without the front outer bezel to display the system's operating state.

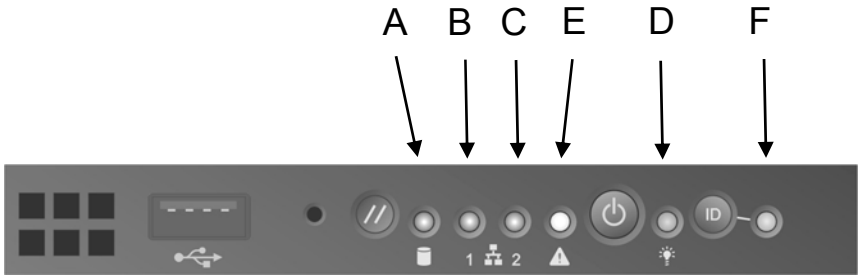


Figure 37. Control Panel LEDs

The following table identifies each LED and describes its functionality.

Table 44. Control Panel LED Functions

Reference	LED	Color	State	Description
A	Disk Activity	Green	Random blink	Provides an indicator for disk activity.
		Off	Off [3]	No hard disk activity
B and C	NIC1 / NIC2 Activity	Green	On	NIC Link
		Green	Blink	NIC Activity
D	Power / Sleep (on standby power)	Green	On	Legacy power on / ACPI S0 state
			Blink [1,4]	Sleep / ACPI S1 state
		Off	Off	Power Off / ACPI S4 or S5 state
E	System Status (on standby power)	Green	On	Running / normal operation
			Blink [1,2]	Degraded
		Amber	On	Critical or non-recoverable condition.
			Blink [1,2]	Non-critical condition.
		Off	Off	POST / system stop.
F	System Identification	Blue	Blink	Identify active via command or button.
		Off	Off	No Identification.

Notes:

1. Blink rate is ~1 Hz at 50% duty cycle.
2. The amber status takes precedence over the green status. When the amber LED is on or blinking, the green LED is off.
3. Also off when the system is powered off (S4/S5) or in a sleep state (S1).
4. The power LED sleep indication is maintained on standby by the chipset. If the system is powered down without going through BIOS, the LED state in effect at the time of power off will be restored when the system is powered on until the BIOS clears it. If the system is not powered down normally, it is possible that the Power LED will be blinking at the same time that the system status LED is off due to a failure or configuration change that prevents the BIOS from running.

The current limiting resistors for the power LED, system fault LED, and NIC LEDs are located on the Intel® Server Board SE7520JR2.

5.2.1 Power / Sleep LED

Table 45. SSI Power LED Operation

State	Power Mode	LED	Description
Power Off	Non-ACPI	Off	System power is off, and the BIOS has not initialized the chipset.
Power On	Non-ACPI	On	System power is on, but the BIOS has not yet initialized the chipset.
S5	ACPI	Off	Mechanical is off, and the operating system has not saved any context to the hard disk.
S4	ACPI	Off	Mechanical is off. The operating system has saved context to the hard disk.
S3-S1	ACPI	Slow blink 1	DC power is still on. The operating system has saved context and has gone into a level of low-power state.
S0	ACPI	Steady on	System and the operating system are up and running.

Note:
1. Blink rate is ~ 1Hz at 50% duty cycle.

5.2.2 System Status LED

Note: Some of the following status conditions may or may not be reported if the system is not configured with an Intel® Management Module Professional Edition or Advanced Edition. Refer to the Server Board SE7520JR2 Technical Product Specification for details.

5.2.2.1 Critical Conditions

A critical condition is any critical or non-recoverable threshold crossing associated with the following events:

- Temperature, voltage, or fan critical threshold crossing.
- Power subsystem failure. The BMC asserts this failure whenever it detects a power control fault (e.g., the BMC detects that the system power is remaining ON even though the BMC has de-asserted the signal to turn off power to the system.
- A hot-swap backplane would use the Set Fault Indication command to indicate when one or more of the drive fault status LEDs are asserted on the hot-swap backplane.
- The system is unable to power up due to incorrectly installed processor(s), or processor incompatibility.
- Satellite controller sends a critical or non-recoverable state, via the Set Fault Indication command to the BMC.

- Critical event logging errors, including System Memory Uncorrectable ECC error, and fatal / uncorrectable bus errors such as PCI SERR and PERR.

5.2.2.2 Non-Critical Conditions

A non-critical condition is threshold crossing associated with the following events:

- Temperature, voltage, or fan non-critical threshold crossing
- Chassis intrusion
- Satellite controller sends a non-critical state, via the Set Fault Indication command, to the BMC.
- Set Fault Indication command from system BIOS. The BIOS may use the Set Fault Indication command to indicate additional 'non-critical' states, such as a system memory or a CPU configuration change.

5.2.2.3 Degraded Conditions

A degraded condition is associated with the following events:

- Non-redundant power supply operation. This applies only when the BMC is configured for a redundant power subsystem.
- One or more processors are disabled by Fault Reliant Booting (FRB) or BIOS.
- The BIOS has disabled or mapped out some of the system memory.

5.2.3 Drive Activity LED

The drive activity LED on the front panel indicates drive activity from the onboard hard disk controllers. The Server Board SE7520JR2 also provides a header giving access to this LED for add-in controllers.

5.2.4 System Identification LED

The blue system identification LED is used to help identify a system for servicing. This is especially useful when the system is installed in a high-density rack or cabinet that is populated with many similar systems. The system ID LED will blink when the System ID button on the control panel is pressed or it can be illuminated remotely through server management software.

5.3 Control Panel Connectors

The standard control panel has one USB 2.0 port. The following table provides the pin-out.

Table 46. External USB Connectors (J1A1)

Pin #	Description
1	PWR_FP_USB2
2	USB_DN2_FP_R
3	USB_DP2_FP_R
4	GND

5.4 Internal Control Panel Assembly Headers

The control panel interface board has two internal headers:

- A 50-pin header (J5B1) provides control and status information to/from the server board through a 50-pin flat cable that provides connectivity to the hot-swap backplane and the server board.
- A 10-pin header (J5A1) is used to provide USB support to the control panel. The round 10-pin cable is routed from the control panel assembly to a matching connector on the server board.

The following tables provide pin-outs for both types of connectors.

Table 47. 50-Pin Control Panel Connector (J5B1)

Description	Pin #	Pin #	Description
PWR_LCD_5VSB	2	1	P5V_STBY
HDD_LED_ACT_R_L	4	3	P5V
RST_P6_PWRGOOD	6	5	FP_SYS_FLT_LED1_R_L
PWR_LED_5VSB	8	7	FP_SYS_FLT_LED2_R_L
FP_PWR_LED_R_L	10	9	FAULT_LED_5VSB
IPMB_5VSB_SDA	12	11	HDD_LED_P3V3_A
IPMB_5VSB_SCL	14	13	GND
FP_PWR_BTN_L	16	15	FP_ID_LED_R_L
HDD_FAULT_LED_R_L	18	17	NIC2_LINK_LED_R_L
FP_RST_BTN_L	20	19	NIC2_ACT_LED_L
GND	22	21	BP_I2C_5V_SDA
FP_ID_SW_L	24	23	BP_I2C_5V_SCL
Unused	26	25	FP_CHASSIS_L
NIC1_ACT_LED_L	28	27	NIC1_LINK_LED_R_L
FP_NMI_BTN_L	30	29	GND
EMP_DSR2_L	32	31	EMP_INUSE_L
EMP_SIN2	34	33	EMP_SOUT2
EMP_RTS2_L	36	35	EMP_CTS2_L
EMP_DTR2_L	38	37	EMP_DCD2_L
VGA_INUSE_L	40	39	1_WIRE_BUS
VGA_VSYNC_FP_L	42	41	GND
VGA_HSYNC_FP_L	44	43	GND
VGA_BLUE_FP	46	45	GND
VGA_GREEN_FP	48	47	GND
VGA_RED_FP	50	49	GND

A 10-pin USB header provides control for one USB port from the server board.

Table 48. Internal USB Header (J5A1)

Pin #	Description
1	PWR_FP_USB2
2	USB_DN2_FP
3	USB_DP2_FP
4	GND
5	GND

Pin #	Description
6	PWR_FP_USB3
7	USB_DN3_FP
8	USB_DP3_FP
9	GND
10	GND

6. Intel® Local Control Panel

The Intel® Local Control Panel utilizes a combination of control buttons, LEDs, and an LCD display to provide system accessibility, monitoring, and control functions. The control panel assembly is pre-assembled and is modular in design. The module slides into a slot on the front of the chassis and is designed so that it can be adjusted for use with or without an outer front bezel.

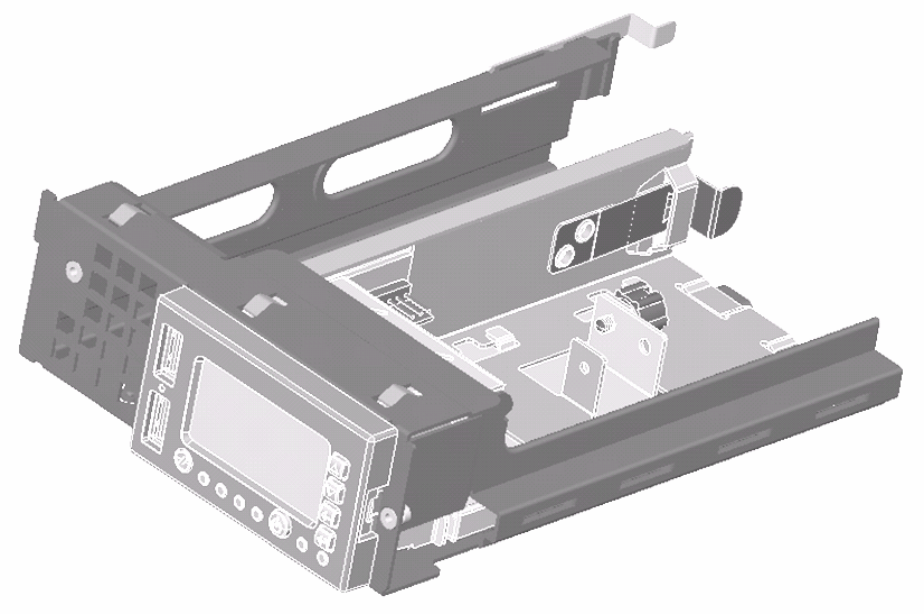
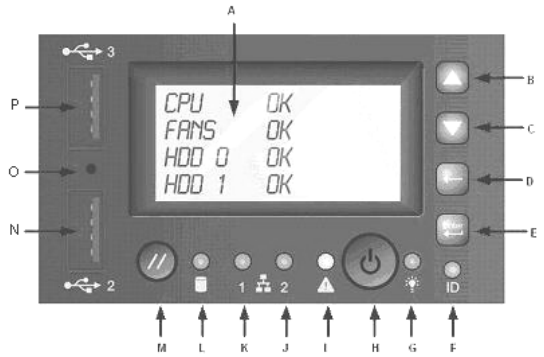


Figure 38. Intel® Local Control Panel Assembly Module

Note: The Intel® Local Control Panel can only be used when either the Intel® Management Module Professional Edition or Advanced Edition is installed in the system.

The following diagram provides an overview of the control panel features.



A	LCD Display	I	System Status LED
B	LCD Menu Control Button – Up	J	NIC 2 Activity LED
C	LCD Menu Control Button – Down	K	NIC 1 Activity LED
D	LCD Menu Control Button – Previous Option	L	Hard Drive Activity LED
E	LCD Menu Control Button – Previous Page	M	System Reset Button
F	ID LED	N	USB 2.0 Port
G	Power LED	O	NMI Buttom (Tool Required)
H	System Power Button	P	USB 2.0 Port

Figure 39. Intel® Local Contol Panel Overview

6.1 LED Functionality

The following table identifies each LED and describes their functionality.

Table 49. Control Panel LED Functions

LED	Color	State	Description
NIC1 / NIC2 Activity	Green	On	NIC Link
	Green	Blink	NIC Activity
Power / Sleep (on standby power)	Green	On	Legacy power on / ACPI S0 state
		Blink [1,4]	Sleep / ACPI S1 state
	Off	Off	Power Off / ACPI S4 or S5 state
System Status (on standby power)	Green	On	Running / normal operation
		Blink [1,2]	Degraded
	Amber	On	Critical or non-recoverable condition.
		Blink [1,2]	Non-critical condition.
	Off	Off	POST / system stop.
Disk Activity	Green	Random blink	Provides an indicator for disk activity.
	Off	Off [3]	No hard disk activity
System Identification	Blue	Blink	Identify active via command or button.
	Off	Off	No Identification.

Notes:
1. Blink rate is ~1 Hz at 50% duty cycle.
2. The amber status takes precedence over the green status. When the amber LED is on or blinking, the green LED is off.
3. Also off when the system is powered off (S4/S5) or in a sleep state (S1).
4. The power LED sleep indication is maintained on standby by the chipset. If the system is powered down without going through BIOS, the LED state in effect at the time of power off will be restored when the system is powered on until the BIOS clears it. If the system is not powered down normally, it is possible that the Power LED will be blinking at the same time that the system status LED is off due to a failure or configuration change that prevents the BIOS from running.

The current limiting resistors for the power LED, the system fault LED, and the NIC LEDs are located on the Server Board SE7520JR2.

6.1.1 Power / Sleep LED

Table 50. SSI Power LED Operation

State	Power Mode	LED	Description
Power Off	Non-ACPI	Off	System power is off, and the BIOS has not initialized the chipset.
Power On	Non-ACPI	On	System power is on, but the BIOS has not yet initialized the chipset.
S5	ACPI	Off	Mechanical is off, and the operating system has not saved any context to the hard disk.
S4	ACPI	Off	Mechanical is off. The operating system has saved context to the hard disk.
S3-S1	ACPI	Slow blink 1	DC power is still on. The operating system has saved context and gone into a level of low-power state.
S0	ACPI	Steady on	System and the operating system are up and running.

Notes:
1. Blink rate is ~ 1Hz at 50% duty cycle.

6.1.2 System Status LED

6.1.2.1 Critical Conditions

A critical condition is any critical or non-recoverable threshold crossing associated with the following events:

- Temperature, voltage, or fan critical threshold crossing.
- Power subsystem failure. The BMC asserts this failure whenever it detects a power control fault (e.g., the BMC detects that the system power is remaining ON even though the BMC has de-asserted the signal to turn off power to the system.
- A hot-swap backplane would use the Set Fault Indication command to indicate when one or more of the drive fault status LEDs are asserted on the hot-swap backplane.
- The system is unable to power up due to incorrectly installed processor(s), or processor incompatibility.
- Satellite controller sends a critical or non-recoverable state, via the Set Fault Indication command to the BMC.
- Critical event logging errors, including System Memory Uncorrectable ECC error, and fatal / uncorrectable bus errors such as PCI SERR and PERR.

6.1.2.2 Non-Critical Conditions

A non-critical condition is threshold crossing associated with the following events:

- Temperature, voltage, or fan non-critical threshold crossing
- Chassis intrusion
- Satellite controller sends a non-critical state, via the Set Fault Indication command, to the BMC.

- Set Fault Indication command from system BIOS. The BIOS may use the Set Fault Indication command to indicate additional 'non-critical' status such as a system memory or a CPU configuration change.

6.1.2.3 Degraded Conditions

A degraded condition is associated with the following events:

- Non-redundant power supply operation. This applies only when the BMC is configured for a redundant power subsystem.
- One or more processors are disabled by Fault Resilient Booting (FRB) or BIOS.
- The BIOS has disabled or mapped out some of the system memory.

6.1.3 Drive Activity LED

The drive activity LED on the front panel indicates drive activity from the onboard hard disk controllers. The Server Board SE7520JR2 also provides a header giving access to this LED for add-in controllers.

6.1.4 System Identification LED

The blue system identification LED is used to help identify a system for servicing. This is especially useful when the system is installed in a high-density rack or cabinet that is populated with many similar systems. The system ID LED will blink when the System ID button on the control panel is pressed or it can be illuminated remotely through server management software.

6.2 Internal Control Panel Headers

The Control Panel interface board has four internal headers:

- A 50-pin header provides control and status information to/from the server board through a 50-pin flat cable that provides connectivity to the hot-swap backplane and the server board.
- A 10-pin header is used to provide USB support to the control panel. The round 10-pin cable is routed from the control panel assembly to a matching connector on the server board.
- A 4-pin IPMI Header (not used)
- A 4-pin NMI/Temp Sensor Header

The following tables provide the pin-outs for each of these headers.

Table 51. 50-Pin Control Panel Connector

Description	Pin #	Pin #	Description
PWR_LCD_5VSB	2	1	P5V_STBY
HDD_LED_ACT_R_L	4	3	P5V
RST_P6_PWRGOOD	6	5	FP_SYS_FLT_LED1_R_L
PWR_LED_5VSB	8	7	FP_SYS_FLT_LED2_R_L
FP_PWR_LED_R_L	10	9	FAULT_LED_5VSB
IPMB_5VSB_SDA	12	11	HDD_LED_P3V3_A
IPMB_5VSB_SCL	14	13	GND
FP_PWR_BTN_L	16	15	FP_ID_LED_R_L

Description	Pin #	Pin #	Description
HDD_FAULT_LED_R_L	18	17	NIC2_LINK_LED_R_L
FP_RST_BTN_L	20	19	NIC2_ACT_LED_L
GND	22	21	BP_I2C_5V_SDA
FP_ID_SW_L	24	23	BP_I2C_5V_SCL
Unused	26	25	FP_CHASSIS_L
NIC1_ACT_LED_L	28	27	NIC1_LINK_LED_R_L
FP_NMI_BTN_L	30	29	GND
EMP_DSR2_L	32	31	EMP_INUSE_L
EMP_SIN2	34	33	EMP_SOUT2
EMP_RTS2_L	36	35	EMP_CTS2_L
EMP_DTR2_L	38	37	EMP_DCD2_L
VGA_INUSE_L	40	39	1_WIRE_BUS
VGA_VSYNC_FP_L	42	41	GND
VGA_HSYNC_FP_L	44	43	GND
VGA_BLUE_FP	46	45	GND
VGA_GREEN_FP	48	47	GND
VGA_RED_FP	50	49	GND

Table 52. Internal USB Header

Pin #	Description
1	PWR_FP_USB2
2	USB_DN2_FP
3	USB_DP2_FP
4	GND
5	GND
6	PWR_FP_USB3
7	USB_DN3_FP
8	USB_DP3_FP
9	GND
10	GND

Table 53. IPMI Header

Pin #	Description
1	IPMB_5VSB_SDA
2	GND
3	IPMB_5VSB_SCL
4	P5V_STBY

Table 54. Internal NMI/Temp Sensor Header

Pin #	Description
1	GND
2	FP_NMI_BTN_L
3	3.3VSB
4	1_WIRE_BUS

7. PCI Riser Cards and Assembly

The Server Board SE7520JR2 provides two PCI riser slots, one supporting only low profile add-in card risers, and the other used for full height add-in card risers. The riser cards for these slots are not interchangeable due to their orientation on the board and connector differences. The Low Profile riser slot is only capable of supporting a riser using PCI-X cards. The Full-Height riser slot is capable of supporting riser cards that follow either the PCI-X or PCI-Express specifications.

The riser assembly for the Server Chassis SR1450 is tool-less. Stand-offs allow the riser cards to slide onto the assembly where a latching mechanism than holds each riser in place. Holding down the latch releases the risers for easy removal.

When re-inserting the riser assembly into the chassis, tabs on the back of the assembly should be aligned with slots on the back edge of the chassis. The tabs fit into the slots securing the riser assembly to the chassis when the top cover is in place.

The riser assembly provides two extraction levers to assist with riser assembly removal from the riser slots.

7.1 Riser Card Options

There are 3 different riser card options offered for use in the Server Chassis SR1450.

- Low Profile PCI-X – capable of supporting a single 66/100 MHz PCI-X add-in card
- Full Height PCI-X – capable of supporting a single PCI-X 66/100/133 MHz card
- Full Height PCI-Express – capable of supporting a single X8 PCI-Express add-in card

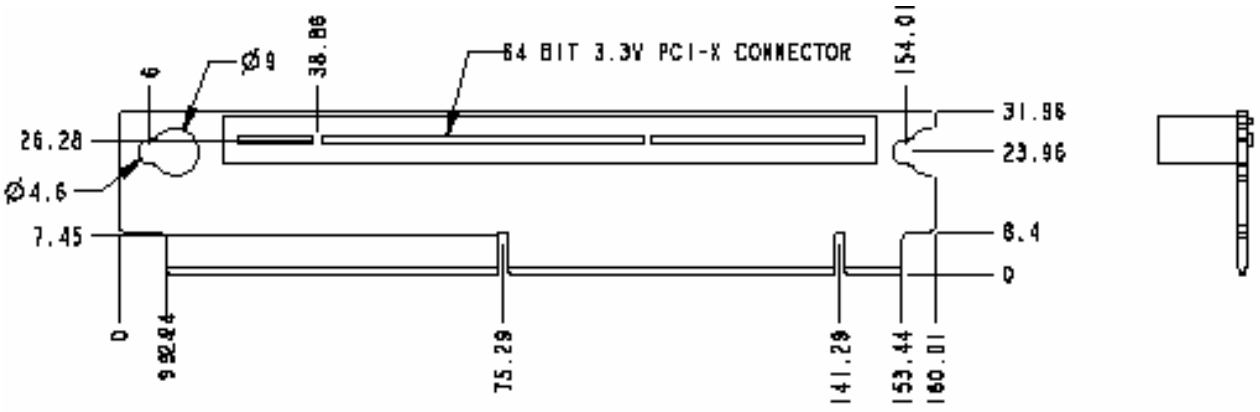


Figure 40. 1U Full-Height PCI-X Riser Card Mechanical Drawing

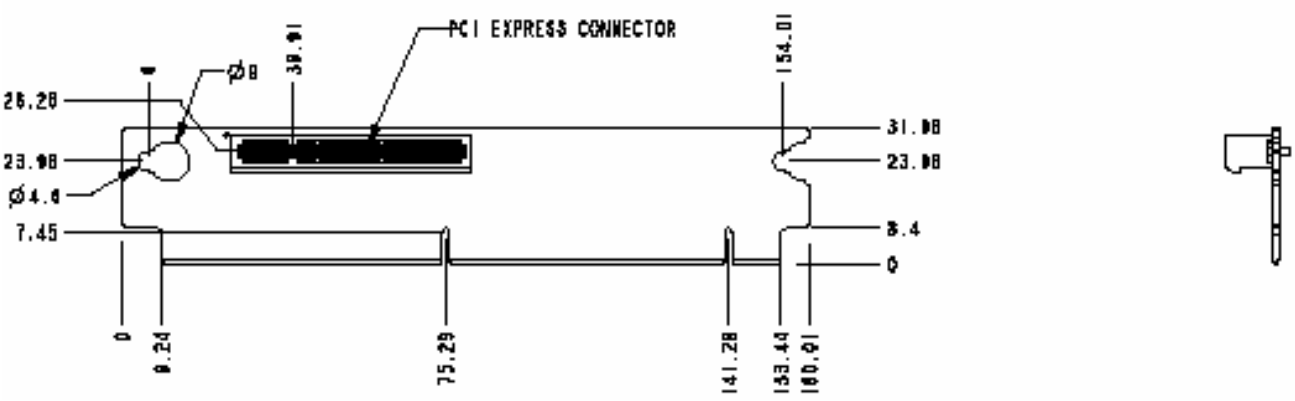


Figure 41. 1U Full-Height PCI-Express Riser Card Mechanical Drawing

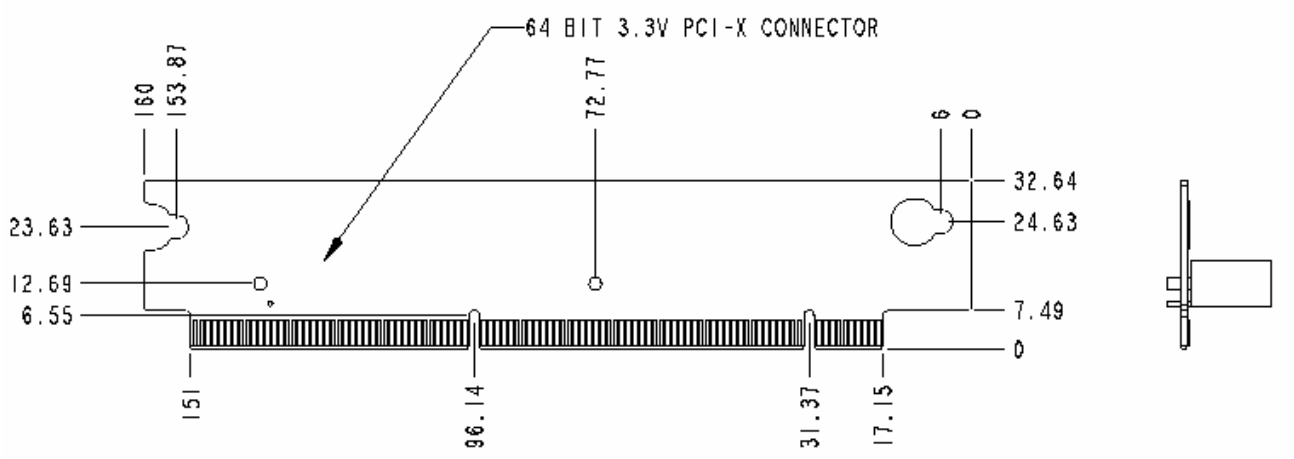


Figure 42. 1U Low-Profile PCI-X Riser Card Mechanical Drawing

8. Supported Intel® Server Boards

The Server Chassis SR1450 is mechanically and functionally designed to support all four SKUs of the Intel® Server Board SE7520JR2.

8.1 Server Board SE7520JR2 SKU Availability

The name SE7520JR2 is used to describe the family of boards that are available under a common product name. The core features for each board will be common; however, each board will have the following distinctions:

Product Code	Feature Distinctions
SE7520JR2SCSID2	Onboard SCSI + Onboard SATA/SAS (RAID) + DDR2 – 400 MHz
SE7520JR2SCSID1	Onboard SCSI + Onboard SATA/SAS (RAID) + DDR – 266/333 MHz
SE7520JR2ATAD2	Onboard SATA/SAS (RAID) + DDR2 – 400 MHz
SE7520JR2ATAD1	Onboard SATA/SAS (RAID) + DDR – 266/333 MHz

8.2 Server Board SE7520JR2 Feature Set

- Dual processor slots supporting 800MHz System Bus Intel® Xeon™ processors
- Intel® E7520 Chipset (MCH, PXH, ICH-5R)
- Two PCI riser slots
  - Riser Slot 1: Supports Low Profile PCI-X 66/100MHz PCI-X cards
  - Riser Slot 2: Using Intel® adaptive slot technology and different riser cards, this slot is capable of supporting Full Height PCI-X 66/100/133 or PCI-Express cards.
- Six DIMM slots supporting DDR2 – 400MHz[1] memory or DDR – 266/333 MHz[2]
- Dual channel LSI* 53C1030 Ultra320 SCSI Controller with integrated RAID 0/1 support
- Dual Intel® 82546GB 10/100/1000 Network Interface Controllers (NICs)
- Onboard ATI* Rage XL video controller with 8MB SDRAM
- Onboard platform instrumentation using a National* PC87431M mini-BMC
- External IO connectors
  - Stacked PS2 ports for keyboard and mouse
  - RJ45 Serial B Port
  - Two RJ45 NIC connectors
  - A 15-pin video connector
  - Two USB 2.0 ports
  - A U320 High density SCSI connector (Channel B)
- Internal IO Connectors / Headers

[1] The use of DDR2 - 400 MHz or DDR - 266/333 MHz DIMMs is dependant on which board SKU is used. DDR-2 DIMMs cannot be used on a board designed to support DDR. DDR DIMMs cannot be used on boards designed to support DDR-2.

[2] The use of DDR2 - 400 MHz or DDR - 266/333 MHz DIMMs is dependant on which board SKU is used. DDR-2 DIMMs cannot be used on a board designed to support DDR. DDR DIMMs cannot be used on boards designed to support DDR-2.

  - Two onboard USB port headers. Each header is capable of supporting two USB 2.0 ports.
  - One 10-pin DH10 Serial A Header
  - One Ultra320 68-pin SCSI Connector (Channel A)
  - Two SATA/SAS connectors with integrated chipset RAID 0/1 support
  - One ATA100 connector
  - One floppy connector
  - SSI-compliant and custom control panel headers
  - SSI-compliant 24-pin main power connector. This supports ATX-12V standard in the first 20 pins
  - Intel® Management Module (IMM) connector
- Intel® Light-Guided Diagnostics on all FRU devices (processors, memory, power)
- Port-80 Diagnostic LEDs displaying POST codes

The following figure shows the board layout of the Server Board SE7520JR2. Each connector and major component is identified by number and is identified in Table 55.

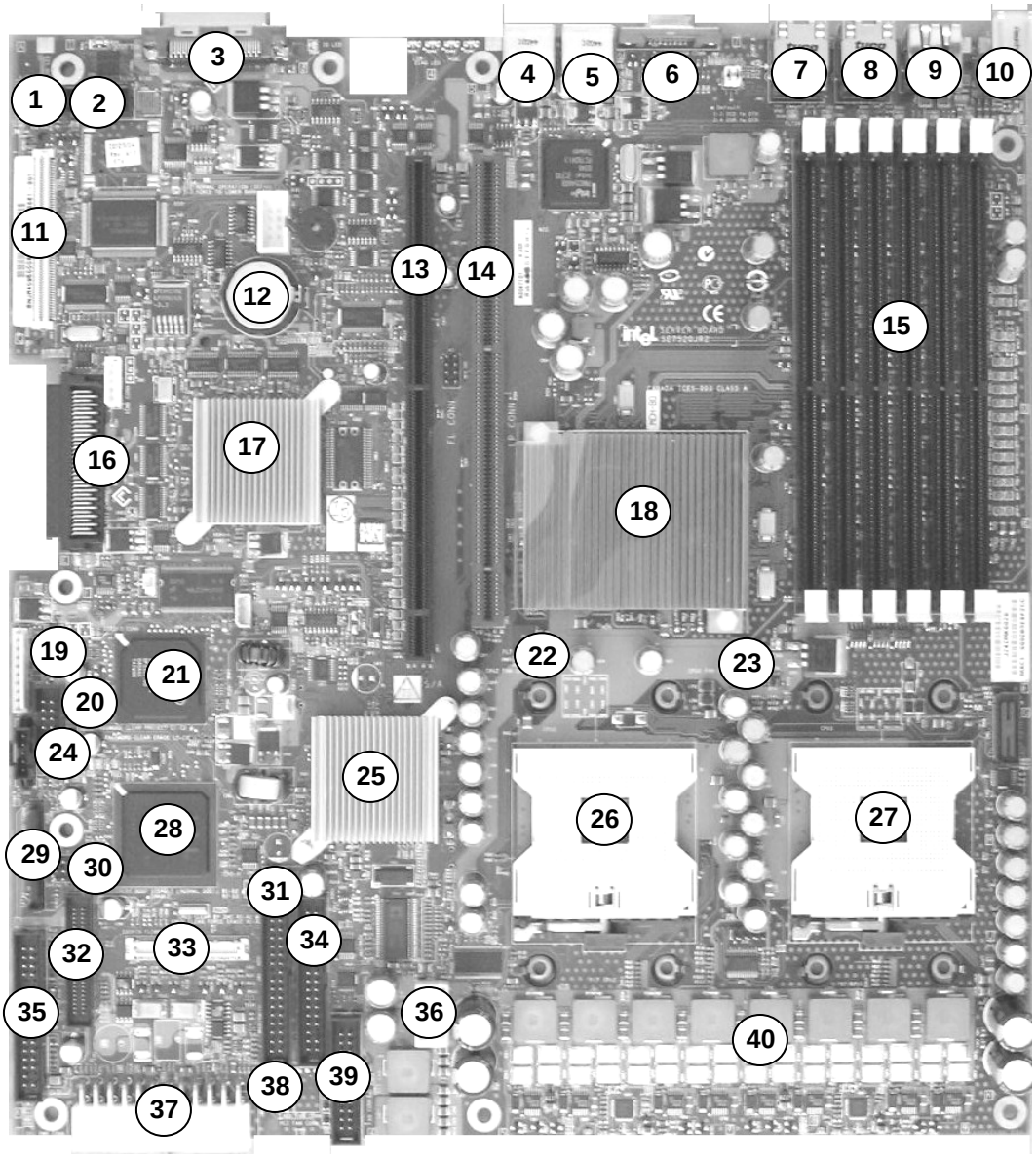


Figure 43. Intel® Server Board SE7520JR2 Layout

Table 55. Baseboard Layout Reference

Ref #	Description	Ref #	Description
1	(J1A1) 2-Pin Chassis Intrusion Header (J1A2) 2-Pin Hard Drive Act LED Header (J1A4) Rolling BIOS Jumper	22	CPU #2 Fan Header
2	10-Pin DH10 Serial A Header	23	CPU #1 Fan Header
3	Ext SCSI Channel B Connector	24	5-pin Power Sense Header
4	USB Port 2	25	PXH – Chipset Component
5	USB Port 1	26	CPU #2 Socket
6	Video Connector	27	CPU #1 Socket
7	NIC #2	28	ICH5-R – Chipset Component
8	NIC #1	29	SATA/SAS Ports
9	RJ-45 Serial B Port	30	(J1H2) Recovery Boot Jumper (J1H3) Password Clear Jumper (J1H4) CMOS Clear Jumper
10	Stacked PS/2 Keyboard and Mouse Ports	31	Legacy ATA-100 connector
11	Intel Management Module Connector	32	50-pin Control Panel Header
12	CMOS Battery	33	100-pin Control Panel, Floppy, IDE Connector
13	Full Height Riser Card Slot	34	Legacy Floppy Connector
14	Low Profile Riser Card Slot	35	SSI 34-pin Control Panel Header
15	DIMM Slots	36	8-Pin AUX Power Connector
16	68-pin SCSI Channel A Connector	37	24-Pin Main Power Connector
17	LSI 53C1030 SCSI Controller	38	SSI System Fan Header
18	MCH – Chipset Component	39	SR1450/SR2400 System Fan Header
19	1x10 USB Header	40	Processor Voltage Regulator Circuitry
20	2x5 USB Header		
21	ATI* RageXL Video Controller		

9. Regulatory, Environmentals, and Specifications

9.1 Product Regulatory Compliance

9.1.1 Product Safety Compliance

The Server Chassis SR1450 complies with the following safety requirements:

- UL60950 – CSA 60950(USA / Canada)
- EN60950 (Europe)
- IEC60950 (International)
- CB Certificate & Report, IEC60950 (report to include all country national deviations)
- GS License (Germany)
- GOST R 50377-92 - License (Russia)
- Belarus License (Belarus)
- Ukraine License (Ukraine)
- CE - Low Voltage Directive 73/23/EEE (Europe)
- IRAM Certification (Argentina)
- GB4943- CNCA Certification (China)

9.1.2 Product EMC Compliance

The Server Chassis SR1450 has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations when installed in a compatible Intel® host system. For information on compatible host system(s), refer to Intel's Server Builder website or contact your local Intel representative.

- FCC /ICES-003 - Emissions (USA/Canada) Verification
- CISPR 22 – Emissions (International)
- EN55022 - Emissions (Europe)
- EN55024 - Immunity (Europe)
- EN61000-3-2 - Harmonics (Europe)
- EN61000-3-3 - Voltage Flicker (Europe)
- CE – EMC Directive 89/336/EEC (Europe)
- VCCI Emissions (Japan)
- AS/NZS 3548 Emissions (Australia / New Zealand)
- BSMI CNS13438 Emissions (Taiwan)
- GOST R 29216-91 Emissions (Russia)
- GOST R 50628-95 Immunity (Russia)
- Belarus License (Belarus)
- Ukraine License (Ukraine)
  RRL MIC Notice No. 1997-41 (EMC) & 1997-42 (EMI) (Korea)
- GB 9254 - CNCA Certification (China)
- GB 17625 - (Harmonics) CNCA Certification (China)

9.1.3 Product Certifications / Registrations / Declarations

- UL Certification (US/Canada)
- CE Declaration of Conformity (CENELEC Europe)
- FCC/ICES-003 Class A Attestation (USA/Canada)
- VCCI Certification (Japan)
- C-Tick Declaration of Conformity (Australia)
- MED Declaration of Conformity (New Zealand)
- BSMI Certification (Taiwan)
- GOST R Certification / License (Russia)
- Belarus Certification / License (Belarus)
- RRL Certification (Korea)
- IRAM Certification (Argentina)
- CNCA Certification (China)
- Ecology Declaration (International)

9.1.4 Product Regulatory Compliance Markings

This product is provided with the following Product Certification Markings.

Regulatory Compliance	Country	Marking
cULus Listing Marks	USA/Canada	
GS Mark	Germany	
CE Mark	Europe	
FCC Marking (Class A)	USA	This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation. Manufactured by Intel Corporation
EMC Marking (Class A)	Canada	CANADA ICES-003 CLASS A CANADA NMB-003 CLASSE A
C-Tick Mark	Australia / New Zealand	
VCCI Marking (Class A)	Japan	この装置は、クラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。VCCI-A
BSMI Certification Number & Class A Warning	Taiwan	

		警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策
GOST R Marking	Russia	
RRL MIC Mark	Korea	
China Compulsory Certification Mark	China	

9.2 Electromagnetic Compatibility Notices

9.2.1 USA

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals, that are not shielded and grounded may result in interference to radio and TV reception.

9.2.2 FCC Verification Statement

Product Type: Intel® Server chassis SR1450; Intel® Server Board SE7520JR2
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124-6497
Phone: 1 (800)-INTEL4U or 1 (800) 628-8686

9.2.3 ICES-003 (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: “Appareils Numériques”, NMB-003 édictée par le Ministre Canadian des Communications.

(English translation of the notice above) This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled “Digital Apparatus,” ICES-003 of the Canadian Department of Communications.

9.2.4 Europe (CE Declaration of Conformity)

This product has been tested in accordance to, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

9.2.5 Japan EMC Compatibility

Electromagnetic Compatibility Notices (International)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:

This is a Class A product based on the standard of the Voluntary Control Council For Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

9.2.6 BSMI (Taiwan)

The BSMI Certification number and the following warning is located on the product safety label which is located on the bottom side (pedestal orientation) or side (rack mount configuration).

警告使用者：

這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策。

9.2.7 Korean RRL Compliance

1. 기기의 명칭(모델명) :
2. 인증번호 :
3. 인증받은 자의 상호 :
4. 제조년월일:
5. 제조자/제조국가 :

English translation of the notice above:

1. Type of Equipment (Model Name): On License and Product
2. Certification No.: On RRL certificate. Obtain certificate from local Intel representative
3. Name of Certification Recipient: Intel Corporation
4. Date of Manufacturer: Refer to date code on product
5. Manufacturer/Nation: Intel Corporation/Refer to country of origin marked on product

9.3 Replacing the Back up Battery

The lithium battery on the server board powers the real time clock (RTC) for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

ADVARSEL!

Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

ADVARSEL

Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

9.4 System Level Environmental Limits

The following table defines the system level operating and non-operating environmental limits (Office or Computer room Environment).

Table 56. Environmental Limits Summary

Parameter	Limits
Operating Temperature	+10°C to +35°C with the maximum rate of change not to exceed 10°C per hour
Non-Operating Temperature	-40°C to +70°C
Non-Operating Humidity	90%, non-condensing @ 35°C
Acoustic noise	Sound Pressure: 55 dBA (Rackmount) in an idle state at typical office ambient temperature. (23 +/- degrees C) Sound Power: 7.0 BA in an idle state at typical office ambient temperature. (23 +/- 2 degrees C)
Shock, operating	Half sine, 2 g peak, 11 mSec
Shock, unpackaged	Trapezoidal, 25 g, velocity change 136 inches/sec (□40 lbs to > 80 lbs)
Shock, packaged	Non-palletized free fall in height 24 inches (40 lbs to > 80 lbs)
Vibration, unpackaged	5 Hz to 500 Hz, 2.20 g RMS random
Shock, operating	Half sine, 2 g peak, 11 mSec
ESD	+/-15kV except I/O port +/-8KV per Intel Environmental test specification
System Cooling Requirement in BTU/Hr	2322 BTU/hour (Based on 520W maximum power, 78% power subsystem efficiency, and 98% power factory correction loss)

9.5 Serviceability

The system is designed to be serviced by qualified technical personnel only.

The desired Mean Time To Repair (MTTR) of the system is 30 minutes, including diagnosis of the system problem. To meet this goal, the system enclosure and hardware have been designed to minimize the MTTR.

Following are the maximum times that a trained field service technician should take to perform the listed system maintenance procedures, after diagnosis of the system.

Table 57. Mean Time To Repair Estimate

Activity	Time Estimate
Remove cover	10 sec
Remove and replace hard disk drive	3 min[1]
Remove and replace power supply module	10 sec
Remove and replace power distribution board	5 min
Remove and replace system fan	2 min
Remove and replace backplane board	5 min
Remove and replace front panel board	5 min
Remove and replace baseboard	10 min

[1] Includes swapping drive from drive bay

9.6 Regulated Specified Components

To maintain the UL listing and compliance to other regulatory certifications and/or declarations, the following regulated components must be used and conditions adhered to. Interchanging or use of other components will void the UL listing and other product certifications and approvals.

- **Server Chassis** (base chassis is provided with power supply and fans) - UL listed.
- **Server board** - must use an Intel server board—UL recognized.
- **Add-in boards** - must have a printed wiring board flammability rating of minimum UL94V-1. Add-in boards containing external power connectors and/or lithium batteries must be UL recognized or UL listed. Any add-in board containing modem telecommunication circuitry must be UL listed. In addition, the modem must have the appropriate telecommunications, safety, and EMC approvals for the region in which it is sold.

Peripheral Storage Devices—must be UL recognized or UL listed accessory and TUV or VDE licensed. Maximum power rating of any one device is 19 watts. Total server configuration is not to exceed the maximum loading conditions of the power supply.

Appendix A: Intel® Server Chassis SR1450 Integration and Usage Tips

This section provides a list of useful information that is unique to the Server Chassis SR1450 and should be kept in mind when integrating and configuring an Intel® Server Board SE7520JR2.

- Only low-profile (1.2 in or 30.48 mm) DIMMs can be used in the Server Chassis SR1450.
- Processor fans are not supported and are not needed in the server chassis SR1450. The system fan modules and power supply fans provide the necessary cooling needed for the system. Using a processor fan in this chassis may cause server management to incorrectly monitor the system fans.
- The CPU Air duct and Air Baffle must be used to maintain system thermals.
- The air dam on the CPU air duct must be in place for single processor configurations. Once the air dam is removed, it cannot be re-installed.
- To maintain system thermals, all hard drive bays must be populated with either a hard drive or drive blank.
- System fans are not hot swappable
- The Intel® Local Control Panel can only be used with systems configured with an Intel® Management Module.
- Use of the shipping screw found on the front edge of the top cover is optional.
- To improve system EMI levels, shielded LAN cables must be used.
- A conversion kit is available to have concurrent support for both a slim-line optical drive and slim-line floppy drive. The kit allows a slim-line floppy drive assembly to be inserted in the center hard drive bay. The conversion kit has the following product order code: AXXFLOPHDDTRAY.
- The FRUSDR utility must be run to load the proper Sensor Data Records for the Server Chassis SR1450 on the server board.
- Make sure the latest system software is loaded on the server. This includes system BIOS, FRUSDR, BMC firmware, and Hot Swap Controller firmware. The latest system software can be downloaded from

  http://support.intel.com/support/motherboards/server/se7520jr2/

Glossary

Word / Acronym	Definition
ACA	Australian Communication Authority
ANSI	American National Standards Institute
BMC	Baseboard Management Controller
CMOS	Complementary Metal Oxide Silicon
D2D	DC-to-DC
EMP	Emergency Management Port
FP	Front Panel
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
IMM	Intel Management Module
ISM	Intel Server Management
LCD	Liquid Crystal Display
LCP	Local Control Panel
LPC	Low-Pin Count
mBMC	Mini-Baseboard Management Controller
MTBF	Mean Time Between Failure
MTTR	Mean Time to Repair
OTP	Over Temperature Protection
OVP	Over Voltage Protection
PDB	Power Distribution Board
PFC	Power Factor Correction
PSU	Power Supply Unit
RI	Ring Indicate
SCA	Single Connector Attachment
SDR	Sensor Data Record
SE	Single-Ended
THD	Total Harmonic Distortion
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VCCI	Voluntary Control Council for Interference