



# **Guide to Interpreting System Event Log (SEL) Messages**

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## *Revision History*

<b>Date</b>	<b>Rev</b>	<b>Modifications</b>
10/5/1999	0.10	Used Revision 0.40 of the ISC SEL document as basis for generating SEL document that is not based on one specific viewer
1/26/00	0.20	Added / verified existing S820PN2 information. Corrected Event Generator ID information
6/12/00	0.30	Removed reference to non-shipping server systems

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# 1 Introduction

This document is provided as a reference to the System Event Log (SEL) information displayed by the SEL viewer in Intel® Server Control (ISC), the Emergency Management Console (EMP), or the System Setup Utility (SSU).

This document begins with a description of the internal workings of the System Event Log and follows with descriptions of the fields as they may be seen in the SEL viewer.

## 1.1 Document Organization

This document is primarily composed of tables of possible SEL data, broken down into base components of the data: the event generator, the source of the event, and a description of the event that generated the event entry.

- **Section 1** contains an introduction to the SEL.
- **Section 2** contains a brief introduction to EMP & the EMP Console.
- **Section 3** contains a brief introduction to ISC & the ISC Console.
- **Section 4** contains a brief introduction to the SSU & the SEL Manager Add-in.
- **Section 5** contains a view of SEL information as it is seen in the SEL viewer.
- **Appendices**, alphabetized by platform, contain tables of SEL information.

## 1.2 SEL Overview

The System Event Log (SEL) is a non-volatile repository for Event Messages. Event Messages contain information about system events and anomalies that occur on the server. They can be triggered by BIOS, Event Generators, or Sensors. Some Event Messages are the result of normal happenings, such as a normal server boot, or possible minor problems, like a disconnected keyboard. Other events may indicate security breaches, such as when the chassis cover is removed, or internal failures, like a component overheat condition.

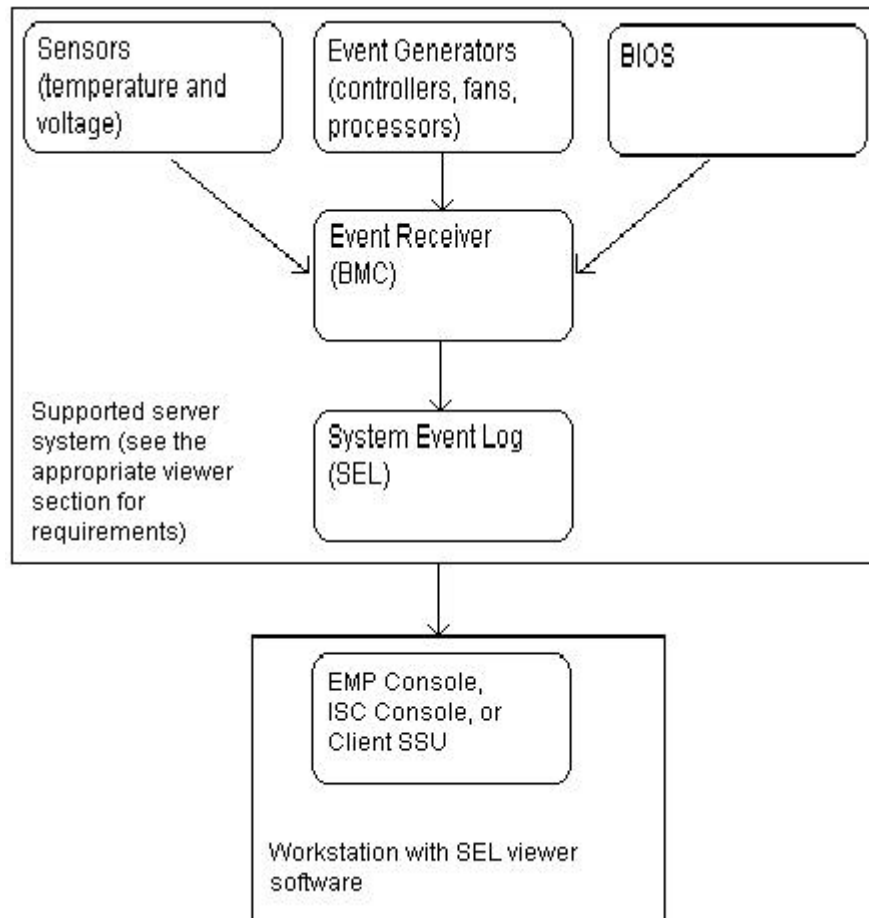
Where appropriate, thresholds, or ranges of acceptable values, exist. As with the other system events, if at any time a parameter crosses one of these defined thresholds, an Event Message is generated.

**Note:** Thresholds can be defined through ISC, but not through EMP or SSU.

Regardless of the event (from system boot to critical failure), the appropriate management controller generates the Event Message. Event Messages are passed to the Baseboard Management Controller (BMC), the primary management controller on the Intel server systems. The BMC passes the Event Message to the System Event Log (SEL) where it becomes available for querying by a SEL Viewer utility.

The SEL Viewer provides an interface for the server administrator to view information in the SEL. A SEL Viewer is available through the Emergency Management Port (EMP) Console, Intel Server Control (ISC), or the System Setup Utility (SSU). The same information is available through each of the interfaces. The administrator can use this information to monitor the server for both warnings, such as when the chassis door on a server has been opened, or for potential critical problems, such as when a processor has failed or a temperature threshold has been crossed.

The following diagram provides an outline of the Event Message flow from the source of the event to the SEL Viewer. The elements pictured in Figure 1-1 are described in the following sections.



**Figure 1-1: Event Message Flow**



## 1.2.1 Sensors

Server system boards that are supported by IPMI contain sensors to monitor system environmental conditions. Some sensors, such as temperature and voltage sensors, are configured with default high and / or low thresholds. Where prudent, these thresholds can be adjusted to fit the needs of the user. Other sensors monitor events like chassis intrusion and secure mode violation.

**Note:** Thresholds can be defined through ISC, but not through EMP or SSU.

## 1.2.2 Event Generator

Event Generators include devices such as the fans, processors, hard drives, and the BMC. Events that are detected by a microcontroller or the BIOS cause an Event Message to be sent to the BMC to be recorded into the SEL. The BMC can be both an Event Generator and an Event Receiver. This means that while the BMC is responsible for recording Event Messages, it can also be the initiator of an event message.

## 1.2.3 Event Receiver (BMC)

The BMC is the Event Receiver. It manages the SEL, determines the source of event messages, and formats them for the SEL.

## 1.2.4 BIOS

The system BIOS (Basic I/O System) firmware serves many important roles in platform management. The BIOS loads and initializes the system management hardware interfaces so that these interfaces can be later accessed by System Management Software and the Operating System. The BIOS works with the system hardware and management controllers during POST to implement checks of the system and management hardware.

Event messages generated from the BIOS and during POST are formatted differently than event messages generated from the controllers. Therefore, in this document, the SEL messages that are generated from the BIOS and POST are found in separate tables from the messages generated by the controllers. The tables are all located in the appendices.

## 1.2.5 System Event Log (SEL)

The System Event Log (SEL) is the repository for the Event Messages. The System Event Log is implemented as non-volatile storage to ensure that critical events can be retrieved for 'post-mortem analysis' should a system failure occur.

## 2 About EMP & the EMP Console

The Emergency Management Port (EMP) is a server management feature that supports remote system management through either a modem or a serial line connection between the console workstation and the COM2 Port on the server.

EMP provides the ability to view the SEL, the Sensor Data Records (SDR), and the Field Replaceable Unit (FRU) information at the server. It also provides the user with the ability to power the server up or down, or reset the server through the serial connection or modem connection. The EMP features, including the SEL viewer, are available regardless of whether the server system is up and running, is powered down, is in a pre-boot stage, or if the operating system is hung.

The EMP Console is the software installed at a workstation that communicates to the EMP features at the server. The Console software provides a graphical user interface to connect to the server and use the above features. The SEL information can be viewed in either verbose or hexadecimal modes. The viewer looks like this when viewed from the EMP Console in hexadecimal mode:

Rec. ID	Event Type	Time Stamp	Generator ID	Emv Rev	Sensor Type and Number	Event Description
5003	02	36c1a28d	0020	02	02 07	06 01 ff ff
6003	02	36c1a28d	0020	02	02 08	06 01 ff ff
7003	02	36c1a28e	0020	02	04 22	06 01 ff ff
8003	02	36c1a299	0020	02	04 21	06 01 ff ff
9003	02	36c1a2a0	0020	02	04 22	06 01 ff ff
a003	02	36c1a2b6	0020	02	04 21	06 01 ff ff
b003	02	36c1a2b7	0020	02	04 22	06 01 ff ff
c003	02	36c1a2b9	0011	02	12 ef	e7 01 ff ff
d003	02	36c1a2c1	0020	02	04 21	06 01 ff ff
e003	02	36c1a2d9	0020	02	04 21	06 01 ff ff
f003	02	36c1a2da	0020	02	04 22	06 01 ff ff
0004	02	36c1a2ec	0020	02	04 22	06 01 ff ff
1004	02	36c1a2f6	0020	02	04 21	06 01 ff ff
2004	02	36c1a30f	0020	02	04 22	06 01 ff ff
3004	02	36c21397	0020	02	04 22	06 01 ff ff
4004	02	36c2139b	0020	02	04 21	06 01 ff ff
5004	02	36c213a8	0020	02	04 22	06 01 ff ff
6004	02	36c213b2	0020	02	04 21	06 01 ff ff
7004	02	36c213b4	0020	02	04 22	06 01 ff ff
8004	02	36c213be	0020	02	04 21	06 01 ff ff
9004	02	36c213bf	0020	02	04 22	06 01 ff ff
a004	02	36c213d0	0020	02	04 21	06 01 ff ff
b004	02	36c213d1	0020	02	04 22	06 01 ff ff
c004	02	36c213db	0020	02	04 21	06 01 ff ff
d004	02	36c213e7	0020	02	04 21	06 01 ff ff

SERVER NAME:      LINE: Direct      MODE: EMP      LINE STATUS: Connected

**Figure 2-1: SEL Viewer in EMP Console**

## 2.1 Viewing SEL Data from the EMP Console

The EMP Console provides a user interface to the SEL. Seven columns of SEL data can be viewed from the EMP Console (see Figure 2-1: SEL Viewer in EMP Console):

- Record ID
- Record Type
- Time Stamp
- Generator ID
- Emv Rev
- Sensor Type and Number
- Event Description

**Note:** When the EMP Console is used as the SEL Viewer, the Generator ID bytes need to be reversed to determine the correct Generator from the tables from the Appendices. In other words, If the Generator ID displays in the EMP Console as 0020, it will display as 20 00 in the tables.

Section 5, Interpreting SEL Data, discusses the definitions of these fields and how they may be translated.

---

## 3 About ISC and the ISC Console

Intel® Server Control (ISC) is a server-management tool that uses the Desktop Management Interface (DMI) 2.0 framework to manage server hardware components. ISC provides real-time monitoring and alerting for server hardware sensors and it provides the system administrator with the ability to:

- Remotely monitor server hardware sensors
- Configure sensor thresholds
- Configure, receive, and act upon alert events
- Configure options to shut down, reboot, or power-off a server system automatically

The ISC Console software displays the DMI information through a Graphical User Interface (GUI) that can be easily read and understood. Through the GUI, a variety of instrumentation settings can be fine-tuned to match environmental needs.

An ISC user is able to track system status and manage hardware conditions such as:

- Temperature
- Voltage
- Cooling fan status
- Chassis intrusion
- ECC memory
- Processor status
- Power supply status

Where appropriate, thresholds or ranges of acceptable values exist. Other sensors, such as the chassis intrusion sensors, detect when the cover to the chassis has been opened. Any time a parameter crosses a defined threshold or a sensor detects an occurrence, such as the chassis cover being opened, an event occurs. These events are logged to the SEL (System Event Log).

The SEL viewer looks like the figure on the following page when viewed from ISC:

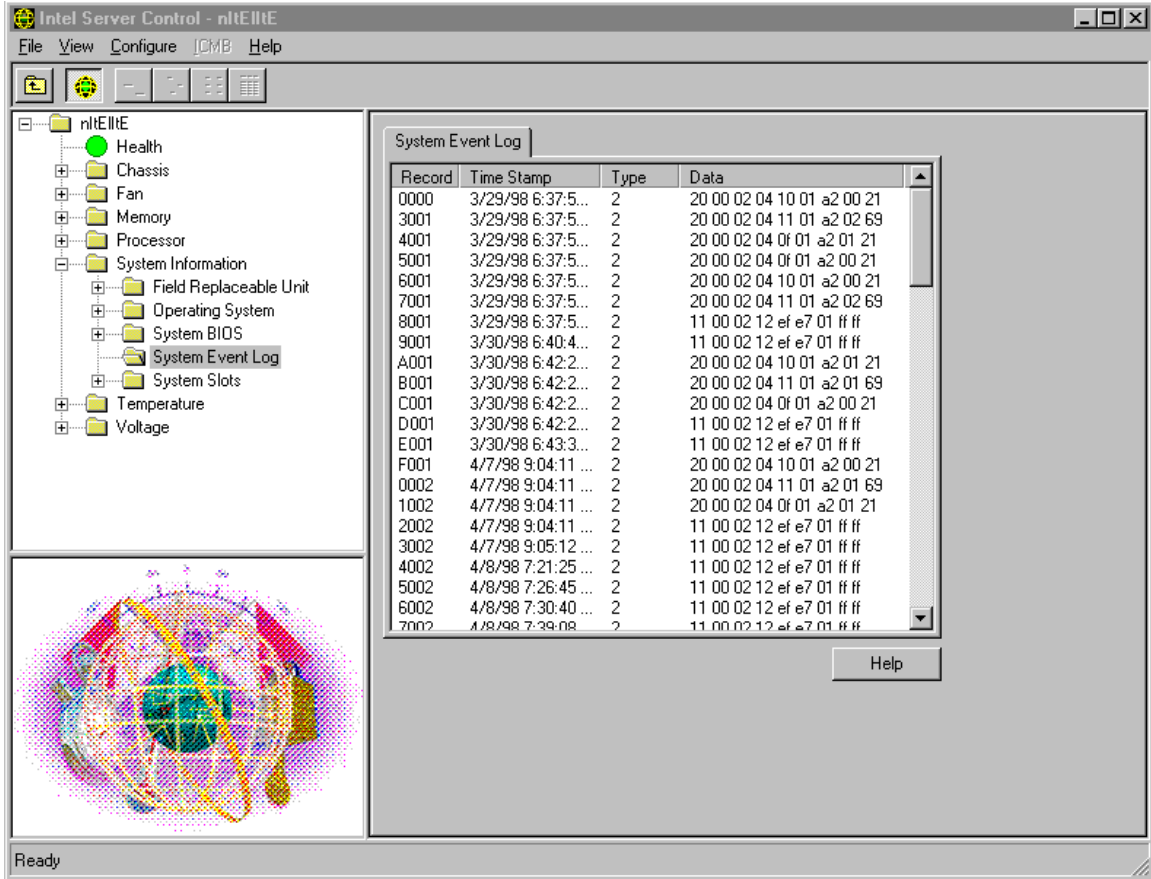


Figure 3-1: SEL Viewer in ISC

### 3.1 Viewing SEL Data from ISC

ISC provides a user interface to the SEL. Four columns of SEL data can be viewed from ISC (see Figure 3-1: SEL Viewer in ISC):

- **Record:** A unique identifying number. Each event is logged with a record number. The record number itself does not contain data that is useful for translating the SEL data.
- **Time Stamp:** The date and time at which the event occurred.
- **Type:** The Type field will always contain “2.” This field is for future use.
- **Data:** The SEL Data column in ISC contains information about the source and description of the event that generated the entry into the SEL. The Data column contains nine bytes of information, broken out as follows:

**Table 3-1: Data Column**

Data Field	Number of Bytes	Description
Generator Id	2	Identifies the device that generated the Event Message. See the Appendix for platform-specific Generator IDs.
EmvRev	1	Identifies revisions of the Event Message format. Currently holds the value of "#02". This field is for future use and is therefore not used in translating SEL data.
Sensor Type	1	Indicates the event class or type of sensor that generated the Event Message. A POST error uses Sensor Type 0F. A BIOS error uses Sensor Type 12, 13, or 0C with Sensor Number EF. See the Appendix for platform-specific Sensor Types.
Sensor Number	1	A unique number within a given sensor type to represent the sensor within the management controller that generated the Event Message. Sensor numbers are used for both identification and access of sensor information, such as getting and setting sensor thresholds. A BIOS error uses Sensor Number EF with Sensor Type 12, 13, or 0C. See the Appendix for platform-specific Sensor Numbers.
Event Description	4	For events generated from the BMC, FPC, or HSC, the first byte of the Event Description indicates the type of event that occurred, such as threshold crossed or device added/removed. Other bytes may be disregarded for identifying the Event Message. For events generated from the BIOS or from POST, as indicated by the Sensor Type and/or Sensor Number, the Event Description provides additional information about the Event Message. See the Appendix for platform-specific Event Descriptions.

When viewing SEL data from ISC, it is necessary to break apart the bytes in the data column into the data field components indicated in Table 3-1. The "Number of Bytes" column in Table 3-1 is used to determine where the component divisions need to be. These separate components are then used with the tables in the Appendix to translate the data.

For example, if the Data column in the ISC SEL viewer contains `20 00 02 04 10 01 a2 00 21`, the string of bytes is divided into:

Generator ID (2 bytes)	EmvRev (1 byte)	Sensor Type (1 byte)	Sensor Number (1 byte)	Event Description (4 bytes)
20 00	02	04	10	01 a2 00 21

If the Data column contains `11 00 02 0F 4B 01 a2 31 01`, the string of bytes is divided into:

Generator ID (2 bytes)	EmvRev (1 byte)	Sensor Type (1 byte)	Sensor Number (1 byte)	Event Description (4 bytes)
11 00	02	0F	4B	01 a2 31 01

## 4 About the SSU and the SEL Manager Add-in

The System Setup Utility (SSU) is a DOS server management utility that supports local and remote system configuration through either a modem or a network connection.

In addition to providing the ability to configure the BIOS and hardware devices on the server system, the SSU provides the ability to view the SEL, the Sensor Data Records (SDR), and the Field Replaceable Unit (FRU) information at the server. As with the EMP and ISC SEL Viewers, the SEL Manger in the SSU provides services to allow users to view the system event log that is stored on the server. The SSU add-in SEL Manager provides support for the user to perform the following:

- Examine all system event log entries that are stored in the non-volatile storage area of the server.
- Examine system event log entries from a previously stored file.
- Save the system event log entries to a file.
- Clear the system event log entries from the non-volatile storage area.

The SSU cannot be run from a DOS box in Windows\*

The SEL viewer looks similar to the following screen shot when it viewed from the SSU: Note that because this is a DOS application, the fields cannot be resized. Therefore, this screen view does not display all possible fields. In addition, the order in which the fields are displayed may vary, depending on the version of SSU run on your system.

The screenshot shows a window titled "SEL Manager" with a menu bar containing "File", "SEL", and "Help". Below the menu bar is a table with three columns: "Num", "Time Stamp", "Sensor Type & Number", and "Event Description". The table contains 12 rows of data. The first 9 rows have "Pre-Init Time Stamp" in the Time Stamp column and "Performance Lags" in the Event Description column. The 10th row has a date and time "07/08/1999 - 15:55:02" in the Time Stamp column and "OEM System Boot Event" in the Event Description column. The 11th and 12th rows have "07/08/1999 - 15:55:12" and "07/08/1999 - 15:55:34" in the Time Stamp column, respectively, and "Performance Lags" in the Event Description column.

Num	Time Stamp	Sensor Type & Number	Event Description
1	Pre-Init Time Stamp	Physical Security (Chass	State Asserted
2	Pre-Init Time Stamp	Voltage #16	Performance Lags
3	Pre-Init Time Stamp	Fan #34	Performance Lags
4	Pre-Init Time Stamp	Fan #36	Performance Lags
5	Pre-Init Time Stamp	Fan #37	Performance Lags
6	Pre-Init Time Stamp	Fan #38	Performance Lags
7	Pre-Init Time Stamp	Fan #39	Performance Lags
8	Pre-Init Time Stamp	Fan #34	Performance Lags
9	Pre-Init Time Stamp	Fan #34	Performance Lags
10	07/08/1999 - 15:55:02	System Event #EF	OEM System Boot Event
11	07/08/1999 - 15:55:12	Fan #34	Performance Lags
12	07/08/1999 - 15:55:34	Fan #34	Performance Lags

Figure 4-1: SEL Viewer in SSU

## Guide to Interpreting System Event Log (SEL) Messages

Seven columns of SEL data can be viewed from the SSU:

- Record ID (or Num, depending on the version of SSU)
- Record Type
- Time Stamp
- Generator ID
- Emv Rev
- Sensor Type and Number
- Event Description

Section 5, Interpreting SEL Data, discusses the definitions of these fields and how they may be translated.



## 5 Interpreting SEL Data

This section provides examples of SEL data translations. The SEL data can be obtained from EMP, ISC, or SSU.

For SEL data obtained from ISC, the Data column must first be divided into individual components as indicated in Section 3.1, Viewing SEL Data from ISC, and as also indicated in the examples below. For SEL data obtained from the EMP Console or from the SSU, data divisions are necessary only to divide the Sensor Type and the Sensor Number.

For SEL data obtained from the EMP Console, the Generator ID bytes need to be reversed, as described in Section 2.1.

The following table provides an overall description of the data that is provided by each field of information from the SEL Viewer. Refer back to this information when using the examples.

**Table 5-1: SEL Data Fields**

Data Field	Number of Bytes	Description
Generator Id	2	Identifies the device that generated the Event Message. See the Appendix for platform-specific Generator IDs.
EmvRev	1	Identifies revisions of the Event Message format. Currently holds the value of "#02". This field is for future use and is therefore not used in translating SEL data.
Sensor Type	1	Indicates the event class or type of sensor that generated the Event Message. A POST error uses Sensor Type 0F. A BIOS error uses Sensor Type 12, 13, or 0C with Sensor Number EF. See the Appendix for platform-specific Sensor Types.
Sensor Number	1	A unique number within a given sensor type to represent the sensor within the management controller that generated the Event Message. Sensor numbers are used for both identification and access of sensor information, such as getting and setting sensor thresholds. A BIOS error uses Sensor Number EF with Sensor Type 12, 13, or 0C. See the Appendix for platform-specific Sensor Numbers.
Event Description	4	For events generated from the BMC, FPC, or HSC, the first byte of the Event Description indicates the type of event that occurred, such as threshold crossed or device added/removed. Other bytes may be disregarded for identifying the Event Message. For events generated from the BIOS or from POST, as indicated by the Sensor Type and/or Sensor Number, the Event Description provides additional information about the Event Message. See the Appendix for platform-specific Event Descriptions.

## 5.1 Example 1: Event Message Generated from a Controller

If the Data column in ISC contains 20 00 02 04 12 01 A2 00 21, the string of bytes needs to first be divided as indicated in the following table. The “Number of Bytes” column in Table 5-1 indicates the number of bytes that are used for each field.

**Table 5-2: Example 1 Event Message**

Generator ID (2 bytes)	EmvRev (1 byte)	Sensor Type (1 byte)	Sensor Number (1 byte)	Event Description (4 bytes)
20 00	02	04	12	01 A2 00 21

**Note:** This example uses data from the AD450NX platform. Therefore, the data translations are taken from **Appendix B: AD450NX Tables**.

- **Generator ID**

Table B.1 in the Appendix indicates that the above Example 1 Event Message was generated by the BMC:

**Excerpt from Table B.1: AD450NX Generator ID Codes**

Generator ID	Description
20 00	BMC

- **EmvRev**

The EmvRev field is reserved for future use and is therefore not applicable.

- **Sensor Type**

The Sensor Type field in Table B.2 in the Appendix is used to determine the description for Sensor Type 04 is “Fan.”

**Excerpt from Table B.2: AD450NX Sensor Codes**

Sensor Type	Sensor Number	Sensor Name
04		Fan

- **Sensor Number**

The Sensor Number field is used to locate the specific sensor within the Sensor Type. In this case, it has been determined by the Sensor Type that the event was triggered by a fan. The Sensor Number is then used to pinpoint the specific fan that caused the event.

Since the sample data indicates the Sensor Number is “12,” it is necessary to look for Sensor Number 12 beneath Sensor Type 04. In this case, the table is used to determine that the Event Message was generated from the Backplane Fan 5 speed sensor.

**Excerpt from Table B.2: AD450NX Sensor Codes**

Sensor Type	Sensor Number	Sensor Name
04		Fan
	0E	Fan 1 speed / Fan 7 speed
	0F	Fan 2 speed / Fan 8 speed
	10	Fan 3 speed / Fan 9 speed
	11	Fan 4 speed
	12	Fan 5 speed
	13	Fan 6 speed

- **Event Description**

As indicated in Table 5-1, if an event is generated from the BMC, FPC, or HSC, the Event Description field determines the type of event that occurred. The Event Message used for the sample data was generated from the BMC.

Using the first byte of the Event Description (01), Table B.3 specifies that a threshold has been crossed.

**Excerpt from Table B.3: AD450NX Event Description Codes**

Event Description	Event Type	Definition
01 — — —	N/A	Threshold crossed

## 5.2 Example 2: Event Message Generated from BIOS or from POST

If the Data column contains 11 00 02 0F 4B 01 A2 31 01, the string of bytes needs to first be divided as indicated in the following table. The “Number of Bytes” column in Table 5-1 indicates the number of bytes that are used for each field.

**Table 5-3: Example 2 Event Message**

Generator ID	EmvRev	Sensor Type	Sensor Number	Event Description
11 00	02	0F	4B	01 A2 31 01

**Note:** This example uses data from the AD450NX platform. Therefore, the data translations are taken from **Appendix B: AD450NX Tables**.

- **Generator ID**

Table B.1 in the Appendix indicates that the above Example 1 Event Message was generated by the BIOS:

**Excerpt from Table B.1**

Generator ID	Description
11 00	BIOS

- **EmvRev**

The EmvRev field is reserved for future use and is therefore not applicable.

- **Sensor Type**

The Sensor Type field in Table B.2 in the Appendix is used to determine the description for Sensor Type 0F is “POST.”

**Excerpt from Table B.2, displaying the Sensor Type**

Sensor Type	Sensor Number	Sensor Name
0F		POST Error

- **Sensor Number**

The Sensor Number field is used to locate the specific sensor within a Sensor Type that triggered the Event. Since the sample data indicates the Sensor Number is “4B,” Sensor Number 4B is located beneath Sensor Type 0F. In this case, 4B indicates the POST table needs to be used to pinpoint the specific cause of this Event Message.

**Excerpt from Table B.2, displaying the Sensor Number associated with Sensor Type 0F**

Sensor Type	Sensor Number	Sensor Name
0F		POST Error
	4B	See POST Table below

- **Event Description**

As stated in Table 5-1, “For events generated from the BIOS or from POST, as indicated by the Sensor Type and/or Sensor Number, the Event Description provides additional information about the Event Message.”

Therefore, the Event Description information is matched against data in the POST table to determine the cause of the Event

The POST and the BIOS Event Messages might not use all four bytes of the Event Description to further specify the source of the Event. The tables in the appendix use “— —” to indicate the bytes that are not used.

In the sample data, the Event Description is 01 A2 31 01. Table B.5 indicates the first two bytes are disregarded. 31 01 indicates a problem with Floppy Drive A:

**Excerpt from Table B.5 displaying a POST Event Description**

Event Description	Event Explanation
— — 31 01	Floppy Drive A:

## Appendix A AC450NX Tables

The tables in this Appendix provide translations for SEL viewer data on the AC450NX server platform. See Table 2 in Section 3 for a description of each field.

**Note:** Data is not provided for the EmvRev field. This field is reserved for future use and currently provides no valuable information.

### A.1 AC450NX Generator ID Codes

Generator ID	Description
11 00	BIOS
20 00	BMC
22 00	FPC
C0 00	HSC

### A.2 AC450NX Sensor Codes

Sensor Type	Sensor Number	Sensor Name
<b>01</b>		<b>Temperature</b>
	01	HSC Board Temp Sensor
	0A	PXB Temp Monitor
	16	CPU Baseboard Temp Sensor
	17	Processor 1 Temp Sensor
	18	Processor 2 Temp Sensor
	19	Processor 3 Temp Sensor
	1A	Processor 4 Temp Sensor
	1B	Memory Module 1 Temp Sensor
	1C	Memory Module 2 Temp Sensor
<b>02</b>		<b>Voltage</b>
	01	I/O Baseboard +3.3V
	02	I/O Baseboard +12V
	03	I/O Baseboard +5V
	04	Vcc_Stdbby
	05	I/O Baseboard -12V
	06	I/O Baseboard -5V
	07	I/O Baseboard SCA_VREF1 (SCSI A Term. 1)
	08	I/O Baseboard SCA_VREF2 (SCSI A Term. 2)
	09	I/O Baseboard SCA_VREF3 (SCSI A Term. 3)
	0B	VccP1
	0C	VccP2
	0D	VccP3
	0E	VccP4
0F	VTT (Processor +1.5V)	
10	Processor +2.5 V	
11	Processor +3.3V	
12	Processor +5V	

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Sensor Type	Sensor Number	Sensor Name
	13	Vcc_L2_1 (For Processor 1 & 2)
	14	Vcc_L2_2 (For Processor 3 & 4)
	15	Processor +12V
	21	Slot 1 VID
	22	Slot 2 VID
	23	Slot 3 VID
	24	Slot 4 VID
	25	L2 1 VID
	26	L2 2 VID
	27	L2 3 VID
	28	L2 4 VID
	50	I/O Baseboard SCB_VREF1 (SCSI B Term. 1)
	51	I/O Baseboard SCB_VREF2 (SCSI B Term. 2)
	52	I/O Baseboard SCB_VREF3 (SCSI B Term. 3)
<b>04</b>		<b>Fan</b>
	0C	Fan 1 speed
	0D	Fan 2 speed
	0E	Fan 3 speed
	0F	Fan 4 speed
	10	Fan 5 speed
	11	Fan 6 speed
<b>06</b>		<b>Secure Mode Violation Attempt</b>
	01	Power Button Secure Mode Violation
	02	Reset Button Secure Mode Violation
<b>07</b>		<b>Processor</b>
	1D	Processor 1 Status
	1E	Processor 2 Status
	1F	Processor 3 Status
	20	Processor 4 Status
<b>08</b>		<b>Power Supply</b>
	06	Power Supply 1
	07	Power Supply 2
	08	Power Supply 3
<b>09</b>		<b>Power Unit</b>
	05	Power Unit Status

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<b>0C</b>		<b>Memory</b>
	29	DIMM1 Presence Memory Module 1
	2A	DIMM2 Presence Memory Module 1
	2B	DIMM3 Presence Memory Module 1
	2C	DIMM4 Presence Memory Module 1
	2D	DIMM5 Presence Memory Module 1
	2E	DIMM6 Presence Memory Module 1
	2F	DIMM7 Presence Memory Module 1
	30	DIMM8 Presence Memory Module 1
	31	DIMM9 Presence Memory Module 1
	32	DIMM10 Presence Memory Module 1
	33	DIMM11 Presence Memory Module 1
	34	DIMM12 Presence Memory Module 1
	35	DIMM13 Presence Memory Module 1
	36	DIMM14 Presence Memory Module 1
	37	DIMM15 Presence Memory Module 1
	38	DIMM16 Presence Memory Module 1
	39	DIMM1 Presence Memory Module 2
	3A	DIMM2 Presence Memory Module 2
	3B	DIMM3 Presence Memory Module 2
	3C	DIMM4 Presence Memory Module 2
	3D	DIMM5 Presence Memory Module 2
	3E	DIMM6 Presence Memory Module 2
	3F	DIMM7 Presence Memory Module 2
	40	DIMM8 Presence Memory Module 2
	41	DIMM9 Presence Memory Module 2
	42	DIMM10 Presence Memory Module 2
	43	DIMM11 Presence Memory Module 2
44	DIMM12 Presence Memory Module 2	
45	DIMM13 Presence Memory Module 2	
46	DIMM14 Presence Memory Module 2	
47	DIMM15 Presence Memory Module 2	
48	DIMM16 Presence Memory Module 2	
	EF	See BIOS Table below
<b>0D</b>		<b>Drive Slot (Bay)</b>
	04	Drive Slot 0 Presence
	05	Drive Slot 1 Presence
<b>0F</b>		<b>POST Error</b>
	4B	See POST Table below
<b>11</b>		<b>Watchdog</b>
	49	BMC Watchdog
<b>12</b>		<b>System Event</b>
		EF
<b>13</b>		<b>Critical Interrupt</b>
	28	See BIOS Table below

Sensor Type	Sensor Number	Sensor Name
	29	See BIOS Table below
	4A	FP NMI
<b>21</b>		<b>PHP Slot</b>
	4C	PHP Slot 1
	4D	PHP Slot 2
	4E	PHP Slot 3
	4F	PHP Slot 4

### A.3 AC450NX Event Description Codes

The purpose of the Event Description field varies, depending on the Generator ID. When the Generator ID is

- 20 00
- 22 00
- C0 00

the first byte of the Event Description is used to indicate the type of event that occurred, such as the crossing of a threshold or the removal of a device.

When the Generator ID is 11 00, the Event Message was generated from the BIOS or from POST and Table A.4 or A.5 should be used to determine the definition of the Event Message. Refer to Section 3 for a complete explanation on table usage. Each “—” in the table below indicates a byte that may be disregarded.

Event Description	Event Type	Definition
01 — — — —	N/A	Threshold crossed
02 — — — —	N/A	Transition to idle, active, or busy
03 — — — —	N/A	State asserted or deasserted
04 — — — —	N/A	Predictive failure asserted or deasserted
05 — — — —	N/A	Limit exceeded
06 — — — —	N/A	Performance lag
07 — — — —	N/A	Presence, Disabled, IERR, Thermal Trip, or FRB3
08 — — — —	N/A	Device added or removed
09 — — — —	N/A	Device enabled or disabled
0A — — — —	N/A	Transition to running or test, on or off-line
EB — — — —	N/A	Redundancy lost, regained, degraded
E7 — — — —	07	Presence, Disabled, IERR, Thermal Trip, FRB3
E7 — — — —	08	Presence or fault
E7 — — — —	09	Power Off or Power Cycle, 240VA, Reserve, Lost AC
E7 — — — —	49	BIOS WD Reset, OS WD Reset, OS WD Shutdown, Power down, Power off



## A.4 AC450NX BIOS Codes

To decode a BIOS error message, locate the Sensor Type and Sensor Number under which the error falls. Then use the Event Description to identify the specific error. This table uses “— —” to indicate bytes which are not applicable to the purposes of this document.

Sensor Type	Sensor Number	Event Description	Event Explanation
0C	EF		
		07 02 FF FF	Memory parity error
		E7 20 board# DIMM#	Single bit memory error at runtime
		E7 21 board# DIMM#	Memory parity error at runtime
		E7 22 board# DIMM#	Single/multi bit memory error during POST
12	EF		
		E7 00 FF FF	System Reconfiguration
		E7 01 FF FF	System Boot
13	28		
		E7 00 FF FF	Front Panel NMI
		E7 01 FF FF	Bus time-out
		E7 02 FF FF	I/O check
		E7 03 FF FF	Software NMI
		E7 10 FF FF	AERR address parity error
		E7 11 FF FF	BERR host bus generic error
		E7 12 FF FF	BINIT host bus hard failure
		E7 13 bus# FF	BINIT protocol violation
		E7 14 bus# FF	BINIT expander parity error
		E7 15 FF FF	BINIT response parity error
		E7 16 FF FF	BINIT request parity error
		E7 17 Syndrome# FF	BINIT host bus ECC error
		E7 18 PXB device# FF	SERR protocol violation
		E7 19 PXB device# FF	SERR parity on transmit
		E7 20 PXB device# FF	SERR parity on receive
		E7 21 PXB device# FF	SERR parity on address error
		E7 22 PXB device# FF	SERR inbound timeout
		E7 23 PXB device# FF	SERR bus parity
		E7 24 PXB device# FF	PCI PERR
E7 25 PXB device# FF	PCI SERR		
E7 26 PXB device# FF	PCI data parity error		
E7 60 IPMB CMD#	IPMB protocol error		

**Note:**

Most of events coming from the system chip set do not have sensor numbers and type codes associated with each event. EFh is specified as the system generic sensor and E7h in type code as system generic type code.

The BIOS will treat the above sensors as discrete sensors. The 4 bit offset field in the first event data byte (E7 XX) indicates the exact cause of error. The following 2 OEM data bytes are used to indicate the physical location of the error, such as the DIMM row number.

## A.5 AC450NX POST Codes

Event Description	Event Explanation
— — 00 08	PCI I/O Port Conflict
— — 00 09	NVRAM Checksum Error, NVRAM Cleared
— — 00 81	Processor 0 failed BIST
— — 00 82	Baseboard Management Controller failed to function
— — 00 84	Switch fault on hot-plug PCI slot Pn
— — 01 05	PCI System Error
— — 01 08	PCI Memory Conflict
— — 01 81	Processor 1 failed BIST
— — 01 82	Front Panel Controller failed to function
— — 01 84	Hot-plug switches overridden by jumper or setup option
— — 02 00	Primary Boot Device Not Found
— — 02 08	PCI IRQ Conflict
— — 02 81	Processor 2 failed BIST
— — 02 84	Power fault on hot-plug PCI slot Pn
— — 03 08	PCI Error Log is full
— — 03 09	NVRAM Data Invalid, NVRAM Cleared
— — 03 81	Processor 3 failed BIST
— — 03 82	Primary Hot-swap Controller failed to function
— — 04 08	PCI ROM not found, May Be OK For This Card:
— — 04 81	Processor 0 Internal error (IERR)
— — 04 82	Secondary Hot-swap Controller failed to function
— — 05 08	Insufficient Memory to Shadow PCI ROM:
— — 05 09	NVRAM Cleared by Jumper
— — 05 81	Processor 1 Internal error (IERR)
— — 06 08	Memory Allocation Failure for Second PCI Segment
— — 06 09	Password Cleared by Jumper
— — 06 81	Processor 0 Thermal Trip error
— — 07 81	Processor 1 Thermal Trip error
— — 08 81	Watchdog timer failed on last boot
— — 09 08	PCI Error Log is full
— — 0B 81	Processor 0 failed initialization
— — 0C 81	Processor 0 disabled
— — 0D 81	Processor 1 disabled
— — 0E 81	Processor 0 failed FRB-3 timer
— — 0F 81	Processor 1 failed FRB-3 timer
— — 10 00	Cache Memory Failure, Do Not Enable Cache
— — 10 05	PCI Parity Error
— — 10 07	System Board Device Resource Conflict
— — 10 08	Floppy Disk Controller Resource Conflict
— — 10 81	Server Management Interface failed to function
— — 11 05	PCI System Error
— — 11 07	Static Device Resource Conflict
— — 11 08	Primary IDE Controller Resource Conflict
— — 12 08	Secondary IDE Controller Resource Conflict
— — 15 00	Primary Output Device Not Found
— — 15 08	Parallel Port Resource Conflict

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Event Description	Event Explanation
— — 16 00	Primary Input Device Not Found
— — 16 08	Serial Port 1 Resource Conflict
— — 17 08	Serial Port 2 Resource Conflict
— — 20 08	Expansion Board Disabled in Slot
— — 28 81	Processor 2 Internal error (IERR)
— — 29 81	Processor 3 Internal error (IERR)
— — 30 04	Timer Channel 2 Failure
— — 30 81	Processor 2 Thermal Trip error
— — 31 01	Floppy Drive A:
— — 31 81	Processor 3 Thermal Trip error
— — 32 01	Floppy Drive B:
— — 35 01	Floppy Disk Controller failure
— — 38 81	Processor 2 failed FRB-3 timer
— — 39 81	Processor 3 failed FRB-3 timer
— — 40 01	Shadow Of System BIOS Failed
— — 40 04	Gate-A20 Failure
— — 40 81	Processor 2 disabled
— — 41 04	Unexpected Interrupt in Protected Mode
— — 41 81	Processor 3 disabled
— — 42 00	ISA Configuration contains invalid information
— — 45 04	Master Interrupt Controller Error
— — 46 04	Slave Interrupt Controller Error
— — 48 81	Processor 1 failed initialization
— — 49 81	Processor 2 failed initialization
— — 4A 81	Processor 3 failed initialization
— — 50 00	PnP Memory Conflict:
— — 50 04	Master DMA Controller Error
— — 50 81	NVRAM Cleared by Jumper
— — 51 00	PnP 32-bit Memory Conflict:
— — 51 04	Slave DMA Controller Error
— — 52 00	PnP IRQ Conflict:
— — 52 04	DMA Controller Error
— — 52 81	ESCD Data Cleared
— — 53 00	PnP DMA Conflict:
— — 53 81	Password Cleared by Jumper
— — 54 00	PnP Error Log Is Full
— — 55 00	Bad PnP Serial ID Checksum:
— — 56 00	Bad PnP Resource Data Checksum:
— — 60 00	Keyboard Is Locked ... Please Unlock It
— — 60 04	Fail-safe Timer NMI Failure
— — 60 81	Unable to apply BIOS update for Processor 1
— — 61 04	Software Port NMI Failure
— — 61 81	Unable to apply BIOS update for Processor 2
— — 62 81	Unable to apply BIOS update for Processor 3
— — 63 81	Unable to apply BIOS update for Processor 4
— — 65 04	Bus Timeout NMI in Slot
— — 67 04	Expansion Board NMI in Slot
— — 68 81	Processor 1 L2 cache failed

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Event Description	Event Explanation
— — 69 81	Processor 2 L2 cache failed
— — 6A 81	Processor 3 L2 cache failed
— — 6B 81	Processor 4 L2 cache failed
— — 70 00	CMOS Time & Date Not Set
— — 70 01	Disabled CPU slot #
— — 70 03	Keyboard Controller Error
— — 70 81	BIOS does not support current stepping for Processor 1
— — 71 01	CPU Failure – CPU # 1
— — 71 81	BIOS does not support current stepping for Processor 2
— — 72 01	CPU Failure – CPU # 2
— — 72 81	BIOS does not support current stepping for Processor 3
— — 73 01	CPU Failure – CPU # 3
— — 73 03	Keyboard Stuck Key Detected
— — 73 81	BIOS does not support current stepping for Processor 4
— — 74 01	CPU Failure – CPU # 4
— — 75 01	CPU modules are incompatible or one is not present.
— — 75 03	Keyboard and Mouse Swapped
— — 76 01	Previous CPU Failure – CPU # 1
— — 77 01	Previous CPU Failure – CPU # 2
— — 78 01	Previous CPU Failure – CPU # 3
— — 79 01	Previous CPU Failure – CPU # 4
— — 80 00	Option ROM has bad checksum
— — 80 01	Attempting to boot with failed CPU
— — 80 07	PCI Segment 1 memory request exceeds 998 MB
— — 80 81	PXB1 failed to respond
— — 81 01	BSP switched, system may be in uni-processor mode
— — 81 07	PCI Segment 1 I/O requests exceeds 12KB
— — 81 81	Mismatch Among Processors Detected
— — 82 07	PCI I/O request exceeds amount available
— — 82 09	I/O Expansion Board NMI in Slot
— — 82 81	L2 cache size mismatch
— — 83 00	Shadow Of PCI ROM Failed
— — 83 07	PCI memory request exceeds amount available
— — 84 07	Illegal bus for memory request below 1 MB
— — 84 09	Expansion Board Disabled in Slot
— — 85 00	Shadow Of ISA ROM Failed
— — 85 07	Memory request below 1 MB exceeds 1 MB
— — 85 09	Fail-safe Timer NMI
— — 86 09	System Reset caused by Watchdog Timer
— — 87 09	Bus Timeout NMI in Slot
— — 89 02	System Memory Size Mismatch
— — 91 01	CMOS Battery Failed
— — 95 01	CMOS System Options Not Set
— — 95 02	Address Line Short Detected
— — 97 02	Base Or Extended Memory Error: Board #, DIMM #
— — 98 01	CMOS Checksum Invalid
— — 99 02	ECC Error Correction Failure

## Appendix B AD450NX Tables

The tables in this Appendix provide translations for SEL viewer data on the AD450NX server platform. See Table 2 in Section 3 for a description of each field.

**Note:** Data is not provided for the EmvRev field. This field is reserved for future use and currently provides no valuable information.

### B.1 AD450NX Generator ID Codes

Generator ID	Description
11 00	BIOS
20 00	BMC
22 00	FPC
C0 00	HSC #1
C2 00	HSC #2

### B.2 AD450NX Sensor Codes

Note that the AD450NX server system includes nine fans and twelve drive slots, but the table below displays some of the fans (Sensor Type 04) and drives (Sensor Type 0D) together under the same Sensor Numbers.

All nine fans and twelve drive slots in the AD450NX server system have Event Messages reported against them. However, the first six fans and the first six drive slots use Generator ID C0 00. The remaining three fans and six drives slots duplicate the Sensor Type / Sensor Number fields used by the first six fans / drive slots, but they use Generator ID C2 00 to uniquely identify them. The second Hot-swap Controller manages these fans and drives.

For example, an Event Message reported against the first fan will display an Event Message of C0 00 02 04 0E 01 a2 00 21. An Event Message reported against the seventh fan will display an Event message of C2 00 02 04 0E 01 a2 00 21.

Sensor Type	Sensor Number	Sensor Name
01		<b>Temperature</b>
	0A	PXB Temp Monitor
	01	Backplane Temperature
	16	Processor Baseboard Temperature Sensor
	17	Processor 1 Temperature Sensor
	18	Processor 2 Temperature Sensor
	19	Processor 3 Temperature Sensor
	1A	Processor 4 Temperature Sensor

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<b>01</b>		<b>Temperature</b>
	1B	Memory Module 1 Temperature Sensor
	1C	Memory Module 2 Temperature Sensor
<b>02</b>		
		<b>Voltage</b>
01		I/O Baseboard +3.3V
02		I/O Baseboard +12V
03		I/O Baseboard +5V
04		VCC _ Stand by
05		I/O Baseboard -12V
06		I/O Baseboard -5V
07		I/O Baseboard SC_VREF1 (SCSI Term. 1)
08		I/O Baseboard SC_VREF2 (SCSI Term. 2)
09		I/O Baseboard SC_VREF3 (SCSI Term. 2)
0B		VccP1
0C		VccP2
0D		VccP3
0E		VccP4
0F		VTT (Processor +1.5V)
10		Processor +2.5 V
11		Processor +3.3V
12		Processor +5V
13		Vcc_L2_1 (for processors 1 & 2)
14		Vcc_L2_1 (for processors 3 & 4)
15		Processor +12
21		Slot 1 VID
22		Slot 2 VID
23		Slot 3 VID
24		Slot 4 VID
25		L2 1 VID
26		L2 2 VID
27		L2 3 VID
28		L2 4 VID
<b>04</b>		
		<b>Fan</b>
0E		Fan 1 speed / Fan 7 speed
0F		Fan 2 speed / Fan 8 speed
10		Fan 3 speed / Fan 9 speed
11		Fan 4 speed
12		Fan 5 speed
13		Fan 6 speed
<b>05</b>		
		<b>Physical Security (Chassis Intrusion)</b>
03		Chassis Intrusion
04		Cover Open
<b>06</b>		
		<b>Secure Mode Violation Attempt</b>
01		Power Button Secure Mode Violation
02		Reset Button Secure mode Violation

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Sensor Type	Sensor Number	Sensor Name
<b>07</b>		<b>Processor</b>
	1D	Processor 1 Status
	1E	Processor 2 Status
	1F	Processor 3 Status
	20	Processor 4 Status
<b>08</b>		<b>Power Supply</b>
	06	Power Supply 1
	07	Power Supply 2
	08	Power Supply 3
	09	Power Supply 4
<b>09</b>		<b>Power Unit</b>
	05	Power Unit Status
<b>0C</b>		<b>Memory</b>
	29	DIMM 1 Presence Memory Module 1
	2A	DIMM 2 Presence Memory Module 1
	2B	DIMM 3 Presence Memory Module 1
	2C	DIMM 4 Presence Memory Module 1
	2D	DIMM 5 Presence Memory Module 1
	2E	DIMM 6 Presence Memory Module 1
	2F	DIMM 7 Presence Memory Module 1
	30	DIMM 8 Presence Memory Module 1
	31	DIMM 9 Presence Memory Module 1
	32	DIMM 10 Presence Memory Module 1
	33	DIMM 11 Presence Memory Module 1
	34	DIMM 12 Presence Memory Module 1
	35	DIMM 13 Presence Memory Module 1
	36	DIMM 14 Presence Memory Module 1
	37	DIMM 15 Presence Memory Module 1
	38	DIMM 16 Presence Memory Module 1
	39	DIMM 1 Presence Memory Module 2
	3A	DIMM 2 Presence Memory Module 2
	3B	DIMM 3 Presence Memory Module 2
	3C	DIMM 4 Presence Memory Module 2
	3D	DIMM 5 Presence Memory Module 2
	3E	DIMM 6 Presence Memory Module 2
3F	DIMM 7 Presence Memory Module 2	
40	DIMM 8 Presence Memory Module 2	
41	DIMM 9 Presence Memory Module 2	
42	DIMM 10 Presence Memory Module 2	
43	DIMM 11 Presence Memory Module 2	

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<b>0C</b>		<b>Memory</b>
	44	DIMM 12 Presence Memory Module 2
	45	DIMM 13 Presence Memory Module 2
	46	DIMM 14 Presence Memory Module 2
	47	DIMM 15 Presence Memory Module 2
	48	DIMM 16 Presence Memory Module 2
	EF	See BIOS Table below
<b>0D</b>		<b>Drive Slot (Bay)</b>
	02	Drive Slot 0 Status / Drive Slot 7 Status
	03	Drive Slot 1 Status / Drive Slot 8 Status
	04	Drive Slot 2 Status / Drive Slot 9 Status
	05	Drive Slot 3 Status / Drive Slot 10 Status
	06	Drive Slot 4 Status / Drive Slot 11 Status
	07	Drive Slot 5 Status / Drive Slot 12 Status
	08	Drive Slot 0 Presence / Drive Slot 7 Status
	09	Drive Slot 1 Presence / Drive Slot 8 Status
	0A	Drive Slot 2 Presence / Drive Slot 9 Status
	0B	Drive Slot 3 Presence / Drive Slot 10 Status
	0C	Drive Slot 4 Presence / Drive Slot 11 Status
	0D	Drive Slot 5 Presence / Drive Slot 12 Status
<b>0F</b>		<b>POST Error</b>
	4B	See POST Table below
<b>11</b>		<b>Watchdog</b>
	49	BMC Watchdog
<b>12</b>		<b>Critical Interrupt</b>
	EF	See BIOS Table below
<b>13</b>		<b>Critical Interrupt</b>
	28	See BIOS Table below
	29	See BIOS Table below
	4A	Front Panel Interrupt
	EF	See BIOS Table below
<b>1B</b>		<b>Cable / Interconnect</b>
	0A	F16 cable 1
	0B	F16 cable 2
	0C	Power Supply 4 Cable



## B.3 AD450NX Event Description Codes

The purpose of the Event Description field varies, depending on the Generator ID. When the Generator ID is

- 20 00
- 22 00
- C0 00
- C2 00

the first byte of the Event Description is used to indicate the type of event that occurred, such as the crossing of a threshold or the removal of a device.

When the Generator ID is 11 00, the Event Message was generated from the BIOS or from POST and Table B.4 or B.5 should be used to determine the definition of the Event Message. Refer to Section 3 for a complete explanation on table usage. Each “—” in the table below indicates a byte that may be disregarded.

Event Description	Event Type	Definition
01 — — —	N/A	Threshold crossed
02 — — —	N/A	Transition to idle, active, or busy
03 — — —	N/A	State asserted or deasserted
04 — — —	N/A	Predictive failure asserted or deasserted
05 — — —	N/A	Limit exceeded
06 — — —	N/A	Performance lag
07 — — —	N/A	Presence, Disabled, IERR, Thermal Trip, or FRB3
08 — — —	N/A	Device added or removed
09 — — —	N/A	Device enabled or disabled
0A — — —	N/A	Transition to running or test, on or off-line
EB — — —	N/A	Redundancy lost, regained, degraded
E7 — — —	07	Presence, Disabled, IERR, Thermal Trip, FRB3
E7 — — —	08	Presence or fault
E7 — — —	09	Power Off or Power Cycle, 240VA, Reserve, Lost AC
E7 — — —	49	BIOS WD Reset, OS WD Reset , OS WD Shutdown, Power down, Power off

## B.4 AD450NX BIOS Codes

To decode a BIOS error message, locate the Sensor Type and Sensor Number under which the error falls. Then use the Event Description to identify the specific error. This table uses “— —” to indicate bytes which are not applicable to the purposes of this document.

Sensor Type	Sensor Number	Event Description	Event Explanation
<b>0C</b>	<b>EF</b>		
		E7 20 [slot] [DIMM]	single bit memory error
		E7 21 [slot] [DIMM]	multi bit memory error
		E7 22 [slot] [DIMM]	memory parity error
<b>12</b>	<b>EF</b>		
		E7 01 — —	System Boot Event
		E7 00 — —	System Reconfiguration
<b>13</b>	<b>28</b>		
		E7 00 FF FF	Front Panel NMI
		E7 01 FF FF	Bus time-out NMI
		E7 02 FF FF	I/O channel check NMI
		E7 03 FF FF	Software NMI
		E7 04 FF FF	NMI PERR
		E7 05 FF FF	NMI SERR
		E7 44 00 14	BINIT Expander Parity
		E7 44 00 26	PCI DATA Parity Error
		E7 44 FF 10	AERR Address Parity Error
		E7 44 FF 15	BINIT Response Parity
		E7 44 FF 16	BINIT Request parity
		E7 45 00 13	BINIT Protocol Violation
		E7 45 00 18	SERR Protocol Violation
		E7 45 00 19	SERR Parity on Transmit
		E7 45 00 20	SERR parity on Receive
		E7 45 00 21	SERR Parity on address
		E7 45 00 22	SERR Inbound Timeout
		E7 45 00 23	SERR BUS parity
		E7 44 00 24	PCI PERR
		E7 45 00 25	PCI SERR
		E7 45 FF 11	BERR HOST BUS generic
		E7 45 FF 12	BINIT Hostbus Hardfail
E7 48 00 00	BINIT Hostbus ECC		
<b>13</b>	<b>29</b>		
		E8 60 00 FF	IMB Command Error

## B.5 AD450NX POST Codes

The Sensor Type is 0F for all POST errors. To decode a POST error message, use the last two bytes in the Event Description to identify the specific error. The first two bytes, indicated by “— —” are not relevant to identifying the error.

Event Description	Event Explanation
— — 00 02	Failure Fixed Disk
— — 00 08	PCI I/O Port Conflict
— — 00 09	NVRAM Checksum Error, NVRAM Cleared
— — 00 81	Processor 0 failed BIST
— — 00 82	Baseboard Management Controller failed to function
— — 01 08	PCI Memory Conflict
— — 01 81	Processor 1 failed BIST
— — 01 82	Front Panel Controller failed to function
— — 02 00	Primary Boot Device Not Found
— — 02 08	PCI IRQ Conflict
— — 02 81	Processor 2 failed BIST
— — 03 09	NVRAM Data Invalid, NVRAM Cleared
— — 03 81	Processor 3 failed BIST
— — 03 82	Primary Hot-swap Controller failed to function
— — 04 08	PCI ROM not found, May Be OK For This Card:
— — 04 81	Processor 0 Internal error (IERR)
— — 04 82	Secondary Hot-swap Controller failed to function
— — 05 08	Insufficient Memory to Shadow PCI ROM:
— — 05 81	Processor 1 Internal error (IERR)
— — 06 08	Memory Allocation Failure for Second PCI Segment
— — 06 81	Processor 0 Thermal Trip error
— — 07 81	Processor 1 Thermal Trip error
— — 08 81	Watchdog timer failed on last boot
— — 0B 81	Processor 0 failed initialization
— — 0C 81	Processor 0 disabled
— — 0D 81	Processor 1 disabled
— — 0E 81	Processor 0 failed FRB-3 timer
— — 0F 81	Processor 1 failed FRB-3 timer
— — 10 00	Cache Memory Failure, Do Not Enable Cache
— — 10 02	Stuck Key
— — 10 05	PCI Parity Error
— — 10 07	System Board Device Resource Conflict
— — 10 08	Floppy Disk Controller Resource Conflict
— — 10 81	Server Management Interface failed to function
— — 11 02	Keyboard error
— — 11 06	IDE configuration changed
— — 11 07	Static Device Resource Conflict
— — 11 08	Primary IDE Controller Resource Conflict
— — 12 02	Keyboard controller failed
— — 12 06	IDE configuration error – device disabled
— — 12 08	Secondary IDE Controller Resource Conflict
— — 13 02	Keyboard locked – Unlock key switch

## Guide to Interpreting System Event Log (SEL) Messages

Event Description	Event Explanation
— — 13 06	COM A configuration changed
— — 14 06	COM A configuration error – device disabled
— — 15 00	Primary Output Device Not Found
— — 15 06	COM B configuration changed
— — 15 08	Parallel Port Resource Conflict
— — 16 00	Primary Input Device Not Found
— — 16 06	COM B configuration error – device disabled
— — 16 08	Serial Port 1 Resource Conflict
— — 17 06	Floppy configuration changed
— — 17 08	Serial Port 2 Resource Conflict
— — 18 06	Floppy configuration error – device disabled
— — 19 06	Parallel port configuration changed
— — 1A 06	Parallel port configuration error – device disabled
— — 20 02	Monitor type does not match CMOS – Run SETUP
— — 20 08	Expansion Board Disabled in Slot
— — 28 81	Processor 2 Internal error (IERR)
— — 29 81	Processor 3 Internal error (IERR)
— — 30 02	System RAM failed at offset
— — 30 04	Timer Channel 2 Failure
— — 30 81	Processor 2 Thermal Trip error
— — 31 01	Floppy Drive A:
— — 31 02	Shadow RAM failed at offset
— — 31 81	Processor 3 Thermal Trip error
— — 32 01	Floppy Drive B:
— — 32 02	Extended RAM failed at address line, or Extended RAM failed at offset
— — 35 01	Floppy Disk Controller Failure
— — 38 81	Processor 2 failed FRB-3 timer
— — 39 81	Processor 3 failed FRB-3 timer
— — 40 01	Shadow Of System BIOS Failed
— — 40 04	Gate-A20 Failure
— — 40 81	Processor 2 disabled
— — 41 04	Unexpected Interrupt in Protected Mode
— — 41 81	Processor 3 disabled
— — 42 00	ISA Config contains invalid info
— — 45 04	Master Interrupt Controller Error
— — 46 04	Slave Interrupt Controller Error
— — 48 81	Processor 1 failed initialization
— — 49 81	Processor 2 failed initialization
— — 4A 81	Processor 3 failed initialization
— — 4B 81	BMC in Update Mode
— — 50 00	PnP Memory Conflict
— — 50 02	System battery is dead – Replace and run SETUP
— — 50 04	Master DMA Controller Error
— — 50 81	NVRAM Cleared by Jumper
— — 51 00	PnP 32-bit Memory Conflict
— — 51 02	System CMOS checksum bad – Default configuration used
— — 51 04	Slave DMA Controller Error
— — 52 00	PnP IRQ Conflict

## Guide to Interpreting System Event Log (SEL) Messages

Event Description	Event Explanation
— — 52 04	DMA Controller Error
— — 52 81	ESCD Data Cleared
— — 53 00	PnP DMA Conflict
— — 53 81	Password Cleared by Jumper
— — 54 00	PnP Error Log Is Full
— — 55 00	Bad PnP Serial ID Checksum
— — 56 00	Bad PnP Resource Data Checksum
— — 60 00	Keyboard Is Locked ... Please Unlock It
— — 60 02	System timer error
— — 60 04	Fail-safe Timer NMI Failure
— — 60 81	Unable to apply BIOS update for Processor 1
— — 61 04	Software Port NMI Failure
— — 61 81	Unable to apply BIOS update for Processor 2
— — 62 81	Unable to apply BIOS update for Processor 3
— — 63 81	Unable to apply BIOS update for Processor 4
— — 65 04	Bus Timeout NMI in Slot
— — 67 04	Expansion Board NMI in Slot
— — 68 81	Processor 1 L2 cache failed
— — 69 81	Processor 2 L2 cache failed
— — 6A 81	Processor 3 L2 cache failed
— — 6B 81	Processor 4 L2 cache failed
— — 70 00	CMOS Time & Date Not Set
— — 70 01	Disabled Processor slot #
— — 70 02	Real time clock error
— — 70 03	Keyboard Controller Error
— — 70 81	BIOS does not support current stepping for Processor 1
— — 71 01	Processor #1 Failure
— — 71 02	Check date and time settings
— — 71 81	BIOS does not support current stepping for Processor 2
— — 72 01	Processor #2 Failure
— — 72 81	BIOS does not support current stepping for Processor 3
— — 73 01	Processor #3 Failure
— — 73 03	Keyboard Stuck Key Detected
— — 73 81	BIOS does not support current stepping for Processor 4
— — 74 01	Processor #4 Failure
— — 75 01	Processor modules are incompatible or one is not present
— — 75 03	Keyboard and Mouse Swapped
— — 76 01	Previous Processor #1 Failure
— — 77 01	Previous Processor #2 Failure
— — 78 01	Previous Processor #3 Failure
— — 79 01	Previous Processor #4 Failure
— — 80 00	Option ROM has bad checksum
— — 80 01	Attempting to boot with failed processor
— — 80 02	Previous boot incomplete – Default configuration used
— — 80 07	PCI Segment 1 memory request exceeds 998 MB
— — 80 81	PXB1 failed to respond
— — 81 01	BSP switched, system may be in uni-processor mode
— — 81 07	PCI Segment 1 I/O requests exceeds 12KB

## Guide to Interpreting System Event Log (SEL) Messages

Event Description	Event Explanation
— — 81 81	Mismatch Among Processors Detected
— — 82 07	PCI I/O request exceeds amount available
— — 82 09	I/O Expansion Board NMI in Slot
— — 82 81	L2 cache size mismatch
— — 83 00	Shadow Of PCI ROM Failed
— — 83 07	PCI memory request exceeds amount available
— — 84 07	Illegal bus for memory request below 1 MB
— — 84 09	Expansion Board Disabled in Slot
— — 85 00	Shadow Of ISA ROM Failed
— — 85 07	Memory request below 1 MB exceeds 1 MB
— — 85 09	Fail-safe Timer NMI
— — 86 09	System Reset caused by Watchdog Timer
— — 87 09	Bus Timeout NMI in Slot
— — 89 02	System Memory Size Mismatch
— — 91 01	CMOS Battery Failed
— — 95 01	CMOS System Options Not Set
— — 95 02	Address Line Short Detected
— — 97 02	Base Or Extended Memory Error: Board #, DIMM #
— — 98 01	CMOS Checksum Invalid
— — 99 02	ECC Error Correction Failure
— — B0 02	Diskette drive A error
— — B1 02	Diskette drive B error
— — B2 02	Incorrect drive A type – Run SETUP
— — B3 02	Incorrect drive B type – Run SETUP
— — D0 02	System cache error – cache disabled
— — F0 02	CPU ID
— — F5 02	DMA test failed
— — F6 02	Software NMI failed
— — F7 02	Fail-safe timer NMI failed

## Appendix C C440GX Tables

The tables in this Appendix provide translations for SEL viewer data on the C440GX server platform. See Table 2 in Section 3 for a description of each field.

**Note:** Data is not provided for the EmvRev field. This field is reserved for future use and currently provides no valuable information.

### C.1 C440GX Generator ID Codes

Generator ID	Description
11 00	BIOS
20 00	BMC
C0 00	HSC

### C.2 C440GX Sensor Codes

Sensor Type	Sensor Number	Sensor Name
01		<b>Temperature</b>
	17	Primary Processor Temp
	18	Secondary Processor Temp
	19	Baseboard Temperature
	1A	Chassis Temperature (PSB)
02		<b>Voltage</b>
	01	Baseboard 5V
	02	Baseboard 3.3V
	03	Primary Processor
	04	Secondary Processor
	05	Processor 2.5V
	06	L2 Cache
	07	Baseboard SCSI-W LVDS Term1
	08	Baseboard SCSI-W LVDS Term2
	09	3V Standby (Wake On LAN)
	0A	Baseboard -12V
	0B	Baseboard SCSI-W SGL Term
	0C	Processor 1.5V
	0D	Baseboard -5V
0E	Baseboard +12V	

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<b>04</b>		<b>Fan</b>
	0F	Baseboard Fan 1
	10	Baseboard Fan 2
	11	Baseboard Fan 3
	12	Baseboard Fan 4
	1F	Digital Fan 1 <sup>(1)</sup>
	20	Digital Fan 2 <sup>(1)</sup>
	21	Digital Fan 3 <sup>(1)</sup>
	22	Digital Fan 4 <sup>(1)</sup>
	29	Primary Processor Fan
	2A	Secondary Processor Fan
	2B	Power Supply 1 Fan
	2C	Power Supply 2 Fan
	2D	Power Supply 3 Fan
	34	Primary Processor Digital Fan
	35	Secondary Processor Digital Fan
36	PSB Aux. Fan	
<b>05</b>		
		<b>Physical Security</b>
	26	Chassis Intrusion
<b>06</b>		
		<b>Secure Mode Sensor</b>
	27	EMP Password
	28	Secure Mode
<b>07</b>		
		<b>Processor</b>
	1B	Primary Processor Status
	1C	Secondary Processor Status
<b>08</b>		
		<b>Power Supply</b>
	2E	Power Supply 1
	2F	Power Supply 2
	30	Power Supply 3
<b>09</b>		
		<b>Power Unit</b>
	31	Redundancy Lost
	32	Power Unit
	0C	Memory
<b>EF</b>		
		<b>See BIOS table</b>
<b>0D</b>		
		<b>Drive Slot (Bay)</b>
	02	Drive Slot 0 Status
	03	Drive Slot 1 Status
	04	Drive Slot 2 Status
	05	Drive Slot 3 Status
	06	Drive Slot 4 Status
<b>0D</b>		
		<b>Drive Slot (Bay)</b>
	07	Drive Slot 0 Presence



Sensor Type	Sensor Number	Sensor Name
	08	Drive Slot 1 Presence
	09	Drive Slot 2 Presence
	0A	Drive Slot 3 Presence
	0B	Drive Slot 4 Presence
<b>0F</b>		<b>POST Error</b>
	25	See POST table
<b>11</b>		<b>Watchdog</b>
	1D	BMC Watchdog
<b>12</b>		<b>System Event</b>
		EF
<b>13</b>		<b>Critical Interrupt</b>
	1E	Front Panel NMI

### C.3 C440GX Event Description Codes

The purpose of the Event Description field varies, depending on the Generator ID. When the Generator ID is

- 20 00
- 22 00
- C0 00

the first byte of the Event Description is used to indicate the type of event that occurred, such as the crossing of a threshold or the removal of a device.

When the Generator ID is 11 00, the Event Message was generated from the BIOS or from POST and Table C.4 or C.5 should be used to determine the definition of the Event Message. Refer to Section 3 for a complete explanation on table usage. Each “—” in the table below indicates a byte that may be disregarded.

Event Description	Event Type	Definition
01 — — —	N/A	Threshold crossed
02 — — —	N/A	Transition to idle, active, or busy
03 — — —	N/A	State asserted or deasserted
04 — — —	N/A	Predictive failure asserted or deasserted
05 — — —	N/A	Limit exceeded
06 — — —	N/A	Performance lag
07 — — —	N/A	Presence, Disabled, IERR, Thermal Trip, or FRB3
08 — — —	N/A	Device added or removed
09 — — —	N/A	Device enabled or disabled
0A — — —	N/A	Transition to running or test, on or off-line
EB — — —	N/A	Redundancy lost, regained, degraded
E7 — — —	07	Presence, Disabled, IERR, Thermal Trip, FRB3
E7 — — —	08	Presence or fault

Event Description	Event Type	Definition
E7 — — —	09	Power Off or Power Cycle, 240VA, Reserve, Lost AC
E7 — — —	49	BIOS WD Reset, OS WD Reset , OS WD Shutdown, Power down, Power off

## C.4 C440GX BIOS Codes

To decode a BIOS error message, locate the Sensor Type and Sensor Number under which the error falls. Then use the Event Description to identify the specific error. This table uses “— —” to indicate bytes which are not applicable to the purposes of this document.

Sensor Type	Sensor Number	Event Description	Event Explanation
12	EF		
		E7 01 — —	System Boot Event
		E7 00 — —	System Reconfiguration
0C	EF		
		E7 40 [DIMM#] —	Single Bit Memory Error
		E7 41 [DIMM#] —	Multi Bit Memory Error
		E7 02 — —	Memory Parity Error
13	28		
		E7 00 — —	Front Panel NMI
13	EF		
		E7 01 — —	Bus Timeout
		E7 02 — —	I/O CHK
		E7 03 — —	Software NMI
		E7 04 — —	PCI PERR

## C.5 C440GX POST Codes

The Sensor Type is 0F for all POST errors. To decode a POST error message, use the last two bytes in the Event Description to identify the specific error. The first two bytes, indicated by “— —” are not relevant to identifying the error.

Event Description	Event Explanation
— — 00 02	Failure Fixed Disk
— — 00 81	Processor 0 failed BIST
— — 01 04	Invalid System Configuration Data - run configuration utility
— — 01 06	Device configuration changed
— — 01 81	Processor 1 failed BIST
— — 02 06	Configuration error - device disabled
— — 03 04	Resource Conflict
— — 04 04	Resource Conflict
— — 04 05	Resource Conflict
— — 04 81	Processor 0 Internal Error (IERR) failure

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Event Description	Event Explanation
— — 05 04	Expansion ROM not initialized
— — 05 05	Expansion ROM not initialized
— — 05 81	Processor 1 Internal Error (IERR) failure
— — 06 04	Warning: IRQ not configured
— — 06 05	Warning: IRQ not configured
— — 06 81	Processor 0 Thermal Trip failure
— — 07 81	Processor 1 Thermal Trip failure
— — 08 81	Watchdog Timer failed on last boot, BSP switched.
— — 0A 81	Processor 1 failed initialization on last boot.
— — 0B 81	Processor 0 failed initialization on last boot.
— — 0C 81	Processor 0 disabled, system in Uni-processor mode
— — 0D 81	Processor 1 disabled, system in Uni-processor mode
— — 0E 81	Processor 0 failed FRB Level 3 timer
— — 0F 81	Processor 1 failed FRB Level 3 timer
— — 10 02	Stuck Key
— — 10 81	Server Management Interface failed to function
— — 11 02	Keyboard error
— — 12 02	Keyboard Controller Failed
— — 13 02	Keyboard locked - Unlock key switch
— — 20 02	Monitor type does not match CMOS - Run SETUP
— — 20 81	IOP sub-system is not functional
— — 30 02	System RAM Failed at offset xx
— — 31 02	Shadow Ram Failed at offset xx
— — 32 02	Extended RAM Failed at offset xx
— — 50 02	System battery is dead - Replace and run SETUP
— — 50 81	NVRAM Cleared by Jumper
— — 51 02	System CMOS checksum bad - Default configuration used
— — 51 81	NVRAM Checksum Error, NVRAM cleared
— — 52 81	NVRAM Data Invalid, NVRAM cleared
— — 60 02	System timer error
— — 62 01	BIOS unable to apply BIOS update to processor 1
— — 63 01	BIOS unable to apply BIOS update to processor 2
— — 64 01	BIOS does not support current stepping for processor 1
— — 65 01	BIOS does not support current stepping for processor 2
— — 70 02	Real time clock error
— — 97 02	ECC Memory error in base (extended) memory test in Bank xx
— — B2 02	Incorrect Drive A type - run SETUP
— — B3 02	Incorrect Drive B type - run SETUP
— — D0 02	System cache error - Cache disabled
— — F5 02	DMA Test Failed
— — F6 02	Software NMI Failed

## Appendix D L440GX Tables

The tables in this Appendix provide translations for SEL viewer data on the L440GX server platform. See Table 2 in Section 3 for a description of each field.

**Note:** Data is not provided for the EmvRev field. This field is reserved for future use and currently provides no valuable information.

### D.1 L440GX Generator ID Codes

Generator ID	Description
11 00	BIOS
20 00	BMC
22 00	FPC
C0 00	HSC #1
C2 00	HSC #2

### D.2 L440GX Sensor Codes

Sensor Type	Sensor Number	Sensor Name
<b>01</b>		<b>Temperature</b>
	01	Backplane Temperature
	17	Primary Processor Temp
	18	Secondary Processor Temp
	19	Baseboard Temperature 1
	1A	Baseboard Temperature 2
<b>02</b>		<b>Voltage</b>
	01	Baseboard 5V
	02	Baseboard 3.3V
	03	Primary Processor
	04	Secondary Processor
	05	Processor 2.5V
	06	5V Standby
	07	Baseboard SCSI-W LVDS Term1
	08	Baseboard SCSI-W LVDS Term2
	09	3V Standby (Wake On LAN)
	0A	Baseboard -12V
	0B	Baseboard SCSI-W SGL Term
	0C	Processor 1.5V
	0D	Baseboard -5V
0E	Baseboard +12V	

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Sensor Type	Sensor Number	Sensor Name
<b>04</b>		<b>Fan</b>
	0C	Backplane Fan 1
	0D	Backplane Fan 2
	0F	Baseboard Fan 0
	10	Baseboard Fan 1
	11	Processor Fan 0
	12	Processor Fan 1
	1F	Digital Fan 1 <sup>1</sup>
	20	Digital Fan 2 <sup>1</sup>
	21	Digital Fan 3 <sup>1</sup>
	22	Digital Fan 4 <sup>1</sup>
<b>05</b>		<b>Physical Security</b>
	26	Chassis Intrusion
<b>06</b>		<b>Secure Mode Sensor</b>
	27	EMP Password
	28	Secure Mode Sensor
<b>07</b>		<b>Processor</b>
	1B	Primary Processor Status
	1C	Secondary Processor Status
<b>0C</b>		<b>Memory</b>
	EF	See BIOS table
<b>0D</b>		<b>Drive Slot (Bay)</b>
	02	Drive Slot 0 Status
	03	Drive Slot 1 Status
	04	Drive Slot 2 Status
	05	Drive Slot 3 Status
	06	Drive Slot 4 Status
	07	Drive Slot 0 Presence
	08	Drive Slot 1 Presence
	09	Drive Slot 2 Presence
	0A	Drive Slot 3 Presence
	0B	Drive Slot 4 Presence
	<b>0F</b>	
25		See POST table
<b>11</b>		<b>Watchdog</b>
	1D	BMC Watchdog

Sensor Type	Sensor Number	Sensor Name
12		<b>System Event</b>
	EF	See BIOS table
13		<b>Critical Interrupt</b>
	1E	Front Panel NMI

- Digital Fans and Tach fans will use the same header connections but will report events using distinct sensor numbers. Depending on the chassis used and the implementation, Tach fans or a combination of Tach and Digital fans may be installed. Events and Sensor Numbers are determined by the Sensor Data Record.

### D.3 L440GX Event Description Codes

The purpose of the Event Description field varies, depending on the Generator ID. When the Generator ID is

- 20 00
- 22 00
- C0 00

the first byte of the Event Description is used to indicate the type of event that occurred, such as the crossing of a threshold or the removal of a device.

When the Generator ID is 11 00, the Event Message was generated from the BIOS or from POST and Table D.4 or D.5 should be used to determine the definition of the Event Message. Refer to Section 3 for a complete explanation on table usage. Each “—” in the table below indicates a byte that may be disregarded.

Event Description	Event Type	Definition
01 — — —	N/A	Threshold crossed
03 — — —	N/A	State Asserted, State Deasserted
06 — — —	N/A	Performance Met or Lags
0B — — —	N/A	Redundancy Lost
6F — — —	N/A	Presence, Failure, Disabled, Predictive fail (fan fail), Watchdog Expired, Hard Reset, Power Down, Power Cycle

### D.4 L440GX BIOS Codes

To decode a BIOS error message, locate the Sensor Type and Sensor Number under which the error falls. Then use the Event Description to identify the specific error. This table uses “— —” to indicate bytes which are not applicable to the purposes of this document.

Sensor Type	Sensor Number	Event Description in hex	Event Type
12	EF		
		E7 01 — —	System Boot Event
		E7 00 — —	System Reconfiguration

Sensor Type	Sensor Number	Event Description in hex	Event Type
0C	EF		
		E7 02 — —	Memory Parity Error
		E7 40 [DIMM#] —	Single Bit Memory Error
		E7 41 [DIMM#] —	Multi Bit Memory Error
13	28		
		E7 00 — —	Front Panel NMI
13	EF		
		E7 01 — —	Bus Timeout
		E7 02 — —	I/O CHK
		E7 03 — —	Software NMI
		E7 04 — —	PCI PERR

## D.5 L440GX POST Codes

The Sensor Type is 0F for all POST errors. To decode a POST error message, use the last two bytes in the Event Description to identify the specific error. The first two bytes, indicated by “— —” are not relevant to identifying the error.

Event Description	Event Explanation
— — 00 02	Failure Fixed Disk
— — 00 81	Processor 0 failed BIST
— — 01 04	Invalid System Configuration Data - run configuration utility
— — 01 06	Device configuration changed
— — 01 81	Processor 1 failed BIST
— — 02 06	Configuration error - device disabled
— — 03 04	Resource Conflict
— — 04 04	Resource Conflict
— — 04 05	Resource Conflict
— — 04 81	Processor 0 Internal Error (IERR) failure
— — 05 04	Expansion ROM not initialized
— — 05 05	Expansion ROM not initialized
— — 05 81	Processor 1 Internal Error (IERR) failure
— — 06 04	Warning: IRQ not configured
— — 06 05	Warning: IRQ not configured
— — 06 81	Processor 0 Thermal Trip failure
— — 07 81	Processor 1 Thermal Trip failure
— — 08 81	Watchdog Timer failed on last boot, BSP switched.
— — 0A 81	Processor 1 failed initialization on last boot.
— — 0B 81	Processor 0 failed initialization on last boot.
— — 0C 81	Processor 0 disabled, system in Uni-processor mode
— — 0D 81	Processor 1 disabled, system in Uni-processor mode
— — 0E 81	Processor 0 failed FRB Level 3 timer
— — 0F 81	Processor 1 failed FRB Level 3 timer
— — 10 02	Stuck Key

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Event Description	Event Explanation
— — 10 81	Server Management Interface failed to function
— — 11 02	Keyboard error
— — 12 02	Keyboard Controller Failed
— — 13 02	Keyboard locked - Unlock key switch
— — 20 02	Monitor type does not match CMOS - Run SETUP
— — 20 81	IOP sub-system is not functional
— — 30 02	System RAM Failed at offset xx
— — 31 02	Shadow Ram Failed at offset xx
— — 32 02	Extended RAM Failed at offset xx
— — 50 02	System battery is dead - Replace and run SETUP
— — 50 81	NVRAM Cleared by Jumper
— — 51 02	System CMOS checksum bad - Default configuration used
— — 51 81	NVRAM Checksum Error, NVRAM cleared
— — 52 81	NVRAM Data Invalid, NVRAM cleared
— — 60 02	System timer error
— — 62 01	BIOS unable to apply BIOS update to processor 1
— — 63 01	BIOS unable to apply BIOS update to processor 2
— — 64 01	BIOS does not support current stepping for processor 1
— — 65 01	BIOS does not support current stepping for processor 2
— — 70 02	Real time clock error
— — 97 02	ECC Memory error in base (extended) memory test in Bank xx
— — B2 02	Incorrect Drive A type - run SETUP
— — B3 02	Incorrect Drive B type - run SETUP
— — D0 02	System cache error - Cache disabled
— — F5 02	DMA Test Failed
— — F6 02	Software NMI Failed



## Appendix E N440BX Tables

The tables in this Appendix provide translations for SEL viewer data on the N440BX server platform. See Table 2 in Section 3 for a description of each field.

**Note:** Data is not provided for the EmvRev field. This field is reserved for future use and currently provides no valuable information.

### E.1 N440BX Generator ID Codes

Generator ID	Description
11 00	BIOS
20 00	BMC
C0 00	HSC

### E.2 N440BX Sensor Codes

Sensor Type	Sensor Number	Sensor Name
<b>01</b>		<b>Temperature</b>
	13	Primary Processor Socket Temp (disabled by default)
	14	Secondary Processor Socket Temp (disabled by default)
	15	Baseboard Temp1 (disabled by default)
	16	Baseboard Temp2 (disabled by default)
	17	Processor1 Temp
	18	Processor2 Temp
	19	Baseboard Temp1
	1A	Baseboard Temp2
	01	Backplane Temperature
<b>02</b>		<b>Voltage</b>
	01	Baseboard 5V
	02	Baseboard 3.3V
	03	Primary Processor
	04	Secondary Processor
	05	Processor 2.5V
	06	5v Standby
	07	Baseboard SCSI-A Term1
	08	Baseboard SCSI-A Term2
	09	Baseboard SCSI Term3
	0A	Baseboard -12V
	0B	Baseboard SCSI-B Term1
	0C	Processor 1.5V
	0D	Baseboard -5V
0E	Baseboard 12	
<b>04</b>		<b>Fan</b>
	0F	Baseboard Fan0
	10	Baseboard Fan1
	11	Processor Fan0

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Sensor Type	Sensor Number	Sensor Name
	12	Processor Fan1
	0C	Backplane Fan1 speed
	0D	Backplane Fan2 speed
<b>05</b>		
		<b>Physical Security (Chassis Intrusion)</b>
	26	Chassis Intrusion
<b>06</b>		
		<b>Secure Mode Violation Attempt</b>
	27	EMP password violation
	28	Secure Mode Violation Attempt (at the time of connecting to the server)
<b>07</b>		
		<b>Processor</b>
	1B	Processor1 Status
	1C	Processor2 Status
<b>0C</b>		
		<b>Memory</b>
	1F	DIMM1 Presence
	20	DIMM2 Presence
	21	DIMM3 Presence
	22	DIMM4 Presence
	EF	See BIOS Table below
<b>0D</b>		
		<b>Drive Bay</b>
	02	Drive Slot 0 Status
	03	Drive Slot 1 Status
	04	Drive Slot 2 Status
	05	Drive Slot 3 Status
	06	Drive Slot 4 Status
	07	Drive Slot 0 Presence
	08	Drive Slot 1 Presence
	09	Drive Slot 2 Presence
	0A	Drive Slot 3 Presence
	0B	Drive Slot 4 Presence
<b>0F</b>		
		<b>POST Error</b>
	25	See POST Table below
<b>11</b>		
		<b>Watchdog</b>
	1D	Watchdog Event
<b>12</b>		
		<b>System Event</b>
	EF	See BIOS Table below
<b>13</b>		
		<b>Critical Interrupt</b>
	EF	See BIOS Table below

## E.3 N440BX Event Description Codes

The purpose of the Event Description field varies, depending on the Generator ID. When the Generator ID is

- 20 00
- C0 00

the first byte of the Event Description is used to indicate the type of event that occurred, such as the crossing of a threshold or the removal of a device. When the Generator ID is 11 00, the Event Message was generated from the BIOS or from POST and the BIOS or POST tables should be used. Refer to Section 3 for a complete explanation on table usage. Each “—” in the tables indicates a byte that may be disregarded.

Event Description	Event Type	Definition
01 — — —	N/A	Threshold crossed
02 — — —	N/A	Transition to idle, active, or busy
03 — — —	N/A	State asserted or deasserted
04 — — —	N/A	Predictive failure asserted or deasserted
05 — — —	N/A	Limit exceeded
06 — — —	N/A	Performance lag
07 — — —	N/A	Presence, Disabled, IERR, Thermal Trip, or FRB3
08 — — —	N/A	Device added or removed
09 — — —	N/A	Device enabled or disabled
0A — — —	N/A	Transition to running or test, on or off-line
EB — — —	N/A	Redundancy lost, regained, degraded
E7 — — —	07	Presence, Disabled, IERR, Thermal Trip, FRB3
E7 — — —	08	Presence or fault
E7 — — —	09	Power Off or Power Cycle, 240VA, Reserve, Lost AC
E7 — — —	49	BIOS WD Reset, OS WD Reset OS WD Shutdown, Power down, Power off

## E.4 N440BX BIOS Codes

To decode a BIOS error message, locate the Sensor Number under which the error falls and then use the first two bytes in the Event Description to identify the specific error.

Sensor Type	Sensor Number	Event Description	Event Explanation
12	EF		
		E7 01 — —	System Boot Event
		E7 00 — —	System Reconfiguration
0C	EF		
		E7 20 — —	Single Bit Memory Error
		E7 21 — —	Double Bit Memory Error
		E7 02 — —	Memory Parity Error

Sensor Type	Sensor Number	Event Description	Event Explanation
13	EF		
		E7 01 — —	Bus Timeout
		E7 02 — —	I/O CHK
		E7 03 — —	Software NMI
		E7 04 — —	PCI PERR
		E7 05 — —	PCI SERR
13	1E		
		E7 00 --- ---	Front Panel NMI

## E.5 N440BX POST Codes

The Sensor Type is 0F for all POST errors. To decode a POST error message, use the last two bytes in the Event Description to identify the specific error. The first two bytes, indicated by “— —” are not relevant to identifying the error.

**Note:** To keep similar events together, this table is sorted by the fourth byte of the Event Description.

Event Description	Event Explanation
— — 62 01	BIOS unable to apply BIOS update to processor 1
— — 63 01	BIOS unable to apply BIOS update to processor 2
— — 64 01	BIOS does not support current stepping for processor 1
— — 65 01	BIOS does not support current stepping for processor 2
— — 00 02	Failure Fixed Disk
— — 10 02	Stuck Key
— — 11 02	Keyboard error
— — 12 02	Keyboard Controller Failed
— — 13 02	Keyboard locked - Unlock key switch
— — 20 02	Monitor type does not match CMOS - Run SETUP
— — 30 02	System RAM Failed at offset xx
— — 31 02	Shadow Ram Failed at offset xx
— — 32 02	Extended RAM Failed at offset xx
— — 50 02	System battery is dead - Replace and run SETUP
— — 51 02	System CMOS checksum bad - Default configuration used
— — 60 02	System timer error
— — 70 02	Real time clock error
— — 97 02	ECC Memory error in base (extended) memory test in Bank xx
— — B2 02	Incorrect Drive A type - run SETUP
— — B3 02	Incorrect Drive B type - run SETUP
— — D0 02	System cache error - Cache disabled
— — F5 02	DMA Test Failed
— — F6 02	Software NMI Failed
— — 01 04	Invalid System Configuration Data - run configuration utility
— — 03 04	Resource Conflict
— — 04 04	Resource Conflict
— — 05 04	Expansion ROM not initialized
— — 06 04	Warning: IRQ not configured

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Event Description	Event Explanation
— — 04 05	Resource Conflict
— — 05 05	Expansion ROM not initialized
— — 06 05	Warning: IRQ not configured
— — 01 06	Device configuration changed
— — 02 06	Configuration error - device disabled
— — 00 81	Processor 0 failed BIST
— — 01 81	Processor 1 failed BIST
— — 04 81	Processor 0 Internal Error (IERR) failure
— — 05 81	Processor 1 Internal Error (IERR) failure
— — 06 81	Processor 0 Thermal Trip failure
— — 07 81	Processor 1 Thermal Trip failure
— — 08 81	Watchdog Timer failed on last boot, BSP switched.
— — 0A 81	Processor 1 failed initialization on last boot.
— — 0B 81	Processor 0 failed initialization on last boot.
— — 0C 81	Processor 0 disabled, system in Uni-processor mode
— — 0D 81	Processor 1 disabled, system in Uni-processor mode
— — 0E 81	Processor 0 failed FRB Level 3 timer
— — 0F 81	Processor 1 failed FRB Level 3 timer
— — 10 81	Server Management Interface failed to function
— — 20 81	IOP sub-system is not functional
— — 50 81	NVRAM Cleared by Jumper
— — 51 81	NVRAM Checksum Error, NVRAM cleared
— — 52 81	NVRAM Data Invalid, NVRAM cleared

## Appendix F OCPRF100 Tables

The tables in this Appendix provide translations for SEL viewer data on the OCPRF100 server platform. See Table 2 in Section 3 for a description of each field.

**Note:** Data is not provided for the EmvRev field. This field is reserved for future use and currently provides no valuable information.

### F.1 OCPRF100 Generator ID Codes

Generator ID	Description
11 00	BIOS
20 00	BMC
22 00	FPC
C0 00	HSC

### F.2 OCPRF100 Sensor Codes

Sensor Type	Sensor Number	Sensor Name
<b>01</b>		<b>Temperature</b>
	1F	I/O Carrier Temp Monitor
	20	Memory Carrier Left Temp Sensor
	21	Memory Carrier Right Temp Sensor
	22	Processor Left 1 Temp Sensor
	23	Processor Left 2 Temp Sensor
	24	Processor Left 3 Temp Sensor
	25	Processor Left 4 Temp Sensor
	26	Processor Right 1 Temp Sensor
	27	Processor Right 2 Temp Sensor
	28	Processor Right 3 Temp Sensor
29	Processor Right 4 Temp Sensor	
<b>02</b>		<b>Voltage</b>
	01	I/O Carrier +3.3V
	02	I/O Carrier +12V
	03	I/O Carrier +5V
	04	Vcc_Stdbby

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<b>02</b>		<b>Voltage</b>
	05	I/O Carrier -12V
	06	I/O Carrier SCWA_VREF0
	07	I/O Carrier SCWA_VREF1
	08	I/O Carrier SCWA_VREF2
	09	I/O Carrier SCWA_VREF0
	0A	I/O Carrier SCWB_VREF1
	0B	I/O Carrier SCWB_VREF2
	0C	VccP1_Left
	0D	VccP2_Left
	0E	VccP3_Left
	0F	VccP4_Left
	10	VTT
	11	Processor +2.5V
	12	Processor +3.3V
	13	Processor +5V
	14	VccP1_Right
	15	VccP2_Right
	16	Processor +12V
	17	VccP3_Right
	18	VccP4_Right
	19	Vcc_L2_12Left
	1A	Vcc_L2_34Left
	1B	Vcc_L2_12Right
	1C	Vcc_L2_34Right
	32	Slot Left 1 VID
	33	Slot Left 2 VID
	34	Slot Left 3 VID
	35	Slot Left 4 VID
	36	Slot Right 1 VID
	37	Slot Right 2 VID
	38	Slot Right 3 VID
	39	Slot Right 4 VID
	3A	L2 Left 1 VID
	3B	L2 Left 2 VID
	3C	L2 Left 3 VID
	3D	L2 Left 4 VID
	3E	L2 Right 1 VID
	3F	L2 Right 2 VID
	40	L2 Right 3 VID
	41	L2 Right 4 VID
<b>04</b>		<b>Fan</b>
	0C	Fan 1 speed
	0D	Fan 2 speed
	0E	Fan 3 speed
	0F	Fan 4 speed
	10	Fan 5 speed
	11	Fan 6 speed

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Sensor Type	Sensor Number	Sensor Name
<b>06</b>		<b>Secure Mode Violation Attempt</b>
	01	Power Button Secure Mode Violation
	02	Reset Button Secure Mode Violation
<b>07</b>		<b>Processor</b>
	2A	Processor Left 1 Status
	2B	Processor Left 2 Status
	2C	Processor Left 3 Status
	2D	Processor Left 4 Status
	2E	Processor Right 1 Status
	2F	Processor Right 2 Status
	30	Processor Right 3 Status
	31	Processor Right 4 Status
<b>08</b>		<b>Power Supply</b>
	06	Power Supply 1
	07	Power Supply 2
	08	Power Supply 3
<b>09</b>		<b>Power Unit</b>
	05	Power Unit Status
<b>10</b>		<b>Event Logging</b>
	02	See BIOS Table below
<b>0C</b>		<b>ECC Memory</b>
	01	See BIOS Table below
<b>0D</b>		<b>Drive Slot (Bay)</b>
	04	Drive Slot 0 Presence
	05	Drive Slot 1 Presence
<b>0F</b>		<b>POST</b>
	4E	See POST Table below
<b>11</b>		<b>Watchdog</b>
	4C	BMC Watchdog
<b>12</b>		<b>System Event</b>
	08	See BIOS Table below
<b>13</b>		<b>System Bus</b>
	03	See BIOS Table below
	04	See BIOS Table below
	06	See BIOS Table below
	4D	FP NMI



Sensor Type	Sensor Number	Sensor Name
19		<b>Coherency Filter</b>
	05	See BIOS Table below
21		<b>PHP Slot<sup>1</sup></b>
	42	PHP Slot 1
	43	PHP Slot 2
	44	PHP Slot 3
	45	PHP Slot 4
	46	PHP Slot 5
	47	PHP Slot 6
	48	PHP Slot 7
	49	PHP Slot 8
	4A	PHP Slot 9
	4B	PHP Slot 10

**Note:**

1. See information regarding Event Description Codes in Section F.3

### F.3 OCPRF100 Event Description Codes

The purpose of the Event Description field varies, depending on the Generator ID. When the Generator ID is

- 20 00
- 22 00
- C0 00

the first byte of the Event Description is used to indicate the type of event that occurred, such as the crossing of a threshold or the removal of a device.

When the Generator ID is 11 00, the Event Message was generated from the BIOS or from POST and Table F.4 or F.5 should be used to determine the definition of the Event Message. Refer to Section 3 for a complete explanation on table usage. Each “—” in the table below indicates a byte that may be disregarded.

Event Description	Event Type	Definition
01 — — —	N/A	Threshold crossed
02 — — —	N/A	Transition to idle, active, or busy
03 — — —	N/A	State asserted or deasserted
04 — — —	N/A	Predictive failure asserted or deasserted
05 — — —	N/A	Limit exceeded
06 — — — <sup>1</sup>	N/A	Performance lag
07 — — — <sup>1</sup>	N/A	Presence, Disabled, IERR, Thermal Trip, or FRB3
08 — — —	N/A	Device added or removed
09 — — —	N/A	Device enabled or disabled
0A — — —	N/A	Transition to running or test, on or off-line

**Note:**

1. The PHP sensors will have an Event Description beginning with either E6 or E7 with an offset of 00 or 05 (hexadecimal view). This may be translated as follows

Event Description	Offset	Definition
06	00	PHP slot fault de-asserted
06	05	PHP slot powered on
07	00	PHP slot fault asserted
07	05	PHP slot powered off

## F.4 OCPRF100 BIOS Codes

To decode a BIOS error message, locate the Sensor Type and Sensor Number under which the error falls. Then use the Event Description to identify the specific error. This table uses “— —” to indicate bytes which are not applicable to the purposes of this document.

Sensor Type)	Sensor Number	Event Description	Event Explanation
<b>0C</b>	<b>10</b>		
		E7 01 40 <sup>a, b</sup>	Correctable ECC Error
		E7 01 <sup>a, b</sup>	Uncorrectable ECC Error
<b>10</b>	<b>02</b>		
		E7 00 FF FF	Correctable Memory Errors Disabled
		E7 41 00 00	Correctable Bus Errors Disabled
<b>12</b>	<b>08</b>		
		E7 01 FF FF	System Boot
<b>13</b>	<b>03</b>		
		E7 02 FF FF	I/O Channel Check NMI Detected
<b>13</b>	<b>04</b>		
		E7 48 09 <sup>d, e</sup>	Address Parity Error
		E7 48 01 FF	Request Parity Error
		E7 48 0A <sup>d</sup>	BINIT, driven by processor
		E7 48 0A <sup>d</sup>	Software NMI
		E7 48 0C <sup>d, e</sup>	Protocol Violation
		E7 48 0e <sup>e</sup>	BERR host bus generic error
		E7 47 00 FF	Correctable Data Error
E7 48 0F <sup>d, e</sup>	Uncorrectable Data Error		
<b>13</b>	<b>06</b>		
		E7 48 15 <sup>e</sup>	Data Parity Error on Transmit Cycle
		E7 48 16 <sup>e</sup>	Address Parity Error
		E7 48 04 <sup>e</sup>	Inbound Timeout Error
		E7 48 05 <sup>e</sup>	Target Abort
		E7 04 00 <sup>e</sup>	Nonspecific Data Parity, PB64 as master
		E7 05 00 <sup>e</sup>	Unknown System Error
E7 44 03 <sup>e</sup>	Nonspecific Data Parity		

**Notes:**

- a: 00h for Left Memory Carrier, 01h for Right Memory Carrier
- b: Hex reference designator or “J-number” of Memory DIMM. For example, 0Dh (translates to 13 in decimal), indicates the DIMM in slot J13
- c: 00h for Left Coherency Filter, 01h for Right Coherency Filter
- d: 00h for Left P6 Bus, 01h for Right P6 Bus, 02h for P6 I/ Bus
- e: C8h for Segment A, D0h for Segment B, D8h for Segment C, C0h for Segment D

## F.5 OCPRF100 POST Codes

The Sensor Type is 0F for all POST errors. To decode a POST error message, use the last two bytes in the Event Description to identify the specific error. The first two bytes, indicated by

“— —“ are not relevant to identifying the error.

Event Description	Event Explanation
— — 00 20	Failure fixed disk
— — 00 82	Baseboard Management Controller failed to function
— — 00 84	Switch fault on PCI hot-plug slot Px
— — 01 82	Front Panel Controller failed to function
— — 01 84	Hot-plug switches overridden by jumper or setup
— — 02 82	Power Share Controller failed to function
— — 05 82	Hot-swap Controller failed to function
— — 08 81	Watchdog timer failed on last boot
— — 10 02	Stuck key
— — 10 81	Server management interface failed to function
— — 10 82	Right Processor 4 failed BIST
— — 11 02	Keyboard error
— — 11 82	Right Processor 3 failed BIST
— — 12 82	Right Processor 2 failed BIST
— — 13 02	Keyboard locked – Unlock key switch
— — 13 82	Right Processor 1 failed BIST
— — 15 82	Left Processor 3 failed BIST
— — 16 82	Left Processor 2 failed BIST
— — 17 82	Left Processor 1 failed BIST
— — 20 02	Monitor type does not match CMOS – Run Setup
— — 20 82	Right Processor 4 internal error (IERR) failure
— — 21 82	Right Processor 3 internal error (IERR) failure
— — 22 82	Right Processor 2 internal error (IERR) failure
— — 23 82	Right Processor 1 internal error (IERR) failure
— — 24 82	Left Processor 4 internal error (IERR) failure
— — 25 82	Left Processor 3 internal error (IERR) failure
— — 26 82	Left Processor 2 internal error (IERR) failure
— — 27 82	Left Processor 1 internal error (IERR) failure
— — 30 02	System RAM failed at offset
— — 30 82	Right Processor 4 thermal trip failure
— — 31 02	Shadow RAM failed at offset
— — 31 82	Right Processor 3 thermal trip failure
— — 32 02	Extended RAM failed at offset
— — 32 82	Right Processor 2 thermal trip failure

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Event Description	Event Explanation
— — 33 82	Right Processor 1 thermal trip failure
— — 34 82	Left Processor 4 thermal trip failure
— — 35 82	Left Processor 3 thermal trip failure
— — 36 82	Left Processor 2 thermal trip failure
— — 37 82	Left Processor 1 thermal trip failure
— — 40 82	Right Processor 4 disabled
— — 41 82	Left Processor 4 failed BIST
— — 41 82	Right Processor 3 disabled
— — 42 82	Right Processor 2 disabled
— — 43 82	Right Processor 1 disabled
— — 44 82	Left Processor 4 disabled
— — 45 82	Left Processor 3 disabled
— — 46 82	Left Processor 2 disabled
— — 47 82	Left Processor 1 disabled
— — 4B 81	BMC in update mode
— — 50 02	System battery is dead – Replace and run Setup
— — 50 81	NVRAM cleared by jumper
— — 50 82	Right Processor 4 failed FRB Level 3 timer
— — 51 02	System CMOS checksum bad – Default configuration used
— — 51 82	Right Processor 3 failed FRB Level 3 timer
— — 52 81	ESCD data cleared
— — 52 82	Right Processor 2 failed FRB Level 3 timer
— — 53 81	Password cleared by jumper
— — 53 82	Right Processor 1 failed FRB Level 3 timer
— — 54 82	Left Processor 4 failed FRB Level 3 timer
— — 55 82	Left Processor 3 failed FRB Level 3 timer
— — 56 82	Left Processor 2 failed FRB Level 3 timer
— — 57 82	Left Processor 1 failed FRB Level 3 timer
— — 60 02	System timer error
— — 60 81	Unable to apply BIOS update for Right Processor 4
— — 60 82	Right Processor 4 failed initialization
— — 61 81	Unable to apply BIOS update for Right Processor 3
— — 61 82	Right Processor 3 failed initialization
— — 62 81	Unable to apply BIOS update for Right Processor 2
— — 62 82	Right Processor 2 failed initialization
— — 63 81	Unable to apply BIOS update for Right Processor 1
— — 63 82	Right Processor 1 failed initialization
— — 64 81	Unable to apply BIOS update for Left Processor 4
— — 64 82	Left Processor 4 failed initialization
— — 65 81	Unable to apply BIOS update for Left Processor 3
— — 65 82	Left Processor 3 failed initialization
— — 66 81	Unable to apply BIOS update for Left Processor 2
— — 66 82	Left Processor 2 failed initialization
— — 67 81	Unable to apply BIOS update for Left Processor 1
— — 67 82	Left Processor 1 failed initialization
— — 68 81	Right Processor 4 L2 cache failed
— — 69 81	Right Processor 3 L2 cache failed
— — 6A 81	Right Processor 2 L2 cache failed

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Event Description	Event Explanation
— — 6B 81	Right Processor 1 L2 cache failed
— — 6C 81	Left Processor 4 L2 cache failed
— — 6D 81	Left Processor 3 L2 cache failed
— — 6E 81	Left Processor 2 L2 cache failed
— — 6F 81	Left Processor 1 L2 cache failed
— — 70 02	Real-time clock error
— — 70 81	BIOS does not support current stepping for Right Processor 4
— — 70 82	Left memory carrier failed
— — 71 02	Check date and time settings
— — 71 81	BIOS does not support current stepping for Right Processor 3
— — 71 82	Right memory carrier failed
— — 72 81	BIOS does not support current stepping for Right Processor 2
— — 72 82	DIMM not fully configured – Left Jx
— — 73 81	BIOS does not support current stepping for Right Processor 1
— — 73 82	DIMM not fully configured – Right Jx
— — 74 81	BIOS does not support current stepping for Left Processor 4
— — 74 82	Memory error detected in DIMM Jx
— — 75 81	BIOS does not support current stepping for Left Processor 3
— — 75 82	Memory error detected in DIMM Right Jx
— — 76 81	BIOS does not support current stepping for Left Processor 2
— — 76 82	DIMM size mismatch
— — 77 81	BIOS does not support current stepping for Left Processor 1
— — 80 02	Previous boot incomplete – Default configuration used
— — 80 81	PB64 failed to respond
— — 80 82	Coherency filter failed left data test
— — 81 02	Memory size found by POST differed from EISA CMOS
— — 81 81	CPUID, processor steppings are different
— — 81 82	Coherency filter failed right data test
— — 82 81	L2 cache size mismatch
— — 86 81	Processor families are different
— — 90 82	Coherency filter failed left address test
— — 91 82	Coherency filter failed right address test
— — 93 82	Coherency filter size mismatch
— — 97 02	Base memory error / extended memory error
— — B0 02	Diskette drive A error
— — B1 02	Diskette drive B error
— — B2 02	Incorrect drive A type – Run Setup
— — B3 02	Incorrect drive B type – Run Setup
— — D0 02	System cache error – Cache disabled
— — F0 02	CPU ID
— — F4 02	EISA CMOS not writeable
— — F5 02	DMA test failed
— — F6 02	Software NMI failed
— — F7 02	Fail-safe timer NMI failed

## Appendix G SC450NX Tables

The tables in this Appendix provide translations for SEL viewer data on the SC450NX server platform. See Table 2 in Section 3 for a description of each field.

**Note:** Data is not provided for the EmvRev field. This field is reserved for future use and currently provides no valuable information.

### G.1 SC450NX Generator ID Codes

Generator ID	Description
11 00	BIOS
20 00	BMC
28 00	ICMB
C0 00	HSC
D8 00	PSC

### G.2 SC450NX Sensor Codes

Sensor Type	Sensor Number	Sensor Name
<b>01</b>		<b>Temperature</b>
	14	Baseboard Temperature 1
	15	Baseboard Temperature 2
	16	Processor 1 Core Temperature
	17	Processor 2 Core Temperature
	18	Processor 3 Core Temperature
	19	Processor 4 Core Temperature
	2D	Power Share Board Temperature
<b>02</b>		<b>Voltage</b>
	01	Baseboard 5v
	02	Baseboard 12v
	03	Baseboard 3.3v
	04	Baseboard -12v
	05	Processor 1 VRM
	06	Processor 2 VRM
	07	Processor 3 VRM
	08	Processor 4 VRM
	09	Processor 1-2 Cache VRM
	0A	Processor 3-4 Cache VRM
	0B	GTL Logic 1.5v
	0C	Logic 2.5v
	0D	SCSI-W A1
	0E	SCSI-W A2

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Sensor Type	Sensor Number	Sensor Name
<b>02</b>		<b>Voltage</b>
	0F	SCSI-W A3
	10	SCSI-W B1
	11	SCSI-W B2
	12	SCSI-W B3
	13	SCSI-n
<b>04</b>		<b>Fan</b>
	1A / 39 <sup>1</sup>	Backplane Fan 1
	1B / 3A	Backplane Fan 2
	1C / 3B	Backplane Fan 3
	1D / 3C	Backplane Fan 4
	1E / 3D	Backplane Fan 5
	1F / 3E	Backplane Fan 6
	20 / 3F	Processor Fan 1
	21 / 40	Processor Fan 2
	22	Power Supply Fan 1
	23	Power Supply Fan 2
	24	Power Supply Fan 3
	0D	Backplane Fan 1 Speed
	0E	Backplane Fan 2 Speed
<b>05</b>		<b>Physical Security (Chassis Intrusion)</b>
	33	Chassis Intrusion
<b>06</b>		<b>Secure Mode Violation Attempt</b>
	34	Secure Mode Violation Attempt
<b>07</b>		<b>Processor</b>
	27	Processor 1 Status
	28	Processor 2 Status
	29	Processor 3 Status
	2A	Processor 4 Status
	EF	See BIOS Table below
<b>08</b>		<b>Power Supply</b>
	2E	Power Supply 1
	2F	Power Supply 2
	30	Power Supply 3
<b>09</b>		<b>Power Unit</b>
	25	Redundancy Lost
	26	Power Unit
<b>0C</b>		<b>Memory</b>
	EF	See BIOS Table below

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Sensor Type	Sensor Number	Sensor Name
<b>0D</b>		<b>Drive Bay</b>
	01	Drive Slot 0 Status
	02	Drive Slot 1 Status
	03	Drive Slot 2 Status
	04	Drive Slot 3 Status
	05	Drive Slot 4 Status
	06	Drive Slot 5 Status
	07	Drive Slot 0 Presence
	08	Drive Slot 1 Presence
	09	Drive Slot 2 Presence
	0A	Drive Slot 3 Presence
	0B	Drive Slot 4 Presence
	0C	Drive Slot 5 Presence
<b>0F</b>		<b>POST Error</b>
	32	See POST Table below
<b>11</b>		<b>Watchdog</b>
	37	BMC Watchdog
<b>12</b>		<b>Critical Interrupt</b>
	EF	See BIOS Table below
<b>13</b>		<b>Critical Interrupt</b>
	28	See BIOS Table below
	29	See BIOS Table below
	36	Front Panel NMI
	EF	See BIOS Table below
<b>15</b>		<b>Module / Board</b>
	2B	Processor Cache 1-2 voltage Mismatch
	2C	Processor Cache 3-4 voltage Mismatch
<b>20</b>		<b>POST</b>
	0F	See BIOS Table below
<b>C0-FF</b>		<b>OEM Reserved</b>
	35	SMI Signal State
	38	NMI Signal State

**Note:**

The baseboard and processor fans in the SC450NX server system may be analog or digital and the sensor number varies according to that. For example if the Sensor Type is "Fan" and the sensor Number is "#39", the fan is a digital fan and if the number is "#1A#", the fan is an analog fan.



### G.3 SC450NX Event Description Codes

The purpose of the Event Description field varies, depending on the Generator ID. When the Generator ID is

- 20 00
- 22 00
- C0 00
- D8 00

the first byte of the Event Description is used to indicate the type of event that occurred, such as the crossing of a threshold or the removal of a device. When the Generator ID is 11 00, the Event Message was generated from the BIOS or from POST and Table J.4 or J.5 should be used to determine the definition of the Event Message. Refer to Section 3 for a complete explanation on table usage. Each “—” in the table below indicates a byte that may be disregarded.

Event Description	Event Type	Definition
01 — — —	N/A	Threshold crossed
02 — — —	N/A	Transition to idle, active, or busy
03 — — —	N/A	State asserted or deasserted
04 — — —	N/A	Predictive failure asserted or deasserted
05 — — —	N/A	Limit exceeded
06 — — —	N/A	Performance lag
07 — — —	N/A	Presence, Disabled, IERR, Thermal Trip, or FRB3
08 — — —	N/A	Device added or removed
09 — — —	N/A	Device enabled or disabled
0A — — —	N/A	Transition to running or test, on or off-line
EB — — —	N/A	Redundancy lost, regained, degraded
E7 — — —	07	Presence, Disabled, IERR, Thermal Trip, FRB3
E7 — — —	08	Presence or fault
E7 — — —	09	Power Off or Power Cycle, 240VA, Reserve, Lost AC
E7 — — —	49	BIOS WD Reset, OS WD Reset, OS WD Shutdown, Power down, Power off

### G.4 SC450NX BIOS Codes

To decode a BIOS error message, locate the Sensor Type and Sensor Number under which the error falls. Then use the Event Description to identify the specific error. This table uses “— —” to indicate bytes which are not applicable to the purposes of this document.

Sensor Type	Sensor Number	Event Description	Event Explanation
07	EF		
		E7 42 Processor# —	BIST failure
0C	EF		
		00 FF — —	Front Panel NMI
		E7 02 — —	Memory parity error
		E7 40 Card# DIMM#	Single bit memory error
		E7 41 Card# DIMM#	Multi bit memory error

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Sensor Type	Sensor Number	Event Description	Event Explanation
12	EF		
		E7 01 — —	System Boot Event
		E7 00 — —	System Reconfiguration
13	EF		
		E7 00 FF FF	Floating point error
		E7 01 FF FF	Bus time-out NMI
		E7 02 FF FF	I/O channel check NMI
		E7 03 FF FF	Software NMI
		E7 04 FF FF	PCI PERR
		E7 05 FF FF	PCI SERR
		E7 44 00 14	BINIT Expander Parity
		E7 44 00 26	PCI DATA Parity Error
		E7 44 FF 10	AERR Address Parity Error
		E7 44 FF 15	BINIT Response Parity
		E7 44 FF 16	BINIT Request parity
		E7 44 FF FF	NMI PERR
		E7 44 nn <sup>1</sup> 00	PCI PERR asserted
		E7 45 00 13	BINIT Protocol Violation
		E7 45 00 18	SERR Protocol Violation
		E7 45 00 19	SERR Parity on Transmit
		E7 45 00 20	SERR parity on Receive
		E7 45 00 21	SERR Parity on address
		E7 45 00 22	SERR Inbound Timeout
		E7 45 00 23	SERR BUS parity
		E7 45 FF 11	BERR HOST BUS generic
		E7 45 FF 12	BINIT Hostbus Hardfail
		E7 45 FF FF	NMI SERR
E7 45 nn <sup>1</sup> 00	PCI SERR asserted		
E7 48 — —	BINIT Hostbus ECC		
E8 60 FF FF	IMB error		
20	0F		
		32 41 lsb msb <sup>2</sup>	POST Code

**Notes:**

1. nn indicates that bits [7:3] contain the PCI device number and bits [2:0] contain the PCI function number
2. lsb msb indicates the order in which the bytes are logged in the SEL. Lsb is the "least significant byte" and msb is the "most significant byte." To interpret these codes, refer to the POST code table below used to determine the message. For example, if the full Event Description is 32 41 11 02, refer to the POST code table entry for 11 02 (Keyboard error)

## G.5 SC450NX POST Codes

The Sensor Type is 0F for all POST errors. To decode a POST error message, use the last two bytes in the Event Description to identify the specific error. The first two bytes, indicated by “— —” are not relevant to identifying the error.

**Note:** To keep similar events together, this table is sorted by the fourth byte of the Event Description.

Event Description	Event Explanation
— — 00 02	Failure Fixed Disk
— — 00 0A	Intelligent System Monitoring Chassis opened
— — 00 81	Processor 0 failed BIST
— — 01 04	Invalid System Configuration Data - run configuration utility
— — 01 06	Device configuration changed
— — 01 81	Processor 1 failed BIST
— — 01 0A	Intelligent System Monitoring Forced Shutdown
— — 02 06	Configuration error - device disabled
— — 02 81	Processor 2 failed BIST
— — 03 81	Processor 3 failed BIST
— — 03 04	Resource Conflict
— — 04 04	Resource Conflict
— — 04 05	Resource Conflict
— — 04 81	Processor 0 Internal Error (IERR) failure
— — 05 04	Expansion ROM not initialized
— — 05 05	Expansion ROM not initialized
— — 05 81	Processor 1 Internal Error (IERR) failure
— — 06 04	Warning: IRQ not configured
— — 06 05	Warning: IRQ not configured
— — 06 81	Processor 0 Thermal Trip failure
— — 07 81	Processor 1 Thermal Trip failure
— — 08 81	Watchdog Timer failed on last boot, BSP switched.
— — 0A 81	Processor 1 failed initialization on last boot
— — 0B 81	Processor 0 failed initialization on last boot
— — 0C 81	Processor 0 disabled
— — 0D 81	Processor 1 disabled
— — 0E 81	Processor 0 failed FRB Level 3 timer
— — 0F 81	Processor 1 failed FRB Level 3 timer
— — 10 02	Stuck Key
— — 10 81	Server Management Interface failed to function
— — 11 02	Keyboard error
— — 11 81	System Power-Down on last boot. FRB-2 count exhausted
— — 12 02	Keyboard Controller Failed
— — 13 02	Keyboard locked - Unlock key switch
— — 14 81	Processor 2 Internal Error (IERR) failure
— — 15 81	Processor 3 Internal Error (IERR) failure
— — 16 81	Processor 2 Thermal Trip failure
— — 17 81	Processor 3 Thermal Trip failure
— — 1A 81	Processor 2 failed initialization on last boot
— — 1B 81	Processor 3 failed initialization on last boot

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Event Description	Event Explanation
— — 1C 81	Processor 2 disabled
— — 1D 81	Processor 3 disabled
— — 1E 81	Processor 2 failed FRB Level 3 timer
— — 1F 81	Processor 3 failed FRB Level 3 timer
— — 20 02	Monitor type does not match CMOS - Run SETUP
— — 20 81	IOP subsystem is not functional
— — 21 81	2:1 core to bus speed ratio: Processor cache disabled
— — 23 81	VPD and backup are corrupted
— — 24 81	VPD was not successfully restored from backup
— — 25 81	VPD was successfully restored from backup
— — 28 81	Processor 2 Internal Error (IERR) failure
— — 29 81	Processor 3 Internal Error (IERR) failure
— — 30 02	System RAM Failed at offset xx
— — 30 81	Processor 2 Thermal Trip failure
— — 31 02	Shadow Ram Failed at offset xx
— — 31 81	Processor 3 Thermal Trip failure
— — 32 02	Extended RAM Failed at offset xx
— — 33 02	Memory type mix
— — 34 02	Memory ECC single
— — 35 02	Memory ECC multiple
— — 38 81	Processor 2 failed FRB Level 3 timer
— — 39 81	Processor 3 failed FRB Level 3 timer
— — 40 81	Processor 2 disabled
— — 41 81	Processor 3 disabled
— — 4B 81	BMC Update Mode
— — 50 02	System battery is dead – Replace and run SETUP
— — 50 81	NVRAM Clear By Jumper
— — 51 02	System CMOS checksum bad – Default configuration used
— — 51 81	NVRAM Checksum Error, NVRAM cleared
— — 52 81	NVRAM Data Invalid, NVRAM cleared
— — 53 81	Configuration clear via BIOS Setup option
— — 60 02	System timer error
— — 62 01	BIOS unable to apply BIOS update to processor 1
— — 63 01	BIOS unable to apply BIOS update to processor 2
— — 64 01	BIOS does not support current stepping for processor 1
— — 65 01	BIOS does not support current stepping for processor 2
— — 70 02	Real time clock error
— — 71 02	Real time clock invalid date
— — 81 81	Mismatch among Processors Detected
— — 97 02	ECC Memory error in base (extended) memory test in Bank xx
— — B0 02	Diskette drive A error
— — B1 02	Diskette drive B error
— — B2 02	Incorrect Drive A type – run SETUP
— — B3 02	Incorrect Drive B type – run SETUP
— — D0 02	System cache error – Cache disabled
— — F5 02	DMA Test Failed
— — F6 02	Software NMI Failed
— — F7 02	Fail-safe timer NMI failed

## Appendix H SPKA4 Tables

The tables in this Appendix provide translations for SEL viewer data on the SPKA4 server platform. See Table 2 in Section 3 for a description of each field.

**Note:** Data is not provided for the EmvRev field. This field is reserved for future use and currently provides no valuable information.

### H.1 SPKA4 Generator ID Codes

Generator ID	Description
11 00	BIOS
20 00	BMC
22 00	FPC
C0 00	HSC #1
C2 00	HSC #2

### H.2 SPKA4 Sensor Codes

Sensor Type	Sensor Number	Sensor Name
01		<b>Temperature</b>
	01	Backplane Temperature
	1C	Baseboard Temperature 1
	1D	Baseboard Temperature 2
	1F	Fan Board Temperature
	1E	PDB Temperature
	20	Processor 1 Core Temperature
	21	Processor 2 Core Temperature
	22	Processor 3 Core Temperature
	23	Processor 4 Core Temperature
02		<b>Voltage</b>
	01	Baseboard 1.5 Volt
	02	Baseboard 1.8 Volt
	03	Baseboard 2.5 Volt
	04	Baseboard 3.3 Volt
	05	Baseboard 3.3 Volt Standby
	06	Baseboard 5 Volt
	07	Baseboard 12 Volt
	08	Baseboard -12 Volt
	09	Processor 1 VRM
	0A	Processor 2 VRM
	0B	Processor 3 VRM
	0C	Processor 4 VRM
	0D	Processor 1 – 2 Cache VRM
	0E	Processor 3 – 4 Cache VRM
0F	Processor 1 OCVR	
10	Processor 2 OCVR	

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Sensor Type	Sensor Number	Sensor Name
	11	Processor 3 OCVR
	12	Processor 4 OCVR
	13	Peripheral Bay 5 Volt
	14	Peripheral Bay 12 Volt
	15	Spare Voltage
	16	LVDS SCSI Channel 1 Terminator 1
	17	LVDS SCSI Channel 1 Terminator 2
	18	LVDS SCSI Channel 2 Terminator 1
	19	LVDS SCSI Channel 2 Terminator 2
	1A	SCSI Wide Upper Segment Terminator
	1B	SCSI Wide Lower Segment SCSI Narrow Terminator
<b>04</b>		
		<b>Fan</b>
	0C	Backplane FAN 1 speed
	0D	Backplane FAN 2 speed
	2C	Tach Fan 1
	2D	Tach Fan 2
	2E	Tach Fan 3
	2F	Tach Fan 4
	30	Tach Fan 5
	31	Tach Fan 6
	32	Tach Fan 7
	33	Tach Fan 8
	34	Digital Fan 1
	35	Digital Fan 2
	36	Digital Fan 3
	37	Digital Fan 4
	38	Digital Fan 5
	39	Digital Fan 6
	3A	Digital Fan 7
	3B	Digital Fan 8
	3C	Aux PDB Tach Fan
<b>05</b>		
		<b>Physical Security</b>
	50	Chassis Intrusion
<b>06</b>		
		<b>Security Violation Attempt</b>
	51	Secure Mode Violation Attempt
	56	EMP Password
<b>07</b>		
		<b>Processor</b>
	42	Processor 1 Status
	43	Processor 2 Status
	44	Processor 3 Status
	45	Processor 4 Status
<b>08</b>		
		<b>Power Supply</b>

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Sensor Type	Sensor Number	Sensor Name
	3D	Power Supply 1
	3E	Power Supply 2
	3F	Power Supply 3
<b>09</b>		
		<b>Power Unit</b>
	40	Power Unit
	41	Redundancy
<b>0F</b>		
		<b>POST Error</b>
	4F	See POST Table below
<b>11</b>		
		<b>Watchdog</b>
	55	BMC Watchdog
<b>13</b>		
		<b>Critical Interrupt</b>
	54	FP NMI
<b>15</b>		
		<b>Module / Board</b>
	46	Processor 1 – 2 Cache Voltage Mismatch
	47	Processor 3 – 4 Cache Voltage Mismatch
	48	Missing Processor or Terminator
<b>21</b>		
		<b>Slot / Connector</b>
	49	Hot Plug PCI Slot 1
	4A	Hot Plug PCI Slot 2
	4B	Hot Plug PCI Slot 3
	4C	Hot Plug PCI Slot 4
	4D	Hot Plug PCI Slot 5
	4E	Hot Plug PCI Slot 6
<b>C0</b>		
		<b>OEM C0</b>
	52	SMI Signal State
	53	NMI Signal State
<b>C7</b>		
		<b>OEM C7</b>
	24	Fan Boost BB Temp 1
	25	Fan Boost BB temp 2
	26	Fan Boost PDB Temp 2
	27	Fan Boost Fan Board Temp
	28	Fan Boost Proc 1 Core Temp
	29	Fan Boost Proc 2 Core Temp
	2A	Fan Boost Proc 3 Core Temp
	2B	Fan Boost Proc 4 Core temp
<b>0D</b>		
		<b>Drive Slot</b>
	02	Drive Slot 0 status
	03	Drive Slot 1 Status

Sensor Type	Sensor Number	Sensor Name
0D	04	Drive Slot 2 Status
	05	Drive Slot 3 status
		<b>Drive Slot</b>
	06	Drive Slot 4 Status
	07	Drive Slot 0 Presence
	08	Drive Slot 1 Presence
	09	Drive Slot 2 Presence
	0A	Drive Slot 3 Presence
	0B	Drive slot 4 Presence

### H.3 SPKA4 Event Description Codes

The purpose of the Event Description field varies, depending on the Generator ID. When the Generator ID is

- 20 00
- 22 00
- C0 00
- C2 00

the first byte of the Event Description is used to indicate the type of event that occurred, such as the crossing of a threshold or the removal of a device. When the Generator ID is 11 00, the Event Message was generated from the BIOS or from POST and the BIOS or POST tables should be used. Refer to Section 3 for a complete explanation on table usage. Each “—” in the tables indicates a byte that may be disregarded.

Event Description	Definition
01 — — —	Threshold crossed
03 — — —	State Asserted, State Deasserted
06 — — —	Performance Met or Lags
0B — — —	Redundancy Lost
6F — — —	Presence, Failure, Disabled, Predictive fail (fan fail), Watchdog Expired, Hard Reset, Power Down, Power Cycle

### H.4 SPKA4 BIOS Codes

To decode a BIOS error message, locate the Sensor Type and Sensor Number under which the error falls. Then use the Event Description to identify the specific error. This table uses “— —” to indicate bytes which are not applicable to the purposes of this document.

Sensor Type	Sensor Number <sup>1</sup>	Event Description	Event Explanation
0C	XX		
		6F A0, card/DIMM#, Syndrome	Single bit memory error
		6F 81, card/DIMM#	Multi-bit memory error
13	XX		
		6F 07 FF FF	System Bus Correctable Error <sup>2</sup>



Sensor Type	Sensor Number <sup>1</sup>	Event Description	Event Explanation
		6F 08 FF FF	System Bus Uncorrectable Error <sup>3</sup>
		6F A4, BUS#, Device/Func	PCI PERR
		6F A5, BUS#, Device/Func	PCI SERR <sup>4</sup>
		6F 05 FF FF	PCI SERR (unknown source)
<b>10</b>	<b>XX</b>		
		6F 00 FF FF	ECC Logging Disabled
		6F 01 FF FF	IMB Error Logging Disabled
<b>07</b>	<b>4f</b>		
		6F 0A, LSB Port 80, MSB Port 80	FRB-2 Error
		4F 03 0F, LSB Port Err, MSB POST Err	POST Error

**Notes:**

1. Sensor # = 0xx (don't care). The system BIOS "sensors" are just logical entities that generate events. BIOS should make sure that each different combination of sensor type (e.g., memory) and event type (e.g., sensor-specific) have a different sensor number. Software should ignore these values.
2. Errors reported by this event include Processor Bus Correctable Error, IMB Bus Retry Error and IMB Bus Timeout Error.
3. Errors reported by this event include Processor Bus Uncorrectable Error, Processor Bus AERR#, Processor Bus BERR#, Processor Bus BINIT#, Processor Bus Protocol Error, IMB Bus Parity Error, IMB Bus Sequence Error, IMB Bus Generic Error, IMB Bus Command Error, and IMB Bus Data Error.
4. Errors reported by this event include PCI SERR#, Received Target Abort, and Address Parity Error.

## H.5 SPKA4 POST Codes

The Sensor Type is 0F for all POST errors. To decode a POST error message, use the last two bytes in the Event Description to identify the specific error. The first two bytes, indicated by

“— —“ are not relevant to identifying the error.

Event Description	Event Explanation
— — 00 08	PCI I/O Port Conflict

## Appendix I T440BX Tables

The tables in this Appendix provide translations for SEL viewer data on the T440BX server platform. See Table 2 in Section 3 for a description of each field.

**Note:** Data is not provided for the EmvRev field. This field is reserved for future use and currently provides no valuable information.

### I.1 T440BX Generator ID Codes

Generator ID	Description
11 00	POST
20 00	BMC

### I.2 T440BX Sensor Codes

Sensor Type	Sensor Number	Sensor Name
<b>01</b>		<b>Temperature</b>
	17	Processor1 Temp
	19	Baseboard Temp1
<b>02</b>		<b>Voltage</b>
	01	Baseboard 5V
	02	Baseboard 3.3V
	03	Primary Processor
	05	Processor 2.5V
	06	5v Standby
	07	Baseboard SCSI-A Term1
	08	Baseboard SCSI-A Term2
	09	Baseboard SCSI Term3
	0A	Baseboard -12V
	0C	Processor 1.5V
	0D	Baseboard -5V
	0E	Baseboard 12
23	Processor1 VID	
<b>04</b>		<b>Fan</b>
	0F	Baseboard Fan0
	10	Baseboard Fan1
	11	Baseboard Fan2
	12	Processor Fan
<b>05</b>		<b>Physical Security (Chassis Intrusion)</b>
	26	Chassis Intrusion
<b>06</b>		<b>Secure Mode Violation Attempt</b>
	27	EMP password violation
	28	Secure Mode Violation Attempt (at the time of connecting to the server)

Sensor Type	Sensor Number	Sensor Name
<b>07</b>		<b>Processor</b>
	1B	Processor1 Status
<b>0C</b>		<b>Memory</b>
	1F	DIMM1 Presence
	20	DIMM2 Presence
	21	DIMM3 Presence
	EF	See BIOS Table D.4 below
<b>0F</b>		<b>POST Error</b>
	25	See POST Table D.5 below
<b>11</b>		<b>Watchdog</b>
	1D	Watchdog Event
<b>12</b>		<b>System Event</b>
	EF	See BIOS Table D.4 below
<b>13</b>		<b>Critical Interrupt</b>
	1E	Front Panel NMI
	EF	See BIOS Table D.4 below

### I.3 T440BX Event Description Codes

The purpose of the Event Description field varies, depending on the Generator ID. When the Generator ID is 20 00, the first byte of the Event Description is used to indicate the type of event that occurred, such as the crossing of a threshold or the removal of a device.

When the Generator ID is 11 00, the Event Message was generated from the BIOS or from POST and Table L.4 or L.5 should be used to determine the definition of the Event Message. Refer to Section 3 for a complete explanation on table usage.

Event Description	Event Type	Definition
01 — — —	N/A	Threshold crossed
02 — — —	N/A	Transition to idle, active, or busy
03 — — —	N/A	State asserted or deasserted
04 — — —	N/A	Predictive failure asserted or deasserted
05 — — —	N/A	Limit exceeded
06 — — —	N/A	Performance lag
07 — — —	N/A	Presence, Disabled, IERR, Thermal Trip, or FRB3
08 — — —	N/A	Device added or removed
09 — — —	N/A	Device enabled or disabled
0A — — —	N/A	Transition to running or test, on or off-line
EB — — —	N/A	Redundancy lost, regained, degraded

Event Description	Event Type	Definition
E7 — — —	07	Presence, Disabled, IERR, Thermal Trip, FRB3
E7 — — —	08	Presence or fault
E7 — — —	09	Power Off or Power Cycle, 240VA, Reserve, Lost AC
E7 — — —	49	BIOS WD Reset, OS WD Reset OS WD Shutdown, Power down, Power off

## I.4 T440BX BIOS Codes

To decode a BIOS error message, locate the Sensor Number under which the error falls and then use the first two bytes in the Event Description to identify the specific error.

Sensor Type	Sensor Number	Event Description	Event Explanation
12	EF		
		E7 01 — —	System Boot Event
		E7 00 — —	System Reconfiguration
0C	EF		
		E7 20 — —	Single Bit Memory Error
		E7 21 — —	Double Bit Memory Error
		E7 02 — —	Memory Parity Error
13	EF		
		E7 00 — —	Bus Timeout
		E7 02 — —	I/O CHK
		E7 03 — —	Software NMI
		E7 04 — —	PCI PERR
		E7 05 — —	PCI SERR

## I.5 T440BX POST Codes

The Sensor Type is 0F for all POST errors. To decode a POST error message, use the last two bytes in the Event Description to identify the specific error. The first two bytes, indicated by “— —” are not relevant to identifying the error.

**Note:** To keep similar events together, this table is sorted by the fourth byte of the Event Description.

Event Description	Event Explanation
— — 62 01	BIOS unable to apply BIOS update to processor 1
— — 63 01	BIOS unable to apply BIOS update to processor 2
— — 64 01	BIOS does not support current stepping for processor 1
— — 65 01	BIOS does not support current stepping for processor 2
— — 00 02	Failure Fixed Disk
— — 10 02	Stuck Key
— — 11 02	Keyboard error
— — 12 02	Keyboard Controller Failed
— — 13 02	Keyboard locked - Unlock key switch
— — 20 02	Monitor type does not match CMOS - Run SETUP

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Event Description	Event Explanation
— — 30 02	System RAM Failed at offset xx
— — 31 02	Shadow Ram Failed at offset xx
— — 32 02	Extended RAM Failed at offset xx
— — 50 02	System battery is dead - Replace and run SETUP
— — 51 02	System CMOS checksum bad - Default configuration used
— — 60 02	System timer error
— — 70 02	Real time clock error
— — 97 02	ECC Memory error in base (extended) memory test in Bank xx
— — B2 02	Incorrect Drive A type - run SETUP
— — B3 02	Incorrect Drive B type - run SETUP
— — D0 02	System cache error - Cache disabled
— — F5 02	DMA Test Failed
— — F6 02	Software NMI Failed
— — 01 04	Invalid System Configuration Data - run configuration utility
— — 03 04	Resource Conflict
— — 04 04	Resource Conflict
— — 05 04	Expansion ROM not initialized
— — 06 04	Warning: IRQ not configured
— — 04 05	Resource Conflict
— — 05 05	Expansion ROM not initialized
— — 06 05	Warning: IRQ not configured
— — 01 06	Device configuration changed
— — 02 06	Configuration error - device disabled
— — 00 81	Processor 0 failed BIST
— — 01 81	Processor 1 failed BIST
— — 04 81	Processor 0 Internal Error (IERR) failure
— — 05 81	Processor 1 Internal Error (IERR) failure
— — 06 81	Processor 0 Thermal Trip failure
— — 07 81	Processor 1 Thermal Trip failure
— — 08 81	Watchdog Timer failed on last boot, BSP switched.
— — 0A 81	Processor 1 failed initialization on last boot.
— — 0B 81	Processor 0 failed initialization on last boot.
— — 0C 81	Processor 0 disabled, system in Uni-processor mode
— — 0D 81	Processor 1 disabled, system in Uni-processor mode
— — 0E 81	Processor 0 failed FRB Level 3 timer
— — 0F 81	Processor 1 failed FRB Level 3 timer
— — 10 81	Server Management Interface failed to function
— — 20 81	IOP sub-system is not functional
— — 50 81	NVRAM Cleared by Jumper
— — 51 81	NVRAM Checksum Error, NVRAM cleared
— — 52 81	NVRAM Data Invalid, NVRAM cleared

## Appendix J Glossary

Term	Definition
BIOS	Basic Input Output System.
BSP	Boot Strap Processor.
BMC	Baseboard Management Controller.
Byte	An 8-bit quantity.
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the baseboard.
DIMM	Dual-inline Memory Module. Name for the plug in modules used to hold the system's DRAM (Dynamic Random Access Memory).
ECC	Error-correcting Code. Refers to a set of additional bits on system RAM that are used to provide a check code that is used to verify memory data integrity.
EvMRev	Event Message Revision
FRB	Fault Resilient Booting. A term used to describe system features and algorithms that improve the likelihood of the detection of, and recovery from, processor failures in a multiprocessor system.
FRU	Field Replaceable Unit.
HSC	Hot-Swap Controller. Name for the microcontroller that implements the SAF-TE command set and controls the fault lights and drive power on a N440BX Backplane.
IERR	Internal Error. A signal from the Pentium® processors indicating an internal error condition.
IPMB	Intelligent Platform Management Bus. Name for the architecture, protocol, and implementation of a special bus that interconnects the baseboard and chassis electronics and provides a communications media for system platform management information.
IPMI	Intelligent Platform Management Interface. This protocol is used for communication between microcontrollers, System Management Software, and other 'intelligent' devices on the IPMB.
NMI	Non-maskable Interrupt. The highest priority interrupt in the system, after SMI. This interrupt has traditionally been used to notify the operating system fatal system hardware error conditions, such as parity errors and unrecoverable bus errors.
NVRAM	Non-Volatile RAM.
PERR	Parity Error. A signal on the PCI bus that indicates a parity error on the bus.
POST	Power On Self Test.
PSC	Power Share Controller.
SAF-TE	SCSI Accessed Fault-tolerant Enclosure specification. Describes a set of SCSI commands whereby drive fault status can be sent to an enclosure for the purpose of presenting that fault information with external indicators, such as fault lights. Other commands are provided so certain management information about the enclosure, such as temperature, voltage, number of drive bays, power status, etc., can be retrieved.
SCU	System Configuration Utility.
SDR	Sensor Data Record. A data record that provides platform management sensor type, locations, event generation, and access information.
SEL	System Event Log. A non-volatile storage area and associated interfaces for storing system platform event information for later retrieval.
SERR	System Error. A signal on the PCI bus that indicates a 'fatal' error on the bus.
SM	Server Management.
SMI	System Management Interrupt.
SMS	Server Management Software.
SSU	System Setup Utility.

