SPKA4 MP Server System

Technical Product Specification

Revision 1.2

July 2000

Enterprise Platforms Group
Server Products Division

Revision History

Date	Revision Number	Modifications
July 2000	1.2	Initial Release

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1. Introduction

This product specification details the features of the SPKA4 MP server system. Low cost, time to market, modularity, and utilization for multiple configurations are primary considerations in the design. The chassis has user friendly features, and is accessible and serviceable.

The SPKA4 MP server system also incorporates features for high availability servers. This includes power and cooling systems with optional redundancy, hot-swap or easy to replace fans, hot-plug PCI slots, and a mass storage system with hot-swappable hard drives. These are key components for increasing the availability of the server. Since the fans and power supplies typically have the lowest Mean Time Between Failure (MTBF) specifications, the optional redundancy of these components will permit the system to continue to operate with a failed fan or power supply and continue to operate, for a limited time, while replacing a power supply. With the use of RAID technology, the system can continue to operate with hard drive failures. The hot-plug hard drives allow a failed hard drive to be replaced while the system continues to operate.

This product specification details the following:

- SPKA4 chassis features.
- Power supply subsystem.
- Chassis cooling.
- Peripheral bays.
- Front panel.
- Baseboard.
- I/O and interconnects.
- System configuration.
- System certifications.
- Environmental limits.
- Reliability, serviceability, and availability.

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2. SPKA4 MP Server Chassis Feature Overview

2.1 Chassis Features

The SPKA4 MP server chassis is 12.25 inches wide, 18.06 inches high, and 25.25 inches deep in the pedestal configuration. The chassis is designed to be modular with a base unit with two easily removable units, one to hold the front panel and drive bays (C-tilt) and one to hold the baseboard and I/O panels (E-bay). The base section is U shaped and holds the power supplies and the power distribution board. The E-bay drops in at the rear of the base unit and the C-tilt drops in from the front. Two captive screws in the front cover fasten both the C-tilt and the E-bay to the base unit. The E-bay fans are plugged into a hot-swap fan holder and installed above the drives and in front of the E-bay. Three bays are supplied in the back of the chassis base unit for power supplies. There are two covers on the right side to provide EMI shielding. One cover provides tool-less access to the hot-plug PCI slots and allows a secondary cover to be removed to provide access to the rest of the baseboard electronics. The second (front) cover allows access to the hot-swappable cooling fans.

A pedestal kit (SKCBPEDMT), consisting of one top cover, one side cover, a pedestal bezel, and two feet, is utilized for pedestal applications.

A rack mount kit (SKCBRACKMT), consisting of two rails, two handles, four brackets, and a rack bezel, can be installed allowing the system to be mounted in a rack as a 7U-rack unit.

2.2 Hot-plug PCI

The system has six hot-plug PCI slots, which are accessible under the side/top access cover, and which can be removed, without tools, while the system continues to run. For each PCI slot, there is a thumb-latch to retain the PCI card, a push-button switch that informs the system software when it is pressed, and a pair of LEDs that show the state of the PCI slot.

2.3 Front Bezel Features

The front bezel is a multiple-part plastic molding. There is one key-lockable door covering the drive bays. The front panel indicator LEDs, power switch, sleep switch, reset switch, and NMI switch are on the upper right for the pedestal chassis.

2.4 Security

At the system level, a variety of security options are provided. A three-position key locks either the front part of the side access cover or the front part of the side access cover and the front bezel door. In addition, there are intrusion switches for the front and rear parts of the side access cover and provision for a small padlock on the drive bay (3.5") door. Provision for a Kensington* lock is provided in the rear panel.

2.5 I/O Panel

All input/output connectors are accessible at the back of the chassis. The built-in interfaces on the baseboard are mapped in the figure below.

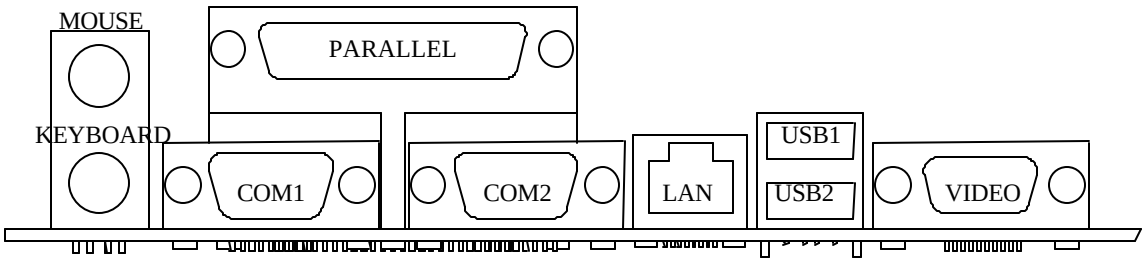

Figure 2-1: I/O Connectors

2.6 Chassis Dimensions

Table 2-1: System Dimensions

Configuration	Pedestal	Rack
Height	18.06 inches with feet	7U
Width	12.22 inches	Fits 19” standard rack
Depth	25.25 inches	25.25 inches
Clearance Front	12 inches	Rack must not restrict airflow
Clearance Rear	9 inches	Rack must not restrict airflow
Clearance Side	0 inches	NA
Weight	120 lb. maximum configuration	120 lb. maximum configuration

2.7 Chassis View

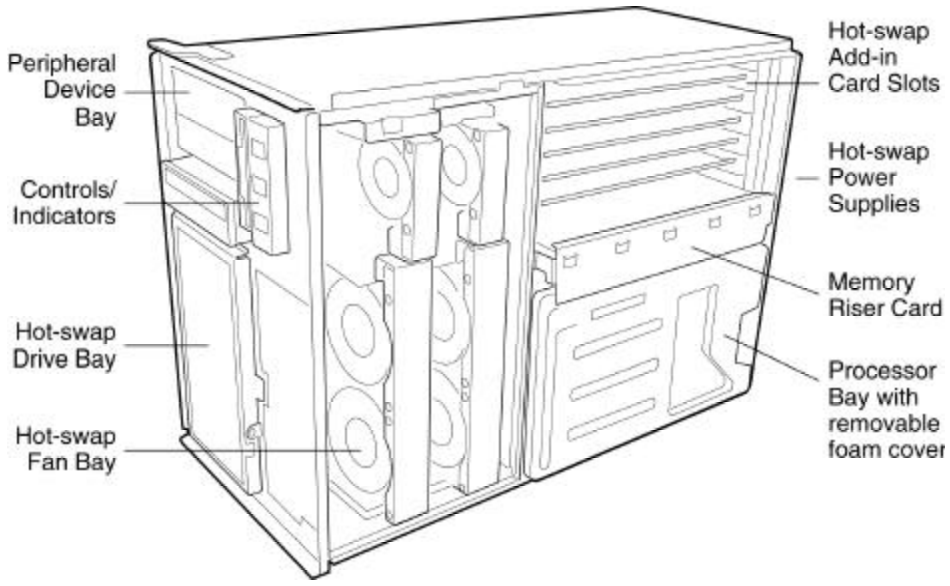

Figure 2-2: SPKA4 MP Server System Drawing with Side Panels and Front Panel Removed

Figure 2-3: SPKA4 MP Server System Photograph with Side Panels and Front Panel Removed

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3. Power Supply Subsystem

3.1 Power Supply Subsystem Feature Overview

This section defines the SSI compliant 375 watt SPKA4 power supply, a universal input switching power supply. The power supply is power factor corrected at AC input with forced current sharing and remote sense regulation at DC output. The supply can be used either singly or with its DC outputs paralleled with other identical supplies to form a redundant power system with hot swap replacement capability. The supply +5 VDC standby output will be present whenever AC power is applied. The power supply is rated to supply the following DC voltage levels:

- +3.3 VDC at 34 A.
- +5 VDC at 34 A.
- +12 VDC at 18 A peak 18.5 A <10mS.
- -12 VDC at 1.0 A.
- +5 V standby at 2 A.

Maximum continuous power output of any combined DC loading shall not exceed 375 watts.

The SPKA4 power subsystem is a modular design. The system may be configured with one, two, or three power supplies. These configurations are referenced as Entry Level Power, Maximum Level Power, and Maximum Level Redundant Power. The power sharing circuitry is internal to each supply and a power distribution board is used for connecting the power supplies together and for connecting the power supplies to the system.

For Maximum Level Redundant Power systems, the loss of a single power supply will not affect the operation of the system. A Power Supply Failure LED on the front panel will be turned on, and the failed supply can be replaced with the system operating. Each supply has LEDs on the rear which indicate the state of the power supply.

Each power supply has its own power cord with a detail provided in the power supply handle to hold the cord and prevent accidental disconnection from the supply. All supplies should be connected to the same AC mains branch circuit.

The power supply is inserted into and removed from the chassis from the rear and is held in place with a pivoting handle which is secured by four screws.

The power supply is located inside an Intel® system assembly. The location and orientation are shown in the figure below. A system may contain one, two, or three power supplies.

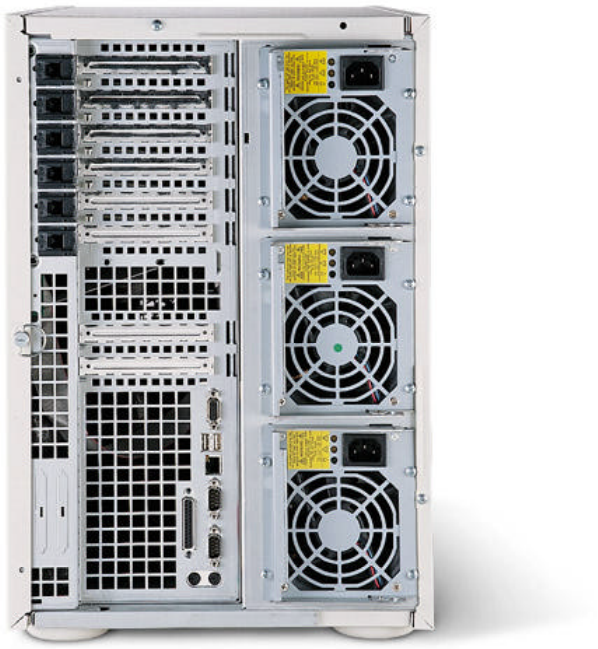

Figure 3-1: Location of the Power Supplies in the SPKA4 Pedestal Configuration (rear view)

3.2 Power Supply Mechanicals

The SPKA4 MP system power supply conforms to the Midrange SSI power supply specification and is equipped with a pivoting latch/handle to allow easy insertion/removal from the system.

The chassis for the power supply has been designed for a 92-mm size fan. There are keying positions on the power supply, which prevents a power supply with the wrong airflow direction from being plugged into a system. Figure 3-2 shows the physical size of the supply with connector locations. The AC inlet can be located on the interior or exterior face of the power supply. The power supply has a required handle and faceplate assembly, which pivots to assist insertion and extraction and provides retention.

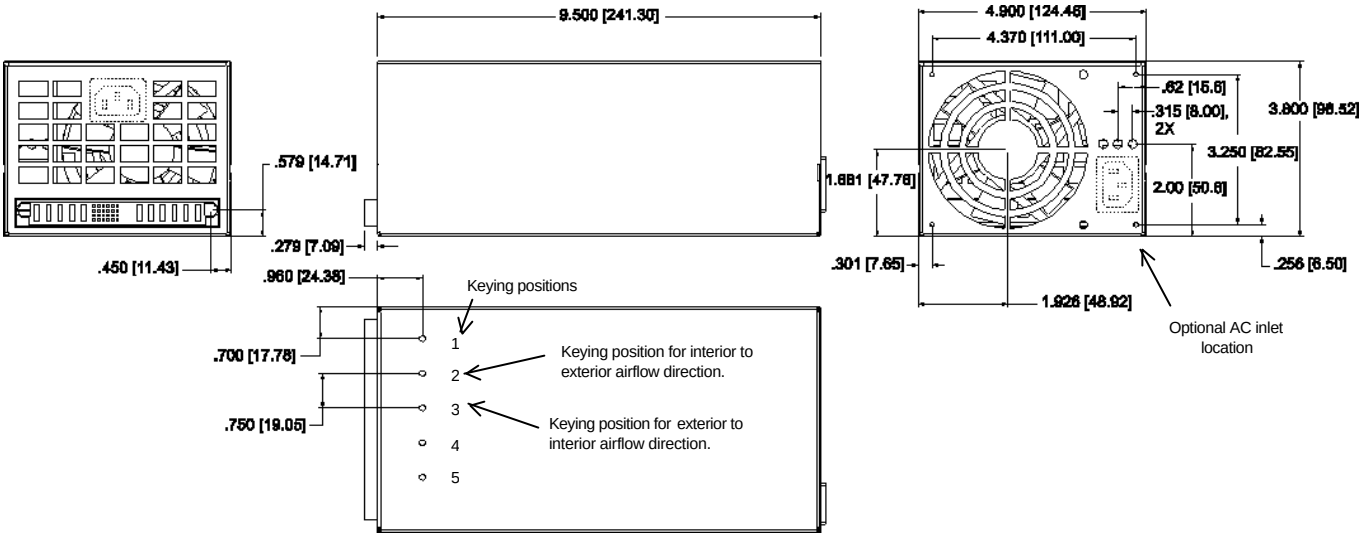

Figure 3-2: Power Supply Mechanical Drawing

3.2.1 Airflow

The airflow intake is from the DC connector face, and the air is exhausted on the handle face of the supply.

The minimum airflow required by the power supply for cooling at high and low fan speeds (Q_{high}, Q_{low}) is shown in Table 3-1.

Table 3-1: Airflow

Item	Description	Min.	Max.	Units
Q_{high}	Airflow through power supply; max. load, $T_{ambient}$=50?C, 5000 ft. elevation.	21		CFM
Q_{low}	Airflow through power supply; max. load, $T_{ambient}$=35?C, 5000 ft. elevation.	17		CFM

3.2.2 Temperature

Table 3-2: Temperature

Item	Description	Min.	Max.	Units
T_{op}	Operating temperature range.	0	50	?C
?T_{ps}	Temperature rise from inlet air to outlet air of power supply. 375 W output power, 21CFM, sea level, 25?C inlet air. 17CFM, 375 W output power, sea level.		 21 26	?C
$T_{non\text{-}op}$	Non-operating temperature range.	-40	70	?C
T_{case}	Maximum case temperature of any external surface of the power supply enclosure; T_{op}=25?C.		50	?C

3.2.3 Acoustics

The power supply incorporates a 92mm low noise fan to exhaust air from the peripheral bay. These fans have thermal sensors for speed control and incorporate a tachometer output.

The power supply runs at LOW fan speed under the conditions defined for Q_{low} in Table 3-1. The power supply has less than 43 dBA of sound pressure noise (L_p) at any bystander microphone location when operating at LOW fan speed. Sound pressure is a measurement of the total noise at the specified microphone location in the room.

3.2.4 DC Output Connector

DC power and control signals are interfaced to the system distribution and control subsystem via connectors which dock with mating connectors when the power supply is inserted into the system power distribution board. The output connector is a blind mating type connector that connects the power supplies' output voltages, control signals, and alarm signals. Connector pin assignments are listed in Table 3-4, and show the pin locations for the output connector. The signal pins are 3A rated contacts. Pin A6 is shortened to allow for hot-swapping of the power supply. The connector is keyed to the power supply by the positioning of the guide/keying pins on either side of the connector. The keying location for the recommended connector is A1.

Table 3-3: Signal Descriptions

Signal	Description		Signal	Description		Signal	Description
12LS	12 V load share bus		PWOK	Power OK output		5VSB	5 V standby output
5LS	5 V load share bus		ACOK#	AC OK output		-12 V	-12 V output
3.3LS	3.3 V load share bus		ACRange	AC input range select		SCL	I_2C clock signal
12VS	12 V remote sense		PSKILL	Supply fast shutdown		SDA	I_2C data signal
5VS	5 V remote sense		FAIL	Failure signal		A0	I_2C address bit 0
3.3VS	3.3 V remote sense		PRFL	Predictive failure signal		A1	I_2C address bit 1
ReturnS	Return remote sense		PRESENT#	Power supply present		FANC	Fan control signal
PSON#	Power enable input						

Table 3-4: Output Connector Pinout

Signal Pins										
	1	2	3	4	5	6				
D	12LS	PWOK	ACOK#	ACRange	ReturnS	-12 V				
C	A0	SCL	FAIL	PRFL	12VS	3.3VSB[1]				
B	A1	SDA	3.3VS	5VS	Reserved	+5VSB				
A	3.3LS	PRESENT#	FANC	5LS	PSON#	PSKILL				
Power Blades										
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11
Reserved	+12V	GND	GND	GND	GND	GND	+5 V	+5 V	+3.3 V	+3.3 V

Notes:
Signals that can be defined as low true or high true use the following convention:
signal# = low true

[1] The 3.3 VSB output is an optional output.

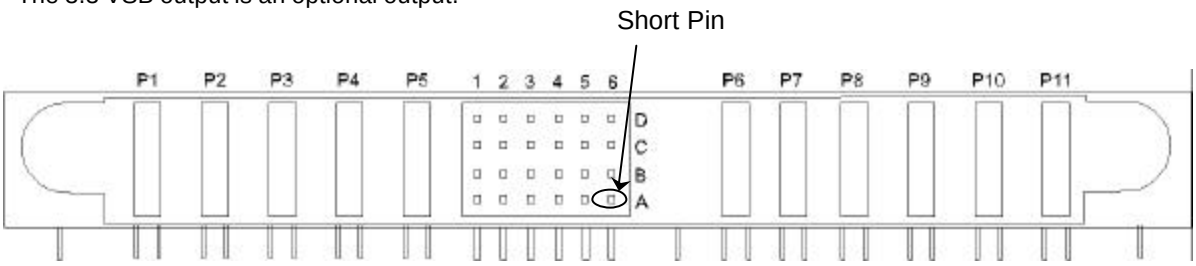

Figure 3-3: Connector Pin Locations

Note: PIN # A6 will be shorter than all others for PSKILL implementation.

3.3 Power Supply Electricals

3.3.1 Efficiency

The power supply has a minimum efficiency of 60% to its DC output pins at maximum load currents, at rated nominal input voltages and frequencies.

3.3.2 AC Input Voltage Specification

The system is specified to operate, without switching, from 100-120 Vac, 200-240 Vac, at 50 or 60 Hz. The power supply incorporates universal power input with active Power Factor Correction (PFC) which shall reduce line harmonics in accordance with the EN61000-3-2 and JEIDA MITI standards. The system is tested to meet these line voltages, and has been tested (but not specified) at +10% and -10% of the voltage ranges, and similarly ? 3 Hz on the line input frequency.

The system is specified to operate without error with line source interruptions not to exceed 20 milliseconds at nominal line conditions and full power supply output load.

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% THD must not cause the power supply to go out of specified limits.

Table 3-5: AC Input Voltage Rating

Parameter	Minimum	Rated	Maximum	Maximum Input Current (375 W)
Voltage (110)	90 V_{rms}	100-127 V_{rms}	132 V_{rms}	7.1 A_{rms}
Voltage (220)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}	3.5 A_{rms}
Frequency	47 Hz		63 Hz	

3.3.2.1 AC Line Dropout

An AC line dropout is defined to be when the AC input drops to 0 VAC for one cycle or less of the AC input during any phase of the AC line. During an AC dropout, the power supply must meet dynamic voltage regulation requirements over the rated load. An AC line dropout shall not cause any tripping of control signals or protection circuits. If the AC dropout lasts longer than one cycle of the AC line, then the power supply should recover and meet all turn on requirements. The power supply must meet the AC dropout requirement over rated AC voltages, frequencies, and output loading conditions. Any dropout of the AC line shall not cause damage to the power supply.

3.3.2.2 AC Line Transient Specification

AC line transient conditions are defined as “sag” and “surge” conditions. The “sag” conditions are also commonly referred to as “brownout.” The “sag” condition is defined as the AC line voltage dropping below nominal voltage. The “surge” conditions are defined as when the AC line voltage rises above nominal voltage. The power supply shall meet the performance requirements under the AC line sag and surge conditions shown in Table 3-6 and Table 3-7, respectively.

Table 3-6: AC Line Sag Transient Performance

AC Line Sag				
Duration	**Sag**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
Continuous	10%	100VAC-127VAC 200VAC-240VAC	50/60 Hz	No loss of function or performance.
0 to 1 AC cycle	100%	100VAC-127VAC 200VAC-240VAC	50/60 Hz	No loss of function or performance.
> 1 AC cycle	>10%	No loss of function or performance	50/60 Hz	Loss of function acceptable, self recoverable.

Table 3-7: AC Line Surge Transient Performance

AC Line Surge				
Duration	**Surge**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
Continuous	10%	100VAC-120VAC 200VAC-240VAC	50/60 Hz	No loss of function or performance.
0 to 1/2 cycle	30%	110VAC, 220VAC	50/60 Hz	No loss of function or performance.

3.3.2.3 Power Recovery

The power supply shall recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria defined in the AC line dropout section above.

3.4 DC Output Specification

The power supply DC output specifications shall be met by one supply, by two supplies, or by three supplies operating with their outputs directly paralleled. When operated in parallel, the supplies shall equally share the total load currents within the limits specified herein while meeting all performance requirements of individual supplies. Failure of a supply in a paralleled group or removal of an operational or failed supply from a paralleled group shall not cause DC output transients in excess of the limits specified. Adding an operational or failed supply to a paralleled group shall not cause DC output transients in excess of the limits specified.

Steady state DC output voltages at the remote sense points shall remain within the limits of Table 3-8, for all combinations of operating line, load, load transient, and environment specified herein.

Table 3-8: DC Output Voltage Limits

Parameter	Min.	Nom.	Max.	Units	Tolerance
+3.3V	+ 3.25	+ 3.30	+ 3.35	V	? 1.5%
+5V	+ 4.90	+5.00	+ 5.10	V	? 2%
+12V	+ 11.76	+12.00	+ 12.24	V	? 2%
-12V	- 13.08	-12.00	- 11.40	V	+ 9% & -5%
+5V Standby †	+ 4.85	+5.00	+ 5.20	V	+ 4% & -3%

Notes:
† +5V standby shall be in reference to the common remote sense returning potential.

3.4.1 DC Outputs Rating

The power supply shall meet the static regulation requirements under the loading conditions specified in Table 3-9. The combined continuous output load applied to the power supply shall not exceed 375 W. If the power supply exceeds 385 W, the power supply should not be subjected to this current draw for more than 12 seconds.

Table 3-9: 375 W Load Ratings

	Single Power Supply Maximum Output Current		
Voltage	Minimum Continuous	Maximum Continuous	Peak
+3.3V	0.5 A	34 A	
+5V	0.5 A	34 A	
+12V	0.5 A	18 A	18.5 A
-12V	0 A	1.0 A	
+5V Standby	0 A	2 A	

Notes:
Under some circumstances, a power supply may have 0 load on any or all of its outputs. Under these conditions, the power supply does not need to meet the output regulation specification described in this document, but it must operate without tripping the over-voltage protection circuit or any other fault protection circuitry. When the supply is subsequently loaded, it must begin to regulate and source current without fault.

The total system maximum load condition at AC input is also shown in Table 3-10 below for reference only. Either two or three power supplies can support the total system maximum load.

Table 3-10: Total System Load at Line AC Input (for reference only)

	Total System Maximum Load Condition		
Voltage	**Minimum Continuous**	**Maximum Continuous**	**Peak**
+3.3V	1.5 A	58 A	
+5V	1.5 A	58 A	
+12V	1.5 A	34 A	35 A
-12V	0.0 A	1.0 A	
+5V Standby	0.0 A	2.0 A	

3.4.2 DC Output Maximum Rating

At requirement AC input, maximum continuous power output shall not exceed 375 W. If the power supply exceeds 385 W, the power supply should not be subjected to this maximum current draw for more than 12 seconds.

3.4.3 Power Timing

This section details the timing requirements for single power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 200 ms. The +3.3 V, +5 V and +12 V output voltages should start to rise approximately at the same time. All outputs must rise monotonically. The +5 V output needs to be greater than the +3.3 V output during any point of the voltage rise, however, never by more than 2.25 V. Each output voltage shall reach regulation within 100ms (T_{vout_on}) of each other and begin to turn off within 100ms (T_{vout_on}) of each other. Refer to

Figure 3-4.

Figure 3-5 shows the timing requirements for a single power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied. The ACOK# signal is not being used to enable the turn on timing of the power supply.

Table 3-11: Output Voltage Timing

Item	Description	Min.	Max.	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	200	msec
T_{vout_off}	All main outputs must be within regulation of		300	msec

Item	Description	Min.	Max.	Units
	each other within this time.			
T_{vout_on}	All main outputs must be within regulation of each other within this time.		100	msec

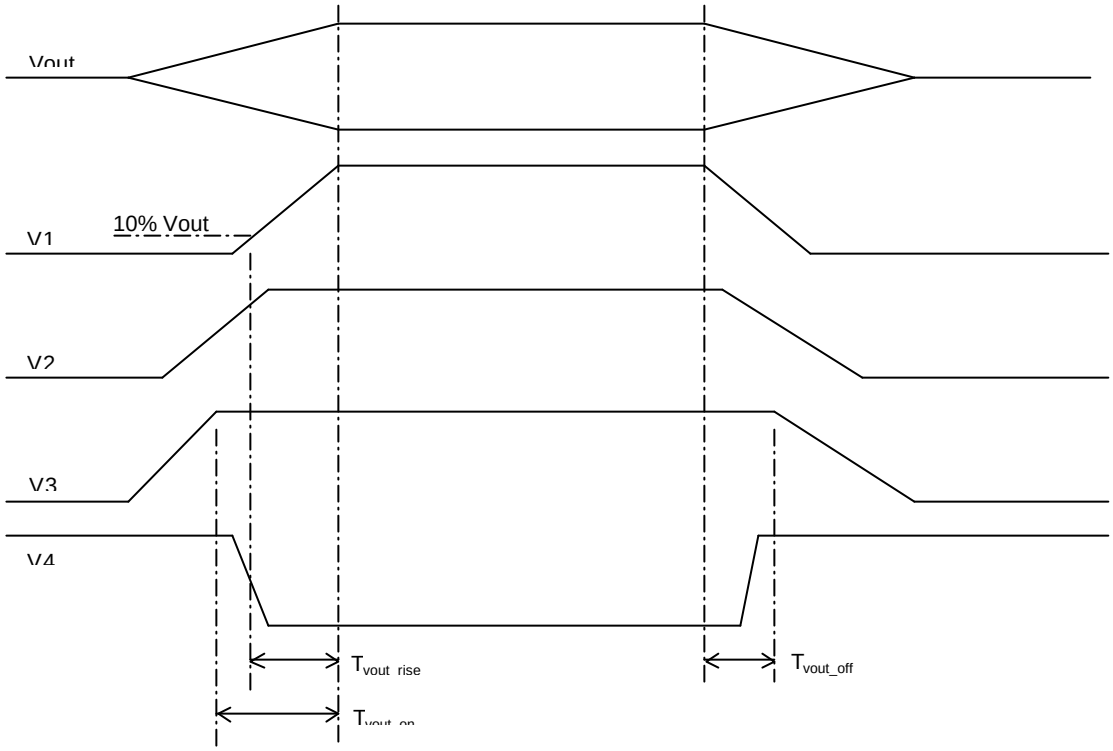

Figure 3-4: Output Voltage Timing

Table 3-12: Turn On/Off Timing

Item	Description	Min.	Max.	Units
$T_{sb\_on\_delay}$	Delay from AC being applied to 5 VSB being within regulation.		1500	msec

Item	Description	Min.	Max.	Units
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	msec
T_{vout_holdup}	Time all output voltages, including 5 VSB, stay within regulation after loss of AC.	21		msec
T_{pwok_holdup}	Delay from loss of AC to deassertion of PWOK.	20		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T_{pson_pwok}	Delay from PSON# deactive to PWOK being deasserted.		50	msec
T_{acok_delay}	Delay from loss of AC input to deassertion of ACOK#.	20		msec
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec
T_{pwok_off}	Delay from PWOK deasserted to output voltages (3.3 V, 5 V, 12 V, -12 V, 5 VSB) dropping out of regulation limits.	1		msec
T_{pwok_low}	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON signal.	100		msec
T_{sb_vout}	Delay from 48 VSB being in regulation to 48 VDC being in regulation at AC turn on.	50	1000	msec

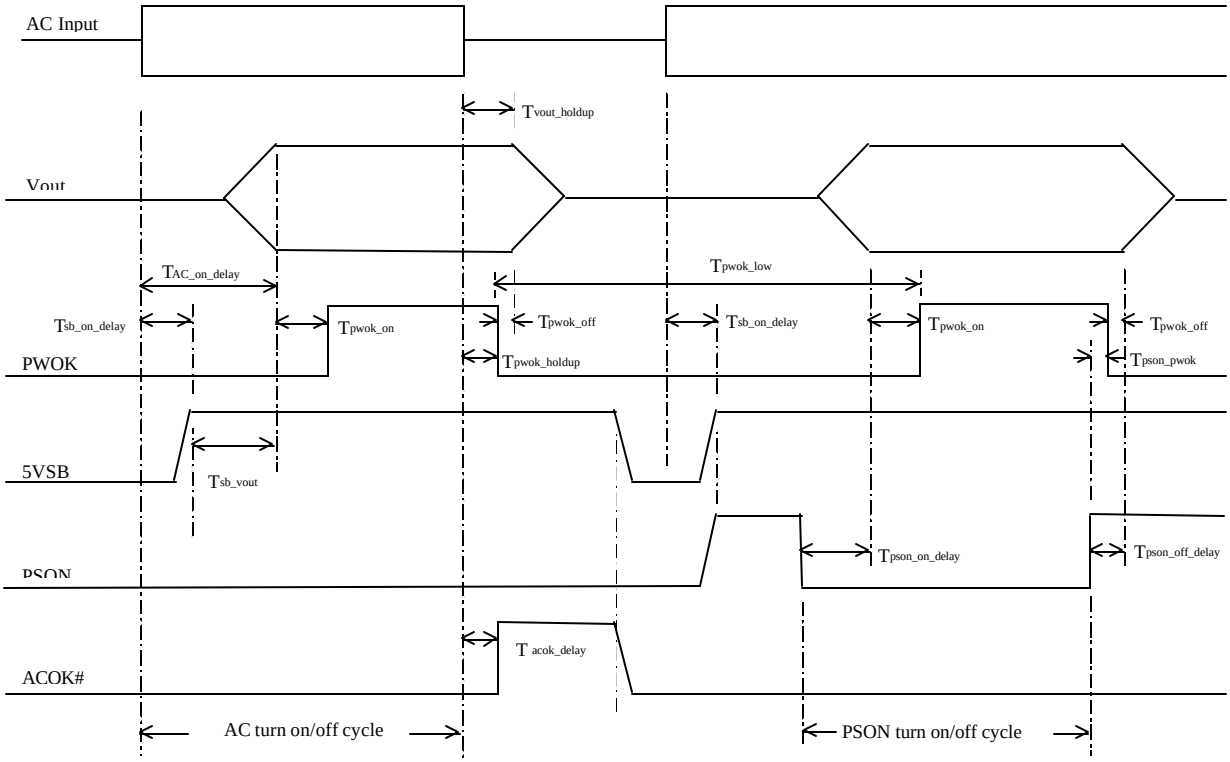

Figure 3-5: Turn On/Off Timing

3.5 Protection Circuits

A protection circuit inside the power supply shall cause only the power supply's main outputs to shut down. The 5 VSB output shall remain powered on if the failure does not involve this output. When a protection circuit shuts down the power supply, both the FAIL LED and the FAIL signal will be activated. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 seconds and a PSON# cycle HIGH for 1 second will reset the power supply.

3.5.1 Over-voltage Protection

The power supply over-voltage protection shall be locally sensed. The power supply shall shut down in a latch off mode after an over-voltage condition. This latch can be cleared by toggling the power supply off and then on or by an AC power interruption of greater than 1 second. This over-voltage limit applies to all specified AC input voltages and output load conditions. The following table contains the over-voltage limits. The values are measured at the output of the power supply DC connector.

Table 3-13: Over-voltage Limits

Output Voltage	Protection Point [V]
+3.3 V	3.8 --- 4.5
+5 V	5.6 --- 6.5
+12 V	13 --- 14.5

3.5.2 Over-current Limit

The power supply has current limits to prevent the +3.3 V, +5 V, and +12 V outputs from exceeding the values shown. The current limiting is the voltage fold-back type. The over-current limit level shall be maintained for a period of 2.6 seconds minimum and the power supply will latch off after 3.6 seconds.

Table 3-14: Over-current Protection

Voltage	Over Current Limit (Iout limit)
+3.3 V	110% minimum; 150% maximum
+5 V	110% minimum; 150% maximum
+12 V	110% minimum; 150% maximum

3.5.3 Over-temperature Protection (OTP)

The power supply is protected against over-temperature conditions caused by a loss of fan cooling or excessive ambient temperature. In an OTP condition, the PSU will shut down. Once the power supply temperature drops within specified limits, the power supply shall restore power automatically. The OTP circuit has built in hysteresis such that the power supply will not oscillate on and off when the temperature drops within specified limits. The power supply shall alert the system under either primary or secondary OTP condition via the power supply FAIL signal and

the FAIL LED. The failed LED will illuminate to indicate such OTP condition in 1+n power supply configurations.

3.5.4 Short Circuit Protection

The protection circuit inside the power supply shall cause only the power supply's main outputs to shut down. The 5 VSB output shall remain powered on if the failure does not involve this output. When a protection circuit shuts down the power supply, the LEDs shall indicate an OCP condition (per Table 3-22) and the FAIL signal shall be activated.

3.5.5 Hot Swap

Hot-swapping a power supply is the process of inserting and extracting a power supply from an operating power system. The power supply can be hot-swapped by the following methods:

- Extraction: The AC power is disconnected from the power supply, then the power supply is removed from the system. Insertion: The power supply is inserted into the system without the AC power applied, then the AC power is applied.
- Server management turning on the hot-swapped power supply. Extraction: Server management turns off only one of the power supplies via the PSON signal, then the power supply is removed from the system. Insertion: Power supply is inserted into the system, server management looks for power supply, depending upon the state of the system (on or off); the system then turns on the power supply via the PSON# signal or goes to standby mode operation.

In general, a failed (off by internal latch or external control) supply may be removed, then replaced with a good power supply; however, hot swap needs to work with operational as well as failed power supplies.

3.5.6 Forced Load Sharing

The +3.3 V, +5 V, and +12 V outputs will have forced load sharing. The outputs will share within 10% at full load. All current sharing functions are implemented internal to the power supply by making use of the 3.3LS, 5LS, and 12LS signals. The system connects the 3.3LS, 5LS, and 12LS signals between the power supplies. The supplies must be able to load share with up to four power supplies in parallel and operate in a hot swap/redundant n+1 configuration where n=1, 2, or 3.

Example of load share accuracy: Power supply #1 = 10.0 A

Power supply #2 > 9.0 A and < 11.0 A

3.5.7 Control Signals

3.5.7.1 PSON

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the 3.3 V, 5 V, 12 V, and –12 V power rails. When this signal is not pulled low by the system, or left open, the outputs (except the 5 VSB) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to Figure 3-5 for the timing diagram.

Table 3-15: PS-ON Signal Characteristic

Signal Type	Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.	
PSON# = Low, PSKILL = Low	ON	
PSON# = Open, PSKILL = Low or Open	OFF	
PSON# = Low, PSKILL = Open	OFF	
	Min.	**Max.**
Logic level low (power supply ON)	0 V	1.0 V
Logic level high (power supply OFF)	2.0 V	5.25 V
Source current, Vpson = low		4 mA
Power up delay: $T_{pson\_on\_delay}$	5 msec	400 msec
Power down delay: $T_{pson\_off\_delay}$	1.1 msec	
PWOK delay: T_{pson_pwok}		50 msec

3.5.7.2 PWOK

PWOK is a power good signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time long enough so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See Figure 3-5 for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall be inhibited as long as any power supply output is in current limit.

Table 3-16: PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located power supply.	
PWOK = High	Power Good	
PWOK = Low	Power Not Good	
	Min.	**Max.**
Logic level low voltage, Isink=4mA	0 V	0.4 V
Logic level high voltage, Isource=200? A	2.4 V	5.25 V
Sink current, PWOK = low		4 mA
Source current, PWOK = high		2 mA
PWOK delay: T_{pwok_on}	100 ms	1000 ms
PWOK rise and fall time		100 ?sec
Power down delay: T_{pwok_off}	1 ms	200 mSec

3.5.7.3 PSKILL Signal

The purpose of the PSKILL pin is to allow for hot-swapping of the power supply. The PSKILL pin on the power supply is shorter than the other signal pins. When a power supply is operating in parallel with other power supplies and then extracted from the system, the PSKILL pin will quickly turn off the power supply and prevent arcing of the DC output contacts. T_{PSKill} (shown below in Table 3-17) is the minimum time delay from the PSKILL pin unmating to when the power pins unmate. The power supply will discharge its output inductor within this time from the unmating of the PSKILL pin. When the PSKILL signal pin is not pulled down or left opened

(power supply is extracting from the system), the power supply should shut down regardless of the condition of the PSON# signal. The mating pin of this signal in the system is tied to ground. Upon receiving a LOW state signal at the PSKILL pin, the power supply will be allowed to turn on via the PSON# signal. Logic LOW on this pin by itself should not turn on the power outputs.

Table 3-17: PSKILL Signal Characteristics

Signal Type (Input Signal to Supply)	Accepts a ground input from the system. Pull-up to VSB located in the power supply.	
PSKILL = Low, PSON# = Low	ON	
PSKILL = Open, PSON# = Low or Open	OFF	
PSKILL = Low, PSON# = Open	OFF	
	Min.	**Max.**
Logic level low (power supply ON)	0 V	1.0 V
Logic level high (power supply OFF)	2.0 V	5.25 V
Source current, Vpskill = low		4 mA
Delay from PSKILL=High to power supply turned off (T_{PSKill})†		100 ?sec

Notes:
† T_{PSKill} is the time from the PSKILL signal deasserting HIGH to the power supply's output inductor.

3.5.7.4 Power Supply Failure (FAIL)

In the event of a power supply failure (OVP at any output, UV at any output, fan failure, or other failure), this signal is allowed to go HIGH by the power supply.

Table 3-18: FAIL Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located system.	
FAIL = High	Failed	
FAIL = Low	OK	
	Min.	**Max.**
Logic level low voltage, Isink=4mA	0 V	0.4 V
Logic level high voltage, Isink=50? A		5.25 V
Sink current, FAIL = low		4 mA
Sink current, FAIL = high		50 ?A
FAIL rise and fall time		100 ?sec

3.5.7.5 Predictive Failure Signal (PRFL)

This signal indicates that the power supply (or power supply fan) is reaching its end of life. The signal indicates a predictive failure when HIGH.

Table 3-19: PRFL Signal Characteristics

Signal Type (Active Low)	Open collector/drain output from power supply. Pull-up to VSB located in system.	
PRFL = High	Failing	
PRFL = Low	OK	
	Min.	Max.
Logic level low voltage, Isink=4mA	0 V	0.4 V
Logic level high voltage, Isink=50? A		5.25 V
Sink current, FAIL = low		4 mA
Sink current, FAIL = high		50 ?A
PRFL rise and fall time		100 ?sec

3.5.7.6 Power Supply Present Indicator (PRESENT)

The PRESENT# signal is used to sense the number of power supplies in the system (operational or not). This signal is connected to the power supply's output ground.

Table 3-20: PRESENT# Signal Characteristics

Signal Type	Output from power supply that is connected to ground. Pull-up to VSB located in system.	
PRESENT# = Low	Present	
PRESENT# = High	Not Present	
	Min.	Max.
Logic level low voltage, Isink=4mA	0 V	0.4 V
Logic level high voltage, Isink=50? A		5.25 V
Sink current, PRESENT# = low		4 mA
Sink current, PRESENT# = high		50 ?A

3.5.7.7 Power Supply FANC

The requirements for the FANC signal are similar to that of the ATX specification.

The FANC signal is a fan speed and sleep mode control signal. The fan speed and sleep mode are controlled by a variable voltage on this pin. This signal allows the system to request control of the power supply fan. The control circuit in the system supplies voltage to this pin from 12 VDC to 0 VDC for the fan control request. If the FANC signal is left open, the fan control defaults to power supply control.

Table 3-21: Power Supply FANC

Signal Type	Accepts an input voltage from the system. Pull-up to 12 V located in power supply.	
FANC < 1V	Fan in SLEEP mode (see note 1)	
2V < FANC < 3V	Fan in LOW speed (see note 1)	
3V < FANC < 10.5V	Fan ramps from LOW to HIGH speed (see note 1)	
FANC > 10.5V	Fan in HIGH speed (see note 1)	
	Min.	Max.

Source current		2 mA
Fan SLEEP mode output power (see note 2)		50 W
Fan LOW speed ambient temperature		35?C

Notes:
1. This is a request from the system to the power supply to operate the fan at this condition. The power supply can override this request and increase the fan speed if the power supply requires more cooling.
2. When the power supply fan is in SLEEP mode the fan must be operating at its minimum RPM, which is slow enough to not output any noticeable audible levels. The power supply must be able to supply 0 W to 50 W of output power at 50?C ambient (any combinations of 3.3 V, 5 V, and 12 V output currents) in the power supply fan SLEEP mode condition without the power supply overriding and turning the fan to LOW or HIGH speed.

3.5.7.8 Power Supply Field Replaceable Unit (FRU) Signals

The FRU data format is compliant with the IPMI specifications. Four pins will be allocated for the FRU information on the power supply connector. One pin is the Serial Clock (SCL). The second pin is used for Serial Data (SDA). Both pins are bi-directional and are used to form a serial bus. Pins three and four are address lines A0 and A1 and indicate to the power supply's EEPROM which position the power supply is located in, in the system.

A0	A1	Address
Low	Low	0xA0
Low	High	0xA2
High	Low	0xA5
High	High	0xA6

The FRU circuits inside the power supply are powered off of 5 VSB on the system side of the OR'ing device and grounded to ReturnS (remote sense return). The write control (or write protect) pin should be tied to ReturnS inside the power supply so that information can be written to the EEPROM.

3.5.8 LED Indicators

The green power LED (PWR) blinks to indicate that AC is applied to the PSU and standby voltages are available. This same LED should go solid to indicate that all the power outputs are available. There is an amber Power Supply Fail LED to indicate that the power supply has failed and replacement of the unit is necessary. There is an amber Predictive Fail LED to indicate that the power supply is about to fail in the near future due to a poorly performing fan. This LED should be blinking to indicate the predictive failure condition and should be latched into a blinking state once the condition has occurred. This latch can be cleared by toggling the PSON# signal or by an AC power interruption of greater than 15 seconds. Refer to Table 3-22 for conditions of the LEDs.

Table 3-22: LED Indicators

	Power Supply LEDs		
Power Supply Condition	**Power LED (Green)**	**Predictive Fail LED (Amber)**	**Fail LED (Amber)**
No AC power to all PSU	OFF	OFF	OFF

Power Supply Condition	Power Supply LEDs		
	Power LED (Green)	Predictive Fail LED (Amber)	Fail LED (Amber)
No AC power to this PSU only	OFF	OFF	ON
AC present/standby outputs on	Blinking	OFF	OFF
Power supply DC outputs ON and OK	ON	OFF	OFF
Power supply failure	OFF	OFF	ON
Current limit	ON	OFF	Blinking
Predictive failure	ON	Blinking/Latched	OFF

The LEDs are visible on the power supply's exterior face. The appearance of three LEDs is in the following order from left to right as viewed in Figure 3-2: Power, Predictive Fail, Fail.

Table 3-23: Power Supply LED Indicators and Control Signal Logic

Conditions	Power Supply LEDs			Power Supply Output Signal States			Input to P.S.
	PWR (Green)	PRFL (Amber)	FAIL (Amber)	P_Good H = Pwr good	Pred. Failure H = Pred. failure	P.S. Failure H = P.S. Fail	P.S. On L = P.S. Enable
No AC power	OFF	OFF	OFF	L	L	H	L
No AC power to this PSU only	OFF	OFF	ON			H	L
AC in/standby on/PS off	Blinking	OFF	OFF	L	L	L	L
DC outputs OK	ON	OFF	OFF	H	L	L	L
Power supply failure (including OVP and OTP)	OFF	OFF	ON	L	L	H	H
Current limit (Including OCP and Short)	ON	OFF	Blinking	L	L	H	L
Predictive failure	ON	Blinking /Latched	OFF	H	H	L	L

The Power LED (green), the Predictive Failure LED (amber), and the Power Supply Failure LED (amber) are marked or labeled near the LEDs with the following markings.

The Power LED is labeled as **PWR**.

The Predictive Failure LED is labeled as **PRFL**.

The Power Supply Failure LED is labeled as **FAIL**.

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4. Power Distribution Board

The SPKA4 MP server system power supplies plug into a power distribution board. This board provides the interconnections between the supplies, the server management interface, and a power converter to provide a controlled voltage for the system fans.

4.1 Introduction

This section describes the feature set of the SPKA4 MP server system power distribution board (PDB). The PDB is used in the chassis to provide connectivity, system fan voltage, and server management features for one, two and three power supply configurations. The two and three supply configurations allow for “one plus one” and “two plus one” redundant power systems respectively.

4.1.1 Feature Overview

- Supports single, dual and triple power supply solutions for powering the chassis.
- Supports server management:
  - Power supply Field Replaceable Unit (FRU) information access.
  - Predictive failure monitoring.
  - Power supply presence.
  - Peripheral voltage monitoring.
  - Chassis fan speed control.

4.2 Physical Description

The printed circuit board has the dimensions, mounting hole placements, and connector placements as shown in the mechanical specification. The board has external dimensions of 15.5" X 3.85".

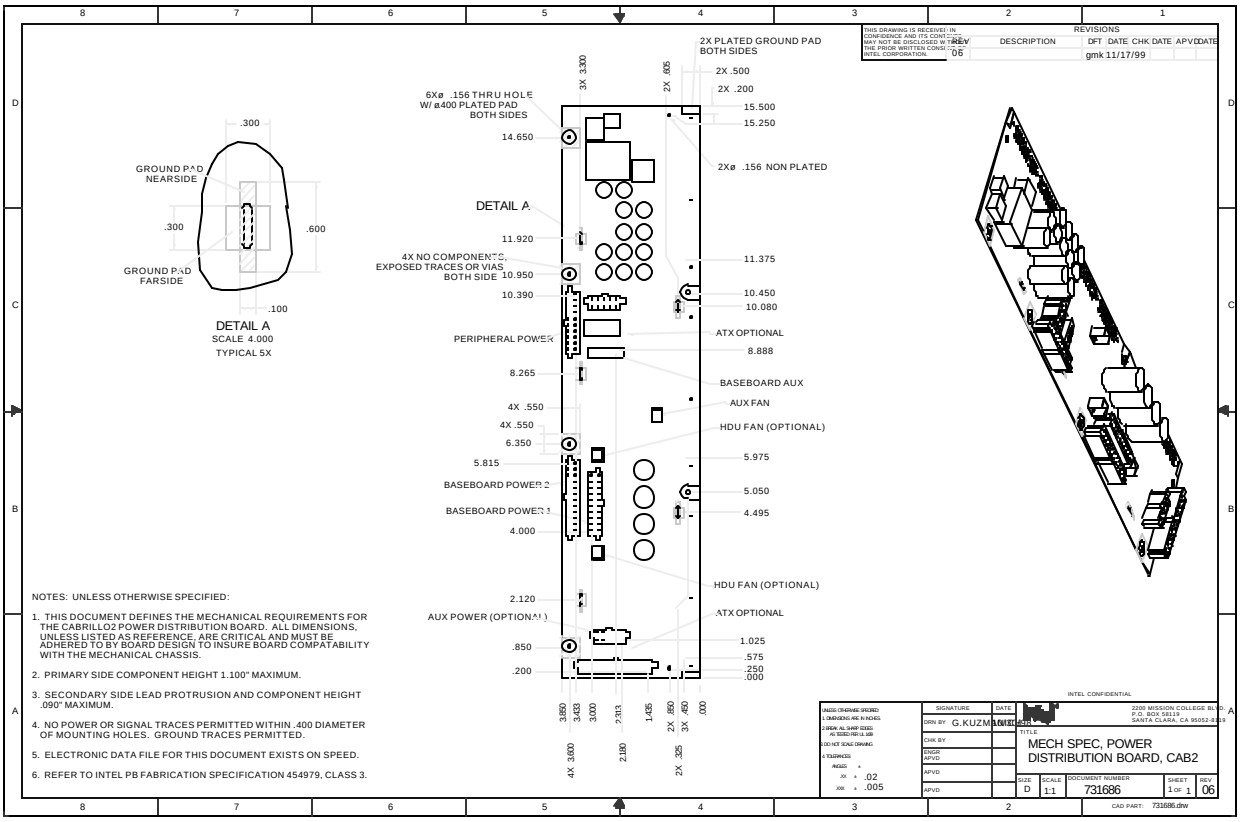

Figure 4-1: Power Distribution Board Diagram

4.2.1 Location

The power distribution board is located in the base of the chassis. Right angle connectors on the PDB allow for blind mating of three power supply connectors. Outputs are provided for power delivery to high performance mid-range server boards, and chassis components.

4.3 Electrical Connections

Connectors on the Power Distribution Board include the following:

- Power supply connectors.
- Baseboard power connectors.
- Baseboard auxiliary connector.
- Peripherals.

4.4 Power Supply Connectors

Table 4-1: Signal Pins and Power Blades

Signal Pins						
	1	**2**	**3**	**4**	**5**	**6**
D	-12V	RS GND	Reserved	Reserved	PWR OK	+12V LSS
C	Reserved	RS +12V	PRDCT FAIL	FAIL	I2C SCL	A1
B	+5V Standby	Reserved	RS +5V	RS +3.3V	I2C SDA	A2
A	PSKILL	PSON*	+5V LSS	FANC	PRESENT*	+3.3V LSS

Power Blades										
P1	**P2**	**P3**	**P4**	**P5**	**P6**	**P7**	**P8**	**P9**	**P10**	**P11**
+3.3V	+3.3V	+5V	+5V	GND	GND	GND	GND	GND	+12V	Reserved

Notes:
Signals that can be defined as low true use the following convention: *signal** = low true.

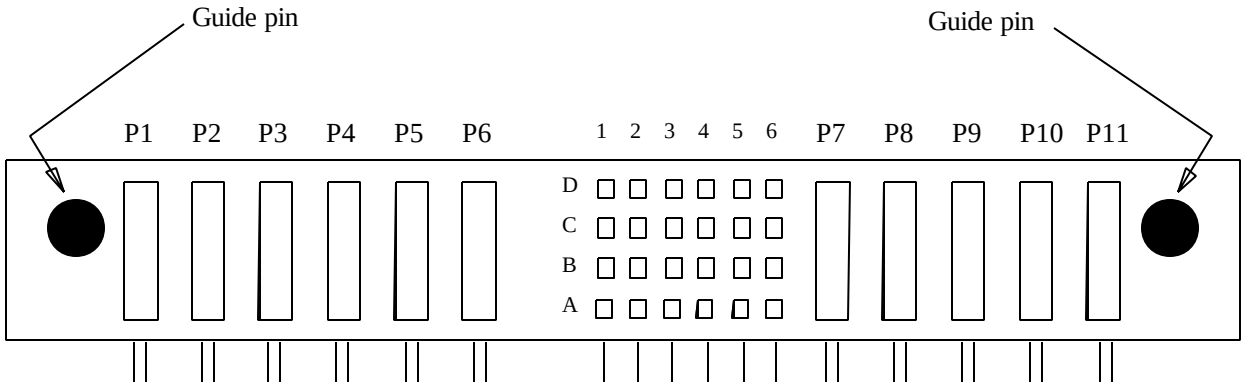

Figure 4-2: Power Supply Mating Connector Pin Locations

Note: The pin on the power supply connector that mates with position A1 will be shorter than all others for PSKILL implementation.

The power supply mating connectors, J1, J2 and J3, conform to the above format.

4.5 Baseboard Power Connectors

Table 4-2: Baseboard Power Connectors

	Pinout		
+3.3	13	1	+3.3
+3.3	14	2	+3.3
+3.3	15	3	+3.3
+3.3	16	4	+3.3
+3.3	17	5	+3.3
+3.3	18	6	+3.3

	Pinout		
GND	19	7	GND
GND	20	8	GND
GND	21	9	GND
GND	22	10	GND
GND	23	11	GND
+12	24	12	+12

J7 conforms to this pinout.

Table 4-3: Connector Pinout

	Pinout		
+5_SB	11	1	+12
GND	12	2	GND
GND	13	3	GND
GND	14	4	GND
GND	15	5	GND
+5	16	6	+5
+5	17	7	+5
+5	18	8	+5
+5	19	9	+5
+5	20	10	+5

J8 conforms to the above format.

These high current circuits provide power for the baseboard circuits. Control and remote sense circuits are routed through the baseboard auxiliary connector.

4.6 Baseboard Auxiliary

Table 4-4: Baseboard Auxiliary

Pin	Signal	Pin	Signal
1	RTN_RS	2	5V_RS
3	3.3V_RS	4	FAN_CTL
5	I2C_SCL	6	I2C_SDA
7	GND	8	PWR_OK
9	PS_ON_L	10	GND
11	-12VCC		KEY
13	12V_RS	14	GND

The baseboard auxiliary connector, J10, conforms to the above format.

PWR_OK (output)

A signal asserted to the baseboard from the power supply(ies) indicating that power supply outputs are within specified operating limits. PWR_OK is asserted when the first power supply's outputs are within specification, and will occur between 100 ms and 1600 ms after PS_ON is applied. PWR_OK will de-assert 1 ms before the last power supply's outputs fall outside specified regulation limits.

-12VCC (output)

The only negative voltage power source for the baseboard. It provides 50 mA maximum current from any supply.

PS_ON_L (input)

A single power supply enable input to the PDB controls all power supplies. This signal must be able to sink 1.5 mA at 0 V. To disable the supplies it must be above 2 V.

FAN_CTL

This analog signal ranges from 0 to +2.5 Vdc and controls the speed of both the system fans, and the power supply fans. This signal drives the input of an amplifier circuit which produces two different outputs. The first is another analog signal that ranges from 0 to +10.5 Vdc (or slightly above). If this signal is 0-1 Vdc, the power supply fans will be running at minimum speed. From 1 V to 10.5 V, the power supply fan speed will increase with the voltage level of this signal. Any voltage above 10.5 V will result in the power supply fans running at maximum speed. A second output of this amplifier is the input voltage from which the system fans are powered. This circuit is capable of 0 to 13.2 Vdc out, with up to 6.3 A of current at 13.2 Vdc. System fan speed is controlled by adjusting this voltage output.

3.3V_RS
5V_RS
12V_RS
RTN_RS
(inputs)

Remote Sensing for +3.3 V, +5 V, and +12 V occurs on the baseboard. These signals are routed via the auxiliary connector to the appropriate power supply control inputs.

4.7 Peripheral Power Connector

Table 4-5: Peripheral Power Connector

	Pinout		
SYS FAN PWR	11	1	GND
FUSED +12 A	12	2	FUSED +5
GND	13	3	GND
FUSED +12 B	14	4	FUSED +5
GND	15	5	GND
FUSED +12 C	16	6	FUSED +5
GND	17	7	GND
FUSED +12 C	18	8	FUSED +12 B
GND	19	9	GND

	Pinout		
SCSI 2 FAN TACH	20	10	SCSI 1 FAN TACH

J13 conforms to the above format.

J13 provides a high current connection to provide power to system peripherals.

4.8 Power Output

The following table describes the current capabilities of each power form.

Table 4-6: Power Form Capabilities

Form	Tolerance	Max. Current	Min. Current
+3.3V	?1.5%	66A	1.5A
+5V	?2%	66A	1.5A
+5V_STDBY	+4% -3%	2A	None
+12V	?2%	34A	0.75A
-12V	+9% - 5%	0.5A	None

- +5V_STDBY provides current for operating the server management system. +5V_SDTBY is present when any power supply has AC power applied.
- -12V. This low current negative voltage is provided from power supply number one. This voltage is provided through the baseboard auxiliary connector.
- +3.3V, +5V, +12V. These are the high current power rails, with forced load sharing.

4.9 Server Management Features

The PDB provides access to the power supply and PDB status through an I2C interface. This is accomplished by the use of an Analog Devices ADM1024*. This chip provides a way to monitor the power subsystem status. Below is a block diagram of the ADM1024.

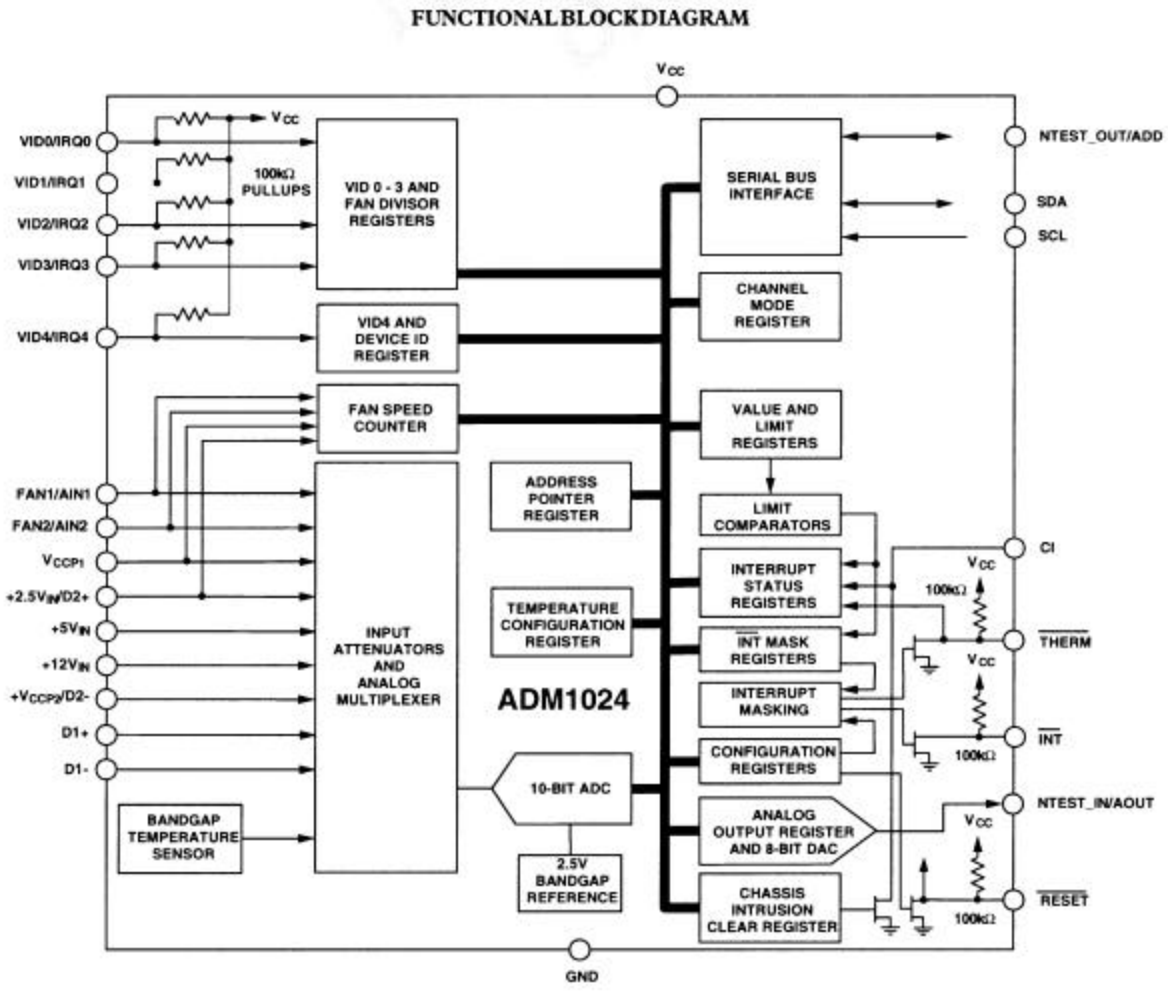

Figure 4-3: ADM1024* Block Diagram

The connection of signals to the ADM1024 is as follows:

Table 4-7: Connection of Signals to ADM1024*

ADM1024* Pin	ADM1024 Signal	Register #	Type	Direction	Power Share Board	Notes
1	NTEST_OUT/ADD		Digital	I/O	Unused (pulled up)	
2	THERM#	42	Digital	I/O	Unused (pulled up)	
3	SDA		Analog	I/O	BMC, EEPROM	I2C Bus Data
4	SCL		Analog	Input	BMC, EEPROM	I2C Bus Clock
5	FAN1/AIN1	5	Analog	Prog. A/D Input	PS1_FAN_FAIL_L	
6	FAN2/AIN2	6	Analog	Prog. A/D Input	PS2_FAN_FAIL_L	
7	CI	42	Digital	I/O	Unused (pulled down)	
8	GND		Analog	Power	GND	

ADM1024* Pin	ADM1024 Signal	Register #	Type	Direction	Power Share Board	Notes
9	VCC		Analog	Power	+5V Standby	+2.5V to +5.5V
10	INT#		Digital	Output	Unused (pulled up)	
11	NTEST_IN/AOUT		Dig/An	D-In/A-Out	Reserved	Future AC_RANGE
12	RESET#		Digital	Reset input	ADM1024 reset circuit	
13	D1-	26	Analog	Input	Unused (n/c)	Diode Temp only
14	D1+	26	Analog	Input	Unused (n/c)	Diode Temp only
15	+12VIN	15	Analog	Prog. Input	+12V	
16	+5VIN	16	Analog	Input	+5V	
17	VCCP2/D2-	25	Analog	Prog. Input	Reserved	Future AC_OK
18	+2.5VIN/D2+	20	Analog	Prog. Input	PS3_FAN_FAIL	
19	+VCCP1	21	Analog	Input	PS3_PWR_SUP_FAIL	
20	VID4	49	Digital	Input	PS3_PWR_SUP_PRESENT_L	
21	VID3	47	Digital	Input	PS2_PWR_SUP_FAIL	
22	VID2	47	Digital	Input	PS2_PWR_SUP_PRESENT_L	
23	VID1	47	Digital	Input	PS1_PWR_SUP_FAIL	
24	VID0	47	Digital	Input	PS1_PWR_SUP_PRESENT_L	

The ADM1024 (U3) is located at I2C address 0x5A.

5. System Cooling

5.1 Fans

Two hot-swappable fan assemblies provide cooling for the processors and the add-in cards in the card cage area. One assembly contains two fans (see Figure 5-1); the second assembly contains one fan (see Figure 5-2). Two additional hot-swappable fan assemblies may be installed for redundant cooling of the processor and add in-cards. The fan assembly that cools the processors contains two fans and an LED that the system turns on when either fan in the assembly fails. The fan assembly that cools the add-in cards has one fan and an LED that the system turns on when the fan fails. Figure 5-3 shows an SPKA4 MP server system configured with four hot-swappable fan assemblies.

Figure 5-1: SPKA4 Dual Fan Assembly for Processor Cooling

Figure 5-2: SPKA4 Fan Assembly for Add-in card Cooling

Figure 5-3: SPKA4 System Showing Four Hot-swappable Fan Assemblies

The power supply fans (attached to the power supplies), an optional fan which is directly connected to the Power Distribution Board and is in the rear of the chassis, and a fan mounted on the rear of each SCSI drive bay supply provide redundant cooling for the hard drives and power supplies.

All system fans provide a fault signal if the fan fails. The baseboard senses this signal and turns on a Cooling Fault LED on the front panel, and, in the case of the hot-swappable fans, also turns on the indicator on the hot-swap assembly. This signal is also available for server management functions.

Removal of the front side/top cover gives access to the fans. Failed fans for processors/add-in cards are hot-swappable. The SCSI drive bay and optional rear fan are easily changed after the system has been shut down. When a second drive bay (3.5") is installed, a third power supply or optional fan must be installed to provide redundant cooling for the drive bay.

5.2 Heat Load

The system maximum configuration heat load is approximately 4250 BTU.

5.3 Fan Distribution Board

This section establishes the physical size and general requirements for the SPKA4 MP server system fan distribution board (FDB). The FDB provides connectivity and power to six fans, which can be hot-swapped in and out of a running system.

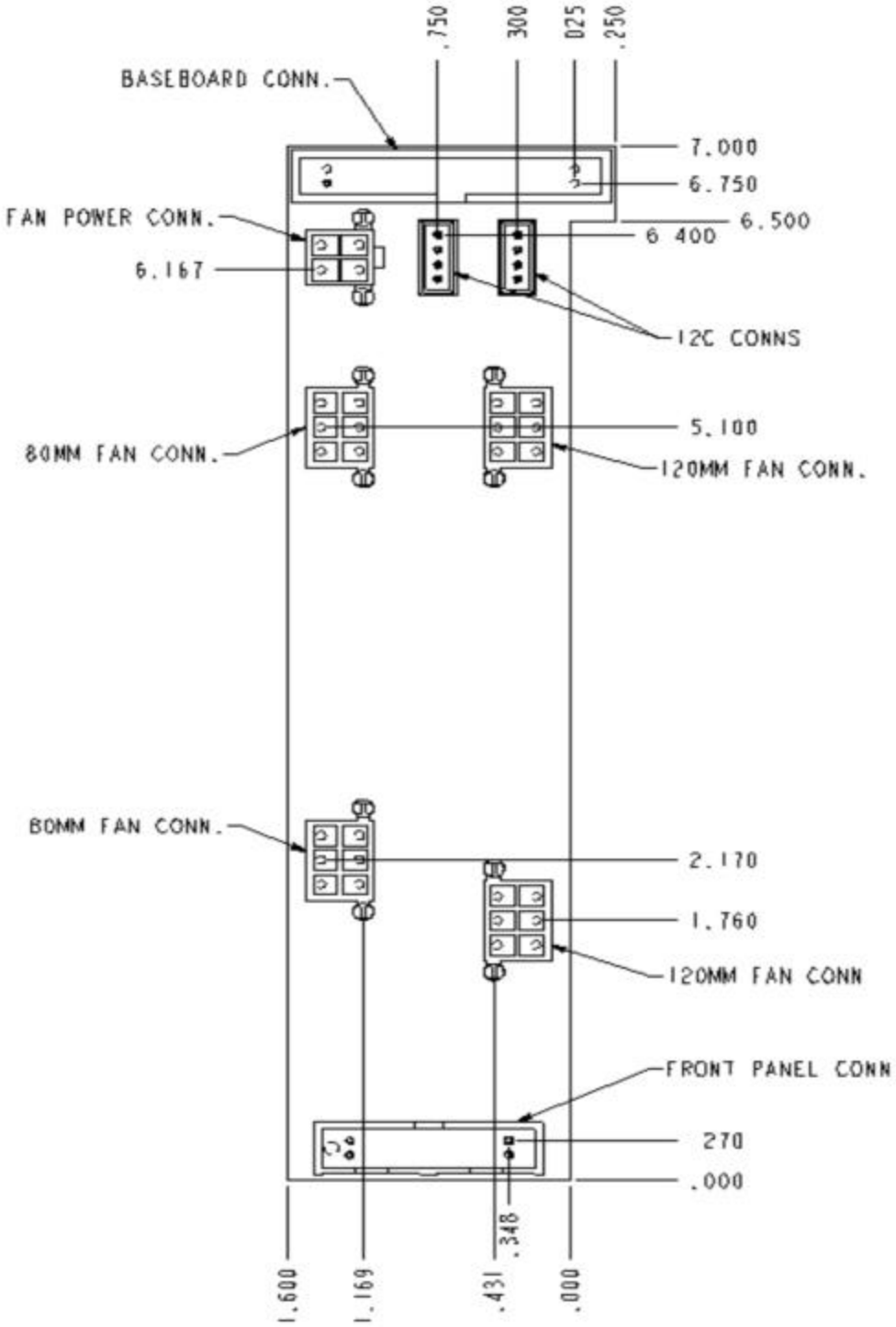

Figure 5-4: FDB Fan Connectors

5.3.1 FDB Features

- Power and connectivity for six hot-swap fans.
- Supports server management:
  - FDB Field Replaceable Unit information access.
  - Fan failure monitoring and indication (LEDs on fans).
  - Fan presence detection.
  - Temperature sensing.
  - Chassis fan speed control.

5.3.2 Physical Description

The printed circuit board has the dimensions, mounting hole placements, and connector placements as shown in Figure 5-4.

5.3.2.1 Location

The fan distribution board is located in the SC7000 chassis on the EPAC material as shown in Figure 5-5. It connects to the baseboard and front panel board through ribbon cables. There is also a connector to the power distribution board that provides power to the fans. The fan distribution board acts as an interface board between the hot-swap backplane (HSBP) and the baseboard.

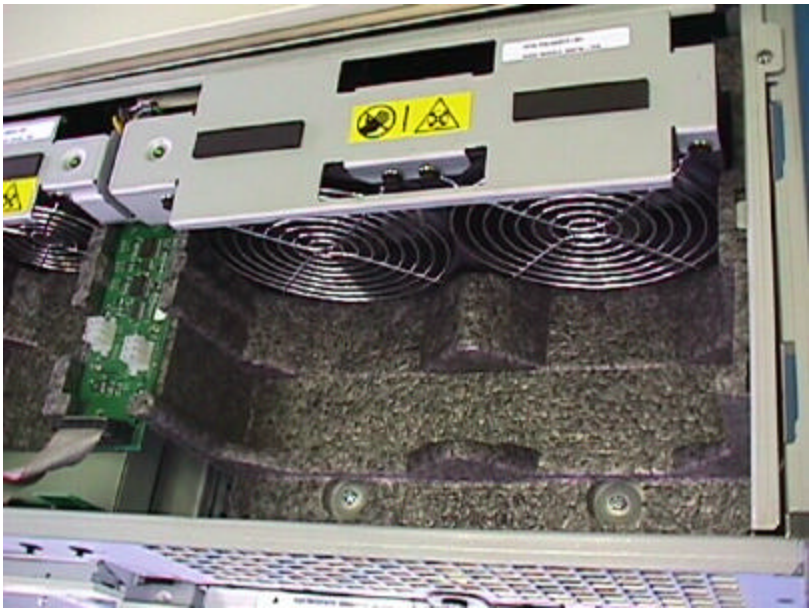

Figure 5-5: Fan Distribution Board Location

5.3.3 Electrical Connections

Connectors on the FDB include the following:

- Power supply connectors.
- Baseboard connector.

- Front panel connector.
- SCSI backplane connectors.
- Hot-swap fan connectors.

5.3.3.1 Baseboard Connector (J9)

Table 5-1: Baseboard Connector (J9)

Pin #	I/O	Description	Current	Voltage
1	I	Speaker (Front Panel)	Iih=37mA	Vih=5VSB
2	I	Ground		
3	O	Chassis Intrusion (Front Panel)	Iol=-0.33mA	Vol=0 V
4	I	Hard Drive Activity LED (Front Panel)	Iil=-19.3mA	Vol=0 V
5	I	VCC (Front Panel)	Iih=20mA	Vih= VCC
6	O	Sleep Switch (Front Panel)	Iol= -0.5mA	Vol =0 V
7	I	Cooling Fault LED (Front Panel)	Iil= -14mA	Vil=0 V
8	I	Power LED (Front Panel)	Iil= -14mA	Vil=0 V
9	I	Power Fault LED (Front Panel)	Iil= -14mA	Vil=0 V
10	I	Ground		
11	I/O	I^2C* Bus Routed to SCSI Backplane (Data – IMB)	N/A	N/A
12	I	NMI Switch (Front Panel)	Iil= -0.5mA	Vil=0 V
13	I/O	I^2C Bus Routed to SCSI Backplane (Clock – IMB)	N/A	N/A
14	I	Reset Switch (Front Panel)	Iil= -0.5mA	Vil=0 V
15	I	5V Standby	107mA	Vih= 5VSB
16	I	Power Switch (Front Panel)	Iil= -0.5mA	Vil=0 V
17	I	No Connect	N/A	N/A
18	I	Ground		
19	O	Tachometer 0 Fan1	Use 4.7K ohm PU	PU to Vcc
20	O	Tachometer 1 Fan2	Use 4.7K ohm PU	PU to Vcc
21	O	Tachometer 2 Fan3	Use 4.7K ohm PU	PU to Vcc
22	O	Tachometer 3 Fan4	Use 4.7K ohm PU	PU to Vcc
23	O	Tachometer 4 Fan5	Use 4.7K ohm PU	PU to Vcc
24	O	Tachometer 5 Fan6	Use 4.7K ohm PU	PU to Vcc
25	O	Tachometer 6 Fan7 (on PDB)	Use 4.7K ohm PU	PU to Vcc
26	O	Tachometer 7 Fan8 (on PDB)	Use 4.7K ohm PU	PU to Vcc

Pin #	I/O	Description	Current	Voltage
27	I	Network Activity LED (Front Panel)	Iil= -14mA	Vil=0 V
28	I	Ground		
29	I	I^2C Bus for FDB (Clock – Private Bus)	Iil= -3mA	Vil=0 V, Vih=5VSB
30	I/O	I^2C Bus for FDB (Data – Private Bus)	Iil= -3mA	Vil=0 V, Vih=5VSB

5.3.3.2 Front Panel Connector

Table 5-2: Front Panel Connector (J4)

Pin #	I/O	Description	Io/Ii	Vo/Vi
1	O	Ground		
2	O	Speaker	Io=37mA	Vo=5VStby
3	O	Hard Drive Activity	Io=19.3mA	Vo=Vcc
4	I	Chassis Intrusion	Io=0.33mA	Vo=3VStby
5	I	Sleep Switch	Io=0.5 mA	Vo=5VStby
6	O	VCC	19.3 mA	
7	O	Power LED	Io=15.8mA	Vo=5VStby
8	O	Cooling Fault LED	Io=15.8mA	Vo=5VStby
9	O	Ground		
10	O	Power Fault LED	Io=15.8mA	Vo=5VStby
11	I	NMI Switch	Io=0.5 mA	Vo=5VStby
12	I/O	I^2C* Bus (Data – IMB)	N/A	N/A
13	I	Reset Switch	Io=10mA	Vo=3VStby
14	I/O	I^2C Bus (Clock – IMB)	N/A	N/A
15	I	Power Switch	Io=0.5 mA	Vo=5VStby
16	O	5V Standby	63.2mA	
17	O	Ground		
18	O	Network Activity LED	Io=15.8mA	Vo=5VStby
19	I	No Connect	N/A	N/A
20	I	No Connect	N/A	N/A

5.3.3.3 Hot-swap Fan Connector

Table 5-3: Hot-swap Fan Connectors (J1, J2, J5, J6)

Pin #	I/O	Description
1	O	Ground
2	I	Present Signal
3	O	Fan Power
4	O	Fan Failure LED
5	I	Tachometer 2
6	I	Tachometer 1

Notes:
1. The present signal detects if a fan is present in the system.
2. Fan power can be varied by the power distribution board from 9V up to 13.8V in the event of a fan failure.

5.3.3.4 Power Connector

Table 5-4: Power Connector (J3)

Pin #	I/O	Description
1	I	Ground
2	I	Fan Power
3	I	Fan Tachometer 6 (from fan run from PDB)
4	I	Fan Tachometer 7 (from fan run from PDB)

5.3.3.5 Hot-swap SCSI Backplane Connector

Table 5-5: Hot-swap SCSI Backplane Connector (J7, J8)

Pin #	I/O	Description
1	O	SM_IMB_5V_SDA
2	O	Ground
3	O	SM_IMB_5V_SCL
4	O	No Connect (J7) OR Ground (J8)

Notes:
Pin 4 is read by the controller on the SCSI backplane to determine if it is the Primary (J7) backplane or the Secondary (J8) backplane.

5.3.4 Functional Architecture

The fan distribution board contains several different functions. Its primary function is to support hot-swap fans. It can support four 120mm fans and two 80mm fans directly on board. It routes tachometer signals for two other fans that can be driven from the power distribution board to the baseboard. Fans are provided to cool the baseboard and the associated processors and cards. Redundant fans can be populated to ensure proper cooling in the event of a fan failure. Two optional fans can have tachometer inputs routed from the power distribution board to the baseboard for a total of eight monitored system fans. Inventory and server management information can be transferred over the I^2C* bus. There are several signals that are routed from the baseboard to the front panel board. Another I^2C bus is routed to the SCSI backplane for server management support. There are several server management functions that support hot-swap fans. Server management is able to detect fans, turn on a failure LED on the fans, and report the temperature of the ambient air. Additionally, FRU information about the board is stored in an EEPROM.

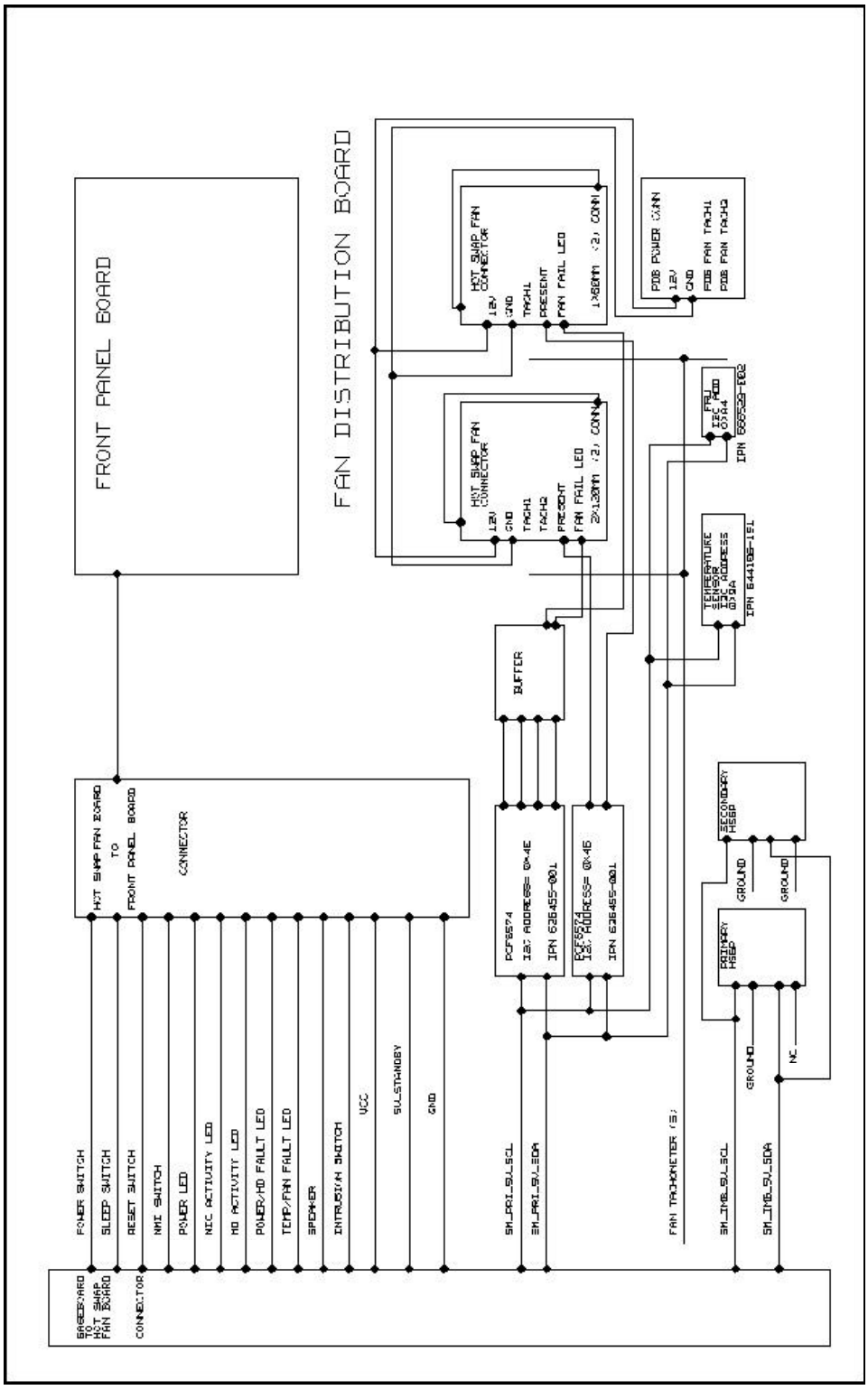

Figure 5-6: Functional Architecture

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6. System Peripheral Bays

6.1 3.5" Floppy Drive Bay

The SPKA4 MP server system ships from the factory with a 3.5" floppy drive bay. To access the bay to install or replace the drive, remove the side cover.

6.2 5.25" Drive Bays

The system design includes three 5.25" half-height peripheral bays designed for peripherals with removable media (e.g., floppy disk, CD-ROM or tape drive). These bays have removable filler panels installed.

Any two adjacent 5.25" bays are convertible to a single full-height bay. A cable from the onboard narrow/wide legacy SCSI controller allows up to three 5.25" half-height SCSI devices to be installed in these bays. A wide SCSI cable is supplied that will support two peripherals. The 5.25" peripherals are removable from the front of the chassis after disconnecting the cables at the rear of the peripheral.

6.3 Internal 3.5" Hard Drive Bays with Hot-swap SCSI Backplane

A hot-swap SCSI drive bay for five 3.5" low profile (1") SCA drives is provided. This drive bay has an LVD Ultra-160 SCSI backplane and a SCSI-Accessed Fault-Tolerant Enclosure (SAF-TE) board. An LED is adjacent to each drive to indicate activity and fault. Each drive can be accessed and replaced from the front of the system. The backplane is designed for LVD SCSI devices using the industry standard 80-pin SCA2 connector. The maximum power per drive is 14 watts.

As part of the hot swap implementation, a drive carrier is furnished with four fasteners into which the drives are mounted. The carrier slides into the chassis and is held by a latch on its handle.

A second hot-swap drive bay may be added for a total of ten 1" drives.

The hot-swap drive bay is also available for three 3.5" half-height (1.6") SCA drives. This drive bay has the same features as the 1” bay except the power per drive can be 18 watts. A Y cable to connect two 1.6” drive bays to one baseboard SCSI connector will be available allowing six 1.6” drives to be used in an array (RAID, etc.).

A single metal EMI door and the plastic door in the bezel cover the drive bays.

6.3.1 Hot-swap SCSI Drive Bay Drawings

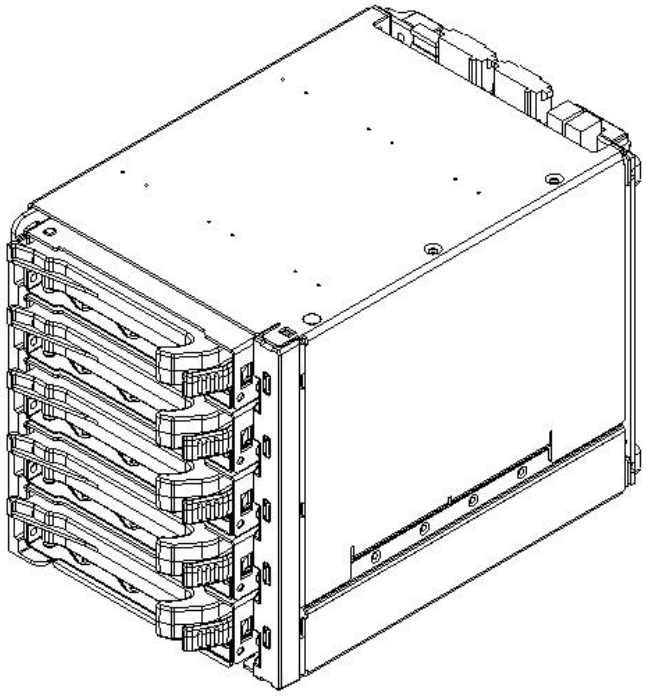

Figure 6-1: Hot-swap Drive Bay, Front Isometric View

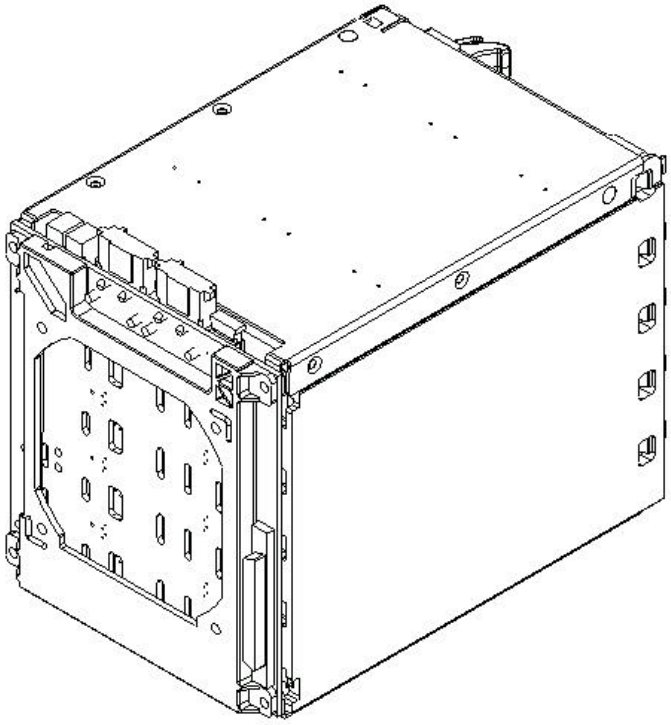

Figure 6-2: Hot-swap Drive Bay, Rear Isometric View

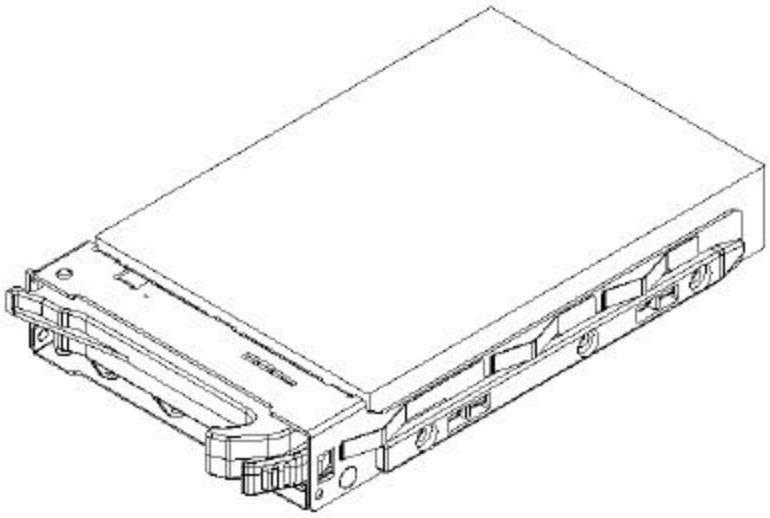

Figure 6-3: Hot-swap Drive Carrier with Drive Installed

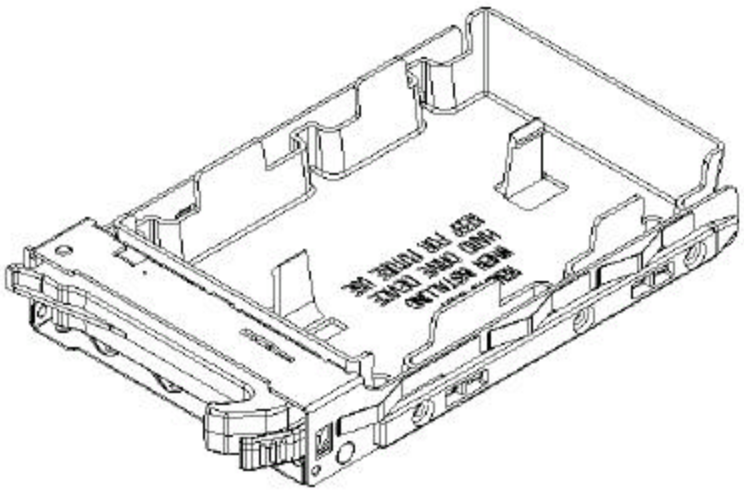

Figure 6-4: Drive Carrier with Air Baffle Installed

7. SCSI Backplane Board Set

7.1 Feature Overview

The SPKA4 SCSI backplane board set is an integral part of the SPKA4 system. It is designed to provide easy power-on (hot-swap) drive replacement, and to provide easy RAID integration over a wide range of RAID controller products. It is designed to be vendor independent. This section provides an overview of the SPKA4 LVD/SE SCSI backplane board set, describing the architecture of backplane board, and physical board layout diagrams.

The SPKA4 SCSI backplane is an LVD/SE SCSI design which provides support for new SCSI devices using Low Voltage Differential Signaling (Ultra 2 and Ultra 160m) as well as older SE SCSI devices (Ultra and older). The single backplane has a single SCSI channel with a SAF-TE controller and microcontroller on an add-in card. The backplane supports hot swapping SCA-2 style drives when mounted in the docking drive carrier.

The single feature that simplifies RAID integration is the addition of an onboard SCSI target whose command set allows vendor independent controller management and monitoring for associated drive functions such as: drive insertion and removal, light indicators, and drive power control. Its use simplifies cable management and eliminates errors caused by the possibility of incorrect correlation of several cables.

The SPKA4 LVD/SE SCSI backplane performs the tasks associated with hot-swappable SCSI drives, and enclosure (chassis) monitoring and management, as specified in the SAF-TE Specification, Revision 1.00. The SPKA4 SCSI backplane board supports the following features:

- Hot-swapping of SCSI drives, that allows connection of SCSI devices while the system power is on.
- SE SCSI and LVD SCSI modes.
- Five 1-inch LVD/SE SCSI drives per board.
- Single connector attachment (SCA-2) connectors to simplify insertion and removal of hard disk drives.
- Insertion and removal of hard drives in any power or SCSI bus state (hot swap).
- FET power control for each hard drive.
- FET short protection.
- Supports SCSI-3 SPI-2 (Ultra SCSI and Ultra2 SCSI) and SCSI-2 (Fast-10).
- Supports SCSI-3 SPI-3 (Ultra3 SCSI).

The SPKA4 SAF-TE card performs the tasks associated with enclosure (chassis) monitoring and management, as specified in the SAF-TE Specification, Revision 1.00. The features supported by the SAF-TE add-in card include the following:

- Monitoring the SCSI bus for enclosure services messages, and acting on them appropriately. Examples of such messages include:
  - Activate a drive fault indicator.
  - Power down a drive that has failed.
  - Report fan tachometer status.

- SAF-TE intelligent agent, which acts as proxy for "dumb" I^2C devices (that have no bus mastering capability) during intra-chassis communications.
- Microcontroller to monitor enclosure services.
- I^2C bus for management information.
- Flash memory for upgrading firmware.
- Thermal friendly mechanical form factor.
- SAF-TE compliant.
- Two fan tachometer monitoring.
- Drive fault and drive activity LEDs for each disk drive.

7.2 Placement Diagrams

The following diagrams show the layout of components and connectors on the hot-swap SCSI backplane printed circuit board set. This solution consists of two separate boards. The first board provides power distribution and SCSI interfacing of the drives. The second board provides the SAF-TE features and drive failure indicators.

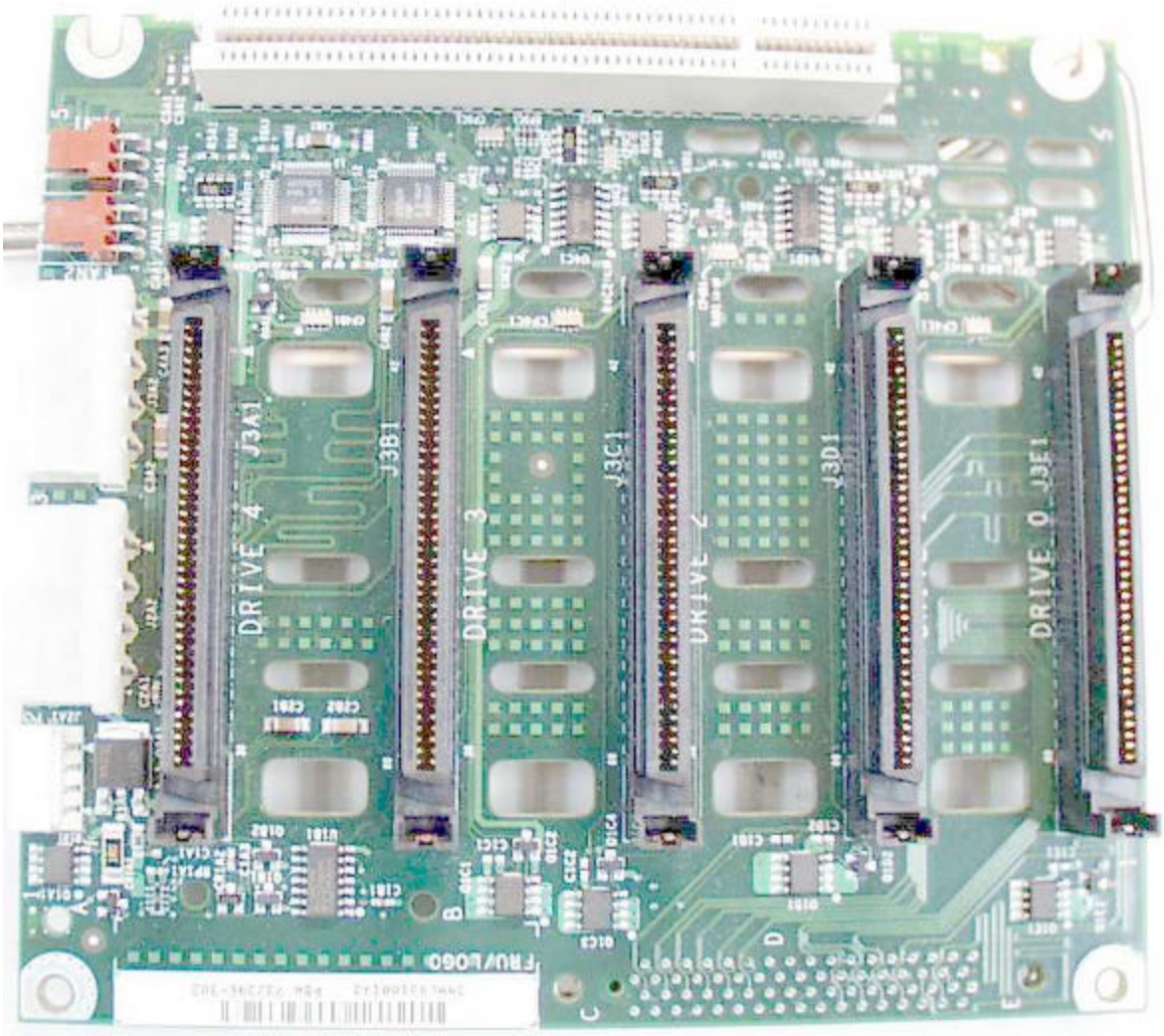

Figure 7-1: SPKA4 SCSI Backplane Placement

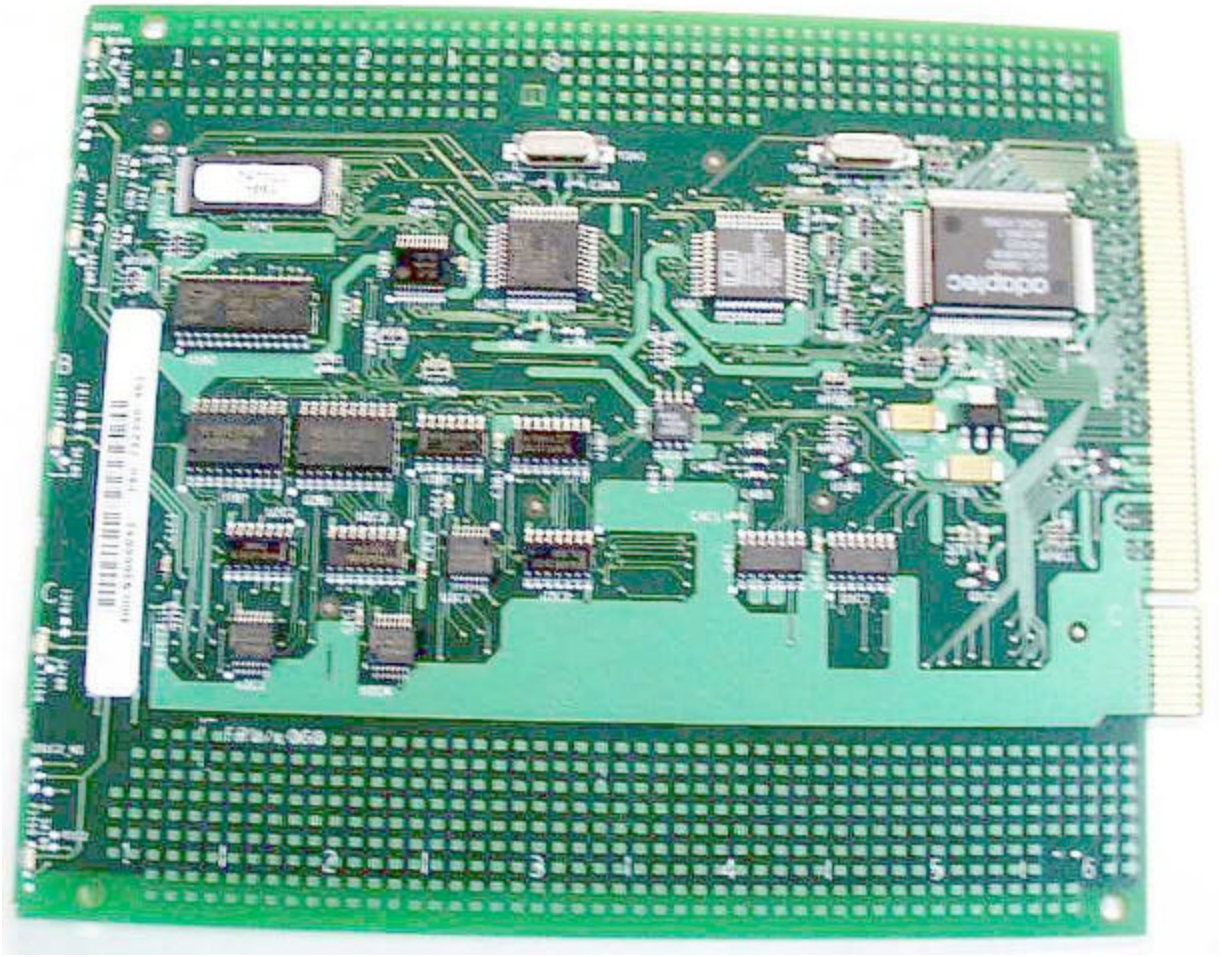

Figure 7-2: SPKA4 SAF-TE Board Placement

7.2.1 SCSI Bus Considerations

The SCSI bus, based on the SCSI-3 SPI-2 specification, is designed to allow any SCSI device to communicate with any other SCSI device. To that end, SPI-2 requires that all SCSI devices be certain distances apart, depending on the media capacitance measured in pF/m. The lower the media capacitance the greater the spacing needs to be because the loading from the device becomes more significant. The 5 x 1" LVD/SE SCSI backplane layout and board stackup was driven from LVD SCSI bus simulation, which yielded the following:

- SCA-2 to SCA-2 electrical distance of 4 inches.
- Six layer board with two internal SCSI layers with 90 Ohm impedance targeted.
- Total backplane SCSI length max 30 inches.

The 3 x 1.6" LVD/SE SCSI backplane layout and board stackup was driven from LVD SCSI bus simulation which yielded the following

- SCA-2 to SCA-2 electrical distance of 5 inches.
- Six-layer board with two internal SCSI layers with 90 Ohm impedance targeted.

- Total backplane SCSI length maximum 20 inches.

The electrical spacing of the SCA-2 connectors was a combination of the faster edge rate and faster transfer speed.

7.2.2 SCSI Bus Notes

The following are key points to remember:

- The LVD (Ultra2) length specification is 15 devices at 12 meters and 1-2 devices at 25 meters.
- The SE (Ultra) length specification is 5-8 devices at 1.5 meters (59 inches) and 1-4devices at 3 meter.
- If used in SE Ultra mode, the 1" drive backplane uses 30 of the 59 inches of the SCSI bus length.
- If used in SE Ultra mode, the 1.6" drive backplane uses 20 of the 59 inches of the SCSI bus length.
- The backplane's SCSI interface counts as one device on the SCSI bus regardless the presence of any SAF-TE compliant host controller.

7.2.3 Deviations from SAF-TE Specification

The SAF-TE specification requires the use of a "PAIR" signal. The intended use of this signal is to allow inter-backplane processor communication. This signal has not been implemented in prior designs and is not implemented here.

7.3 Architectural Overview

This section defines the architecture of the SPKA4 LVD/SE SCSI backplane, including descriptions of functional blocks and how they operate.

The SPKA4 hot-swap SCSI backplane board set is made up of the following functional blocks:

- SCSI bus with SCA (Single Connector Attach) drive connectors, and active LVDS terminators.
- Microcontroller with program Flash and RAM.
- SCSI interface that allows the microcontroller to respond as a SCSI target.
- I2C interface to server board.
- SCSI drive power control.
- Fault indicator support.
- Support for two cooling fans (fan-tach inputs and power control).
- Temperature sensor.
- Configuration jumpers.

The hot-swap SCSI backplane board set resides in the hot-swap drive bay of the SPKA4 chassis.

The following figure shows the functional blocks of the LVD/SE SCSI backplane. The two boards are split such that the backplane has the SCSI connectors and termination, and the SAF-TE add-in card contains the rest of the functional blocks. An overview of each block follows.

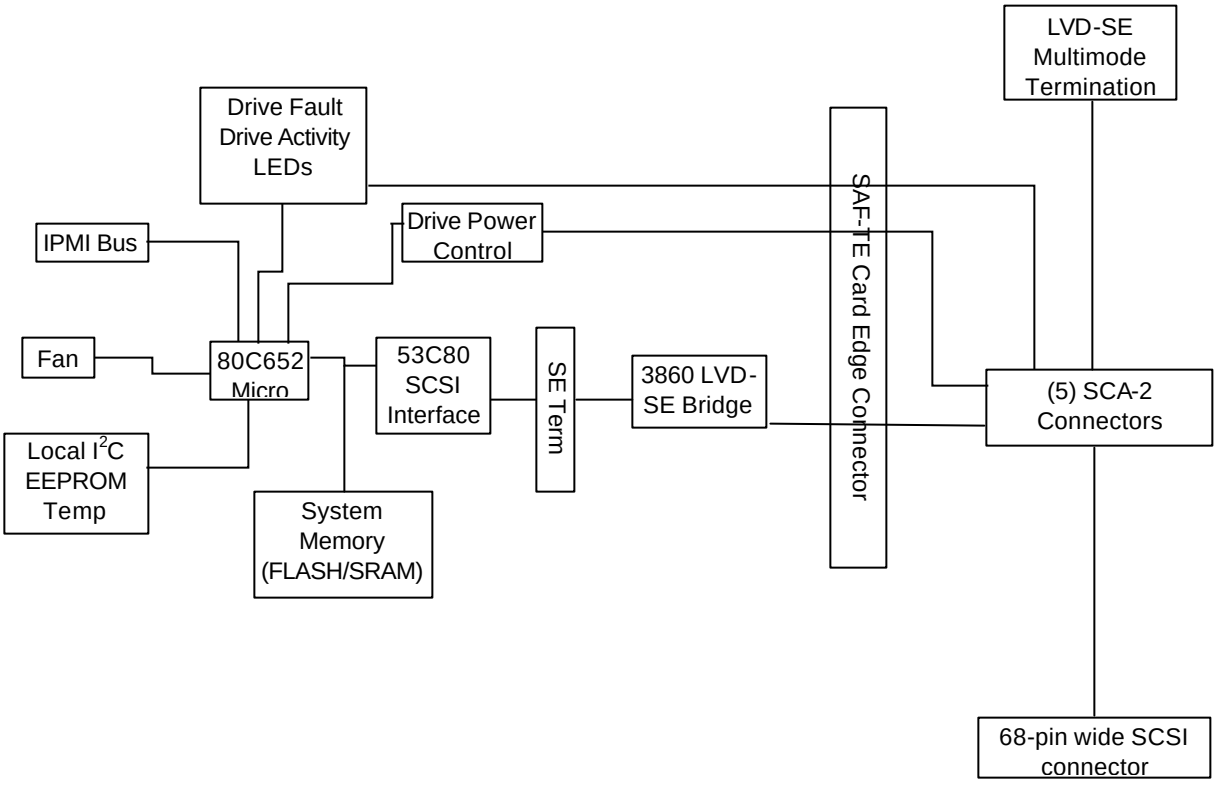

Figure 7-3: Functional Block Diagram

7.3.1 Wide SCSI Connector

SCSI input from host SCSI controller (baseboard or RAID card) is a press-fit connector.

7.3.2 SCA-2 Connectors

The LVD/SE SCSI backplane has five SCA-2 connectors which provide power and SCSI signals using a single connector. Each connector has control signals that enable the backplane to provide SCSI ID assignments as well as to drive motor spin-up configuration. Each SCSI drive attaches to the backplane using one of these connectors.

7.3.3 SCSI Multi-mode Termination

The multi-mode terminators provide SCSI-3 SPI-2 compliant termination for the backplane. These terminators provide termination in both SE modes as well as in LVD mode.

7.3.4 SCSI Interface

The SCSI interface on the LVD/SE SCSI backplane provides the link between the SCSI bus and the microcontroller (containing the intelligence for LVD/SE SCSI backplane). This interface

allows the microcontroller to respond as a SCSI target to implement the SAF-TE protocol. This is implemented using an LSI Logic* 53C80S SCSI interface chip (or equivalent).

7.3.5 Power Control

Without the population of the SAF-TE card, power to the drives is always on. Power control on the LVD/SE SCSI backplane supports the following features.

- Spin-down of a drive when failure is detected and reported (using enclosure services messages) via the SCSI bus. An application or RAID controller detects a drive-related problem that indicates a data risk. In response, it takes the drive out of service and sends a spin down SCSI command to the drive. This decreases the likelihood that the drive is damaged during removal from the hot-swap drive bay. When a new drive is inserted, the power control waits a small amount of time for the drive to be fully seated, and then applies power with a controlled power ramp.
- If system power is on, the LVD/SE SCSI backplane immediately powers off a drive slot when it detects that a drive has been removed. This prevents possible damage to the drive when it is partially removed and re-inserted while full power is available, and disruption of the entire SCSI array from possible sags in supply voltage and resultant current spikes.

7.3.6 FET Short Protection

The FET short protection circuit is useful to protect both 12 volt and 5 volt power control FETs located on the LVD/SE SCSI backplane.

7.3.7 Microcontroller

The microcontroller provides all the intelligence for the LVD/SE SCSI backplane. It is an 80C652 microcontroller, with a built-in I^2C interface. The 80C652 microcontroller uses Flash for program code storage, and static RAM for program variables and buffers.

7.3.8 Device SCSI ID

Each device on a SCSI bus must have a unique SCSI ID. The 3 x 1.6" LVD/SE SCSI backplane device SCSI ID is dependant on whether it is configured as a primary or a secondary backplane. This configuration is defined by the logic of pin 1 on the I^2C connector (J2A1).

Table 7-1: SCSI ID Assignment 3 x 1.6" Backplane

Device	SCSI ID as Primary Backplane I^2C* Connector (J2A1) Pin1=1	SCSI ID as Secondary Backplane I^2C Connector (J2A1) Pin1=0
Drive 1	0x0H	0x8H
Drive 2	0x1H	0x9H
Drive 3	0x2H	0xAH

Table 7-2: SCSI ID Assignment 5 x 1" Backplane

Device	SCSI ID as Primary Backplane I^2C* Connector (J2A1) Pin1=1

Device	SCSI ID as Primary Backplane I^2C* Connector (J2A1) Pin1=1
Drive 1	0x0H
Drive 2	0x1H
Drive 3	0x2H
Drive 4	0x3H
Drive 5	0x4H

7.3.9 Hard Drive Fault LED

The hot-swap controller is responsible for turning the drive fault LEDs on or off according to the states specified via commands received via SAF-TE and the IMB. The drive fault LEDs are yellow and indicate failure status for each drive. The LEDs are physically located on the LVD/SE SCSI backplane, and are driven from the backplane.

During initialization, the microcontroller flashes the LEDs for 2s to signal that POST completed successfully.

Additionally, a green LED is turned on when the respective drive is accessed.

7.3.10 IMB (I^2C* bus)

The I^2C bus is a system-wide server management bus. It provides a way for various system components to communicate independently of the standard system interfaces (e.g., PCI bus or processor/memory bus). The I^2C bus controller is integrated into the microcontroller.

7.3.11 Fan

The LVD/SE SCSI backplane supports up to two tach fans with a digital-output that can be used by the microcontroller to assess the fans' operating condition before total failure (which may result in collateral hardware damage). Microcontroller program code is responsible for monitoring the fans' speed (fan speed is directly controlled from backplane), and reporting of fans condition via the I^2C bus.

It is responsibility of the HSC to report fan speed. Fan speed is sensed by the HSC and compared against a low speed threshold. The HSC issues a message on the IMB when the fan speed falls below this threshold. If a fan is not working it should be replaced; the backplane does not detect second fan failure.

7.3.12 Temperature

The DS1624 on the SAF-TE add-in card provides a temperature sensor in the center of the SAF-TE add-in card. This is accessed by a private I^2C bus.

7.3.13 Serial EEPROM

The DS1624 provides 256 bytes of non-volatile storage. This is used to hold the serial number, part number, FRU inventory information and miscellaneous application code about the LVD/SE SCSI backplane that is used by firmware. This is accessed by a private I^2C bus.

7.4 Firmware Information

This section describes firmware information for the SPKA4 hot-swap SCSI backplane. The information in this section is an overview only.

The firmware for the SPKA4 hot-swap SCSI backplane is stored in the Flash ROM. It is divided into two sections, the 8 KB boot block area and the 24 KB operational code area. The boot block area contains the basic IMB communication routines and the firmware transfer commands. The code in this area is stored permanently. The operational code area contains the run-time code, including the SCSI and SAF-TE routines, monitoring routines, and IMB routines. All code in this area can be updated using the firmware transfer commands.

7.5 Interface Specifications

This section specifies electrical characteristics of the connector pins.

7.5.1 SCSI Input Connector 68P

The SCSI input connector is a non-shielded device connector.

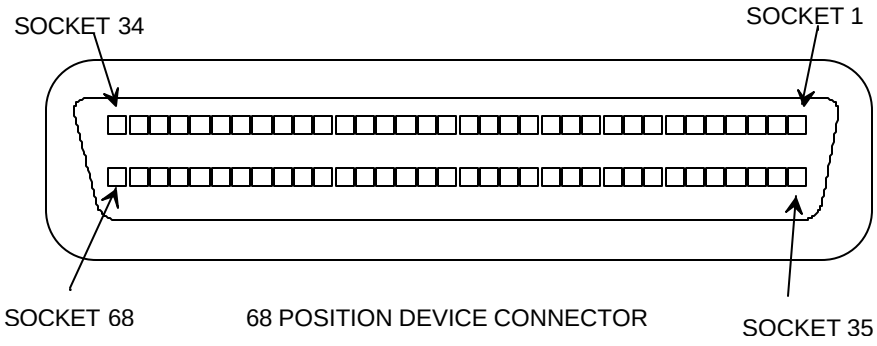

Figure 7-4: SCSI Input Connector 68P Non-shielded

Table 7-3: SCSI Input Connector (J1D1)

Signal Name	Connector Contact Number	SCSI Bus Conductor Number	SCSI Bus Conductor Number	Connector Contact Number	Signal Name
+DB(12)	1	1	2	35	-DB(12)
+DB(13)	2	3	4	36	-DB(13)
+DB(14)	3	5	6	37	-DB(14)
+DB(15)	4	7	8	38	-DB(15)
+DB(P1)	5	9	10	39	-DB(P1)
+DB(0)	6	11	12	40	-DB(0)
+DB(1)	7	13	14	41	-DB(1)
+DB(2)	8	15	16	42	-DB(2)

Signal Name	Connector Contact Number	SCSI Bus Conductor Number	SCSI Bus Conductor Number	Connector Contact Number	Signal Name
+DB(3)	9	17	18	43	-DB(3)
+DB(4)	10	19	20	44	-DB(4)
+DB(5)	11	21	22	45	-DB(5)
+DB(6)	12	23	24	46	-DB(6)
+DB(7)	13	25	26	47	-DB(7)
+DB(P)	14	27	28	48	-DB(P)
GROUND	15	29	30	49	GROUND
GROUND	16	31	32	50	GROUND
RESERVED	17	33	34	51	RESERVED
RESERVED	18	35	36	52	RESERVED
RESERVED	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
+ATN	21	41	42	55	-ATN
GROUND	22	43	44	56	GROUND
+BSY	23	45	46	57	-BSY
+ACK	24	47	48	58	-ACK
+RST	25	49	50	59	-RST
+MSG	26	51	52	60	-MSG
+SEL	27	53	54	61	-SEL
+C/D	28	55	56	62	-C/D
+REQ	29	57	58	63	-REQ
+I/O	30	59	60	64	-I/O
+DB(8)	31	61	62	65	-DB(8)
+DB(9)	32	63	64	66	-DB(9)
+DB(10)	33	65	66	67	-DB(10)
+DB(11)	34	67	68	68	-DB(11)

7.5.1.1 SCSI SCA-2 Drive Connector

In this board the SCA-2 press-fit connector is used on the secondary side of the board. The pinout is the same as SCA1. Connector pin assignment is for the current draft SFF-8046 Rev. 1.1 document.

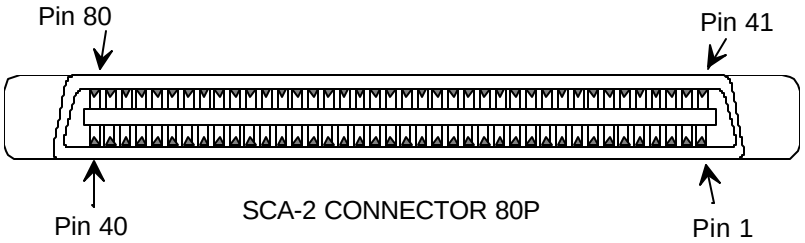

Figure 7-5: SCA-2 Connector 80P

Table 7-4: SCA-2 Connectors (J3E1, J3D1, J3C1, J3B1, J3A1)

	80-pin connector contact and signal name		Cable conductor numbers are not applicable		80-pin connector contact and signal name	
1	12V PreCharge	(L)		(L)	12V Ground	41
2	12V	(S)		(L)	12V Ground	42
3	12V	(S)		(L)	12V Ground	43
4	12V	(S)		(S)	Mated 1	44
5	3.3V	(S)		(L)	3.3V PreCharge	45
6	3.3V	(S)		(L)	DIFFSNS	46
7	-DB(11)	(S)		(S)	+DB(11)	47
8	-DB(10)	(S)		(S)	+DB(10)	48
9	-DB(9)	(S)		(S)	+DB(9)	49
10	-DB(8)	(S)		(S)	+DB(8)	50
11	-I/O	(S)		(S)	+I/O	51
12	-REQ	(S)		(S)	+REQ	52
13	-C/D	(S)		(S)	+C/D	53
14	-SEL	(S)		(S)	+SEL	54
15	-MSG	(S)		(S)	+MSG	55
16	-RST	(S)		(S)	+RST	56
17	-ACK	(S)		(S)	+ACK	57
18	-BSY	(S)		(S)	+BSY	58
19	-ATN	(S)		(S)	+ATN	59
20	-DB(P)	(S)		(S)	+DB(P)	60
21	-DB(7)	(S)		(S)	+DB(7)	61
22	-DB(6)	(S)		(S)	+DB(6)	62
23	-DB(5)	(S)		(S)	+DB(5)	63
24	-DB(4)	(S)		(S)	+DB(4)	64
25	-DB(3)	(S)		(S)	+DB(3)	65
26	-DB(2)	(S)		(S)	+DB(2)	66
27	-DB(1)	(S)		(S)	+DB(1)	67
28	-DB(0)	(S)		(S)	+DB(0)	68
29	-DB(P1)	(S)		(S)	+DB(P1)	69
30	-DB(15)	(S)		(S)	+DB(15)	70
31	-DB(14)	(S)		(S)	+DB(14)	71
32	-DB(13)	(S)		(S)	+DB(13)	72
33	-DB(12)	(S)		(S)	+DB(12)	73
34	5V	(S)		(S)	Mated 2	74
35	5V	(S)		(L)	5V Ground	75
36	5V PreCharge	(L)		(L)	5V Ground	76
37	Spindle Sync	(L)		(L)	Active LED Out	77
38	RMT_START	(L)		(L)	DLYD_START	78
39	SCSI ID (0)	(L)		(L)	SCSI ID (1)	79
40	SCSI ID (2)	(L)		(L)	SCSI ID (3)	80

7.5.1.2 I²C* Connector

Table 7-5. I²C Connector (J2A1)*

Pin	Signal
1	I2C_SDA
2	Ground
3	I2C_SCLK
4	I2C_ADDR_CNTRL

7.5.1.3 Power Connector

Table 7-6. Power Connector (J4A1, J3A2)

Pin	Signal
1	12V
2	Ground
3	Ground
4	+5V

7.5.1.4 Fan 3-pin Connector

There are two 3-pin fan connectors on the backplane. The table below shows the pinout of each connector. Fan power is defaulted to a voltage close to +12V and can be controlled by turning off the SAF-TE card.

Table 7-7. Fan Connector

Pin	Signal (J2A2)	Signal (J2A3)
1	Ground	Ground
2	FAN1 (tach)	FAN2 (tach)
3	Fan power	Fan power

7.5.1.5 SAF-TE PCI Connector Interface

The PCI connector interfaces the LVD bus to the AIC3860 on the SAF-TE card.

Table 7-8 PCI Connector (J5C1)

Pin	Signal	Pin	Signal
A1	Ground	B1	Ground
A2	LVD_SCSI: 1	B2	LVD_SCSI: 0
A3	LVD_SCSI: 28	B3	LVD_SCSI: 27
A4	LVD_SCSI: 3	B4	LVD_SCSI: 2
A5	LVD_SCSI: 30	B5	LVD_SCSI: 29
A6	LVD_SCSI: 5	B6	LVD_SCSI: 4
A7	LVD_SCSI: 32	B7	LVD_SCSI: 31
A8	LVD_SCSI: 7	B8	LVD_SCSI: 6
A9	LVD_SCSI: 34	B9	LVD_SCSI: 33
A10	LVD_SCSI: 9	B10	LVD_SCSI: 8

Pin	Signal	Pin	Signal
A11	LVD_SCSI: 36	B11	LVD_SCSI: 35
A12	LVD_SCSI: 11	B12	LVD_SCSI: 10
A13	LVD_SCSI: 38	B13	LVD_SCSI: 37
A14	LVD_SCSI: 13	B14	LVD_SCSI: 12
A15	LVD_SCSI: 40	B15	LVD_SCSI: 39
A16	LVD_SCSI: 15	B16	LVD_SCSI: 14
A17	LVD_SCSI: 42	B17	LVD_SCSI: 41
A18	LVD_SCSI: 17	B18	LVD_SCSI: 16
A19	LVD_SCSI: 44	B19	LVD_SCSI: 43
A20	LVD_SCSI: 19	B20	LVD_SCSI: 18
A21	LVD_SCSI: 46	B21	LVD_SCSI: 45
A22	LVD_SCSI: 21	B22	LVD_SCSI: 20
A23	LVD_SCSI: 48	B23	LVD_SCSI: 47
A24	LVD_SCSI: 23	B24	LVD_SCSI: 22
A25	LVD_SCSI: 50	B25	LVD_SCSI: 49
A26	LVD_SCSI: 25	B26	LVD_SCSI: 24
A27	LVD_SCSI: 52	B27	LVD_SCSI: 51
A28	LVD_SCSI: 53	B28	LVD_SCSI: 26
A29	Ground	B29	Ground
A30	DRVPRSN:0	B30	DRVACT:0
A31	DRVPRSN:1	B31	DRVACT:1
A32	DRVPRSN:2	B32	DRVACT:2
A33	DRVPRSN:3	B33	DRVACT:3
A34	DRVPRSN:4	B34	DRVACT:4
A35	Ground	B35	Ground
A36	DIFFSENSE	B36	PWRON:0
A37	FAN_CNTRL	B37	PWRON:1
A38	FAN1_TACH	B38	PWRON:2
A39	FAN2_TACH	B39	PWRON:3
A40	Ground	B40	PWRON:4
A41	IMB_SDA	B41	Ground
A42	IMB_CLK	B42	VCC
A43	I2C_ADDR_CNTRL	B43	VCC
A44	Ground	B44	Ground
A45	Ground	B45	Ground
A46	Ground	B46	Ground
A47	Ground	B47	+12V
A48	Ground	B48	+12V
A49	Ground	B49	Ground
A50	Ground	B50	Ground
A51	Ground	B51	Ground
A52	Ground	B52	Ground
A53	Ground	B53	Ground
A54	Ground	B54	Ground
A55	Ground	B55	Ground
A56	Ground	B56	Ground
A57	Ground	B57	Ground

Pin	Signal	Pin	Signal
A58	Ground	B58	Ground
A59	Ground	B59	Ground
A60	Ground	B60	Ground
A61	Ground	B61	Ground
A62	Ground	B62	Ground

7.5.2 Cables

7.5.2.1 Flat Ribbon Cables

- One wide SCSI cable from the embedded PCI SCSI controller card on the baseboard.
- One cable which connects I^2C from either the front panel or baseboard.

7.5.2.2 Wire Bundles

- Two power cables, from peripheral devices to the disk backplane.
- Two fan cables, from fans to the disk backplane. (Optional)

8. Front Panel Board

The front panel is located in the upper portion of the right side of the system. The front panel contains four momentary switches and five LEDs. The four switches control Power On/Off, Sleep mode, System Reset, and NMI. These switches are behind the front door of the bezel. The NMI switch is accessible via a small hole in the front of the chassis and requires a small instrument to push it.

The five front panel LEDs are: a green Power On LED, a green NIC activity LED, a green HDU activity LED, a yellow system temperature fault (system over-temperature, fan fail) LED, and a yellow system fault (power supply, hard drive) LED. These LEDs are visible through the bezel. The fault LEDs will blink for a non-critical fault and be on continuously for a critical fault. Two of the five LEDs provide multi-mode indications. The power LED indicates system power in a steady-on state and Advanced Configuration and Power Interface (ACPI) sleep mode when blinking. Likewise the Cooling Fault LED indicates a fan failure when blinking and an over temperature situation in the chassis when in the steady-on state. The Network Interface Card (NIC) Activity LED is on during network activity. The two remaining LEDs indicate any system hard drive activity and a power fault. There is also a loudspeaker mounted on the front panel.

The front panel also contains three connectors. A 20-pin connector provides control and status information to/from the baseboard via the Fan Distribution Board. Additionally, there are two connectors for chassis intrusion switches.

Table 8-1: Front Panel Features

Feature	Function
Switches:	
Power	Toggle system power.
Sleep	Activate sleep mode.
Reset	Reset system.
NMI	Assert NMI to baseboard.
LED Indicators:	
Power	Green, indicates system power on, blinks in sleep mode.
NIC Activity	Green, indicates network activity.
Hard Drive Activity	Green, indicates any system hard drive activity.
Power Fault / HD Fault	Yellow, indicates power supply failure OR a SCSI hard drive failure.
Cooling Fault	Yellow, indicates any over temperature, blinks if any system fan fails.
Connectors:	
Fan Distribution Conn	Interconnect to baseboard signals via the Fan Distribution Board.
Chassis Intrusion	Interconnect to chassis intrusion switches.

8.1 Connector Pinout

8.1.1 Fan Distribution Board/Front Panel Interface (J3)

Table 8-2: Fan Distribution Board/Front Panel Interface

Pin #	I/O	Description
1	I	5V pulse speaker input
2	PWR	GND
3	O	TTL High True = chassis intrusion
4	I	TTL Low true = hard disk activity
5	PWR	5V VCC
6	O	TTL Low True = toggle ACPI sleep
7	I	TTL Low True = cooling fault condition
8	I	TTL Low True = system power on condition for SKA4 baseboard TTL pulse = system in sleep mode
9	I	TTL Low True = power fault condition
10	PWR	GND
11	I/O	I^2C – SDA
12	O	TTL Low True = NMI to CPU
13	I/O	I^2C – SCL
14	O	TTL Low True = reset system
15	PWR	5V VCC Standby
16	O	TTL Low True = toggle system power
17	I	TTL Low True = network activity
18	PWR	GND
19	-	NC
20	-	NC

8.1.2 Chassis Intrusion Switch Connector Interface (J1, J2)

Table 8-3: Chassis Intrusion Switch Connector Interface

Pin #	I/O	Description
1	O	TTL High True = Chassis switch
2	PWR	Chassis switch GND
3	O	TTL High True = Chassis switch

8.2 Signal Descriptions

Table 8-4: Signal Descriptions

Signal Name	Type	Description
POWER_SW_L	O	Toggle power to main board
RESET_SW_L	O	Reset main board
NMI_SW_L	O	Execute Non-Maskable Interrupt
SLEEP_SW_L	O	Toggle ACPI sleep mode
POWER_LED_L	I	System main power on OR system in sleep mode (blink)

Signal Name	Type	Description
NIC_ACT_L	I	Network activity
HD_ACT_L	I	Accessing hard drive
POWER_FAULT_L	I	Power supply failure OR SCSI hard drive failure
COOLING_FAULT_L	I	System over temperature OR fan failure (blink)
SPEAKER_IN	I	Speaker input signal
SM_IMB_5V_SDA	I/O	I2C serial data
SM_IMB_5V_SCL	I/O	I2C clock
CHASSIS_INTR	I/O	Unauthorized chassis intruder detected
SB5V	PWR	5V Standby power
VCC	PWR	5V power
GND	PWR	Ground

8.3 SKA4 Front Panel Mechanical Outline

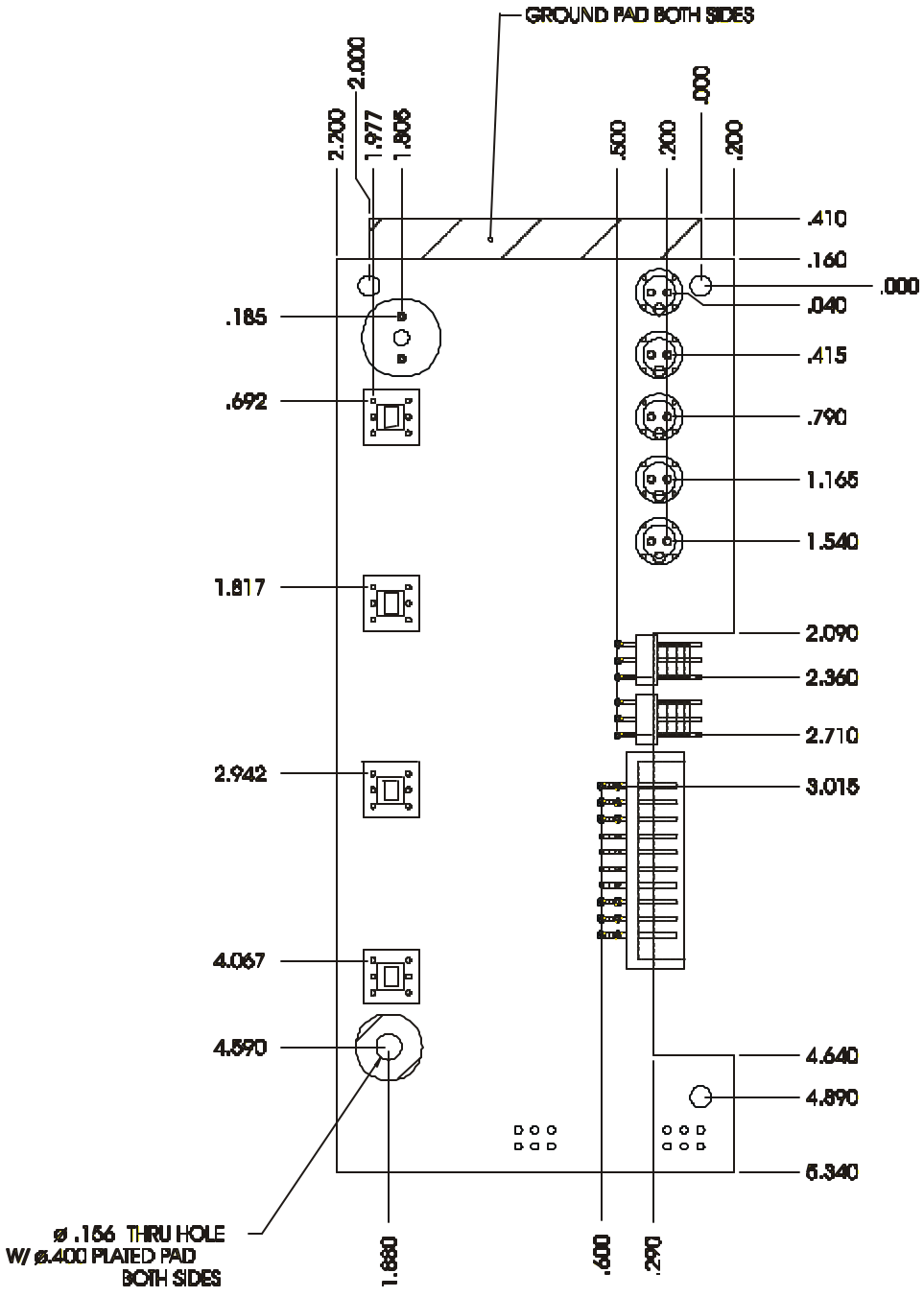

Figure 8-1: SKA4 Front Panel Mechanical Specification

9. SKA4 Board Set

9.1 SKA4 Architecture Overview

The E-bay for the SPKA4 MP chassis was designed to incorporate the SKA4 board set. Please refer to the *SKA4 Baseboard and Memory Board Technical Product Specification* for a detailed description of the system baseboard.

10. System Interconnection

10.1 I/O Panel Connectors

- PS/2 keyboard connector.
- PS/2 mouse connector.
- Two 9-pin serial ports.
- 25-pin parallel port.
- 15-pin video port.
- Two USB connectors.
- One LAN connector.

10.2 System Internal Cables

Baseboard to Fan Power Distribution Board

- One 30-wire ribbon cable.

Baseboard to SCSI Devices

- Two 68-pin wide SCSI cables to the hot-swap backplanes and the rear panel (optional).
- One 68-pin wide SCSI cable to the peripheral bay.
- 50-pin narrow SCSI cable to the peripheral bay.

Baseboard to IDE Devices

- One IDE cable to a 5.25" IDE drive and/or CD-ROM.

Baseboard to Floppy Device

- One 2X17 floppy cable to a 3.5" floppy drive.

Power Share Board to Peripheral Devices

- One 20-wire cable for SCSI backplane power, three 5.25" drive bay connectors, floppy drive, and fan power distribution board.

Baseboard to Power Share Board

- One 24-wire cable for baseboard power.
- One 20-wire cable for baseboard power.
- One 14-wire ribbon cable for auxiliary power.

Fan Power Distribution Board to Hot-swap SCSI Backplanes

- Two 1X4 connectors for cabling I^2C from fan distribution to hot-swap SCSI backplanes.

Fan Distribution Board to Front Panel

- One 2X10 connector with 20-wire cable control.

Front Panel Chassis Intrusion Cables

?? Two 2-wire cables from chassis intrusion micro-switches to front panel.

Fan Connectors

?? One 3-pin connector on the power distribution board for optional rear fan.
?? Two 3-pin connectors on each SCSI backplane. One used on each backplane.
?? Four 3-pin connectors on baseboard. Not used.

Hot Plug Indicator

?? One 20-wire ribbon cable from HPIB to baseboard**.**

10.3 System Cabling Diagram

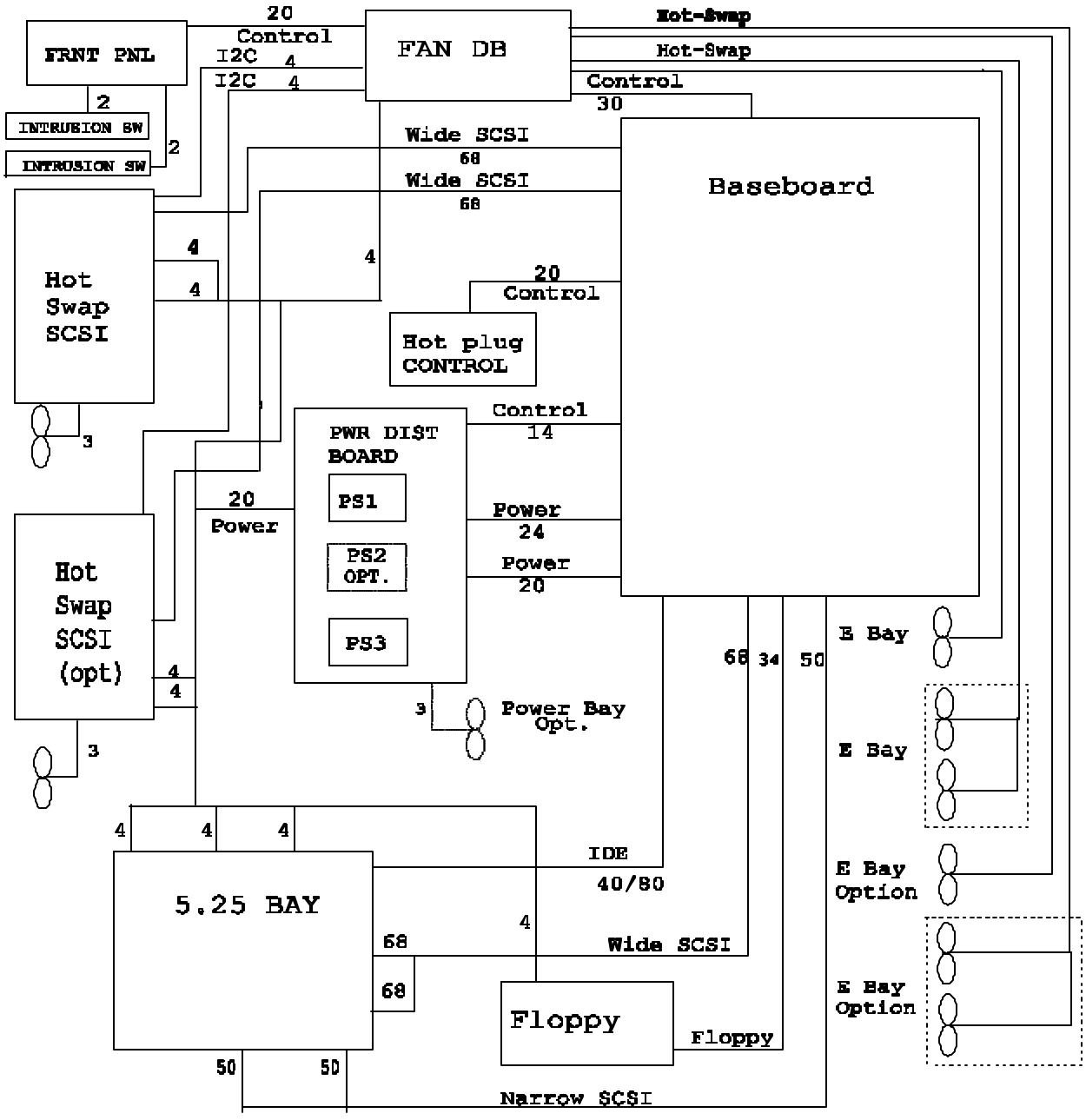

Figure 10-1: SPKA4 MP Server System Cabling Diagram

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11. Certification

11.1 Safety Standards/Certifications

UL 1950 – CSA 950-95

Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)

EN60 950 (CE Mark –LV Directive – 73/23/EEC)

Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)

IEC60 950

Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

EMKO-TSE (74-SEC) 207/94 [1]

Standard for Safety of Information Technology Equipment including Electrical Business Equipment.

11.2 Electromagnetic Compatibility (EMC) Regulations

FCC, Class A

Title 47 of the Code of Federal Regulation, Part 2 and 15, Subpart TBD, pertaining to unintentional radiators. (USA)

CISPR 22, Class A

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)

EN55022 Class A

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)

EN555024 (CE Mark – EMC Directive – 89/336EEC)

ITE Generic Immunity Standard. (Europe)

[1] Summary of Nordic deviations to EN60-950 (Norway, Sweden, Denmark, Finland).

EN61000-3& -2 – Voltage Flicker and Harmonics

RRL Class A (Korea)

BSMI Class A – CNS13438 (Taiwan)

VCCI Class A (ITE) (VCCI Mark)

Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)

ICES-003, Class A

Interference-Causing Equipment Standard, Digital Apparatus. (Canada)

AS/NZS 3548 (C-Tick Mark)

Illustrate Compliance via CISPR 22 EMC Test Report – for Australia and New Zealand.

11.3 Mandatory/Standard Certifications; Registration; Declarations

- UL, cUL Listing.
- German GS Mark.
- CE Mark – Declaration of Conformity.
- VCCI Certification.
- RRL Certification.
- BSMI Certification.
- GOST Certification.
- Industry Canada Declaration.
- MOC (New Zealand) – Declaration of Conformity.
- ACA – (Australia) Declaration of Conformity.

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12. Environmental Limits

12.1 System Office Environment

Table 12-1: System Office Environment Summary

Operating Temperature	+10°C to +35°C. De-rated 0.5°C/1000 ft. Altitude to 10,000 ft. max. Maximum rate of change of 10°C per hour.
Non-operating Temperature	-40°C to +70°C.
Non-operating Humidity	95%, non-condensing @ 30°C.
Acoustic Noise	< 47 dBA with one power supply @28°C+-2°C. < 50 dBA with two power supplies @28°C+-2°C. < 55 dBA with three power supplies @28°C+-2°C.
Operating Shock	No errors with a half sine wave shock of 2 G (with 11-millisecond duration).
Package Shock	Operational after a 12-inch free fall, although cosmetic damage may be present.
ESD	15kV per Intel® Environmental test specification.

12.2 System Environmental Testing

The system will be tested per the Intel® Environmental & Reliability Board and System Validation Test Handbook. These tests shall include:

- Temperature Operating and Non-operating.
- Humidity Non-operating.
- Shock Packaged and Unpackaged.
- Vibration Packaged and Unpackaged.
- AC Voltage, Freq. & Source Interrupt.
- AC Surge.
- Acoustics.
- ESD.

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13. Reliability, Serviceability and Availability

The system is designed to be serviced by qualified technical personnel only.

The desired mean time to repair (MTTR) of the system is 30 minutes including diagnosis of the system problem. To meet this goal, the system enclosure and hardware have been designed to minimize the MTTR.

Following are the maximum times that a trained field service technician should take to perform the listed system maintenance procedures, after diagnosis of the system.

- Remove front cover: 2 minutes.
- Remove rear cover: 1 minute.
- Remove and replace disk drive: 1 minute.
- Remove and replace power supply: 3 minutes.
- Remove and replace drive bay fan: 7 minutes.
- Remove and replace hot-swap fan: 3 minutes.
- Remove and replace fan power distribution board: 5 minutes.
- Remove and replace expansion board: 2 minutes.
- Remove and replace front panel board: 4 minutes.
- Remove and replace baseboard (with no expansion boards): 10 minutes.
- Remove and replace power backplane: 15 minutes.
- Remove and replace SCSI backplane: 15 minutes.
- Replace memory module: 4 minutes.
- Replace/add DIMMs: 6 minutes.
- Replace/add processor: 5 minutes.
- Replace/add ICMB: 2/5 minutes.
- Overall MTTR: 20 minutes.

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Appendix A: Glossary

Word / Acronym	Definition
ACPI	Advanced Configuration and Power Interface
BMC	Baseboard Management Controller
EMC	Electromagnetic Compatibility
FDB	Fan Distribution Board
FRU	Field Replaceable Unit
HSBP	Hot-swap Backplane
MTTR	Mean Time To Repair
NIC	Network Interface Card
OTP	Over-temperature Protection
OVP	Over-voltage Protection
PDB	Power Distribution Board
PFC	Power Factor Correction
PSU	Power Supply Unit
SAF-TE	SCSI Accessed Fault Tolerant Enclosures
USB	Universal Serial Bus

Appendix B: Reference Documents