Intel® Server System SR870BH2

Technical Product Specification

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Disclaimers

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1. Introduction

This document provides an overview of SR870BH2 server system and includes information on chassis hardware, cables, connectors, power subsystem, system boards, and regulatory compliance.

1.1 Document Structure and Outline

This document is organized into the following chapters:

Chapter 1: Introduction
Provides an overview of this document.

Chapter 2: System Overview
Provides an overview of the system hardware.

Chapter 3: System Chassis and Sub-Assemblies
Provides an overview of the chassis and major sub-assemblies.

Chapter 4: Cables and Connectors
Describes the cables and connectors used to interconnect the S870BH2 board set and the server system components.

Chapter 5: Power Subsystem
Describes the specifications for the power supplies and power distribution board.

Chapter 6: Peripheral board
Describes the peripheral board used in the SR870BH2 server system.

Chapter 7: SCSI Backplane Board
Describes the SCSI backplane board used in the SR870BH2 server system.

Chapter 8: Peripheral Adapter Board
Describes the Integrated Device Electronics (IDE) peripheral device adapter board used in the SR870BH2 server system.

Chapter 9: Regulatory Specifications
Describes system compliance to regulatory specifications.

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2. System Overview

This chapter describes the features of the SR870BH2 server system. This chapter is organized into the following sections:

Section 2.1: System Feature Summary
Provides a list and brief description of the features of the SR870BH2 server system.

Section 2.2: Introduction
Provides an overview and block diagram of SR870BH2 server system.

Section 2.3: External Chassis Features - Front
Describes features located at the front of the SR870BH2 system chassis in detail (buttons, switches, bezel, etc.).

Section 2.4: External Chassis Features - Rear
Describes features located at the rear of the SR870BH2 system chassis in detail (user-accessible connectors).

Section 2.5: System Board Set
Provides an overview of the SR870BH2 system board set.

Section 2.6: Power Subsystem
Provides an overview of the SR870BH2 power subsystem.

Section 2.7: Cooling Subsystem
Describes the SR870BH2 cooling subsystem.

Section 2.8: Server Management
Describes the server management features of the SR870BH2 server system.

Section 2.9: Reliability, Availability and Serviceability (RAS)
Describes the reliability, availability, and serviceability features of the SR870BH2 server system.

Section 2.10: Expansion Support
Describes the expansion support features of the SR870BH2 server system.

Section 2.11: Specifications
Describes the environmental and physical specifications of the SR870BH2 server system.

2.1 System Feature Summary

Table 1 provides a list and brief description of the features of the SR870BH2 server system.

Table 1. SR870BH2 Server System Feature List

Feature	Description	
Compact, high-density system	Rack-mount server with a height of 2U (3 1/2 inches) and a depth of 28 inches	
Configuration flexibility	1-2 way capability in low profile and cost effective packaging Stand-alone system including external I/O slots/disk expansion as needs grow Intel® Itanium 2 processor support 16-GB Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) memory support	
Serviceability	Front access to hot-swap hard disk drives Hot-swap fans Front access to hot-swap power supplies Dockable power to main board System power and reset status LEDs System ID switch on front panel and LEDs on front and back Color-coded parts to identify hot-swap and non-hot-swap serviceable components	
Availability	Three PCI-X slots Three hot-swap 350-W power supplies in a redundant (2+1) configuration Dual redundant power cords (1+1) when 3 power supplies are present Six hot-swap system fans in a redundant (5+1) configuration Two hot-swap 1-inch Ultra*-320 SCSI hard disk drives	
Manageability	Remote management Emergency Management Port (EMP) Intelligent Platform Management Interface (IPMI) 1.5 compliant Wired For Management (WfM) 2.0 compliant Remote diagnostics support	
Upgradeability and investment protection	Supports Itanium 2 processor family Field upgradeable to next generation processor family Multi-generational chassis	
System-level scalability	Up to 16-GB DDR SDRAM (using 2-GB DIMMs) One to two Itanium 2 processors External I/O (3 slots) / disk expansion External SCSI connector	
Front panel	System Power switch and LED System Reset switch System Diagnostic Interrupt (SDINT) switch System ID switch and LED	System Status LED Hard Drive Fault LED LAN1 & LAN2 Status LEDs Video Connector Dual USB 1.1 Ports

2.2 Introduction

SR870BH2 is a compact, high-density, rack mount server system with support for one to two Intel® Itanium 2 processors and 16-GB DDR SDRAM memory. SR870BH2 supports several high availability features such as hot-swap and redundant power supply modules, hot-swap and redundant fans for cooling, and hot-swap hard disk drives. Serviceability features include LED indicators for system, reset, hard drive & LAN status and system identification.

Additional features include video connector and dual USB ports accessible from the front panel. Color-coded parts identify hot-swap and non-hot-swap serviceable components. The scaleable architecture of the SR870BH2 system supports Symmetric Multiprocessing (SMP) and a variety of operating systems.

Figure 1 and Figure 2 show the front and rear isometric views of the system.

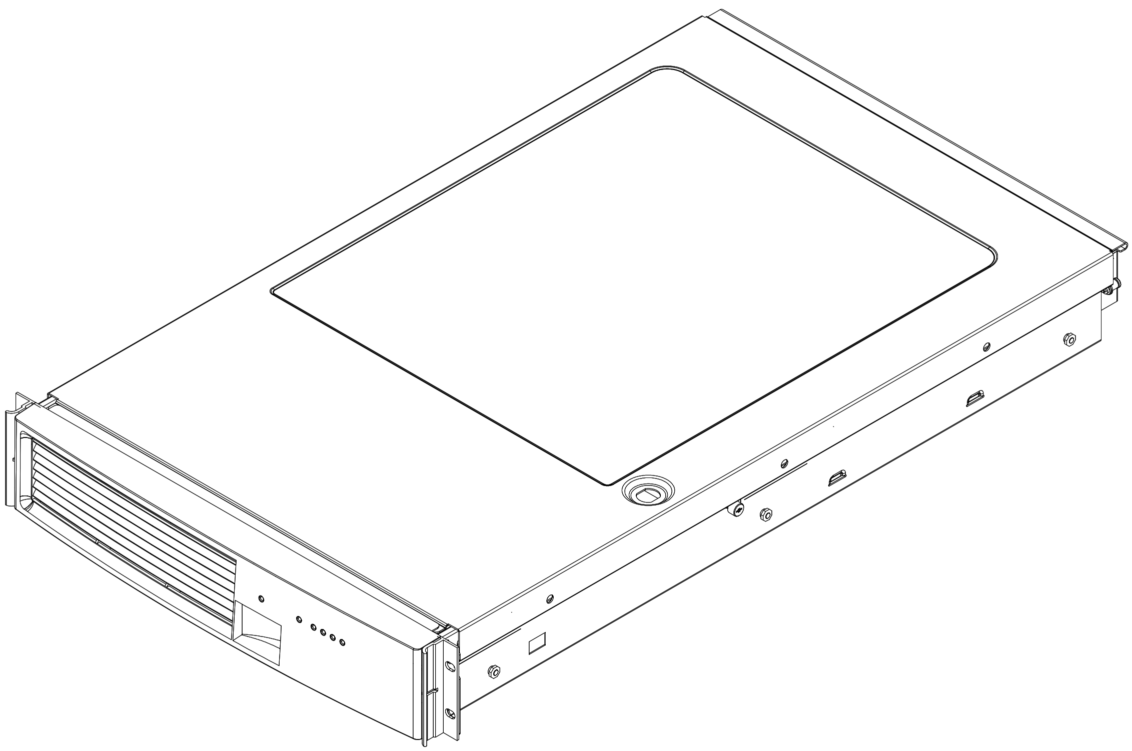

Figure 1. SR870BH2 Server System (Front Isometric View)

The SR870BH2 system is based on the S870BH2 board set and Intel® *E8870* chip set.

The main board contains sockets for installing up to two Itanium 2 processors and supports up to two power pods. It contains connectors for eight DDR SDRAM DIMM slots and supports up to 16 GB of memory as well as the system I/O devices. The main board is installed horizontally in the electronics bay. The electronics bay is installed at the rear of the chassis and mates with the power bay in the front of the chassis.

The PCI riser board plugs vertically to the main board via 2 VHDM connectors and contains three 64-bit PCI slots.

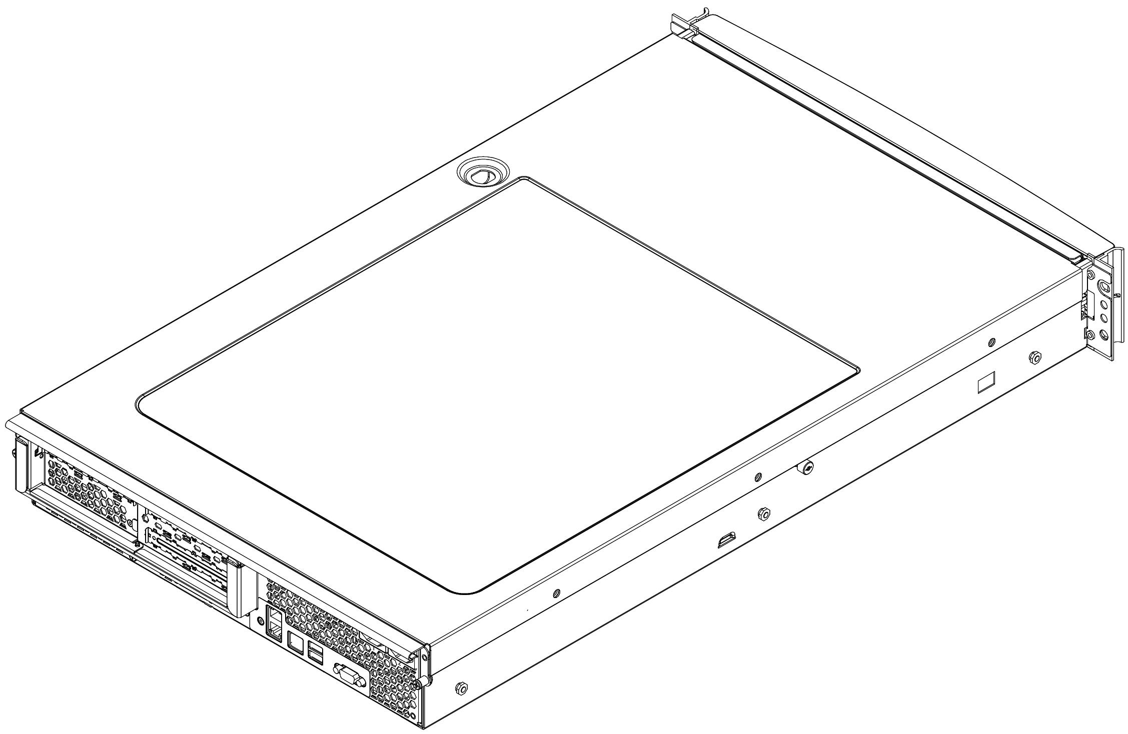

Figure 2. SR870BH2 Server System (Rear Isometric View)

The peripheral bay consists of the SCSI backplane board, two 1-inch SCSI hard disk drive bays, one slim-line (½-inch) DVD/CD drive bay and the front panel. The peripheral bay is installed at the front of the system above the power bay.

The front panel is located on the right of the peripheral bay and provides user interface for system management via switches and status indicator LEDs. Additional status indicator LEDs are located on the peripheral bay, the system fans, and the power supply modules.

The power bay consists of the power supply modules, the AC transfer switch, and the power distribution board. The power bay is installed at the front of the system below the peripheral bay. The system supports up to three Server System Infrastructure (SSI)-compliant hot-swap power supply modules in a 2+1 redundant configuration.

The cooling subsystem contains an array of 6 hot-swap, redundant (5+1) system fans installed in the fan bay The fan bay is part of the power bay and is located towards the middle of the system. System fans plug into connectors provided on the power distribution board which also contains the fan control circuitry. Each system fan contains an individual status indicator LED, illuminating in an amber color to indicate a fan failure.

The front bezel is installed with snap-on features and can be customized to meet Original Equipment Manufacturer (OEM) industrial design requirements. The bezel design allows adequate airflow to cool system components

Figure 3 shows a block diagram of the SR870BH2 server system.

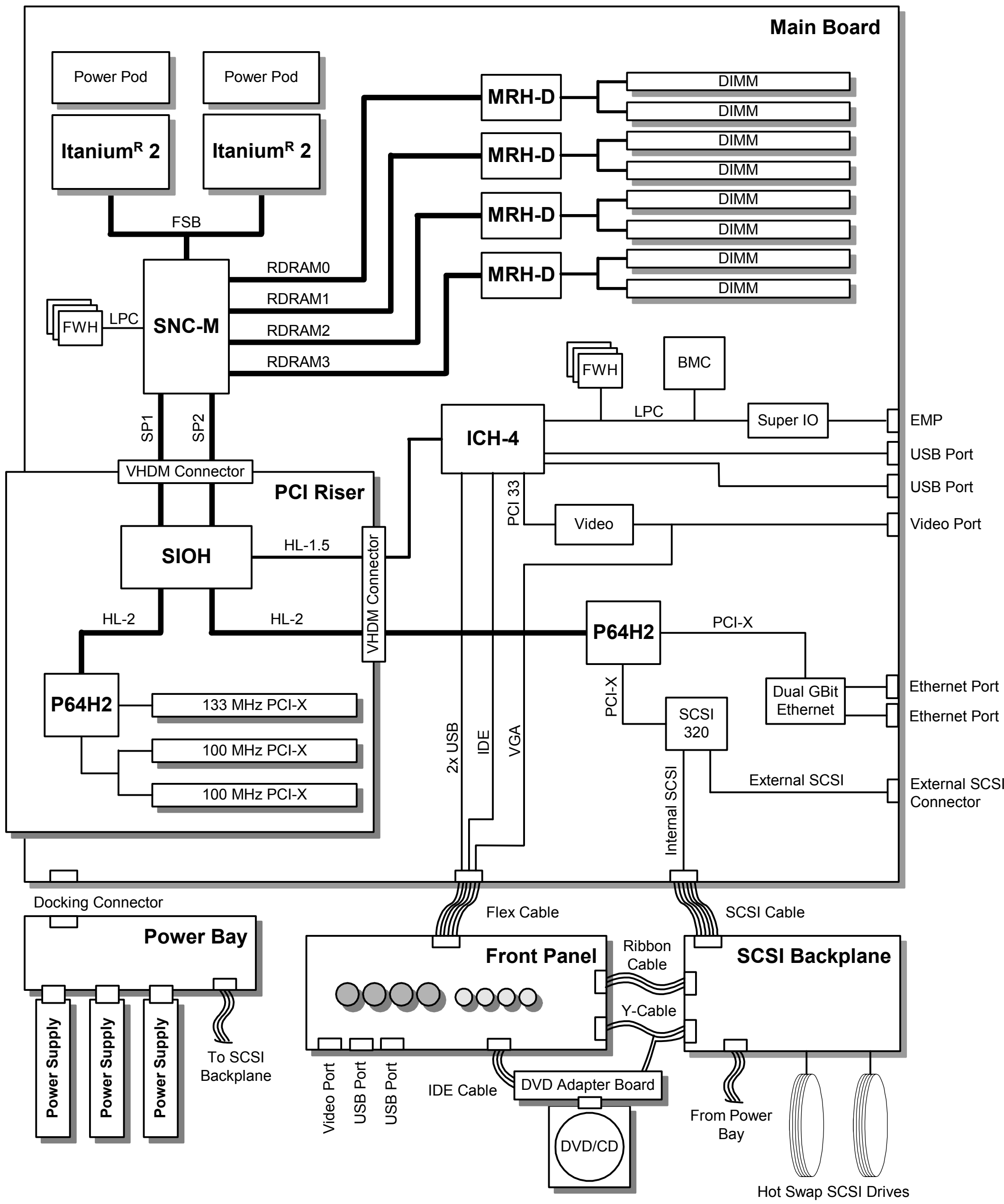

Figure 3. SR870BH2 Server System Block Diagram

2.3 External Chassis Features – Front

Figure 4 shows the front view of the system. Figure 5 shows the front view of the system with the front bezel removed. The front bezel provides access to the following user-accessible areas:

- Front panel swicthes and LEDs
- User accessible connectors (front)
- Peripheral bay
- Power bay (described in Section 2.6)

These areas are described in detail in the following sections.

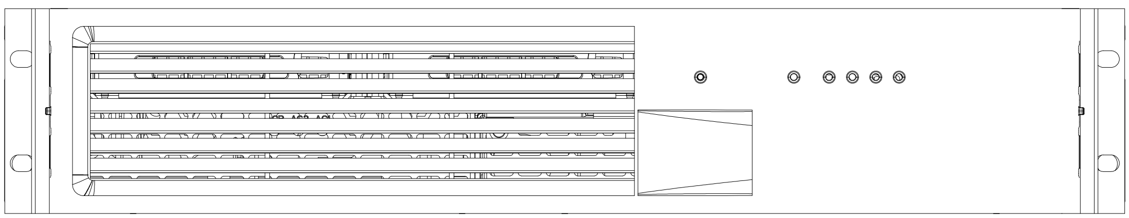

Figure 4. Front View of SR870BH2 Server System

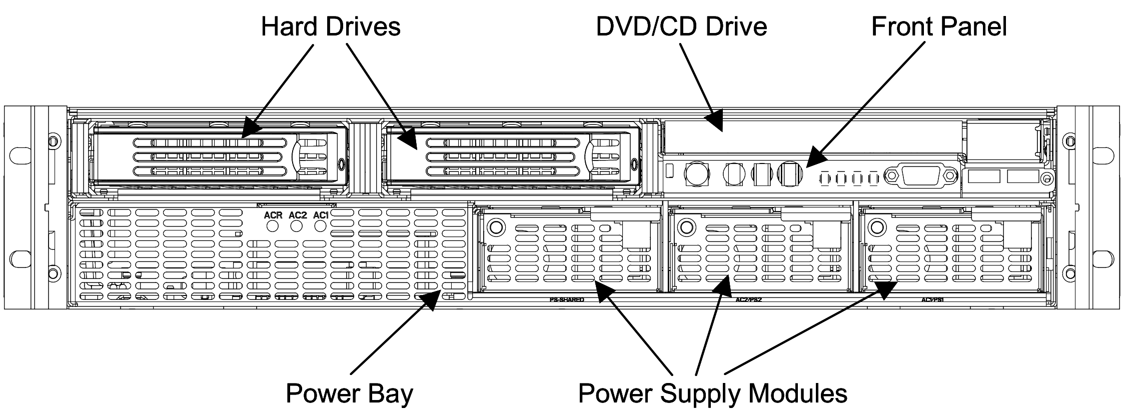

Figure 5. Front View of SR870BH2 Server System (Shown with Bezel Removed)

2.3.1 Front Panel

The front panel contains system control switches and LED status indicators. It also contains one video connector, two USB 1.1 ports and the system speaker. Front panel features are shown in Figure 6 and described in Table 2. The front bezel must be removed to access the front panel swicthes and connectors. All LEDs are visible with the front bezel installed. The peripheral board is installed in the peripheral bay. Refer to Chapter 6 for a detailed description of the peripheral board.

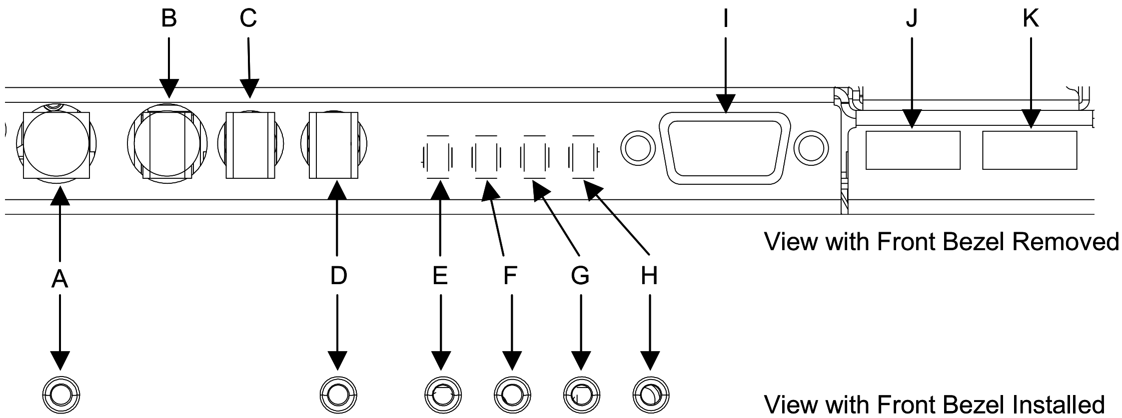

Figure 6. Front Panel Features

Table 2. Front Panel Details

<table>
<tr><th>Item</th><th>Feature</th><th colspan="3">Description</th></tr>
<tr><td colspan="5">Front Panel Switches and LED Indicators</td></tr>
<tr><td rowspan="6">A</td><td rowspan="6">System Power switch & LED</td><td colspan="3">Toggles system power.</td></tr>
<tr><td>LED</td><td>State</td><td>ACPI</td></tr>
<tr><td>Off</td><td>Power off</td><td>No</td></tr>
<tr><td>On</td><td>Power on</td><td>No</td></tr>
<tr><td>Off</td><td>S5</td><td>Yes</td></tr>
<tr><td>On</td><td>S0</td><td>Yes</td></tr>
<tr><td>B</td><td>System Reset switch</td><td colspan="3">Resets the system.</td></tr>
<tr><td>C</td><td>SDINT (System Diagnostic Interrupt) switch</td><td colspan="3">Asserts SDINT.</td></tr>
<tr><td>D</td><td>System ID switch and LED (Blue)</td><td colspan="3">See Section 2.3.1.1 for details.</td></tr>
<tr><td rowspan="7">E</td><td rowspan="7">System Status/Fault LED (Green/Amber)</td><td colspan="3">Indicates system status.</td></tr>
<tr><td>LED</td><td>State</td><td>Description</td></tr>
<tr><td>Off</td><td>Not ready</td><td>Post err/NMI Ev/CPU missing</td></tr>
<tr><td>Green, On</td><td>Ready</td><td>No Alarms</td></tr>
<tr><td>Green, Blinking</td><td>Ready – Degraded</td><td>CPU Fault, DIMM killed</td></tr>
<tr><td>Amber, On</td><td>Critical Alarm</td><td>Critical of Pwr Flt, Fan, Voltage, and Temperature failures.</td></tr>
<tr><td>Amber, Blinking</td><td>Non-Critical Alarm</td><td>Non-Critical of redundant Pwr Flt, redundant Fan, Voltage, and Temperature failures.</td></tr>
<tr><td>F</td><td>Hard Drive Fault LED (Amber)</td><td colspan="3">Indicates Hard drive subsystem fault status.</td></tr>
</table>

Item	Feature	Description		
		LED	***State***	***Description***
		Off	Drive Missing	Slot Empty, Online, Prepare for removal.
		On	Inactive	Drive Failed
		Blinking		Drive Identity, Rebuild, Predictive Fail, Rebuild Interrupt or Rebuild on empty slot.
G, H	LAN1, LAN2 Status LEDs (Green)	Indicates LAN activity status.		
		LED	***State***	***Description***
		Off	Idle / not connected	No physical connection
		On	Inactive / Link	Link - No network Access
		Blinking	Active	Access to network
Front Panel Connectors				
I	Video connector	Video port, standard VGA compatible, 15-pin connector		
J	USB3 connector	USB port 3, 4-pin connector		
K	USB4 connector	USB port 4, 4-pin connector		

2.3.1.1 System ID Switches and LEDs

The system contains two System ID switches and two blue System ID LEDs. One switch/LED pair is located on the front panel and a second switch/LED pair is located at the rear of the system. The System ID LEDs can be activated either by the System ID switches or remotely via server management software to easily locate/identify the system.

Table 3. System ID LED Details

LED State	Description
Off	System ID inactive.
On	System ID active via switch.
Blinking	System ID active via remote command.

Pressing a switch turns the LEDs on *Solid*. Pressing a switch again turns them off.

If the LEDs were activated by a switch, they cannot be turned off remotely. If the LEDs were activated remotely, the switches cannot turn them off.

2.3.2 User-Accessible Connectors (Front)

One video connector and 2 USB ports are accessible from the front of the SR870BH2 system as listed in Table 2.

2.3.3 Peripheral Bay

Peripheral bay, shown in Figure 7, consists of the following:

- SCSI backplane board
- Two 1-inch hot-swap Ultra 320 SCSI hard disk drive bays
- One ½-inch IDE DVD-ROM, CD-ROM or CD-RW drive
- Peripheral board

Note: Installation of an IDE hard disk drive in removable media bays is not supported due to cooling and Electromagnetic Interference (EMI) constraints.

Note: The SR870BH2 peripheral bay has been specifically designed to support only LVD SCSI drives. SE device support is available via the secondary external SCSI channel, located at the rear of the chassis. SE device support is not available in the two SR870BH2 hot-swap peripheral bays.

Note: DVD/CD drive utilizes an ATAPI (IDE) interface, this is not a hot-swap device. System power must be turned off when installing or removing these drives.

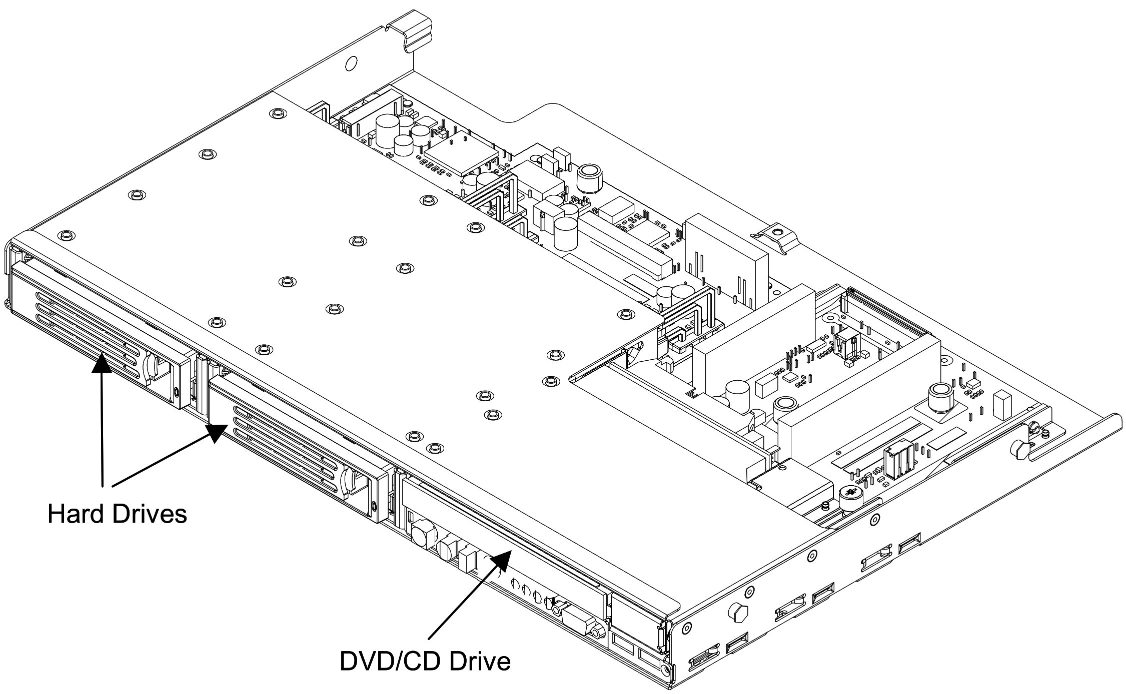

Figure 7. Peripheral Bay

The SCSI backplane board is communicates with the main board via a 68 pin SCSI cable and a Flex cable. It contains two industry standard 80-pin Single Connector Attachment (SCA)-2 connectors for hot-swap hard disk drives. Ultra 320 (or lower) SCSI technology SCA type hard disk drives can be installed in this bay. The backplane is designed to accept hard drives up to 15,000-RPM. SR870BH2 peripheral bay is designed to support Low Voltage Differential (LVD) SCSI disk drives only. Single-Ended (SE) SCSI devices are not supported in the peripheral bay, however SE device suppor is available via the secondary external SCSI channel at the rear of the chassis.

Note: Because all hard disk drives have different cooling, power, and vibration characteristics, Intel will validate specific hard disk drive types in the SR870BH2 system. Refer to the *SR870BH2 Hardware & Operating System Validation List* for a list of these drives.

Hard drive carriers (described in Chapter 3) that accommodate 3.5-inch by 1.0-inch SCSI disk drives are required as part of the hot-swap implementation. The disk drive is attached to the carrier with four fasteners, and is retained in the chassis by a locking handle.

The SCSI backplane board contains a dual color LED for each hard drive to display status as described in Table 4. The LED signal is transmitted to the front of the system via a light pipe integrated in the hard drive carrier.

Table 4. SCSI Hard Drive LED Details

LED State	Description
Green On	The hard drive is powered.
Green Blinking	The hard drive is active.
Yellow/Green Blinking	Indicates a hard drive fault and hard drive is powered.
Yellow/Blank Blinking	Indicates a hard drive fault and hard drive is not powered.

The IDE signals are carried from the peripheral board via a ribbon cable to the IDE adaptor board that interfaces to the ½-inch DVD/CD drive. The DVD/CD drive and the adapter board are installed in plastic carriers as described in Chapter 3 and then installed in the peripheral bay.

The SCSI backplane board performs the tasks associated with hot-swapping of the hard disk drives and enclosure (chassis) monitoring and management, as specified in the *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification*. The SAF-TE-specified features supported by the SCSI backplane board include, but are not limited to, the following:

- Monitoring the SCSI bus for enclosure services messages and acting on them appropriately. Examples of such messages include: Activation of a drive fault indicator; Powering down a drive that has failed or reporting backplane temperature.
- SAF-TE intelligent agent, acts as a proxy for “simple” I^2C* devices (that do not have bus mastering capability) during intra-chassis communications.

Refer to Chapter 7 for a detailed description of the SCSI backplane board.

2.4 External Chassis Features – Rear

Figure 8 shows the rear view of the system. The user-accessible connectors and electronics bay located at the rear of the system are described in the following sections.

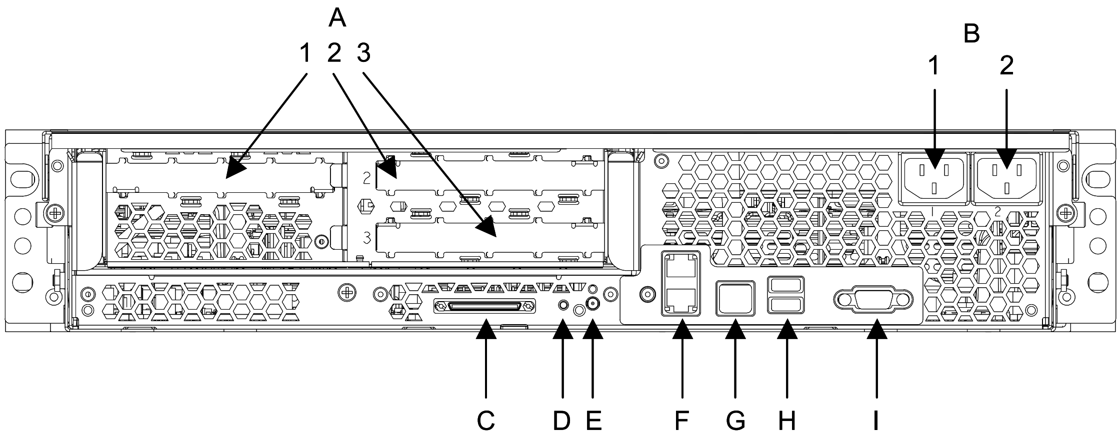

Figure 8. Rear View of System

2.4.1 User-Accessible Connectors, Swicthes and LEDs (Rear)

Table 5 lists the user-accessible connectors at the rear of the SR870BH2 system.

Table 5. User-Accessible Connectors, Switches and LEDs (Rear)

Item	Description	
A	PCI Slots	
	Slot 1	100 MHz, 64-bit PCI-X slot, full length
	Slot 2	100 MHz, 64-bit PCI-X slot, full length
	Slot 3	133 MHz, 64-bit PCI-X slot, full length
B	Two AC input power connectors	
C	External SCSI connector[1]	
D	System ID switch, See Section 2.3.1.1.	
E	System ID LED (blue), See Section 2.3.1.1.	
F	Two LAN ports, RJ45 connector (LAN1 on bottom, LAN2 on top) LAN port LEDs:	
	Status LED (Green)	On – ethernet link is detected Off – no ethernet connection Blinking – ethernet link is active
	Speed LED (Green/Amber dual color)	Off – 10 Mbps Green On – 100 Mbps Amber On – 1000 Mbps
G	Serial port[2], RJ45 connector	
H	Two USB 1.1 ports, 4-pin connectors (USB0 on bottom, USB1 on top)	
I	Video port, standard VGA compatible, 15-pin connector	

Notes:
1. External SCSI bus supports both LVDS and SE signals via the external SCSI connector.
2. EMP access is provided via shared serial port.

2.4.2 Electronics Bay

Electronics Bay, shown in Figure 9 and Figure 10, consists of the following:

- Main board
- PCI Riser board
- 2 Processor and 2 Power Pod locations
- 8 DIMM slots
- Air duct for the processor area
- PCI Riser bracket to support PCI Riser board and PCI cards
- various connectors, switches and LEDs at the rear of the system

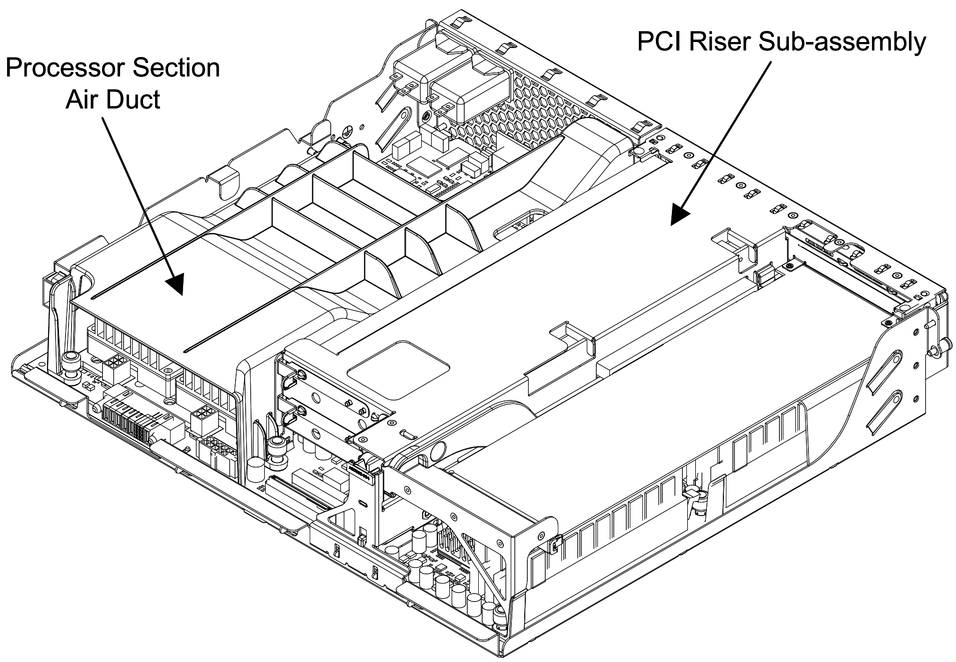

Figure 9. Electronics Bay

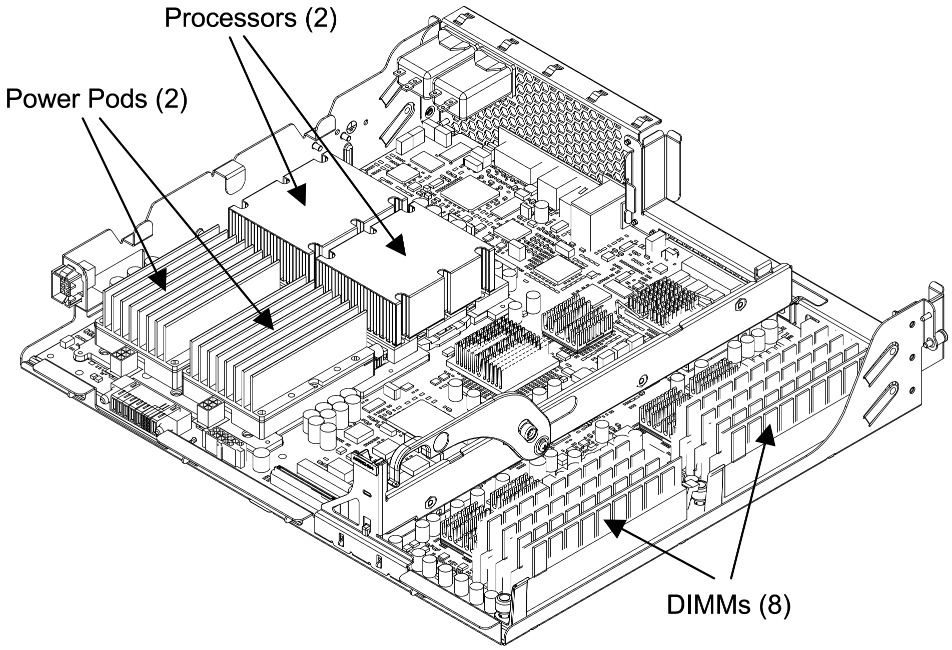

Figure 10. Electronics Bay (with Air Duct & PCI Riser Sub-assembly removed)

2.5 System Board Set

This section highlights the main features of the S870BH2 board set. Refer to the *S870BH2 Board Set External Product Specification* for a detailed description of the board set.

Figure 3 shows the functional blocks of the S870BH2 board set. Major components of the board set include:

- Itanium 2 processors
- E8870 chip set
- High-capacity DDR SDRAM memory
- High-bandwidth I/O subsystem supporting PCI and PCI-X

The S870BH2 board set contains the following boards:

1. Main board
2. PCI Riser board

In addition, the SR870BH2 server contains the following system boards:

3. Peripheral board
4. SCSI Backplane board
5. Peripheral adapter board

6. Power Distribution Board and AC Transfer switch

Boards 1-2 are described in detail in *S870BH2 Board Set External Product Specification*. Additional information and detail regarding Power distribution and AC Transfer switch are can be found in chapter 5 of this document.

2.5.1 Main Board

The main board supports the following features:

- Two Itanium 2 processor sockets
- Two Itanium 2 processor power pod sites
- 8 Eight 184-pin, DDR-SDRAM DIMM sockets
- SNC-M (Scalable Node Controller) of the E8870 chip set
- Four Memory Repeater Hub – DDR (MRH-D) components of the E8870 chip set
- One P64H2 component (to drive SCSI controller and NIC)
- One I/O Control Hub 4 (ICH4) component
  - Four Universal Serial Bus (USB) ports (2 rear, 2 through Front Panel)
  - One IDE bus routed through the Flex cable to the Peripheral board supporting one ATA33 device
- SCSI 320 Controller
- Network Interface Card (NIC) 10/100/1000 Ethernet controller
  - Two LAN ports
- Low Pin Count (LPC) Super I/O*
  - One serial port
- Integrated ATI Rage* XL video controller and memory
  - 2 Video ports (1 rear, 1 through Front Panel)
- 8-MB Flash using four Firmware Hub (FWH) components
- VHDM connectors for PCI Riser board
- Retention mechanism for processors and power pods
- In-Target Probe (ITP) port
- 200 MHz Front Side Bus (FSB)
- Four 400-MHz Rambus channels for memory interface
- Core ratio programming via the SNC-M
- Server management logic support
- Joint Test Action Group (JTAG)/boundary scan support through ITP or external source
- Clock buffering
- Six I^2C system management buses (SMBus)
- Embedded D2D converters
- BMC server management controller
- Power control - Advanced Configuration and Power Interface (ACPI)
- Speaker control
- I^2C logic

- Field Replaceable Unit (FRU) device ID accessed through a private I^2C bus
- Temperature sensors

Refer to *S870BH2 Board Set External Product Specification* for a detailed description of this board.

2.5.2 PCI Riser Board

The PCI Riser board supports the following features:

- One Server I/O Hub (SIOH) component of the E8870 chip set
- One P64H2 component
- Three non-hot-plug PCI slots
  - One 64-bit, 133 MHz PCI-X, full length
  - Two 64-bit, 100 MHz PCI-X, full length
- One integrated D2D
- Server management logic
- I^2C logic
  - Field Replaceable Unit (FRU) device ID accessed through a private I^2C bus
  - Temperature sensor

Refer to *S870BH2 Board Set External Product Specification* for a detailed description of this board.

2.5.3 Peripheral Board

The peripheral board contains switches, LEDs, connectors and speaker for system interface as described in Section 2.3.1. It also routes the IDE bus from the main board to the DVD/CD drive. Refer to Chapter 6 for a detailed description of this board.

2.5.4 SCSI Backplane Board

The SCSI backplane board supports two LVDS hard drives. Its features include:

- Two SCA connectors for hot-swap 1-inch SCSI hard drives
- SCSI accessed fault-tolerant enclosures (SAF-TE) logic

Refer to Chapter 7 for a detailed description of this board.

2.5.5 Power Distribution Board and AC Transfer Switch

The power distribution board and the AC transfer switch are installed in the power bay. The power distribution board provides the interface with the up to three 48 V hot-swap power supply modules. It also contains connectors for six hot-swap system fans. Refer to Chapter 5 for a detailed description of this board.

2.5.6 Peripheral Adapter Board

The DVD/CD adapter board provide the interface between the ½-inch IDE DVD/CD drive and the Peripheral board. This board is described in detail in Chapter 8.

2.6 Power Subsystem

SR870BH2 power subsystem contains the power bay (with the AC transfer switch and the power distribution board), the SSI power supply modules, the embedded D2D converters and the processor power pods. The total power requirement for the SR870BH2 server system exceeds the 240 VA energy hazard limit that defines an operator-accessible area. As a result, only qualified technical individuals should access the processor, memory, and non-hot-swap areas while the system is energized.

2.6.1 Power Bay

The Power Bay shown in Figure 11 is located in the lower front half of the system. Redundant power status LED indicators are in the left portion of the power bay and three hot-swap power supply modules dock into the three bays on the right. The power bay also contains the fan bay to support 6 system fans.

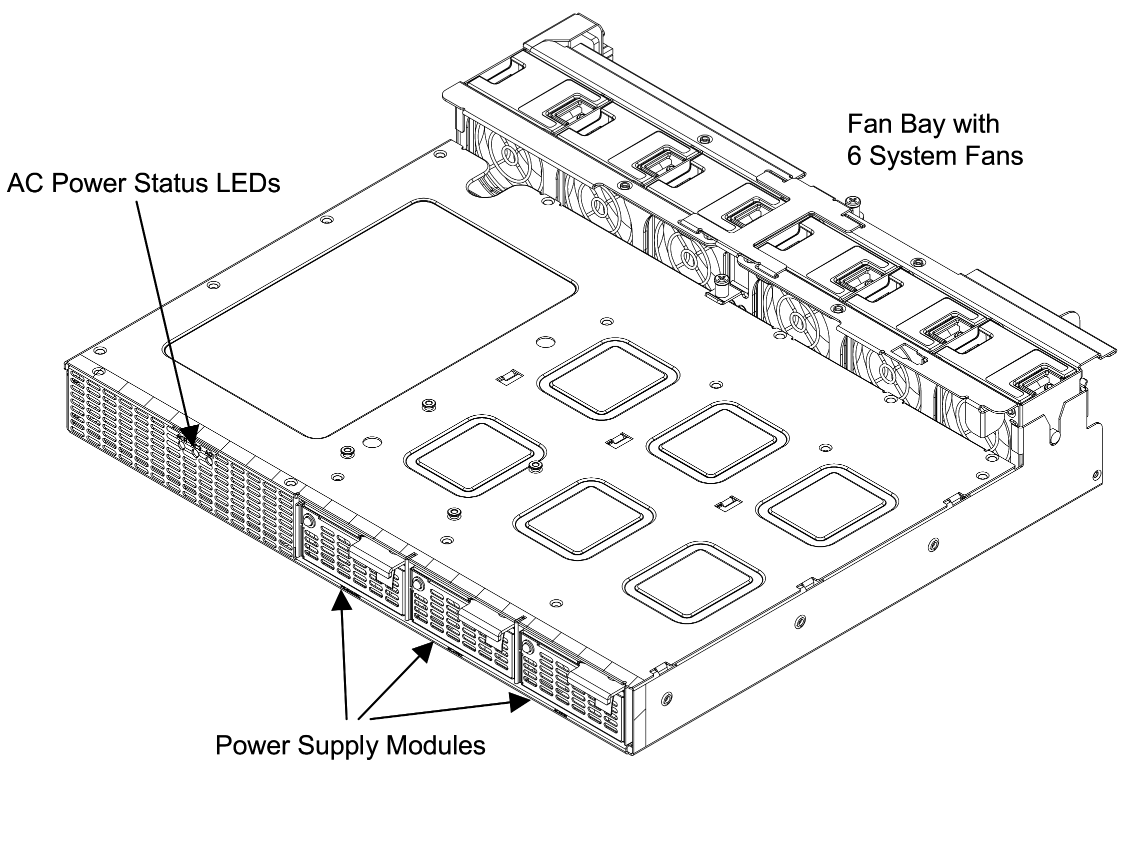

Figure 11. Power Bay

The power subsystem can be configured as following:

- Three power supply modules installed, (2+1) redundancy for a fully configured system
- Two power supply modules installed, non-redundant for a fully configured system

Note: The power supply modules must be populated in locations starting from the right to left. The left power supply module is optional (non-redundant configuration). If no module is installed in the left slot, a filler panel is required for proper system cooling.

Two power supply modules are capable of handling the worst-case power requirements for a fully configured SR870BH2 server system. This includes two Itanium 2 processors, 16 GB of memory, three PCI add-in cards, two hard disk drives, and a DVD/CD drive.

When the system is configured with three power supply modules, the hot-swap feature allows the user to replace a failed power supply module while the system is running, without affecting the system functionality.

The power subsystem receives AC power through two power cords. When three power supply modules and two power cords are installed, the system supports (1+1) power cord redundancy. This feature allows the system to be powered by two separate AC sources. In this configuration, the system will continue to function without interruption if one of the AC sources was to fail.

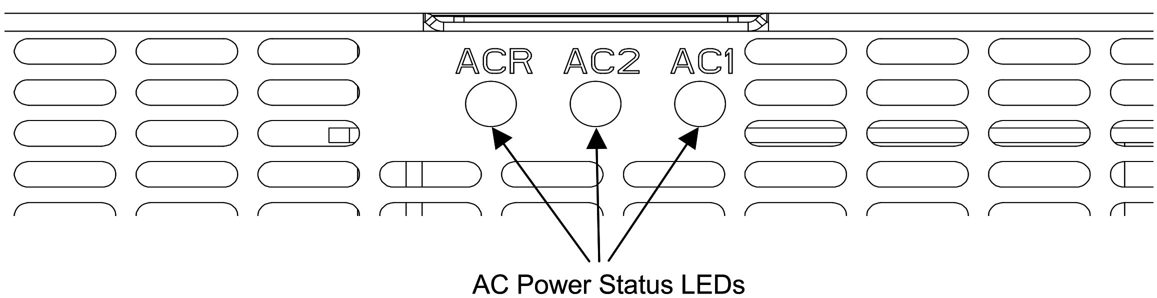

Figure 12. AC Power Status LEDs

Table 6. AC Power Status LED Details

LED	Description
AC1 (green)	On - AC input #1 available. Off - AC input #1 unavailable or below voltage threshold to power up the system.
AC2 (green)	On - AC input #2 available. Off - AC input #2 unavailable or below voltage threshold to power up the system.
ACR (green)	On - redundant feature is available. Off - redundant feature is not available

The power redundancy feature requires all of the following four conditions be present.

- AC input #1 available
- AC input #2 available
- Power good signals asserted from all three power supply modules
- TS-OK signal is asserted

Refer to *Chapter 5: Power Subsystem* of this document for detailed specifications.

2.6.2 Power Supply Module

The hot-swap, SSI-compliant power supply modules are rated at 650-watts over an input range of 200-240 VAC and 100-127 Alternating Current Voltage (VAC). These modules are accessed from the front of the chassis. Refer to *Chapter 5: Power Subsystem* of this document for detailed specifications.

2.6.3 Processor Power Pod

A dedicated power pod supplies power to each processor. The input connector of the power pod is connected to the 12 V power rail on the main board via a short Y-cable. One Y-cable supports two power pods mounted on the main board. The output connector of the power pod mates directly with the processor package.

2.7 Cooling Subsystem

A single bank of six (6) Delta FFB0612EHE-S18Z hot-swap system fans provide the airflow necessary to cool the SR870BH2 system components. These fans are installed in the Fan Bay located in the Power Bay. Figure 13 shows the cooling subsystem layout.

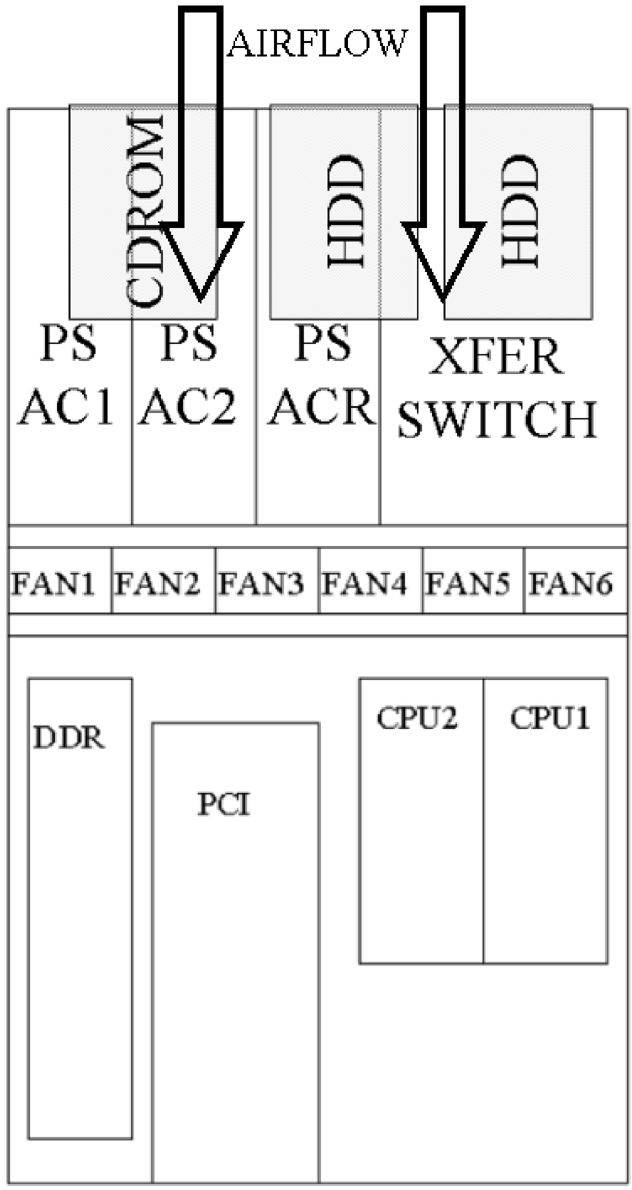

Figure 13. Cooling Subsystem Layout

The cooling subsystem is designed to be redundant and hot-swap capable. In the event of a cooling component failure the system is cooled such that all components will continue to meet their temperature specifications. Following a failure, the failed cooling component can be hot-swapped, while cooling for the system is maintained.

SR870BH2 supports only a fully populated system fan configuration. However, the system will continue to meet thermal specifications with either a system fan or a power supply failure (Power supply redundancy feature applies to systems with three power modules installed).

Hot-swap system fans drop into the fan bay and interface with connectors on the fan baseboard. Each system fan contains a status LED. A system fan failure is indicated by the corresponding fan LED and also by the Cooling Fault LED on the front panel. All system fans have tachometer output and external Pulse Width Modulation (PWM) speed control.

To maintain adequate cooling for system components, system fans must be hot-swapped within a two minute period (this period only applies to the time that the fan or power supply is physically removed, not from the time of failure).

2.7.1 System Acoustic Description

The SR870BH2 system is designed to meet the acoustic requirements that are defined in the *Intel Environmental Standards Handbook.* Passing criteria for this specification will be met at predefined ambient room temperatures and not under failure conditions.

To enable the system to meet the acoustic specifications, all fans will run at a lower speed when the ambient room temperature is below a pre-determined value, assuming failures have not been detected (resulting in fan boost). This value is referred to as the acoustic threshold. Tests are performed on fully configured systems to meet the acoustic specifications.

The acoustic specifications for the system was designed pass sound pressure of 55 dBA at room temperatures of 23 °C and not under failure conditions. To enable the system to meet these specifications requires that fans run at a slower speed when the room ambient is below 23 °C and there are no failures. To account for a 2 °C hysteresis, a room ambient temperature of 25 °C will be referred to as the acoustic threshold ($T_{acoustic}$) in this document.

2.7.2 System Thermal Control

To enable the system to meet all thermal and acoustic requirements, system actions must be taken in the event of cooling failures and high ambient temperature. The thermal control system performs these functions using both hardware and firmware.

To ensure that all system components meet their specifications, higher fan speeds (fan boost) must be applied when the following conditions occur:

- Room ambient exceeds the preset acoustic threshold
- A system fan or power supply failbure occurs.

Thermal sensors are placed on the Main board, I/O board, SCSI board and Peripheral board. The sensors are either on the chip set or on board locations. The sensed temperatures are used for fan speed control and to provide the user with indicators of system thermal performance.

2.7.2.1 Fan Boost Due to High Ambient Temperature

In the case of room ambient excursion above the acoustic threshold, all system fans increase to a higher speed. Fan speed will return to low speed only after the room ambient temperature falls below the acoustic threshold minus a hysteresis value.

A sensor on the Peripheral board measures unheated air coming from the surrounding room. This sensor determines whether an ambient excursion above the acoustic threshold has occurred and controls the fan speed (All sensors can theoretically control fan speed, however this specific sensor controls the fan speed due to its narrow threshold range).

2.7.2.2 Fan Boost Due to Fan or Power Supply Failure

The system can continue to operate and meet all thermal requirements if a single failure occurs.

A failure is detected when the RPM of a fan falls below a predetermined minimum threshold (Approx. 5000 RPM). If a system fan falls below this threshold, all fans will be boosted to operate at a higher speed (Approx. 8500 RPM)

If a power supply fails for any reason (including loss of AC power) the the system fans will also operate at a higher speed. The exception is if the Redundant (ACR) power supply fails, the system fans will not be effected.

After detection of the fan or power supply failure, all fan speeds are changed to boost levels. Following a failure, all fans remain at high speed until the failed fan or power supply is replaced. Replacement of the failed fan is detected by a change in state of the fan presence signal. Following the replacement of the failing unit (detected by fan presence signal), fan failure monitoring at the lower speed levels is reactivated. Replacement of a power supply is detected by server management.

2.7.3 System Fan Status LEDs

Each system fan contains an integrated status LED as shown in Figure 14. The color of this LED is amber and it turns on if a system fan failure occurs. Slide the rear section of the top cover backward to view these LEDs.

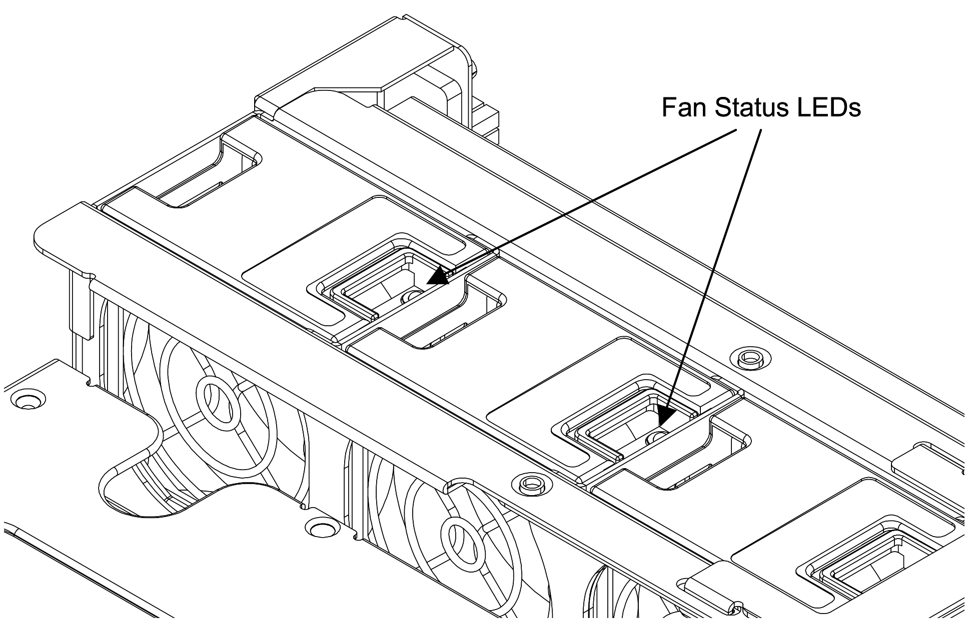

Figure 14. System Fan Status LED

2.8 Server Management

The SR870BH2 server management subsystem is based on the IPMI specifications and conforms to the *IPMI v1.5 Specification*. The server management features are implemented using two microcontrollers: the Sahalee Baseboard Management Controller (BMC) on the main board, and the SCSI hot-swap controller on the SCSI backplane board. The functions of each component are summarized in the following sections.

The firmware of each microcontroller is field-upgradeable using the *Server Management Firmware Update Utility*. Refer to the *SR870BH2 Server Management External Architecture Specification* for more details.

2.8.1 Baseboard Management Controller (BMC)

The BMC is comprised of a Sahalee microcontroller and associated circuitry located on the main board. The primary purpose of the BMC is to autonomously monitor for system platform management events, and log their occurrence in the non-volatile System Event Log (SEL). This includes events such as over-temperature and over-voltage conditions, fan failures, etc. The BMC also provides the interface to the monitored information so system management software can poll and retrieve the present status of the platform.

The BMC also provides the interface to the non-volatile 'Sensor Data Record (SDR) Repository'. Sensor Data Records provide a set of information that system management software can use to automatically configure itself for the number and type of IPMI sensors (e.g., temperature sensors, voltage sensors, etc.) in the system.

The following is a list of the major functions for the BMC:

- System Power Control
  - ACPI Power Control
  - ACPI Sleep Support (S0 and S5 states only)
  - Minimum Power Off Time
- System Reset Control
- System Initialization
  - Processor Temperature and Voltage Threshold Setting
  - Fault Resilient Booting (FRB)
- Front Panel User Interface
  - Power LED control
  - System Status (Green) LED control
  - System Status (Amber) LED control
  - System ID LED control
  - Reset Button control
  - Power Button control
  - SDINT Button control
  - System ID Button control

  - CMOS Clearing
- System Fan Management
- System Management Watchdog Timer
- System Event Log (SEL) interface
- Sensor Data Record (SDR) Repository interface
- SDR/SEL Timestamp Clock
- FRU Inventory Device
- Diagnostics and Beep Code generation
- Event Message Generation and Reception
- Platform Event Paging and Filtering (PEP & PEF)
- Dial Page Alerting
- Alert over LAN
- Alert over Serial/PPP
- Serial over LAN (SOL)
- Terminal Mode (TM)
- Command Line Interface (CLI)
- Processor Core Ratio programming
- Battery monitoring
- Sensor monitoring
  - Temperature monitoring
  - Voltage monitoring
  - Fan monitoring
  - Processor Presence monitoring
  - Interlock Status monitoring
  - Power Supply monitoring
- Itanium 2 Processor Information ROM (PIROM) and Electrically Erasable Programmable ROM (EEPROM) access
- IPMB Communication interface
- EMP interface
- LAN interface
- ICMB interface

Refer to the *SR870BH2 Baseboard Management Controller External Product Specification* for further details.

2.8.2 Hot Swap Controller (HSC)

The Hot Swap Controller (HSC) resides on the SCSI backplane board. The primary functions of the HSC are as follows:

- Implements the SAF-TE command set
- Controls the SCSI Hard Drive fault LEDs
- Provides a path for management information via the SCSI bus

- Retrieves hard disk drive fault status, SCSI backplane temperature, and fan failure information via IPMB
- Queries the status of the power distribution board by retrieving information from the Sahalee server management controller via IPMB
- Controls hard disk drive power-on and power-down, facilitating hot-swapping

2.9 Reliability, Availability and Serviceability (RAS)

SR870BH2 supports the following reliability, availability, and serviceability (RAS) features:

- **Reliability features**
  - Machine check architecture
  - Error checking code (ECC) in main memory and processor caches
  - ECC, parity, and protocol checking on the FSB
  - ECC on SP data; parity on SP FLITs; link level retries on SP bus
  - ECC on HL-2.0 interface; parity on the HL-1.5 interface
  - Parity checking on PCI buses
  - Voltage and temperature monitoring throughout the system

- **Availability features**
  - Redundant hot-swap power supplies
  - Dual redundant power cords (when populated with 3 power supply modules)
  - Hot-swap SCSI hard drives
  - Redundant hot-swap system fans

- **Serviceability features**
  - Modular design
  - Tool less installation and removal of major modules
  - Color coded parts to identify serviceable components
    - Green – Hot-swap or hot-plug components
    - Blue – Non-hot-swap components
  - System ID switches and LEDs on front panel and at rear of the system
  - LED indicators for System Power, AC Power, System, Hard Drive, and LAN status

Notes: System errors routed to the PCI bus SERR# are elevated to machine check errors.

All boards are connected by a server management bus to satisfy the system RAS requirements.

When the system has been powered down, voltages are still present on the system board powering server management logic. All AC power cords must be disconnected to service non-hot-swap components.

2.10 Expansion Support

Table 7 summarizes the expansion support provided by the SR870BH2 server system.

Table 7. SR870BH2 Server System Expansion Support

Quantity	Item
1	64-bit, 133 MHz PCI-X expansion bus slots
2	64-bit, 100 MHz PCI-X expansion bus slots
2	Ultra 320 SCA-2 hard disk drive bays
8	DDR SDRAM Registered DIMM slots

2.11 Specifications

2.11.1 Environmental Specifications

The SR870BH2 server system will be tested to the environmental specifications as indicated in Table 8.

Table 8. Environmental Specifications Summary

Environment	Specification
Temperature operating	10 °C to 35 °C (50 °F to 95 °F)
Temperature non-operating	-40 °C to 70 °C (-40 °F to 158 °F)
Altitude	-30 to 1,500 m (-100 to 5,000 ft)
Humidity non-operating	95 %, non-condensing at temperatures of 25 °C (77 °F) to 30 °C (86 °F)
Vibration non-operating	2.2 Grms, 10 minutes per axis on each of the three axes
Shock operating	Half-sine 2 G, 11 ms pulse, 100 pulses in each direction, on each of the three axes
Shock non-operating	Trapezoidal, 25 G, two drops on each of six faces ∆V : 175 inches/sec on bottom face drop, 90 inches/sec on other 5 faces
Safety	UL60 950, CSA60 950, AS/NZS 3562, GB4943-1995, EN60 950 & 73/23/EEC, IEC 60 950, EMKO-TSE (74-SEC) 207/94, GOST-R 50377-92
Emissions	Certified to FCC Class A; tested to CISPR 22 Class A, EN 55022 Class A & 89/336/EEC, VCCI Class A, AS/NZS 3548 Class A, ICES-003 Class A, GB9254-1998, MIC Notice 1997-42 Class A, GOST-R 29216-91 Class A, BSMI CNS13438
Immunity	Verified to comply with EN55024, CISPR 24, GB9254-1998, MIC Notice 1997-41, GOST-R 50628-95
Electrostatic discharge	Tested to ESD levels up to 15 kilovolts (kV) air discharge and up to 8 kV contact discharge without physical damage
Acoustic	Sound pressure: < 55 dBA at ambient temperature < 23° C measured at bystander, floor standing position Sound power: < 7.0 BA at ambient temperature < 23° C measured using the Dome Method GOST MsanPiN 001-96

2.11.2 Physical Specifications

Table 9 describes the physical specifications of the SR870BH2 server system.

Table 9. Physical Specifications

Specification	Value
Height	3.4 inches (87 mm)
Width	17.7 inches (449 mm)
Depth	29.4 inches (747 mm)
Front clearance	3 inches (76 mm)
Side clearance	1 inch (25 mm)
Rear clearance	6 inches (152 mm)
Weight[1]	65 lbs (30 kg)

Note: 1. The system weight listed above is an estimate for a fully configured system and will vary depending on number of peripheral devices and add-in cards, as well as the number of processors and DIMMs installed in the system.

3. System Chassis and Sub-Assemblies

This chapter describes the SR870BH2 system chassis and sub-assemblies that reside within the chassis. This chapter is organized into the following sections:

Section 3.1: Main Chassis and Top Covers

Section 3.2: Power Subsystem and Fan Bay

Section 3.3: Processor/Memory Subsystem

Section 3.4: Peripheral Bay and Front Panel

Section 3.5: Bezel

3.1 Base Chassis and Top Covers

3.1.1 Base Chassis

The SR870BH2 system utilizes a standard 19-inch EIA chassis that is 2U high x 29.4-inches deep. The 2U height is defined by standard EIA rack units where 1U = 1.75-inches. ((2U x 1.75"/U) – 0.080" = 3.42"). The 28.8-inch depth, as measured from the front mounting flange to the back of the PCI slots, does not include cables or bezel.

The chassis has been designed to be moduar for serviceability and manufacturability. All major modules in the chassis are easily accessible. Hot-swap component replacement capability is provided for system fans, hard drives, and power supplies.

All system FRU's utilize either captive hardware or tool-less retention mechanisims.

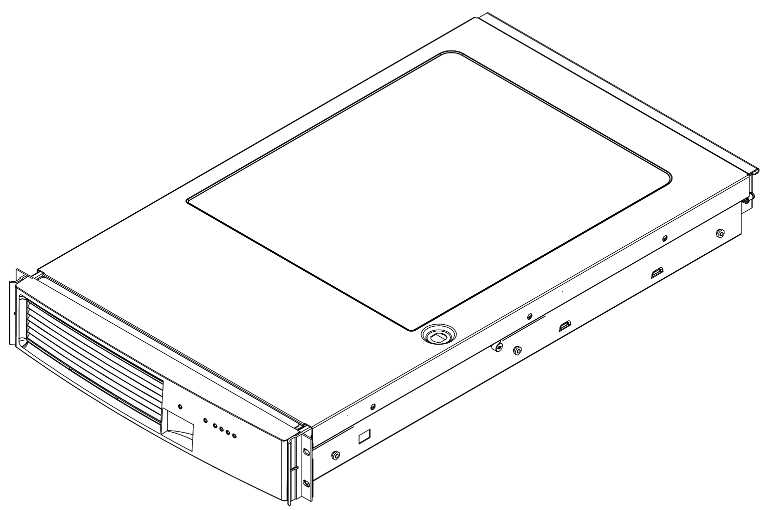

Figure 15. SR870BH2 Server Chassis

3.1.2 Top Cover

The top cover is a one piece design. The top cover is attached to the chassis with a series of L-Shaped interlock tabs. The top cover interlock tabs locate into corresponding reception points in the sides of the chassis. Depress the two blue latches located at the midpoint of the cover and apply a moderate rearword pressure to slide the cover towards the rear of the chassis, lift the cover to remove. Conversley, locate the top cover tabs into corresponding the reception points and the top cover drops down sliding forward to install. There is a lock feature on the top cover that requires a tool (not a key) to open. (refer to figure 1)

3.1.3 Slide Rails

The SR870BH2 server chassis is designed to accommodate slide rails to mount the chassis into standard 19-inch racks. The slide rails attach to T-studs on the sides of the chassis using key-hole features on the slide rails without the use of hardware.

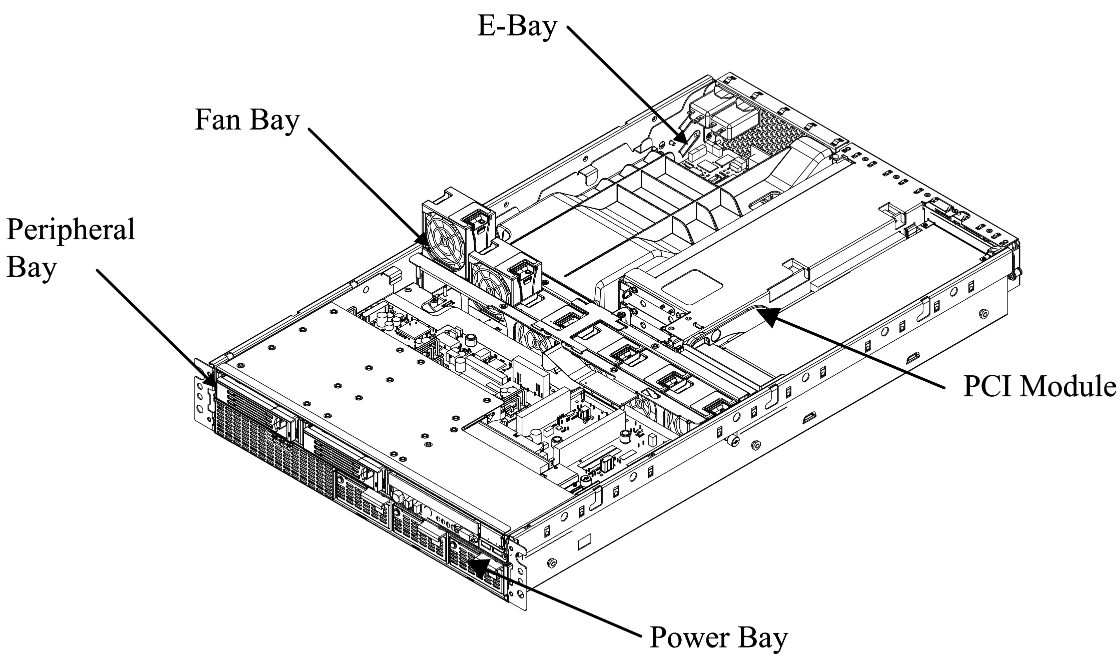

Figure 16. Front Isometric View

3.2 Power Bay and Fan Bay

3.2.1 Power Bay

The power bay provides space for three SSI-compliant TPS multi-output power supplies, AC Switch components, and the Power Distribution Board (PDB).

The Power Distribution Board (PDB) distributes the power to two points, a connector which mates the PDB to the main board and a cable that routes to the peripheral bay. The PDB also includes the connectors for the 6 fans.

The power bay is mounted in the lower front portion of the chassis by dropping straight down over 2 guide pins in the bottom of the chassis. There are 2 captive fastners that hold the power bay in place.

The redundant AC power inputs enter the power bay through a connector that is mounted to a bracket at the rear of the bay. The connector docks to the AC inlet power cable that is part of the electronics bay. The AC power is filtered with a combination 15 Amp power plug/filter.

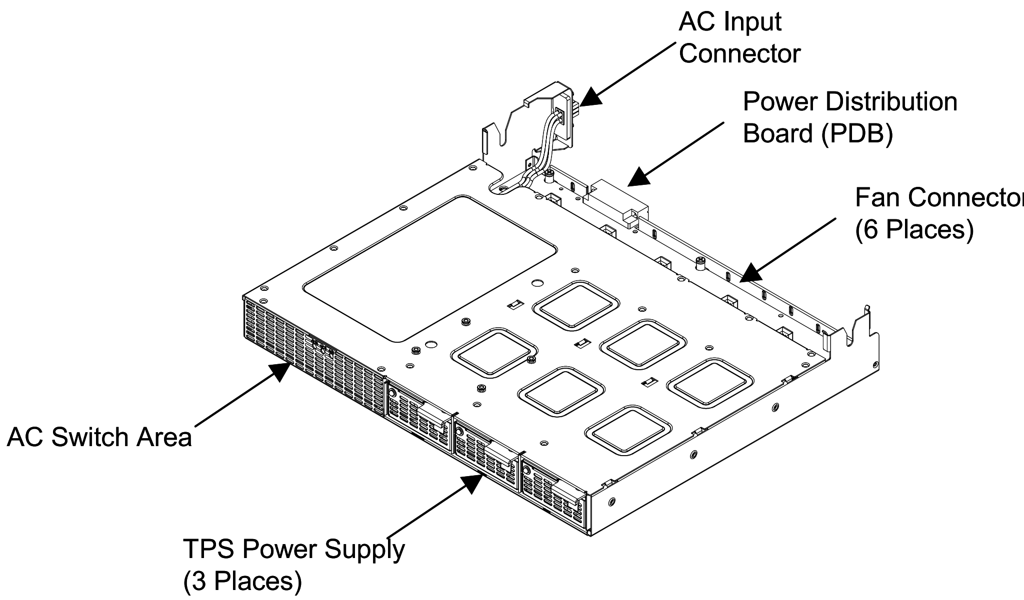

Figure 17. Power Bay

3.2.2 Fan Bay

The Fan Bay Houses the 6-60mm system fans. It mounts in the chassis over the PDB with 3 captive fasteners that also help hold the back of the power bay in place.

3.2.2.1 Fans

The fans are assembled into a molded plastic shell. The molded shell includes a color-coded plastic latch that indicates that the fan is hot-swappable. The assembly has an integrated amber LED wired to the top of the plastic shell that will turn on when the fan is not functioning within specifications. Standard wire finger guards are attached to side of the fan assembly. The fan connector extends from the bottom bracket.

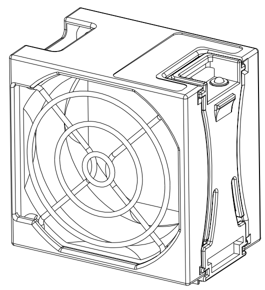

Figure 18. Fan

3.3 Electronics Bay

The Electronics Bay is made up of the main board, the sheet metal tray, the PCI riser subassembly, the air flow duct over the processors, and the AC Inlet Cable

The main board mounts to the sheet metal tray with 2 captive screws. There are also 4 captive screws used to hold the air flow duct inplace, also keeping the main board secured. The AC Inlet, power filters, and cable attach to left side of the tray. The AC Cables have a connector mounted to the front of the tray that docks to AC connector on the back of the power bay when the electronics bay is inserted in the system.

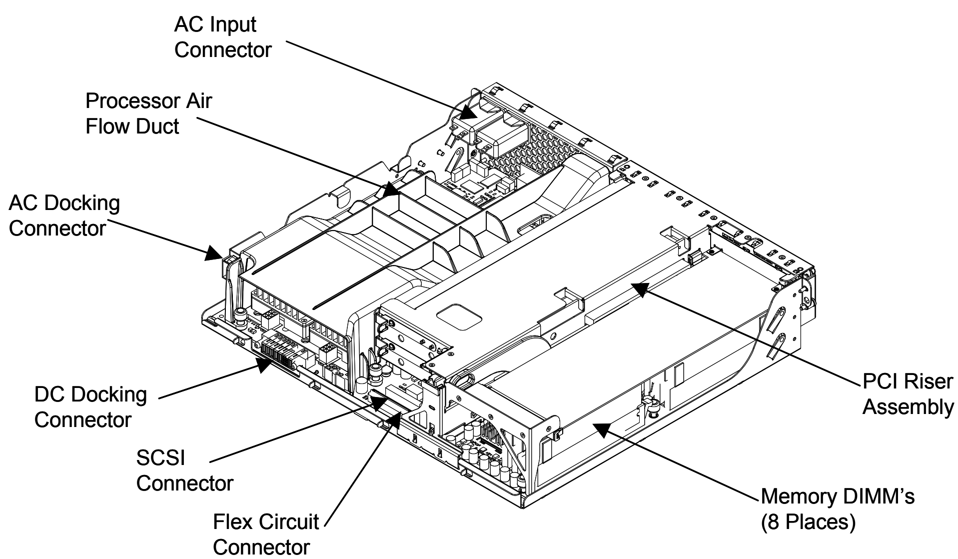

Figure 19. Electronics Bay

3.3.1 PCI Riser

The PCI Riser assembly is made up of 2 sub-assemblies. The first is the PCI Riser insertion/extraction mechanism that mounts to the electronics bay and also holds the main board in place. The second subassembly is the PCI riser that includes the PCI riser board and a sheet metal frame. The board mounts to the frame with captive screws. The frame supplies three (3) PCI slots with guidance and locking features to secure PCI adapters. The frame also has features to guide the riser assembly into the connectors on the main board and attach to the camming insertion/extraction mechanism.

The electronics bay slides into the back of the system and is secured to the chassis using 2 captive screws. The AC inlet connector on the electronics bay docks to the power bay and the DC power connector on the back of the PDB docks to the DC power connector on the front of the main board.

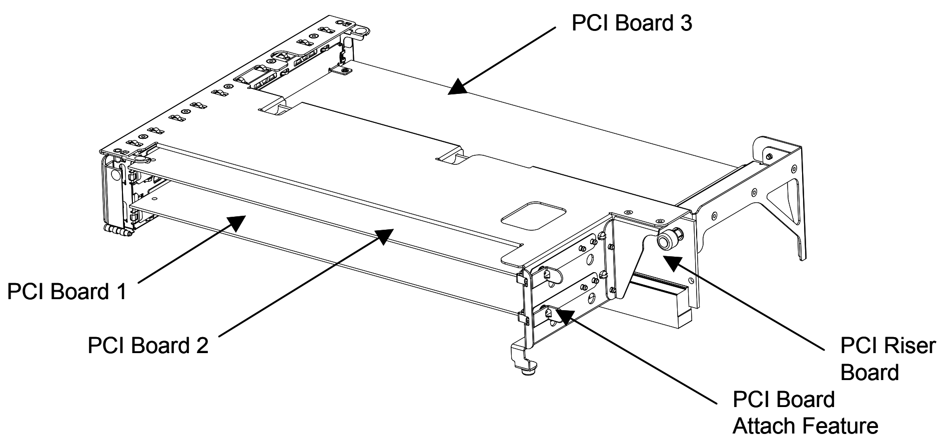

Figure 20. PCI Riser

3.4 Peripheral Bay

The peripheral bay contains two 1-inch SCSI hard drives, one ½-inch DVD/CD drive, the SCSI backplane, and the peripheral board. The SCSI hard drives are hot-swappable. The peripheral bay is secured into the chassis with features in the sides of the chassis and one (1) captive screw.

The peripheral bay is a sheet metal enclosure with structures to mount the hard drives and CD/DVD peripheral. The SCSI backplane board is installed by sliding the key-hole slots on the board onto studs in the peripheral bay. Two captive screws are also used to secure the board to the bay. The peripheral board is attached to the bay by sliding it in on card guides and securing it with 2 captive screws.

There is a power cable and a signal cable that run between the SCSI Backplane and Peripheral board. There is a power cable that routes from the power bay to the SCSI Backplane, A Flex Circuit that runs from the main board to the Peripheral board, and a SCSI cable that runs from the main board to the SCSI backplane.

The Front Panel switches, LED's, and Connectors are defined in Chapter 2.

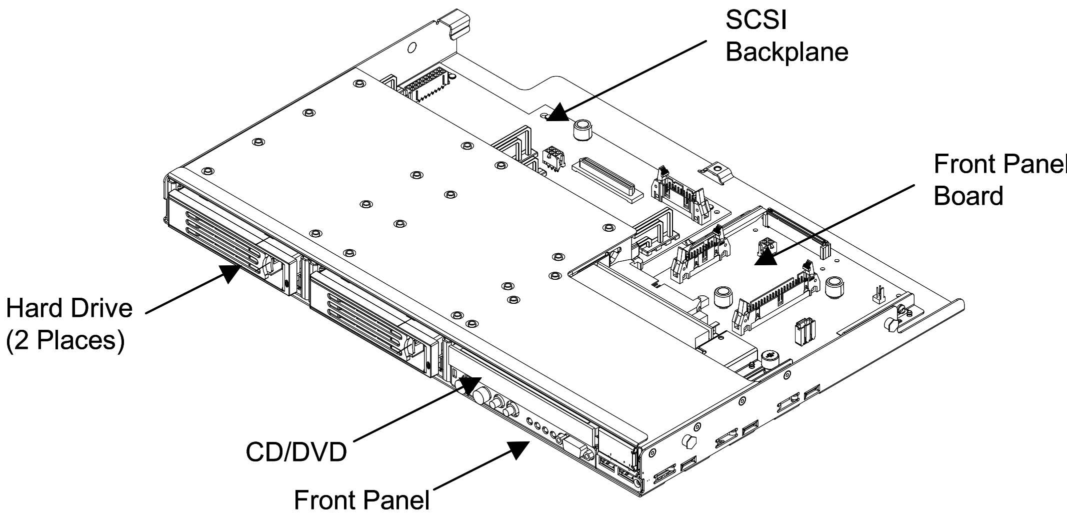

Figure 21. Peripheral Bay

3.4.1 Hard Drive Carrier

The hard drive carrier is a plastic assembly that provides guidance for hot-swapping. It contains an integrated light pipe to transfer the LED indicator light from the SCSI backplane to the front, and an insertion/extraction mechanism that includes a hard drive bezel, which can be customized.

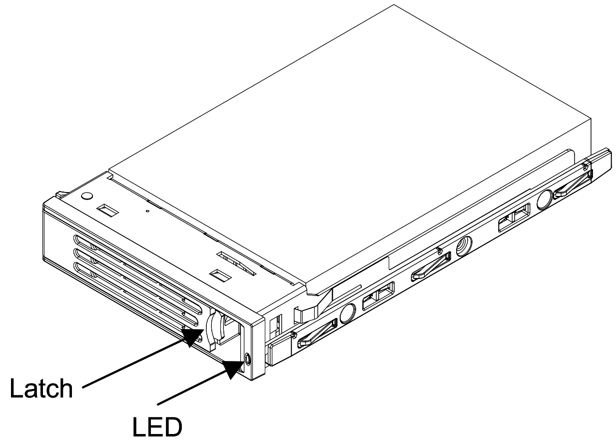

Figure 22. Hard Drive Carrier

3.5 Front Bezel

The front bezel assembly is a one piece design that attaches to features on the front of the chassis and covers the hard drives, peripheral device, and front panel switches/connectors. The front panel LED's are visable through the bezel.

There are 2 black plastic pull handles that cover the EIA mounting flanges and give a feature to pull to extend the chassis from the rack.

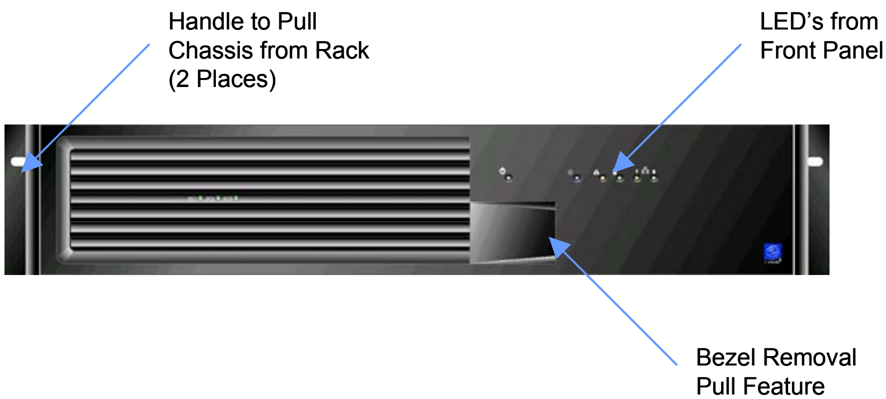

Figure 23. Front Bezel

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4. Cables and Connectors

This chapter describes interconnections between the various components of the SR870BH2 server system. Also, this chapter includes an overview diagram of the SR870BH2 server system interconnections, as well as tables describing the signals and pin-outs for the user accessible connectors. Refer to the *Bar Harbor Board Set External Product Specification* for all other connector signal descriptions and pin-outs. This chapter is organized into the following sections:

Section 4.1: Interconnect Block Diagram
Provides an overview of system interconnects.

Section 4.2: Cable and System Interconnect Descriptions
Provides a list of all the connectors and cables in the system.

Section 4.3: User-Accessible Interconnects
Describes the form-factor and pin-out of user-accessible interconnects.

4.1 Interconnect Block Diagram

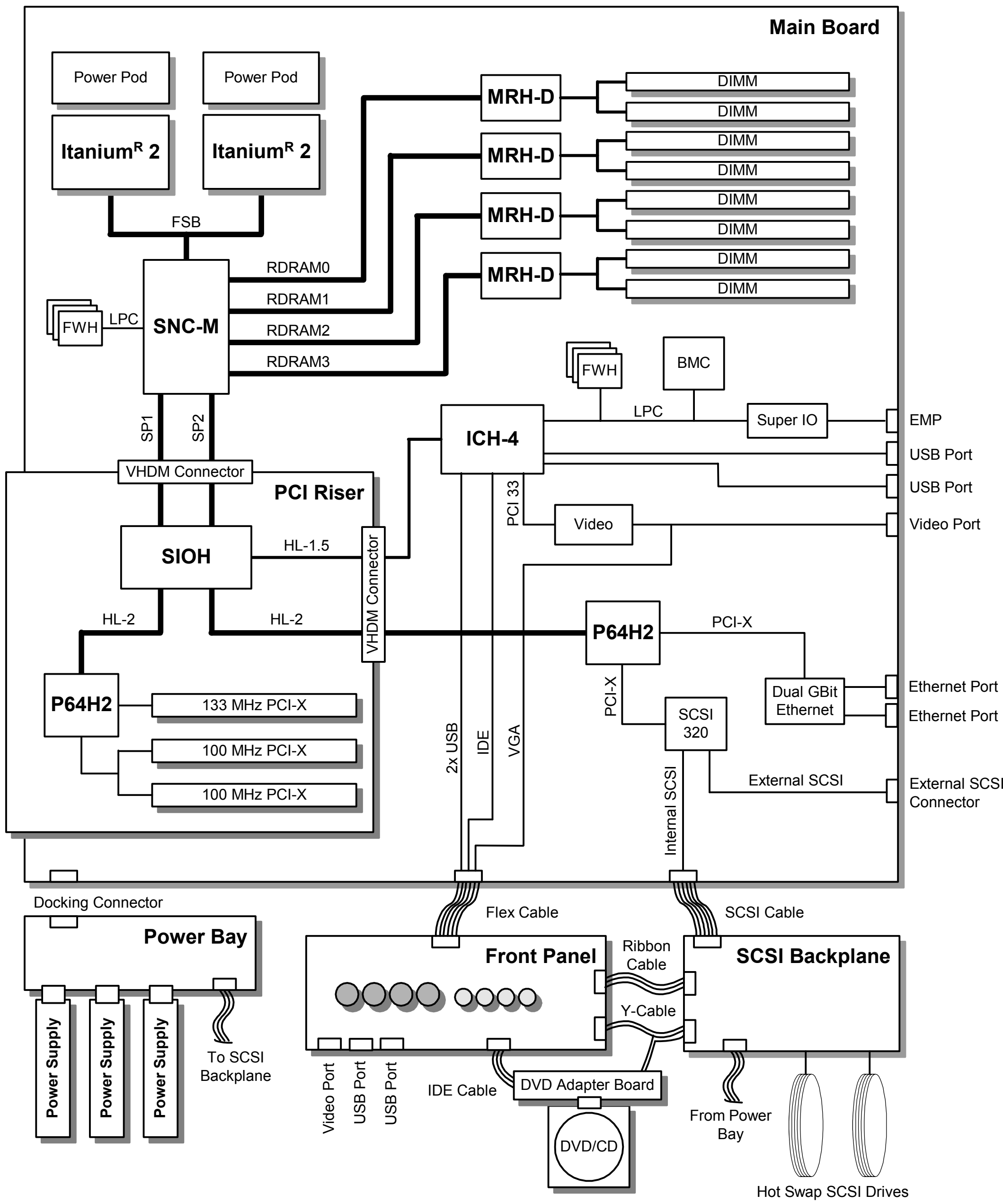

Figure 24. Interconnect Block Diagram

4.2 Cable and Interconnect Descriptions

The following table describes all cables and connectors of the SR870BH2 server system.

Table 10. Cable and Connector Descriptions

Type	Qty	From	To	Interconnect Description
USB	2	Peripheral board	External interface	1x4 pin USB connector
USB	2	Main Board	External interface	1x4 pin USB connector
Ethernet	2	Main Board	External interface	RJ45 connector port
Video	1	Main Board	External interface	15-pin, monitor device
Video	1	Peripheral board	External interface	15-pin, monitor device
I/O Riser Connector	2	Main Board	PCI riser	VHDM connector
External Wide Ultra 320 SCSI, Port 2	1	Main Board	External interface	Right angle board mounted VHDCI connector
Emergency Management Port	1	Main Board	External interface	RJ45 connector port
AC Power	2	Power cord	External interface	IEC filtered 15A recepticle
AC Power	1	IEC filter recepticle	Chassis mounted docking connector	Molex Mini Fit 2 X 3 panel mount connector
AC Power	1	Chassis mounted docking connector	Power bay mounted docking connector	Molex Mini Fit 2 X 3 panel mount connector
DC main power	1	Power supply bay	Main Board	SSI power blade docking connector
DC peripheral power	1	Power supply bay	SCSI backplane	Molex Micro Fit 2 X 10 connector
BIOS/SM firmware update/recovery	4	Main Board	Jumper	Group of 4 jumper blocks, 1 X 3 pin headers
System Fans	6	Power supply bay	Fan module	2x3 Blind Mate micro connectors
ITP	1	Main Board	Internal interface	2x13 header
ISP	1	Main board	Internal interface	2x4 header
Aux IPMB	1	Main Board	Internal interface	1x3 header
IDE/Front Panel Flex cable	1	Main Board	Peripheral board	120 pin .7mm pitch surface mount header
SCSI	1	Main Board	Peripheral board	68 pin wide SCSI Ultra-320 cable
Processor Signals	4	Processor	Main Board	700-pin Intel® Itanium 2 Zero Insertion Force (ZIF) socket
Power Pod Power	1	Main board	Power Pod	Y-Cable, Molex Mini Fit 2 X 6 to two 2 x 3
Memory	8	Memory board	DDR memory	184-pin card edge connector
SCA-2 Hard Disk Drive (HDD) connectors	2	SCSI backplane	1-inch SCSI HDD	80-pin SCA-2 connector

Type	Qty	From	To	Interconnect Description
Front panel Signal	1	Front Panel	SCSI Backplane	20 pin ribbon cable
DVD/CDROM signal	1	Front Panel	DVD adaptor board	40 pin ribbon cable
Peripheral power	1	SCSI backplane	Front Panel and DVD adaptor boards	Y cable, Molex micro fit connectors
½-inch DVD device	1	½-inch DVD adapter	½-inch DVD (or RW-CD) device	2x25 pin JAE* connector

4.3 User-Accessible Interconnects

4.3.1 Serial Port

The Main board provides a rear panel RJ45 serial port.

The COM serial port can be used either as an EMP or as a normal serial port. As an EMP, COM is used as a communication path by the server management RS-232 connection to the Sahalee. This provides a level of emergency management through an external modem. The RS-232 connection can be monitored by the Sahalee when the system is in a powered down (standby) state. Additional information can be found in the *Emergency Management Port Interface External Product Summary*.

Table 11. COM Serial Connector Pin-out

Signal Name	J3A2 Pin
COM2_RTS_L	1
COM2_DTR_L	2
COM2_TXD	3
GND	4
COM2_RI_L	5
COM2_RXD	6
COM2_DSR_DCD_L	7
COM2_CTS_L	8
GND	9
GND	10

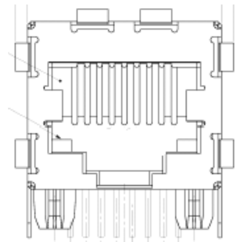

Figure 25. COM Serial Connector

4.3.2 Video Port

The Main and Peripheral boards provide a video port interface with a standard VGA-compatible, 15-pin connector. Only one port is enabled at a time through auto detection of a connected monitor. Onboard video is supplied by an ATI* Rage* XL video controller with 8 MB of onboard video SDRAM.

Table 12. Video Connector Pin-out

Pin	Signal
1	VID_R (analog color signal red)
2	VID_G (analog color signal green)
3	VID_B (analog color signal blue)
4	No connection
5	GND
6	GND
7	GND
8	GND
9	No connection
10	GND
11	No connection
12	MONID1 (to support DDCx, " Display Data Channel* Standard)
13	VID_HSYNC (horizontal sync)
14	VID_VSYNC (vertical sync)
15	MONID2 (to support DDCx, "Display Data Channel* Standard)

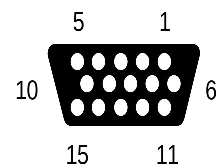

Figure 26. Video Connector

4.3.3 Universal Serial Bus (USB) Interface

The Main Board provides a double-stacked USB port and the Peripheral board provides two single USB port connectors. These built-in USB ports permit the direct connection of four USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports.

Table 13. Dual USB Connector Pin-out

Pin	Signal
A1	Fused Voltage Controlled Current (VCC) (+5 V /w overcurrent monitor of both port 1 and 2)
A2	USBPxM (differential data line)
A3	USBPxP (differential data line)
A4	GND (ground)
B1	Fused VCC (+5 V /w overcurrent monitor of both port 1 and 2)
B2	USBPxM (differential data line)
B3	USBPxP (differential data line)
B4	GND (ground)

Note: ‘x’ indicates port in question.

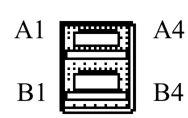

Figure 27. Dual USB Connector

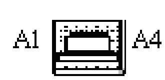

Figure 28. Single USB Connector

4.3.4 Ethernet Connector

The Main Board provides a dual-RJ45 connector (JA4A1) for Ethernet connection. Below are definitions of the speed/status LEDs.

1. Speed LED: Yellow On, 1000-Mbps Ethernet
2. Speed LED: Green On, 100-Mbps Ethernet
3. Speed LED: Off, 10-Mbps Ethernet
4. Status LED: Green On, Ethernet link detected
5. Status LED: Off, Ethernet link not found
6. Status LED: Green Flashing, Ethernet data activity

Table 14. Ethernet Connector Pin-out

Signal	Description	JA4A1 Pin
LED Signals:		
NIC1_LED_CA_L	Lower (Port 1) green status LED cathode signal indicating Port 1	27
NIC1_LED_AN_L	Lower (Port 1) green status LED anode to 100-ohm pullup to 3.3V	28
LINK100A_L	Lower (Port 1) green speed LED cathode, yellow LED anode	29
LINK1000A_L	Lower (Port 1) yellow speed LED cathode, green LED anode	30
NIC2_LED_CA_L	Upper (Port 2) green status LED cathode signal indicating Port 2	31
NIC2_LED_AN_L	Upper (Port 2) green status LED anode to 100-ohm pullup to 3.3V	32
LINK100B_L	Upper (Port 2) green speed LED cathode, yellow LED anode	33
LINK1000B_L	Upper (Port 2) yellow speed LED cathode, green LED anode	34
Ethernet Signals:		
PORT1_MDI0P	Port 1 transceiver 0 positive of differential pair	15
PORT1_MDI0M	Port 1 transceiver 0 negative of differential pair	21
PORT1_MDI1P	Port 1 transceiver 1 positive of differential pair	23
PORT1_MDI1M	Port 1 transceiver 1 negative of differential pair	16
PORT1_MDI2P	Port 1 transceiver 2 positive of differential pair	18
PORT1_MDI2M	Port 1 transceiver 2 negative of differential pair	24
PORT1_MDI3P	Port 1 transceiver 3 positive of differential pair	26
PORT1_MDI3M	Port 1 transceiver 3 negative of differential pair	19
PORT2_MDI0P	Port 2 transceiver 0 positive of differential pair	6
PORT2_MDI0M	Port 2 transceiver 0 negative of differential pair	13
PORT2_MDI1P	Port 2 transceiver 1 positive of differential pair	11
PORT2_MDI1M	Port 2 transceiver 1 negative of differential pair	5
PORT2_MDI2P	Port 2 transceiver 2 positive of differential pair	3
PORT2_MDI2M	Port 2 transceiver 2 negative of differential pair	10
PORT2_MDI3P	Port 2 transceiver 3 positive of differential pair	8
PORT2_MDI3M	Port 2 transceiver 3 negative of differential pair	2
Power Signals:		
+2.5V Standby		4, 7, 9, 12, 14, 17, 22, 25
Chassis Ground	Ground	1, 20, 35, 36, 37, 38

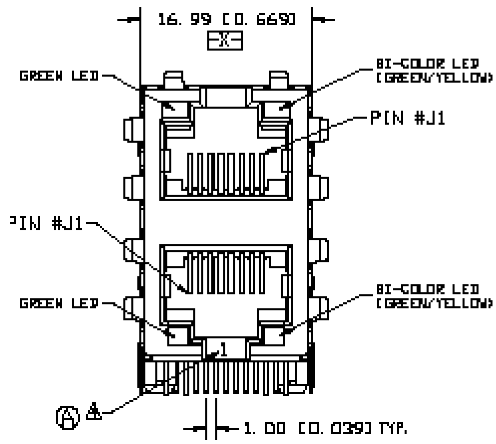

Figure 29. Ethernet Connector

4.3.5 Ultra 320 SCA-2 HDD Connector

The SCSI backplane board provides two SCA-2 (80 pin) connectors for hot-swapping Ultra 320 hard drives. These SCSI ports are controlled by SCSI port 1 of the LSI53C1030 LVDS controller component located on the Main Board. The connector pin assignment is for the current draft *Small Form Factor-8046,* Revision. 1.1 document.

Table 15. SCA-2 Connector Pin-out

80-pin Connector Contact and Signal Name		80-pin Connector Contact and Signal Name	
1	12-V Charge	12-V Ground	41
2	12-V Charge	12-V Ground	42
3	12-V Charge	12-V Ground	43
4	12-V Charge	Mated 1	44
5	Reserved/ESI-1	-EFW	45
6	Reserved/ESI-2	DIFFSNS	46
7	-DB(11)	+DB(11)	47
8	-DB(10)	+DB(10)	48
9	-DB(9)	+DB(9)	49
10	-DB(8)	+DB(8)	50
11	-I/O	+I/O	51
12	-REQ	+REQ	52
13	-C/D	+C/D	53
14	-SEL	+SEL	54
15	-MSG	+MSG	55

80-pin Connector Contact and Signal Name		80-pin Connector Contact and Signal Name	
16	-RST	+RST	56
17	-ACK	+ACK	57
18	-BSY	+BSY	58
19	-ATN	+ATN	59
20	-P_CRCA	+P_CRCA	60
21	-DB(7)	+DB(7)	61
22	-DB(6)	+DB(6)	62
23	-DB(5)	+DB(5)	63
24	-DB(4)	+DB(4)	64
25	-DB(3)	+DB(3)	65
26	-DB(2)	+DB(2)	66
27	-DB(1)	+DB(1)	67
28	-DB(0)	+DB(0)	68
29	-DB(P1)	+DB(P1)	69
30	-DB(15)	+DB(15)	70
31	-DB(14)	+DB(14)	71
32	-DB(13)	+DB(13)	72
33	-DB(12)	+DB(12)	73
34	5-V Charge	Mated 2	74
35	5-V Charge	5-V Ground	75
36	5-V Charge	5-V Ground	76
37	Spindle Sync	Active LED Out	77
38	MTRON	DLYD_START	78
39	SCSI ID (0)	SCSI ID (1)	79
40	SCSI ID (2)	SCSI ID (3)	80

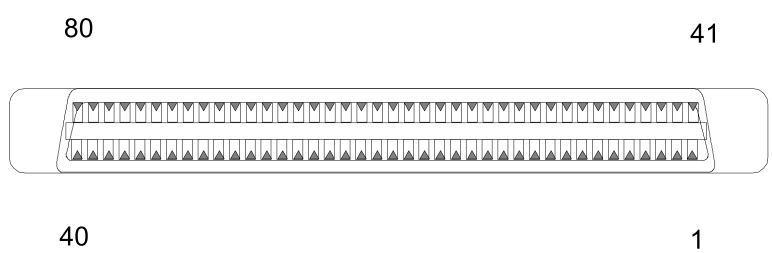

Figure 30. SCA-2 Connector

4.3.6 External Ultra* 320 SCSI Connector

As an option, the server system can support a shielded external (68 pin) SCSI connection. This SCSI port is controlled by SCSI port 2 of the LSI53C1030 LVDS controller component located on the Main Board.

Table 16. Ultra 320 SCSI Connector Pin-out

Signal Name	Pin	Pin	Signal Name
+DB(12)	1	35	-DB(12)
+DB(13)	2	36	-DB(13)
+DB(14)	3	37	-DB(14)
+DB(15)	4	38	-DB(15)
+DB(P1)	5	39	-DB(P1)
+DB(0)	6	40	-DB(0)
+DB(1)	7	41	-DB(1)
+DB(2)	8	42	-DB(2)
+DB(3)	9	43	-DB(3)
+DB(4)	10	44	-DB(4)
+DB(5)	11	45	-DB(5)
+DB(6)	12	46	-DB(6)
+DB(7)	13	47	-DB(7)
+P_CRCA	14	48	+P_CRCA
GND	15	49	GND
DIFFSENS	16	50	GND
TERMPWR	17	51	TERMPWR
TERMPWR	18	52	TERMPWR
NC	19	53	NC
GND	20	54	GND
+ATN	21	55	-ATN
GND	22	56	GND
+BSY	23	57	-BSY
+ACK	24	58	-ACK
+RST	25	59	-RST
+MSG	26	60	-MSG
+SEL	27	61	-SEL
+C/D	28	62	-C/D
+REQ	29	63	-REQ
+I/O	30	64	-I/O
+DB(8)	31	65	-DB(8)
+DB(9)	32	66	-DB(9)
+DB(10)	33	67	-DB(10)
+DB(11)	34	68	-DB(11)

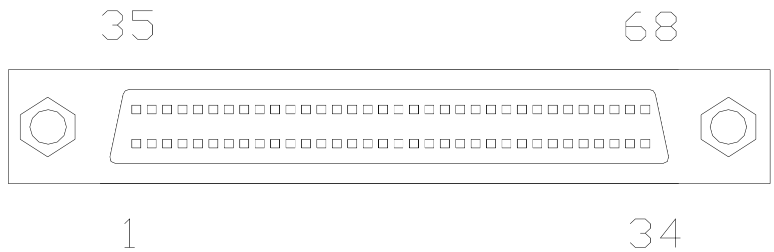

Figure 31. Ultra 320 SCSI Connector

4.3.7 AC Power Input

Two IEC320-C14 15A receptacles are provided at the rear of the server. It is recommended to use an appropriately-sized power cord and AC main. Refer to the power section of this document for system voltage, frequency, and current draw specifications. An external AC cord retention feature is supported by the chassis and is not supplied with the system.

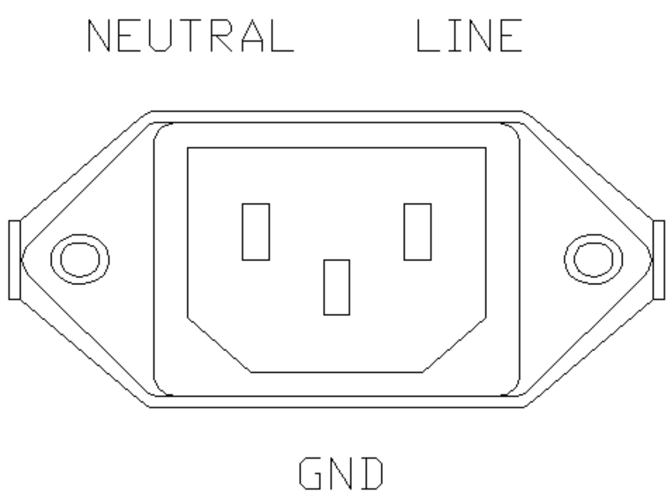

Figure 32. AC Power Input Connector

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5. Power Subsystem

This chapter describes the SR870BH2 Power Bay.

5.1 Mechanical Outline

The mechanical outline and dimensions are shown in Figure 33 through Figure 35. The unit of measurement is in millimeters (mm). The following mechanical sketches should be used for preliminary reference only.

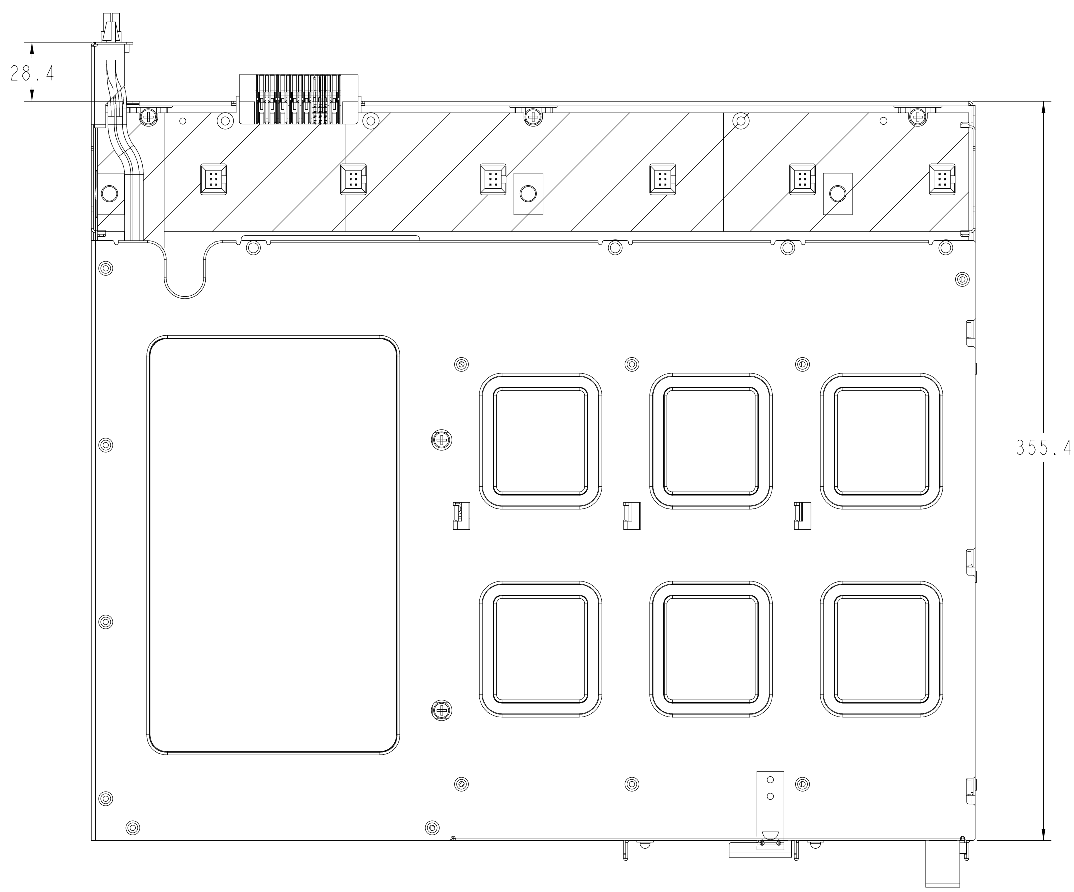

Figure 33. Power Bay Top View

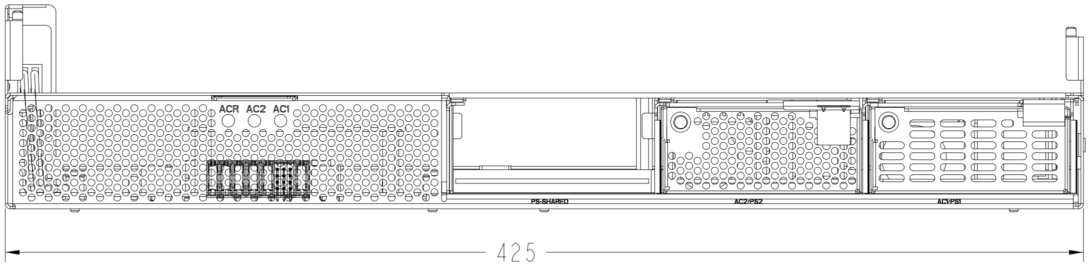

Figure 34. Power Bay Front View

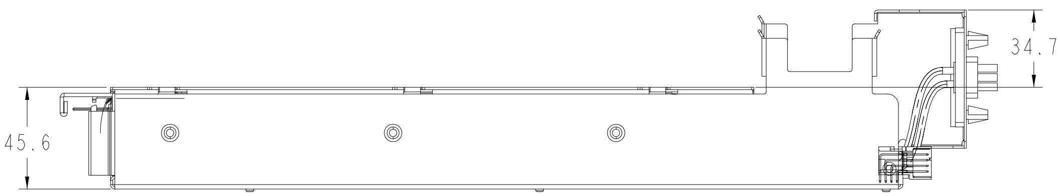

Figure 35. Power Bay Side View

5.2 Power Bay Output Interface

5.2.1 12VB & 12VP Assignment

The main +12 rail has been routed into two rails: 12VB and 12VP on power distribution board. 12VP connects power to the fans and the peripheral connector, and 12VB connects power to the blade connector.

5.2.2 Blade Connector

The power distribution board's output power and control signals interface to the systems power blade board via a PwrBlade* right angle connector FCI 51939-004 or equivalent.

The power supply module's +12V remote sense signal is terminated at the output power blade, P1. A removable jumper (or zero-watt resistor) is required on the power distribution board's +12V remote sense trace, this jumper will provide a connection to the corresponding +12V rail. This jumper should be used for disabling the +12V remote sense function.

Table 17. Blade Pin Assignment

P1	1	2	3	P2	P3	P4	P5	P6	ROW
12*VB	PSON_L_L	Reserved	PWOK_ORED	5V	3.3V	Return	Return	Return	D
	P3_3_SENSE	SENSE_RTN	I2C_IO_SDA						C
	P5_SENSE	Reserved	+5VSTDBY						B
	-12V	I2C_IO_SCL	5VSTDBY						A

5.2.3 DC Output Pin Orientation

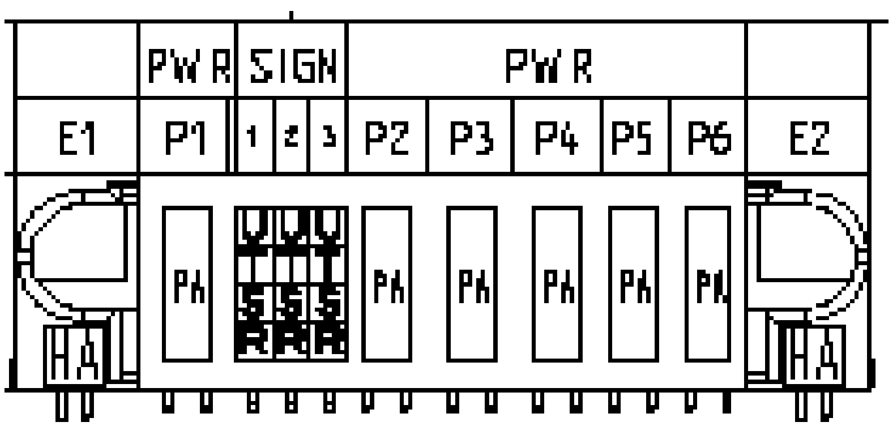

Figure 36. Blade Connector Pin Orientations

5.2.4 Peripheral Interface Cable

The peripheral leads attach from the PCB board to a Molex Micro-fit* connector (43025-2000 or equivalent). Refer to Figure 37 for pin orientation. The connector uses Molex contact female crimp (43030-0001 or equivalent). The maximum cable lengths are 130mm +/-5mm, referring to Figure 37. The wire gauge and definition are in Table 18.

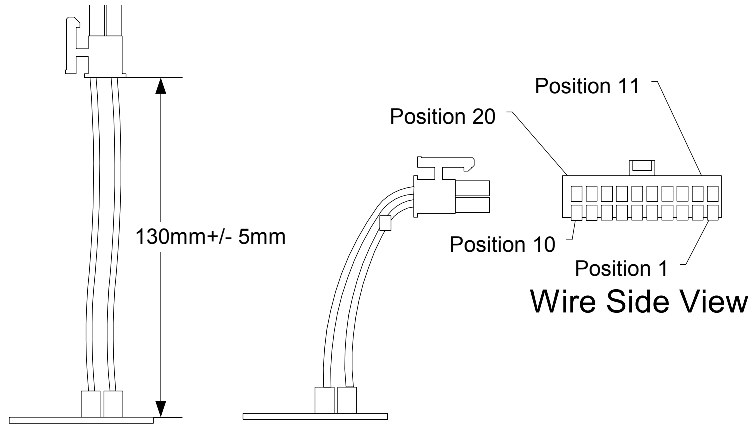

Figure 37. Peripheral Interface Harness Drawing

Table 18. Interface Harness Pin-out

Pin	Wire Gauge	Signal	Color	Pin	Wire Gauge	Signal	Color
1	20 AWG	+3.3V	Orange	11	20 AWG	NC	
2	20 AWG	5VSB	Purple	12	20 AWG	GND	Black
3	20 AWG	+5V	Red	13	20 AWG	GND	Black
4	20 AWG	+5V	Red	14	20 AWG	GND	Black
5	20 AWG	+5V	Red	15	20 AWG	NC	
6	20 AWG	+5V	Red	16	20 AWG	GND	Black
7	20 AWG	+12V	Yellow	17	20 AWG	GND	Black
8	20 AWG	+12V	Yellow	18	20 AWG	GND	Black
9	20 AWG	+12V	Yellow	19	20 AWG	GND	Black
10	20 AWG	+12V	Yellow	20	20 AWG	GND	Black

5.2.5 Fan Input Connectors

Six Foxconn* (HL440330 or the equivalent) fan connectors are used on power distribution board. The number assignment for each connector is sequential, J1 to J6, from right to left.

5.2.5.1 Fan Input Connector Pin Assignment

Table 19. Fan Connector and Pin-out

Signal	Pin	Pin	Signal
LED Anode (White)	1	4	12V Return to fan (Black)
+12V (Yellow)	2	5	LED Cathode (Orange)
LED Cathode (Green)	3	6	Tach

Note: The LED circuit is not to be electrically connected to the fan leads. Pins 3 and 5 (Cathode) are common connections either at the connector or at the LED.

5.2.6 Power Supply Module Output Connector

5.2.6.1 Power Supply Module Mechanical Keying

The top portion (lable side) of the power supply module’s case is be keyed with two channels running from the front to the rear. This key is designed to guarantee that the power supply module will be correctly oriented upon insertion into the system or enclosure. The printed circuit board edge conector is also keyed to ensure proper airflow is applied to the power supply.

Table 20. Edge connector keying position

Keying Position	Between	Airflow direction through power supply
1 and 2	Pin 11-12 &17-18	Exterior face to the interior face or interior face to the exterior face

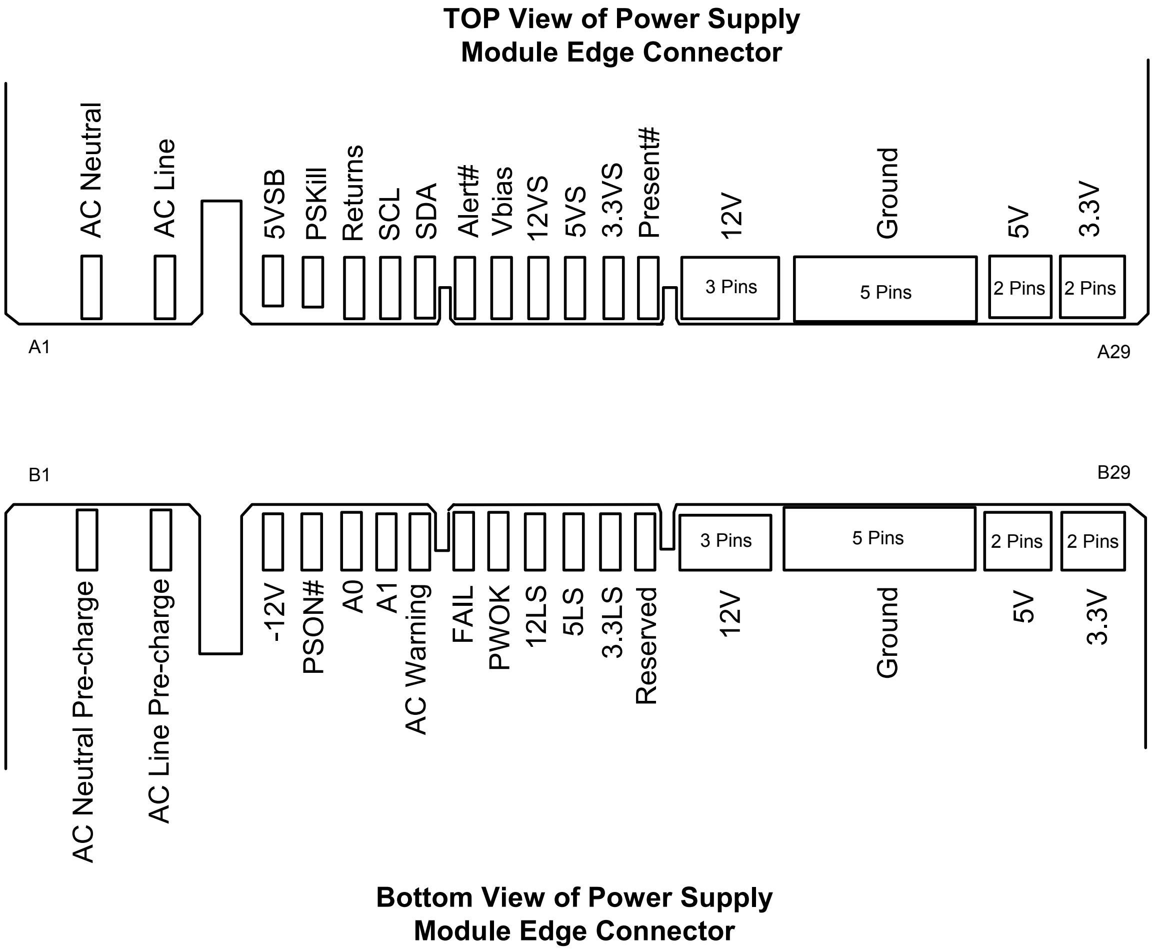

Figure 38. Edge Connector Pin Assignment

Table 21. Module Connector Pin-out

Description	Pin#		Pin#	Description
NC	B1		A1	NC
AC Neutral Pre-charge	B2		A2	AC Neutral
NC	B3		A3	NC
AC Line Pre-charge	B4		A4	AC Line
NC	B5		A5	NC
NC	B6		A6	NC
-12V	B7		A7	5VSB
PSON#	B8		A8	PSKill
A0	B9		A9	ReturnS
A1	B10		A10	SCL
ACWarning	B11		A11	SDA

Description	Pin#	Pin#	Description
Fail	B12	A12	Alert#
PWOK	B13	A13	Vbias
12LS	B14	A14	12VS
5LS	B15	A15	5VS
3.3LS	B16	A16	3.3VS
Reserved	B17	A17	Present#
12V	B18	A18	12V
12V	B19	A19	12V
12V	B20	A20	12V
Ground	B21	A21	Ground
Ground	B22	A22	Ground
Ground	B23	A23	Ground
Ground	B24	A24	Ground
Ground	B25	A25	Ground
5V	B26	A26	5V
5V	B27	A27	5V
3.3V	B28	A28	3.3V
3.3V	B29	A29	3.3V

5.3 AC Input Requirement

5.3.1 AC Input Voltage Specification

The nominal input voltage range specified in AC volts rms is 100-240 Vac. The power supply incorporates a universal power input with active power factor correction, which reduces line harmonics in accordance with EN61000-3-2 and JEIDA MITI standards. The ratings are marked on the supply labels as referenced in Table 22.

Table 22. AC Input Rating

PARAMETER	MIN	RATED	MAX	Max Input Current
Voltage (110)	90 V_{rms}	100-127 V_{rms}	140 V_{rms}	12.0A_{rms}
Voltage (220)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}	6.0A_{rms}
Frequency	47 Hz		63 Hz	

5.3.2 Efficiency

The power supply has a minimum efficiency of 65% to its DC output pins at maximum load currents and at rated nominal input voltages and frequencies.

5.3.3 AC Line Dropout

AC line dropout condition is a transient condition defined when the line voltage input to the power supply drops to 0 volts. AC line dropout will not damage the power supply under any load conditions. While operating at full load, an AC line dropout condition, with a period equivalent to a complete cycle of AC input power frequency (i.e., 20 milliseconds at 50 Hz) or less, will not cause any out of regulation conditions, such as overshoot or undershoot, nor will it cause any nuisance trips of any of the power supply protection circuits.

5.3.4 Dual AC Inputs

The power bay has two AC inlets located at the rear of the chassis, the inlets are labled AC1 and AC2 Refer *to* Figure 8*. chassis rear view of SR870BH2 Server System*.

AC1 is connected to the inputs of Power supply module PS1. AC2 is connected to module PS2 and the redundant power module PS3 through normally closed transfer switch contacts. The PS number assignment can be seen by referring to Figure 5. Front View of SR870BH2 Server System (Shown with Bezel Removed)

If AC1 input fails (or exceeds the specified voltage range), AC2 will transfer power to the two modules located in the positions labled PS2 and PS3.

If AC2 input fails, the AC transfer switch automatically switches from AC2 to AC1. As result, AC1 connects to the two power supply modules located in locations PS1 and PS3. Once (if) AC2 recovers, the AC transfer switch resets to its original state Refer to Figure 40*. LED block diagram*. .

5.3.5 AC Line Fuse

The inputs to both AC1 and AC2 are internally fused. AC in-rush current will not cause the AC line fuses to blow under any conditions. Protection circuits in the power supply will not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions. The DC load short circuit protection circuits will shut down or limit power supply without causing the AC line fuse to blow.

5.3.6 Power Factor Correction

The power supply incorporates a power factor correction circuit.

The power supply is tested as described in *EN 61000-3-2: Electromagnetic Compatibility (EMC) Part 3: Limits- Section 2: Limits for Harmonic Current Emissions*, and meets the current harmonic emissions limits specified for ITE equipment.

The power supply is tested as described in *JEIDA MITI Guideline for Suppression of High Harmonics in Appliances and General-Use Equipment* and meets the current harmonic emissions limits specified for ITE equipment.

5.4 DC Output

5.4.1 Hot Swap

Hot swapping is the process of inserting and extracting a power supply from an operating power bay. During this process, A system with a redundant power module is designed to operate normally, the output voltages will remain within the limits specified (refer to Table 23).

5.4.2 DC Output

The DC output specification for the power supply is met by two power supply modules operating in the power bay (A third power module may be inserted to enable redundancy). When operated in parallel, the power modules share the total load currents equally within the limits specified, and meet all performance requirements.

In the unlikley event a power module was to fail in a redundantly paralleled group, or upon the removal of an operational or failed supply from a redundantly paralleled group, the action will not cause DC output transients in excess of specified limits. Conversley, adding an operational or failed supply to a paralleled group will not cause DC output transients in excess of the limits specified.

Table 23. DC Output Voltage Regulation Limits

Output	MIN	MAX	Tolerance
+3.3V	3.20 V	3.46 V	+5 / -3 %
+5V	4.80 V	5.25 V	+5 / -4 %
12VB &12VP	11.52 V	12.6 V	+5 / -4 %
+5VSB	4.80 V	5.25 V	+5 / -4%

5.4.3 Output Current Rating

The combined continuous output power for all outputs have been designed such that they will not exceed 650W. Each output has a maximum and minimum current rating shown in Table 1 650W Load Ratings.

Table 24. 650W Load Ratings

# of modules	Current	3.3V	5V	12VB	12VP & FANS	-12V	5VSB	Vbias	Power (W)
2 & 3	Minimum (A)	0	0	0	0	0	0	0	0
2 & 3	Maximum (A)	30.0	30.0	37.5	15	0.5	2.0	50mA	650

5.4.4 Over-Voltage Protection

The power supply's over-voltage protection is locally sensed. The power supply will shut down in a latch-off mode after an over voltage condition on any of the voltage outputs. This latch-off mode on the power supply modules can be cleared by toggling the PSON# signal or by an AC power interruption. The only exception is the latch-off 5VSB & Vbias output, which can be cleared by an AC power interruption only. The following table contains the over voltage limits. The values are measured at the output of the power supply DC connector.

Table 25. Over Voltage Limits

Output Voltage	MIN (V)	MAX (V)
+3.3 V	3.9	4.5
+5 V	5.7	6.5
+12 V	13.3	14.5
-12V	-13.3	-14.5
+5VSB	5.7	6.5
Vbias	21	30

5.4.5 240VA Protection and OCP

The power bay provides three 240VA protections and one OCP (over current protection). If current limit is exceeded on any one of these protections, the power bay shall shutdown the power supply modules. The protection circuits can be reset via the PSON# signal or by cycling the AC power.

Table 26. OCP Channel Limits

Channel	240VA Protection	Connector	Tripping limit	Allowance of Tolerance	Minimum time to trip
3.3V	Yes	Blade & Peripheral	35A	10%	500mS
5V	Yes	Blade & Peripheral	35A	10%	500mS
12VB	No	Blade	48A	10%	500mS
12VP	Yes	Fans & Peripheral	18A	10%	500mS

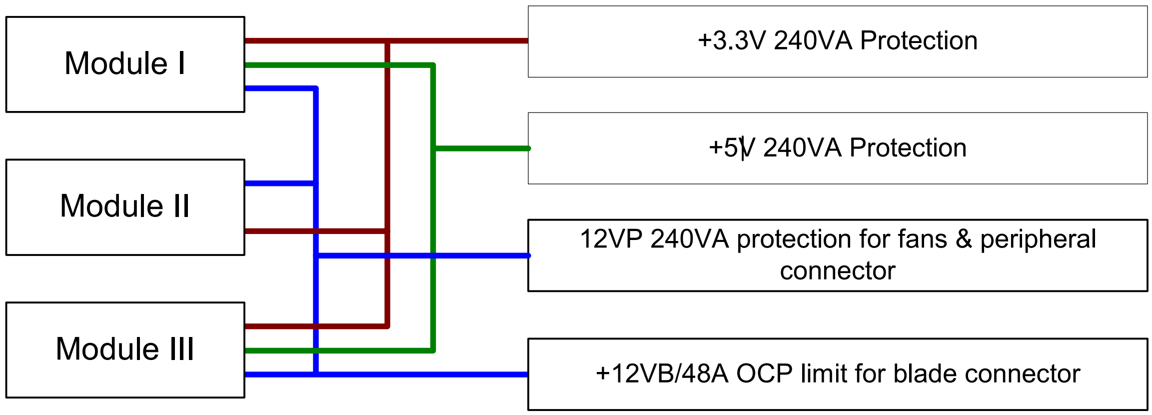

Figure 39. OCP Channel

5.4.6 Short Circuit Protection

A short circuit applied to any of the DC outputs will not damage the power bay or the power supply module. When a hard short circuit is sensed, the power supply will shut down immediately. A hard short circuit is defined when the load level is less than 10 mΩ.

5.4.7 Over Temperature Protection Requirements

The power supply is protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an Over Temperature Protection (OTP) condition the power supply will shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically. The OTP circuit has a built in hysteresis to ensure that the power supply will not oscillate (cylcle on and off) due to a temperature recovery condition.

5.4.8 Power Supply Module LED indicators

There will be a single bi-color LED to indicate power supply status. When AC is applied to the Power Supply Unit (PSU) and standby voltages are available the LED indicator BLINKS GREEN. The LED will change to SOLID GREEN to indicate that all the power outputs are available. The LED will change to SOLID AMBER to indicate that the power supply has incurred a failure condition such as: A shutdown due to over current, A shutdown due to over temperature, or indicates a predictive failure. Refer to Table 27.

Table 27. LED Indicators

Power Supply Condition	Power Supply LED
No AC power - to all PSU	OFF
No AC power - to this PSU only	AMBER
AC present / Only Standby Outputs On	BLINK GREEN
Power supply DC outputs ON and OK	GREEN
Power supply failure (includes over voltage, over temperature)	AMBER
Current limit	AMBER

5.4.9 Power Bay LED indicators

The Power Bay LEDs (AC1, AC2 and ACR) indicates the state of the AC power inputs to the power bay.

- LED AC1 green indicates AC input #1 available; LED AC1 off indicates AC input #1 unavailable or below a threshold of voltage to power up the bay.
- LED AC2 green indicates AC input #2 available; LED AC2 off indicates AC input #2 unavailable or below a threshold of voltage to power up the bay.
- LED ACR green indicates the redundant feature is available; ACR LED off indicates the redundancy feature is not available. Redundancy feature requires all of the following four conditions be present.

  1. AC input #1 available
  2. AC input #2 available
  3. Power good signals asserted from all three power supply modules
  4. TS-OK signal is asserted

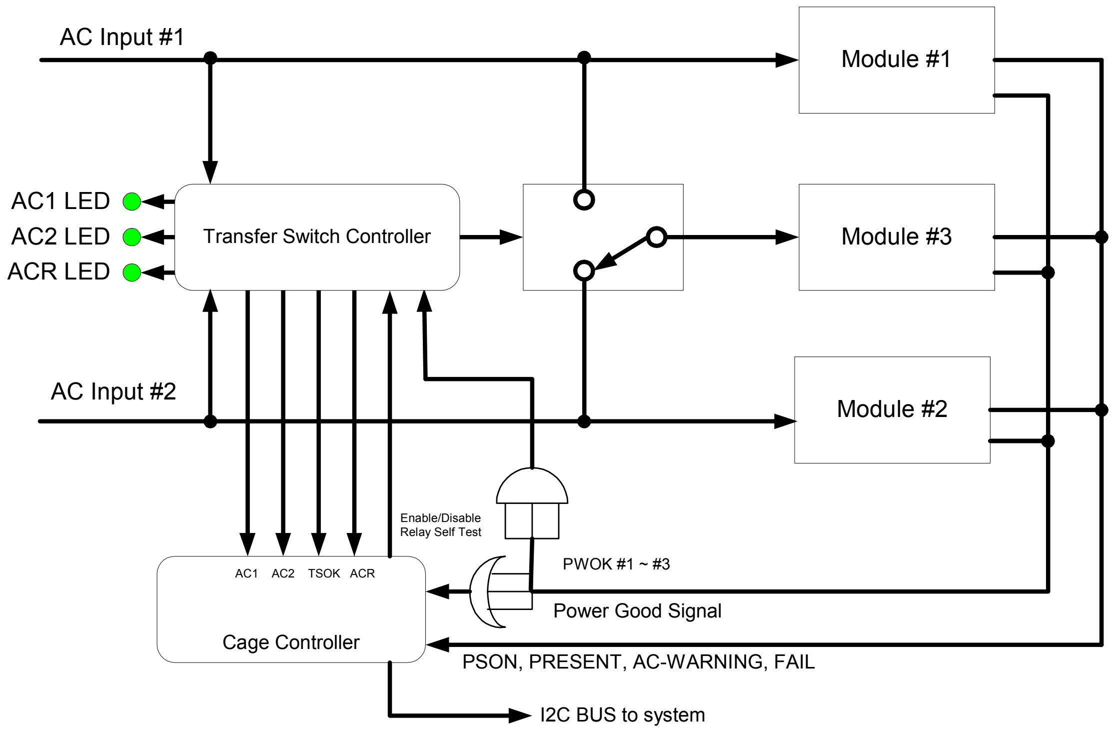

Figure 40. LED Block Diagram

5.5 Regulatory Agency Requirements

The power supply meets or exceeds UL requirements, CSA or cUL certification to Level 3, or any NORDIC CENELEC*-certified (such as SEMKO, NEMKO or SETI) markings demonstrating compliance. The power supply must also meet FCC Class B, VDE 0871 Level B, and CISPR Class B requirements. Refer to section 9 of this document for specifications and regulations.

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6. Peripheral board

This chapter describes the SR870BH2 Front Panel. This chapter is organized into the following sections:

Section 0: **Introduction**
Provides an overview of the SR870BH2 Front Panel showing functional blocks and board layout.

Section 6.2: **Functional Architecture**
Describes the SR870BH2 Front Panel's functional blocks.

Section 6.3: **Signal Descriptions**
Summary of the SR870BH2 Front Panel's internal signals and connector signals, and the connector signal pin names and the signal descriptions. Signal mnemonics appear throughout this chapter.

Section 0: **Electrical, Environmental, and Mechanical Specifications**
Specifies operational parameters and considerations, and connector pin-outs.

6.1 Introduction

The SR870BH2 Front Panel is designed to give the end user support for front panel switches and LEDs and an IDE connector to support a DVD drive. The following block diagram, architectural overview, and placement diagram will give a general idea how the Front Panel works.

6.1.1 Block Diagram

Figure 41 block diagram breaks down the SR870BH2 Front Panel into physical and functional blocks. Arrows represent buses and signals. Blocks represent the physical and functional blocks. Figure 41 illustrates the general architecture of the SR870BH2 Front Panel.

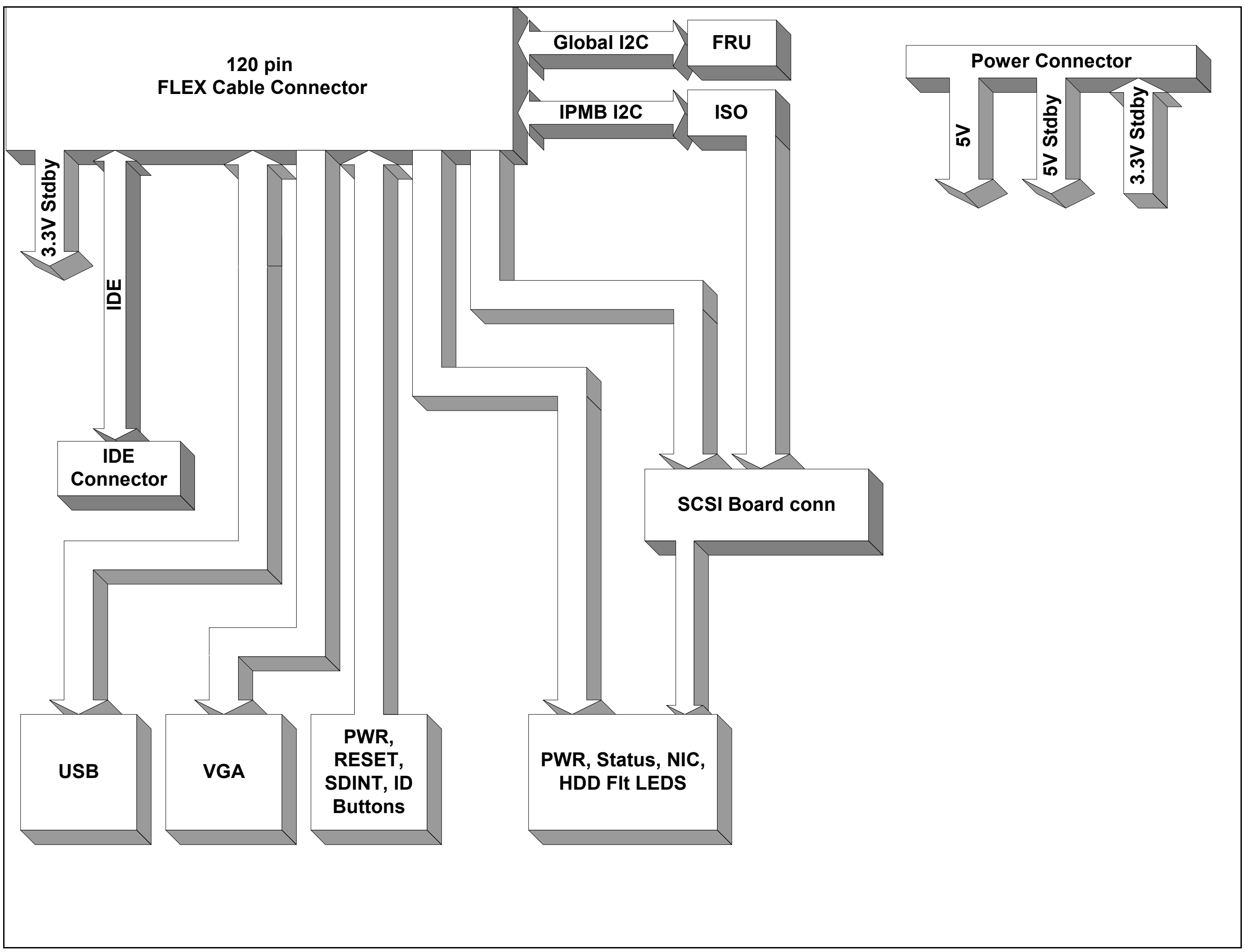

Figure 41. Front Panel Block Diagram

6.1.2 Architectural Overview

The SR870BH2 Front Panel provides three main functions for the system. The first function is to pass the IDE signals between the Main Board and the DVD drive. The second function is to provide the front panel interface for the system. The third function is to provide I^2C server management interface.

Functional blocks:

- IDE bus passes IDE signals between the IDE DVD and the Main Board
  - The 120 pin FLEX Cable Connector from Main Board provides IDE connectivity along with auxiliary signals
  - Single IDE channel pass-thru connection to IDE connector for support of an IDE peripheral

- Front Panel Functions
  - Two USB 1.1 connections
  - Power, Reset, SDINT and ID buttons
  - LEDs for power, both NIC channels, ID, system and drive failure
  - VGA connector providing video from Main board controller

- Server management
  - I^2C isolation to SCSI board
  - Temperature sensor

6.1.3 Component Location

Figure 42 shows the 2D placement of the major components and connectors on the Front Panel. Figure 43 shows the 3D placement.

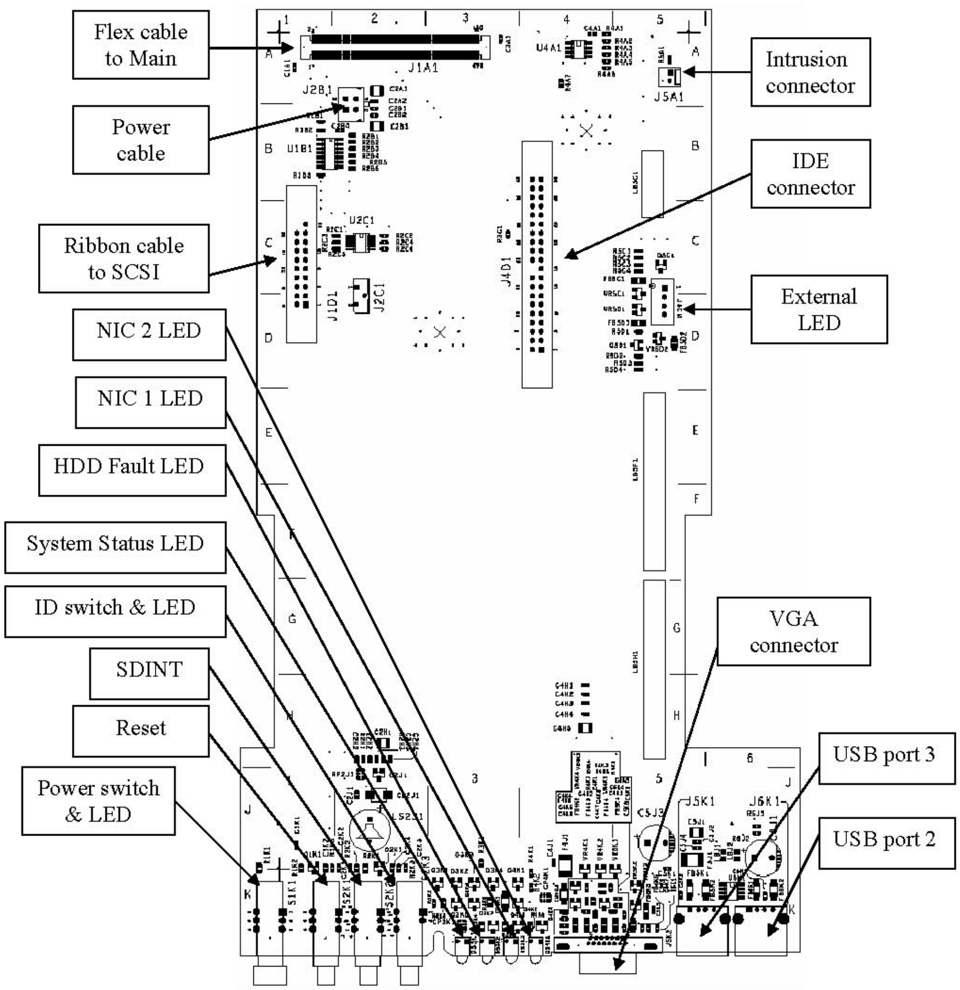

Figure 42. Front Panel 2D Placement Diagram

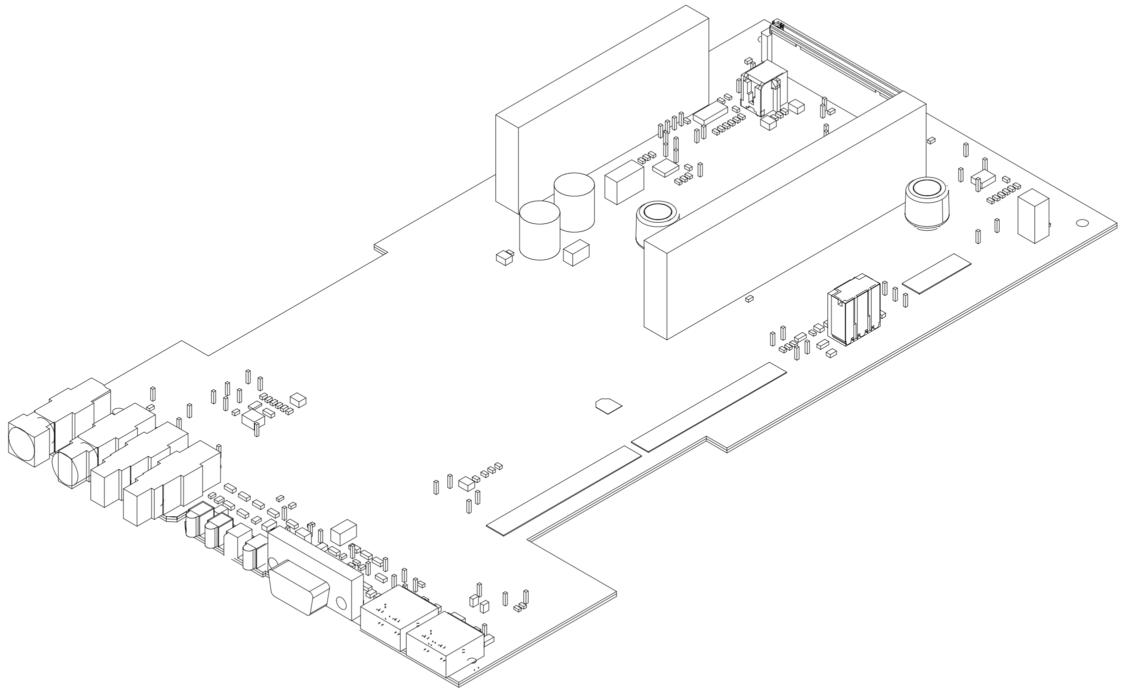

Figure 43. Front Panel 3D Placement Diagram

6.2 Functional Architecture

This section provides a more detailed architectural description of the SR870BH2 Front Panel's functional blocks.

6.2.1 IDE Bus

The SR870BH2 Front Panel passes an IDE bus from the IO board to the IDE connector. The IDE bus is DMA-33 capable. The IDE bus connects from the 120 pin FLEX Cable Connector (Main Board) to the IDE connector.

6.2.2 Server Management Interface

The SR870BH2 Front Panel will support the following Server Management features:

6.2.2.1 I/O I^2C* Bus

The I/O I^2C bus connects Main board to the DS75 (Front panel temperature sensor) for temperature information.

6.2.2.2 Global I^2C Bus (IPMB)

The global I^2C bus connects the SCSI Backplane micro-controller to the system. The micro-controller is isolated from the system until the system PWRGRD signal is asserted.

6.2.2.3 I^2C Addresses

Three I^2C devices and their addresses are listed in Table 28. There is only one I^2C device that can be addressed on the SR870BH2 Front Panel.

- SR870BH2 Front Panel Temperature Sensor

Table 28. I^2C IO Bus Addresses

Device	Address	Bus/Location	Description
DS75	0x90	Legacy I^2C/ SR870BH2 Front Panel	I/O I^2C bus SR870BH2 temperature sensor

6.2.3 Reset

All reset for logic on the SR870BH2 Front Panel is supplied by the RST_PCIRST_L signal from the Main Board.

6.2.4 Connector Interlocks

The SR870BH2 Front Panel has interlock signals on some of its connectors.

6.2.4.1 FLEX Cable Connector (120pin)

An Interlock signal is used by the Main Board to determine if the SR870BH2 Front Panel is properly mated. Flex cable interlock is defined by the INTERLOCK_TO_SCSI_L and INTERLOCK_FROM_SCSI_L signals. These signals are passed on to the SCSI backplane.

6.2.4.2 SCSI Backplane ribbon cable connector

An Interlock signal is used by the Main Board to determine if the SR870BH2 Front Panel is properly mated to the SCSI backplane. SCSI backplane interlock is defined by the INTERLOCK_TO_SCSI_L and INTERLOCK_FROM_SCSI_L signals.

6.2.4.3 VGA connector

An Interlock signal is used by the Main Board to determine if a monitor is connected to the Front Panel video connector. The V_PRES_L signal will be pulled low by most monitor cables. This will cause the Main board to redirect its video output to the Front Panel.

6.3 Signal Descriptionss

The following notations are used to describe the signal type, from the perspective of the SR870BH2 Front Panel:

I	Input pin to the SR870BH2 Front Panel
O	Output pin from the SR870BH2 Front Panel
I/O	Bi-directional (input/output) pin
PWR	Power Supply pin

The signal description also includes the type of buffer used for the particular signal:

TTL	5V TTL signals
CMOS	5V CMOS signals
3.3V CMOS	3.3V CMOS signals
Analog	Typically a voltage reference or specialty power supply
hs	This suffix is added to indicate high speed requirements that would make any modifications subject to detailed review

6.3.1 Molex Power Connector

Table 29 is a summary of power connector pins, including the signal mnemonic, the name, and a brief description.

Table 29. Power Interface Signals – J2B1

Signal	Type	Driver	Name and Description
+3.3VSTDBY	O	PWR	+3.3 Volt supply to SCSI backplane.
+5V	I	PWR	+5 Volt supply from SCSI backplane.
+5VSTBY	I	PWR	+5 Volt supply from SCSI backplane.

6.3.2 FLEX Cable Connector (120pin)

The 120 pin FLEX Cable Connector carries signals between the SR870BH2 Front Panel and Main Board. The signal groups are Primary IDE, USB, Power Good, and I^{2}C. Table 30 provides a description of the 120 pin FLEX Cable Connector.

Table 30. 120 pin FLEX Cable Connector Signal Description – J1A1

Signal		Type	Driver	Name and Description
I^{2}C	I2C_IO_SCL	I/O	CMOS	**Docking IPMB Serial Clock.** This pin I2C bus for the FRU.
	I2C_IO_SDA	I/O	CMOS	**Docking IPMB Serial Data.** This pin I2C bus for the FRU.
	I2C_IPMB_SCL	I/O	CMOS	**Docking IO Serial Clock.** This pin supplies the global IPMB Bus clock for the SR870BH2 Front Panel. The GEM Microcontroller is on this Bus.

Signal		Type	Driver	Name and Description
	I2C_IPMB_SDA	I/O	CMOS	**Docking IO Serial Data.** This pin supplies the global IPMB Bus data for the SR870BH2 Front Panel. The GEM Microcontroller is on this Bus.
MISC	INTERLOCK_TO_SCSI_L	I/O	TTL	**Interlock Loop-back**. Two pins are used to indicate to the main board that the Flex cable has been installed between the Front Panel and the Main Board and that the ribbon cable has been installed betweeen the Front Panel and the SCSI Backplane.
	INTERLOCK_FROM_SCSI_L	I/O	TTL	**Interlock Loop-back**. Two pins are used to indicate to the main board that the Flex cable has been installed between the Front Panel and the Main Board and that the ribbon cable has been installed betweeen the Front Panel and the SCSI Backplane.
	INTRUSION_L	O		**Chassis Intrusion Detection.** This net is used in Telco products for the intrusion detection logic. In the SR870BH2 Front Panel it is pulled to +5VSTDBY.
	BMC_SPKR	I	TTL	**Speaker Signal.** This signal is buffered on the Front Panel and delivered to the speaker on the Front Panel.
	RST_PCI_RST_L	I		**Reset.** This reset is used for all reset and power good purposes on the Front Panel.
Power	+3.3V STDBY	I	PWR	**+3.3V Standby.** +3.3V standby supplied by the Main Board
In System Programmable	ISP_SYS_EN_L	I	CMOS	**ISP Programming Enable.** Driven by an external programming device to enable the ISP part for programming.
	ISP_ SYS_TCK	I	CMOS	**ISP Programming Clock.** Driven by an external programming device to provide the ISP part a clock for programming.
	ISP_ SYS_MODE	I	CMOS	**ISP Programming Mode.** Driven by an external programming device to indicate to the ISP part what programming mode is desired.
	ISP_ SYS_TDI	I	CMOS	**ISP Programming Data In.** Driven by an external programming device to provide the ISP part data for programming.
	ISP_ SYS_TDO	O	CMOS	**ISP Programming Data Out.** Driven by the SR870BH2 Front Panel ISP part to propagate programming data back to an external programming device.
IDE	IDE_DD<15..0>	I/O	hs	**ISA Data**.
	IDE_DREQ	O	hs	**Direct Memory Access (DMA) Request**.
	IDE_DIOW_L	I	hs	**Write Request**. Handshake request for write operations.
	IDE_DIOR_L	I	hs	**Read Request**. Handshake request for read operations.
	IDE_IORDY	O	hs	**Ready**. Device ready for operation (high).
	IDE_DACK_L	I	hs	**Direct Memory Access (DMA) Acknowledge**.
	IDE_IRQ	I	hs	**Interrupt Request**.
	IDE_DA<2..0>	I	hs	**Register Select Address.** (from ISA address bus).
	IDE_CS1_L	I	hs	**Select Command Register Block** (0x1F0-0x1F7)
	IDE_CS3_L	I	hs	**Select Control Register Block**. (0x3f6-0x3f7)
Switche	FP_ID_BTN_L	O		**This signal is from the ID switch**

	Signal	Type	Driver	Name and Description
	FP_RST_BTN_L	O		**This signal is from the RESET switch**
	FP_SDINT_BTN_L	O		**This signal is from the SDINT switch**
	FPPWR_BTN_L	O		**This signal is from the Power switch**
LED Control	GEN_FLT_GRN_LED	I		**This signal is used by the Front Panel to illuminate the green Status LED**
	GEN_FLT_AMB_LED	I		**This signal is used by the Front Panel to illuminate the amber Status LED**
	NIC1_LED	I		**This signal is used by the Front Panel to illuminate the green NIC 1 LED**
	NIC2_LED	I		**This signal is used by the Front Panel to illuminate the green NIC 2 LED**
	ID_LED	I		**This signal is used by the Front Panel to illuminate the blue LED**
	SCSI_CHB_LED	I		**This signal is not connected**
	FP_PWR_LED_BUF	I		**This signal is used by the Front Panel to illuminate the power LED**
	CYA_FSRL_RXD	O		**This signal is passed from the SCSI Backplane to the Main board to indicate the appropriate LED model.**
	CYB_FSRL_DCD_L	O		**This signal is passed from the SCSI Backplane to the Main board to indicate the appropriate LED model.**
USB	USB_OC2_OC3_R_L	O		
	USB_P2_M	I/O	hs	
	USB_P2_P	I/O	hs	
	USB_P3_M	I/O	hs	
	USB_P3_P	I/O	hs	
Video	VID_FRNT_R	I		
	VID_FRNT_G	I		
	VID_FRNT_B	I		
	VHSYNC_FRNT	I		
	VHSYNC_FRNT	I		
	VID_FRNT_SCL	I		
	VID_FRNT_SDA	I/O		
	VID_FRNT_PRES_L	O		

6.3.3 IDE Connector

Table 31 is a summary of IDE connector pins, including the signal mnemonic, the name, and a brief description.

Table 31. IDE Board Signal Decsription – J4D1

Signal	Type	Driver	Name and Description
IDE_DD<15..0>	I/O	hs	**ISA Data**.
IDE_DREQ	I	hs	**Direct Memory Access (DMA) Request**.
IDE_DIOW_L	O	hs	**Write Request**. Handshake request for write operations.
IDE_DIOR_L	O	hs	**Read Request**. Handshake request for read operations.
IDE_IORDY	I	hs	**Ready**. Device ready for operation (high).
IDE_DACK_L	O	hs	**Direct Memory Access (DMA) Acknowledge**.
IDE_IRQ	O	hs	**Interrupt Request**.
IDE_DA<2..0>	O	hs	**Register Select Address.** (from ISA address bus).
IDE_CS1_L	O	hs	**Select Command Register Block** (0x1F0-0x1F7)
IDE_CS3_L	O	hs	**Select Control Register Block**. (0x3f6-0x3f7)
IDE_RST_BUF_R_L	O	hs	
IDE_DASP_L_PU	O		

6.3.4 Front Panel USB Connectors

These connectors provide two USB 1.1 ports.

Table 32. USB Connector Signal Description – J6K1, J5K1

Signal		Type	Driver	Name and Description
USB port 2(J6K1)	USB_FB_OC2			
	USB_P2_CONN_M	I/O		
	USB_P2_CONN_P	I/O		
	USB_P2_CABLE_GND			
USB port 3(J5K1)	USB_FB_OC3			
	USB_P3_CONN_M	I/O		
	USB_P3_CONN_P	I/O		
	USB_P3_CABLE_GND			

6.3.5 Front Panel VGA Connector

This connector provides a DB-15 video port.

Table 33. VGA Connector Signal Description – J5K2

Signal		Type	Driver	Name and Description
RGB VGA	RED	O		
	GREEN	O		
	BLUE	O		
	HSYNC	O		
	VSYNC	O		

Signal		Type	Driver	Name and Description
I^2C	VID_SCL	O		
	VID_SDA	I/O		
	V_PRES_L	I		
	VIDPWR	O		

6.3.6 SCSI Backplane Ribbon Connector

This connector provides the connection to the SCSI Backplane.

Table 34. SCSI Backplane Ribbon Connector Signal Description – J1D1

Signal		Type	Driver	Name and Description
ISP	ISP_SYS_EN_L	O	CMOS	**ISP Programming Enable.** Driven by an external programming device to enable the ISP part for programming.
	ISP_ SYS_TCK	O	CMOS	**ISP Programming Clock.** Driven by an external programming device to provide the ISP part a clock for programming.
	ISP_ SYS_MODE	O	CMOS	**ISP Programming Mode.** Driven by an external programming device to indicate to the ISP part what programming mode is desired.
	ISP_ SYS_TDI	O	CMOS	**ISP Programming Data In.** Driven by an external programming device to provide the ISP part data for programming.
	ISP_ SYS_TDO	I	CMOS	**ISP Programming Data Out.** Driven by the SR870BH2 Front Panel ISP part to propagate programming data back to an external programming device.
MISC	INTERLOCK_TO_SCSI_L	I/O	TTL	**Interlock Loop-back**. Two pins are used to indicate to the main board that the Flex cable has been installed between the Front Panel and the Main Board and that the ribbon cable has been installed betweeen the Front Panel and the SCSI Backplane.
	INTERLOCK_FROM_SCSI_L	I/O	TTL	**Interlock Loop-back**. Two pins are used to indicate to the main board that the Flex cable has been installed between the Front Panel and the Main Board and that the ribbon cable has been installed betweeen the Front Panel and the SCSI Backplane.
	INTRUSION_L	I		**Chassis Intrusion Detection.** This net is used in Telco products for the intrusion detection logic.
	PLD_RST_BUF_R_L	O		**Reset.** This reset is used for all reset and power good purposes on the Front Panel.
LED Ctrl	DFLT_LED	I		**This signal is used by the Front Panel to illuminate the DRIVE FAULT LED**
	CYA_FSRL_RXD	I		**This signal is passed from the SCSI Backplane to the Main board to indicate the appropriate LED model.**

Signal		Type	Driver	Name and Description
	CYB_FSRL_DCD_L	I		**This signal is passed from the SCSI Backplane to the Main board to indicate the appropriate LED model.**
I^2C	I2C_IPMB_SCL_GEM	O		**Docking IO Serial Clock.** This pin supplies an isolated version of the global IPMB Bus clock to the SCSI Backplane. The GEM Microcontroller is on this bus.
	I2C_IPMB_SDA_GEM	I/O		**Docking IO Serial Data.** This pin supplies an isolated version of the global IPMB Bus data to the SCSI Backplanel. The GEM Microcontroller is on this bus.

6.3.7 External LED Connector

This connector provides the connections to allow the use of an external two element LED..

Table 35. External LED Connector Signal Description – J5C1

Signal	Type	Driver	Name and Description
CYA_FB	O		LED A element control
CYB_FB	O		LED B element control
FP_LED_EN_FP	I		External LED presence to turn off on-board LEDs.

6.3.8 Intrusion Connector

The Intrusion connector provides an optional connection for a chassis intrusion switch.

Table 36. Intrusion Connector Signal Description – J5A1

Signal	Type	Driver	Name and Description
INTRUSION_L	I		Chassis Intrusion

6.4 Electrical, Environmental, and Mechanical Specifications

This section specifies the operational parameters and physical characteristics for the SR870BH2 Front Panel. This is a board-level specification only. System specifications are beyond the scope of this chapter.

Further topics in this section specify normal operating conditions for the SR870BH2 Front Panel, and mechanical specifications for the module and connector interfaces to the board.

6.4.1 Electrical Specifications

The power budget for the SR870BH2 Front Panel and pin-outs of the external interface connectors are defined here.

Table 37. Electrical Specifications

Feature	Absolute Maximum Rating
Voltage of any signal with respect to ground	-0.3 V to Vcc[1] to Vcc[1]+0.3 V
+5 Volt standby supply with respect to ground	-0.3 V to +5.25 V
+3.3 Volt standby supply with respect to ground	-0.3 V to +3.465 V
+5 Volt supply with respect to ground	-0.3 V to +5.25 V

Note: 1. Vcc means supply voltage for the device.

6.4.1.1 Power Consumption

Table 38 shows the power consumed on each supply line for the SR870BH2 Front Panel.

Note: The numbers in Table 38 are provided only to show design limits. Actual power consumption will vary depending on the exact configuration.

Table 38. Maximum Power Consumption

Devices	Power Dissipation
+5 Volt	15W
+5 Volt standby	1W
+3.3 Volt standby	.5W

6.4.1.2 Power Supply Requirements

The external and internal power supply must meet the following requirements:

- Rise time of less than 50 msec (for all voltages).
- Delay of 5 msec (minimum) from valid power to power good.
- See Table 39 for voltage regulation requirements.

Table 39. DC Voltage Regulation

DC Voltage	Acceptable Tolerance
+5 V standby	± 5%
+5 V	± 5%
+3.3 V standby	± 5%

6.4.2 Connector Specifications

Table 40 shows the reference designators, quantity, manufacturer, and part number for connectors on the baseboard. Refer to the manufacturer's documentation for more information. Pin-outs for the connectors follow.

Table 40. SR870BH2 Front Panel Connector Specifications

Item	Reference Designator(s)	Quantity	Manufacturer* and Part Number (or equivalent)	Description
1	J4D1	1	Foxconn HL93207-LD2	IDE connector
2	J1D1	1	Foxconn HL93107-LD2	SCSI Backplane Ribbon cable connector
3	J5C1	1	Tyco 104450-3 Foxconn HF14040-P1 Wieson 2175C888-001	External LED Connector
4	J6K1, J5K1	2	Tyvo 787616-6	USB connectors
5	J5J1	1	Tyco 5-179009-5	120 pin Flex Cable Connector
6	J2B1	1	Molex 43045-0412	2x2 Power connector
7	J5K2	1	Tyco 2-788574-1	VGA DB-15 connector
8	J5A1	1	Foxconn HF06021-P1	Intrusion connector

6.4.2.1 USB Connector Pin-out

The USB connectors provide front panel connectivity for USB 1.1 ports.

Table 41. USB Connector Pin-out – J5K1, J6K1

Pin	Signal
1	USB_FB_OCX
2	USB_PX_CONN_M
3	USB_PX_CONN_P
4	USB_PX_CABLE_GND
5	GND
6	GND

6.4.2.2 External LED Connector Pin-out

The External LED connector provides an optional connection for 2 LED elements.

Table 42. LED Connector Pin-out – J5C1

Pin	Signal
1	CYB_FB
2	CYA_FB
3	FP_LED_EN_FB
4	GND

6.4.2.3 Intrusion Connector Pin-out

The Intrusion connector provides an optional connection for a chassis intrusion switch.

Table 43. Intrusion Connector Pin-out – J5A1

Pin	Signal
1	INTRUSION_L
2	GND

6.4.2.4 Molex Power Connector Pin-out

The Molex power connector delivers power to and from the SCSI Backplane to the SR870BH2 Front Panel.

Table 44. Molex Power Connector Pin-out – J2B1

Pin	Signal	Pin	Signal
1	+5V	3	3.3VSTDBY(O)
2	+5VSTDBY	4	GND

6.4.2.5 120 pin FLEX Cable Connector Pin-out

Table 45. 120 pin FLEX Cable Connector Pin-out – J1A1

Pin	Signal	Pin	Signal
1	INTERLOCK_FROM SCSI_L	2	GND
3	VID_FRNT_R	4	VHSYNC_FRNT
5	VID_FRNT_G	6	VID_FRNT_PRES_L
7	VID_FRNT_B	8	VVSYNC_FRNT
9	GND	10	GND

Pin	Signal	Pin	Signal
11	NC	12	NC
13	GND	14	GND
15	ISP_SYS_TCK	16	ISP_PBAY_TDO
17	ISP_SYS_EN_L	18	GND
19	ISP_SYS_MODE	20	ISP_PBAY_TDI
21	GND	22	GND
23	CYB_FSRL_DCD_L	24	NC
25	CYA_FSRL_RXD	26	NC
27	NC	28	NC
29	NC	30	NC
31	USB_OC2_OC3_R_L	32	INTRUSION_L
33	GND	34	GND
35	USB_P3_M	36	USB_P2_M
37	USB_P3_P	38	USB_P2_P
39	GND	40	GND
41	GEN_FLT_GRN_LED	42	GEN_FLT_AMB_LED
43	NIC1_LED	44	ID_LED
45	NIC2_LED	46	NC
47	GND	48	PLD1_FLEX_XLINK
49	FP_ID_BTN_L	50	FP_SDINT_BTN_L
51	FP_RST_BTN_L	52	FP_PWR_BTN_L
53	I2C_IO_SCL	54	FP_PWR_LED_BUF
55	I2C_IO_SDA	56	+3.3VSTDBY
57	+3.3VSTDBY	58	+3.3VSTDBY
59	I2C_IPMB_SCL	60	BMC_SPKR
61	I2C_IPMB_SDA	62	VID_FRNT_SCL
63	VID_FRNT_SDA	64	RST_PCIRST_L
65	IDE_DD7	66	GND
67	GND	68	IDE_DD8
69	IDE_DD6	70	GND
71	GND	72	IDE_DD9
73	IDE_DD5	74	GND
75	GND	76	IDE_DD10
77	IDE_DD4	78	GND
79	GND	80	IDE_DD11
81	IDE_DD3	82	GND
83	GND	84	IDE_DD12
85	IDE_DD2	86	GND
87	GND	88	IDE_DD13
89	IDE_DD1	90	GND
91	GND	92	IDE_DD14
93	IDE_DD0	94	GND
95	GND	96	IDE_DD15

Pin	Signal	Pin	Signal
97	IDE_DREQ	98	GND
99	GND	100	IDE_DIOW_L
101	IDE_DIOR_L	102	GND
103	GND	104	IDE_IORDY
105	IDE_DACK_L	106	GND
107	GND	108	IDE_IRQ
109	IDE_DA1	110	GND
111	GND	112	IDE_DA0
113	IDE_DA2	114	GND
115	GND	116	IDE_CS1_L
117	IDE_CS3_L	118	GND
119	GND	120	INTERLOCK_TO_SCSI_L

6.4.2.6 IDE Connector Pin-out

Table 46 provides a pin-out for the IDE Board connector.

Table 46. IDE Board Connector Pin-out – J2E1

Pin	Signal	Pin	Signal
1	IDE_RST_BUF_R_L	2	GND
3	IDE_DD7	4	IDE_DD8
5	IDE_DD6	6	IDE_DD9
7	IDE_DD5	8	IDE_DD10
9	IDE_DD4	10	IDE_DD11
11	IDE_DD3	12	IDE_DD12
13	IDE_DD2	14	IDE_DD13
15	IDE_DD1	16	IDE_DD14
17	IDE_DD0	18	IDE_DD15
19	GND	20	
21	IDE_DREQ	22	GND
23	IDE_DIOW_L	24	GND
25	IDE_DIOR_L	26	GND
27	IDE_IORDY	28	100 ohm Pull down
29	IDE_DACK_L	30	GND
31	IDE_IRQ	32	NC
33	IDE_DA1	34	NC
35	IDE_DA0	36	IDE_DA2
37	IDE_CS1_L	38	IDE_CS3_L
39	IDE_DASP_L_PU	40	GND

6.4.3 Cooling requirements

The SR870BH2 Front Panel does not dissipate any significant heat. Cooling should not be required to maintain ambient temperatures.

6.4.4 Mechanical Specifications

Figure 44 shows the mechanical specifications and the connector positions for the SR870BH2 Front Panel. The board outline dimensions are 10.6” x 6.3". The board is routed to shape after assembly. Board thickness is 0.062” +.008/-.005”. All dimensions are in inches.

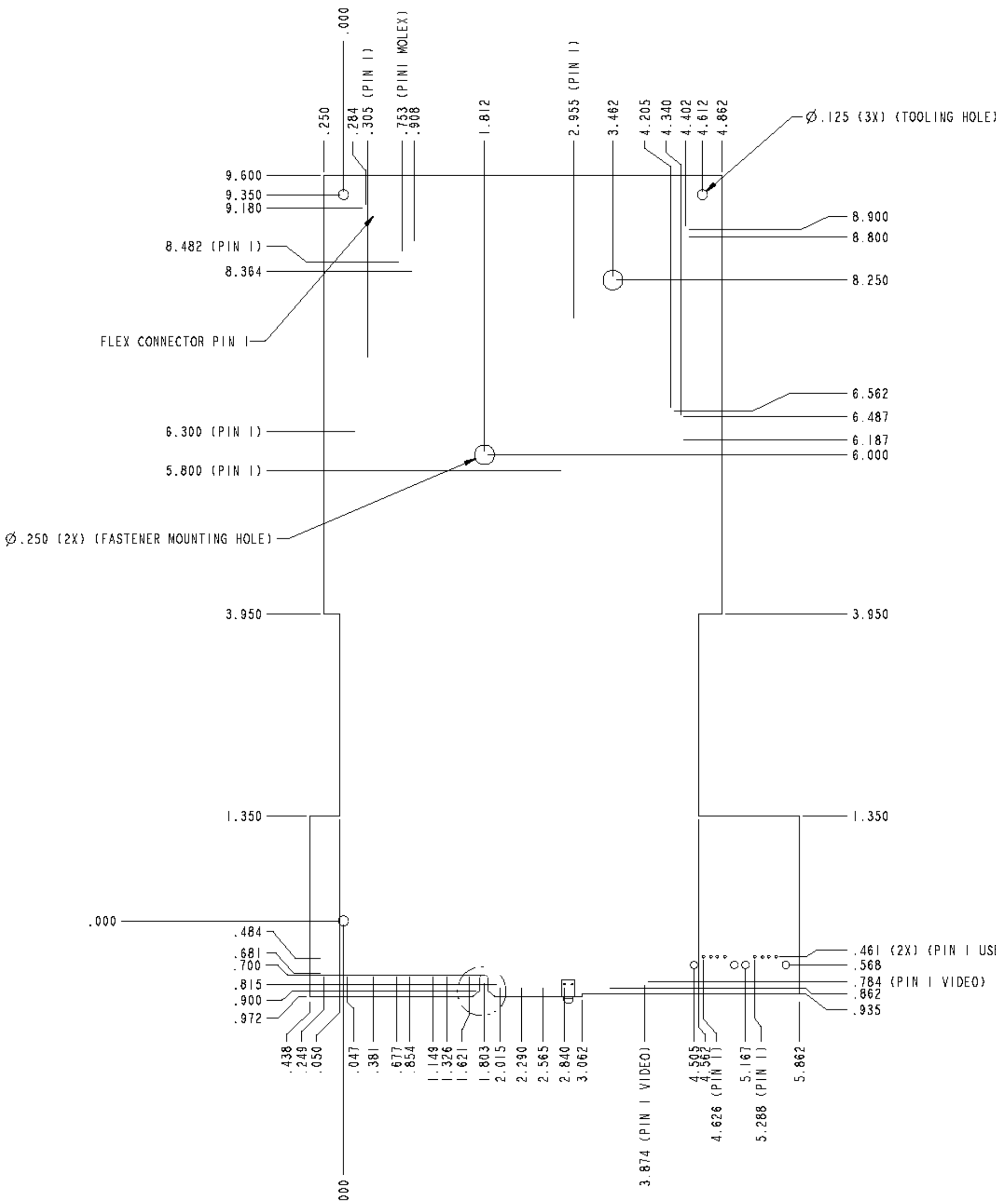

Figure 44. Front Panel Mechanical Specification

7. SCSI Backplane Board

This chapter describes the SR870BH2 SCSI Backplane. This chapter is organized into the following sections:

Section 7.1: Introduction
Provides an overview of the SR870BH2 SCSI Backplane showing functional blocks and board layout.

Section 7.2: Functional Architecture
Describes the SR870BH2 SCSI Backplane's functional blocks.

Section 7.3: Signal Descriptions
Summary of the SR870BH2 SCSI Backplane's internal signals and connector signals, and the connector signal pin names and the signal descriptions. Signal mnemonics appear throughout this chapter.

Section 7.4: Electrical, Environmental, and Mechanical Specifications
Specifies operational parameters and considerations, and connector pin-outs.

7.1 Introduction

The SR870BH2 SCSI Backplane is designed to give the end-user support for two SCSI hard drives. The design enables easy use and replacement of the SCSI hard drives without powering down the system. The following block diagram, architectural overview, and placement diagram will give a general idea how the SCSI Backplane back plane works.

7.1.1 Block Diagram

Figure 45 block diagram breaks down the SR870BH2 SCSI Backplane into physical and functional blocks. Arrows represent buses and signals. Blocks represent the physical and functional blocks. Figure 45 illustrates the general architecture of the SR870BH2 SCSI Backplane.

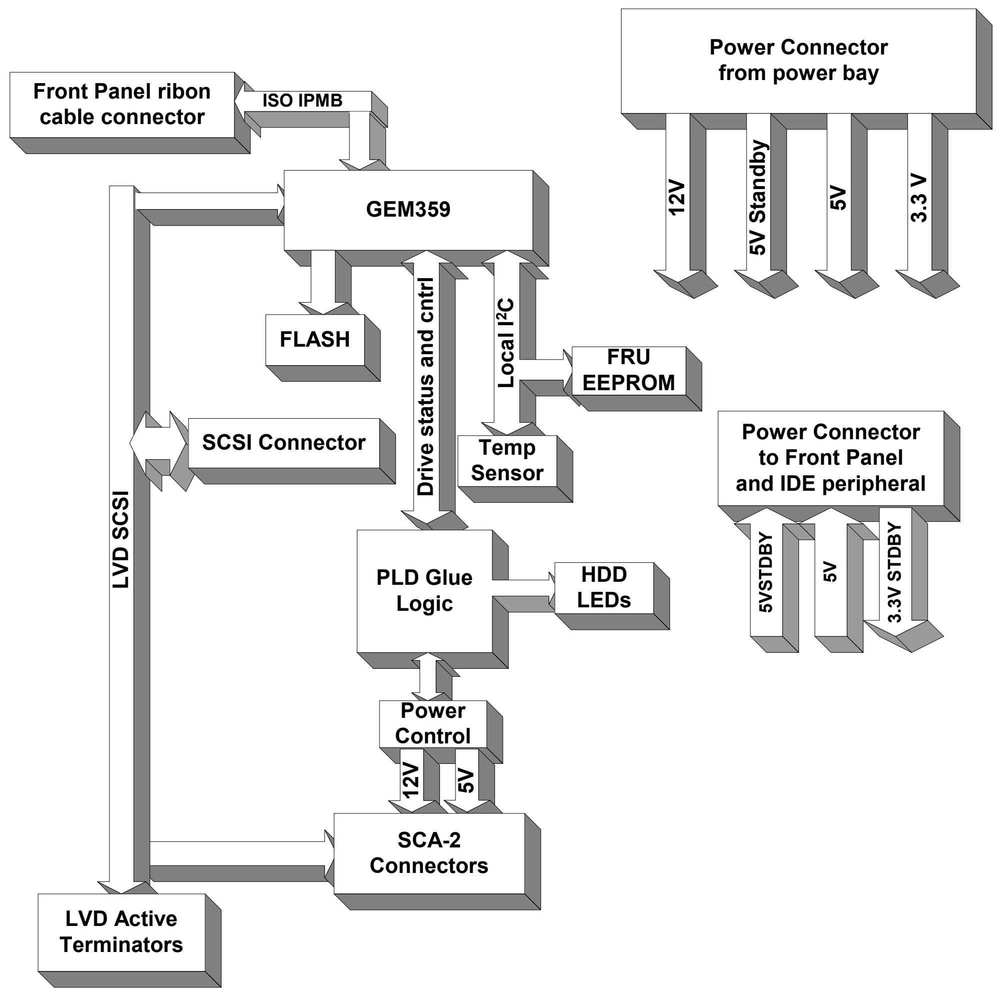

Figure 45. SCSI Backplane Block Diagram

7.1.2 Architectural Overview

The SR870BH2 SCSI Backplane provides three main functions for the system. The SCSI Backplane passes the SCSI signals between the Main board and the SCSI drives. The second function is to provide hooks for enclosure management. The third function is to provide I^2C server management interface

Functional blocks:

- Ultra 320 LVD SCSI bus passes SCSI signals between the SCSI drives and the Main board
  - A standard 68 pin SCSI connector provides the SCSI connection to the Main board.
  - Two 80 pin SCA-2 blind-mate connectors to mate with HS LVD SCSI drives
- Fault Tolerant Enclosure Management.
  - SAF-TE
  - SCSI Power Control
  - LED control logic
- Server management
  - I^2C interface
  - I^2C Serial CMOS EEPROM (FRU)
  - Temperature sensor

7.1.3 Component Location

Figure 46 shows the 2D placement of the major components and connectors on the SCSI Backplane. Figure 47 shows the 3D placement.

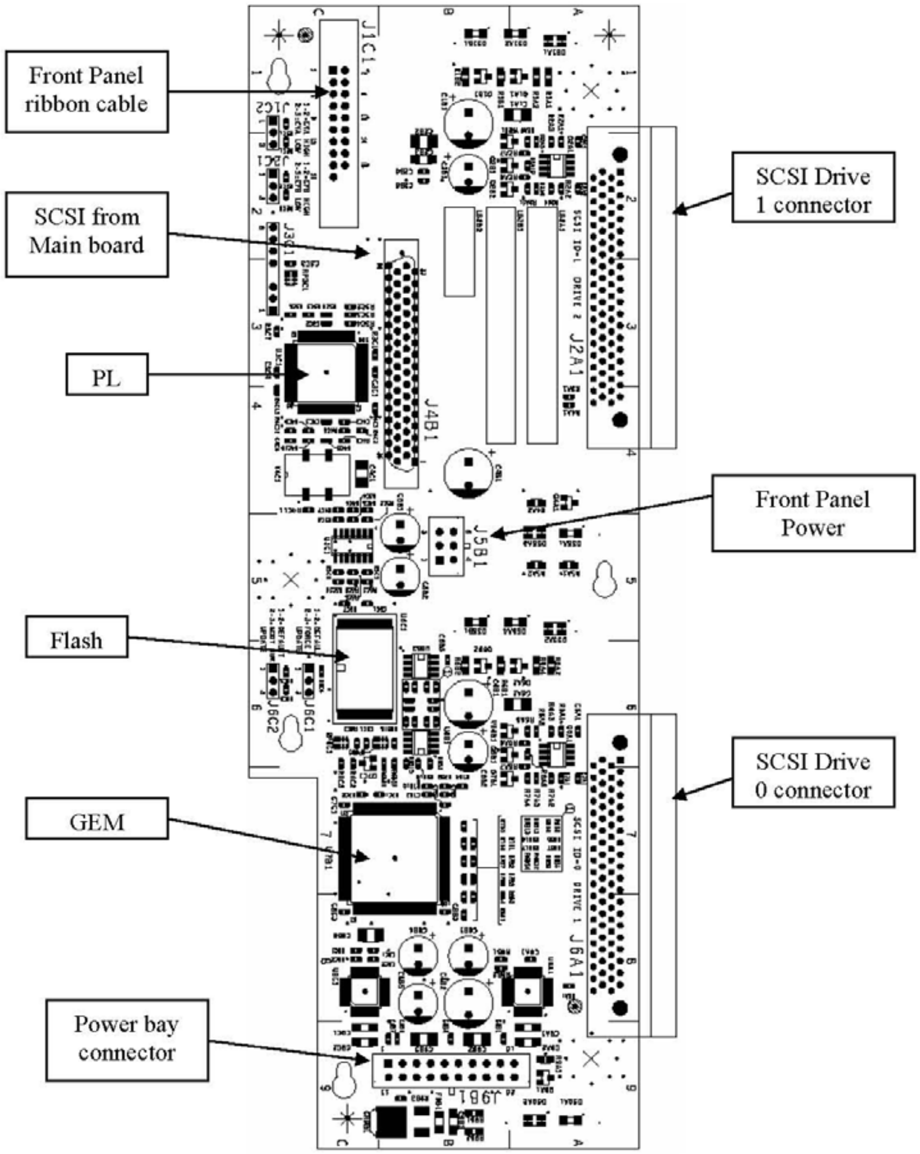

Figure 46. SCSI Backplane 2D Placement Diagram

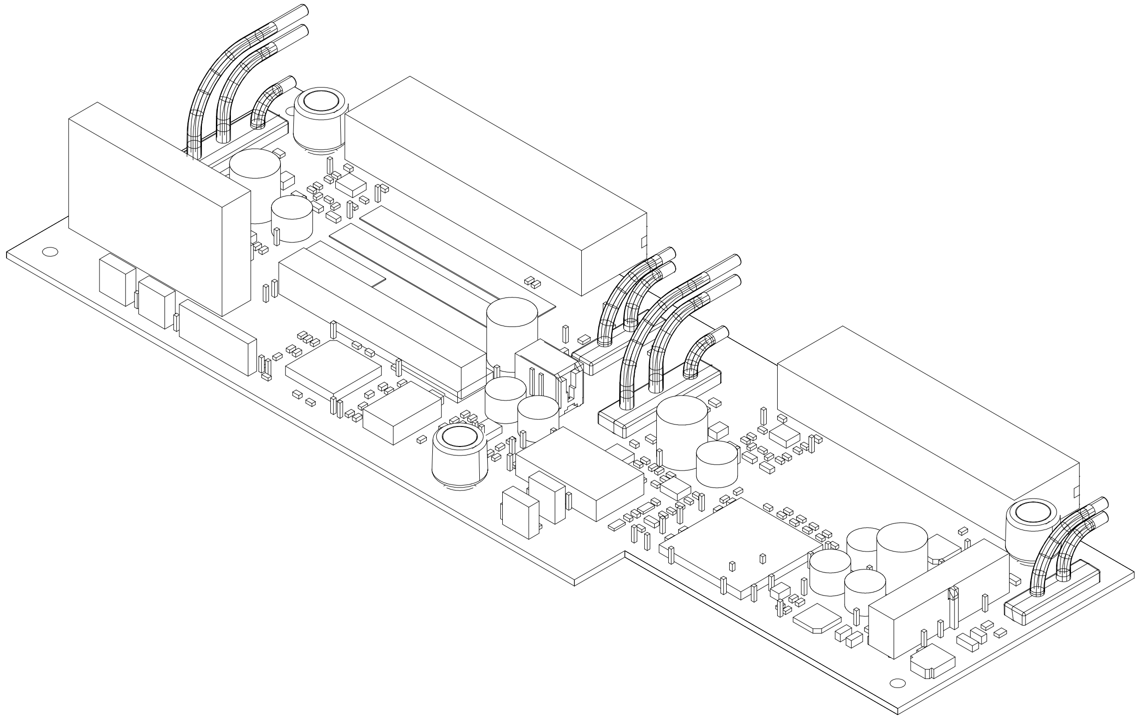

Figure 47. SCSI Backplane 3D Placement Diagram (light-pipes shown for ref only)

7.2 Functional Architecture

This section provides a more detailed architectural description of the SR870BH2 SCSI Backplane's functional blocks.

7.2.1 SCSI Bus

The SR870BH2 SCSI Backplane passes the SCSI bus from the IO board to the internal SCSI drives. The SCSI bus is Ultra 320 capable. SE drives are not supported. Do not install internal SE drive as the behavior of the drives in unpredictable and data corruption could result. The bus is comprised of 68 signals. The bus clock is 80 MHz. The 320 Mbytes data rate results from double transition (DT) data transfers on a two byte wide bus. The SCSI bus attaches to the Main board via a standard 68 pin SCSI connector.

320 Mbytes/s = 2 byte bus * 80 MHz clock * double transitions.

NOTE: Drives and SCSI controller on Main board determine actual SCSI bus data rate.

7.2.1.1 SCSI Drive Power Control

SCSI Power Control is provided on the SR870BH2 SCSI Backplane. SCSI Power Control includes SCSI drive power switching, initial power-on charge pumping, over-current protection, system status notification, and SCSI drive status LEDS.

If a SCSI drive is detected, the system will be notified. Then the system will instruct the SR870BH2 SCSI Backplane to apply power to the designated internal SCSI drive. Status LEDs will provide the user with visual indicators for the internal SCSI drive.

Once the system is powered up, the user can request the system to remove power to a SCSI drive. The system will instruct the SR870BH2 SCSI Backplane to remove power from the designated internal SCSI drive. The user can then safely remove the internal SCSI drive. Upon reinserting an internal SCSI drive, the user must notify the system. The system will then instruct the SR870BH2 SCSI Backplane to apply power to the specified drive.

7.2.1.1.1 Internal SCSI Drive Power Switching

Each SCSI drive is supplied with +12 V and +5 V. Separate MOSFET switches apply and remove the +12 V and +5 V to each internal SCSI drive.

7.2.1.1.2 Initial Power-on Charge pumping

When power is first applied to a SCSI drive there is a large initial current surge (up to 20 Amps). To reduce this initial current surge the SR870BH2 SCSI Backplane charge pumps the drives for ~700 us. Charge pumping the drives keeps the average power-on current to approximately three amps.

7.2.1.1.3 Over-current Protection

If either of the drive's power rails exceeds 5 amps, the MOSFET switch for the problematic rail will be turned off. Removing power will protect the MOSFET and system from damage in the event of a short on one of the power rails. After one third of a second the MOSFET will be turned on to see if the short has been removed. Turning on and checking for a short every one third of a second will continue until the system instructs the SR870BH2 backplane to remove power or the fault disappears.

When the MOSFET is first enabled, the over current condition is not detected during the power-up period. This no OCP period allows the initial current surge produced by many SCSI drives. The power-up period is short enough not allow damage to occur to the MOSFETS or the system.

7.2.1.1.4 Power Control Interlock

The Power Control Interlock prevents drives from powering on at the same time. Since only one drive can power on at once the board power requirements can be kept lower. After one drive starts the next drive will start one third of a second later.

7.2.1.1.5 System Status Notification

Internal SCSI drive status information is collected by the micro-controller. The micro-controller passes the information to the Server Management via the global I^2C bus and Enclosure Management via the SCSI bus.

7.2.1.1.6 SCSI Status LEDs

The status LEDs give the user a visual indication of the drives' condition. There are 3 separate LED models supported by the SR870BH2 SCSI Backplane. One has a single bi-color(amber and green) LED for each drive. The second model has two LEDs(one amber and one green) for each drive. The third model has a bicolor (amber and green) and a separate green LED for each drive. The LEDs use a combination of color and blinking frequency to indicate multiple conditions.

7.2.2 SCSI Enclosure Management

SCSI Enclosure Management allows the SR870BH2 SCSI Backplane to report on SCSI drive status via the SCSI bus. Normally a RAID controller will interface with Enclosure Management. The SCSI Enclosure Management subsystem consists of a Qlogic* GEM359 controller, Flash, and PLD (Programmable Logic Device).

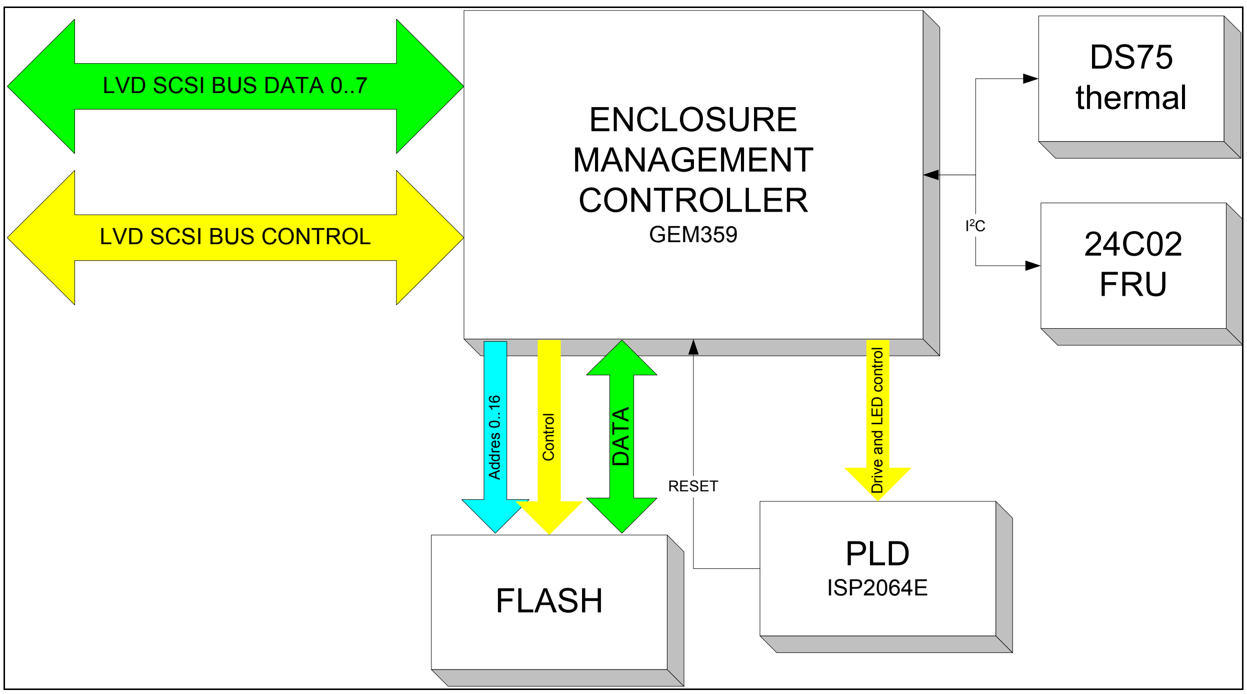

Figure 48. Enclosure Management Signal Flow Diagram

7.2.2.1 Qlogic* GEM359 Enclosure Management Controller

The GEM359 sends acquired board information to the SCSI bus and IPMB bus. The GEM359 also acts on requests from both the SCSI bus and IPMB bus. GEM359 GPIOs send LED and drive power control to the PLD.

7.2.2.2 4 Meg Flash

The GEM359's code is stored in a 4 Meg FLASH (512K x 8). The FLASH boot block is in the top 16k of the block. The boot block is protected. Non-protected FLASH can be updated via the IPMB bus.

7.2.2.3 PLD

The PLD uses the LED information and drive control data to control the LEDs and SCSI power control circuits.

7.2.3 Server Management Interface

The SR870BH2 SCSI Backplane will support the following Server Management features:

Local I²C Interface

- SR870BH2 SCSI Backplane Field Replaceable Unit (FRU)
- SR870BH2 SCSI Backplane temperature sensor
- Micro-controller interface

System I²C Interface

- Micro-controller IPMB interface

7.2.3.1 Local I²C Bus

The local I²C bus connects the DS75* (or equivalent) thermal sensor and Atmel AT24C02N* (or equivalent) serial EEPROM (with FRU data) to the micro-controller.

7.2.3.2 Isolated Global I²C Bus (IPMB)

The global I²C bus connects the micro-controller to the system. The global I²C bus has been isolated from the system until the system PWRGRD before it reaches the SR870BH2 SCSI Backplane

7.2.3.3 I²C Addresses

Three I²C devices and their addresses are listed in Table 47 and

Table 48. There are three I²C devices that can be addressed on or through the SR870BH2 SCSI Backplane.

- Hot Swap Micro Controller
- SR870BH2 SCSI Backplane FRU EEPROM
- SR870BH2 SCSI Backplane Temperature Sensor

Table 47. I²C Local Bus Addresses

Device	Address	Bus/Location	Description
AT24C02	0xA0	Legacy I²C/ SR870BH2 SCSI Backplane	Private SR870BH2 SCSI Backplane FRU EEPROM
DS75	0x90	Legacy I²C/ SR870BH2 SCSI Backplane	Private SR870BH2 SCSI Backplane temperature sensor

Table 48. I^2C Global Bus Addresses (IPMB Bus)

Device	Address	Bus/Location	Description
GEM359	0xC0	Legacy I^2C/ SR870BH2 SCSI Backplane	Micro controller public IPMB bus

7.2.4 Reset

All reset for logic on the SR870BH2 SCSI Backplane is supplied by the PLD_RST_BUF_R_L signal from the Main board via the Front panel connection.

7.2.5 Connector Interlocks

The SR870BH2 SCSI Backplane has interlocks on some of its connectors.

7.2.5.1 Front Panel ribbon cable connector

An Interlock signal is used by Main board to determine if the SR870BH2 SCSI Backplane is properly mated. The Front Panel connector interlock signal is currently labled as INTRUSION_L (The signal lable may be changed to INTERLOCK_L in a future fab).

7.2.5.2 SCA-2 Connector

Interlock is used by the SR870BH2 SCSI Backplane to determine if SCSI device is present. This interlock is defined by the SCSI_MATED# signals. Drive presence is used by enclosure management.

7.2.6 Clock Generation

There is a single local clock on the SR870BH2 SCSI Backplane.

10.0 MHz – supplies clock input to the GEM359 and PLD

7.2.7 Programmed Devices

There are three programmed devices on the SR870BH2 SCSI Backplane.

7.2.7.1 FLASH

Flash contains program code to be run by the onboard micro-controller.

Memory configuration: 512 K x 8

7.2.7.2 Field Replaceable Unit (FRU)

The FRU is initially programmed in the factory at ATE prior to functional test.

Memory Configuration: 2 k serial

7.2.7.3 Programmable Logic Device (PLD)

The PLD governs the SCSI Power Control circuit, controls LEDs, and can control IDE bus master/slave settings. The PLD is In System Programmable (ISP) and is attached to an ISP chain through the 120 pin FLEX Cable Connector.

7.3 Signal Descriptions

The following notations are used to describe the signal type, from the perspective of the SR870BH2 SCSI Backplane:

I	Input pin to the SR870BH2 SCSI Backplane
O	Output pin from the SR870BH2 SCSI Backplane
I/O	Bi-directional (input/output) pin
PWR	Power Supply pin

The signal description also includes the type of buffer used for the particular signal:

LVD	Low Voltage Differential SCSI
SE	Standard Single Ended SCSI
TTL	5V TTL signals
CMOS	5V CMOS signals
3.3V CMOS	3.3V CMOS signals
Analog	Typically a voltage reference or specialty power supply
hs	This suffix is added to indicate high speed requirements that would make any modifications subject to detailed review

7.3.1 Power Bay Connector

Table 49 is a summary of power connector pins, including the signal mnemonic, the name, and a brief description.

Table 49. Power Bay Interface Signals – J8E1

Signal	Type	Driver	Name and Description
+12V	I	PWR	+12 Volt supply from power bay.
+5V	I	PWR	+5 Volt supply from power bay.
+5VSTBY	I	PWR	+5 Volt supply from power bay.
+3.3V	I	PWR	+3 Volt supply from power bay.

7.3.2 Front Panel Power Connector

Table 50 is a summary of power connector pins, including the signal mnemonic, the name, and a brief description.

Table 50. Front Panel Power Interface Signals – J5B1

Signal	Type	Driver	Name and Description
+3.3VSTDBY	O	PWR	+3.3 Volt supply to SCSI backplane.
+5V	I	PWR	+5 Volt supply to Front Panel / IDE Peripheral
+5VSTBY	I	PWR	+5 Volt supply to Front Panel

7.3.3 Front Panel Ribbon Cable Connector

The Front Panel Ribbon Cable Connector carries signals between the SR870BH2 SCSI Backplane and Front Panel. The signal groups are ISP and I^2C. Table 51 provides a description of the Front Panel Ribbon Cable Connector.

Table 51. Front Panel Ribbon Connector Signal Description – J1C1

Signal		Type	Driver	Name and Description
ISP	ISP_SYS_EN_L	I	CMOS	**ISP Programming Enable.** Driven by an external programming device to enable the ISP part for programming.
	ISP_ SYS_TCK	I	CMOS	**ISP Programming Clock.** Driven by an external programming device to provide the ISP part a clock for programming.
	ISP_ SYS_MODE	I	CMOS	**ISP Programming Mode.** Driven by an external programming device to indicate to the ISP part what programming mode is desired.
	ISP_ SYS_TDI	I	CMOS	**ISP Programming Data In.** Driven by an external programming device to provide the ISP part data for programming.
	ISP_ SYS_TDO	O	CMOS	**ISP Programming Data Out.** Driven by the SR870BH2 Front Panel ISP part to propagate programming data back to an external programming device.
MISC	INTRUSION_L	I/O	TTL	**Interlock Loop-back**. Two pins are used to indicate to the main board that the Flex cable has been installed between the Front Panel and the Main Board and that the ribbon cable has been installed betweeen the Front Panel and the SCSI Backplane. (*Note: should have been INTERLOCK_L may be corrected in future fab)
	PLD_RST_BUF_R_L	I		**Reset.** This reset is used for all reset and power good purposes on the Front Panel.
LED Ctrl	DFLT_LED	O		This signal is used by the Front Panel to illuminate the DRIVE FAULT LED

Signal		Type	Driver	Name and Description
	CYA_FSRL_RXD	O		This signal is passed from the SCSI Backplane to the Main board to indicate the appropriate LED model.
	CYB_FSRL_DCD_L	O		This signal is passed from the SCSI Backplane to the Main board to indicate the appropriate LED model.
I^2C	I2C_IPMB_SCL_GEM	I		**Docking IO Serial Clock.** This pin supplies an isolated version of the global IPMB Bus clock to the SCSI Backplane. The GEM Microcontroller is on this bus.
	I2C_IPMB_SDA_GEM	I/O		**Docking IO Serial Data.** This pin supplies an isolated version of the global IPMB Bus data to the SCSI Backplanel. The GEM Microcontroller is on this bus.

7.3.4 LVD SCSI Connector

The LVD SCSI Connector carries SCSI signals between the SR870BH2 SCSI Backplane and Main board. Table 52 provides a description of the LVD SCSI Connector.

Table 52. LVD SCSI Connector Signal Description – J4B1

Signal	Type	Driver	Name and Description
LVD_DB[15..0]_[P, N]	I/O	LVD hs	**SCSI Data Bus.** These pins are the data bits for the differential SCSI bus
LVD_DBP_[P, N] LVD_DBP1_[P, N]	I/O	LVD hs	**SCSI Data Parity.** These pins support parity on the SCSI bus. DB_P0[P/N] supports parity for data [7..0]. DB_P1[P/N] supports parity for data [15..8].
DIFFSENSE	I	Analog	**Differential Sense.** The voltage level determines the operating mode of the target devices on the SCSI bus. If the voltage on the DIFFSENSE signal is from –0.35 V to +0.5 V the mode will be SE. If it is from +0.7 V to 1.9 V the mode will be LVD.
LVD_ATN_[P, N]	I/O	LVD hs	**SCSI Bus Attention.** These pins are asserted by a SCSI device in initiator mode to alert the target that the initiator has a message to transfer.
LVD_BSY_[P, N]	I/O	LVD hs	**SCSI Bus Busy.** These pins indicate that the SCSI bus is being used. Can be driven by both the initiator and the target device.
LVD_ACK_[P, N]	I/O	LVD hs	**SCSI Bus Acknowledge.** These pins driven by an initiator, indicating an acknowledgement for a SCSI data transfer.
LVD_RST_[P, N]	I/O	LVD hs	**SCSI Bus Reset.** These pins indicated a SCSI bus reset condition.
LVD_MSG_[P, N]	I/O	LVD hs	**SCSI Bus Message Phase.** These pins are driven by a SCSI target to indicate it is in the Message Phase.
LVD_SEL_[P, N]	I/O	LVD hs	**SCSI Bus Select.** These pins are used by an initiator to select a target or by a target to reselect an initiator.
LVD_CD_[P, N]	I/O	LVD hs	**SCSI Bus Control/Data Phase.** Driven by a target, these pins indicate that control or data information is being transferred over the SCSI bus.
LVD_REQ_[P, N]	I/O	LVD hs	**SCSI Bus Request.** Driven by a target, these pins indicate a request for a SCSI data-transfer handshake.

Signal	Type	Driver	Name and Description
LVD_IO_[P, N]	I/O	LVD hs	**SCSI Bus I/O Phase.** Driven by the target, these pins control the direction of data transfer on the SCSI bus. When asserted, this signal indicates input to the initiator. When not asserted, this signal indicates output from the initiator.
GND	I/O	PWR	**Ground.** These pins provide Secondary Ground reference.

7.3.5 LVD SCSI Drive Connectors

The LVD connector carries signals between the SR870BH2 SCSI Backplane and internal SCSI drives. The LVD SCSI bus' signals are driven by either the I/O baseboard SCSI controller, the LVD Transceiver, or the internal SCSI drives. Table 53 provides a description of each signal on the SCSI connectors.

Table 53. LVD SCSI Bus Signals –J2A1, and J6A1

Signal	Type	Driver	Name and Description
LVD_DB[15..0]_[P, N]	I/O	LVD hs	**SCSI Data Bus.** These pins, with the DBP[1/0][P/N] pins form the bi-directional SCSI data bus.
LVD_DBP_[P, N] LVD_DBP1_[P, N]	I/O	LVD hs	**SCSI Data Parity.** These pins support parity on the SCSI bus. DBP[P/N] supports parity for data [7..0] DBP1[P/N] supports parity for data [15..8]
DIFFSENSE	I	Analog	**Differential Sense.** This pin monitors the DIFFSENSE signal from the terminator. The voltage level determines the operating mode of the target devices on the SCSI bus. If the voltage on the DIFFSENSE signal is from –0.35 V to +0.5 V the mode will be SE. If it is from +0.7 V to 1.9 V the mode will be LVD.
LVD_ATN_[P, N]	I/O	LVD hs	**SCSI Bus Attention.** These pins are asserted by a SCSI device in initiator mode to alert the target that the initiator has a message to transfer.
LVD_BSY_[P, N]	I/O	LVD hs	**SCSI Bus Busy.** In SE mode, these pins are bi-directional and are asserted to gain use of the SCSI bus and to indicate that that SCSI bus is in use.
LVD_ACK_[P, N]	I/O	LVD hs	**SCSI Bus Acknowledge.** These pins are asserted by a SCSI device in initiator mode to acknowledge the target's request for a data transfer.
LVD_RST_[P, N]	I/O	LVD hs	**SCSI Bus Reset.** In SE mode, these pins are bi-directional and are asserted when all the SCSI devices attached to the SCSI bus need to be reset.
LVD_MSG_[P, N]	I/O	LVD hs	**SCSI Bus Message Phase.** These pins are asserted by a SCSI device in target mode to indicate the Message In or Message Out phase.
LVD_SEL_[P, N]	I/O	LVD hs	**SCSI Bus Select.** In SE mode, these pins are bi-directional and are asserted by the controller when attempting to select or reselect a SCSI device.
LVD_CD_[P, N]	I/O	LVD hs	**SCSI Bus Control/Data Phase.** These pins are asserted or de-asserted by a SCSI device in target mode to indicate that control or data information is being transferred over the SCSI bus

Signal	Type	Driver	Name and Description
LVD_REQ_[P, N]	I/O	LVD hs	**SCSI Bus Request.** These pins are asserted by a SCSI device in target mode to indicate that the target is requesting a data transfer over the SCSI bus.
LVD_IO_[P, N]	I/O	LVD hs	**SCSI Bus I/O Phase.** These pins are asserted by a SCSI device in target mode to indicate the direction of data movement on the SCSI bus between the target and the initiator.
SCSI_ID	O	GND/OPEN	**SCSI ID.** Sets internal SCSI ID depending on slot. Drive 0 has SCSI address 0. Drive 1 has SCSI address 1.
SCSI_MATED [1,2]	I/O	TTL	**SCSI MATED.** Pins are used to determine if SCSI is present and has proper contact. See T10/1302D Annex C for additional information.
GND	I/O	PWR	**Ground. These pins provide Secondary Ground reference.**
+12V	O	PWR	**+12 Volt supply.** Max 1 amp of continuous current. Max 6 amps peak current.
+5V	O	PWR	**+5 Volt supply.** Max 1.4 amps of continuous current. Max 6 amps peak current.

7.3.6 Internal Logic Signals

Table 54 is a summary of the signals that route between logic on the SR870BH2 SCSI Backplane.

Table 54. Internal Logic Signals

	Signal	Type	Driver	Name and Description
Clks	CLK_10MHz	O	CMOS	**10-MHz Clock.** This signal is the 10-MHz clock used by the GEM359 and PLD.
GEM359 Logic Contrl	ADDR<16..0>	O	CMOS	**Address/Bus.** These pins are used as address bus for the FLASH.
	PROM_VPP_L	O	CMOS	**FLASH PROGRAM VOLTAGE ENABLE.** This pin in driven by the SR870BH2 SCSI Backplane GEM359 to all FLASH to be programmed.
	PROM_OE_L	O	CMOS	**FLASH Output Enable.** This pin is driven by the SR870BH2 SCSI Backplane GEM359 to enable the Flash for writing data on the bus.
	PROM_CE_L	O	CMOS	**FLASH Output Enable.** This pin is driven by the SR870BH2 SCSI Backplane PLD to enable the Flash.
	PROM_WE_L	I	CMOS	**FLASH Chip Enable.** This pin is driven by the SR870BH2 SCSI Backplane GEM359 to enable the Flash to be written to.
SCSI Power Control	KCK_5V_L [0,1]	0	Analog	**5 Volt KICK START.** Primes 5 Volt FET to start delivering power to drive
	KCK_12V_L [0,1]	0	Analog	**12 Volt KICK START.** Primes 12 Volt FET, to start delivering power to drive.
	FLT_5V_L [0,1]	I	CMOS	**5 Volt HOTSWAP FAULT.** Indicates greater than 5 amps of current drawn from 5V rail.

Signal		Type	Driver	Name and Description
	FLT_12V_L [0,1]	I	CMOS	**12 Volt HOTSWAP FAULT.** Indicates greater than 5 amps of current drawn from 12-V rail.
	STP_5V_L[0,1]	I	Analog	**5 Volt STOP.** Stops 5 Volt FET from delivering power to drive.
	STP_12V_L[0,1]	I	Analog	**12 Volt STOP.** Stops 12 Volt FET from delivering power to drive.
	PWR_TIMER	O	Analog	**Power Timer.** Starts one second timer for FET reset.
	TMR_DONE	I	Analog	**TIMER DONE.** One second reset timer complete.

7.4 Electrical, Environmental, and Mechanical Specifications

This section specifies the operational parameters and physical characteristics for the SR870BH2 SCSI Backplane. This is a board-level specification only. System specifications are beyond the scope of this chapter.

Further topics in this section specify normal operating conditions for the SR870BH2 SCSI Backplane, and mechanical specifications for the module and connector interfaces to the board.

7.4.1 Electrical Specifications

The power budget for the SR870BH2 SCSI Backplane and pin-outs of the external interface connectors are defined here.

Table 55. Electrical Specifications

Feature	Absolute Maximum Rating
Voltage of any signal with respect to ground	-0.3 V to Vcc[1] to Vcc[1]+0.3 V
+5 Volt standby supply with respect to ground	-0.3 V to +5.25 V
+3.3 Volt standby supply with respect to ground	-0.3 V to +3.465 V
+3 Volt supply with respect to ground	-0.3 V to +3.465 V
+5 Volt supply with respect to ground	-0.3 V to +5.25 V
+12 Volt supply with respect to ground	-0.3 V to +12.6 V

Note: 1. Vcc means supply voltage for the device.

7.4.1.1 Power Consumption

Table 56 shows the power consumed on each supply line for the SR870BH2 SCSI Backplane.

Note: The numbers in Table 56 are provided only to show design limits. Actual power consumption will vary depending on the exact configuration.

Table 56. Maximum Power Consumption

Devices	Power Dissipation
12 V	60W
5 V	20W
5 V Standby	.5W
3 V	2W
3.3 V Standby	.5W

7.4.1.2 SCSI Drive Supplied Power

The SCSI drives installed in the system must fall within power limits shown in Table 57. The SR870BH2 SCSI Backplane was originally designed to work with the Seagate Cheetah* X15-18LP ST318451, however drives that meet the following requirements can be used.

Table 57. SR870BH2 SCSI Backplane Power Limits per Drive

Device constraint	+5 V	+12 V
Peak Start Current	0.73	1.5 amps
Max Operating Current	0.81	1.15 amps
Average Idle	0.68 amps	0.61 amps

7.4.1.3 Power Supply Requirements

The external and internal power supply must meet the following requirements:

- Rise time of less than 50 msec (for all voltages).
- Delay of 5 msec (minimum) from valid power to power good.
- See Table 58 for voltage regulation requirements.

Table 58. DC Voltage Regulation

DC Voltage	Acceptable Tolerance
+5 V standby	± 5%
+5 V	± 5%
+12 V	± 5%
+3.3 V	± 5%
+3.3 V standby	± 5%

7.4.2 Connector Specifications

Table 59 shows the reference designators, quantity, manufacturer, and part number for connectors on the baseboard. Refer to the manufacturer's documentation for more information. Pin-outs for the connectors follow.

Table 59. SR870BH2 SCSI Backplane Connector Specifications

Item	Reference Designator(s)	Quantity	Manufacturer and Part Number (or equivalent)	Description
1	J9B1	1	Molex 43045-2012	Power Bay connector
2	J5B1	1	Molex 43045-0612	FP Power connector
3	J2A1, J6A1	2	FoxConn LS24403-J3M	80 pin SCA-2 connector
4	J4B1	1	FoxConn QA01343-P4M Molex 015870314	SCSI Connector to Main board
5	J1C1	1	Foxconn HL93107-LD2	FP Ribbon Cable connector

7.4.2.1 Power Bay Connector Pin-out

The Power Bay connector delivers power from the power cage to the SR870BH2 SCSI Backplane.

Table 60. Power Bay Connector Pin-out – J9B1

Pin	Signal	Pin	Signal
11	NC	1	+3.3V
12	GND	2	+5VSTDBY
13	GND	3	+5V
14	GND	4	+5V
15	NC	5	+5V
16	GND	6	+5V
17	GND	7	+12V
18	GND	8	+12V
19	GND	9	+12V
20	GND	10	+12V

7.4.2.2 Front Panel Power Connector Pin-out

The Front Panel Power connector delivers power from the power cage to the SR870BH2 SCSI Backplane.

Table 61. Front Panel Power Connector Pin-out – J9B1

Pin	Signal	Pin	Signal
4	+5V	1	+3.3VSTDBY
5	+5VSTDBY	2	GND
6	+5V	3	GND

7.4.2.3 SCSI Connector Pin-out

The SCSI input connector is a non-shielded device connector.

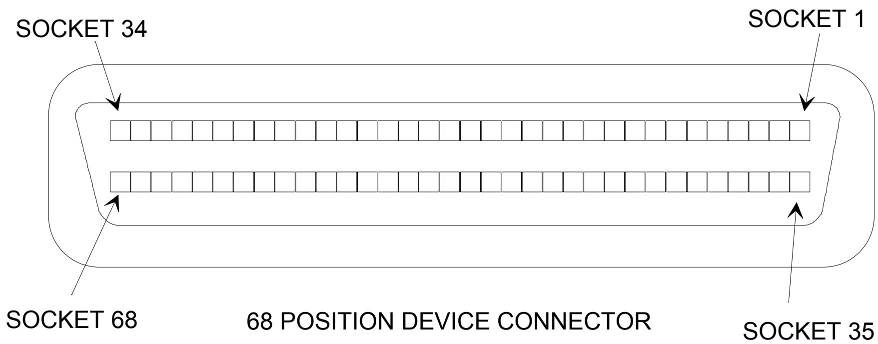

Figure 49. SCSI Input connector 68P Non-Shielded

Table 62. SCSI Connector Pin-out – LVDS Mode – J4B1

Signal Name	Conn. Pin	Cable Pin	Cable Pin	Conn. Pin	Signal Name
SCSI(A:B)_DB_P12	1	1	2	35	SCSI(A:B)_DB_N12
SCSI(A:B)_DB_P13	2	3	4	36	SCSI(A:B)_DB_N13
SCSI(A:B)_DB_P14	3	5	6	37	SCSI(A:B)_DB_N14
SCSI(A:B)_DB_P15	4	7	8	38	SCSI(A:B)_DB_N15
SCSI(A:B)_DB_PP1	5	9	10	39	SCSI(A:B)_DB_NP1
SCSI(A:B)_DB_P0	6	11	12	40	SCSI(A:B)_DB_N0
SCSI(A:B)_DB_P1	7	13	14	41	SCSI(A:B)_DB_N1
SCSI(A:B)_DB_P2	8	15	16	42	SCSI(A:B)_DB_N2
SCSI(A:B)_DB_P3	9	17	18	43	SCSI(A:B)_DB_N3
SCSI(A:B)_DB_P4	10	19	20	44	SCSI(A:B)_DB_N4
SCSI(A:B)_DB_P5	11	21	22	45	SCSI(A:B)_DB_N5
SCSI(A:B)_DB_P6	12	23	24	46	SCSI(A:B)_DB_N6
SCSI(A:B)_DB_P7	13	25	26	47	SCSI(A:B)_DB_N7
SCSI(A:B)_DP0_P	14	27	28	48	SCSI(A:B)_DP0_N
GND	15	29	30	49	GND
SCSI(A:B)_DIFFSENSE	16	31	32	50	GND
SCSI(A:B)_TERMPWR	17	33	34	51	SCSI(A:B)_TERMPWR
SCSI(A:B)_TERMPWR	18	35	36	52	SCSI(A:B)_TERMPWR
RESERVED (NC)	19	37	38	53	RESERVED
GND	20	39	40	54	GND
SCSI(A:B)_ATN_P	21	41	42	55	SCSI(A:B)_ATN_N
GND	22	43	44	56	GND
SCSI(A:B)_BSY_P	23	45	46	57	SCSI(A:B)_BSY_N
SCSI(A:B)_ACK_P	24	47	48	58	SCSI(A:B)_ACK_N
SCSI(A:B)_RST_P	25	49	50	59	SCSI(A:B)_RST_N
SCSI(A:B)_MSG_P	26	51	52	60	SCSI(A:B)_MSG_N
SCSI(A:B)_SEL_P	27	53	54	61	SCSI(A:B)_SEL_N
SCSI(A:B)_CD_P	28	55	56	62	SCSI(A:B)_CD_N
SCSI(A:B)_REQ_P	29	57	58	63	SCSI(A:B)_REQ_N
SCSI(A:B)_IO_P	30	59	60	64	SCSI(A:B)_IO_N
SCSI(A:B)_DB_P8	31	61	62	65	SCSI(A:B)_DB_N8
SCSI(A:B)_DB_P9	32	63	64	66	SCSI(A:B)_DB_N9
SCSI(A:B)_DB_P10	33	65	66	67	SCSI(A:B)_DB_N10
SCSI(A:B)_DB_P11	34	67	68	68	SCSI(A:B)_DB_N11

Table 63 provides a pin-out for the SCSI connector.

Table 63. SCSI Drive Connector Pin-out – J2A1, and J6A1

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+12V	21	LVD_DB7_N	41	GND	61	LVD_DB7_P
2	+12V	22	LVD_DB6_N	42	GND	62	LVD_DB6_P
3	+12V	23	LVD_DB5_N	43	GND	63	LVD_DB5_P

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
4	+12V	24	LVD_DB4_N	44	SCSI_MATED	64	LVD_DB4_P
5	NC	25	LVD_DB3_N	45	NC	65	LVD_DB3_P
6	NC	26	LVD_DB2_N	46	DIFFSENSE	66	LVD_DB2_P
7	LVD_DB11_N	27	LVD_DB1_N	47	LVD_DB11_P	67	LVD_DB1_P
8	LVD_DB10_N	28	LVD_DB0_N	48	LVD_DB10_P	68	LVD_DB0_P
9	LVD_DB9_N	29	LVD_DBP1_N	49	LVD_DB9_P	69	LVD_DBP1_P
10	LVD_DB8_N	30	LVD_DB15_N	50	LVD_DB8_P	70	LVD_DB15_P
11	LVD_IO_N	31	LVD_DB14_N	51	LVD_IO_P	71	LVD_DB14_P
12	LVD_REQ_N	32	LVD_DB13_N	52	LVD_REQ_P	72	LVD_DB13_P
13	LVD_CD_N	33	LVD_DB12_N	53	LVD_CD_P	73	LVD_DB12_P
14	LVD_SEL_N	34	+5V	54	LVD_SEL_P	74	SCSI_MATED
15	LVD_MSG_N	35	+5V	55	LVD_MSG_P	75	GND
16	LVD_RST_N	36	+5V	56	LVD_RST_P	76	GND
17	LVD_ACK_N	37	NC	57	LVD_ACK_P	77	SCSI_ACT
18	LVD_BSY_N	38	GND	58	LVD_BSY_P	78	NC
19	LVD_ATN_N	39	SCSI_ID (0)	59	LVD_ATN_P	79	SCSI_ID(1)
20	LVD_DBP_N	40	SCSI_ID (2)	60	LVD_DBP_P	80	SCSI_ID(3)

7.4.3 Cooling requirements

The SR870BH2 SCSI Backplane cooling requirements have not been finalized. The cooling requirements of the SCSI drives that will be docked into the SCSI Backplane are expected to be more significant than those associated with the power dissipation of the SCSI Backplane components themselves.

7.4.4 Mechanical Specifications

Figure 50 shows the mechanical specifications and the connector positions for the SR870BH2 SCSI Backplane. The board outline dimensions are 5.3" x 9.7". The board is routed to shape after assembly. Board thickness is 0.062” +.008/-.005”. All dimensions are in inches.

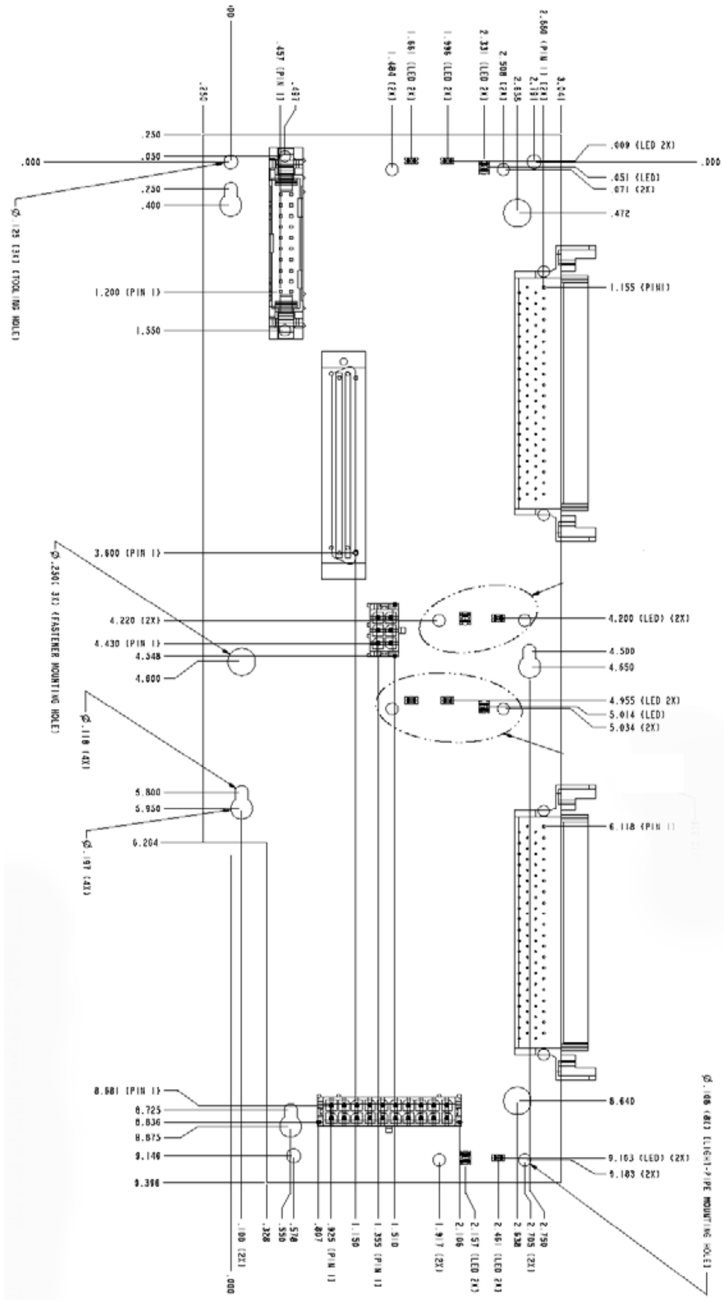

Figure 50. SCSI Backplane Mechanical Specification

8. Peripheral Adapter Board

This chapter describes the DVD/CD peripheral adapter board used in the SR870BH2 server system. The DVD/CD adapter board transitions from the JAE slimline peripheral connector to a standard 40 pin IDE ribbon cable and separate power connector.

8.1 Mechanical Outline

Mechanical outline drawings of the DVD/CD adapter board are shown in Figure 51 and an isometric view in Figure 2.

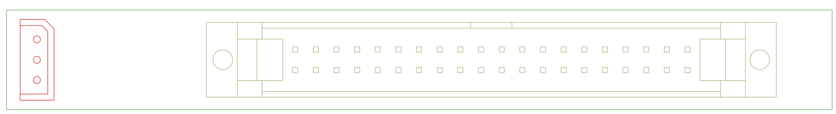

Figure 51. Mechanical Outline of Peripheral Adapter Boards

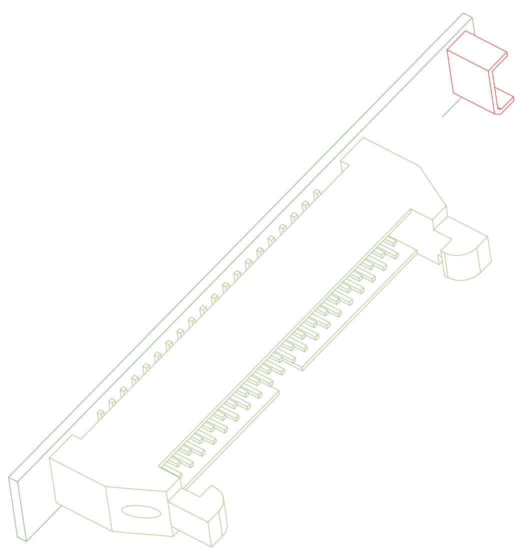

Figure 52. Isometric View of Peripheral Adapter Board

8.2 Connector Pin-outs

Connector pin-outs of peripheral adapter boards are listed in the following tables. Table 64 is the JAE connector from Peripheral to adaptor board, Table 2 is the standard 40 pin IDE connector and Table 3 is the power connector.

Table 64. Peripheral Adapter Board JAE Connector Pin-out

Pin	Signal	Signal	Pin
1	Audio L-Ch	Audio R-Ch	2
3	Audio GND	GND	4
5	RESET-	DD8	6
7	DD7	DD9	8
9	DD6	DD10	10
11	DD5	DD11	12
13	DD4	DD12	14
15	DD3	DD13	16
17	DD2	DD14	18
19	DD1	DD15	20
21	DD0	DMARQ	22
23	GND	/DIOR	24
25	DIOW-	GND	26
27	IORDY	/DMACK	28
29	INTRQ	/IOCS16	30
31	DA1	/PDIAG	32
33	DA0	DA2	34
35	/CS1FX	/CS3FX	36
37	/DASP	+5V	38
39	+5V	+5V	40
41	+5V	+5V	42
43	GND	GND	44
45	GND	GND	46
47	CSEL	GND	48
49	RESERV	RESERV	50

Table 65. Peripheral Adapter Board 40 Pin Connector Pin-out

Pin	Signal	Signal	Pin
1	RESET	GND	2
3	DD7	DD8	4
5	DD6	DD9	6
7	DD5	DD10	8
9	DD4	DD11	10
11	DD3	DD12	12
13	DD2	DD13	14
15	DD1	DD14	16
17	DD0	DD15	18
19	GND	KEYPIN (NC)	20
21	DMARQ	GND	22
23	DIOW	GND	24
25	DIOR	GND	26
27	IORDY	CSEL	28
29	DMACK	GND	30
31	INTRQ	RESERVED	32
33	DA1	PDIAG	34
35	DA0	DA2	36
37	CS0	CS1	38
39	DASP	GND	40

Table 66. Peripheral Adapter Board Power Pin-outs

Pin	Signal	Signal	Pin
1	Ground	+5V	2

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9. Regulatory Specifications

The SR870BH2 server system meets the specifications and regulations for safety and EMC defined in this chapter.

9.1 Important Safety Information

Only a technically qualified person should access, integrate, configure, and service this product.

9.2 Intended Application Uses

This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other Product Categories and Environments (such as medical, industrial, alarm systems, and test equipment), other than an ITE application, may require further evaluation.

9.3 Product Safety

Argentina	Resolution S.I.C.M No. 92/98
Australia / New Zealand	AS/NZS 3562
Canada / USA	UL60 950 – CSA60 950
China	GB4943-1995
European Union	EN60 950 & 73/23/EEC
Germany	EN60 950
International	IEC 60 950, 3rd Edition
Nordics	EMKO-TSE (74-SEC) 207/94
Russia	GOST-R 50377-92

9.4 Electromagnetic Compatibility (EMC) - Emissions

Australia / New Zealand	AS/NZS 3548 (Class A)
Canada	ICES-003 (Class A)
China	GB9254-1998
European Union	EN55022: 1994 (Class A) & 89/336/EEC
International	CISPR 22, 3rd Edition (Class A)
Japan	VCCI (Class A)
Korea	MIC Notice 1997-42 (Class A)
Russia	GOST-R 29216-91 (Class A)
Taiwan	BSMI CNS13438
USA	Title 47 CFR, Part 15 (Class A)

9.5 Electromagnetic Compatibility - Immunity

China	GB9254-1998
European Union	EN55024: 1998
International	CISPR 24: 1st Edition
Korea	MIC Notice 1997-41
Russia	GOST-R 50628-95

9.6 Power Line Harmonics / Voltage Flicker

China	GB17625.1-1998
European Union	EN61000-3-2 / EN61000-3-3
International	IEC61000-3-2
Japan	JEIDA

9.7 Product Regulatory Compliance Markings

Table 67. Product Regulatory Compliance Markings

Country	Markings on Product or Packaging	Marking Description
Australia / New Zealand	N232	EMC Compliance Mark. Note : As shown indicates that the compliance folder is held in Australia
China		CCC EMC & Safety Compliance Marking
	声明 此为 A 级产品，在生活环境中，该产品可能会造成无线电干擾。 在这種情況下，可能需要用戶对其干擾采取可行的措施。	EMC Class A Warning
Canada	c UL us	System Compliance Safety Mark (same for USA)
	CANADA ICES-003 CLASS A	EMC Compliance Mark
European Union / Nordics	CE	Declaration of Conformity Mark
Germany	Nemko GS geprüfte Sicherheit	System Safety Compliance Mark
Japan	この装置は、クラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。VCCI-A	EMC Compliance Mark – Class A
Korea	MIC	EMC Compliance Mark
Russia		Safety & EMC Compliance Mark
Taiwan	R33025	BSMI Certification NumberRPC Marking
	警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策	BSMI EMC Warning for Class A Devices

Country	Markings on Product or Packaging	Marking Description
USA		System Compliance Safety Mark (same for Canada)
	This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation. Manufactured by Intel Corporation	EMC Compliance Marking Statement – Class A Products

9.8 Regional EMC Compliance Notices / Information

Table 68. Regional EMC Compliance Information

Country	Compliance Information
USA	**FCC Verification Notice (Class A)** This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. For questions related to the EMC performance of this product, contact: Intel Corporation 5200 N.E. Elam Young Parkway Hillsboro, OR 97124 1-800-628-8686 This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are NOT designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: Reorient or relocate the receiving antenna. Increase the separation between the equipment and the receiver. Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected. Consult the dealer or an experienced radio/TV technician for help.
CANADA	**INDUSTRY CANADA (Class A)** This Class A digital apparatus complies with Canadian ICES-003. Cet appereil numérique de la classe A est conforme à la norme NMB-003 du Canada.
CHINA	声明 此为 A 级产品，在生活环境中，该产品可能会造成无线电干擾。 在这種情況下，可能需要用戶对其干擾采取可行的措施。
EUROPE	**CE Declaration of Conformity** This product has been tested in accordance to, and complies with the European Low Voltage Directive (73/23/EEC) and European EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

Country	Compliance Information
JAPAN	**VCCI (Class A)** この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。 English translation of the notice above is as follow: This is a Class A product based on the standard of the Voluntary Control Council For Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.
TAIWAN	**BSMI Certification Information** The following BSMI Certification information is marked on the product R33025 BSMI EMC Class A Warning 警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策
KOREA	**RRL Certification Information** MIC 1. 기기의 명칭(모델명) : 2. 인증번호 : 3. 인증받은 자의 상호 : 4. 제조년월일: 5. 제조자/제조국가 : The English translation for the above is as follows: 1. Type of Equipment (Model Name): SR870BH2 2. Certification No.: Contact Intel representative. 3. Name of Certification Recipient: Intel Corporation. 4. Date of Manufacturer: Refer to date code on product. 5. Manufacturer / Nation: Intel / Refer to manufacturing label on product.

Appendix A: Glossary

Word / Acronym	Definition
ACPI	Advanced Configuration and Power Interface
ANSI	American National Standards Institute
ASL	ACPI Source Language
BIOS	Basic Input / Output System
BMC	Baseboard Management Controller
CE	Community European
CISPR	International Special Committee on Radio Interference
CMOS	Complementary Metal-Oxide Semi-Conductor
COM	Communications
CPD	Component Data Sheets
CRU	Customer Replaceable Unit
CSA	Canadian Standards Organization
D2D	DC-to-DC converter
DB	Data Bus
dBA	deciBel Acoustic
DDR	Double Data Rate
DIMM	Dual In-Line Memory Module
DMA	Direct Memory Access
DPC	Direct Platform Control
DPS	Distributed Power Supply
DSS	Decision Support System
DT	Double Transition
ECC	Error Checking and Correcting
EEPROM	Electrically Erasable Programmable ROM
EMI	Electromagnetic Interference
EMP	Emergency Management Port
EPS	External Product Specification
ESD	Electro Static Discharge
FCC	Federal Communications Commission
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
FWH	Firmware Hub
GND	Ground
GUI	Graphical User Interface
HDD	Hard Disk Drive
HDM	High Density Metric
HL	Hub-Link
HPC	High Pin Count
HPIB	Hot-Plug Indicator Board
HSC	Hot Swap Controller

Word / Acronym	Definition
I/O	Input / Output
IC	Integrated Circuit
ICH2	I/O Control Hub 2
ICMB	Intelligent Chassis Management Bus
IDE	Integrated Device Electronics
IEC	International Electrotechnical Commission
IMB	Intelligent Management Bus
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
ISA	Industry Standard Architecture
ISP	In System Programmable
ITE	Information Technology Equipment
ITP	In-Target Probe
JAE	Japan Aviation Electronics
JTAG	Joint Test Action Group
LAN	Local Area Network
LED	Light Emitting Diode
LPC	Low Pin Count
LVDS	Low Voltage Differential SCSI
MRH-D	Memory Repeater Hub – DDR
MTBF	Mean Time Between Failures
NIC	Network Interface Card
OEM	Original Equipment Manufacturer
OLTP	On-line Transaction Processing
OS	Operating System
OTP	Over-Temperature Protection
OVP	Over-Voltage Protection
PAL	Programmable Array Logic
PCI	Peripheral Component Interconnect
PDB	Power Distribution Board
PEF	Platform Event Filtering
PEP	Platform Event Paging
PFC	Power Factor Correction
PIROM	Processor Information ROM
PLD	Programmable Logic Device
PSU	Power Supply Unit
PVC	Poly Vinyl Chloride – a plastic
PWM	Pulse Width Modulator
RAID	Redundant Array of Independent Disks
RAS	Reliability, Availability and Serviceability
RH	Relative Humidity
RPM	Revolutions Per Minute
SAF-TE	SCSI Accessed Fault-Tolerant Enclosure
SCA	Single Connector Attachment

Word / Acronym	Definition
SCL	Serial Clock
SCSI	Small Computer Systems Interface
SDA	Serial Data
SDINT	System Diagnostic Interrupt
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic RAM
SE	Single Ended
SEEPROM	Serial Electrically Erasable Programmable Read Only Memory
SEL	System Event Log
SIOH	Server I/O Hub
SMB	Server Management Bus
SMP	Symmetric Multiprocessing
SNC-M	Scalable Node Controller
SSI	Server System Infrastructure
TPS	Technical Product Specification
TTL	Transistor-Transistor Logic
USB	Universal Serial Bus
UV	Under-Voltage
VAC	Alternating current (AC) voltage
VCC	Voltage Controlled Current
VCCI	Voluntary Control Council for Interference by Information Technology Equipment
VGA	Video Graphics Array
VID	Voltage ID
VSB	Voltage StandBy
WfM	Wired For Management
ZIF	Zero Insertion Force

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Appendix B: Reference Documents

Refer to the following documents for additional information:

- *SR870BH2 Hardware & Operating System Validation List*
- *Emergency Management Port Interface External Product Summary*, Intel Corporation.
- Small Form Factor-8046.

ACPI

- *Advanced Configuration And Power Interface Specification*, http://www.teleport.com/~acpi/.

BIOS

- *El Torito CD-ROM Boot Specification*, Version1.0.
- *System Management BIOS Reference Specification*, Version 2.3.1, http://developer.intel.com/ial/WfM/wfm20/design/BIBLIOG.HTM.
- *POST Memory Manager Specification*, Version 1.01.
- *Plug and Play BIOS Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.
- *Clarification to Plug and Play BIOS Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

DDR SDRAM

- *DDR SDRAM Registered DIMM Design Specification*, May 2000.
- *Double Data Rate (DDR) SDRAM Specification*, JEDEC Standard No. 79, June 2000, http://www.jedec.org/.
- *Intel DDR 200 JEDEC Specification Addendum*, Revision 0.85, May 19, 2000, Intel Corporation.

Ethernet

- *RS-82550EY Fast Ethernet Multifunction PCI/CardBus Controller Product Preview Datasheet*, Intel Corporation.

I_2O

- *Intelligent I/O (I2O) Architecture Specification*, Version 2.0, March 1999, I2O Special Interest Group, http://www.intelligent-io.com/.

MPS

- *MultiProcessor Specification*, Version 1.4, Intel Corporation, http://www-techdoc.intel.com/design/intarch/manuals/242016.htm.

PCI

- *PCI Bus Power Management Interface Specification*, Revision 1.1, PCI Special Interest Group, http://www.pcisig.com/.
- *PCI Local Bus Specification*, Revision 2.2, PCI Special Interest Group, http://www.pcisig.com/.

Regulatory

- *UL1950/CSA 950: Safety of Information Technology Equipment*, 3rd Edition.
- *IEC 60950: Safety of Information Technology Equipment*, 3rd Edition.
- *EN 60950: Safety of Information Technology Equipment*, 2nd edition plus A1-A4.
- *EN55022: Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment.*
- *EN55024: Information Technology Equipment - Immunity Characteristics Limits and Methods of Measurement*.
- *EN61000-4-2: ESD Immunity*.
- *EN61000-4-3: Radiated Fields Immunity*.
- *EN61000-4-4: Electrical Fast Transients/Bursts*.
- *EN61000-4-5: AC Surge Immunity*.
- *EN61000-4-6: RF Conducted Immunity*.
- *EN61000-4-8: Power Frequency Magnetic Fields*.
- *EN61000-4-11: Voltage Fluctuations and Short Interrupts*.
- *EN61000-3-3: Voltage Flicker*.
- *CISPR 22: Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment*, 2nd Edition.
- *CFR 47: Federal Communications Commission (FCC) Compliance with the Class A Limits for Computing Devices (FCC Mark)*, Part 2 & 15.

- *ANSI C63.4: American National Standard for Methods of Measurement of Radio-Noise Emissions from Low Voltage Electronic Equipment in the Range of 9kHz to 40GHz for EMI Testing*, 1992.
- *ICES-003: Canadian Radio Interference Regulations for Digital Apparatus*.
- *EN 61000-3-2: Electromagnetic Compatibility (EMC)* Part 3: Limits - Section 2: Limits for Harmonic Current Emissions.
- *JEIDA MITI Guideline for Suppression of High Harmonics in Appliances and General-Use Equipment*.

SCSI

- *SCSI Parallel Interface - 4 (SPI-4)*, Project Number: 1365-D, Project Phase: Development, Rev. 03, T10 Technical Committee, http://www.t10.org/.
- *QLogic Corporation: ISP12160A/33 and ISP12160A/66 Intelligent, Dual SCSI Processors Datasheet*, QLogic Corporation, March 22, 1999, 83216-580-01 A.
- *QLogic Corporation: ISP12160/12160A Intelligent, Dual SCSI Processors, Designer's Guide*, QLogic Corporation, June 18, 1999, 83216-508-00 A.
- *ISP12160B Intelligent, Dual SCSI Processors Designer's Guide*, ISBN 83216-508-00 B, February 21, 2000.
- *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification*, http://www.safte.org/.

Server Management

- *IPMI v1.5 Specification*, Draft 1, Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation, Adopter Review Release version - currently available for IPMI adopters and contributors review only. Targeted for publication in February 2001. http://developer.intel.com/design/servers/ipmi/spec.htm.
- *Intelligent Platform Management Interface Specification*, Version 1.0, August 26, 1999, Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation, http://developer.intel.com/design/servers/ipmi/spec.htm.
- *Addenda, Errata, and Clarifications, Intelligent Platform Management Interface Specification*, Version 1.0, Revision 1.1, Addendum Document Revision 3, June 6, 2000, Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation, http://developer.intel.com/design/servers/ipmi/spec.htm.
- *Intelligent Platform Management Bus (IPMB) Communications Protocol Specification*, Version1.0, Revision 1.0, September 16, 1998, Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation, http://developer.intel.com/design/servers/ipmi/spec.htm.
- *Intelligent Chassis Management Bus (ICMB) Bridge Specification*, Version 1.0, Revision 1.2, May 11, 2000, Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation, http://developer.intel.com/design/servers/ipmi/spec.htm.
- *Platform Event Trap Format Specification*, December 7, 1998, http://developer.intel.com/design/servers/ipmi/spec.htm.

- *IPMB v1.0 Address Allocation*, Version 1.0, September 16, 1998, Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation, http://developer.intel.com/design/servers/ipmi/spec.htm.
- *IPMI Platform Management Information Storage Definition*, Version 1.0, September 27, 1999, Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation, http://developer.intel.com/design/servers/ipmi/spec.htm.

Super I/O

- *SMSC LPC47B27x: 100 Pin Enhanced Super I/O Controller with LPC Interface for Consumer Applications*, http://www.smsc.com/.

USB

- *Universal Serial Bus Specification*, http://www.usb.org/developers.

VGA

- *ATI RAGE™ XL Graphics Controller Specifications - Technical Reference Manual*, rev 2.03, ATI Technologies Inc., 2000, http://www.ati.com/.

Wired for Management

- *Wired for Management (WfM) Baseline Specifications*, Version 2.0, Intel Corporation, http://developer.intel.com/ial/wfm/wfmspecs.htm.

Windows

- *Hardware Design Guide Version 3.0 for Microsoft Windows 2000 Server*, Intel Corporation and Microsoft Corporation, June 30, 2000, http://www.microsoft.com/HWDEV/serverdg.htm.