SRPL8 MP Server System Board Set

Specification Update

Revision History

Date	Modifications
9/31/01	This document is the first Specification Update for the *Intel® SRPL8 MP Server System Board Set Technical Product Specification. See the SRPM8* Specification Update for previously published errata.
10/31/01	Monthly Update
2/8/02	Monthly update

Disclaimers

The SRPL8 MP Server System Board Set Server System may contain design defects or errors known as errata that may cause the product to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

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Preface

This document is an update to the specifications contained in the *SRPL8 MP Server System Board Set Technical Product Specification* (Order Number [TPS order number]). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain specification changes, specification clarifications, errata, and document changes.

Refer to the *Intel® Pentium₇ III Xeon™ Processor Specification Update* (Order Number 244460-021) for specification updates concerning the Pentium® Xeon™ III processor. Items contained in the *Pentium® III Xeon™ Processor Specification Update* that either do not apply to the [product] or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

- ?? **Specification Changes** are modifications to the current published specifications for the SBT2 server boards. These changes will be incorporated in the next release of the specifications.

- ?? **Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

- ?? **Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

- ?? **Errata** are design defects or errors. Errata may cause the SBT2 server board's behavior to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.

Table 1: Glossary

Word / Acronym	Definition
AC	Alternating current
BIOS	Basic Input/Output System
CPU	Central processing unit
DC	Direct current
DOS	Disk operating systme
EISA	Extended ISA
ESG	Enterprise Server Group
I/O	Input/output
ISA	Industry standard architecture

Word / Acronym	Definition
JTAG	Joint Test Action Group
MAC	Memory access controller
MHz	Megahertz
MP	Multiprocessor
OS	Operating system
PB64	PCI host bridge hot-plug controller
PBA	Printed board assembly
PCI	Peripheral component interconnect
PHP	PCI hot plug
PMD	Performance Microprocessor Division
POST	Power-on Self Test
RAM	Random access memory
ROM	Read-only memory
SEL	System event log
SMI	Server management interrupt
SMM	Server management mode
V	Volts
VRM	Voltage regulator module

General Information

For a complete revision history of system and board set level components, refer to the most recent Monthly Conversion Summary document for the SRPL8 and SRPL8 products. Basic SRPL8 MP server board set identification information is shown in the Table 2.

Table 2: Basic SRPL8 MP Server System Board Set Identification Information

Component (Module) Description	Base PBA Number	PBA Revision Number	Fab Rev	Released BIOS/SSU/ Firmware Revision	Suggested BIOS/SSU/ Firmware Revision	Notes (See below)
Profusion* Carrier	736365	403	4.0	VMC0.9		
Mezzanine Board	753356	300	3.0			MM# 829179
I/O Baseboard	753695	305	3.0	BIOS PR3, BMC 26, SMIC 86, SDR 27	BIOS PR3, BMC 26, SMIC 86, SDR 27	MM# 829177
Memory Board	714518	204	2.0			
PCI Hot-plug LED Board	731027	002	1.4			
I/O Riser Card	679267	201	3.0			
Midplane	704130	405	4.0			
Front Panel	703106	301	3.0	FPC 19	FPC 19	
Power Supply	676912	008	1.8			
PCI Hot-plug LED Board	731027	002	1.4			Fab spin to change switch from mechanical to magnetic
Cascades Upgrade Kit: Mezzanine Board Memory Board	831860	NA	NA			Also includes 1mb CCF modules front bezel and more

The Enterprise Server Group (ESG) supports the Performance Microprocessor Division's (PMD) position on mixed steppings in MP systems; however, please note that you can not mix processors with cache steppings requiring different voltages in the same system. The SRPL8 system architecture implements one voltage regulator module (VRM) to supply the same voltage to the cache core of two processors.

Table 3 indicates which stepping of the Pentium® III Xeon？ processor can be mixed within the same system. An "X" denotes which stepping can be mixed and a blank indicates the SRPM8 MP server board set does not support the given BIOS/stepping combination. NS indicates that processors with that S-Spec number are not supported in the SRPL8 server system.

Table 3: Supported Pentium® III Xeon™ Processor/BIOS Combinations

PROCESSOR STEPPING	A0	A0'	A1	B0	A0	A0'	A1	A1	B0	B0
FREQUENCY	700MHz	700MHz	700MHz	700MHz	700MHz	700MHz	700MHz	700MHz	700MHz	900MHz
CACHE SIZE	1M	1M	1M	1M	2M	2M	2M	2M	2M	2M
STEPPING ID										
S-SPEC	SL3U5	SL4GE	SL49Q	TBD	SL3X2	SL4GG	SL49S	SL49W	TBD	SL4XZ
SL3U5	X		X	X						
SL4GE		X	X	X						
SL49Q	X	X	X	X						
TBD	X	X	X	X						
SL3X2					X		X	X	X	
SL4GG						X	X	X	X	
SL49S					X	X	X	X	X	
SL49W					X	X	X	X	X	
TBD					X	X	X	X	X	
TBD										X
BIOS										**PR2/3**
PRODUCTION RELEASE 1	x	x	x		x	x	x	x	x	x
PRODUCTION RELEASE 2	x	x	x		x	x	x	x	x	x
PRODUCTION RELEASE 3	x	x	x		x	x	x	x	x	x

Speed jumpers should be removed for 900 MHz processors. Use autodetect only.

Summary Tables of Changes

The following tables indicate the errata and the document dhanges that apply to the SRPL8 MP Server System Board Set. Intel intends to fix some of the errata in a future stepping of components, and to account for the other outstanding issues through documentation or specification changes as noted. The tables use the following notations:

Doc: Intel intends to update the appropriate documentation in a future revision.

Fix: Intel intends to fix this erratum in a future release of the component.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

Shaded: This erratum is either new or has been modified from the previous specification update.

Table 4. Errata Summary

No.	Plans	Description of Errata
1.	Fixed	BIOS PR1 requires CCF's in system for proper system operation
2.	Fixed	Reversed silkscreen and diode on I/O baseboard prevent 3.3 Volt standby on PCI bus from functioning
3.	Fix	Possible Blue screen on Windows 2000 after updating from BIOS 2 to BIOS 3
4.	No Fix	256 MB of Physical Memory Appears to Be Missing When 4 GB of Memory Is Installed
5.		

Table 5. Documentation Changes

No.	Plans	Description of Documentation Change
1.	Fix	Quick Start Guide processor changes
2.		
3.		
4.		
5.		

Following are in-depth descriptions of each erratum / documentation change indicated in the tables above. The errata and docmentation change numbers below correspond to the numbers in the tables.

Errata

1. BIOS Production Release 1 requires Cache Coherency Filters for proper system operation.

2. Reversed silkscreen and diode on I/O baseboard prevent 3.3 Volt standby on PCI bus from functioning. Intel Engineering discovered this issue in a routine design review and we have had no reports of any issues related to this from the field. 3.3 Volt standby to the PCI bus is required for PCI 2.2 compliance, including support of Wake-On-LAN via the Power Management Event signal with no WOL cable attached.

3. Updating the system BIOS from PR2 to PR3 when running Windows 2000 requires Qlogic SCSI driver 7.20 or later. This change was for Microsoft WHQL certification and incorporates a new Subsystem Vendor ID for the Qlogic part. The published procedure to upgrade the system when running Windows 2000 is as follows: From Windows 2000 go to the device manager screen and select the Qlogic SCSI device. Select update driver and use the 7.20 version of the driver or later version if available. Once the driver update is complete; shutdown Windows and reboot the system. Flash the BIOS from PR2 to PR3. Windows will load and continue to function. If the NVRAM on the onboard Qlogic SCSI is cleared and defaults are loaded the system will not boot Windows. At this point there are only two options: 1. Step the system back to BIOS PR2. 2. Re-install Windows 2000. We are investigating a fix for this condition.

4. If you are using a computer that has over 4 gigabytes (GB) of memory installed, System properties, Microsoft System Diagnostics (WinMSD) or other system utilities report a memory value that is 256 megabytes (MB) less than the total physical memory that is installed. This issue can occur if a server is using the Intel Profusion chipset. In the read-only (ROM) memory of the computer, the upper 256-MB memory region is reserved for memory-mapped input/output (I/O) devices. The amount of reserved physical memory may increase to 512 MB or more depending on the number of I/O devices that are installed on the computer. Typically, a computer that has 4 gigabytes (GB) of actual physical memory looks as if it has 3.84 GB of total physical memory.   This behavior is by design.

5.

Documentation Changes

1.